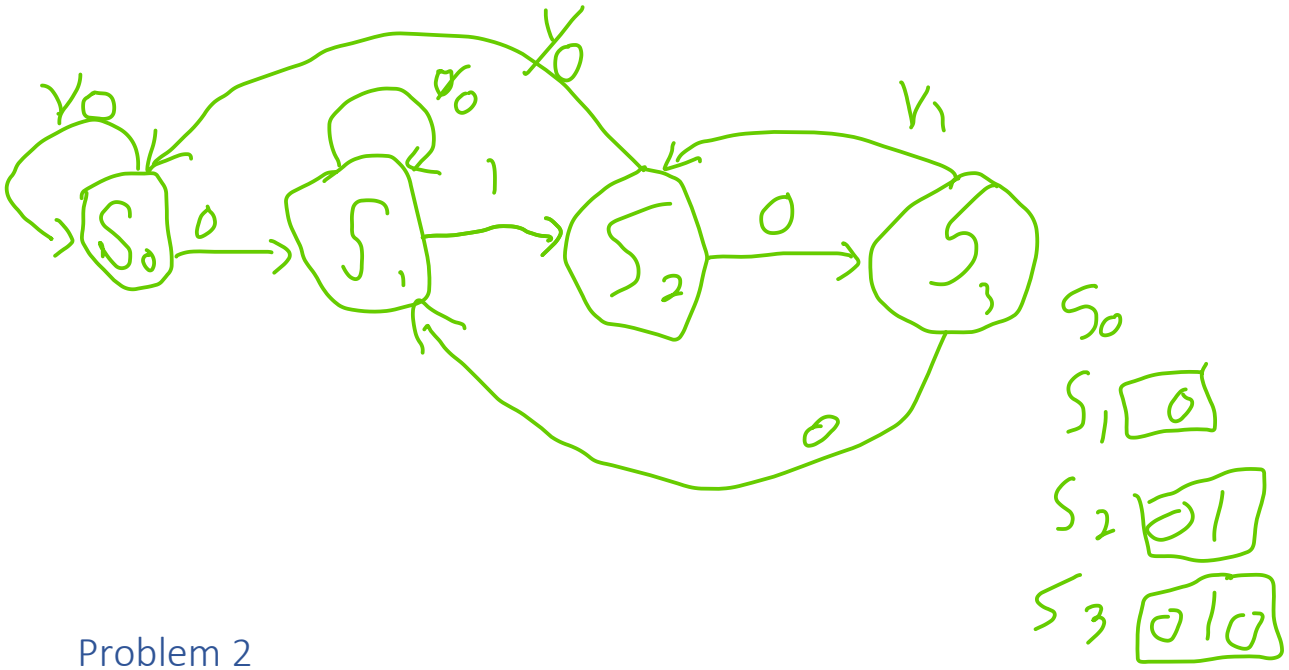
Haegang Yang

Homework 10

- All homework must be turned in on PDF format. This can be scanned or typed in any paper size, but the format must be PDF and the file must be readable. This document can be modified for your homework submission. An additional homework template is available on Canvas to assist you in creating your answers, and content from lecture notes can be used.
- All final answers must be circled or in green.
- All homework must have a name on the top of **every** page.
- Submission errors (not in PDF, illegible, etc.) will not be re-graded.

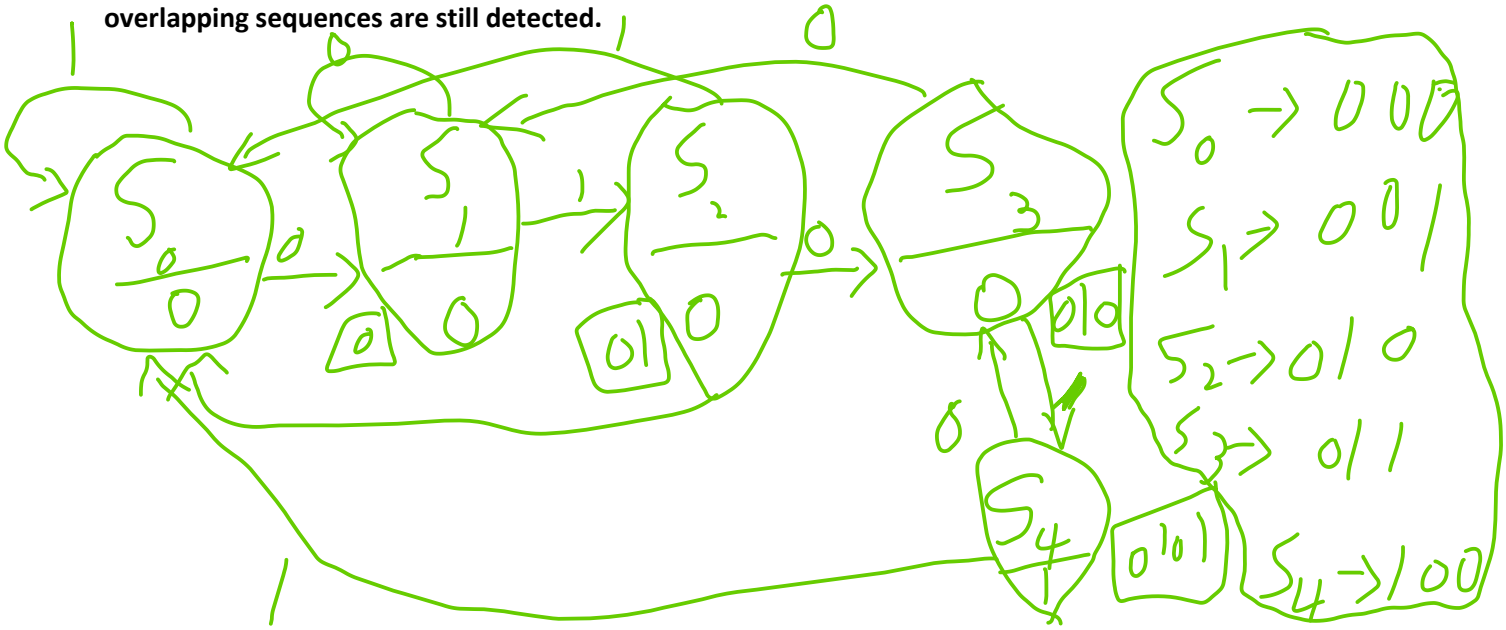
Problem 1

Create a state diagram which detects the input sequence "0->1->0->1". Overlapping sequences are detected. The output changes immediately upon detecting the sequence.



Problem 2

Repeat the previous problem, except have the output remains high for an entire clock cycle. **NOTE: overlapping sequences are still detected.**



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Problem 3

Given your answers for the previous two problems, describe one benefit and one disadvantage of the FSM made using the diagram from Problem 1.

The states in problem 1 are less and the output comes fast when the sequence detects. In the design, output makes asynchronously while the state changes synchronous to clock.

Problem 4

Create a timing diagram for the above two circuits (on the same timing diagram plot with two outputs). In this timing diagram, the machine is made with falling-edge triggered flip-flops, and the machine starts in the “0” state. The values x = 0110101011 are captured at the falling edge of the clock, but inputs and the clock never change at the same time. The machine output and current state must be in the diagram, but other signals are allowed.