

Homework 6

- All homework must be turned in on PDF format. This can be scanned or typed in any paper size, but the format must be PDF and the file must be readable. This document can be modified for your homework submission. An additional homework template is available on Canvas to assist you in creating your answers, and content from lecture notes can be used.
- All final answers must be circled or in green.
- All homework must have a name on the top of **every** page.
- Submission errors (not in PDF, illegible, etc.) will not be re-graded.

Problem 1 (2 pts)

Make the following equation using the minimum number of NAND gates

$$f(a, b, c, d) = \prod M(1, 3, 4, 9, 14) \cdot D(0, 2, 5, 6, 8, 11, 12)$$

Handwritten solution for Problem 1:

Given function: $f(a, b, c, d) = \prod M(1, 3, 4, 9, 14) \cdot D(0, 2, 5, 6, 8, 11, 12)$

Karnaugh Map (K-map) for $f(a, b, c, d)$:

| cd \ ab | 00 | 01 | 11 | 10 |
|---------|----|----|----|----|
| 00 | 1 | 1 | 1 | 1 |
| 01 | 1 | 1 | 1 | 1 |
| 11 | 1 | 1 | 1 | 1 |
| 10 | 1 | 1 | 1 | 1 |

Grouping the 1s in the K-map, the simplified expression is:

$$f(a, b, c, d) = \overline{b} + \overline{c} + \overline{d}$$

Implementation using NAND gates:

First, implement \overline{b} , \overline{c} , and \overline{d} using NAND gates with one input tied to 1 (or $\overline{b} = \overline{b \cdot 1}$, etc.).

Then, implement the OR operation using NAND gates:

$$\overline{b} + \overline{c} + \overline{d} = \overline{\overline{\overline{b} + \overline{c}} \cdot \overline{\overline{b} + \overline{c}} \cdot \overline{\overline{b} + \overline{c}}}$$

The final circuit uses 6 NAND gates: 3 for the individual complements and 3 for the OR operation.

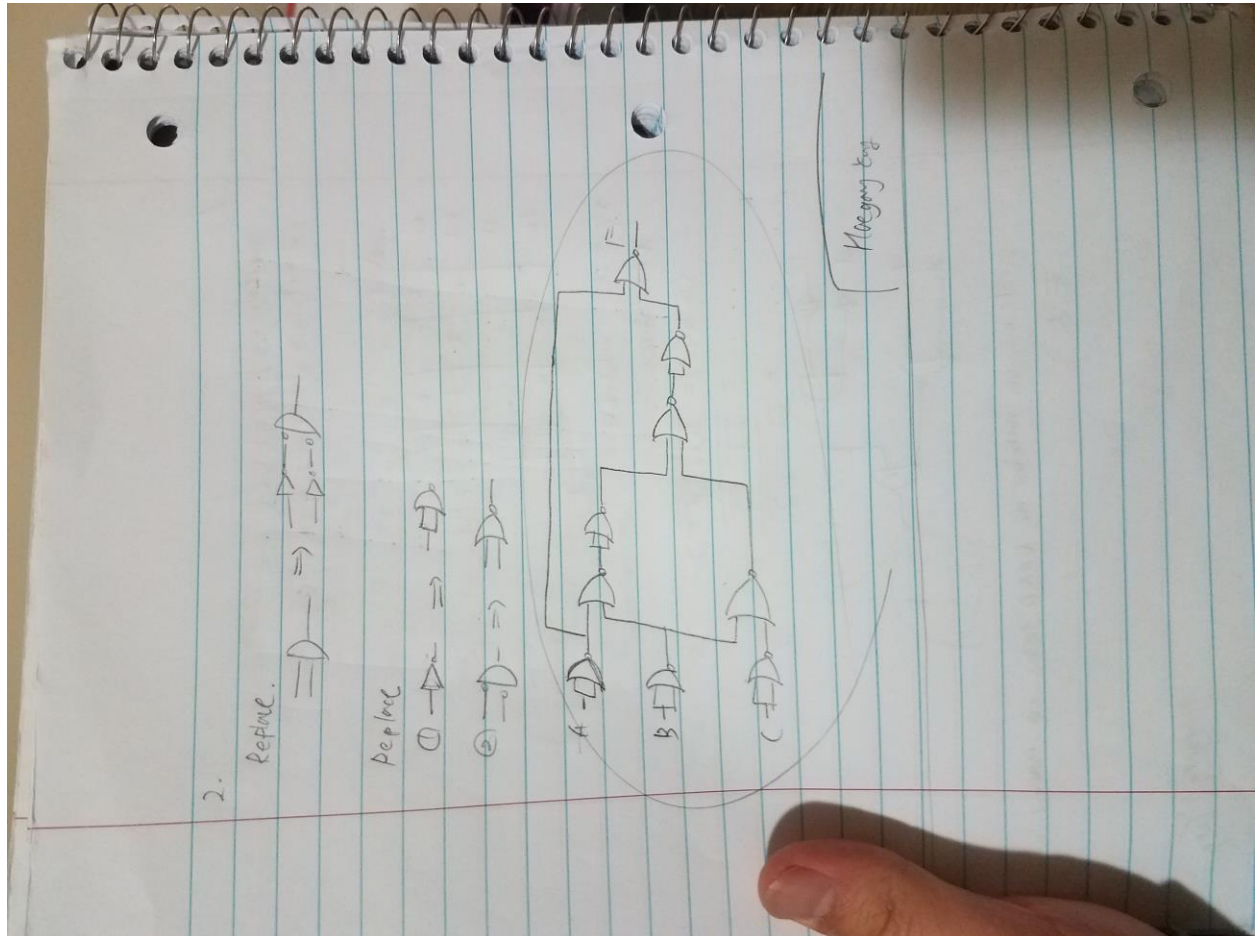
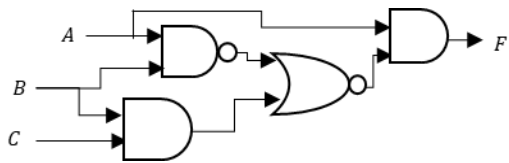
Minimum number of NAND gates required: 6

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Problem 2 (2 pts)

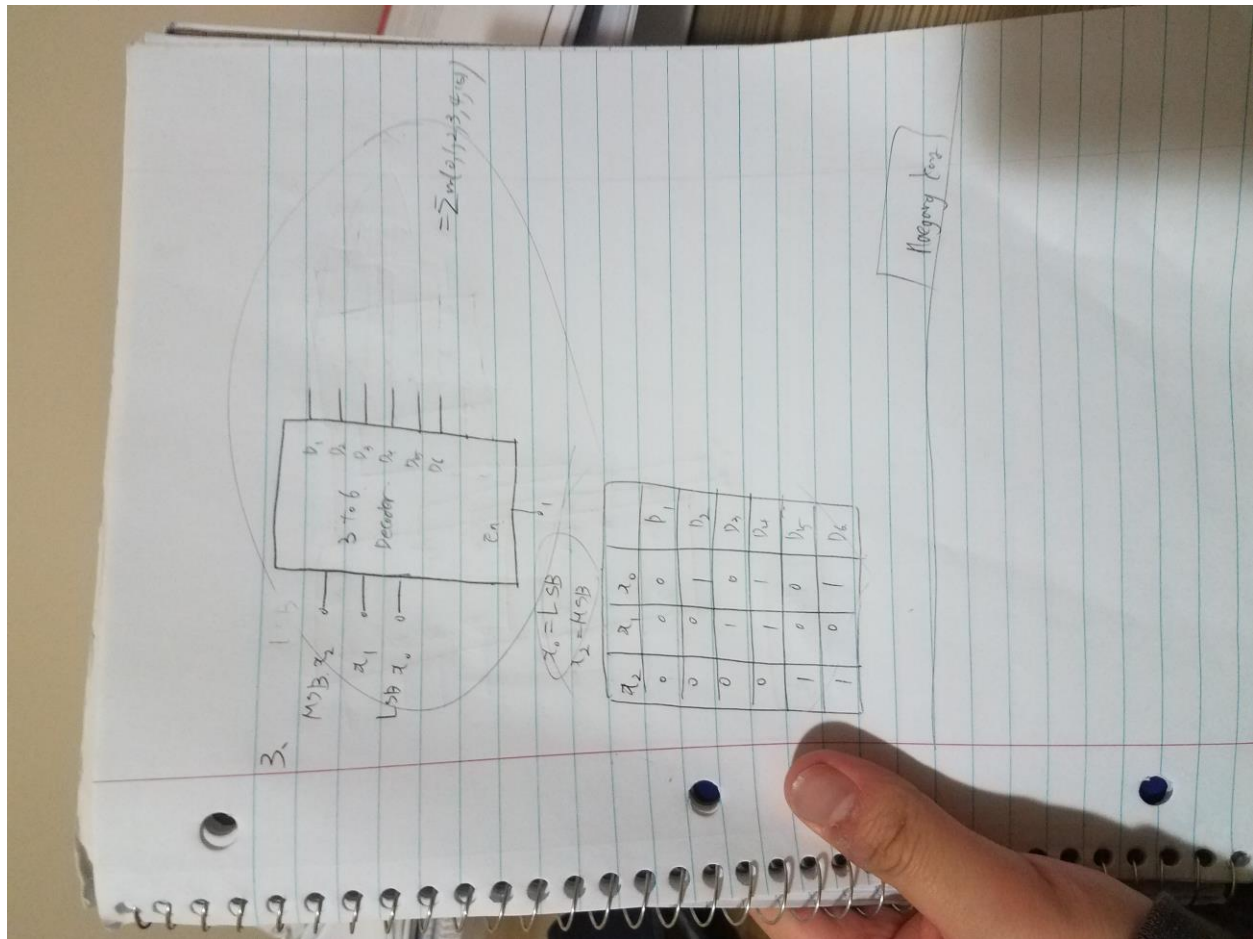
Convert the following circuit into one using only NOR gates (and no inverters). Do not optimize the circuit except for the number of "inverters".

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Problem 3 (2 pts)

Create a 3-to-6 active-low decoder with an active-high enable. Name your inputs $\{x_2, x_1, x_0\}$ (with x_0 as the LSB).



Problem 4 (4 pts)

Design a 3-to-8 active-low decoder using only 2-to-4 active-low decoder modules. No other gate types or modules may be used (you may use constant values). Assume that each 2-to-4 decoder has one active-low enable input, E.

