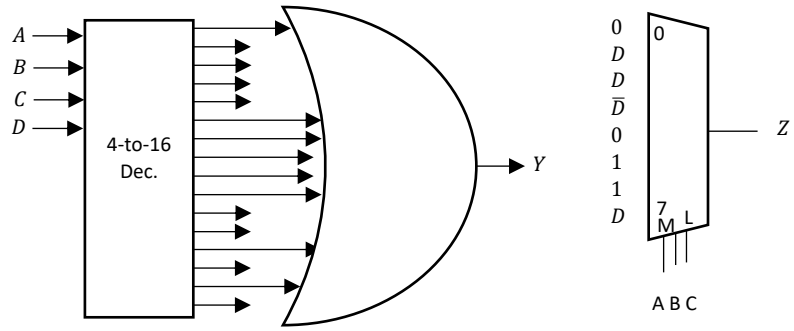
Haegang Yang

Homework 8

- All homework must be turned in on PDF format. This can be scanned or typed in any paper size, but the format must be PDF and the file must be readable. This document can be modified for your homework submission. An additional homework template is available on Canvas to assist you in creating your answers, and content from lecture notes can be used.
- All final answers must be circled or in green.
- All homework must have a name on the top of **every** page.
- Submission errors (not in PDF, illegible, etc.) will not be re-graded.

Problem 1

For the following circuit, complete the given timing diagram (you may insert additional rows, but rows corresponding to outputs must be completed).



A

B

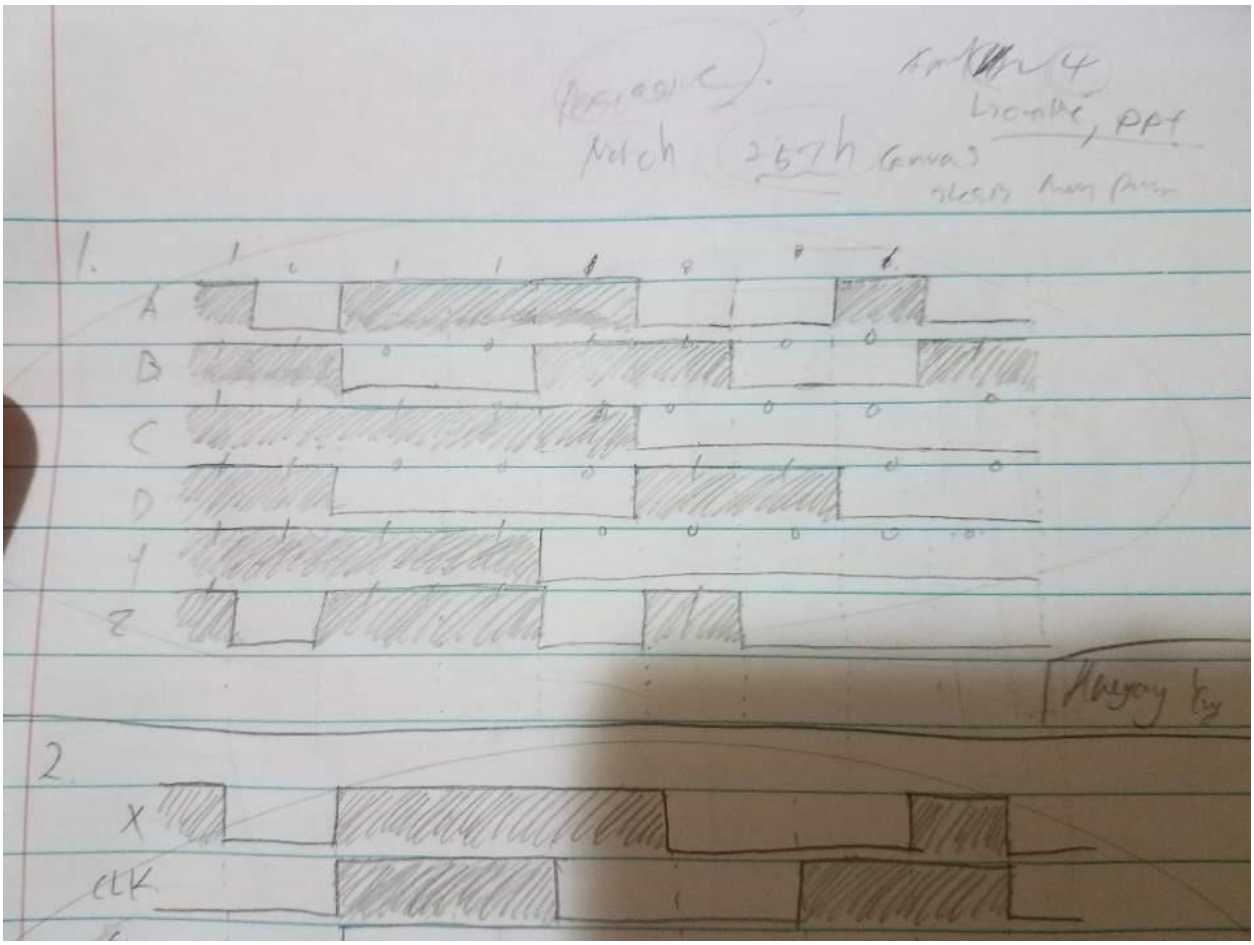
C

D

Y

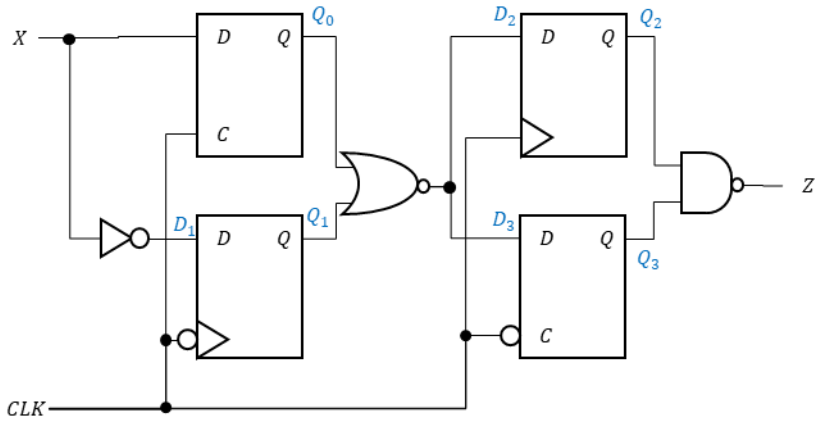
Z

Haegang Yang

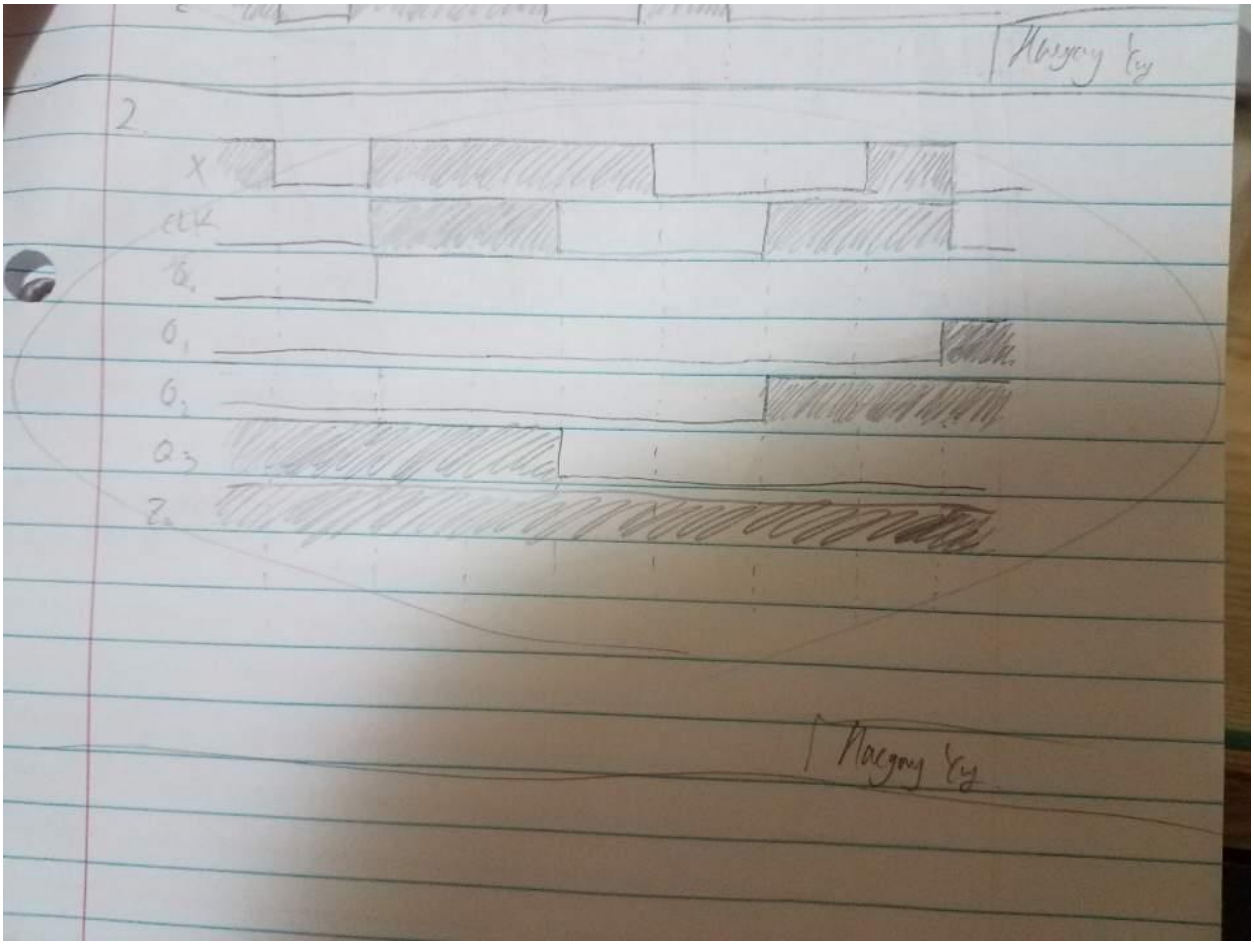


Problem 2

For the following circuit, complete the given timing diagram. You may insert additional rows if desired, but blank rows given must be completed.



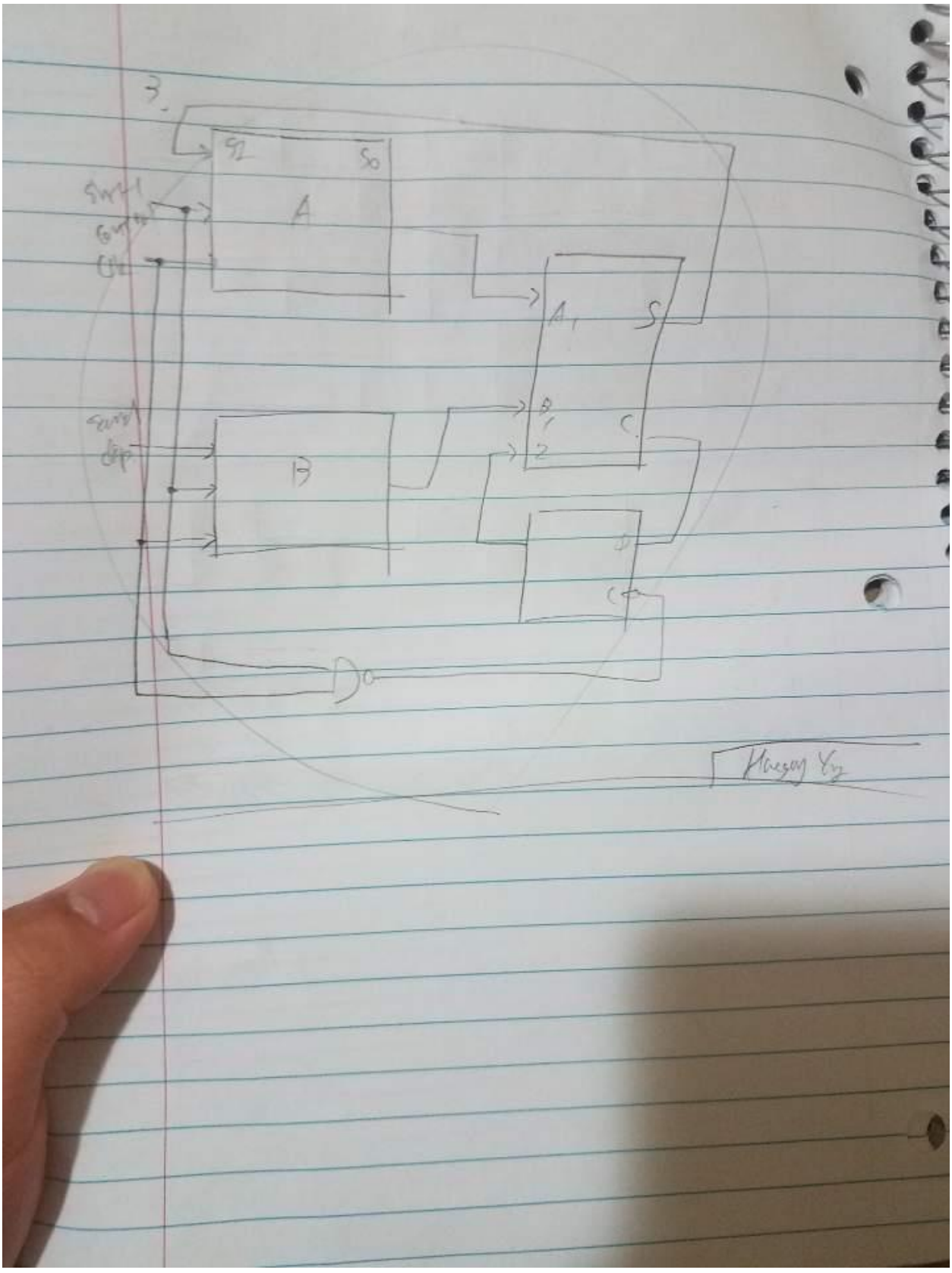
Haegang Yang



Problem 3

Create a 2-bit serial adder: this adder adds $A_{1,0}$ and $B_{1,0}$ and provides the sum, $S_{1,0}$. At the negative edge of an input clock, Clk, the carry-out from a given summation is captured and provided to the next $A_{1,0}$ and $B_{1,0}$ to be added.

Haegang Yang



Haegang Yang

Problem 4

Using only NAND gates and NOT gates, create a negative-edge-triggered delay flip-flop.

Haegang Yang