# –36-V, –1-A, Ultralow-Noise Negative Voltage Regulator

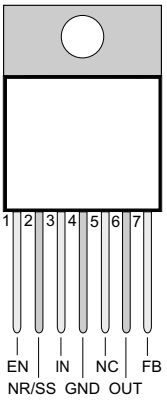
## FEATURES

- **Input Voltage Range: –3 V to –36 V**
- **Noise:**
  - **16 $\mu V_{RMS}$ (10 Hz to 100 kHz)**
- **Power-Supply Ripple Rejection:**
  - **72 dB (10 kHz)**
- **Adjustable Output: –1.18 V to –33 V**
- **Maximum Output Current: 1 A**
- **Stable with Ceramic Capacitors ≥ 10 µF**
- **Built-In Current-Limit and Thermal Shutdown Protection**
- **Available in an External Heatsink-Capable, High Thermal Performance TO-220 Package**
- **Operating Temperature Range: –40°C to +125°C**

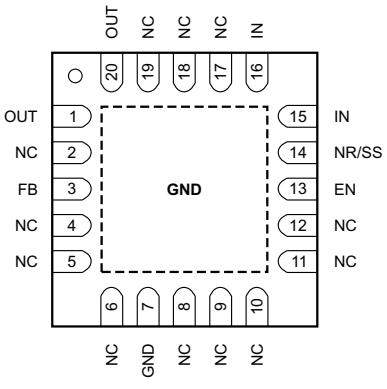
## APPLICATIONS

- **Supply Rails for Op Amps, DACs, ADCs, and Other High-Precision Analog Circuitry**
- **Audio**
- **Post DC/DC Converter Regulation and Ripple Filtering**
- **Test and Measurement**
- **Medical**
- **Industrial Instrumentation**
- **Base Stations and Telecom Infrastructure**
- **12-V and 24-V Industrial Buses**

KC PACKAGE
TO-220-7
(Top View)




RGW PACKAGE
5-mm × 5-mm QFN-20
(Top View)




**NOTE: RGW package is product preview.**

## DESCRIPTION

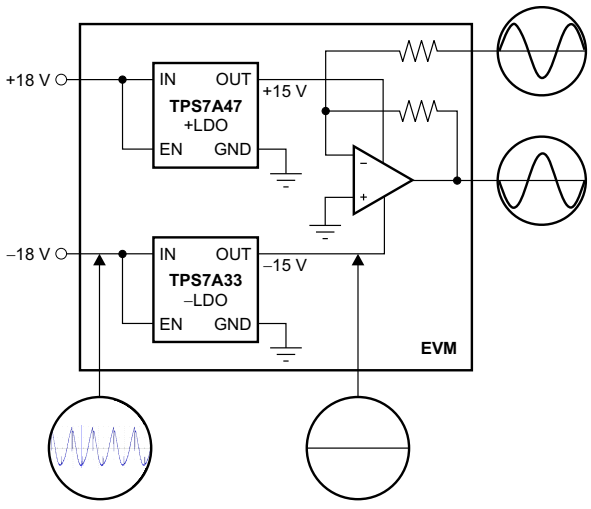
The TPS7A33 series of linear regulators are negative voltage (–36 V), ultralow-noise (16 $\mu V_{RMS}$, 72 dB PSRR) linear regulators capable of sourcing a maximum load of 1 A.

The TPS7A33 series include a complementary metal oxide semiconductor (CMOS) logic-level-compatible enable pin (EN) to allow for user-customizable power management schemes. Other features available include built-in current limit and thermal shutdown features to protect the device and system during fault conditions.

The TPS7A33 family is designed using bipolar technology primarily for high-accuracy, high-precision instrumentation applications, where clean voltage rails are critical to maximize system performance. This feature makes it ideal to power operational amplifiers, analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and other high-performance analog circuitry.

In addition, the TPS7A33 family of linear regulators is suitable for post dc-dc converter regulation. By filtering out the output voltage ripple inherent to dc-dc switching conversion, maximum system performance is ensured in sensitive instrumentation, medical, test and measurement, audio, and RF applications.

For applications where positive and negative high-performance rails are required, consider the TPS7A4700 positive high-voltage, ultra-low noise, low-dropout linear regulator as well.




**Typical Application: Post DC/DC Converter Regulation for High-Performance Analog Circuitry**

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ORDERING INFORMATION(1)

| PRODUCT | $V_{OUT}$ |
|---|---|
| TPS7A33**xxyyyz** | **XX** is nominal output voltage (01 = Adjustable).(2)<br>**YYY** is package designator.<br>**Z** is package quantity. |

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.
(2) For fixed –1.2-V operation, tie FB to OUT.

## ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range –40°C ≤ $T_J$ ≤ +125°C, unless otherwise noted.

| | | VALUE | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| Voltage | IN pin to GND pin | –36 | +0.3 | V |
| | OUT pin to GND pin | –33 | +0.3 | V |
| | OUT pin to IN pin | –0.3 | +36 | V |
| | FB pin to GND pin | –2 | +0.3 | V |
| | FB pin to IN pin | –0.3 | +36 | V |
| | EN pin to GND pin | –36 | +10 | V |
| | NR/SS pin to IN pin | –0.3 | +36 | V |
| | NR/SS pin to GND pin | –2 | +0.3 | V |
| Current | Peak output | Internally limited | | |
| Temperature | Operating virtual junction, $T_J$, absolute maximum range (2) | –40 | +150 | °C |
| | Storage, $T_{stg}$ | –65 | +150 | °C |
| Electrostatic discharge rating | Human body model (HBM) | | 1 | kV |
| | Charged device model (CDM) | | 500 | V |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.
(2) No permanent damage will occur to the part operating within this range though electrical performance is not ensured outside the operating free-air temperature range.

## THERMAL INFORMATION

| THERMAL METRIC(1) | | TPS7A33 | | UNITS |
|---|---|---|---|---|
| | | KC (TO-220) | RGW (QFN)(2) | |
| | | 7 PINS | 20 PINS | |
| $\theta_{JA}$ | Junction-to-ambient thermal resistance | 31.2 | 30.5 | °C/W |
| $\theta_{JC(top)}$ | Junction-to-case(top) thermal resistance | 40.0 | 27.6 | |
| $\theta_{JB}$ | Junction-to-board thermal resistance | 17.4 | N/A | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 6.4 | 0.37 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 17.2 | 10.6 | |
| $\theta_{JC(bottom)}$ | Junction-to-case(bottom) thermal resistance | 0.8 | 4.1 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The RGW package is product preview.

## ELECTRICAL CHARACTERISTICS(1)

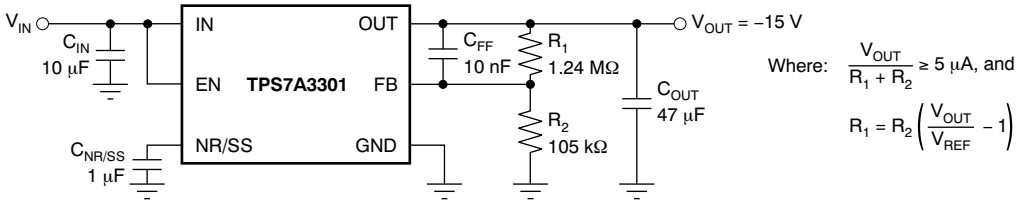
At –40°C ≤ $T_J$ ≤ +125°C, $|V_{IN}| = |V_{OUT(NOM)}| + 1.0$ V or $|V_{IN}| = 3.0$ V (whichever is greater), $V_{EN} = V_{IN}$, $I_{OUT}$ = 1 mA, $C_{IN}$ = 10 µF, $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 0 nF, and FB tied to OUT, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | TPS7A33 | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| $V_{IN}$ | Input voltage range | | –35.0 | | –3.0 | V |
| $V_{REF}$ | Internal reference | $T_J$ = +25°C, $V_{FB} = V_{REF}$ | –1.192 | –1.175 | –1.157 | V |
| $V_{UVLO}$ | Under-voltage lockout threshold | | | -2.0 | | V |
| $V_{OUT}$ | Output voltage range(2) | $\|V_{IN}\| \geq \|V_{OUT(NOM)}\| + 1.0$ V | –33.2 | | $V_{REF}$ | V |
| | Nominal accuracy | $T_J$ = +25°C, $\|V_{IN}\| = \|V_{OUT(NOM)}\| + 0.5$ V | –1.5 | | 1.5 | $\%V_{OUT}$ |
| | Overall accuracy | 5.0 V ≤ $\|V_{IN}\|$ ≤ 35 V<br>1 mA ≤ $I_{OUT}$ ≤ 1 A | | ±1.0 | | $\%V_{OUT}$ |
| | | $\|V_{OUT(NOM)}\| + 1.0$ V ≤ $\|V_{IN}\|$ ≤ 35 V<br>1 mA ≤ $I_{OUT}$ ≤ 1 A | –2.5 | | 2.5 | $\%V_{OUT}$ |
| $\Delta V_{O(\Delta VI)}$ | Line regulation | $\|V_{OUT(NOM)}\| + 1.0$ V ≤ $\|V_{IN}\|$ ≤ 35 V | | 0.14 | | $\%V_{OUT}$ |
| $\Delta V_{O(\Delta IL)}$ | Load regulation | 1 mA ≤ $I_{OUT}$ ≤ 1 A | | 0.4 | | $\%V_{OUT}$ |
| $\|V_{DO}\|$ | Dropout voltage | $V_{IN}$ = 95% $V_{OUT(NOM)}$, $I_{OUT}$ = 500 mA | | 290 | | mV |
| | | $V_{IN}$ = 95% $V_{OUT(NOM)}$, $I_{OUT}$ = 1 A | | 325 | 800 | mV |
| $I_{LIM}$ | Current limit | $V_{OUT}$ = 90% $V_{OUT(NOM)}$ | | 1900 | | mA |
| $I_{GND}$ | Ground current | $I_{OUT}$ = 0 mA | | 210 | 350 | µA |
| | | $I_{OUT}$ = 500 mA | | 5 | | mA |
| $\|I_{SHDN}\|$ | Shutdown supply current | $V_{EN}$ = +0.4 V | | 1.0 | 3.0 | µA |
| | | $V_{EN}$ = –0.4 V | | 1.0 | 3.0 | µA |
| $I_{FB}$ | Feedback current(3) | | | 14 | 100 | nA |
| $\|I_{EN}\|$ | Enable current | $V_{EN} = \|V_{IN}\| = \|V_{OUT(NOM)}\| + 1.0$ V | | 0.48 | 1.0 | µA |
| | | $V_{IN} = V_{EN}$ = –35 V | | 0.51 | 1.0 | µA |
| | | $V_{IN}$ = –35 V, $V_{EN}$ = +10 V | | 0.50 | 1.0 | µA |
| $V_{+EN\_HI}$ | Positive enable high-level voltage | | 2.0 | | 10 | V |
| $V_{+EN\_LO}$ | Positive enable low-level voltage | | 0 | | 0.4 | V |
| $V_{–EN\_HI}$ | Negative enable high-level voltage | | $V_{IN}$ | | –2.0 | V |
| $V_{–EN\_LO}$ | Negative enable low-level voltage | | –0.4 | | 0 | V |
| $V_n$ | Output noise voltage | $V_{IN}$ = –3 V, $V_{OUT(NOM)} = V_{REF}$, $C_{OUT}$ = 22 µF, $C_{NR/SS}$ = 10 nF, BW = 10 Hz to 100 kHz | | 16 | | $\mu V_{RMS}$ |
| PSRR | Power-supply rejection ratio | $V_{IN}$ = –6.2 V, $V_{OUT(NOM)}$ = –5 V, $C_{OUT}$ = 22 µF, $C_{NR/SS}$ = 10 nF, $C_{FF}$(4) = 10 nF, f = 10 kHz | | 72 | | dB |
| $T_{SD}$ | Thermal shutdown temperature | Shutdown, temperature increasing | | +170 | | °C |
| | | Reset, temperature decreasing | | +150 | | °C |
| $T_J$ | Operating junction temperature range | | –40 | | +125 | °C |

(1) At operating conditions, $V_{IN} \leq 0$ V, $V_{OUT(NOM)} \leq V_{REF} \leq 0$ V. At regulation, $V_{IN} \leq V_{OUT(NOM)} - |V_{DO}|$. $I_{OUT} > 0$ flows from OUT to IN.
(2) To ensure stability at no load conditions, a current from the feedback resistive network equal to or greater than 5 µA is required.
(3) $I_{FB} > 0$ flows into the device.
(4) $C_{FF}$ refers to a feed-forward capacitor connected to the FB and OUT pins.

## PARAMETRIC MEASUREMENT INFORMATION

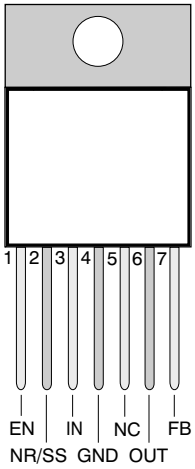
## TYPICAL APPLICATION CIRCUIT



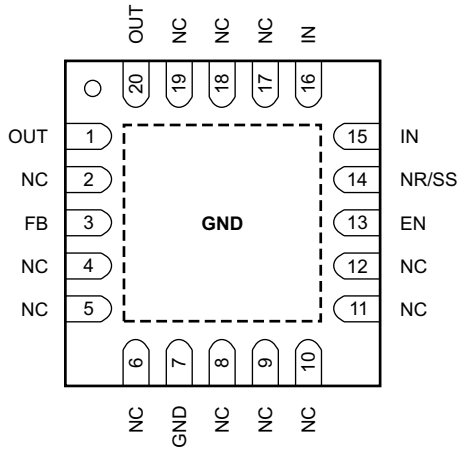

**Maximize PSRR Performance and Minimize RMS Noise**

## PIN CONFIGURATIONS

**KC PACKAGE**
**TO-220-7**
**(TOP VIEW)**




**RGW PACKAGE**
**5-mm × 5-mm QFN-20**
**(TOP VIEW)**

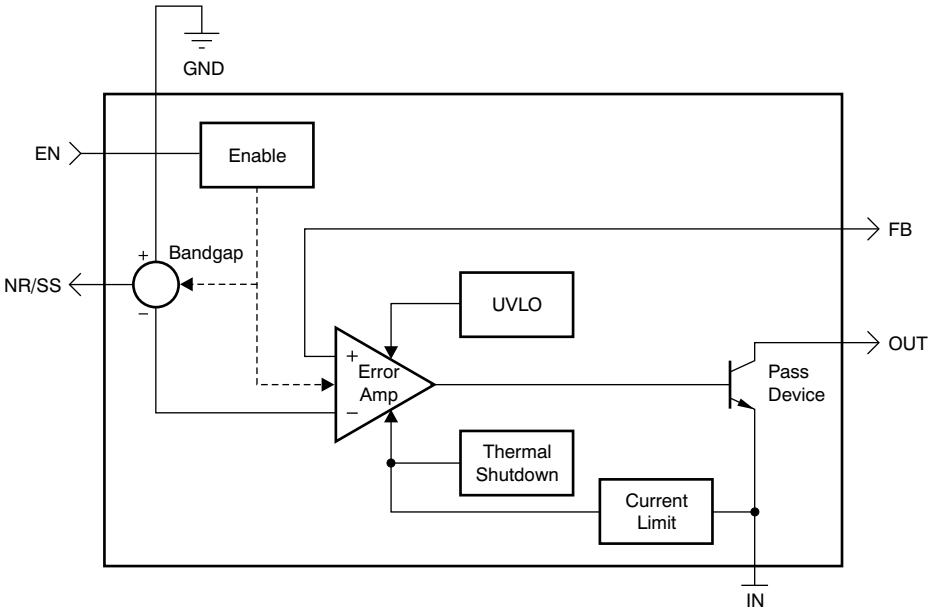



## PIN DESCRIPTIONS

| NAME | NO. KC | NO. RGW[1] | DESCRIPTION |
|---|---|---|---|
| EN | 1 | 13 | This pin turns the regulator on or off. If $V_{EN} \geq V_{+EN\_HI}$ or $V_{EN} \leq V_{–EN\_HI}$, the regulator is enabled. If $V_{+EN\_LO} \geq V_{EN} \geq V_{–EN\_LO}$, the regulator is disabled. The EN pin can be connected to IN, if not used. $\lvert V_{EN}\rvert \leq \lvert V_{IN}\rvert$. |
| FB | 7 | 3 | This pin is the input to the control-loop error amplifier. It is used to set the output voltage of the device. It is recommended to connect a 0.01-µF capacitor from FB to OUT (as close to the device as possible) to maximize ac performance. |
| GND | 4 | 7 | Ground |
| IN | 3 | 15, 16 | Input supply. A capacitor greater than or equal to 10 nF must be tied from this pin to ground to assure stability. It is recommended to connect a 10-µF capacitor from IN to GND (as close to the device as possible) to reduce circuit sensitivity to printed-circuit-board (PCB) layout, especially when long input traces or high source impedances are encountered. |
| NC | 5 | 2, 4-6, 8-12, 17-19 | This pin can be left open or tied to any voltage between GND and IN. |
| NR/SS | 2 | 14 | Noise reduction pin. A capacitor connected from this pin to GND controls the soft-start function and allows RMS noise to be reduced to very low levels. It is recommended to connect a 1-µF capacitor from NR/SS to GND (as close to the device as possible) to bypass the noise generated by the internal bandgap and maximize ac performance. |
| OUT | 6 | 1, 20 | Regulator output. A capacitor greater than or equal to 10 µF must be tied from this pin to ground to assure stability. It is recommended to connect a 47-µF ceramic capacitor from OUT to GND (as close to the device as possible) to maximize ac performance. |
| Tab | Tab | — | TAB is internally connected to GND. An external heatsink can be installed to provide additional thermal performance. |

(1) RGW is a product-preview device.

## FUNCTIONAL BLOCK DIAGRAM



## TYPICAL CHARACTERISTICS

At $T_J$ = –40°C to +125°C, $|V_{IN}| = |V_{OUT(NOM)}| + 1.0$ V or $|V_{IN}| = 3.0$ V (whichever is greater), $V_{EN} = V_{IN}$, $I_{OUT}$ = 1 mA, $C_{IN}$ = 22 µF, $C_{OUT}$ = 22 µF, $C_{NR/SS}$ = 0 nF, and the FB pin tied to OUT, unless otherwise noted.

**FEEDBACK VOLTAGE vs INPUT VOLTAGE**

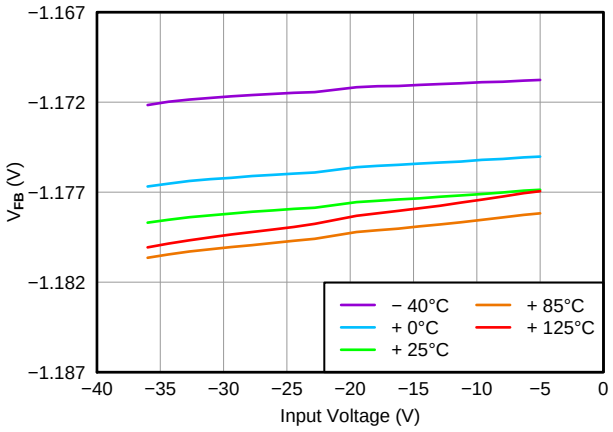



**Figure 1.**

**FEEDBACK CURRENT vs TEMPERATURE**

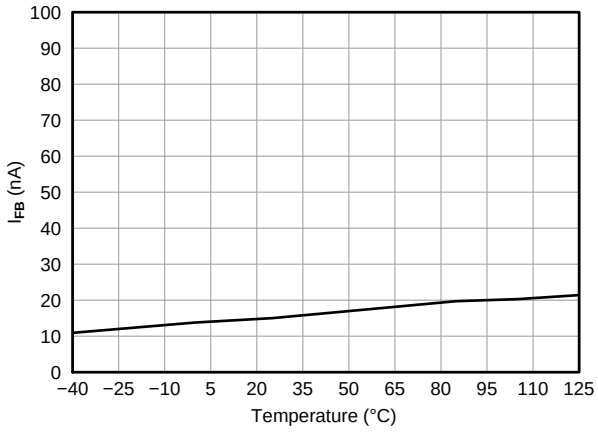



**Figure 2.**

**GROUND CURRENT vs INPUT VOLTAGE**

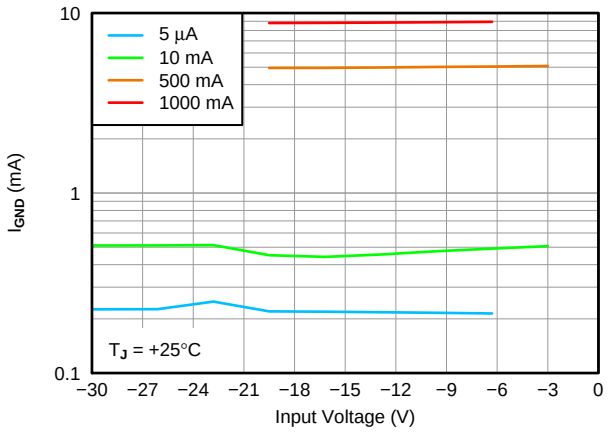



**Figure 3.**

**GROUND CURRENT vs INPUT VOLTAGE**

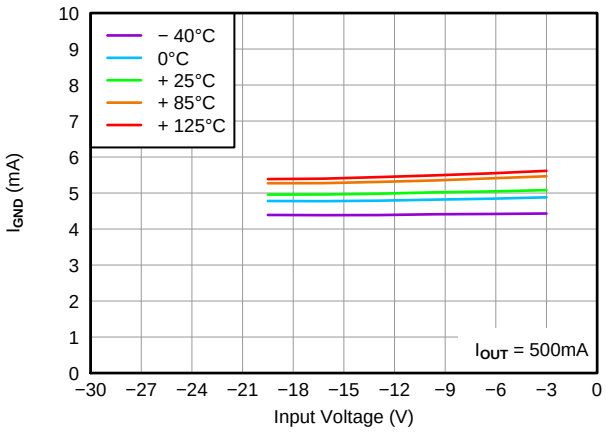



**Figure 4.**

**GROUND CURRENT vs OUTPUT CURRENT**

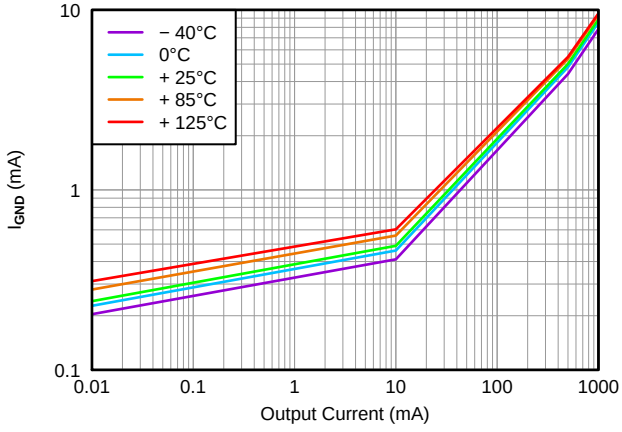



**Figure 5.**

**ENABLE CURRENT vs ENABLE VOLTAGE**

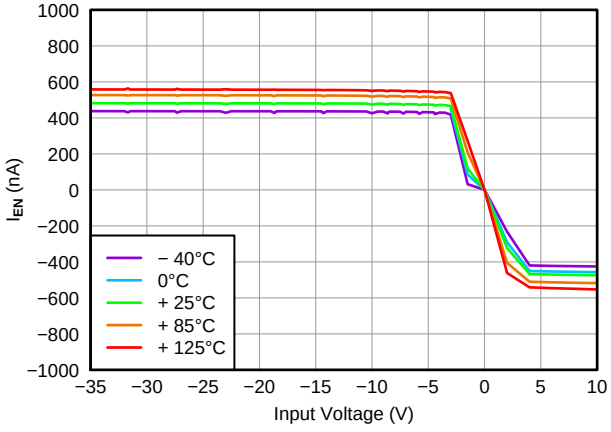



**Figure 6.**

## TYPICAL CHARACTERISTICS (continued)

At $T_J$ = –40°C to +125°C, $|V_{IN}| = |V_{OUT(NOM)}|$ + 1.0 V or $|V_{IN}|$ = 3.0 V (whichever is greater), $V_{EN} = V_{IN}$, $I_{OUT}$ = 1 mA, $C_{IN}$ = 22 µF, $C_{OUT}$ = 22 µF, $C_{NR/SS}$ = 0 nF, and the FB pin tied to OUT, unless otherwise noted.

**QUIESCENT CURRENT vs INPUT VOLTAGE**

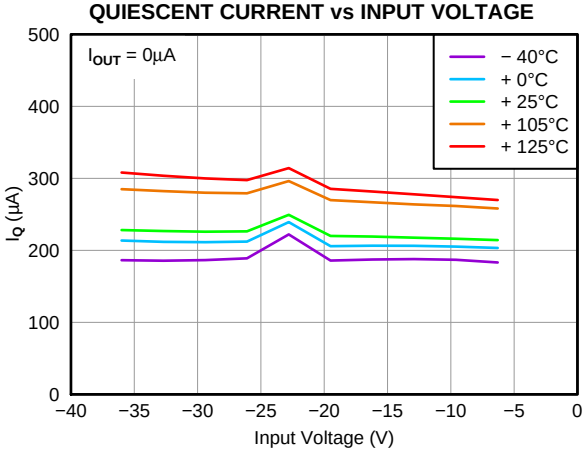



**Figure 7.**

**SHUTDOWN CURRENT vs INPUT VOLTAGE**

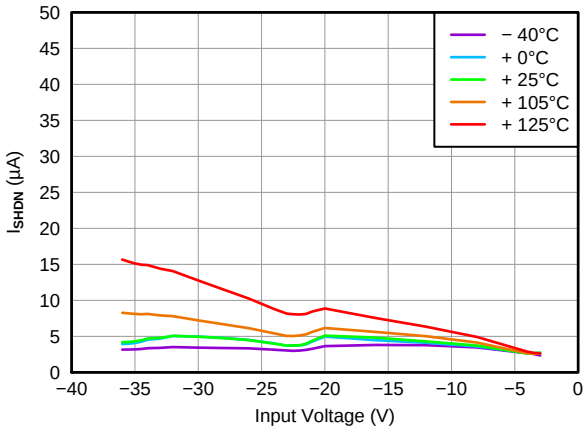



**Figure 8.**

**DROPOUT VOLTAGE vs OUTPUT CURRENT**

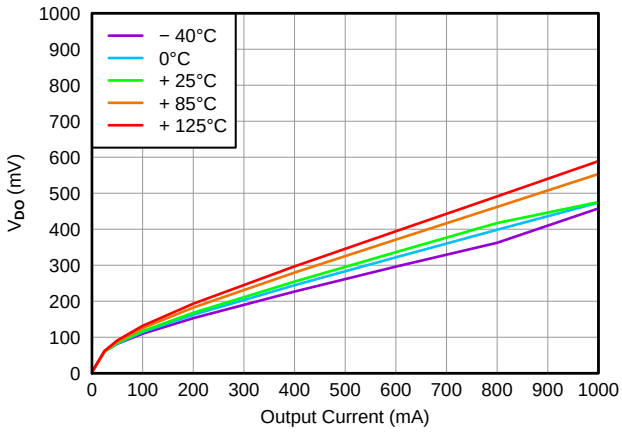



**Figure 9.**

**DROPOUT VOLTAGE vs TEMPERATURE**

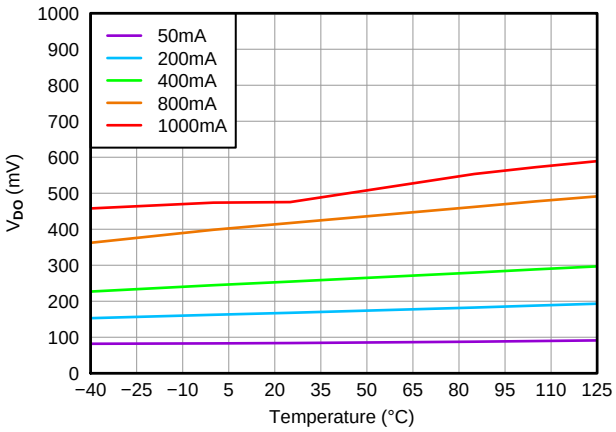



**Figure 10.**

**ENABLE THRESHOLD VOLTAGE vs TEMPERATURE**

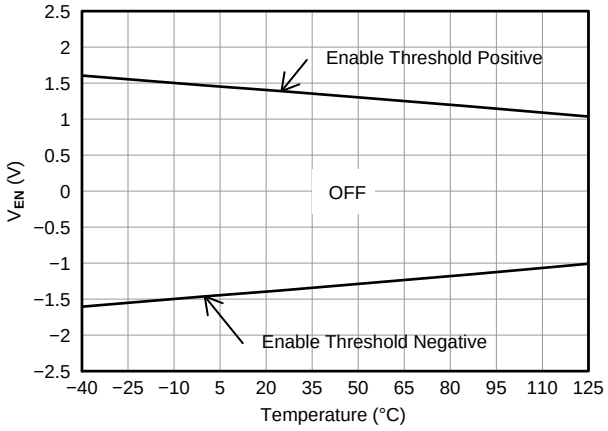



**Figure 11.**

**LINE REGULATION**

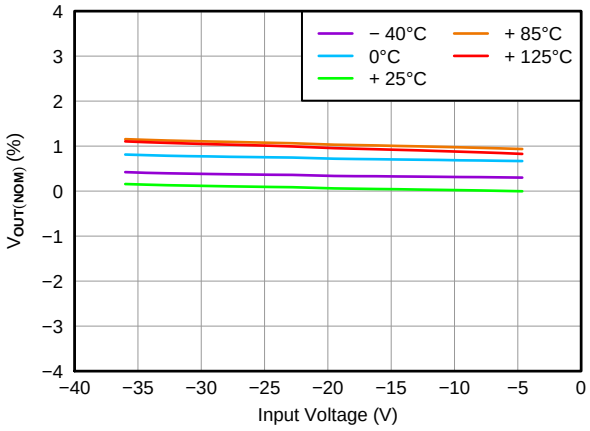



**Figure 12.**

## TYPICAL CHARACTERISTICS (continued)

At $T_J$ = –40°C to +125°C, $|V_{IN}| = |V_{OUT(NOM)}|$ + 1.0 V or $|V_{IN}|$ = 3.0 V (whichever is greater), $V_{EN} = V_{IN}$, $I_{OUT}$ = 1 mA, $C_{IN}$ = 22 µF, $C_{OUT}$ = 22 µF, $C_{NR/SS}$ = 0 nF, and the FB pin tied to OUT, unless otherwise noted.

**LOAD REGULATION**

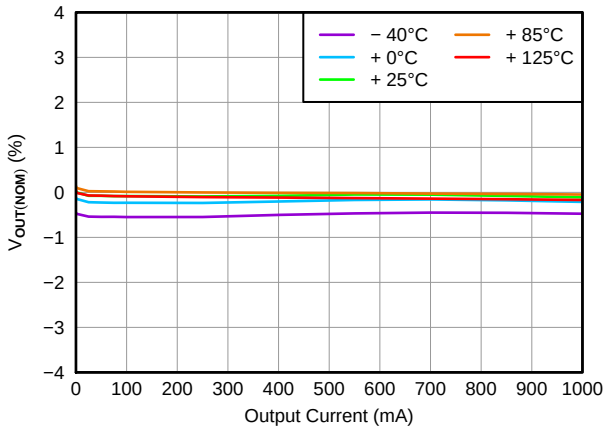



**Figure 13.**

**POWER-SUPPLY REJECTION RATIO vs $C_{OUT}$**

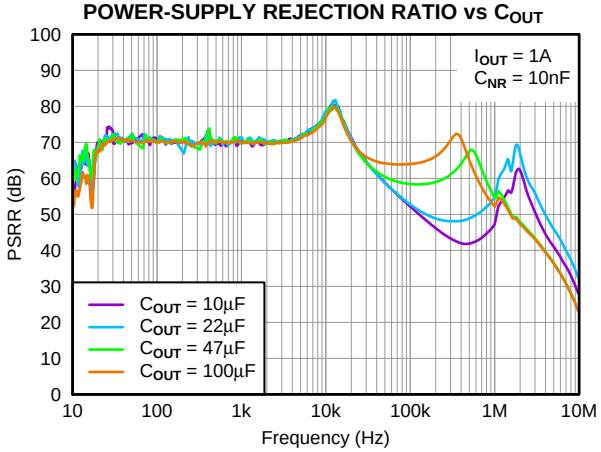



**Figure 14.**

**POWER-SUPPLY REJECTION RATIO vs $C_{NR/SS}$**

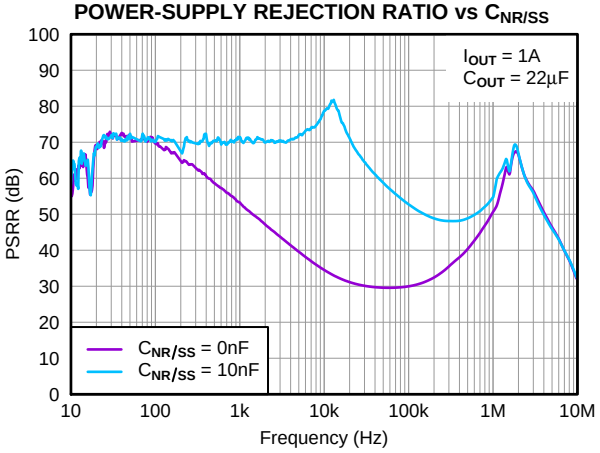



**Figure 15.**

**POWER-SUPPLY REJECTION RATIO vs $C_{FF}$**

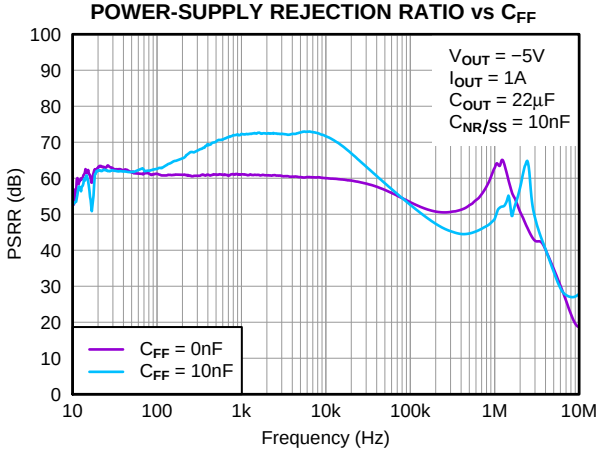



**Figure 16.**

**POWER-SUPPLY REJECTION RATIO vs $I_{OUT}$**

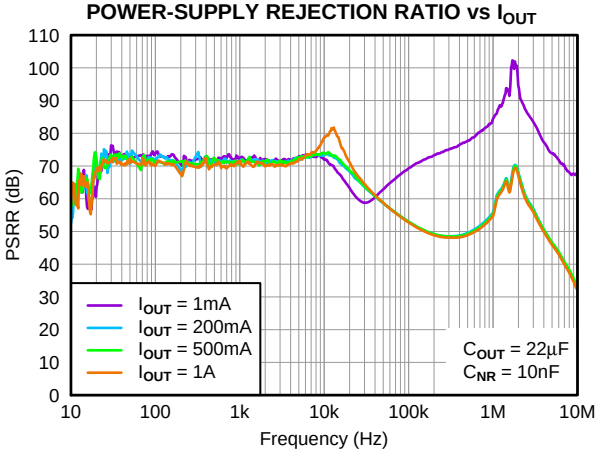



**Figure 17.**

**POWER-SUPPLY REJECTION RATIO vs $V_{OUT}$**

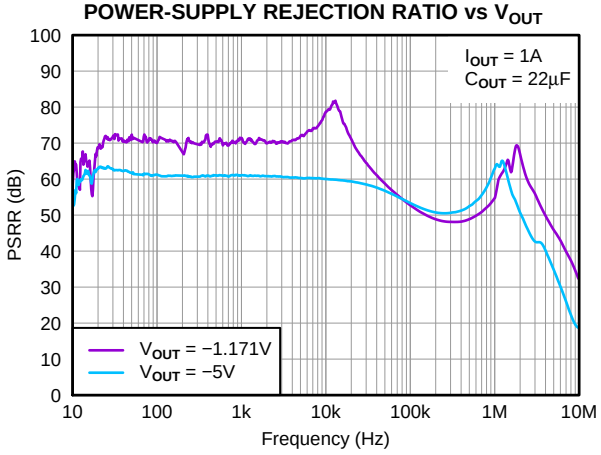



**Figure 18.**

## TYPICAL CHARACTERISTICS (continued)

At $T_J$ = –40°C to +125°C, $|V_{IN}| = |V_{OUT(NOM)}| + 1.0$ V or $|V_{IN}| = 3.0$ V (whichever is greater), $V_{EN} = V_{IN}$, $I_{OUT}$ = 1 mA, $C_{IN}$ = 22 µF, $C_{OUT}$ = 22 µF, $C_{NR/SS}$ = 0 nF, and the FB pin tied to OUT, unless otherwise noted.

**POWER-SUPPLY REJECTION RATIO vs $V_{DO}$**

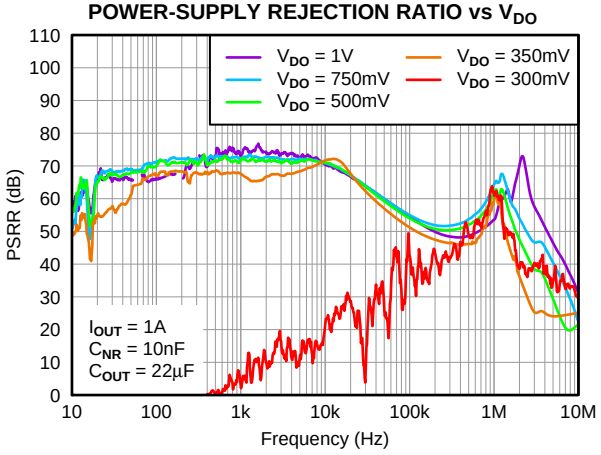



**Figure 19.**

**OUTPUT SPECTRAL NOISE DENSITY vs OUTPUT CURRENT**

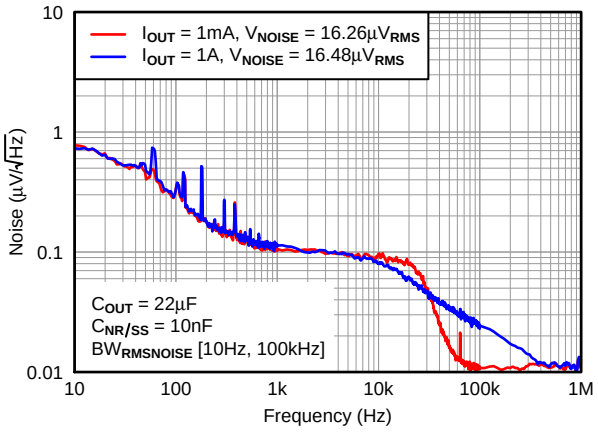



**Figure 20.**

**OUTPUT SPECTRAL NOISE DENSITY vs $C_{NR/SS}$**

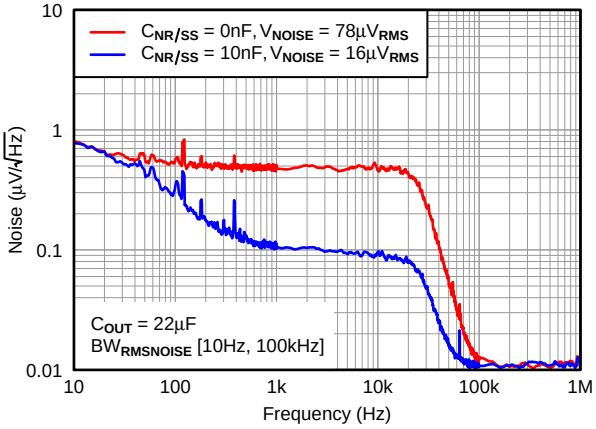



**Figure 21.**

**OUTPUT SPECTRAL NOISE DENSITY vs $V_{OUT(NOM)}$**

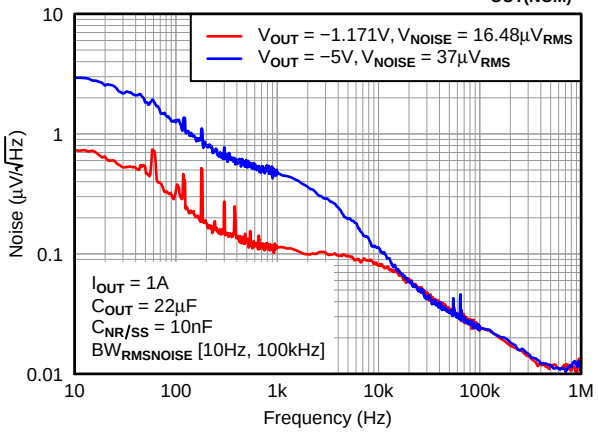



**Figure 22.**

**LOAD TRANSIENT**

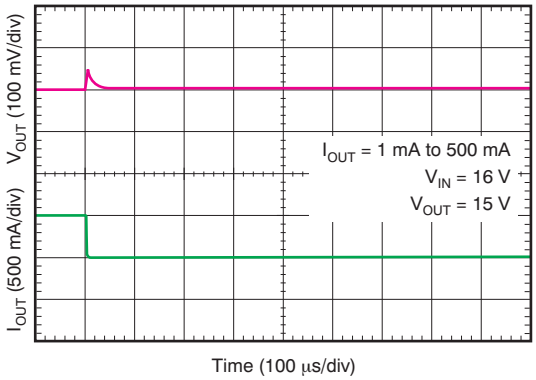



**Figure 23.**

**LOAD TRANSIENT**

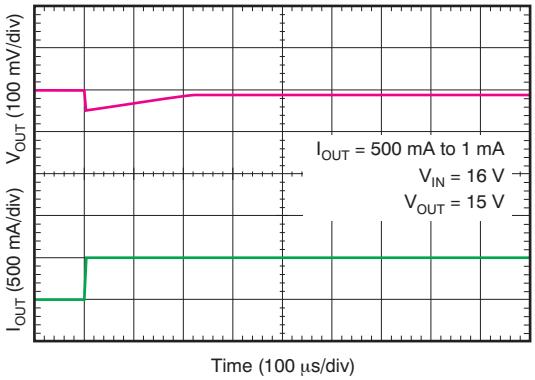



**Figure 24.**

## TYPICAL CHARACTERISTICS (continued)

At $T_J$ = –40°C to +125°C, $|V_{IN}| = |V_{OUT(NOM)}| + 1.0$ V or $|V_{IN}| = 3.0$ V (whichever is greater), $V_{EN} = V_{IN}$, $I_{OUT}$ = 1 mA, $C_{IN}$ = 22 µF, $C_{OUT}$ = 22 µF, $C_{NR/SS}$ = 0 nF, and the FB pin tied to OUT, unless otherwise noted.

**LINE TRANSIENT**

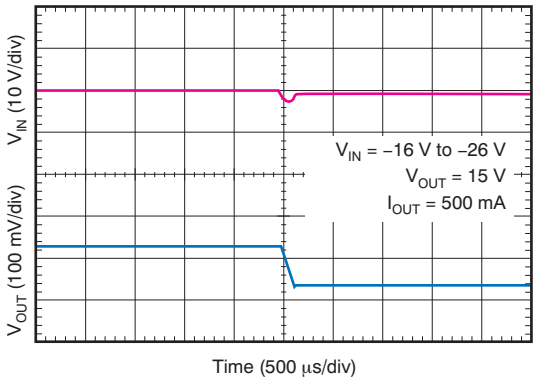



**Figure 25.**

**LINE TRANSIENT**

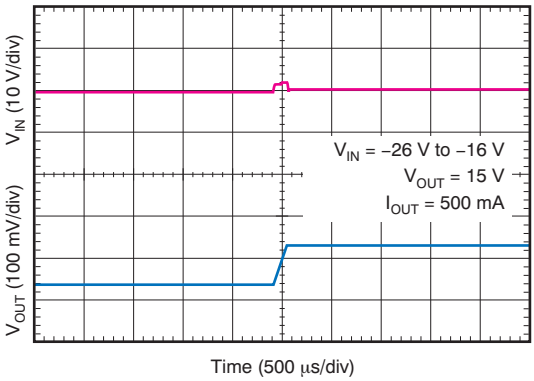



**Figure 26.**

**CAPACITOR-PROGRAMMABLE SOFT-START**

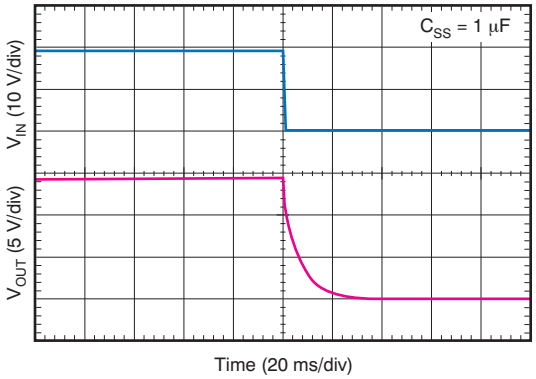



**Figure 27.**

# THEORY OF OPERATION

## GENERAL DESCRIPTION

The TPS7A33 belongs to a family of new-generation linear regulators that use an innovative bipolar process to achieve ultralow-noise and very high PSRR levels at a wide input voltage and current range. These features, combined with the external heatsink-capable, high thermal performance TO-220 package, make this device ideal for high-performance analog applications.

## ADJUSTABLE OPERATION

The TPS7A3301 has an output voltage range of –1.182 V to –33 V. The nominal output voltage of the device is set by two external resistors, as shown in Figure 28.

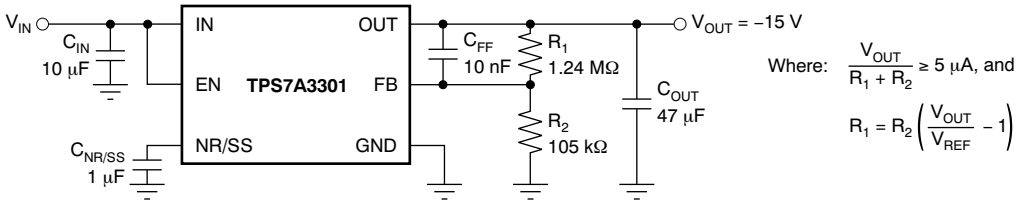



**Figure 28. Adjustable Operation for Maximum AC Performance**

$R_1$ and $R_2$ can be calculated for any output voltage range using Equation 1. To ensure stability under no load conditions at $V_{OUT} > V_{REF}$, this resistive network must provide a current equal to or greater than 5 µA.

$$R_1 = R_2 \left( \frac{V_{OUT}}{V_{REF}} - 1 \right), \quad \text{where } \frac{V_{OUT}}{R_1 + R_2} \geq 5\ \mu A \tag{1}$$

If greater voltage accuracy is required, take into account the output voltage offset contributions because of the feedback pin current and use 0.1% tolerance resistors.

Table 1 shows the resistor combination to achieve a few of the most common rails using commercially-available, 0.1%-tolerance resistors to maximize nominal voltage accuracy while abiding to the formula shown in Equation 1:

**Table 1. Suggested Resistors for Common Voltage Rails**

| $V_{OUT}$ | $R_1$ | $R_2$ | $V_{OUT}/(R_1+R_2)$ | NOMINAL ACCURACY |
|---|---|---|---|---|
| –1.171 V | 0 Ω | ∞ | 0 µA | ±1.5% |
| –1.8 V | 76.8 kΩ | 143 kΩ | 8.18 µA | ±(1.5% + 0.08%) |
| –3.3 V | 200 kΩ | 110 kΩ | 10.64 µA | ±(1.5% + 0.13%) |
| –5 V | 332 kΩ | 102 kΩ | 11.48 µA | ±(1.5% + 0.50%) |
| –10 V | 1.62 MΩ | 215 kΩ | 5.44 µA | ±(1.5% + 0.23%) |
| –12 V | 1.5 MΩ | 162 kΩ | 7.22 µA | ±(1.5% + 0.29%) |
| –15 V | 1.24 MΩ | 105 kΩ | 11.15 µA | ±(1.5% + 0.18%) |
| –18 V | 3.09 MΩ | 215 kΩ | 5.44 µA | ±(1.5% + 0.19%) |
| –24 V | 1.15 MΩ | 59 kΩ | 19.84 µA | ±(1.5% + 0.21%) |

## ENABLE PIN OPERATION

The TPS7A33 provides a dual-polarity enable pin (EN) that turns on the regulator when $|V_{EN}|$ > 2.0 V, whether the voltage is positive or negative, as shown in Figure 29.

This functionality allows for different system power management topologies; for example:

- Connecting the EN pin directly to a negative voltage, such as $V_{IN}$, or
- Connecting the EN pin directly to a positive voltage, such as the output of digital logic circuitry.

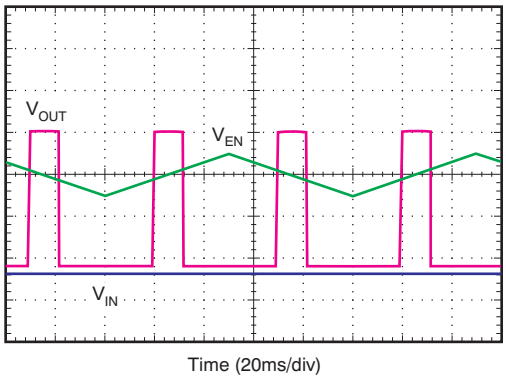



**Figure 29. Enable Pin Positive/Negative Threshold**

## CAPACITOR RECOMMENDATIONS

Low equivalent series resistance (ESR) capacitors should be used for the input, output, noise reduction, and bypass capacitors. Ceramic capacitors with X7R and X5R dielectrics are preferred. These dielectrics offer more stable characteristics. Ceramic X7R capacitors offer improved over-temperature performance, while ceramic X5R capacitors are the most cost-effective and are available in higher values.

Note that high-ESR capacitors may degrade PSRR.

## INPUT AND OUTPUT CAPACITOR REQUIREMENTS

The TPS7A33 family of negative, high-voltage linear regulators achieve stability with a minimum input and output capacitance of 10 µF; however, it is highly recommended to use a 47-µF capacitor to maximize ac performance.

## NOISE REDUCTION AND FEED-FORWARD CAPACITOR REQUIREMENTS

Although the noise-reduction ($C_{NR/SS}$) and feed-forward ($C_{FF}$) capacitors are not needed to achieve stability, it is highly recommended to use a 0.01-µF feed-forward capacitor and a 1-µF noise-reduction capacitor to minimize noise and maximize ac performance.

## MAXIMUM AC PERFORMANCE

In order to maximize noise and PSRR performance, it is recommended to include 47-µF or higher input and output capacitors, 1-µF noise-reduction capacitors, and 0.01-µF feed-forward capacitors, as shown in Figure 28. The solution shown delivers minimum noise levels of 16 $\mu V_{RMS}$ and power-supply rejection levels above 55 dB from 10 Hz to 1 MHz; see Figure 19.

## OUTPUT NOISE

The TPS7A33 provides low output noise when a noise-reduction capacitor ($C_{NR/SS}$) is used.

The noise-reduction capacitor serves as a filter for the internal reference. By using a 1-µF noise reduction capacitor, the output noise is reduced by almost 80% (from 80 $\mu V_{RMS}$ to 17 $\mu V_{RMS}$); see Figure 21.

The TPS7A33 low output voltage noise makes it an ideal solution for powering noise-sensitive circuitry.

## POWER-SUPPLY REJECTION

The 1-µF noise-reduction capacitor greatly improves TPS7A33 power-supply rejection, achieving up to 10 dB of additional power-supply rejection for frequencies between 140 Hz and 500 KHz.

Additionally, ac performance can be maximized by adding a 0.01-µF feed-forward capacitor ($C_{FF}$) from the FB pin to the OUT pin. This capacitor greatly improves power-supply rejection at lower frequencies, for the band from 100 Hz to 100 kHz; see Figure 15.

The very-high power-supply rejection of the TPS7A33 makes it a good choice for powering high-performance analog circuitry, such as operational amplifiers, ADCs, DACS, and audio amplifiers.

## TRANSIENT RESPONSE

As with any regulator, increasing the size of the output capacitor reduces over/undershoot magnitude, but increases duration of the transient response.

# APPLICATION INFORMATION

## POWER FOR PRECISION ANALOG

One of the primary TPS7A33 applications is to provide ultralow-noise voltage rails to high-performance analog circuitry in order to maximize system accuracy and precision.

The TPS7A33 family of negative, high-voltage linear regulators provides ultralow noise, positive and negative voltage rails to high-performance analog circuitry such as operational amplifiers, ADCs, DACs, and audio amplifiers.

Because of the ultralow noise levels at high voltages, analog circuitry with high-voltage input supplies can be used. This characteristic allows for high-performance analog solutions to optimize the voltage range, thus maximizing system accuracy.

## POST DC-DC CONVERTER FILTERING

Most of the time, the voltage rails available in a system do not match the voltage specifications demanded by one or more of its circuits; these rails must be stepped up or down, depending on specific voltage requirements.

DC-DC converters are the preferred solution to stepping up or down a voltage rail when current consumption is not negligible. They offer high efficiency with minimum heat generation, but they have one primary disadvantage: they introduce a high-frequency component, and the associated harmonics, on top of the dc output signal.

If not filtered properly, this high-frequency component degrades analog circuitry performance, reducing overall system accuracy and precision.

The TPS7A33 offers a wide-bandwidth, very-high power-supply rejection ratio. This specification makes it ideal for post dc-dc converter filtering, as shown in Figure 30. It is highly recommended to use the maximum performance schematic shown in Figure 28. Also, verify that the fundamental frequency (and its first harmonic, if possible) is within the bandwidth of the regulator PSRR, shown in Figure 16.

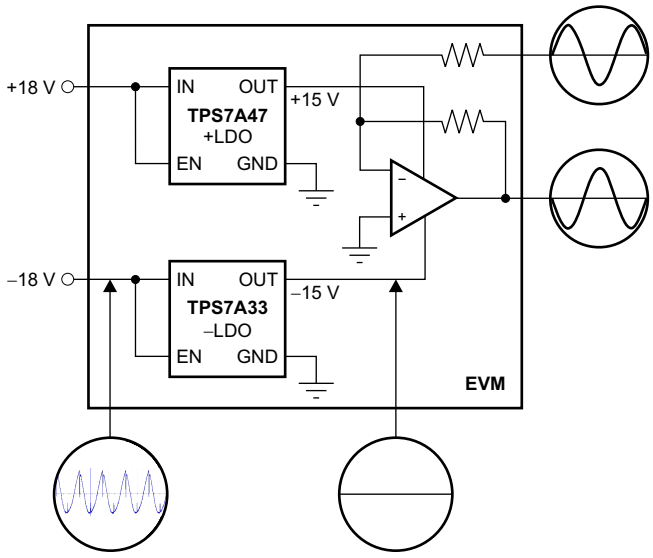



**Figure 30. Post DC-DC Converter Regulation to High-Performance Analog Circuitry**

## AUDIO APPLICATIONS

Audio applications are extremely sensitive to any distortion and noise in the audio band from 20 Hz to 20 kHz. This stringent requirement demands clean voltage rails to power critical high-performance audio systems.

The very-high power-supply rejection ratio (> 60 dB) and low noise at the audio band of the TPS7A33 maximize performance for audio applications; see Figure 16.

# LAYOUT

## POWER DISSIPATION

The primary TPS7A33 application is to provide ultralow noise voltage rails to high-performance analog circuitry in order to maximize system accuracy and precision. The high-current and high-voltage characteristics of this regulator means that, often enough, high power (heat) is dissipated from the device itself. This heat, if dissipated into the PCB (as is the case with SMT packages), creates a temperature gradient in the surrounding area that causes nearby components to react to this temperature change (drift). In high-performance systems, such drift may degrade overall system accuracy and precision.

Compared to surface-mount packages, the TO-220 (KC) package allows for an external heatsink to be used to maximize thermal performance and keep heat from dissipating into the PCB.

Power dissipation depends on input voltage and load conditions. Power dissipation ($P_D$) is equal to the product of the output current times the voltage drop across the output pass element, as shown in Equation 2:

$$P_D = (V_{IN} - V_{OUT})\, I_{OUT} \quad (2)$$

## THERMAL PERFORMANCE AND HEATSINK SELECTION

Heat flows from the device to the ambient air through many paths, each of which represents resistance to the heat flow; this is called thermal resistance.

The total thermal resistance of a system is defined by: $\theta_{JA} = (T_J - T_A)/P_D$; where: $\theta_{JA}$ is the thermal resistance (in °C/W), $T_J$ is the allowable juntion temperature of the device (in °C), $T_A$ is the maximum temperature of the ambient cooling air (in °C), and $P_D$ is the amount of power (heat) dissipated by the device (in W).

Whenever a heatsink is installed, the total thermal resistance ($\theta_{JA}$) is the sum of all the individual resistances from the device, going through its case and heatsink to the ambient cooling air ($\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$). Reallistically, only two resistances can be controlled: $\theta_{CS}$ and $\theta_{SA}$. Therefore, for a device with a known $\theta_{JC}$, $\theta_{CS}$ and $\theta_{SA}$ become the main design variables in selecting a heat sink.

The thermal interface between the case and the heat sink ($\theta_{CS}$) is controlled by selecting the correct heat-conducting material. Once the $\theta_{CS}$ is selected, the required thermal resistance from the heatsink to ambient is calculated by the following equation: $\theta_{SA} = [(T_J - T_A)/P_D] - [\theta_{JC} + \theta_{CS}]$. This information allows the the most appropriate heatsink to be selected for any particular application.

## PACKAGE MOUNTING

The TO-220 (KC) 7-lead, straight-formed package lead spacing poses a challenge when creating a suitable PCB footprint without bending the leads. Component forming pliers, such as Excelta's Q-6482, can be used to manually bend the package leads into a 7-lead stagger pattern with increased lead spacing that can be more easily used.

The TPS7A33 evaluation board layout can be used as a guideline on suitable PCB footprints, available at www.ti.com

## BOARD LAYOUT RECOMMENDATIONS TO IMPROVE PSRR AND NOISE PERFORMANCE

To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate planes for IN, OUT, and GND. The IN and OUT planes should be isolated from each other by a GND plane section. In addition, the ground connection for the output capacitor should connect directly to the GND pin of the device.

Equivalent series inductance (ESL) and equivalent series resistance (ESR) must be minimized in order to maximize performance and ensure stability. Every capacitor ($C_{IN}$, $C_{OUT}$, $C_{NR/SS}$, $C_{FF}$) must be placed as close as possible to the device and on the same side of the printed circuit board (PCB) as the regulator itself.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. The use of vias and long traces is strongly discouraged because they may impact system performance negatively and even cause instability.

If possible, and to ensure the maximum performance specified in this product datasheet, use the same layout pattern used for the TPS7A33 evaluation board, available at www.ti.com.

## THERMAL PROTECTION

Thermal protection disables the output when the junction temperature rises to approximately +170°C, allowing the device to cool. When the junction temperature cools to approximately +150°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to a maximum of +125°C. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least +35°C above the maximum expected ambient condition of your particular application. This configuration produces a worst-case junction temperature of +125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS7A33 has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS7A33 into thermal shutdown degrades device reliability.

## SUGGESTED LAYOUT AND SCHEMATIC

Layout is a critical part of good power-supply design. There are several signal paths that conduct fast-changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power-supply performance. To help eliminate these problems, the IN pin should be bypassed to ground with a low ESR ceramic bypass capacitor with a X5R or X7R dielectric.

It may be possible to obtain acceptable performance with alternative PCB layouts; however, the layout shown in Figure 31 and the schematic shown in Figure 32 have been shown to produce good results and are meant as a guideline.

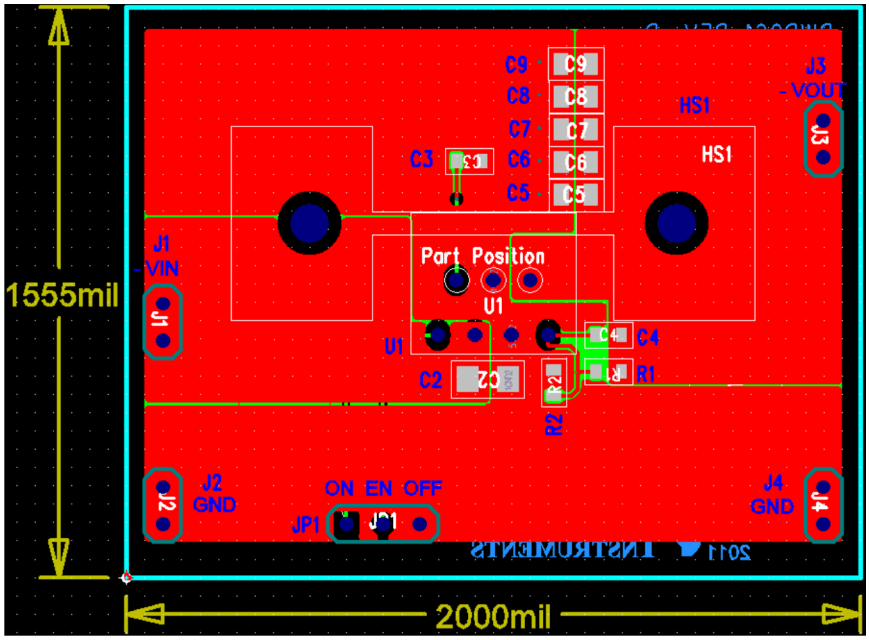



**Figure 31. PCB Layout Example: Top Layer**

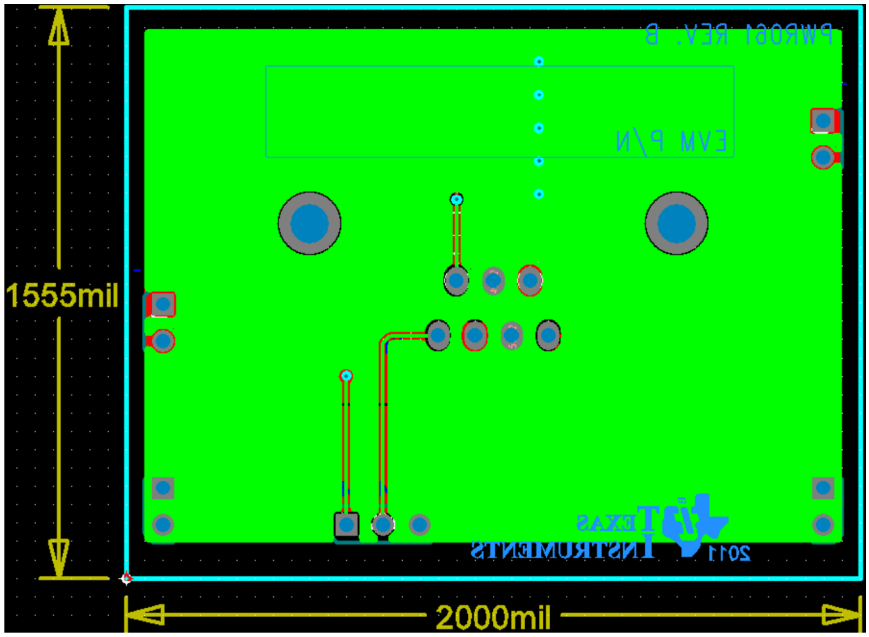



**Figure 32. PCB Layout Example: Bottom Layer**

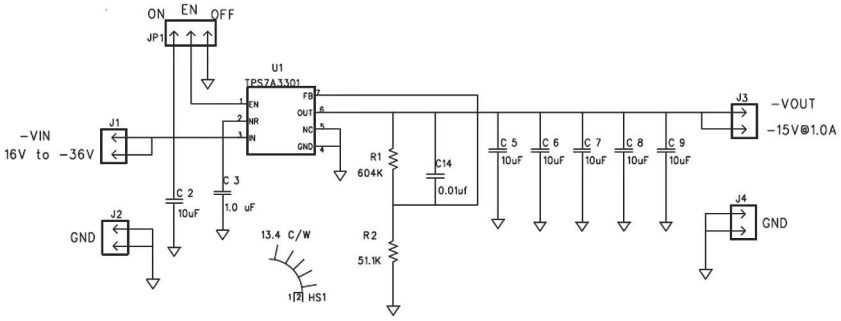



**Figure 33. Schematic for PCB Layout Example**

## REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision B (March 2012) to Revision C** **Page**

- Changed product status from Mixed Status to Production Data ..... 1
- Added last paragraph in Description section ..... 1
- Changed typical application block diagram ..... 1
- Updated Figure 30 ..... 14

**Changes from Revision A (December 2011) to Revision B** **Page**

- Changed product status from Production Data to Mixed Status ..... 1
- Added RGW pin out drawing ..... 1
- Added RGW column to Thermal Information table ..... 2
- Added RGW pin out drawing to Pin Configurations section ..... 4
- Added RGW and footnote 1 to Pin Descriptions table ..... 4

**Changes from Original (December 2011) to Revision A** **Page**

- Changed product status from Product Preview to Production Data ..... 1

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS7A3301KC | ACTIVE | TO-220 | KC | 7 | 50 | Pb-Free (RoHS) | CU SN | Level-2-260C-1 YEAR | -40 to 125 | PPQQ | Samples |
| TPS7A3301RGWR | ACTIVE | VQFN | RGW | 20 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PXQQ | Samples |
| TPS7A3301RGWT | ACTIVE | VQFN | RGW | 20 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PXQQ | Samples |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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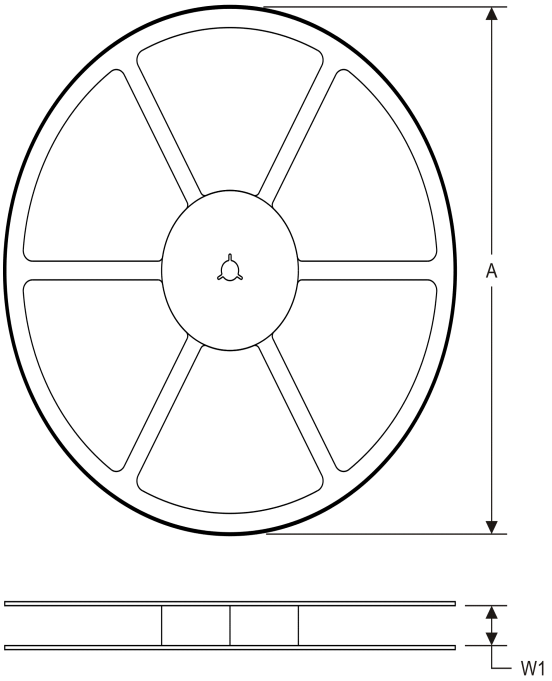
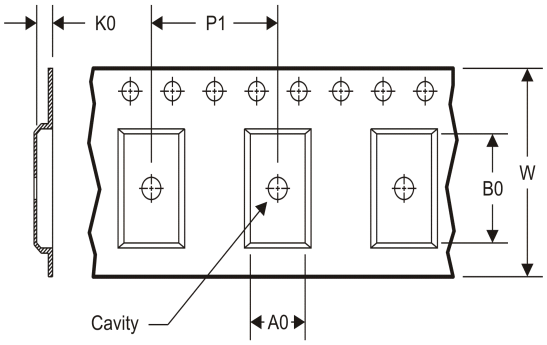
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**




**TAPE DIMENSIONS**



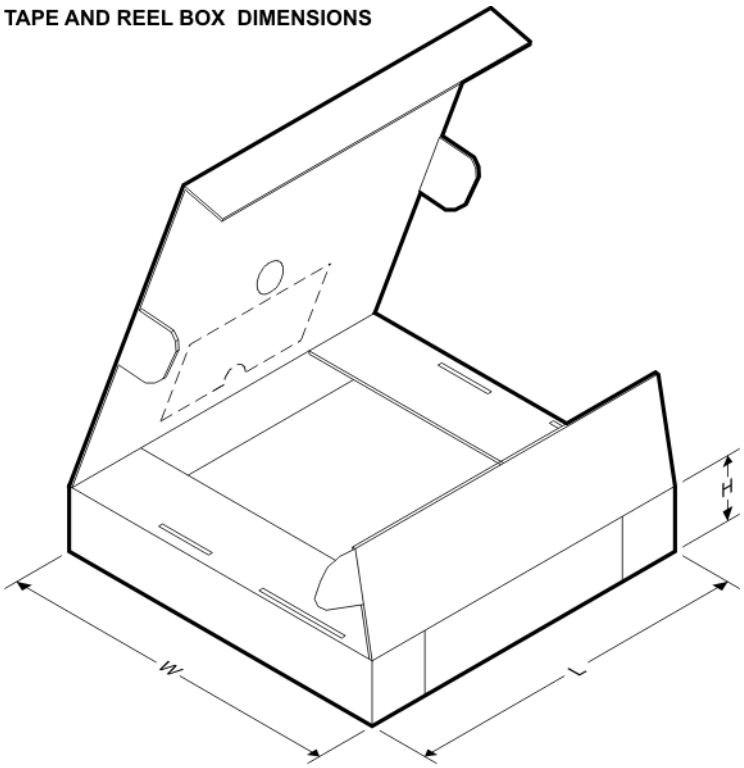

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**TAPE AND REEL INFORMATION**

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS7A3301RGWR | VQFN | RGW | 20 | 3000 | 330.0 | 12.4 | 5.3 | 5.3 | 1.5 | 8.0 | 12.0 | Q2 |
| TPS7A3301RGWT | VQFN | RGW | 20 | 250 | 180.0 | 12.4 | 5.3 | 5.3 | 1.5 | 8.0 | 12.0 | Q2 |

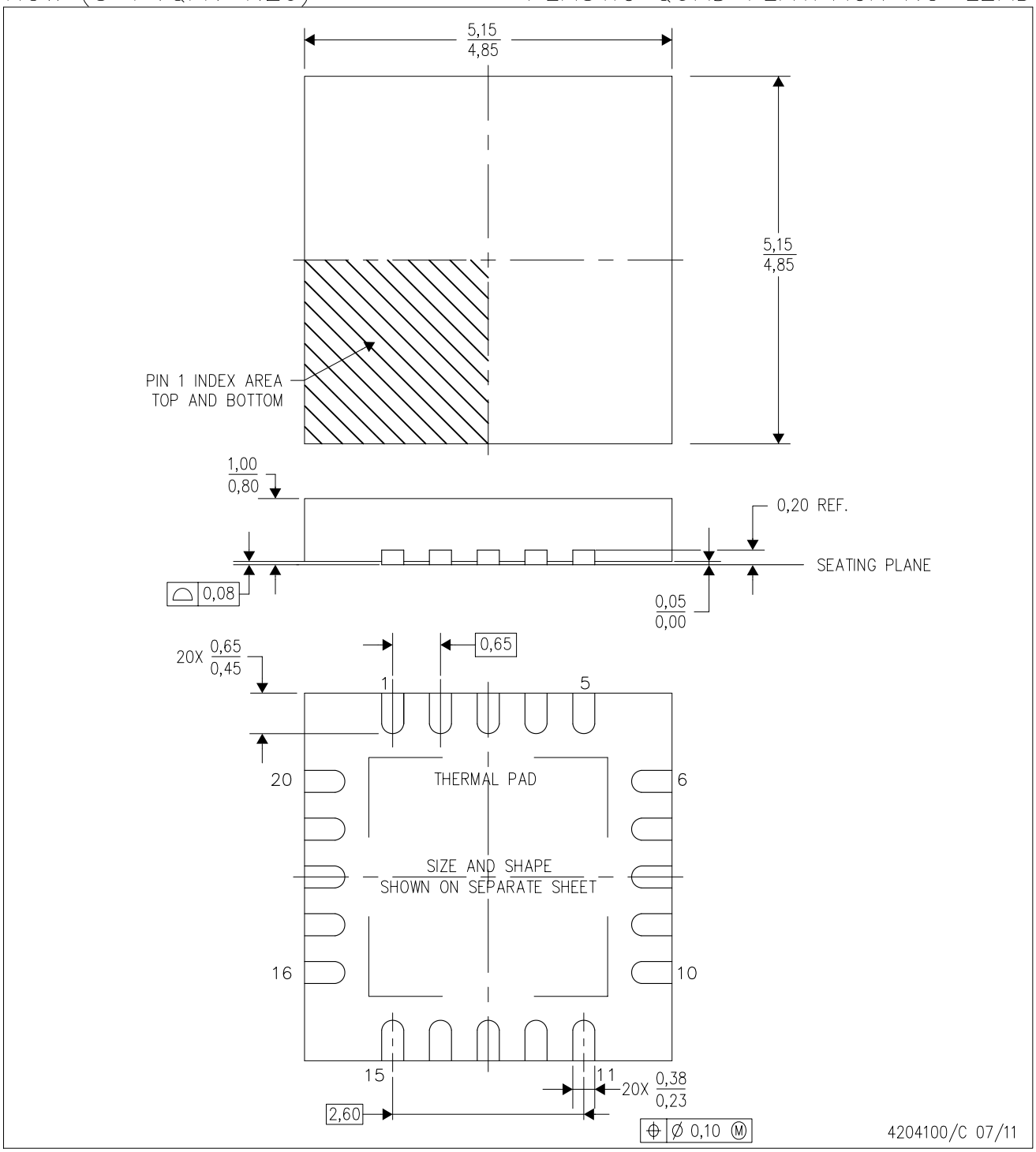
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS7A3301RGWR | VQFN | RGW | 20 | 3000 | 367.0 | 367.0 | 35.0 |
| TPS7A3301RGWT | VQFN | RGW | 20 | 250 | 210.0 | 185.0 | 35.0 |

RGW (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flat pack, No–leads (QFN) package configuration
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

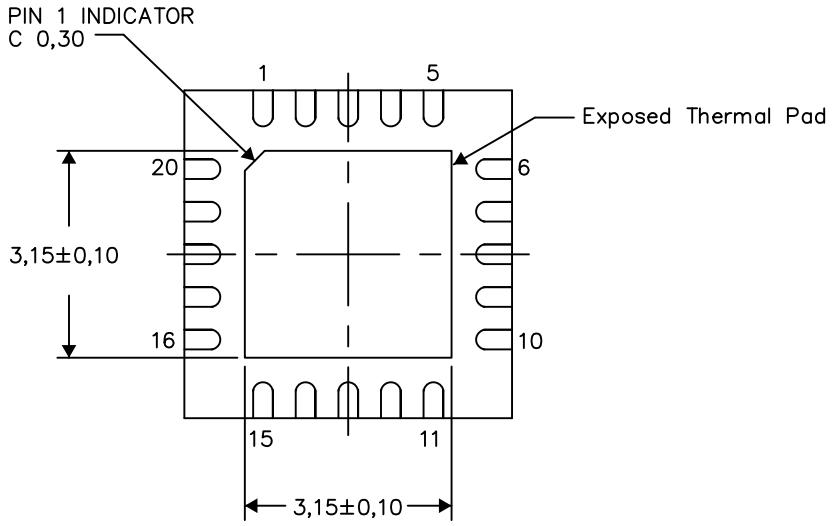
RGW (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



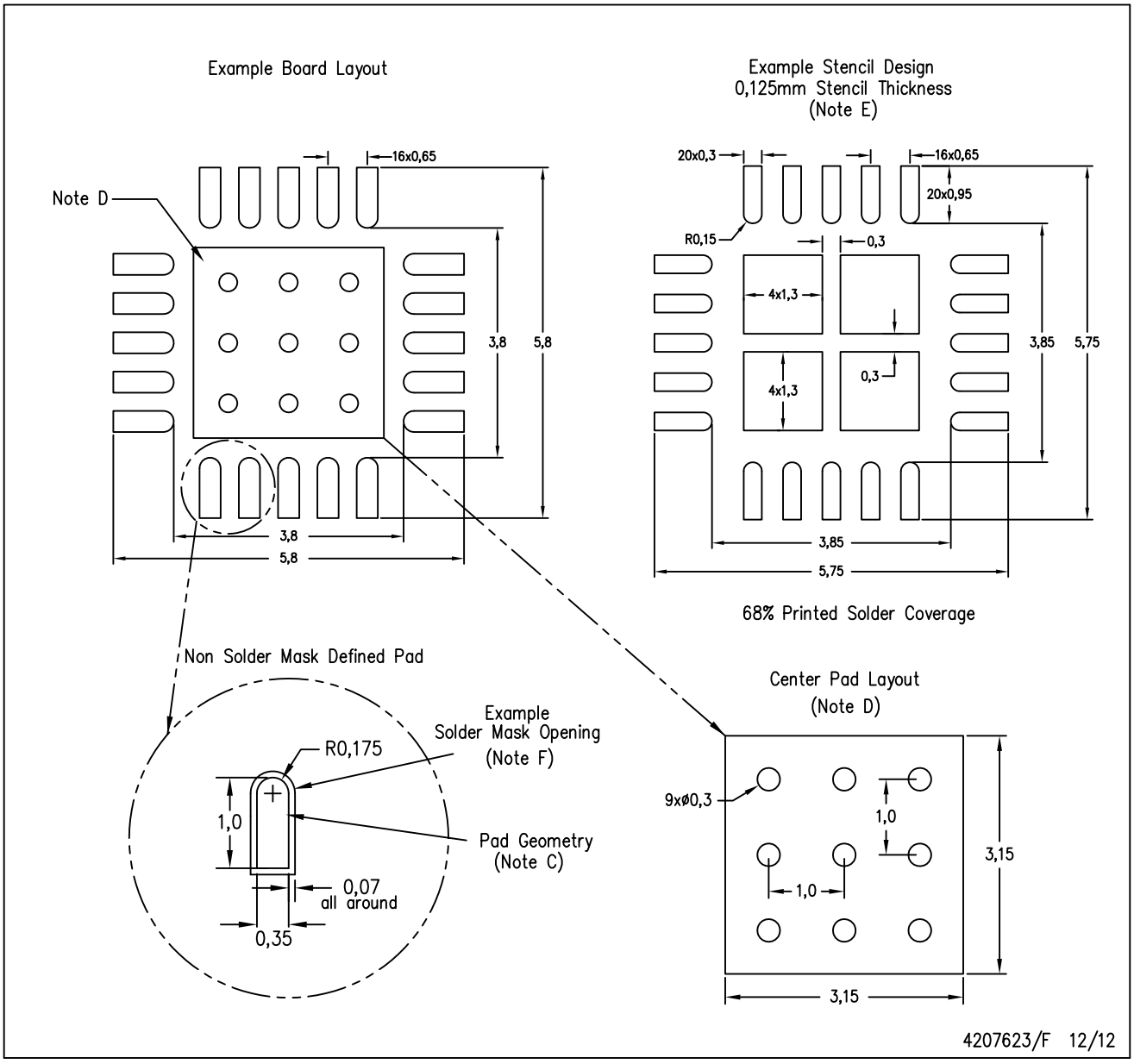

Bottom View

Exposed Thermal Pad Dimensions

4206352–2/K 12/12

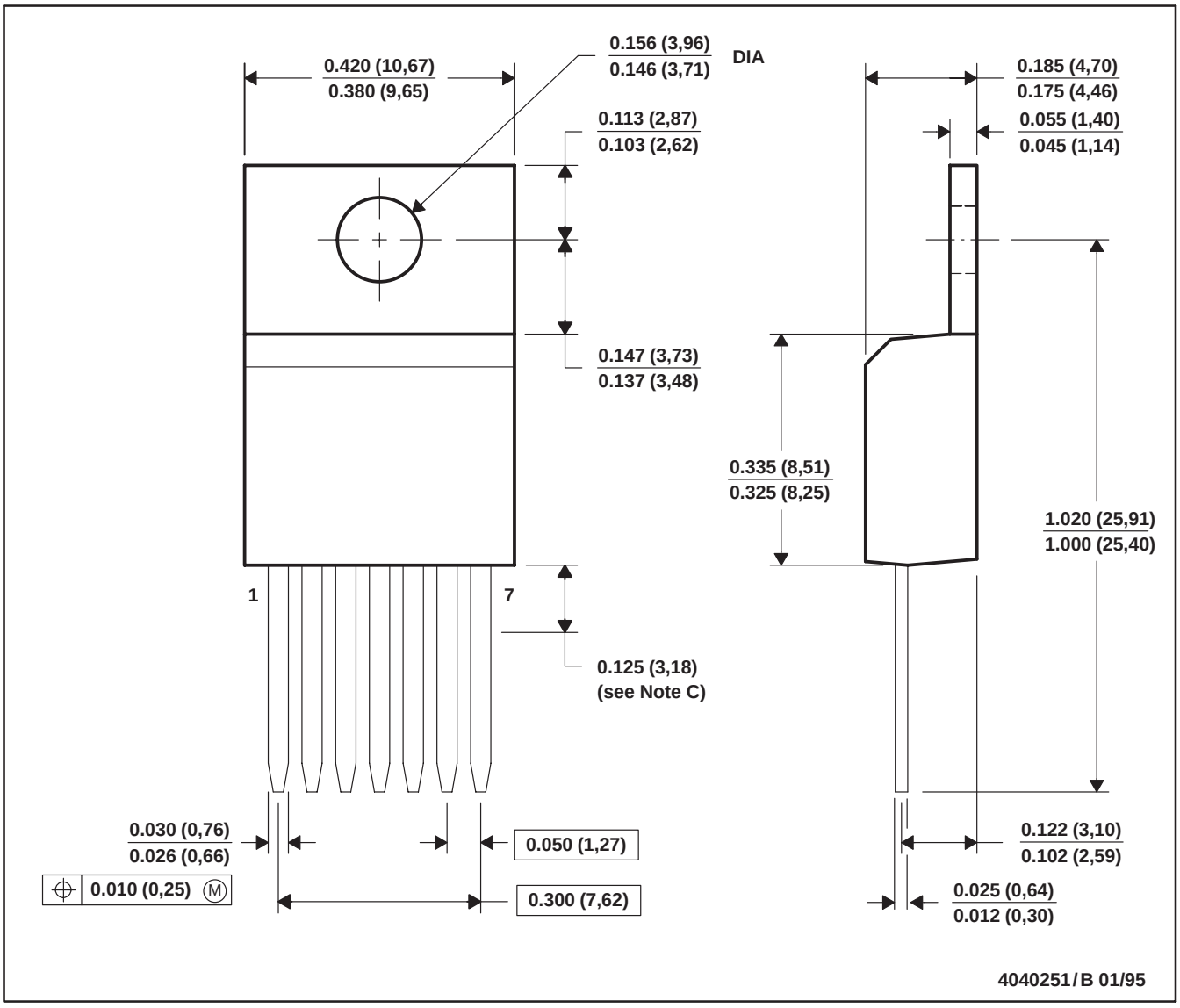
NOTE: All linear dimensions are in millimeters

# RGW (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

**KC (R-PSFM-T7)** **PLASTIC FLANGE-MOUNT PACKAGE**




NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Lead dimensions are not controlled within this area.
D. All lead dimensions apply before solder dip.
E. The center lead is in electrical contact with the mounting tab.

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