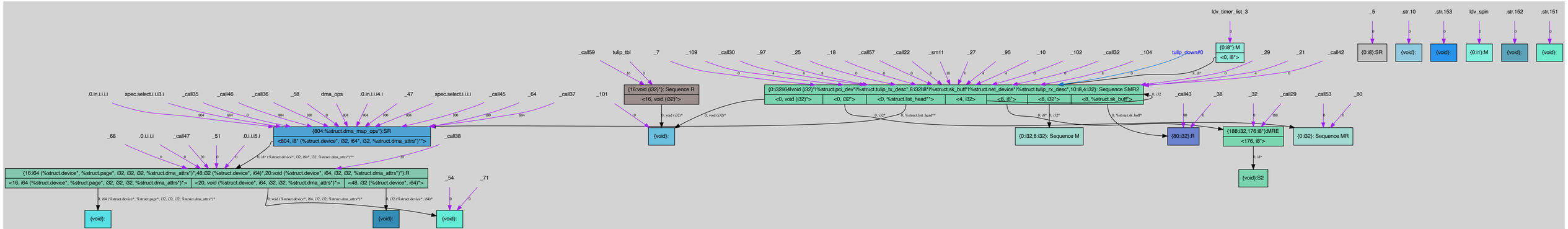
ldv_timer_list_3
{0:i8*}:M
<0, i8*>
_5
.str.10
.str.153
ldv_spin
.str.152
.str.151
{0:i8}:SR
{void}:
{void}:
{0:i1}:M
{void}:
{void}:
_call59
tulip_tbl
_7
_109
_call30
_97
_25
_18
_call57
_call22
_sm11
_27
_95
_10
_102
_call32
_104
tulip_down#0
_29
_21
_call42
{16:void (i32)*}: Sequence R
<16, void (i32)*>
{0:i32|i64|void (i32)*|1%struct.pci_dev*|%struct.tulip_tx_desc*,8:i32|i8*|1%struct.sk_buff*|%struct.net_device*|%struct.tulip_rx_desc*,10:i8,4:i32}: Sequence SMR2
<0, void (i32)*> | <0, i32*> | <0, %struct.list_head**> | <4, i32> | <8, i8*> | <8, i32*> | <8, %struct.sk_buff*>
.0.in.i.i.i.i
spec.select.i.i.i3.i
_call35
_call46
_call36
_58
dma_ops
.0.in.i.i.i4.i
_47
spec.select.i.i.i.i
_call45
_64
_call37
_101
_call43
_38
_32
_call29
_call53
_80
{804:%struct.dma_map_ops*}:SR
<804, i8* (%struct.device*, i32, i64*, i32, %struct.dma_attrs*)**>
{void}:
{0:i32,8:i32}: Sequence M
{80:i32}:R
{188:i32,176:i8*}:MRE
<176, i8*>
{0:i32}: Sequence MR
_68
.0.i.i.i.i
_call47
_51
.0.i.i.i5.i
_call38
{16:i64 (%struct.device*, %struct.page*, i32, i32, i32, %struct.dma_attrs*)*,48:i32 (%struct.device*, i64)*,20:void (%struct.device*, i64, i32, i32, %struct.dma_attrs*)*}:R
<16, i64 (%struct.device*, %struct.page*, i32, i32, i32, %struct.dma_attrs*)*> | <20, void (%struct.device*, i64, i32, i32, %struct.dma_attrs*)*> | <48, i32 (%struct.device*, i64)*>
{void}:S2
_54
_71
{void}:
{void}:
{void}: