

#### SOFTWARE ENGINEER | COMPUTER VISION RESEARCHER

5F., No. 336, Sec. 4, Chenggong Rd., Neihu Dist., Taipei City 114, Taiwan (R.O.C.)

□ (+886) 965-316-851 | sensibleoverwhelm@gmail.com | cheng-yao-hong

# **Education**

#### **National Taiwan University**

Taipei, Taiwan

M.S. IN ELECTRICAL AND COMPUTER ENGINEERING

Sep. 2014 - Aug. 2017

GPA: 4.01/4.3(scale)

• Thesis: Design of Timing-Error Detection and Correction System for Wide-Range Variation-Tolerant Microprocessors

### **National Chiao-Tung University**

Hsinchu, Taiwan

Sep. 2008 - Jun. 2012

**B.S. IN ELECTRONICS ENGINEERING** 

• **GPA:** 3.1/4.0(scale)

• Senior Project: Implementing Telematics for Enhanced Security and Real-Time Traffic Navigation

# **Selected Publications**

### **Peer-Reviewed Conference Papers**

- [1] **Cheng-Yao Hong**, Yu-Ying Chou, and Tyng-Luh Liu. Attention discriminant sampling for point clouds. In *IEEE/CVF International Conference on Computer Vision*, (*ICCV*), 2023.
- [2] Wan-Cyuan Fan\*, **Cheng-Yao Hong**\*, Yen-Chi Hsu, and Tyng-Luh Liu. IoU-aware multi-expert cascade network via dynamic ensemble for long-tailed object detection. In *IEEE International Conference on Acoustics, Speech and Signal Processing (ICASSP)*, 2023.
- [3] Chun-Hsiao Yeh, **Cheng-Yao Hong**, Yen-Chi Hsu, Tyng-Luh Liu, Yubei Chen, and Yann LeCun. Decoupled contrastive learning. In *17th European Conference on Computer Vision (ECCV)*, 2022.
- [4] Yen-Chi Hsu, **Cheng-Yao Hong**, Ming-Sui Lee, and Tyng-Luh Liu. Query-driven multi-instance learning. In *The Thirty-Fourth AAAI Conference on Artificial Intelligence (AAAI) (Spotlight)*, 2020.

### **Journal Article**

[1] Yen-Chi Hsu\*, **Cheng-Yao Hong\***, Ming-Sui Lee, Davi Geiger, Tyng-Luh Liu. ABC-Norm Regularization for Fine-Grained and Long-Tailed Image Classification. IEEE Transactions on Image Processing (TIP) 2023.

# Research Experience \_

## Academia Sinica, Institute of Information Science, Computer Vision Lab

Taipei, Taiwan

SOFTWARE ENGINEER | RESEARCH ASSISTANT

Jun. 2018 - Present

- · Proposed a token merging mechanism for the multimodal diffusion model, enhancing throughput by 2.9-fold.
- Enhanced face detection in sequential face manipulation by 5.22% through the application of MIL concepts.
- Proposed an attention-based sampling method for 3-D feature learning, enhancing performance by approximately 2% in several 3-D downstream tasks. (ICCV)
- Implemented a regularization-based method, achieving a 2.1% improvement in FGVC and long-tailed datasets. (TIP)
- Improved self-supervised learning accuracy in ImageNet by **5.1%** with a modified contrastive loss term.(ECCV)
- Formulated a multi-head-based approach for long-tailed object recognition, increasing mAP by increases 7% mAP in LVIS dataset.(ICASSP)
- Enhanced contrastive learning accuracy in ImageNet-100 by 2% via self-training and attention mechanisms. (ICASSP)
- Pioneered a neural architecture search algorithm, reducing computation time by 6%.(ICIP)
- · Developed an anchor-based approach for video summarization, competitive with leading methods. (ICIP)
- Innovated a weakly-supervised method, enhancing action recognition in video clips and MIML datasets (MNIST, CIFAR10, Scene) by (7.5%). (AAAI)

## University of California, Berkeley, Redwood Center for Theoretical Neuroscience

Online

RESEARCH INTERN

• Implemented the unsupervised learning algorithm for the audio framework.

June. 2021 - Aug. 2021

### National Taiwan University, Energy Efficient Circuit, and System Lab

Taipei, Taiwan Jan. 2017 - Apr. 2018

IC DESIGN ENGINEER · RESEARCH ASSISTANT

· Implemented an energy-efficient system using a deep learning algorithm and hardware co-optimization. (JSCC)

DECEMBER 1, 2023 CHENG-YAO HONG · RÉSUMÉ

## **Honors & Awards**

### INTERNATIONAL

2020	Silver, Top 2% (51/2265), Deepfake Detection Challenge	Kaggle
2020	<b>7th Place</b> , Large Vocabulary Instance Segmentation Challenge	Online
2019	<b>5th Place</b> , Large Vocabulary Instance Segmentation Challenge	Seoul, Korea

#### **DOMESTIC**

2020	<b>Scholarship</b> , Academia Sinica Scholarship for Young Scholars to Attend International Conferences.	Taipei, Taiwan
2020	<b>Scholarship</b> , Appier Award for Top Research in Artificial Intelligence and Information Technology.	Taipei, Taiwan

# **Academic Service**

CONFERENCE REVIEWER 2020 - Present

CVPR'21, ICCV'21, CVPR'22, ECCV'22, CVPR'23, ICCV'23, CVPR'24

# **Teaching Experience**

### **Advanced Integrated Circuit Design, National Taiwan University**

Taipei, Taiwan

TEACHING ASSISTANT, INSTRUCTED BY PROF. TSUNG-TE, LIU

Jan. 2017 - Apr. 2018

# **Selected Projects**

## **Deepfake Detection Challenge**

Taipei, Taiwan

Pytorch, python

Mar. 2020

- Deepfake techniques present realistic Al-generated videos of people doing and saying fictional things. The goal of the challenge is to build technologies that can help detect deepfakes and manipulated media.
- The proposed model, on the public dataset, gets the Top 2% in Deepfake Detection Challenge (DFDC) on Kaggle.

LVIS Challenge Taipei, Taiwan

PYTORCH, MMDECT AND PYTHON

Oct. 2019

- Addressed challenges in large-scale object detection with thousands of categories due to long-tail data distributions.
- Utilized non-local and semantic concepts; the proposed model achieved **30.2** mAP accuracy and secured 5th place in the International Conference on Computer Vision (ICCV) 2019.

### **Low Power Accelerator for Handwriting Number Recognition**

Taipei, Taiwan

VERILOG, DESIGN COMPILER, IC COMPILER

Jul. 2018

 Implemented the hardware of the trained model, employing techniques like memory hierarchy pruning and quantization to reduce power consumption.

# **Technical Strengths**

### **Deep learning and Computer vision:**

- Proficient in Python, C/C++, and Verilog
- · Experienced in developing algorithms using PyTorch, TensorFlow, MMDetection, Detetron2, OpenSelfSup, Pytorch3D, Diffuser

### IC design and Signal processing:

- Skilled in embedded system implementation and signal analysis using ARM DS-5 and Matlab
- Proficient in cell-based circuit design using Verilog Design Compiler and IC Compiler
- · Experienced in circuit design using Liberate, Spectre, and HSPICE

# **Full Publications**

## **Peer-Reviewed Conference Papers**

- [1] First Author. Promptable Token Merging. (Submitted), 2023.
- [2] First Author. Contrastive Learning for DeepFake Classification and Localization via Multi-Label Ranking. (Submitted), 2023.
- [3] **Cheng-Yao Hong**, Yu-Ying Chou and Tyng-Luh Liu. Attention Discriminant Sampling for Point Clouds. IEEE/CVF International Conference on Computer Vision, (ICCV), 2023.
- [4] Wan-Cyuan Fan\*, **Cheng-Yao Hong**\*, Yen-Chi Hsu and Tyng-Luh Liu. IoU-Aware Multi-Expert Cascade Network via Dynamic Ensemble for Long-tailed Object Detection. IEEE International Conference on Acoustics, Speech and Signal Processing (ICASSP), 2023.
- [5] Chun-Hsiao Yeh, **Cheng-Yao Hong**, Yen-Chi Hsu, Tyng-Luh Liu, Yubei Chen and Yann LeCun. Decoupled Contrastive Learning. 17th European Conference on Computer Vision (ECCV), 2022.
- [6] Chun-Hsiao Yeh\*, **Cheng-Yao Hong**\*, Yen-Chi Hsu\* and Tyng-Luh Liu. SAGA: Self-Augmentation with Guided Attentions for Representation Learning. IEEE International Conference on Acoustics, Speech and Signal Processing (ICASSP), 2022.
- [7] Jun-Liang\* Lin, Yi-Lin\* Sung, **Cheng-Yao Hong**\*, Han-Hung Lee and Tyng-Luh Liu. The Maximum a Posterior Estimation of Darts. IEEE International Conference on Image Processing, (ICIP), 2021.
- [8] Yi-Lin Sung, **Cheng-Yao Hong**, Yen-Chi Hsu and Tyng-Luh Liu. Video Summarization with Anchors and Multi-Head Attention. IEEE International Conference on Image Processing, (ICIP), 2020.
- [9] Yen-Chi Hsu, **Cheng-Yao Hong**, Ming-Sui Lee and Tyng-Luh Liu. The Thirty-Fourth AAAI Conference on Artificial Intelligence (AAAI) (**Spotlight**), 2020.

#### **Journal Article**

- [1] Yen-Chi Hsu\*, **Cheng-Yao Hong\***, Ming-Sui Lee, Davi Geiger and Tyng-Luh Liu. ABC-Norm Regularization for Fine-Grained and Long-Tailed Image Classification. IEEE Transactions on Image Processing (TIP), 2023.
- [2] **Cheng-Yao Hong** and Tsung-Te Liu. A Variation-Resilient Microprocessor With a Two-Level Timing Error Detection and Correction System in 28-nm CMOS. IEEE Journal of Solid-State Circuits 55.8 (JSSC), 2019.