RTL Design Sherpa

APB PM/ACPI Micro-Architecture Specification 1.0

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2 APB PM/ACPI - Overview

2.1 Introduction

The APB PM/ACPI controller provides ACPI-compatible power management functionality with an APB interface. It handles system power states, events, and timer functionality.

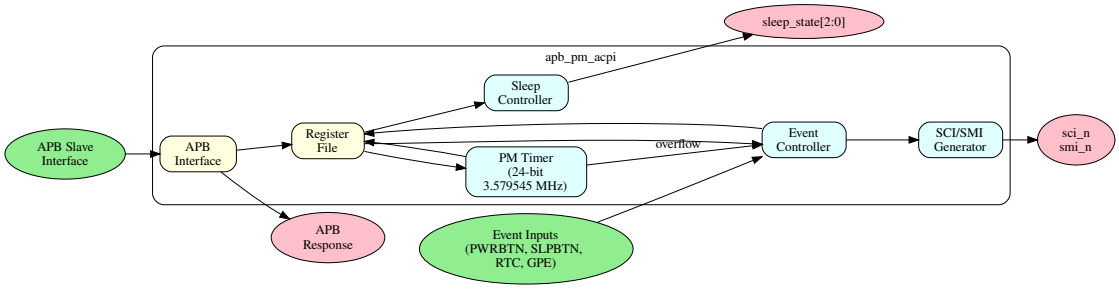
2.2 Key Features

- ACPI power management events
- PM1a/PM1b event blocks
- PM1 control block
- PM timer (24-bit, 3.579545 MHz)
- GPE (General Purpose Events) support
- System sleep state control
- Sci/SMI generation

2.3 Applications

- System power management
- Sleep state transitions (S0-S5)
- Wake event handling
- Power button events
- Thermal events

2.4 Block Diagram

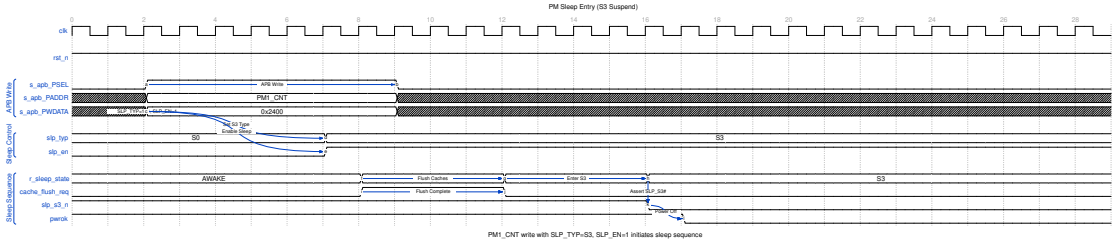


PM/ACPI Block Diagram

2.5 Timing Diagrams

2.5.1 Sleep Entry (S3 Suspend)

Software initiates sleep by writing to PM1_CNT.

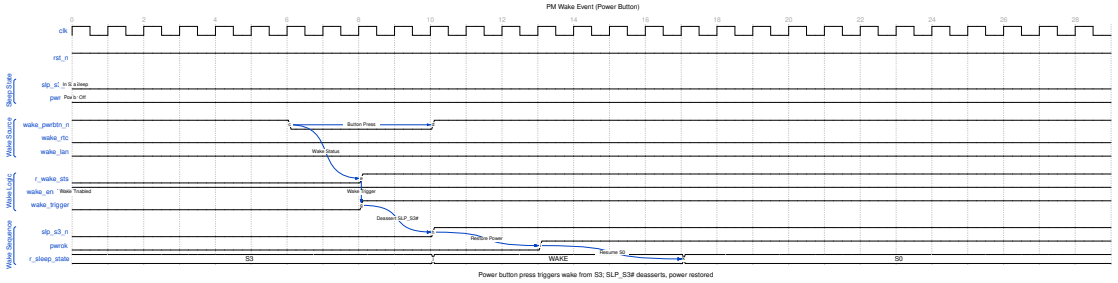


PM Sleep Entry

The sequence: 1. OS writes PM1_CNT with SLP_TYP (sleep type) and SLP_EN (enable) 2. PM controller initiates cache flush 3. Asserts SLP_S3# signal 4. Power removed from non-essential components

2.5.2 Wake Event

Power button or other source triggers wake from sleep.

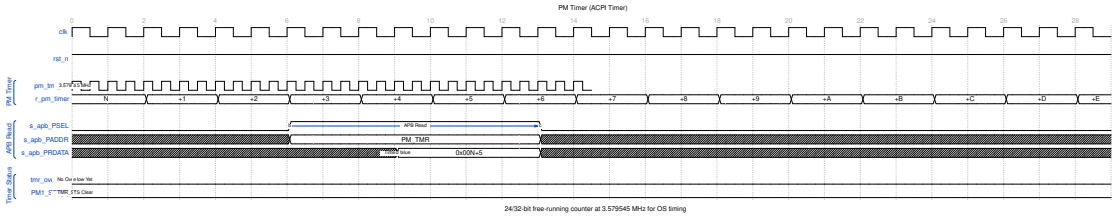


PM Wake Event

Wake sequence: 1. Wake source detected (power button, RTC alarm, LAN, etc.) 2. Wake status latched 3. SLP_Sx# deasserted 4. Power restored, system resumes to S0

2.5.3 PM Timer

ACPI timer for OS timing services.

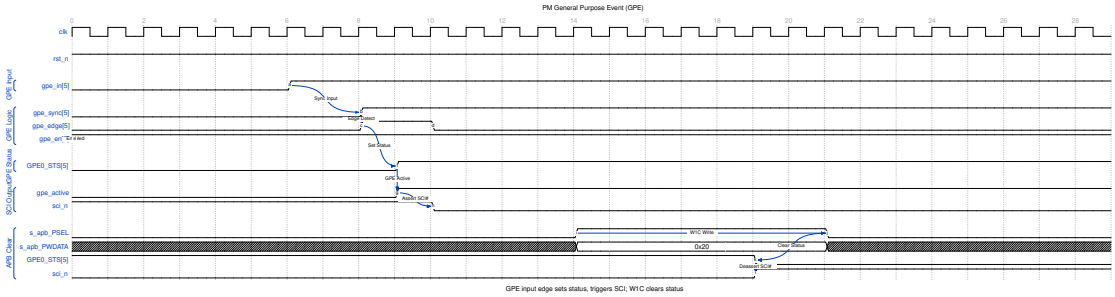


PM Timer

The 24-bit (or 32-bit) free-running counter clocked at 3.579545 MHz provides high-resolution timing for the OS. Timer overflow generates TMR_STS if enabled.

2.5.4 General Purpose Event (GPE)

External events trigger SCI interrupt to OS.



PM GPE Event

GPE input edge sets status bit, which triggers SCI# if enabled. OS reads status, handles event, then writes 1-to-clear the status bit.

2.6 Register Summary

Offset	Name	Description
0x00	PM1_STS	PM1 Event Status
0x04	PM1_EN	PM1 Event Enable
0x08	PM1_CNT	PM1 Control
0x0C	PM_TMR	PM Timer (24-bit)
0x10	GPE0_STS	GPE0 Status

Offset	Name	Description
0x14	GPE0_EN	GPE0 Enable
0x18	GPE1_STS	GPE1 Status
0x1C	GPE1_EN	GPE1 Enable

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3 APB PM/ACPI - Register Map

3.1 Register Summary

Offset	Name	Access	Description
0x00	PM1_STS	RO/W1C	PM1 Status
0x04	PM1_EN	RW	PM1 Enable
0x08	PM1_CNT	RW	PM1 Control
0x0C	PM_TMR	RO	PM Timer
0x10	GPE0_STS	RO/W1C	GPE0 Status
0x14	GPE0_EN	RW	GPE0 Enable
0x18	GPE1_STS	RO/W1C	GPE1 Status
0x1C	GPE1_EN	RW	GPE1 Enable

3.2 PM1_STS (0x00)

Bit	Name	Access	Description
0	TMR_STS	W1C	Timer overflow status
4	BM_STS	W1C	Bus master status

Bit	Name	Access	Description
5	GBL_STS	W1C	Global release status
8	PWRBTN_STS	W1C	Power button status
9	SLPBTN_STS	W1C	Sleep button status
10	RTC_STS	W1C	RTC alarm status
15	WAK_STS	W1C	Wake status

3.3 PM1_EN (0x04)

Bit	Name	Access	Description
0	TMR_EN	RW	Timer overflow enable
5	GBL_EN	RW	Global release enable
8	PWRBTN_EN	RW	Power button enable
9	SLPBTN_EN	RW	Sleep button enable
10	RTC_EN	RW	RTC alarm enable

3.4 PM1_CNT (0x08)

Bit	Name	Access	Description
0	SCI_EN	RW	SCI enable
1	BM_RLD	RW	Bus master reload
2	GBL_RLS	RW	Global release
12:10	SLP_TYP	RW	Sleep type

Bit	Name	Access	Description
13	SLP_EN	RW	Sleep enable

3.5 PM_TMR (0x0C)

Bits	Name	Access	Description
23:0	TMR_VAL	RO	Timer value (3.579545 MHz)

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