RTL Design Sherpa

APB SMBus Micro-Architecture Specification 1.0

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2 APB SMBus - Overview

2.1 Introduction

The APB SMBus controller provides System Management Bus communication with APB interface. It supports host controller functionality for accessing SMBus devices.

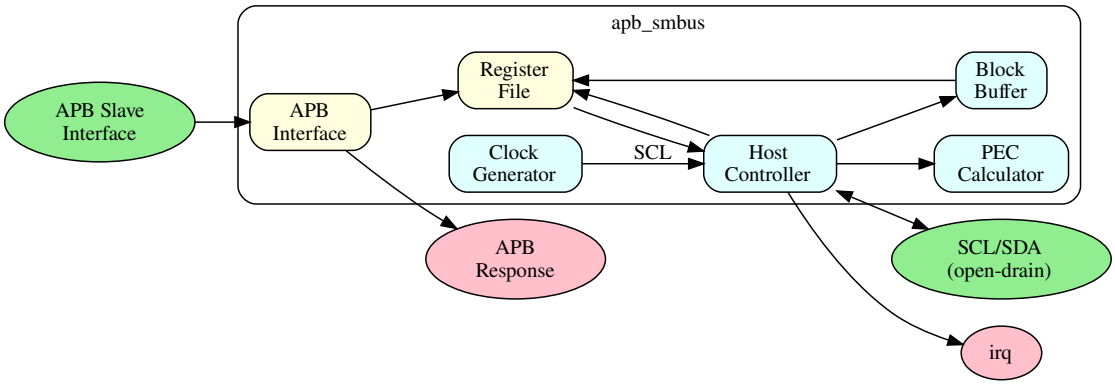
2.2 Key Features

- SMBus 2.0 compatible
- Host controller mode
- Quick Command, Send/Receive Byte
- Read/Write Byte/Word
- Block Read/Write (up to 32 bytes)
- PEC (Packet Error Checking) support
- Programmable clock divider
- Interrupt-driven operation
- Timeout detection

2.3 Applications

- Temperature monitoring
- Voltage monitoring
- Fan control
- EEPROM access
- Power management
- System health monitoring

2.4 Block Diagram

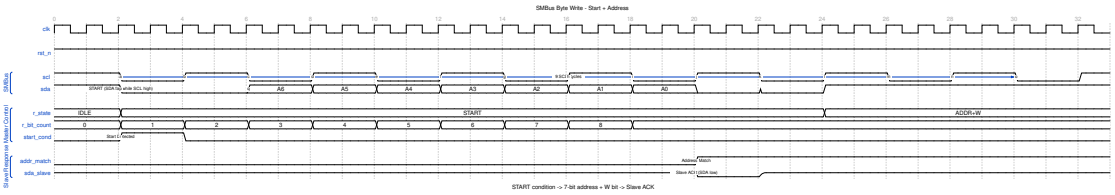


SMBus Block Diagram

2.5 Timing Diagrams

2.5.1 Byte Write (Start + Address)

Shows the START condition and 7-bit address transmission.

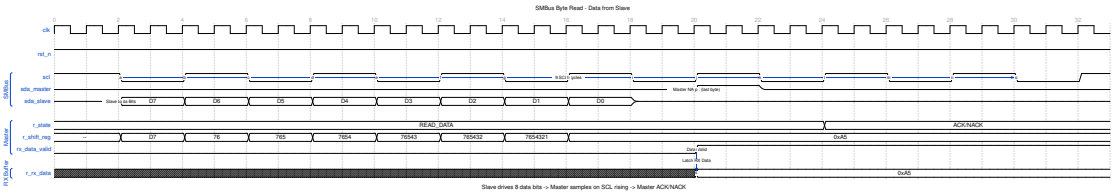


SMBus Byte Write

START condition is SDA falling while SCL is high. The 7-bit slave address plus R/W bit is clocked out, followed by slave ACK (SDA low during 9th clock).

2.5.2 Byte Read

Shows slave-to-master data transfer.

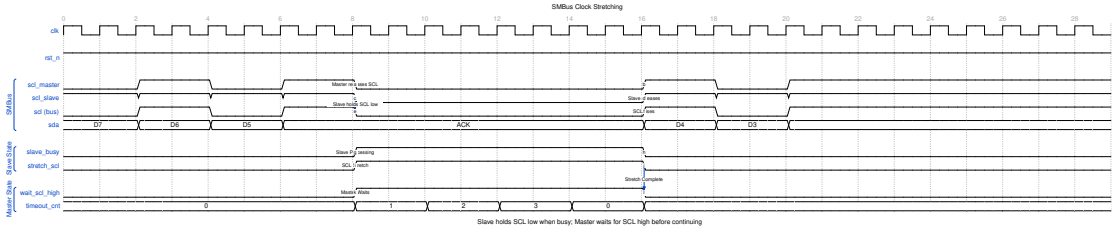


SMBus Byte Read

Slave drives 8 data bits while master clocks SCL. Master samples each bit on SCL rising edge, then provides ACK (more data) or NACK (last byte).

2.5.3 Clock Stretching

Slave flow control by holding SCL low.

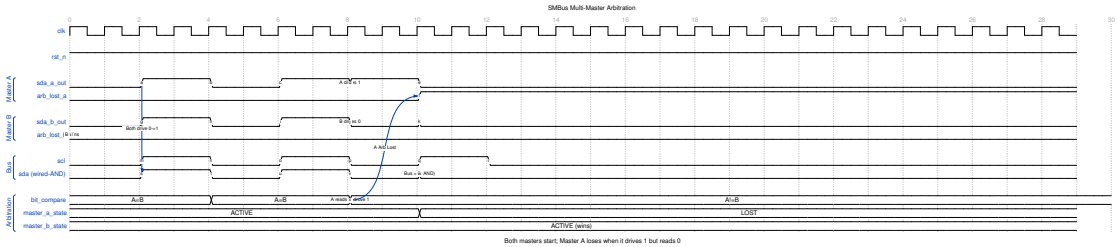


SMBus Clock Stretch

When the slave needs processing time, it holds SCL low after the master releases it. Master waits for SCL to rise before continuing. This provides backpressure without data loss.

2.5.4 Multi-Master Arbitration

Collision detection when multiple masters start simultaneously.

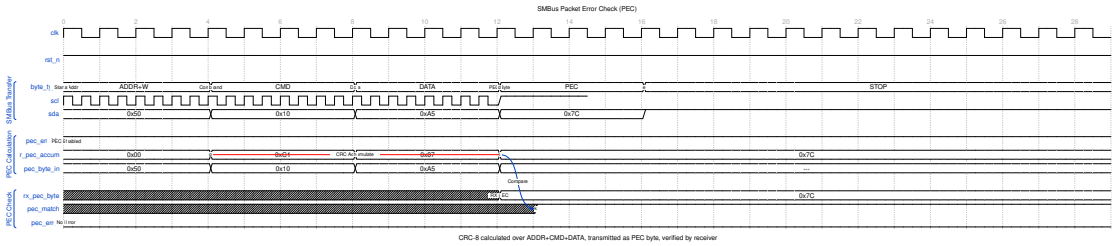


SMBus Arbitration

Both masters monitor SDA while transmitting. If a master drives 1 but reads 0 (wired-AND bus), it loses arbitration and backs off. The winner continues the transaction.

2.5.5 Packet Error Check (PEC)

CRC-8 error detection for data integrity.



SMBus PEC

PEC is calculated over address, command, and data bytes using CRC-8. The PEC byte is transmitted after data and verified by the receiver to detect transmission errors.

2.6 Register Summary

Offset	Name	Description
0x00	SMBUS_STATUS	Status register
0x04	SMBUS_CONTROL	Control register
0x08	SMBUS_COMMAND	Command type
0x0C	SMBUS_ADDRESS	Target address
0x10	SMBUS_DATA0	Data byte 0
0x14	SMBUS_DATA1	Data byte 1
0x18	SMBUS_BLOCK	Block data count
0x1C	SMBUS_PEC	PEC value
0x20	SMBUS_AUXCTL	Auxiliary control
0x80-0x9F	SMBUS_BLOCKDATA	Block data buffer

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3 APB SMBus - Register Map

3.1 Register Summary

Offset	Name	Access	Description
0x00	SMBUS_STATUS	RO/W1C	Status
0x04	SMBUS_CONTROL	RW	Control
0x08	SMBUS_COMMAND	RW	Command byte
0x0C	SMBUS_ADDRESS	RW	Slave address
0x10	SMBUS_DATA0	RW	Data byte 0
0x14	SMBUS_DATA1	RW	Data byte 1
0x18	SMBUS_BLOCK_CNT	RW	Block count
0x1C	SMBUS_PEC	RO	PEC value
0x20	SMBUS_AUXCTL	RW	Auxiliary control
0x80-0x9F	SMBUS_BLOCK_DATA	RW	Block buffer (32 bytes)

3.2 SMBUS_STATUS (0x00)

Bit	Name	Access	Description
0	BUSY	RO	Transaction in progress
1	INTR	W1C	Interrupt pending
2	DEV_ERR	W1C	Device error
3	BUS_ERR	W1C	Bus error
4	FAILED	W1C	Transaction failed

Bit	Name	Access	Description
5	ALERT	W1C	SMBus alert received
6	TIMEOUT	W1C	Timeout occurred
7	PEC_ERR	W1C	PEC error

3.3 SMBUS_CONTROL (0x04)

Bit	Name	Access	Description
2:0	CMD_TYPE	RW	Command type
3	START	RW	Start transaction
4	PEC_EN	RW	Enable PEC
5	INTREN	RW	Enable interrupt
6	KILL	RW	Abort transaction
7	RESET	RW	Soft reset

3.3.1 Command Types

CMD_TYPE	Description
000	Quick Command
001	Send Byte
010	Receive Byte
011	Write Byte
100	Read Byte
101	Write Word
110	Read Word
111	Block Read/Write

3.4 SMBUS_ADDRESS (0x0C)

Bits	Name	Description
6:0	ADDR	7-bit slave address
7	RW	0=Write, 1=Read

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