

# Table of Contents

## Smbus Index

**Generated:** 2025-12-06

## APB SMBus Specification - Table of Contents

**Component:** APB System Management Bus (SMBus) Controller **Version:** 1.0 **Last Updated:** 2025-12-01 **Status:** Production Ready

---

### Document Organization

#### Chapter 1: Overview

- [01\\_overview.md](#) - Component overview
- [02\\_architecture.md](#) - Architecture

#### Chapter 2: Blocks

- [00\\_overview.md](#) - Block hierarchy

#### Chapter 3: Interfaces

- [00\\_overview.md](#) - Interface summary

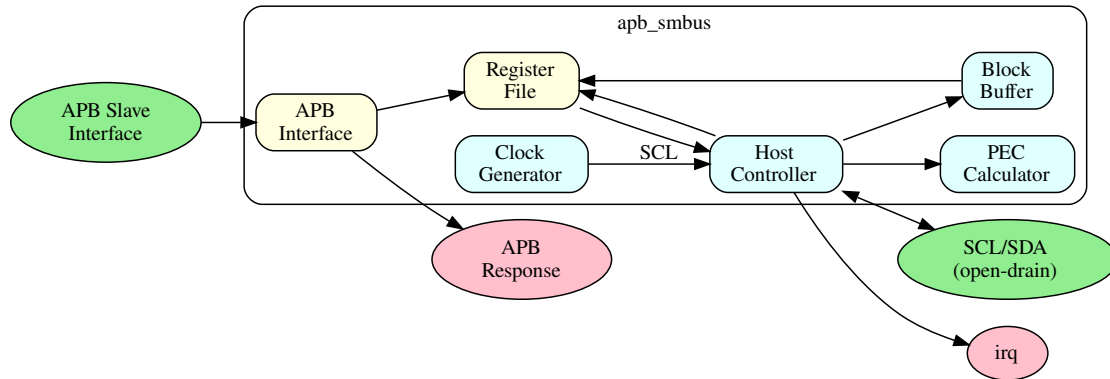
#### Chapter 4: Programming Model

- [00\\_overview.md](#) - Programming overview

#### Chapter 5: Registers

- [01\\_register\\_map.md](#) - Register map
-

## Block Diagram



### SMBus Block Diagram

---

## Version History

Version	Date	Author	Changes
1.0	2025-12-01	RTL Design Sherpa	Initial specification

## APB SMBus - Overview

### Introduction

The APB SMBus controller provides System Management Bus communication with APB interface. It supports host controller functionality for accessing SMBus devices.

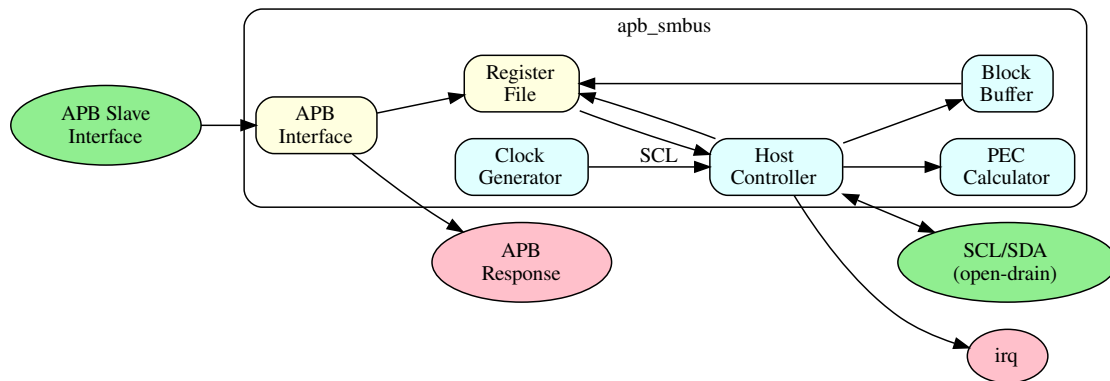
### Key Features

- SMBus 2.0 compatible
- Host controller mode
- Quick Command, Send/Receive Byte
- Read/Write Byte/Word
- Block Read/Write (up to 32 bytes)
- PEC (Packet Error Checking) support
- Programmable clock divider
- Interrupt-driven operation
- Timeout detection

## Applications

- Temperature monitoring
- Voltage monitoring
- Fan control
- EEPROM access
- Power management
- System health monitoring

## Block Diagram



### *SMBus Block Diagram*

## Register Summary

Offset	Name	Description
0x00	SMBUS_STATUS	Status register
0x04	SMBUS_CONTROL	Control register
0x08	SMBUS_COMMAND	Command type
0x0C	SMBUS_ADDRESS	Target address
0x10	SMBUS_DATA0	Data byte 0
0x14	SMBUS_DATA1	Data byte 1
0x18	SMBUS_BLOCK	Block data count
0x1C	SMBUS_PEC	PEC value
0x20	SMBUS_AUXCTL	Auxiliary control
0x80-0x9F	SMBUS_BLOCKDATA	Block data buffer

Next: [02\\_architecture.md](#)

## APB SMBus - Register Map

### Register Summary

Offset	Name	Access	Description
0x00	SMBUS_STATU S	RO/W1C	Status
0x04	SMBUS_CONTR OL	RW	Control
0x08	SMBUS_COMM AND	RW	Command byte
0x0C	SMBUS_ADDRE SS	RW	Slave address
0x10	SMBUS_DATA0	RW	Data byte 0
0x14	SMBUS_DATA1	RW	Data byte 1
0x18	SMBUS_BLOCK _CNT	RW	Block count
0x1C	SMBUS_PEC	RO	PEC value
0x20	SMBUS_AUXCT L	RW	Auxiliary control
0x80-0x9F	SMBUS_BLOCK _DATA	RW	Block buffer (32 bytes)

### SMBUS\_STATUS (0x00)

Bit	Name	Access	Description
0	BUSY	RO	Transaction in progress
1	INTR	W1C	Interrupt pending
2	DEV_ERR	W1C	Device error
3	BUS_ERR	W1C	Bus error
4	FAILED	W1C	Transaction failed
5	ALERT	W1C	SMBus alert received

Bit	Name	Access	Description
6	TIMEOUT	W1C	Timeout occurred
7	PEC_ERR	W1C	PEC error

### SMBUS\_CONTROL (0x04)

Bit	Name	Access	Description
2:0	CMD_TYPE	RW	Command type
3	START	RW	Start transaction
4	PEC_EN	RW	Enable PEC
5	INTREN	RW	Enable interrupt
6	KILL	RW	Abort transaction
7	RESET	RW	Soft reset

### Command Types

CMD_TYPE	Description
000	Quick Command
001	Send Byte
010	Receive Byte
011	Write Byte
100	Read Byte
101	Write Word
110	Read Word
111	Block Read/Write

### SMBUS\_ADDRESS (0x0C)

Bits	Name	Description
6:0	ADDR	7-bit slave address
7	RW	0=Write, 1=Read

**Back to:** [SMBus Specification Index](#)