RTL Design Sherpa

APB PIC 8259 Micro-Architecture Specification 1.0

January 4, 2026

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2 APB PIC 8259 - Overview

2.1 Introduction

The APB PIC 8259 is an 8259A-compatible Programmable Interrupt Controller with an APB interface. It provides interrupt management for legacy PC-compatible systems.

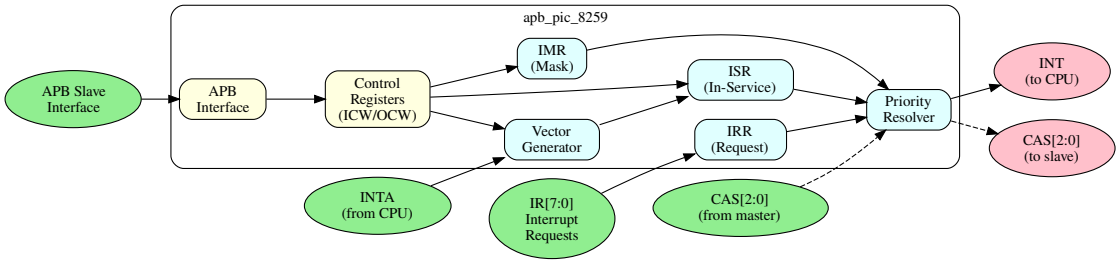
2.2 Key Features

- 8 interrupt inputs per controller
- Master/Slave cascade support
- Programmable priority modes
- Edge or level triggering
- Automatic EOI option
- Interrupt masking
- Polling mode support
- Special fully nested mode

2.3 Applications

- PC-compatible interrupt management
- Legacy device support
- x86 system integration

2.4 Block Diagram

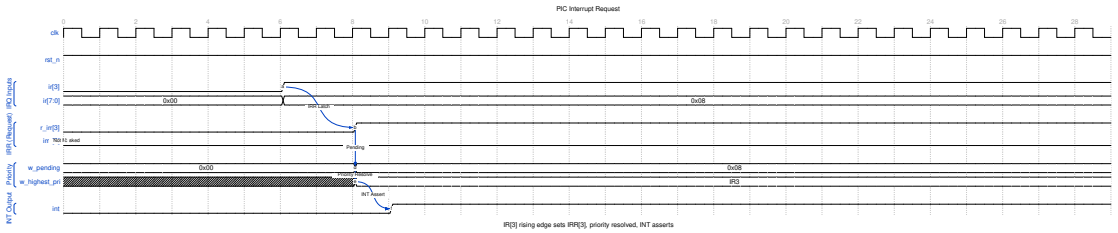


PIC 8259 Block Diagram

2.5 Timing Diagrams

2.5.1 Interrupt Request

Shows an IRQ input assertion triggering the interrupt process.

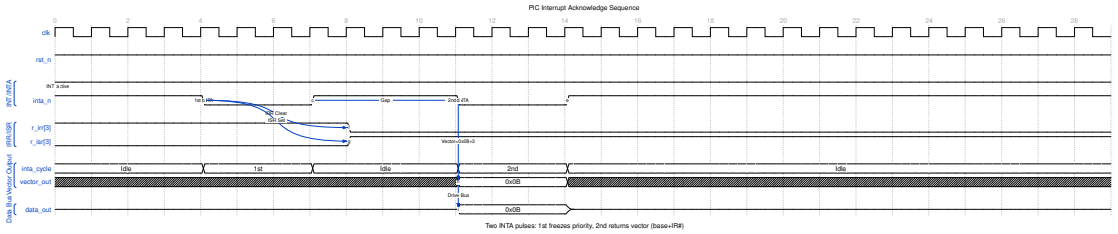


PIC Interrupt Request

When an IR pin asserts, the corresponding IRR bit is set. The priority resolver selects the highest priority unmasked interrupt and asserts INT to the CPU.

2.5.2 Interrupt Acknowledge Sequence

The two-pulse INTA sequence from CPU to PIC.

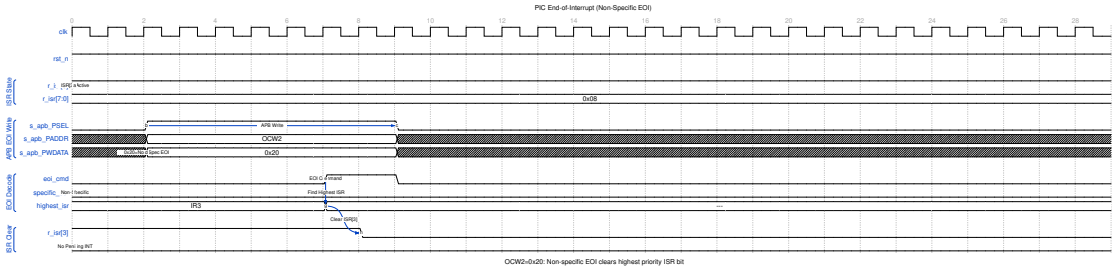


PIC Interrupt Acknowledge

On the first INTA pulse, priority is frozen and IRR transfers to ISR. On the second INTA pulse, the PIC outputs the interrupt vector (base + IR number) on the data bus.

2.5.3 End-of-Interrupt (EOI)

Software clears the in-service bit with an EOI command.

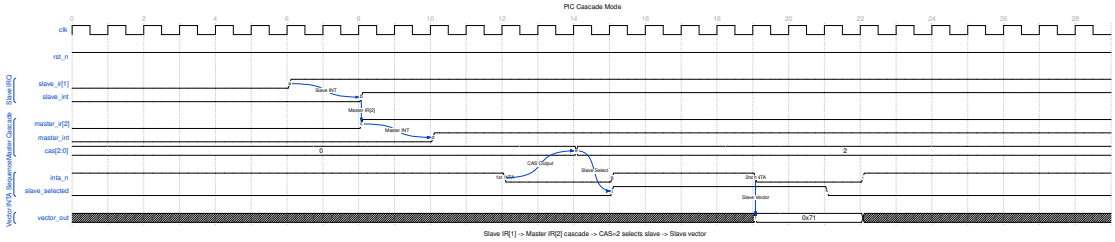


PIC EOI

Non-specific EOI (0x20) clears the highest priority ISR bit. Specific EOI (0x60-0x67) clears a designated IR.

2.5.4 Cascade Mode

Master-slave configuration for 15 IRQ sources.

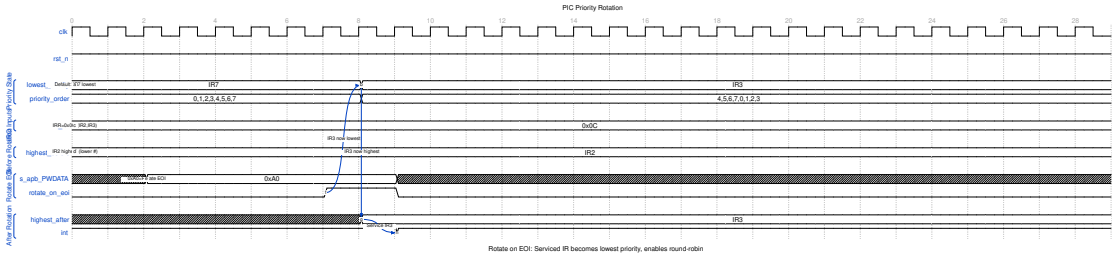


PIC Cascade

Slave INT connects to master IR2. During INTA, master outputs cascade select (CAS) lines. Slave with matching ID provides the interrupt vector.

2.5.5 Priority Rotation

Automatic priority rotation for equal-service scheduling.



PIC Priority Rotation

Rotate-on-EOI (0xA0) makes the just-serviced IR the lowest priority, implementing round-robin scheduling among interrupt sources.

2.6 Register Summary

Offset	A0	Read	Write
0x00	0	IRR/ISR	ICW1/OCW2/ OCW3
0x04	1	IMR	ICW2/ICW3/ ICW4/OCW1

2.7 Interrupt Priority

IRQ	Default Priority
IR0	Highest (0)
IR1	1
IR2	2 (cascade in master)
IR3	3
IR4	4
IR5	5
IR6	6
IR7	Lowest (7)

2.8 Priority Modes

- **Fixed Priority**: IR0 highest, IR7 lowest
- **Rotating Priority**: Lowest priority rotates after EOI
- **Specific Priority**: Programmable lowest priority

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3 APB PIC 8259 - Register Map

3.1 Register Access

Offset	A0	Read	Write
0x00	0	IRR/ISR (OCW3 select)	ICW1 / OCW2 / OCW3
0x04	1	IMR	ICW2 / ICW3 / ICW4 / OCW1

3.2 Initialization Command Words (ICW)

3.2.1 ICW1 (Address 0x00, Write)

Bit	Name	Description
0	IC4	ICW4 needed
1	SNGL	Single mode (no cascade)
2	ADI	Call address interval
3	LTIM	Level triggered mode
4	1	Must be 1 (identifies ICW1)
7:5	A7-A5	Interrupt vector address (MCS-80)

3.2.2 ICW2 (Address 0x04, Write after ICW1)

Bits	Name	Description
7:3	T7-T3	Interrupt vector base address
2:0	A10-A8	Address bits (MCS-80 only)

3.2.3 ICW3 (Address 0x04, Write if cascade)

Master: | Bits | Description | |——|————-| | 7:0 | S7-S0: 1=slave on IR[n] |

Slave: | Bits | Description | |——|————-| | 2:0 | Slave ID (0-7) |

3.2.4 ICW4 (Address 0x04, Write if IC4=1)

Bit	Name	Description
0	uPM	1=8086 mode, 0=MCS-80
1	AEOI	Auto EOI mode
2	M/S	Master(1)/Slave(0) buffer
3	BUF	Buffered mode
4	SFNM	Special fully nested mode

3.3 Operation Command Words (OCW)

3.3.1 OCW1 - IMR (Address 0x04)

Bits	Description
7:0	Interrupt mask (1=masked)

3.3.2 OCW2 (Address 0x00)

Bits	Name	Description
2:0	L2-L0	IR level for specific EOI
4:3	00	OCW2 identifier
7:5	R,SL,EOI	EOI command type

EOI Commands: | R | SL | EOI | Command | |—|—-|—-|———| | 0 | 0 | 1 | Non-specific EOI | | 0 | 1 | 1 | Specific EOI | | 1 | 0 | 1 | Rotate on non-specific EOI | | 1 | 1 | 1 | Rotate on specific EOI | | 1 | 0 | 0 | Set priority (L=lowest) | | 1 | 1 | 0 | Rotate on auto EOI (set) | | 0 | 0 | 0 | Rotate on auto EOI (clear) |

3.3.3 OCW3 (Address 0x00)

Bits	Name	Description
1:0	RIS,RR	Read register select
2	P	Poll command
4:3	01	OCW3 identifier

Bits	Name	Description
6:5	ESMM,SMM	Special mask mode

3.4 Internal Registers

3.4.1 IRR (Interrupt Request Register)

Bits set when interrupt requested, cleared when acknowledged.

3.4.2 ISR (In-Service Register)

Bits set when interrupt acknowledged, cleared by EOI.

3.4.3 IMR (Interrupt Mask Register)

1 = Interrupt masked (disabled).

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