

APB HPET Specification - Table of Contents

Component: APB High Precision Event Timer (HPET) **Version:** 1.0 **Last Updated:** 2025-10-18 **Status:** Production Ready (5/6 configurations 100% passing)

Document Organization

This specification is organized into five chapters covering all aspects of the APB HPET component:

Chapter 1: Overview

Location: ch01_overview/

- 01_overview.md - Component overview, features, applications
- 02_architecture.md - High-level architecture and block hierarchy
- 03_clocks_and_reset.md - Clock domains and reset behavior
- 04_acronyms.md - Acronyms and terminology
- 05_references.md - External references and standards

Chapter 2: Blocks

Location: ch02_blocks/

- 00_overview.md - Block hierarchy overview
- 02_hpet_config_regs.md - Configuration register wrapper
- 03_hpet_regs.md - PeakRDL generated register file
- 04_apb_hpet_top.md - Top-level integration
- 05_fsm_summary.md - FSM state summary table

PlantUML Diagrams: puml/ - hpet_core_fsm.puml - HPET core timer FSM
- timer_config_fsm.puml - Timer configuration FSM

Chapter 3: Interfaces

Location: ch03_interfaces/

- 01_top_level.md - Top-level signal list
- 02_apb_interface_spec.md - APB protocol specification
- 03_hpet_clock_interface.md - HPET clock domain interface
- 04_interrupt_interface.md - Timer interrupt outputs

Chapter 4: Programming Model

Location: ch04_programming/

- 01_initialization.md - Software initialization sequence

- 03_interrupt_handling.md - Interrupt service routines
- 04_use_cases.md - Common use case examples

Chapter 5: Registers

Location: ch05_registers/

- 01_register_map.md - Complete register address map and field descriptions
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Quick Navigation

For Software Developers

- Start with Chapter 4: Programming Model
- Reference Chapter 5: Registers

For Hardware Integrators

- Start with Chapter 1: Overview
- Reference Chapter 3: Interfaces

For Verification Engineers

- Start with Chapter 2: Blocks
- Reference FSM Summary

For System Architects

- Start with Architecture Overview
 - Reference Use Cases
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Document Conventions

Notation

- **bold** - Important terms, signal names
- `code` - Register names, field names, code examples
- *italic* - Emphasis, notes

Signal Naming

- pclk - APB clock
- hpet_clk - HPET timer clock
- timer_irq[N] - Timer interrupt outputs

Register Notation

- HPET_CONFIG - Register name
 - HPET_CONFIG[0] - Specific bit field
 - 0x000 - Register address (hexadecimal)
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Version History

Version	Date	Author	Changes
1.0	2025-10-18	RTL Design Sherpa	Initial specification based on production-ready implementation

Related Documentation: - PRD.md - Product Requirements Document -
CLAUDE.md - AI integration guide - TASKS.md - Development tasks and status
- IMPLEMENTATION_STATUS.md - Test results and validation status