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*Click **here** to ask an associate for production status of specific part numbers.*

MAX96712/B

Quad GMSL2 to CSI-2 Deserializer with GMSL1 Compatibility

General Description

The MAX96712/B deserializer converts four GMSL™ inputs into MIPI CSI-2 D/C-PHY outputs. Links receive bidirectional control data and forward video simultaneously over industry-standard coax or shielded twisted-pair (STP) cables. This device supports up to 6G/187Mbps GMSL2 data and up to 3.125Gbps of GMSL1 data.

The MAX96712/B supports video data aggregation to a single output. Alternatively, multiple sensors can be synchronized and concatenated into a single superframe. Data routing via virtual channel IDs or data type enables demultiplexing of streams to independent CSI-2 outputs. The CSI-2 interface supports 2x4 and 4x2 lane configurations and can replicate data on identical ports.

Three I^2C/UART ports support redundant, immediate, local access and any combination of remote serializer, peripheral or tunneled peripheral communication. Two SPI ports and several GPIOs provide tunneling interfaces to remote peripherals (GMSL2).

Contact the factory for the GMSL2 Channel Specification.

Table 1. Typical Maximum Cable Length vs. Attenuation

	3.2mm Ø 50Ω Coax, Foam Dielectric	2.7mm Ø 50Ω Coax, Solid Dielectric	100Ω Shielded Twisted Pair, AWG26
Attenuation at 3GHz (Typ, Room Temp)	0.9dB/m	1.6dB/m	1.8dB/m
Attenuation at 3GHz (Max, Aged, +105°C)	1.1dB/m	2.0dB/m	2.2dB/m
GMSL Fwd/Rev Data Rate	**Typical Maximum Cable Length at +105°C**		
3Gbps/187.5Mbps	20m	10m	11m
6Gbps/187.5Mbps	15m	9m	8m

Applications

- High-Resolution Camera Systems
  - Rear-View Cameras
  - Driver Monitoring Systems
  - Gesture Cameras
- Safety Critical ADAS/Autonomous Driving Sensors
  - RADAR
  - LIDAR
  - Surround-View Cameras
  - High-Resolution Cameras
- Synchronized Multisensor Systems

Benefits and Features

- MIPI CSI-2 v1.3 Output Configurable as 2x4 Lane, 1x4 Lane + 2x2 Lane, or 4x2 Lane
  - Selectable D-PHY v1.2 at 80Mbps to 2.5Gbps/lane or C-PHY v1.0 at 182Mbps to 5.7Gbps/lane
  - 16/32-Channel Virtual Channel Support (D/C-PHY)
  - Flexible Aggregation and Routing of Incoming Data via CSI-2 VC or Frame Concatenation
  - Data can be Replicated and Routed to any CSI Port
  - Supports RAW8/10/12/14/16/20, RGB565/666/888, YUV422 8/10-Bit Formats
  - Double Pixel Mode for Transmission Efficiency
  - CSI-2 Lane Reassignment and Polarity Flip
  - MIPI/GMSL Video PRBS Generator and Checker
  - Checkerboard/Color Gradient Pattern Generator
  - Raw CSI-2 PRBS Generator
  - Independent Configuration of all Video Paths and GMSL/CSI-2 Ports
- Quad GMSL Inputs with Independently Configurable GMSL1/2 Operation, Link Speed, and Video Format
  - Mixed GMSL1/GMSL2 and 3G/6G Support
  - Backward compatible with GMSL1 Serializers
  - GMSL1 Forward Link Speed up to 3.12Gbps
  - GMSL2 Link Speed of 3Gbps or 6Gbps (Forward) and 187.5Mbps (Reverse)
  - Simultaneous Support of Both Synchronized and Non-Synchronized Cameras
  - Precisely Synchronizes Multiple Serializers
  - GMSL PRBS Generator/Checker for Link Testing
  - Eye-Opening Monitor for Continuous Diagnostics
  - Adaptive Equalization Enables up to 15m Coax Cable with Multiple In-Line Connectors
  - Compatible with 50Ω Coax or 100Ω STP
- RoR for Crystal-Free Operation on Serializers
- ASIL-B Compliant (GMSL2)
  - Video Watermark Insertion and Detection
  - 16-Bit CRC Protection of Control-Channel Data with Retransmission Upon Error Detection
  - Optional 32-Bit CRC Protection of Video Line Data
  - ECC Protection of Video Data Memory
  - CRC Protection of CSI-2 Data Streams
- Concurrent Control Channel for Device Configuration and Communicating with Remote Peripherals
  - 3x I^2C/UART, 2x SPI, 17x GPIO
  - Eight Hardware-Selectable Device Addresses
- Programmable Spread Spectrum for EMI Reduction
- 64-lead 9mm x 9mm TQFN with Exposed Pad

***Ordering Information** appears at end of data sheet.*

19-100544; Rev 4; 11/23

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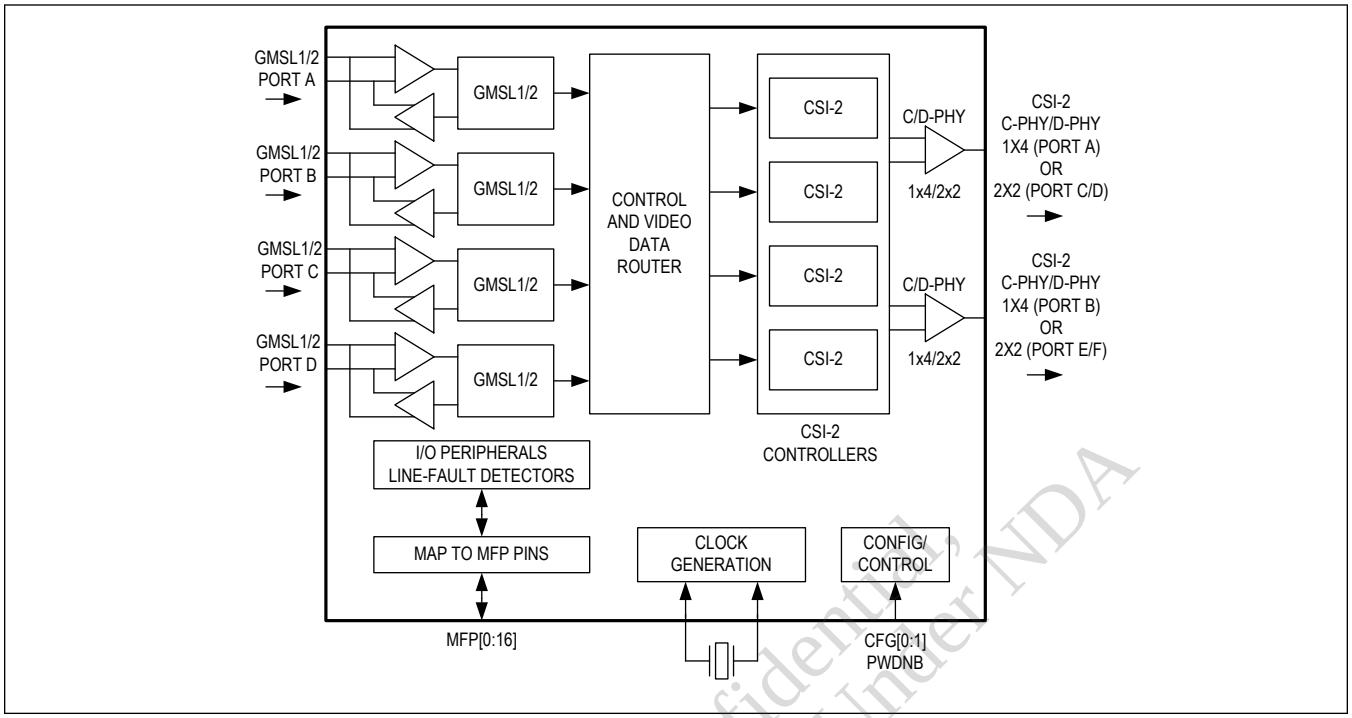
Simplified Block Diagram



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Absolute Maximum Ratings

(All voltages with respect to ground.) .....
V_{DDIO} ..... -0.3V to +3.9V
V_{DD18} ..... -0.3V to +2.0V
V_{DD} ..... -0.3V to +2.0V
V_{TERM} ..... -0.3V to +1.32V
CAP_VDD ..... -0.3V to +1.2V
SIO_ (Active State) (Note a)..... (V_{DD18} - 1.1V) to V_{DD18}
SIO_ (Inactive State) (Note a) ..... -0.3V to +1.1V
DA/B_P/N, CKA/B/C/FP/N (Note b)..... -0.3V to (V_{TERM} + 0.1V)
XRES, X2..... -0.3V to (V_{DD18} + 0.3V)
All Other Pins (Note c) ..... -0.3V to (V_{DDIO} + 0.3V)
Continuous Power Dissipation, Multilayer Board (Note d).....2412mW
Storage Temperature Range .....-40°C to +150°C
Soldering Temperature (reflow) .....+260°C

Note a: Active state means device powered-up and not in sleep or power-down modes. Inactive state means device not powered-up, or powered-up in sleep or power-down mode.

Note b: Specified maximum voltage or 1.36V, whichever is lower.

Note c: Specified maximum voltage or 3.9V, whichever is lower.

Note d: Derate 44mW/°C above T_A = +70°C. Maximum dissipation is determined using specified θ_{JA} and assuming maximum acceptable die temperature of 125°C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

64-pin TQFN

Package Code	T6499+2
Outline Number	21-100060
Land Pattern Number	90-100053
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	22.8°C/W
Junction to Case (θ_{JC})	5.4°C/W

64-pin TQFN-SW (Side-Wettable)

Package Code	T6499Y+2
Outline Number	21-100326
Land Pattern Number	90-100053
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	22.8°C/W
Junction to Case (θ_{JC})	5.4°C/W

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Electrical Characteristics

(V_{TERM} = 1.14V to 1.26V, V_{DD18} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.05V or V_{DD} = 1.14V to 1.26V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{TERM} = 1.2V, V_{DD18} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = +25°C, unless otherwise noted. (Note 1))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS / GMSL2 REVERSE CHANNEL SERIAL OUTPUTS - Figure 1							
Output Voltage Swing (Single-ended)	V_O	R_L = 100Ω ±1%		190	250	310	mV
Output Voltage Swing (Differential)	V_{ODT}	R_L = 100Ω ±1% peak-to-peak differential voltage		380	500	620	mV
Change in V_{OD} Between Complementary Output States	ΔV_{OD}	R_L = 100Ω ±1% $\lvert V_{OD(H)} - V_{OD(L)} \rvert$				25	mV
Differential Output Offset Voltage	V_{OS}	R_L = 100Ω ±1% offset voltage in each output state		V_{DD18} - 0.45	V_{DD18} - 0.3	V_{DD18} - 0.15	V
Change in V_{OS} Between Complementary Output States	ΔV_{OS}	R_L = 100Ω ±1% $\lvert V_{OS(H)} - V_{OS(L)} \rvert$				25	mV
Termination Resistance (Internal)	R_T	Any pin to V_{DD18}		50	55	60	Ω
DC ELECTRICAL CHARACTERISTICS / GMSL1 REVERSE CHANNEL SERIAL OUTPUTS - Figure 2							
Differential High Output Peak Voltage $V_{(SIO_P)}$ - $V_{(SIO_N)}$	V_{RODH}	Forward channel disabled STP mode R_L = 100Ω	HIM disabled	30		70	mV
			HIM enabled	50		110	
Differential Low Output Peak Voltage $V_{(SIO_P)}$ - $V_{(SIO_N)}$	V_{RODL}	Forward channel disabled STP mode R_L = 100Ω	HIM disabled	-70		-30	mV
			HIM enabled	-110		-50	
Single-Ended High Output Peak Voltage	V_{ROSH}	Forward channel disabled coax mode R_L = 100Ω	HIM disabled	30		70	mV
			HIM enabled	50		110	
Single-Ended Low Output Peak Voltage	V_{ROSL}	Forward channel disabled coax mode R_L = 100Ω	HIM disabled	-70		-30	mV
			HIM enabled	-110		-50	
Differential Output Offset Voltage ($V_{(SIO_P)}$ + $V_{(SIO_N)}$)/2	V_{OS}	STP mode		V_{DD18} - 0.3		V_{DD18}	V
Termination Resistance (Internal)	R_T	Any pin to V_{DD18}		50	55	60	Ω
DC ELECTRICAL CHARACTERISTICS / C-PHY and D-PHY LP TRANSMITTER							
Thevenin High-Level Output Voltage	V_{OH}	Figure 3, Figure 6		0.95	1.2	1.3	V
Thevenin Low-Level Output Voltage	V_{OL}	Figure 3, Figure 6		-50		50	mV
Output Impedance	Z_{OLP}			110			Ω

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Electrical Characteristics (continued)

(V_{TERM} = 1.14V to 1.26V, V_{DD18} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.05V or V_{DD} = 1.14V to 1.26V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{TERM} = 1.2V, V_{DD18} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = +25°C, unless otherwise noted. (*Note 1*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS / D-PHY HS TRANSMITTER						
HS Transmit Static Common-Mode Voltage	V_{CMTX}	Figure 3	150	200	250	mV
V_{CMTX} Mismatch when Output is Differential-1 or Differential-0	$\lvert\Delta V_{CMTX(1,0)}\rvert$	$\Delta V_{CMTX(1,0)} = (V_{CMTX(1)} - V_{CMTX(0)}) / 2$ Figure 4			5	mV
HS Transmit Differential Voltage	$\lvert V_{OD}\rvert$	Figure 5	140	200	270	mV
V_{OD} Mismatch when Output is Differential-1 or Differential-0	$\lvert\Delta V_{OD}\rvert$	Figure 4			14	mV
HS Output High Voltage	V_{OHHS}	Figure 3			360	mV
Single-Ended Output Impedance	Z_{OS}		40	50	62.5	Ω
Single-Ended Output Impedance Mismatch	ΔZ_{OS}				10	%
DC ELECTRICAL CHARACTERISTICS / C-PHY HS TRANSMITTER						
HS Transmit Static Common-Point Voltage	V_{CPTX}	Z_{ID} = 100Ω, Figure 6	175		310	mV
V_{CPTX} Mismatch when Output is in any of the Six High-Speed States	$\lvert\Delta V_{CPTX(HS)}\rvert$	Figure 7			9	mV
HS Transmit Differential Voltage of the Differential Strong 1 and Strong 0	$\lvert V_{OD}\rvert$ strong	Z_{ID} = 100Ω, Figure 8			300	mV
HS Transmit Differential Voltage of the Differential Weak 1 and Weak 0	$\lvert V_{OD}\rvert$ weak	Z_{ID} = 100Ω, Figure 8	97			mV
V_{OD} Mismatch Between the Absolute Values of the Differential Strong 1 and Strong 0 Output Voltages in any of the Six Possible High-Speed States	$\lvert\Delta V_{OD}\rvert$	Figure 7			17	mV
HS Output High Voltage	V_{OHHS}	Z_{ID} =100Ω, Figure 6			425	mV
Single-Ended Output Impedance	Z_{OS}		40	50	60	Ω
Single-Ended Output Impedance Mismatch	ΔZ_{OS}				10	%
DC ELECTRICAL CHARACTERISTICS / I/O PINS						
High-Level Input Voltage	V_{IH}		0.7 x V_{DDIO}			V

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Electrical Characteristics (continued)

(V_{TERM} = 1.14V to 1.26V, V_{DD18} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.05V or V_{DD} = 1.14V to 1.26V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{TERM} = 1.2V, V_{DD18} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = +25°C, unless otherwise noted. (*Note 1*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Low-Level Input Voltage	V_{IL}				0.3 x V_{DDIO}	V
High-Level Output Voltage	V_{OH}	I_{OH} = -4mA	V_{DDIO} - 0.4			V
Low-Level Output Voltage	V_{OL}	I_{OL} = 4mA			0.4	V
Input Current	I_{IN}	All pullup/pulldown devices disabled. V_{IN} = 0V to V_{DDIO}			1	µA
Input Capacitance	C_{IN}			3		pF
Internal Pullup/Pulldown Resistance	R_{IN}	40kΩ enabled		40		kΩ
		1MΩ enabled		1		MΩ
DC ELECTRICAL CHARACTERISTICS / OPEN-DRAIN PINS						
High-Level Input Voltage	V_{IH}		0.7 x V_{DDIO}			V
Low-Level Input Voltage	V_{IL}				0.3 x V_{DDIO}	V
Low-Level Open-Drain Output Voltage	V_{OL}	I_{OL} = 4mA			0.4	V
Input Current	I_{IN}	All pullup/pulldown devices disabled. V_{IN} = 0V to V_{DDIO}			1	µA
Input Capacitance	C_{IN}			3		pF
Internal Pullup Resistance	R_{PU}	40kΩ enabled		40		kΩ
		1MΩ enabled		1		MΩ
DC ELECTRICAL CHARACTERISTICS / PWDNB INPUT						
High-Level Input Voltage	V_{IH}		0.7 x V_{DDIO}			V
Low-Level Input Voltage	V_{IL}				0.3 x V_{DDIO}	V
Input Current	I_{IN}	V_{IN} = 0V to V_{DDIO}			6	µA
Internal Pulldown Resistance	R_{PD}			1		MΩ
Input Capacitance	C_{IN}			3		pF
DC ELECTRICAL CHARACTERISTICS / PUSH-PULL OUTPUTS						
High-Level Output Voltage	V_{OH}	I_{OH} = -4mA	V_{DDIO} - 0.4			V
Low-Level Output Voltage	V_{OL}	I_{OL} = 4mA			0.4	V
DC ELECTRICAL CHARACTERISTICS / LINE-FAULT DETECTION INPUTS						
Open Pin Voltage	V_{O0}	LMN0, LMN2, LMN4, LMN6		1.25		V
	V_{O1}	LMN1, LMN3, LMN5, LMN7		0.75		
DC ELECTRICAL CHARACTERISTICS / REFERENCE CLOCK INPUT (CRYSTAL) (X1/OSC, X2)						
X1 Input Capacitance	C_{IN_X1}			3		pF

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Electrical Characteristics (continued)

(V_{TERM} = 1.14V to 1.26V, V_{DD18} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.05V or V_{DD} = 1.14V to 1.26V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{TERM} = 1.2V, V_{DD18} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = +25°C, unless otherwise noted. (*Note 1*))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
X2 Input Capacitance	C_{IN_X2}				1		pF
Internal X2 Limit Resistor	R_{LIM}				1.2		kΩ
Internal Feedback Resistor	R_{FB}				10		kΩ
Transconductance	g_m				28		mA/V
DC ELECTRICAL CHARACTERISTICS / REFERENCE CLOCK INPUT (EXTERNAL INPUT ON X1/OSC, X2 UNCONNECTED) - ONLY SUPPORTED WITH MAX96712							
High-Level Input Voltage	V_{IH}			0.9			V
Low-Level Input Voltage	V_{IL}					0.4	V
Input Impedance	R_{IN}				10		kΩ
X1 Input Capacitance	C_{IN_X1}				3		pF
DC ELECTRICAL CHARACTERISTICS / POWER SUPPLY CURRENT—GMSL2 MODE (*Note 3*)							
Supply Current	I_{DD1}	4x 3Gbps input 1x 4-lane output 2500Mbps/lane 4 video pipes enabled RGB888 D-PHY	V_{TERM}		19	25	mA
			V_{DD18}		268	325	
			V_{DD}, LDO Disabled		251	750	
			V_{DD}, LDO Enabled		240	725	
		4x 6Gbps input 1x 4-lane output 5700Mbps/lane 4 video pipes enabled RGB888 C-PHY	V_{TERM}		20	35	
			V_{DD18}		247	325	
			V_{DD}, LDO Disabled		315	800	
			V_{DD}, LDO Enabled		304	780	
	I_{DD2}	Replicate mode 4x 3Gbps input 2x 4-lane output 2500Mbps/lane 4 video pipes enabled RGB888 D-PHY	V_{TERM}		35	50	
			V_{DD18}		268	325	
			V_{DD}, LDO Disabled		285	800	
			V_{DD}, LDO Enabled		273	760	
		Replicate mode 4x 6Gbps input 2x 4-lane output 5700Mbps/lane 4 video pipes enabled RGB888 C-PHY	V_{TERM}		39	70	
			V_{DD18}		247	325	
			V_{DD}, LDO Disabled		358	850	
			V_{DD}, LDO Enabled		347	825	
Maximum V_{DDIO} Supply Current (*Note 4*)	I_{DDIO}	Per toggling GPIO, C_L = 20pF	V_{DDIO} = 1.8V Range		44		µA/MHz
			V_{DDIO} = 3.3V Range		81		

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Electrical Characteristics (continued)

(V_{TERM} = 1.14V to 1.26V, V_{DD18} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.05V or V_{DD} = 1.14V to 1.26V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{TERM} = 1.2V, V_{DD18} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = +25°C, unless otherwise noted. (Note 1))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS / POWER SUPPLY CURRENT—GMSL1 MODE (Note 3)							
Supply Current	I_{DD1}	4x 3Gbps input 1x 4-lane output 2500Mbps/lane RGB888 D-PHY	V_{TERM}		15.6	25	mA
			V_{DD18}		135	190	
			V_{DD}, LDO Disabled		93	575	
			V_{DD}, LDO Enabled		83	550	
	I_{DD2}	Replicate Mode 4x 3Gbps input 2x 4-lane output 2500Mbps/lane RGB888 D-PHY	V_{TERM}		29	50	
			V_{DD18}		135	190	
			V_{DD}, LDO Disabled		100	625	
			V_{DD}, LDO Enabled		91	600	
Maximum V_{DDIO} Supply Current (Note 4)	I_{DDIO}	Per toggling GPIO, C_L = 20pF	V_{DDIO} = 1.8V Range		44		µA/MHz
			V_{DDIO} = 3.3V Range		81		
DC ELECTRICAL CHARACTERISTICS / POWER-DOWN CURRENT							
Maximum Power-Down Current	I_{DD}	V_{TERM} = 1.26V	T_A = +25°C		< 1		µA
			T_A = +105°C		< 1		
		V_{DD18} = 1.9V	T_A = +25°C		< 1		
			T_A = +105°C		14		
		V_{DD} = 1.26V	T_A = +25°C		< 1		
			T_A = +105°C		< 1		
		V_{DDIO} = 3.6V	T_A = +25°C		7		
			T_A = +105°C		7		
DC ELECTRICAL CHARACTERISTICS / SLEEP CURRENT							
Maximum Sleep Current	I_{DD}	V_{TERM} = 1.26V	T_A = +25°C		< 1		µA
			T_A = +105°C		< 1		
		V_{DD18} = 1.9V	T_A = +25°C		5		
			T_A = +105°C		19		
		V_{DD} = 1.26V	T_A = +25°C		< 1		
			T_A = +105°C		< 1		
		V_{DDIO} = 3.6V	T_A = +25°C		9		
			T_A = +105°C		9		
AC ELECTRICAL CHARACTERISTICS / GMSL2 FORWARD CHANNEL							
Lock Time	t_{LOCK2}	From power-up, one-shot reset, or rising edge of PWDNB to rising edge of LOCK. (Note 11, Note 12)			45	60	ms
Maximum Video Initialization Time	$t_{VIDEOSTART}$	Time from GMSL2 video packets at SIO_ to valid packets at the CSI-2 output (assumes link locked and registers configured)			0.1ms + (6600 x t_{PCLK})		ms

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Electrical Characteristics (continued)

(V_{TERM} = 1.14V to 1.26V, V_{DD18} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.05V or V_{DD} = 1.14V to 1.26V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{TERM} = 1.2V, V_{DD18} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = +25°C, unless otherwise noted. (*Note 1*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Video Latency	t_{VL}	Time from the first pixel in a GMSL2 packet at SIO_ to the first pixel in the CSI-2 output packet. Figure 9		1 video line + (128 x t_{PCLK})		s
PWDNB Hold Time	t_{HOLD_PWDNB}	The minimum duration PWDNB must be held LOW to reset the device.		1		ms
AC ELECTRICAL CHARACTERISTICS / GMSL2 REVERSE CHANNEL						
GMSL Reverse Channel Transmitter Rise/Fall Time	t_R, t_F	20% to 80%, V_O = 250mV, R_L = 100Ω		2300		ps
Total Serial Output p-p Jitter	t_{TSOJ}	PRBS7, single-ended or differential output		0.15		UI
Deterministic Serial Output p-p Jitter	t_{DSOJ}	PRBS7, single-ended or differential output		0.1		UI
GPI-GPO Delay Reverse Path	t_{GPDR}	Delay-Compensated Mode Table 6, Figure 10		15		µs
		Non-Delay-Compensated Mode Table 6, Figure 10		6		
GPI-GPO Skew Reverse Path	t_{SKEW}	Delay-Compensated Mode Figure 10		7		ns
AC ELECTRICAL CHARACTERISTICS / GMSL1						
Maximum Lock Time	t_{LOCK1}	Figure 11		4		ms
Maximum Power-up Time	t_{PU}	Figure 12		8.5		ms
Maximum Video Latency	t_{VL}	Time from the first pixel in a video line at SIO_ to the first pixel in the CSI-2 output packet. Figure 13		1 video line + (128 x t_{PCLK})		s
PWDNB Hold Time	t_{HOLD_PWDNB}	The minimum duration PWDNB must be held LOW to reset the device		1		ms
Reverse Control-Channel Output Rise Time	t_R	No forward channel data transmission Figure 2, (*Note 2*)	100		400	ns
Reverse Control-Channel Output Fall Time	t_F	No forward channel data transmission Figure 2, (*Note 2*)	100		400	ns
GPI-to-GPO Delay	t_{GPIO}	Deserializer GPI to serializer GPO (cable delay not included) Figure 14, (*Note 2*)			350	µs
AC ELECTRICAL CHARACTERISTICS / C-PHY and D-PHY LP TRANSMITTER (*Note 2*)						
15% to 85% Rise Time and Fall Time	t_{RLP}/t_{FLP}	(*Note 5*)			25	ns
30% to 85% Rise Time	t_{REOT}	Figure 15, Figure 19, (*Note 6*)			35	ns
Load Capacitance	C_{LOAD}	(*Note 5*)	0		70	pF

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Electrical Characteristics (continued)

(V_{TERM} = 1.14V to 1.26V, V_{DD18} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.05V or V_{DD} = 1.14V to 1.26V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{TERM} = 1.2V, V_{DD18} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = +25°C, unless otherwise noted. (*Note 1*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AC ELECTRICAL CHARACTERISTICS / D-PHY HS TRANSMITTER (*Note 2*)						
Common-Level Variations, HF	$\Delta V_{CMTX(HF)}$	> 450MHz, Figure 4			15	mV_{RMS}
Common-Level Variations, LF	$\Delta V_{CMTX(LF)}$	50MHz to 450MHz, Figure 4			25	mV_{PEAK}
20%-80% Rise Time and Fall Time	t_R and t_F				0.4	UI
			50			ps
Differential-Mode Reflection Coefficient (*Note 7*)	Sdd_{TX}	f_{hMAX} = 1.25GHz		-4.5		dB
		f_{MAX} = 1.875GHz		-2.5		
Common-Mode Reflection Coefficient (*Note 7*)	Scc_{TX}	f_{MAX} = 1.875GHz		-2.5		dB
Data Lane Bit Rate	DL_{BR}		80		2500	Mbps
Clock Lane Frequency	CL_{FREQ}		40		1250	MHz
CSI-2 Output Inter-packet Spacing	t_{SPACE}			300ns + 370UI		ns
AC ELECTRICAL CHARACTERISTICS / D-PHY DATA-CLOCK TIMING (*Note 2*)						
UI Instantaneous	UI_{INST}		0.4		12.5	ns
UI Variation	ΔUI	UI ≥ 1ns within a single burst	-10%		10%	UI
		0.667ns ≤ UI ≤ 1ns within a single burst	-5%		5%	
Data to Clock Skew	t_{SKEW}	0.08 to 1.0Gbps, Figure 16	-0.15		0.15	UI_{INST}
		> 1.0Gbps to 1.5Gbps, Figure 16	-0.2		0.2	
Static Data to Clock Skew	t_{SKEW} Static	> 1.5Gbps, Figure 16	-0.2		0.2	UI_{INST}
Dynamic Data to Clock Skew	t_{SKEW} Dynamic	> 1.5Gbps, Figure 16	-0.15		0.15	UI_{INST}
AC ELECTRICAL CHARACTERISTICS / D-PHY GLOBAL OPERATION TIMING (*Note 2*)						
Time that the HS Clock must be Driven by the Transmitter Prior to any Associated Data Lane Beginning the Transition from LP to HS Mode	$t_{CLK-PRE}$	Figure 18	8			UI
Time that the Transmitter Drives the Clock Lane LP-00 Line State Immediately Before the HS-0 Line State Starting the HS Transmission	$t_{CLK-PREPARE}$	Figure 18	38		95	ns

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Electrical Characteristics (continued)

(V_{TERM} = 1.14V to 1.26V, V_{DD18} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.05V or V_{DD} = 1.14V to 1.26V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{TERM} = 1.2V, V_{DD18} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = +25°C, unless otherwise noted. (*Note 1*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$T_{CLK-PREPARE}$ + Time that the Transmitter Drives the HS-0 State Prior to Starting the Clock	$t_{CLK-PREPARE}$ + $t_{CLK-ZERO}$	Figure 18	300			ns
Transmitted Time Interval from the Start of $T_{HS-TRAIL}$ or $T_{CLK-TRAIL}$, to the Start of the LP-11 State Following a HS Burst	t_{EOT}	Figure 15, Figure 17, Figure 18			105 + 12xUI	ns
Time that the Transmitter Drives LP-11 Following a HS Burst	$t_{HS-EXIT}$	Figure 15, Figure 17, Figure 18	100			ns
Time that the Transmitter Drives the Data Lane LP-00 Line State Immediately Before the HS-0 Line State Starting the HS Transmission	$t_{HS-PREPARE}$	Figure 15, Figure 17, Figure 18	40 + 4xUI		85 + 6xUI	ns
$T_{HS-PREPARE}$ + Time that the Transmitter Drives the HS-0 State Prior to Transmitting the Sync Sequence	$t_{HS-PREPARE}$ + $t_{HS-ZERO}$	Figure 15	145 + 10xUI			ns
Time that the Transmitter Drives the Flipped Differential State After Last Payload Data Bit of a HS Transmission Burst	$t_{HS-TRAIL}$	Figure 15, Figure 17	60 + 4xUI			ns
Initialization Time	t_{INIT}		100			µs
Transmitted Length of any Low-Power State Period	t_{LPX}	Figure 15, Figure 17, Figure 18	50			ns
Time that the Transmitter Drives the Skew-Calibration Sync Pattern, 0xFFFF	$t_{SKEWCAL_SYNC}$	Figure 17		16		UI
Time that the Transmitter Drives the Skew-Calibration Pattern in the Initial Skew-Calibration Mode	$t_{SKEWCAL}$	Figure 17			100	µs
		Figure 17	2^{15}			UI

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Electrical Characteristics (continued)

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Time that the Transmitter Drives the Skew-Calibration Pattern in the Periodic Skew-Calibration Mode	$t_{SKEWCAL}$	Figure 17			10	µs
		Figure 17	2^{10}			UI
AC ELECTRICAL CHARACTERISTICS / C-PHY HS TRANSMITTER (*Note 2*)						
Common-Level Variations	$\Delta V_{CPTX(HF)}$	> 450MHz			15	mV_{RMS}
	$\Delta V_{CPTX(LF)}$	50MHz to 450MHz			25	mV_{PEAK}
Rise Time	t_R	Strong 0 to Weak 1 transition, -58mV to +58mV, Z_{ID} = 100Ω			0.285	UI
Fall Time	t_F	Strong 1 to Weak 0 transition, +58mV to -58mV, Z_{ID} = 100Ω			0.285	UI
Rise Time and Fall Time Limit	$t_{RISE-FALL-MAX}$	-58mV to +58mV, Z_{ID} = 100Ω (*Note 9*)			360	ps
Differential-Mode Reflection Coefficient (*Note 8*)	Sdd_{TX}	f_{hMAX} = 1.25GHz		-5		dB
		f_{MAX} = 1.875GHz		-3		
Common-Mode Reflection Coefficient (*Note 8*)	Scc_{TX}	f_{MAX} = 1.875GHz		-3		dB
C-PHY Lane Bit Rate	C_{BR}		182		5700	Mbps
CSI-2 Output Inter-Packet Spacing	t_{SPACE}			300ns + 370UI		ns
UI Instantaneous	UI_{INST}		0.4		12.5	ns
AC ELECTRICAL CHARACTERISTICS / C-PHY GLOBAL OPERATION TIMING - Figure 19 (*Note 2*)						
Time that the Transmitter Drives the 3-Wire LP-000 Line State Immediately Before the HS_+x Line State Starting the HS Transmission	$t_{3-PREPARE}$		38		95	ns
Time that the Transmitter Drives LP-111 Following a HS Burst	$t_{3-HS-EXIT}$		100			ns
Transmitted Length of any Low-Power State Period	t_{LPX}		50			ns
Initialization Time	t_{INIT}		100			µs
AC ELECTRICAL CHARACTERISTICS / I^2C/UART PORT TIMING						
Output Fall Time	t_F	70% to 30%, C_L = 20pF to 100pF, 1kΩ pullup to V_{DDIO} (*Note 2*)	20 x V_{DDIO}/5.5V		150	ns

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Electrical Characteristics (continued)

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I^2C/UART Wake Time	t_{WAKEUP}	From power-up, or rising edge of PWDNB to local register access. For remote register access, I^2C/UART wake time is the same as lock time ($t_{LOCK_}$).		4		ms
AC ELECTRICAL CHARACTERISTICS / I^2C TIMING - Figure 20						
SCL Clock Frequency	f_{SCL}	Low f_{SCL} range: (I2C_MST_BT = 010, I2C_SLV_SH = 10)	9.6		100	kHz
		Mid f_{SCL} range: (I2C_MST_BT = 101, I2C_SLV_SH = 01)	100		400	
		High f_{SCL} range: (I2C_MST_BT = 111, I2C_SLV_SH = 00)	400		1000	
Start Condition Hold Time	$t_{HD:STA}$	f_{SCL} range, low	4			µs
		f_{SCL} range, mid	0.6			
		f_{SCL} range, high	0.26			
Low Period of SCL Clock	t_{LOW}	f_{SCL} range, low	4.7			µs
		f_{SCL} range, mid	1.3			
		f_{SCL} range, high	0.5			
High Period of SCL Clock	t_{HIGH}	f_{SCL} range, low	4			µs
		f_{SCL} range, mid	0.6			
		f_{SCL} range, high	0.26			
Repeated Start Condition Setup Time	$t_{SU:STA}$	f_{SCL} range, low	4.7			µs
		f_{SCL} range, mid	0.6			
		f_{SCL} range, high	0.26			
Data Hold Time	$t_{HD:DAT}$	f_{SCL} range, low	0			ns
		f_{SCL} range, mid	0			
		f_{SCL} range, high	0			
Data Setup Time	$t_{SU:DAT}$	f_{SCL} range, low	250			ns
		f_{SCL} range, mid	100			
		f_{SCL} range, high	50			
Setup Time for Stop Condition	$t_{SU:STO}$	f_{SCL} range, low	4			µs
		f_{SCL} range, mid	0.6			
		f_{SCL} range, high	0.26			
Bus Free Time	t_{BUF}	f_{SCL} range, low	4.7			µs
		f_{SCL} range, mid	1.3			
		f_{SCL} range, high	0.5			
Data Valid Time	$t_{VD:DAT}$	f_{SCL} range, low			3.45	µs
		f_{SCL} range, mid			0.9	
		f_{SCL} range, high			0.45	

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Electrical Characteristics (continued)

(V_{TERM} = 1.14V to 1.26V, V_{DD18} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.05V or V_{DD} = 1.14V to 1.26V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{TERM} = 1.2V, V_{DD18} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = +25°C, unless otherwise noted. (*Note 1*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Valid Acknowledge Time	$t_{VD:ACK}$	f_{SCL} range, low			3.45	µs
		f_{SCL} range, mid			0.9	
		f_{SCL} range, high			0.45	
Pulse Width of Spikes Suppressed	t_{SP}	f_{SCL} range, low			50	ns
		f_{SCL} range, mid			50	
		f_{SCL} range, high			50	
Capacitive Load On Each Bus Line	C_B	(*Note 2*)			100	pF
AC ELECTRICAL CHARACTERISTICS / SPI MAIN - *Figure 22* (*Note 10*)						
Operating Frequency	f_{MCK}	(*Note 2*)	0.588		25	MHz
SCLK Period	t_{MCK}			$1/f_{MCK}$		ns
SCLK Output Pulse-Width High/Low	t_{MCH}, t_{MCL}	(*Note 2*)	$t_{MCK}/2$ - 3	$t_{MCK}/2$		ns
MOSI Data Output Delay	t_{MOD}	After SCLK Falling Edge (*Note 2*)	-2.3		2.3	ns
MISO Input Setup Time	t_{MIS}	Before Programmed Sampling Edge (*Note 2*)	13.5			ns
MISO Input Hold Time	t_{MIH}	After Programmed Sampling Edge (*Note 2*)	-2			ns
AC ELECTRICAL CHARACTERISTICS / SPI SUBORDINATE *Figure 23* (*Note 10*)						
Operating Frequency	f_{SCK}	(*Note 2*)			50	MHz
SCLK Period	t_{SCK}			$1/f_{SCK}$		ns
MISO Data Output Delay	t_{SOD}	After SCLK Falling Edge (*Note 2*)	2.0		11.3	ns
MOSI Input Setup Time	t_{SIS}	Before SCLK Rising Edge (*Note 2*)	5			ns
MOSI Input Hold Time	t_{SIH}	After SCLK Rising Edge (*Note 2*)	3			ns
AC ELECTRICAL CHARACTERISTICS / REFERENCE CLOCK REQUIREMENTS (CRYSTAL)(X1/OSC, X2) (*Note 2*)						
Frequency	f_{XTAL}			25		MHz
Frequency Stability + Frequency Tolerance	f_{TN}				±200	ppm
AC ELECTRICAL CHARACTERISTICS / REFERENCE CLOCK REQUIREMENTS (EXTERNAL CLOCK INPUT ON X1/OSC, X2 UNCONNECTED) - ONLY SUPPORTED WITH MAX96712 (*Note 2*)						
Frequency	f_{REF}			25		MHz
Frequency Stability + Frequency Tolerance	f_{TN}				±200	ppm
Input Jitter		Link Speed = 6Gbps/187.5Mbps sinusoidal jitter < 1MHz (falling edge) upstream serializer using crystal reference			600	ps p-p
Input Duty Cycle	t_{DUTY}		40		60	%
Input Fall Time	t_F	80% to 20%			4	ns

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Note 1: Limits are 100% tested at T_A = +105°C unless otherwise noted. Limits within the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

Note 2: Not production tested. Guaranteed by design and characterization. External oscillator is only supported with the MAX96712.

Note 3: Color bar pattern. For $V_{TERM}/V_{DD}/V_{DD18}$ supply current specifications, V_{DDIO} = 1.8V/3.3V typ/max. For $V_{TERM}/V_{DD18}/V_{DDIO}$ supply current specifications, V_{DD} = 1V.

Note 4: MFP pin speed programmed to fastest setting (TTS = 00). See *Multifunction Pin Configuration* for details regarding MFP speed programming.

Note 5: C_{LOAD} includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be < 10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.

Note 6: Additional capacitance up to 60pF (D-PHY) or 90pF (C-PHY) at RX termination center tap.

Note 7: Differential-mode and common-mode reflection coefficient are compliant with MIPI D-PHY V1.2 requirements over all specified operating frequencies.

Note 8: Differential-mode and common-mode reflection coefficient are compliant with MIPI C-PHY V1.0 requirements over all specified operating frequencies.

Note 9: For rates ≤ 1.5Gbps, t_R and t_F shall be ≤ min (0.4UI, $t_{RISE-FALL-MAX}$)

Note 10: Measured at 50MHz. For V_{DDIO}<2.25V, speed group A and C TTS = 00 and for V_{DDIO}≥2.25V, speed group A and C TTS = 01. See *Multifunction Pin Configuration* for details regarding MFP speed programming.

Note 11: Production tested using ECS ECS-250-18-33Q-DS crystal.

Note 12: From power-up, release of RESET_LINK, or rising edge of the PWDNB pin to rising edge of the LOCK pin, t_{RD} must be < 90ms if serializer powers up or is released from link reset before deserializer. For more information, see the *GMSL2 Link Lock* section.

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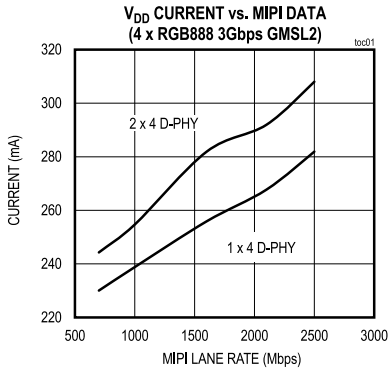
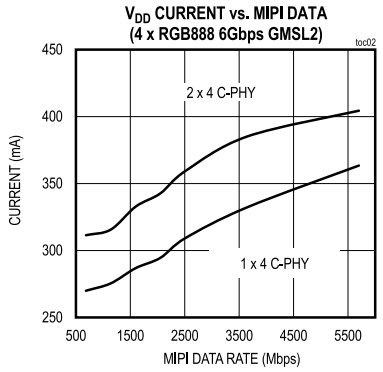
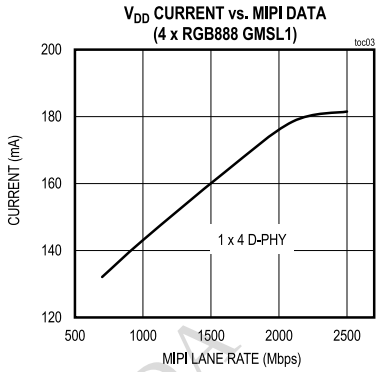
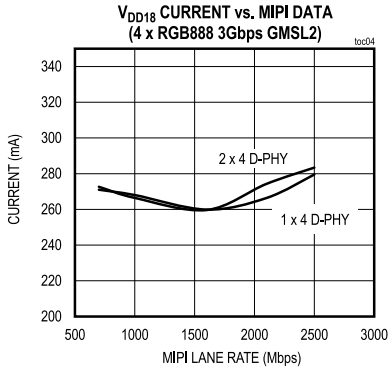
Typical Operating Characteristics

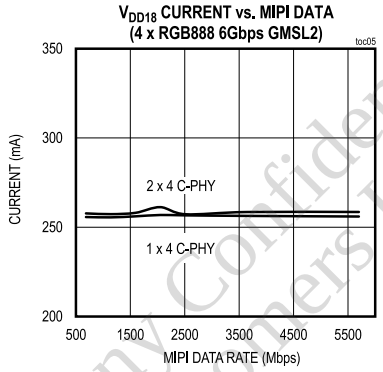
(V_{TERM} = 1.2V, V_{DD18} = 1.8V, V_{DDIO} = 3.3V, V_{DD} = 1.0V, Coax Mode, RGB888 video format, all GMSL links active with identical configuration, dual port MIPI configurations utilize replication, T_A = +25°C, unless otherwise noted.)

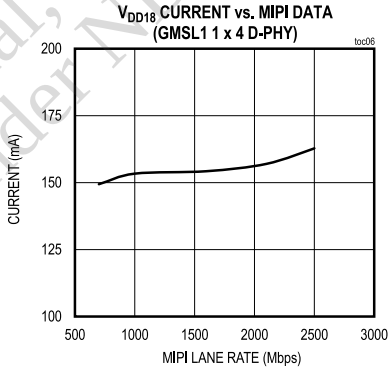


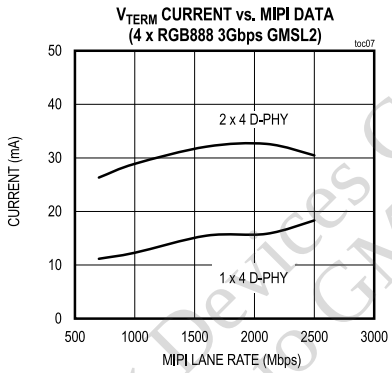


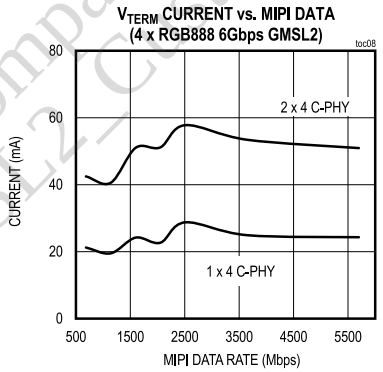


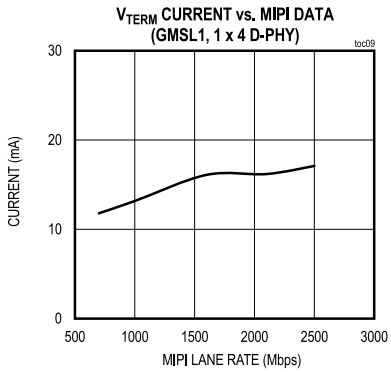












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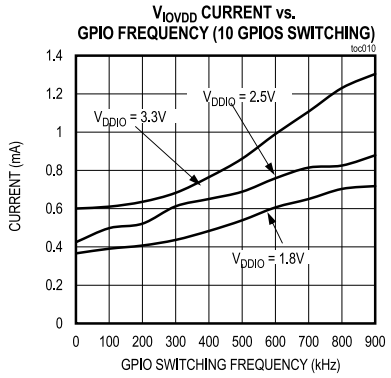
Typical Operating Characteristics (continued)

(V_{TERM} = 1.2V, V_{DD18} = 1.8V, V_{DDIO} = 3.3V, V_{DD} = 1.0V, Coax Mode, RGB888 video format, all GMSL links active with identical configuration, dual port MIPI configurations utilize replication, T_A = +25°C, unless otherwise noted.)



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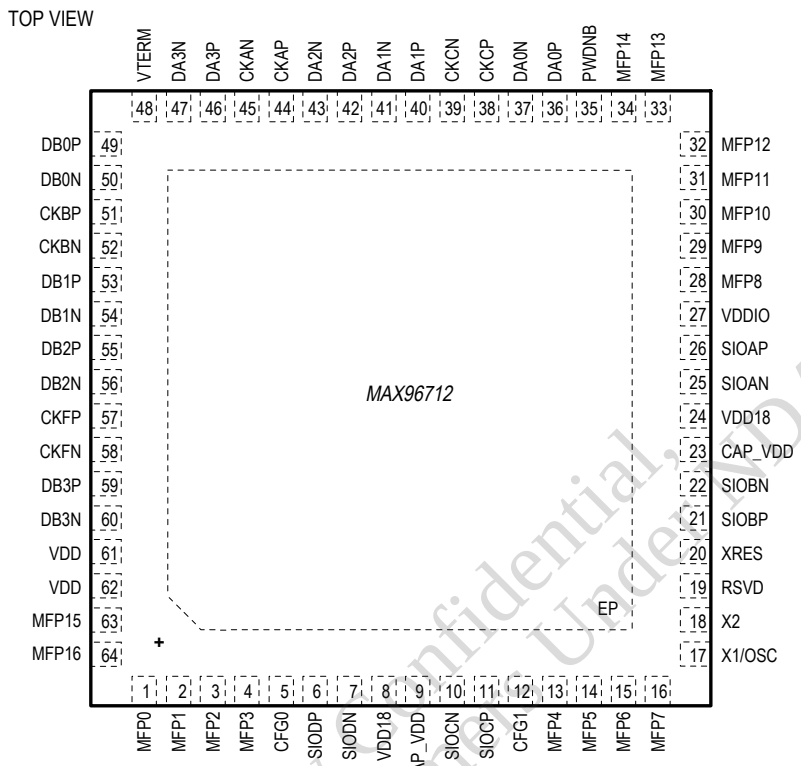
Pin Configuration



Pin Description

PIN	NAME	FUNCTION MODE		FUNCTION
		GMSL2	GMSL1	
GMSL2/GMSL1 SERIAL LINK				
26	SIOAP	SIOAP	SIOAP	Noninverted Coax/Twisted-Pair Serial-Data I/O A.
25	SIOAN	SIOAN	SIOAN	Inverted Twisted-Pair Serial-Data I/O A.
21	SIOBP	SIOBP	SIOBP	Noninverted Coax/Twisted-Pair Serial-Data I/O B.
22	SIOBN	SIOBN	SIOBN	Inverted Twisted-Pair Serial-Data I/O B.
11	SIOCP	SIOCP	SIOCP	Noninverted Coax/Twisted-Pair Serial-Data I/O C.
10	SIOCN	SIOCN	SIOCN	Inverted Twisted-Pair Serial-Data I/O C.
6	SIODP	SIODP	SIODP	Noninverted Coax/Twisted-Pair Serial-Data I/O D.
7	SIODN	SIODN	SIODN	Inverted Twisted-Pair Serial-Data I/O D.

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PIN	NAME	FUNCTION MODE		FUNCTION
		GMSL2	GMSL1	
CSI-2 INTERFACE - PORT A/C/D (* denotes default state after power-up)				
36	DA0P	DA0P* DC0P A0A C0A	DA0P* DC0P A0A C0A	DA0P: D-PHY Port A Data Lane 0 Noninverted Output (4-lane mode). DC0P: D-PHY Port C Data Lane 0 Noninverted Output (2-lane mode). A0A: C-PHY Port A Lane 0 Output A (4-lane mode). C0A: C-PHY Port C Lane 0 Output A (2-lane mode).
37	DA0N	DA0N* DC0N A0B C0B	DA0N* DC0N A0B C0B	DA0N: D-PHY Port A Data Lane 0 Inverted Data Output (4-lane mode). DC0N: D-PHY Port C Data Lane 0 Inverted Output (2-lane mode). A0B: C-PHY Port A Lane 0 Output B (4-lane mode). C0B: C-PHY Port C Lane 0 Output B (2-lane mode).
40	DA1P	DA1P* DC1P A1B C1B	DA1P* DC1P A1B C1B	DA1P: D-PHY Port A Data Lane 1 Noninverted Output (4-lane mode). DC1P: D-PHY Port C Data Lane 1 Noninverted Output (2-lane mode). A1B: C-PHY Port A Lane 1 Output B (4-lane mode). C1B: C-PHY Port C Lane 1 Output B (2-lane mode).
41	DA1N	DA1N* DC1N A1C C1C	DA1N* DC1N A1C C1C	DA1N: D-PHY Port A Data Lane 1 Inverted Output (4-lane mode). DC1N: D-PHY Port C Data Lane 1 Inverted Output (2-lane mode). A1C: C-PHY Port A Lane 1 Output C (4-lane mode). C1C: C-PHY Port C Lane 1 Output C (2-lane mode).
42	DA2P	DA2P* DD0P A2A D0A	DA2P* DD0P A2A D0A	DA2P: D-PHY Port A Data Lane 2 Noninverted Output (4-lane mode). DD0P: D-PHY Port D Data Lane 0 Noninverted Output (2-lane mode). A2A: C-PHY Port A Lane 2 Output A (4-lane mode). D0A: C-PHY Port D Lane 0 Output A (2-lane mode).

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PIN	NAME	FUNCTION MODE		FUNCTION
		GMSL2	GMSL1	
43	DA2N	DA2N* DD0N A2B D0B	DA2N* DD0N A2B D0B	DA2N: D-PHY Port A Data Lane 2 Inverted Output (4-lane mode). DD0N: D-PHY Port D Data Lane 0 Inverted Output (2-lane mode). A2B: C-PHY Port A Lane 2 Output B (4-lane mode). D0B: C-PHY Port D Lane 0 Output B (2-lane mode).
46	DA3P	DA3P* DD1P A3B D1B	DA3P* DD1P A3B D1B	DA3P: D-PHY Port A Data Lane 3 Noninverted Output (4-lane mode). DD1P: D-PHY Port D Data Lane 1 Noninverted output (2-lane mode). A3B: C-PHY Port A Lane 3 Output B (4-lane mode). D1B: C-PHY Port D Lane 1 Output B (2-lane mode).
47	DA3N	DA3N* DD1N A3C D1C	DA3N* DD1N A3C D1C	DA3N: D-PHY Port A Data Lane 3 Inverted Output (4-lane mode). DD1N: D-PHY Port D Data Lane 1 Inverted Output (2-lane mode). A3C: C-PHY Port A Lane 3 Output C (4-lane mode). D1C: C-PHY Port D Lane 1 Output C (2-lane mode).
44	CKAP	CKAP* CKDP DISABLED A2C D0C	CKAP* CKDP DISABLED A2C D0C	CKAP: D-PHY Port A Clock Lane Noninverted Output (4-lane mode). CKDP: D-PHY Port D Clock Lane Noninverted Output (2-lane mode). DISABLED: D-PHY Clock Output Function is Disabled in 4-Lane Mode When CKAP/N(alt) Function is Enabled, and CKAP/N Pins Drive D-PHY LP00 State. Port A clock output is driven from CKCP/N pins. A2C: C-PHY Port A Lane 2 Output C (4-lane mode). D0C: C-PHY Port D Lane 0 Output C (2-lane mode).
45	CKAN	CKAN* CKDN DISABLED A3A D1A	CKAN* CKDN DISABLED A3A D1A	CKAN: D-PHY Port A Clock Lane Inverted Output (4-lane mode). CKDN: D-PHY Port D Clock Lane Inverted Output (2-lane mode). DISABLED: D-PHY Clock Output Function is Disabled in 4-Lane Mode When CKAP/N(alt) Function is Enabled, and CKAP/N Pins Drive D-PHY LP00 State. Port A clock output is driven from CKCP/N pins. A3A: C-PHY Port A Lane 3 Output A (4-lane mode). D1A: C-PHY Port D Lane 1 Output A (2-lane mode).

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PIN	NAME	FUNCTION MODE		FUNCTION
		GMSL2	GMSL1	
38	CKCP	DISABLED* CKCP CKAP(alt) A0C C0C	DISABLED* CKCP CKAP(alt) A0C C0C	DISABLED: D-PHY Clock Output Function is Disabled by Default in 4-Lane Mode, and CKCP/N Pins Drive D-PHY LP00 State. Port A clock output is driven from CKAP/N pins. CKCP: D-PHY Port C Clock Lane Noninverted Output (2-lane mode). CKAP(alt): D-PHY Port A Clock Lane Noninverted Output Alternate (4-lane mode). When CKAP/N(alt) function is enabled, CKAP/N pins drive D-PHY LP00 state. A0C: C-PHY Port A Lane 0 Output C (4-lane mode). C0C: C-PHY Port C Lane 0 Output C (2-lane mode).
39	CKCN	DISABLED* CKCN CKAN(alt) A1A C1A	DISABLED* CKCN CKAN(alt) A1A C1A	DISABLED: D-PHY Clock Output Function is Disabled by Default in 4-Lane Mode, and CKCP/N Pins Drive D-PHY LP00 State. Port A clock output is driven from CKAP/N pins. CKCN: D-PHY Port C Clock Lane Inverted Output (2-lane mode). CKAN(alt): D-PHY Port A Clock Lane Inverted Output Alternate (4-lane mode). When CKAP/N(alt) function is enabled, CKAP/N pins drive D-PHY LP00 state. A1A: C-PHY Port A Lane 1 Output A (4-lane mode). C1A: C-PHY Port C Lane 1 Output A (2-lane mode).
CSI-2 INTERFACE - PORT B/E/F (* denotes default state after power-up)				
49	DB0P	DB0P* DE0P B0A E0A	DB0P* DE0P B0A E0A	DB0P: D-PHY Port B Data Lane 0 Noninverted Output (4-lane mode). DE0P: D-PHY Port E Data Lane 0 Noninverted Output (2-lane mode). B0A: C-PHY Port B Lane 0 Output A (4-lane mode). E0A: C-PHY Port E Lane 0 Output A (2-lane mode).
50	DB0N	DB0N* DE0N B0B E0B	DB0N* DE0N B0B E0B	DB0N: D-PHY Port B Data Lane 0 Inverted Output (4-lane mode). DE0N: D-PHY Port E Data Lane 0 Inverted Output (2-lane mode). B0B: C-PHY Port B Lane 0 Output B (4-lane mode). E0B: C-PHY Port E Lane 0 Output B (2-lane mode).

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PIN	NAME	FUNCTION MODE		FUNCTION
		GMSL2	GMSL1	
53	DB1P	DB1P* DE1P B1B E1B	DB1P* DE1P B1B E1B	DB1P: D-PHY Port B Data Lane 1 Noninverted Output (4-lane mode). DE1P: D-PHY Port E Data Lane 1 Noninverted Output (2-lane mode). B1B: C-PHY Port B Lane 1 Output B (4-lane mode). E1B: C-PHY Port E Lane 1 Output B (2-lane mode).
54	DB1N	DB1N* DE1N B1C E1C	DB1N* DE1N B1C E1C	DB1N: D-PHY Port B Data Lane 1 Inverted Output (4-lane mode). DE1N: D-PHY Port E Data Lane 1 Inverted Output (2-lane mode). B1C: C-PHY Port B Lane 1 Output C (4-lane mode). E1C: C-PHY Port E Lane 1 Output C (2-lane mode).
55	DB2P	DB2P* DF0P B2A F0A	DB2P* DF0P B2A F0A	DB2P: D-PHY Port B Data Lane 2 Noninverted Output (4-lane mode). DF0P: D-PHY Port F Data Lane 0 Noninverted Output (2-lane mode). B2A: C-PHY Port B Lane 2 Output A (4-lane mode). F0A: C-PHY Port F Lane 0 Output A (2-lane mode).
56	DB2N	DB2N* DF0N B2B F0B	DB2N* DF0N B2B F0B	DB2N: D-PHY Port B Data Lane 2 Inverted Output (4-lane mode). DF0N: D-PHY Port F Data Lane 0 Inverted Output (2-lane mode). B2B: C-PHY Port B Lane 2 Output B (4-lane mode). F0B: C-PHY Port F Lane 0 Output B (2-lane mode).
59	DB3P	DB3P* DF1P B3B F1B	DB3P* DF1P B3B F1B	DB3P: D-PHY Port B Data Lane 3 Noninverted Output (4-lane mode). DF1P: D-PHY Port F Data Lane 1 Noninverted Output (2-lane mode). B3B: C-PHY Port B Lane 3 Output B (4-lane mode). F1B: C-PHY Port F Lane 1 Output B (2-lane mode).
60	DB3N	DB3N* DF1N B3C F1C	DB3N* DF1N B3C F1C	DB3N: D-PHY Port B Data Lane 3 Inverted Output (4-lane mode). DF1N: D-PHY Port F Data Lane 1 Inverted Output (2-lane mode). B3C: C-PHY Port B Lane 3 Output C (4-lane mode). F1C: C-PHY Port F Lane 1 Output C (2-lane mode).

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PIN	NAME	FUNCTION MODE		FUNCTION
		GMSL2	GMSL1	
51	CKBP	CKBP* CKEP DISABLED B0C E0C	CKBP* CKEP DISABLED B0C E0C	CKBP: D-PHY Port B Clock Lane Noninverted Output (4-lane mode). CKEP: D-PHY Port E Clock Lane Noninverted Output (2-lane mode). DISABLED: D-PHY Clock Output Function is Disabled in 4-Lane Mode When CKBP/N(alt) Function is Enabled, and CKBP/N Pins Drive D-PHY LP00 State. Port B clock output is driven from CKFP/N pins. B0C: C-PHY Port B Lane 0 Output C (4-lane mode). E0C: C-PHY Port E Lane 0 Output C (2-lane mode).
52	CKBN	CKBN* CKEN DISABLED B1A E1A	CKBN* CKEN DISABLED B1A E1A	CKBN: D-PHY Port B Clock Lane Inverted Output (4-lane mode). CKEN: D-PHY Port E Clock Lane Inverted Output (2-lane mode). DISABLED: D-PHY Clock Output Function is Disabled in 4-Lane Mode When CKBP/N(alt) Function is Enabled, and CKBP/N Pins Drive D-PHY LP00 State. Port B clock output is driven from CKFP/N pins. B1A: C-PHY Port B Lane 1 Output A (4-lane mode). E1A: C-PHY Port E Lane 1 Output A (2-lane mode).
57	CKFP	DISABLED* CKFP CKBP(alt) B2C F0C	DISABLED* CKFP CKBP(alt) B2C F0C	DISABLED: D-PHY Clock Output Function is Disabled by Default in 4-Lane Mode, and CKFP/N Pins Drive D-PHY LP00 State. Port B clock output is driven from CKBP/N pins CKFP: D-PHY Port F Clock Lane Noninverted Output (2-lane mode). CKBP(alt): D-PHY Port B Clock Lane Noninverted Output Alternate (4-lane mode). When CKBP/N(alt) function is enabled, CKBP/N pins drive D-PHY LP00 state. B2C: C-PHY Port B Lane 2 Output C (4-lane mode). F0C: C-PHY Port F Lane 0 Output C (2-lane mode).

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PIN	NAME	FUNCTION MODE		FUNCTION
		GMSL2	GMSL1	
58	CKFN	DISABLED* CKFN CKBN(alt) B3A F1A	DISABLED* CKFN CKBN(alt) B3A F1A	DISABLED: D-PHY Clock Output Function is Disabled by Default in 4-Lane Mode, and CKFP/N Pins Drive D-PHY LP00 State. Port B clock output is driven from CKBP/N pins CKFN: D-PHY Port F Clock Lane Inverted Output (2-lane mode). CKBN(alt): D-PHY Port B Clock Lane Inverted Output Alternate (4-lane mode). When CKBP/N(alt) function is enabled, CKBP/N pins drive D-PHY LP00 state. B3A: C-PHY Port B Lane 3 Output A (4-lane mode). F1A: C-PHY Port F Lane 1 Output A (2-lane mode).
MULTIFUNCTION PINS **(* denotes default state after power-up)** **(** GMSL1 has limited GPIO tunneling capability; generic GPIO functions are accessible by register read/write only)**				
1	MFP0	MS LMN6 GPIO0*	MS LMN6 GPIO0(*)**	MS: UART Mode Select with Internal 1MΩ Pulldown to Ground. Set MS = low to select base mode. Set MS = high to select bypass mode. MS state may also be temporarily overwritten by a register write. LMN6: Line-Fault Monitor Input 6. Use in conjunction with LMN7 for STP applications. GPIO0: Configurable General Purpose Input or Output. Power-up default is I/O disabled with 1MΩ pulldown to ground.
2	MFP1	LOCK* GPIO1	LOCK* GPIO1**	LOCK: Open-Drain Lock Indication Output with Internal 40kΩ Pullup to V_{DDIO}. GPIO1: Configurable General Purpose Input or Output.
3	MFP2	FSYNC GPIO2*	FSYNC GPI1 GPIO2(*)**	FSYNC: Frame Sync Output (main) or Input (subordinate). GPI1: CMOS Input for Dedicated GPI-GPO Sync Signal GPI1 in GMSL1 Mode. GPIO2: Configurable General Purpose Input or Output. Power-up default is I/O disabled with 1MΩ pulldown to ground.
4	MFP3	ERRB* GPIO3	ERRB* GPIO3**	ERRB: Open-Drain Error Indication Output with Internal 40kΩ Pullup to V_{DDIO}. ERRB = low indicates that a data error or interrupt has been detected. GPIO3: Configurable General Purpose Input or Output.

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PIN	NAME	FUNCTION MODE		FUNCTION
		GMSL2	GMSL1	
13	MFP4	SDA2* RX2* VS GPIO4	SDA2* RX2* GPI0 VS GPIO4**	SDA2: Port 2 I^{2}C Data Input/Open-Drain Output with Internal 40kΩ Pullup to V_{DDIO} (SDA or RX specified by I2CSEL/MFP13 at power-up). RX2: Port 2 UART Input (SDA or RX specified by I2CSEL/MFP13 at power-up). GPI0: CMOS Input for Dedicated GPI-GPO Sync Signal GPI0 in GMSL1 Mode. VS: Vertical Sync Monitor Push-Pull Output. GPIO4: Configurable General Purpose Input or Output.
14	MFP5	SCLK_0 LMN7 GPIO5*	LMN7 GPIO5(*)**	SCLK_0: SPI Interface 0 Clock. When configured as main, push-pull clock output. When configured as subordinate, clock input with internal 1MΩ pulldown to ground. LMN7: Line-Fault Monitor Input 7. Use in conjunction with LMN6 for STP applications. GPIO5: Configurable General Purpose Input or Output. Power-up default is I/O disabled with 1MΩ pulldown to ground.
15	MFP6	MOSI_0 LMN0 GPIO6*	CNTL1 LMN0 GPIO6(*)**	MOSI_0: SPI Interface 0 Main Out Subordinate In. When configured as main, push-pull output that drives data to external subordinate. When configured as subordinate, input with internal 1MΩ pulldown to ground that receives data from external main. CTNL1: GMSL1 Control Output 1 with Push-Pull Driver. Tunnels from corresponding input pin on serializer. LMN0: Line-Fault Monitor Input 0. Use in conjunction with LMN1 for STP applications. GPIO6: Configurable General Purpose Input or Output. Power-up default is I/O disabled with 1MΩ pulldown to ground.
16	MFP7	MISO_0 LMN1 GPIO7*	CNTL2 LMN1 GPIO7(*)**	MISO_0: SPI Interface 0 Main In Subordinate Out. When configured as main, input with internal 1MΩ pulldown to ground that receives data from external subordinate. When configured as subordinate, push-pull output that drives data to an external main. CNTL2: GMSL1 Control Output 2 with Push-Pull Driver. Tunnels from corresponding input pin on serializer. LMN1: Line-Fault Monitor Input 1. Use in conjunction with LMN0 for STP applications. GPIO7: Configurable General Purpose Input or Output. Power-up default is I/O disabled with 1MΩ pulldown to ground.

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PIN	NAME	FUNCTION MODE		FUNCTION
		GMSL2	GMSL1	
28	MFP8	SDA1(ALT) RX1(ALT) BNE_0 SS1_0 LMN2 GPIO8*	SDA1(ALT) RX1(ALT) CNTL3 LMN2 GPIO8(*)**	SDA1(ALT): Alternate Port 1 I^2C Data Input/Open-Drain Output with Internal 40kΩ Pullup to V_{DDIO} (SDA or RX specified by I2CSEL/MFP13 at power-up, user must specify alternate function mapping via register configuration). RX1(ALT): Alternate Port 1 UART Input (SDA or RX specified by I2CSEL/MFP13 at power-up, user must specify alternate function mapping via register configuration). BNE_0: SPI interface 0. When Configured as Subordinate, SPI Buffer Not Empty Push-pull Output. BNE = high indicates SPI data is available. SS1_0: SPI interface 0. When Configured as Main, SPI Subordinate 1 Select Push-Pull Output. CNTL3: GMSL1 Control Output 3 with Push-Pull Driver. Tunnels from corresponding input pin on serializer. LMN2: Line-Fault Monitor Input 2. Use in conjunction with LMN3 for STP applications. GPIO8: Configurable General Purpose Input or Output. Power-up default is I/O disabled with 1MΩ pulldown to ground.
29	MFP9	SCL1(ALT) TX1(ALT) RO_0 SS2_0 LMN3 GPIO9*	SCL1(ALT) TX1(ALT) CNTL0 LMN3 GPIO9(*)**	SCL1(ALT): Alternate Port 1 I^2C Clock Input/Open-Drain Output with Internal 40kΩ Pullup to V_{DDIO} (SCL or TX specified by I2CSEL/MFP13 at power-up, user must specify alternate function mapping via register configuration). TX1(ALT): Alternate Port 1 UART Output with Internal 40kΩ Pullup to V_{DDIO} (SCL or TX specified by I2CSEL/MFP13 at power-up, user must specify alternate function mapping via register configuration). RO_0: SPI Interface 0. When configured as subordinate, SPI mode-select input with internal 1MΩ pulldown to ground. RO = high enables main read from MISO. RO = low enables main write to MOSI. SS2_0: SPI Interface 0. When configured as main, SPI subordinate 2 select push-pull output. CNTL0: GMSL1 Control Output 0 with Push-Pull Driver. Tunnels from corresponding input pin on serializer. LMN3: Line-Fault Monitor Input 3. Use in conjunction with LMN2 for STP applications. GPIO9: Configurable General Purpose Input or Output. Power-up default is I/O disabled with 1MΩ pulldown to ground.

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PIN	NAME	FUNCTION MODE		FUNCTION
		GMSL2	GMSL1	
30	MFP10	FSYNC(ALT) SCLK_1 LMN4 GPIO10*	FSYNC(ALT) GPI2 LMN4 GPIO10(*)**	FSYNC(ALT): Alternate Frame Sync Output (main) or Input (subordinate) (user must specify alternate function mapping via register configuration). SCLK_1: SPI Interface 1 Clock. When configured as main, push-pull clock output. When configured as subordinate, clock input with internal 1MΩ pulldown to ground. GPI2: CMOS Input for Dedicated GPI-GPO Sync Signal GPI2 in GMSL1 Mode. LMN4: Line-Fault Monitor Input 4. Use in conjunction with LMN5 for STP applications. GPIO10: Configurable General Purpose Input or Output. Power-up default is I/O disabled with 1MΩ pulldown to ground.
31	MFP11	SDA1* RX1* MOSI_1 GPIO11	SDA1* RX1* GPIO11**	SDA1: Port 1 I^2C Data Input/Open-Drain Output with Internal 40kΩ Pullup to V_{DDIO} (SDA or RX specified by I2CSEL/MFP13 at power-up). RX1: Port 1 UART Input with Internal 40kΩ Pullup to V_{DDIO} (SDA or RX specified by I2CSEL/MFP13 at power-up). MOSI_1: SPI Interface 1 Main Out Subordinate In. When configured as main, push-pull output that drives data to external subordinate. When configured as subordinate, input with internal 1MΩ pulldown to ground that receives data from external main. GPIO11: Configurable General Purpose Input or Output.
32	MFP12	SCL1* TX1* MISO_1 GPIO12	SCL1* TX1* GPIO12**	SCL1: Port 1 I^2C Clock Input/Open-Drain Output with Internal 40kΩ Pullup to V_{DDIO} (SCL or TX specified by I2CSEL/MFP13 at power-up). TX1: Port 1 UART Output with Internal 40kΩ Pullup to V_{DDIO} (SCL or TX specified by I2CSEL/MFP13 at power-up). MISO_1: SPI Interface 1 Main In Subordinate Out. When configured as main, input with internal 1MΩ pulldown to ground that receives data from external subordinate. When configured as subordinate, push-pull output that drives data to an external main. GPIO12: Configurable General Purpose Input or Output.

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PIN	NAME	FUNCTION MODE		FUNCTION
		GMSL2	GMSL1	
33	MFP13	I2CSEL BNE_1 SS1_1 HS GPO13*	I2CSEL HS CNTL4 GPO13(*)**	I2CSEL: Control-Channel Interface Select Input for all I^2C/UART Interfaces. State is latched at power-up. Function changes to GPO13 after I2CSEL is latched. Connect pullup resistor to V_{DDIO} to select I^2C interface. Connect pulldown resistor to ground to select UART interface. BNE_1: SPI Interface 1. When configured as subordinate, SPI buffer not empty push-pull output. BNE = high indicates SPI data is available. SS1_1: SPI Interface 1. When configured as main, SPI subordinate 1 select push-pull output. HS: Horizontal Sync Monitor Push-Pull Output. CNTL4: GMSL1 Control Output 4 with Push-Pull Driver. Tunnels from corresponding input pin on serializer. GPO13 (GPIO13): Configurable General Purpose Output. Power-up default following I2CSEL state latching is logic low output. GPIO functionality with input receiver can be enabled following power-up by writing ASIL_GPIO_EN = 1.
34	MFP14	SCL2* TX2* RO_1 SS2_1 LMN5 DE GPIO14	SCL2* TX2* GPI3 LMN5 DE GPIO14**	SCL2: Port 2 I^2C Clock Input/Open-Drain Output with Internal 40kΩ Pullup to V_{DDIO} (SCL or TX specified by I2CSEL/MFP13 at power-up). TX2: Port 2 UART Output With Internal 40kΩ Pullup to V_{DDIO} (SCL or TX specified by I2CSEL/MFP13 at power-up). RO_1: SPI Interface 1. When configured as subordinate, SPI mode-select input with internal 1MΩ pulldown to ground. RO = high enables main read from MISO. RO = low enables main write to MOSI. SS2_1: SPI Interface 1. When configured as main, SPI subordinate 2 select push-pull output. GPI3: CMOS Input for Dedicated GPI-GPO Sync Signal GPI3 in GMSL1 Mode. LMN5: Line-Fault Monitor Input 5. Use in conjunction with LMN4 for STP applications. DE: Data Enable Monitor Push-Pull Output. GPIO14: Configurable General Purpose Input or Output.

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PIN	NAME	FUNCTION MODE		FUNCTION
		GMSL2	GMSL1	
63	MFP15	SDA* RX* ODO15/GPI15	SDA* RX* ODO15/GPI15**	SDA: Port 0 I^2C Data Input/Open-Drain Output with Internal 40kΩ Pullup to V_{DDIO} (SDA or RX specified by I2CSEL/MFP13 at power-up). RX: Port 0 UART Input with Internal 40kΩ Pullup to V_{DDIO} (SDA or RX specified by I2CSEL/MFP13 at power-up). ODO15/GPI15: Configurable General Purpose Input and/or Open-Drain Output with Selectable Internal Pullup.
64	MFP16	SCL* TX* ODO16/GPI16	SCL* TX* ODO16/GPI16**	SCL: Port 0 I^2C Clock Input/Open-Drain Output with Internal 40kΩ Pullup to V_{DDIO} (SCL or TX specified by I2CSEL/MFP13 at power-up). TX: Port 0 UART Output with Internal 40kΩ Pullup to V_{DDIO} (SCL or TX specified by I2CSEL/MFP13 at power-up). ODO16/GPI16: Configurable General Purpose Input and/or Open-Drain Output with Selectable Internal Pullup.
MISCELLANEOUS—SEE Table 3				
5	CFG0	CFG0	CFG0	Configuration Pin 0. Voltage at pin sets device mode, which is latched at power-up. Connect to a resistor divider between V_{DDIO} and ground. See Table 9 for configuration details.
12	CFG1	CFG1	CFG1	Configuration Pin 1. Voltage at pin sets device mode, which is latched at power-up. Connect to a resistor divider between V_{DDIO} and ground. See Table 10 for configuration details.
35	PWDNB	PWDNB	PWDNB	Active Low Power-Down Input with 1MΩ Pulldown to Ground. Apply logic low to place device in power-down mode. Connect to V_{DDIO}/logic high for normal operation.
17	X1/OSC	X1	X1	X1: Crystal Input. Connect to either one terminal of a ±200ppm 25MHz crystal OSC: Oscillator support is only for the MAX96712; B variant does not include oscillator support.
18	X2	X2	X2	X2: Crystal Input. Connect to one terminal of a 25MHz ±200ppm crystal.
19	RSVD	RSVD	RSVD	Reserved: Make No Electrical Connection to this Pin.
20	XRES	XRES	XRES	Connect 402Ω 1% Resistor Between XRES and Ground.
POWER SUPPLIES—SEE Table 3				
8,24	V_{DD18}	V_{DD18}	V_{DD18}	1.8V Analog Power Supply. Place decoupling capacitor connected to PCB ground plane as close as possible to each pin.
27	V_{DDIO}	V_{DDIO}	V_{DDIO}	1.8V to 3.3V I/O Power Supply. Place decoupling capacitor connected to PCB ground plane as close to pin as possible.

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PIN	NAME	FUNCTION MODE		FUNCTION
		GMSL2	GMSL1	
48	V_{TERM}	V_{TERM}	V_{TERM}	1.2V CSI C-PHY/D-PHY Power Supply. Place decoupling capacitor connected to PCB ground plane as close to pin as possible.
61,62	V_{DD}	V_{DD}	V_{DD}	1.0V Core Power Supply. This pin includes an optional on-chip LDO. Connect a 1V (0.95V to 1.05V) supply to bypass LDO. Connect a 1.2V (1.14V to 1.26V) supply to use the internal 1.0V regulator. In order to use the internal 1V regulator, first write REG_ENABLE = 1, and then write REG_MNL = 1. Place decoupling capacitor connected to PCB ground plane as close to pin as possible.
9,23	CAP_VDD	CAP_VDD	CAP_VDD	Decoupling Capacitor for 1.0V Core Power Supply. Place decoupling capacitor connected to PCB ground plane as close as possible to each pin. Connect CAP_VDD pins together on board with low impedance copper pour.
EP	EP	EP	EP	Exposed Pad. EP is internally connected to device ground. EP must be connected to the PCB ground plane through an array of vias for proper thermal and electrical performance.

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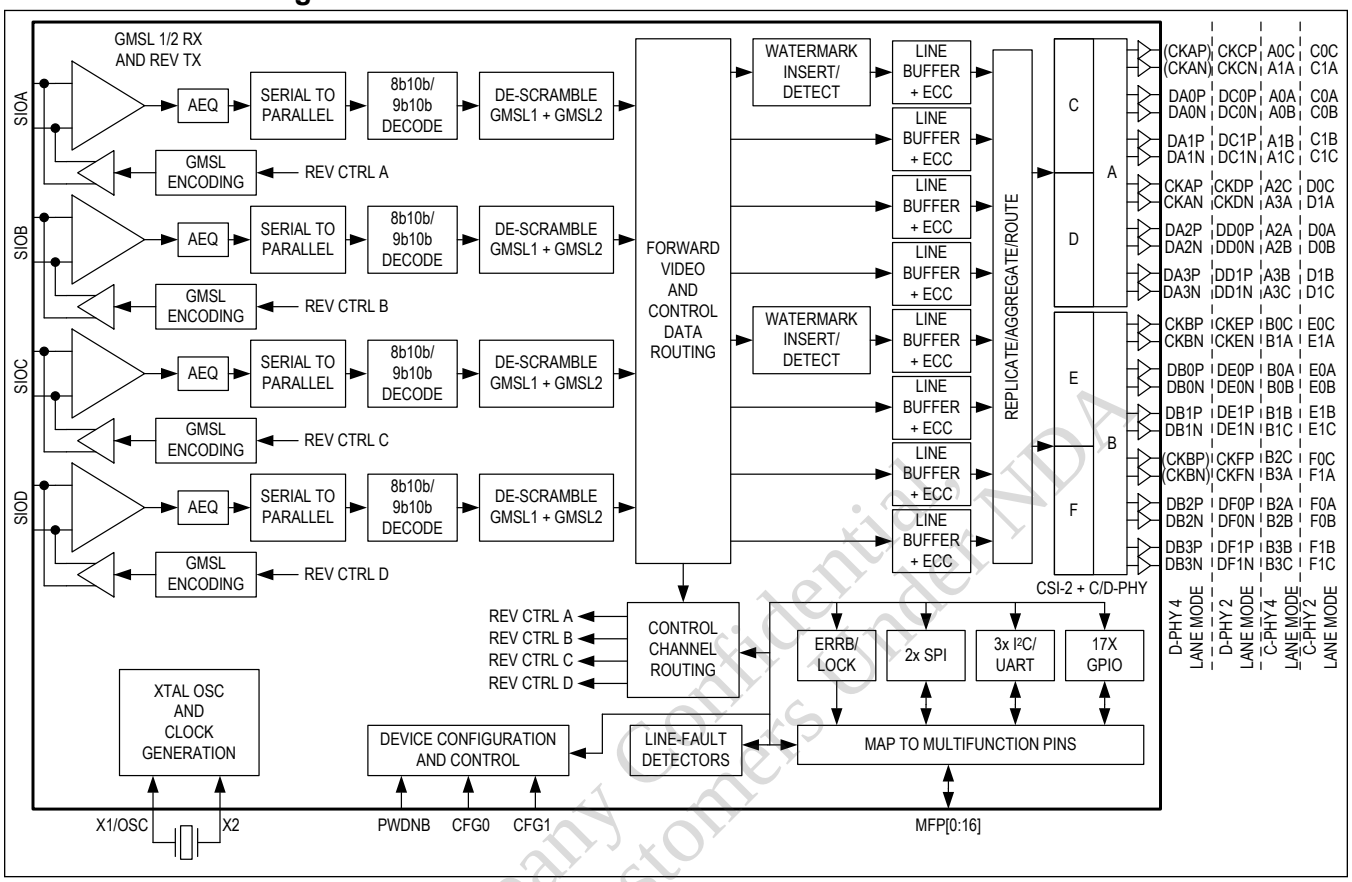
Functional Diagrams

Functional Block Diagram



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Recommended Operating Conditions

Recommended Operating Conditions

Table 2. Recommended Operating Conditions

PARAMETER	PIN	NOMINAL VOLTAGE	MIN	TYP	MAX	UNIT
Supply Range	V_{TERM}		1.14	1.2	1.26	V
	V_{DD18}		1.7	1.8	1.9	
	V_{DD}	1.0V	0.95	1.0	1.05	
		1.2V	1.14	1.2	1.26	
	V_{DDIO}		1.7		3.6	
Maximum Supply Noise (supply noise frequency < 1MHz)	V_{TERM}			50		mVp-p
	V_{DD18}			25		
	V_{DD}	1.0V		25		
		1.2V		50		
	V_{DDIO}	1.8V		50		
		3.3V		100		
Operating Junction Temperature (T_J)			-40		125	ºC

External Component Requirements

Table 3 details critical components that must be connected to the specified pins for correct functionality. This table is not an exhaustive listing of all components that may be needed in a typical application. Please refer to the MAX96712/B EV Kit schematic for a detailed example of a typical application circuit.

Table 3. External Component Requirements

COMPONENT	SYMBOL	CONDITION		VALUE	UNIT
XRES	R_{XRES}	Connect R_{XRES} resistor between XRES pin and ground.		402 ±1%. Use a single resistor.	Ω
Link Isolation Capacitors	C_{LINK}	Place in series with and in close proximity to the SIO pins (pins 6, 7, 10, 11, 21, 22, 25, 26)	GMSL2 Mode, GMSL1 Mode (HIM enabled)	0.1	µF
			GMSL1 Mode (HIM disabled) (also compliant with GMSL2 and GMSL1/ HIM operation)	0.22	
Termination Resistors for SIO_N pins in Coax mode	R_{TERM}	Connect in series with C_{LINK} capacitor between SIO_N and ground when GMSL link is configured in Coax mode. Place near associated SIO_N pin.		49.9 ±1%	Ω
Crystal		Place as close as possible to pins X1/OSC (pin 17) and X2 (pin 18) and connect between these two pins.		25MHz ±200ppm	
Crystal Load Capacitors		Use crystal loading capacitor guidance from the crystal manufacturer. Select values that compensate for X1/OSC (pin 17) and X2 (pin 18) and PCB node capacitances. Place the capacitors as close as possible to pins X1/OSC (pin 17) and X2 (pin 18).			
V_{DDIO} Decoupling Capacitors*		Place 0.01µF capacitor as close as possible to pin V_{DDIO} (pin 27). Include a minimum of 10µF bulk decoupling on the PCB.		0.01+ 10	µF

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Table 3. External Component Requirements (continued)

COMPONENT	SYMBOL	CONDITION		VALUE	UNIT
V_{DD18} Decoupling Capacitors*		Place a 0.01µF capacitor as close as possible to each V_{DD18} pin (pin 8 and pin 24). Include a minimum of 10µF bulk decoupling on the PCB.		(2x) 0.01 + 10	µF
V_{DD} Decoupling Capacitors*		Place a 0.1µF capacitor as close as possible to each V_{DD} pin (pin 61 and pin 62). Include a minimum of 10µF bulk decoupling on the PCB.		(2x) 0.1 + 10	µF
V_{TERM} Decoupling Capacitors*		Place 0.01µF capacitor as close as possible to pin V_{TERM} (pin 48). Include a minimum of 10µF bulk decoupling on the PCB.		0.01 + 10	µF
CAP_VDD Decoupling Capacitors		Place a 0.1µF capacitor as close as possible to each CAP_VDD pin (pin 9 and pin 23). Include a minimum of 10µF bulk decoupling on the PCB.		(2x) 0.1 + 10	µF
Miscellaneous External Resistors		Application-specific. Quantity and values depend on multifunction GPIO pin configurations. Series termination resistors and pullup/pulldown resistors may be required depending on application.			
Resistors for Configuration Pin Resistor Dividers (CFG0, CFG1)	R1, R2	Place resistor divider close to pin CFG0 (pin 5). Resistor values depend on desired configuration.		Use ±1% Tolerance Resistors. See Table 9.	Ω
	R1, R2	Place resistor divider close to pin CFG1 (pin 12). Resistor values depend on desired configuration.		Use ±1% Tolerance Resistors. See Table 10.	Ω
Line-Fault Pulldown Resistor	R_{PD}	Connect to ground at far end of cable opposite active line-fault detector. Line-fault detection cannot be used in conjunction with PoC.		49.9 ± 1%	kΩ
Line-Fault Resistor	R_{EXT}	Connect between GMSL interconnect and LMN line-fault detector input. Line-fault detection cannot be used in conjunction with PoC.	LMN0/2/4/6 STP Mode	42.2 ± 1%	kΩ
			LMN0/2/4/6 Coax Mode	48.7 ± 1%	
			LMN1/3/5/7 STP/ Coax Mode	48.7 ± 1%	
Power-over-Coax (PoC) Network		If PoC is used to power remote camera modules, connect PoC components to active GMSL links to provide remote power feed. Contact the factory for recommended PoC network designs and suggested component placement. The far-end of the link (camera side) should include a corresponding PoC network to receive power if this feature is used. PoC cannot be used in conjunction with line-fault detection.			

* With the exception of CAP_VDD, power supply decoupling capacitor values are recommendations only. It is the responsibility of the board designer to determine what decoupling is necessary for the specific application.

ESD Protection

Table 4. ESD Protection

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
SIO__	V_{ESD}	Human Body Model (HBM), R_D = 1.5kΩ, CS = 100pF		±8		kV
		ISO10605, R_D = 330Ω, CS = 150pF, Contact Discharge, Coax Configuration		±6		
		ISO10605, R_D = 330Ω, CS = 150pF, Contact Discharge, STP Configuration		±4		
		ISO10605, R_D = 330Ω, CS = 150pF, Air Discharge		±8		

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Table 4. ESD Protection (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
		AEC-Q100-011 Rev-C1, Charged Device Model (CDM)		750		V
All Other Pins	V_{ESD}	Human Body Model (HBM), R_D = 1.5kΩ, C_S = 100pF		±4		kV
		AEC-Q100-011 Rev-C1, Charged Device Model (CDM)		750		V

Functional Diagrams

GMSL2 Serial Output Parameters

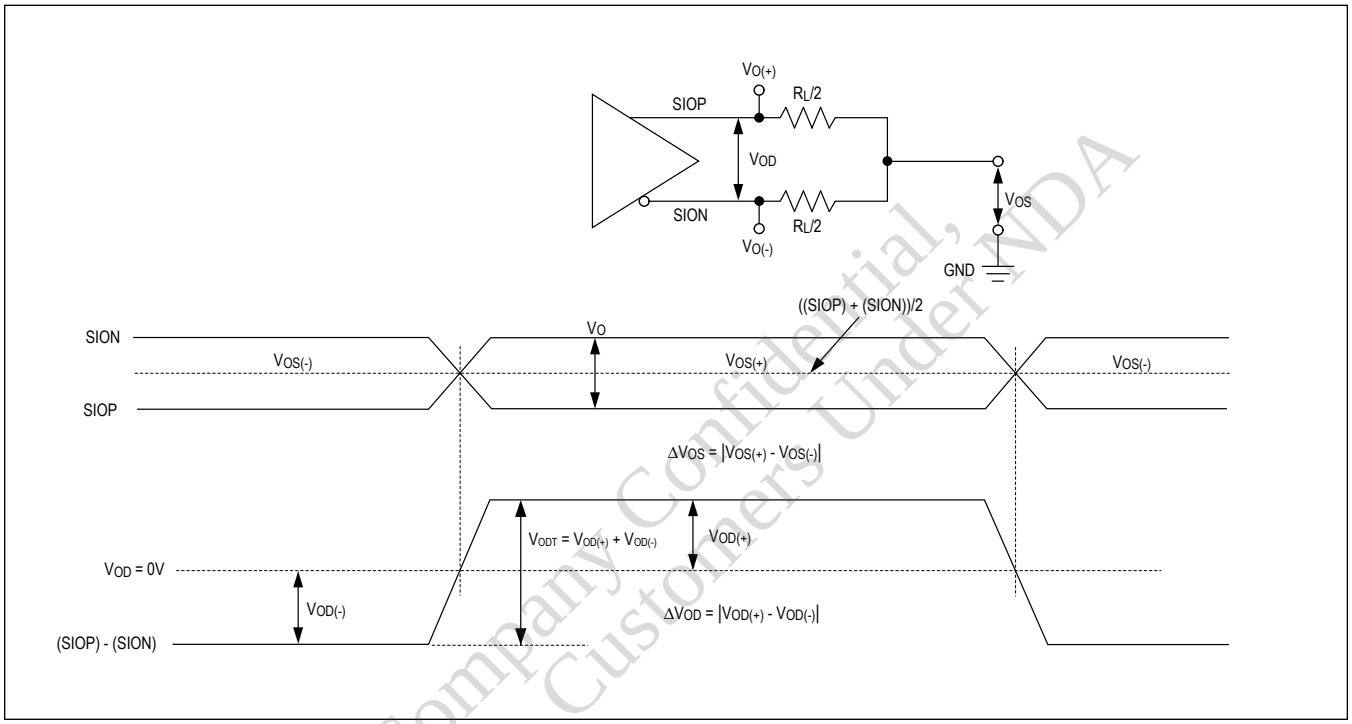

Figure 1. GMSL2 Serial Output Parameters

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GMSL1 Serial Output Parameters

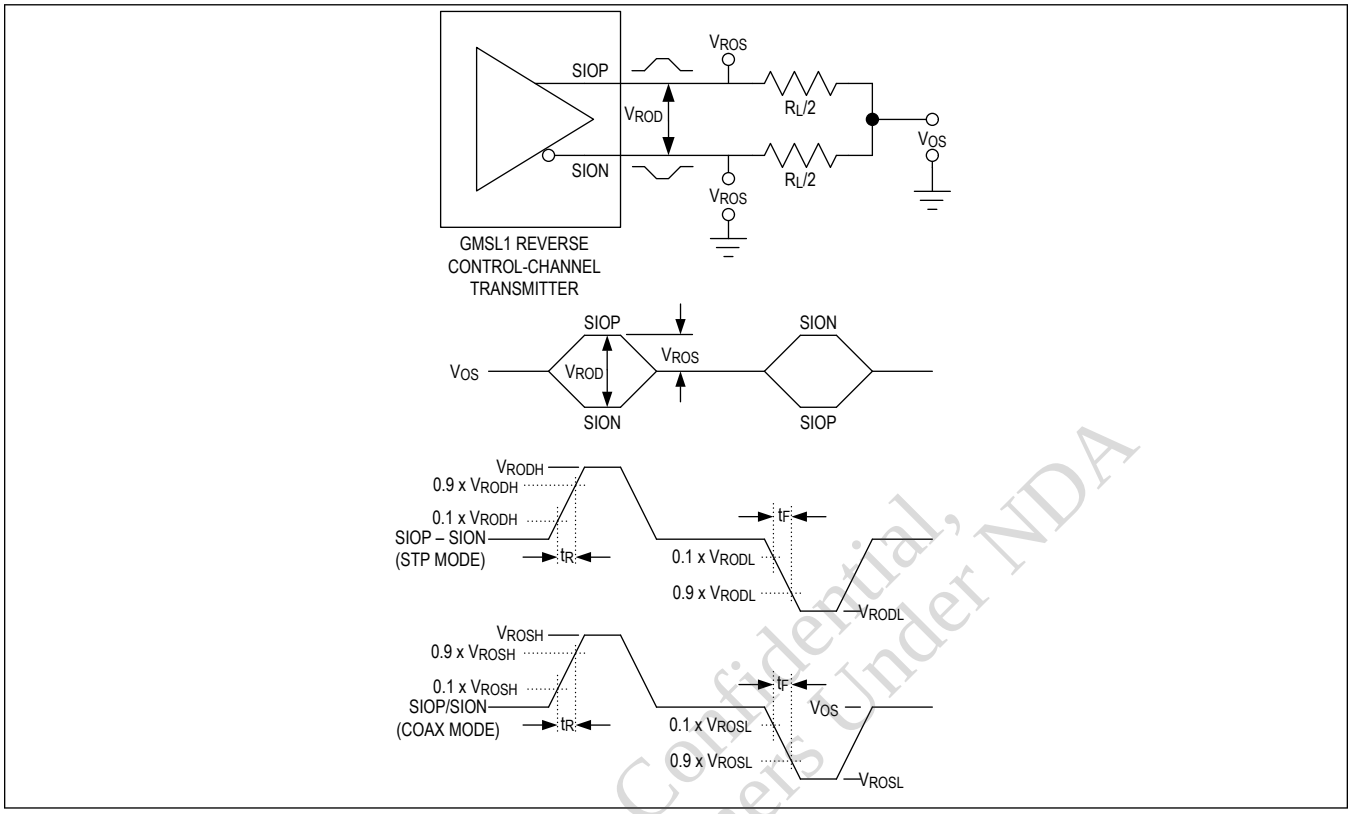

Figure 2. GMSL1 Serial Output Parameters

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D-PHY DC Characteristics

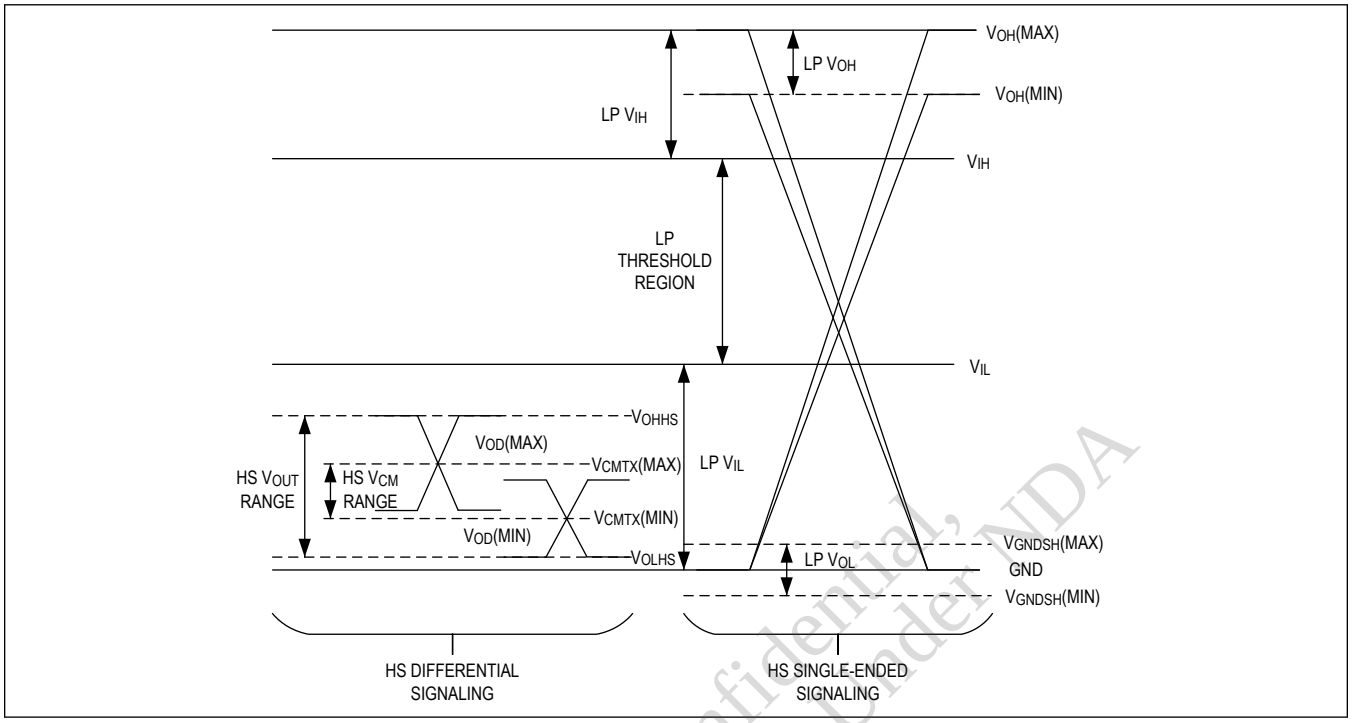

Figure 3. D-PHY DC Characteristics

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D-PHY Possible ΔV_{CMTX} and ΔV_{OD} Distortions of Single-Ended HS Signals

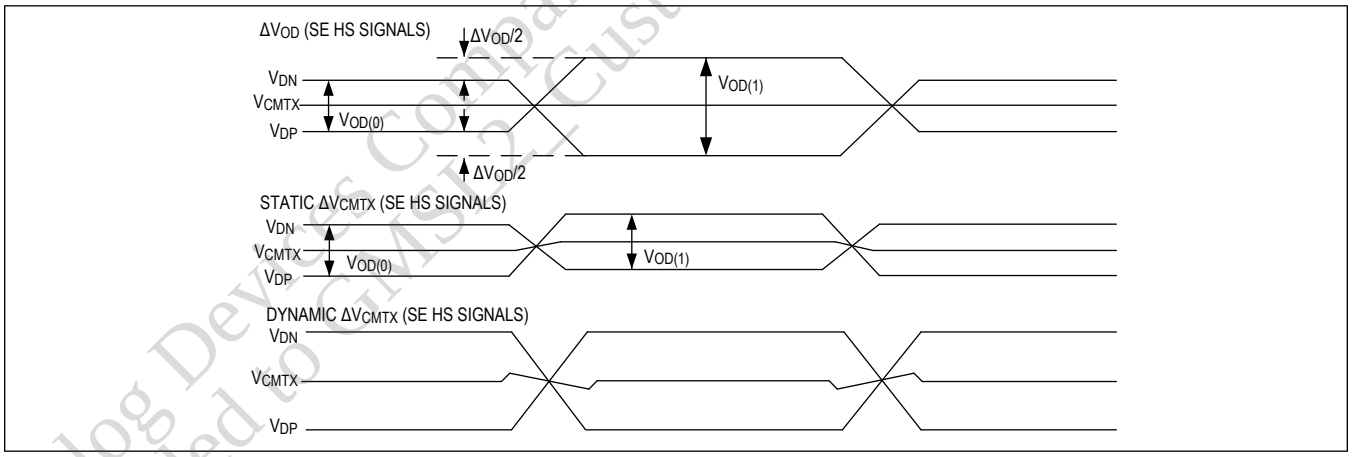

Figure 4. D-PHY Possible ΔV_{CMTX} and ΔV_{OD} Distortions of Single-Ended HS Signals

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D-PHY Ideal Single-Ended and Resulting Differential HS Signals

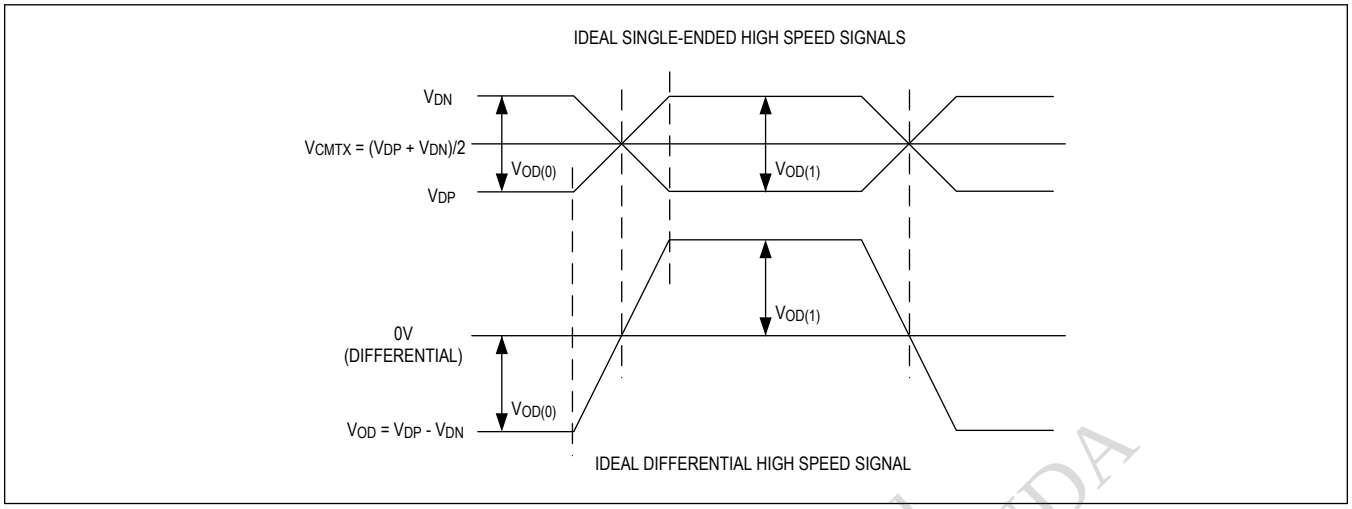

Figure 5. D-PHY Ideal Single-Ended and Resulting Differential HS Signals

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C-PHY DC Characteristics

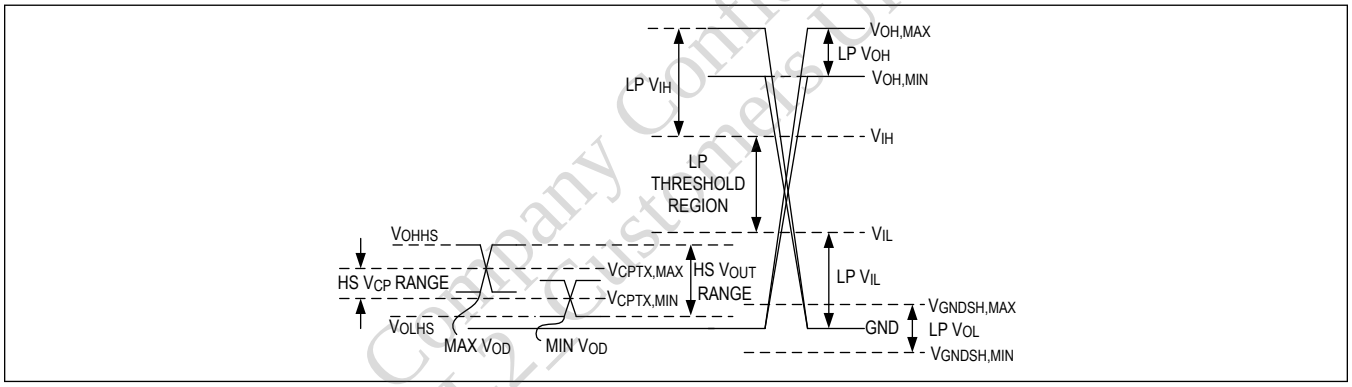

Figure 6. C-PHY DC Characteristics

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C-PHY Possible ΔV_{CPTX} and ΔV_{OD} Distortions of Single-Ended HS Signals

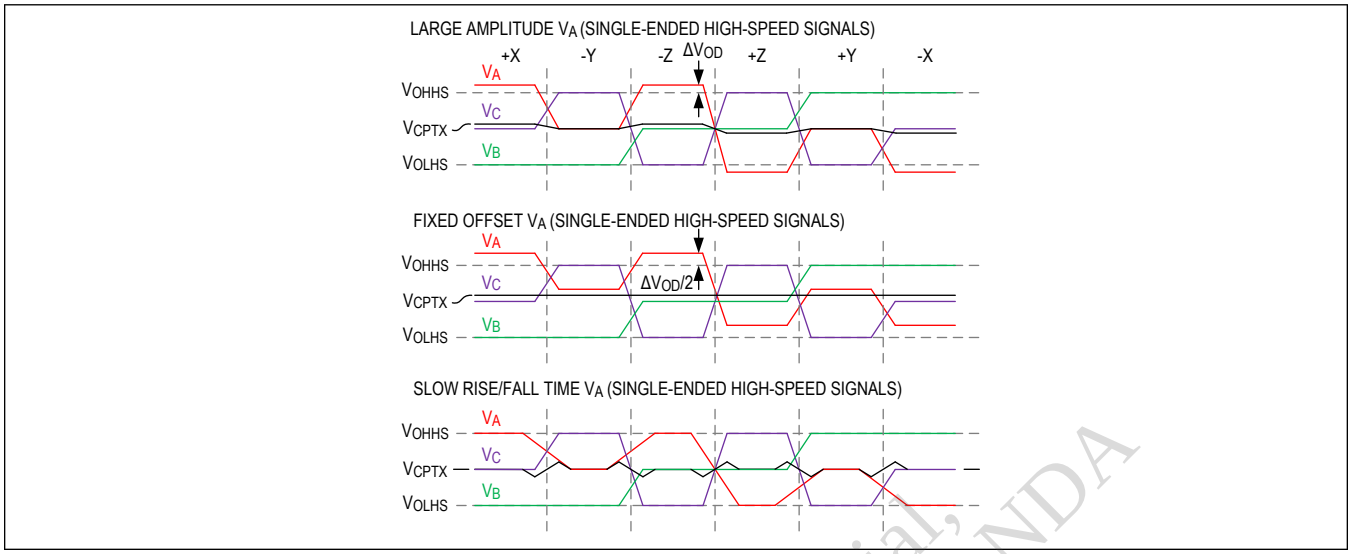

Figure 7. C-PHY Possible ΔV_{CPTX} and ΔV_{OD} Distortions of Single-Ended HS Signals

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C-PHY Ideal Single-Ended and Resulting Differential High-Speed Signals

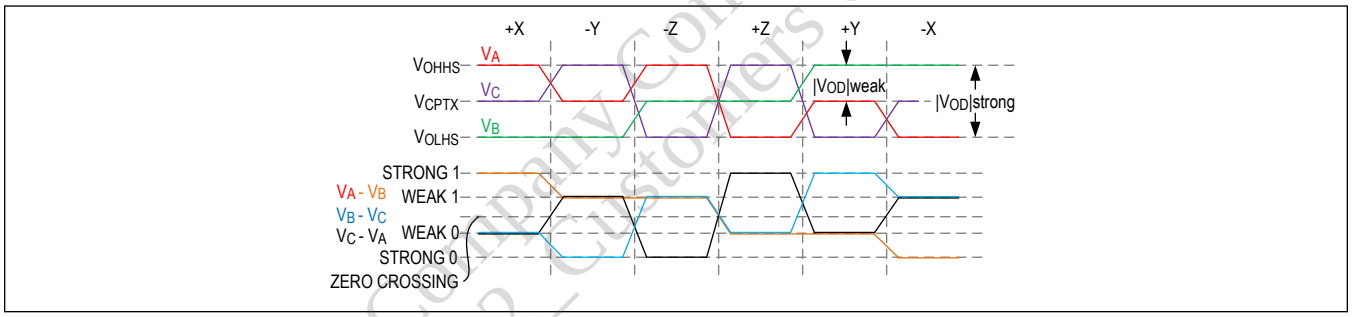

Figure 8. C-PHY Ideal Single-Ended and Resulting Differential High-Speed Signals

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GMSL2 Video Latency

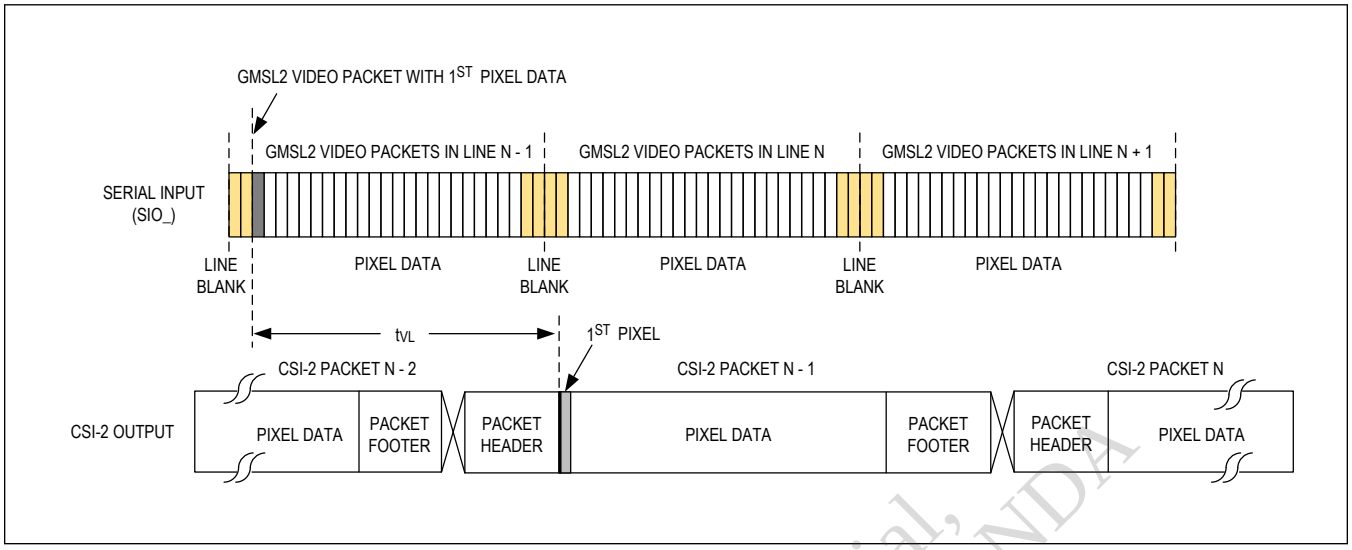

Figure 9. GMSL2 Video Latency

GMSL2 GPI-to-GPO Delay and Skew

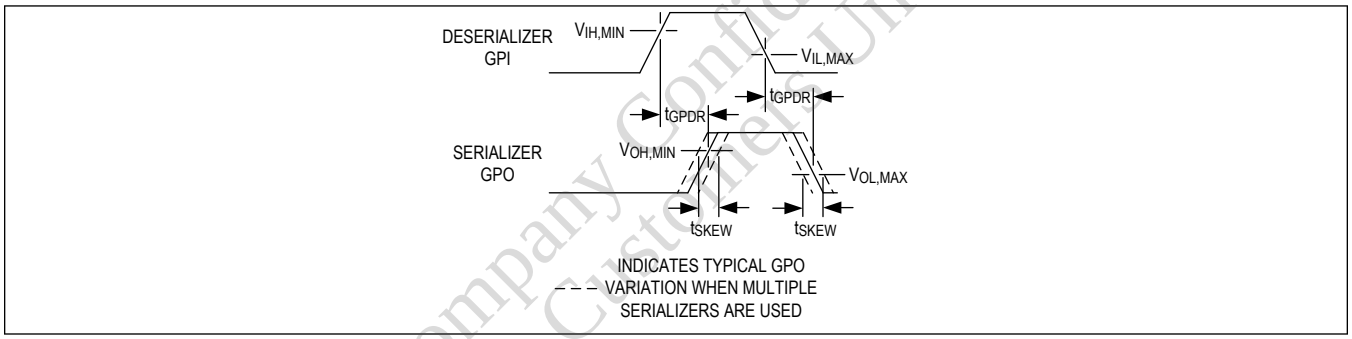

Figure 10. GMSL2 GPI-to-GPO Delay and Skew

GMSL1 Lock Time

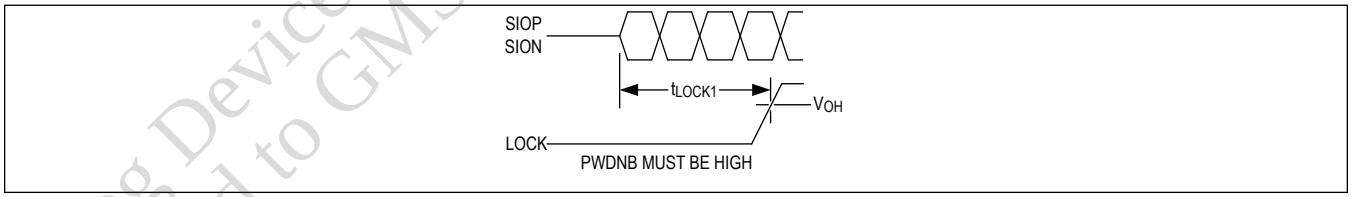

Figure 11. GMSL1 Lock Time

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GMSL1 Power-up Delay

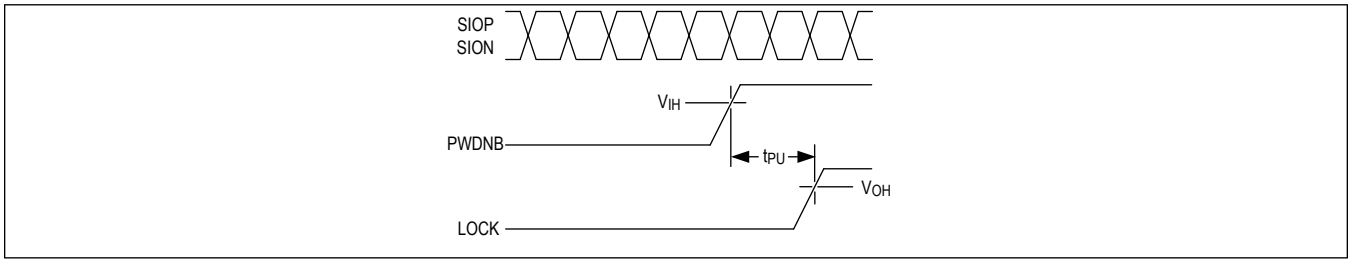

Figure 12. GMSL1 Power-up Delay

GMSL1 Video Latency

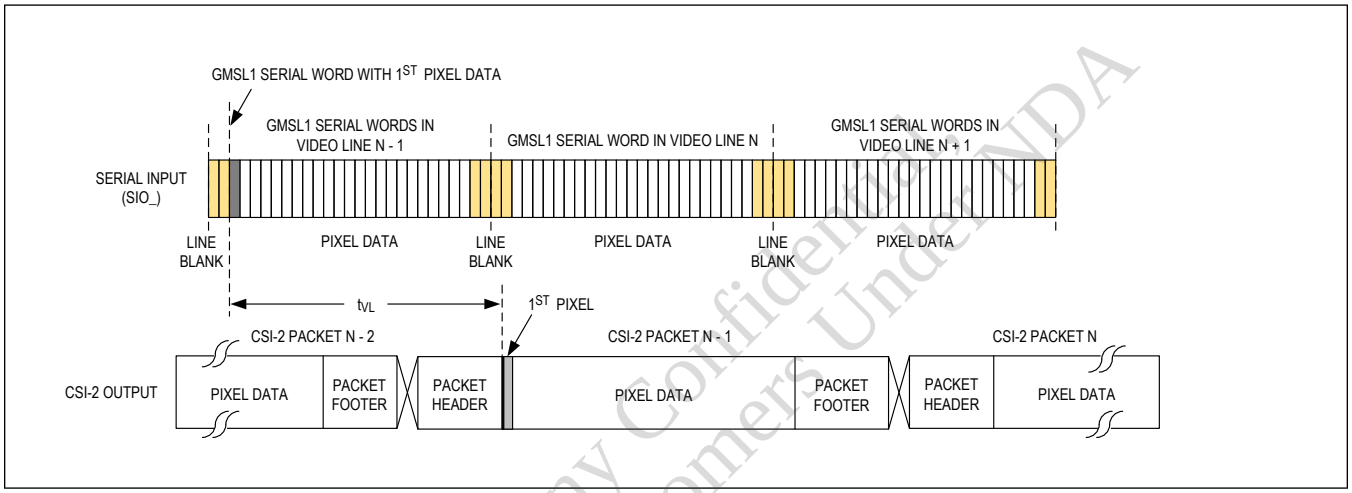

Figure 13. GMSL1 Video Latency

GMSL1 GPI-to-GPO Delay

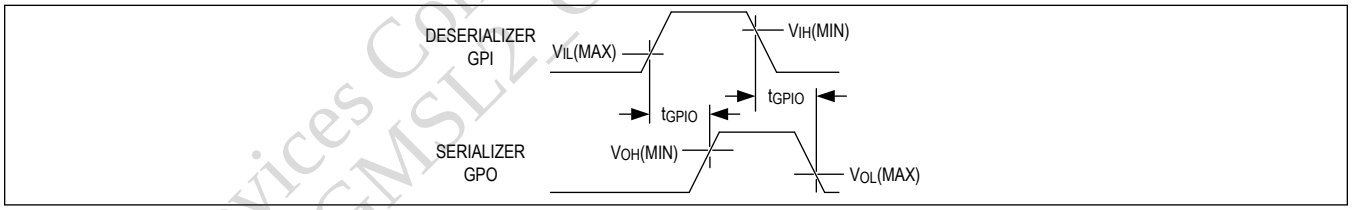

Figure 14. GMSL1 GPI-to-GPO Delay

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D-PHY HS Burst Data Transmission

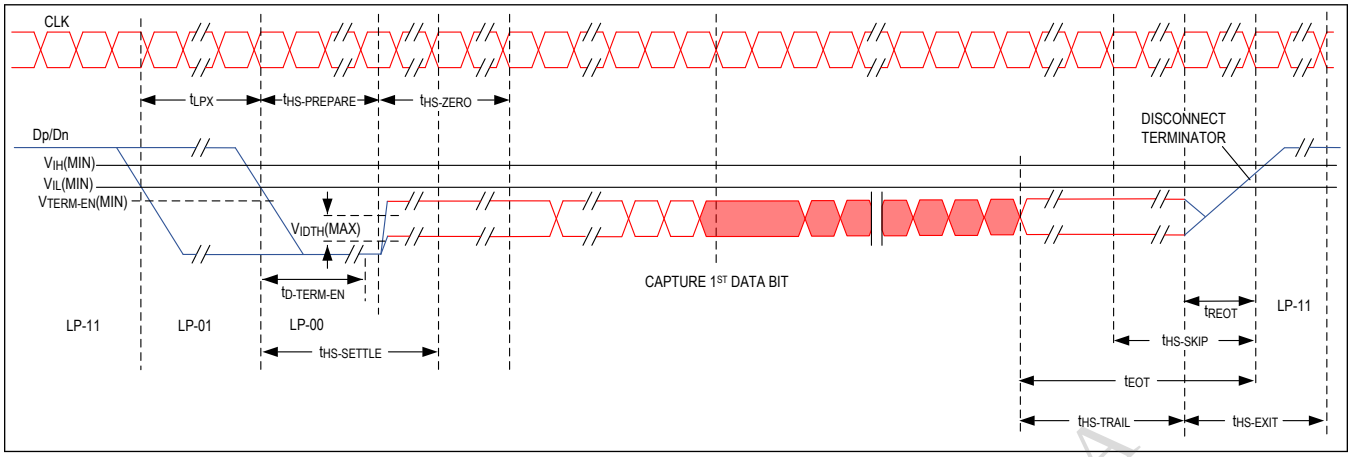

Figure 15. D-PHY HS Burst Data Transmission

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D-PHY Data Clock Timing

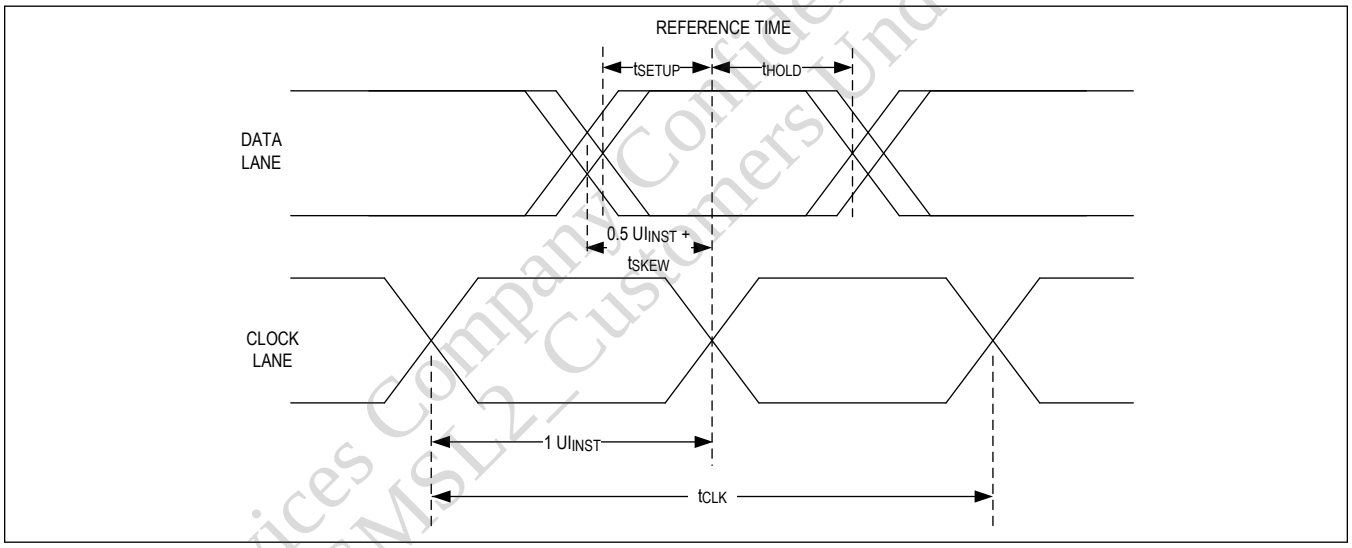

Figure 16. D-PHY Data Clock Timing

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D-PHY High-Speed Skew Calibration

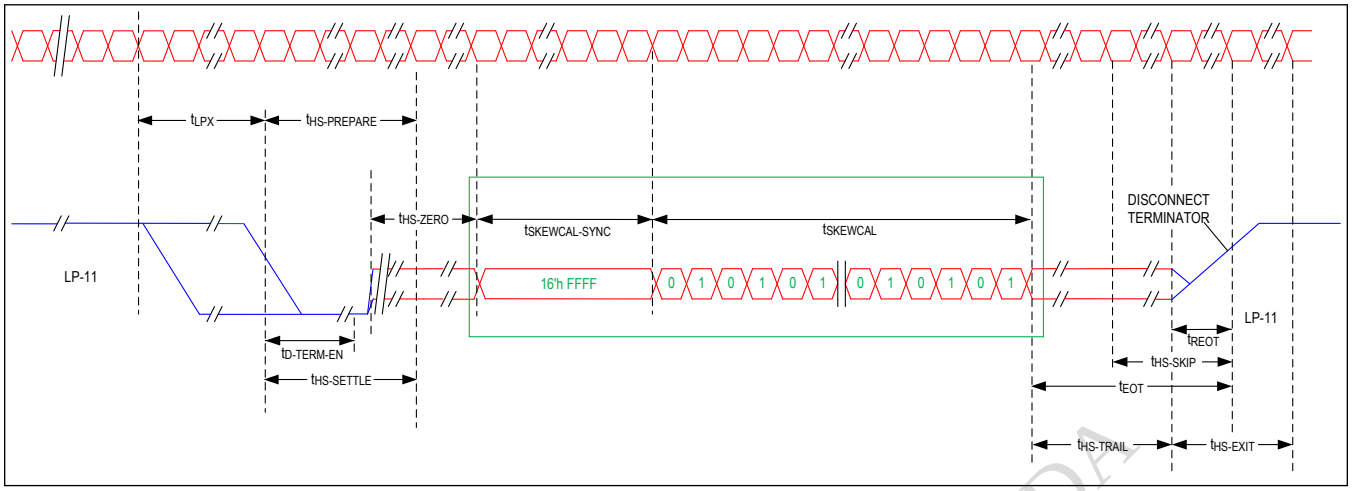

Figure 17. D-PHY High-Speed Skew Calibration

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D-PHY Switching Clock Lane From Active Transmission to Low-Power Mode

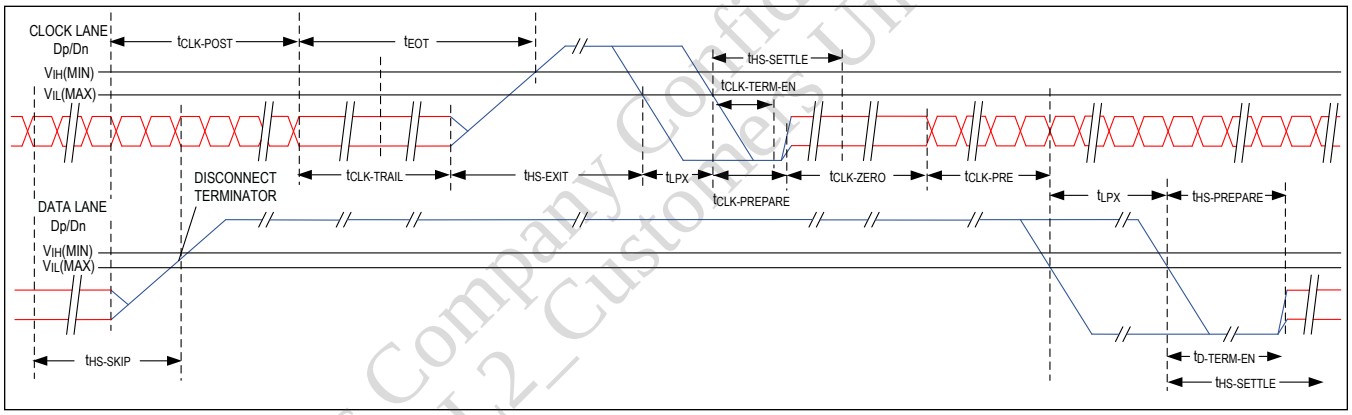

Figure 18. D-PHY Switching Clock Lane From Active Transmission to Low-Power Mode

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C-PHY HS Burst Data Transmission

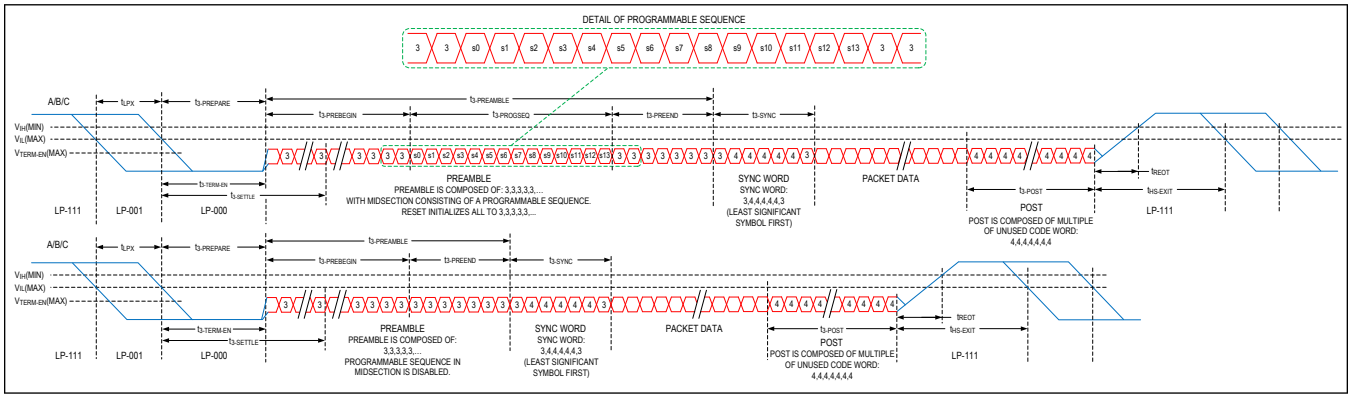

Figure 19. C-PHY HS Burst Data Transmission

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I²C Timing Parameters

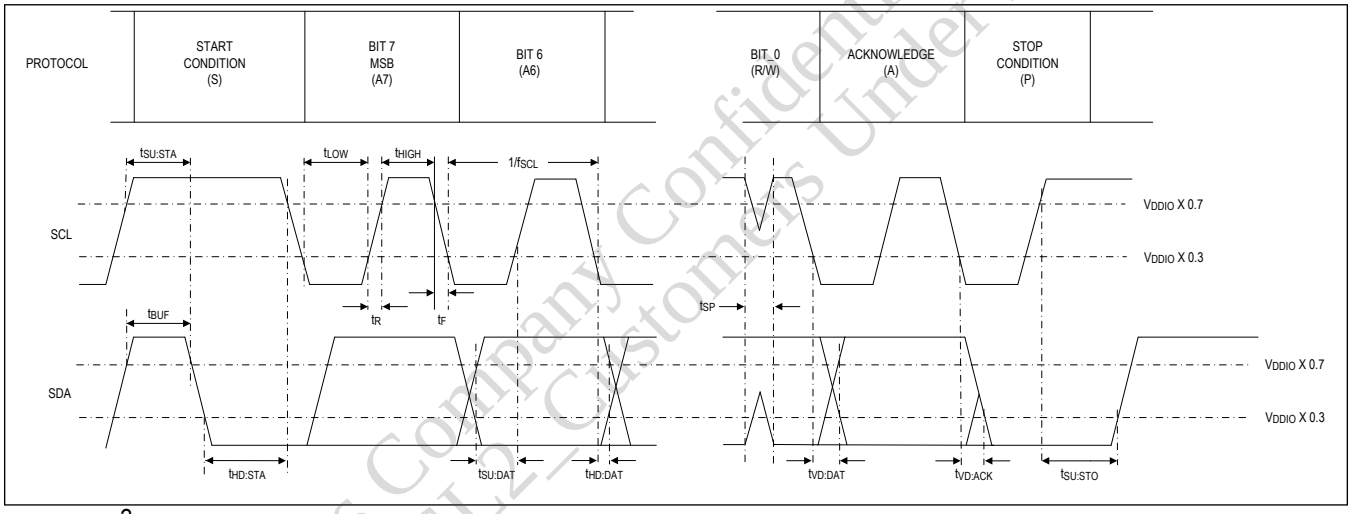

Figure 20. I²C Timing Parameters

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SPI Main Mode Timing Parameters

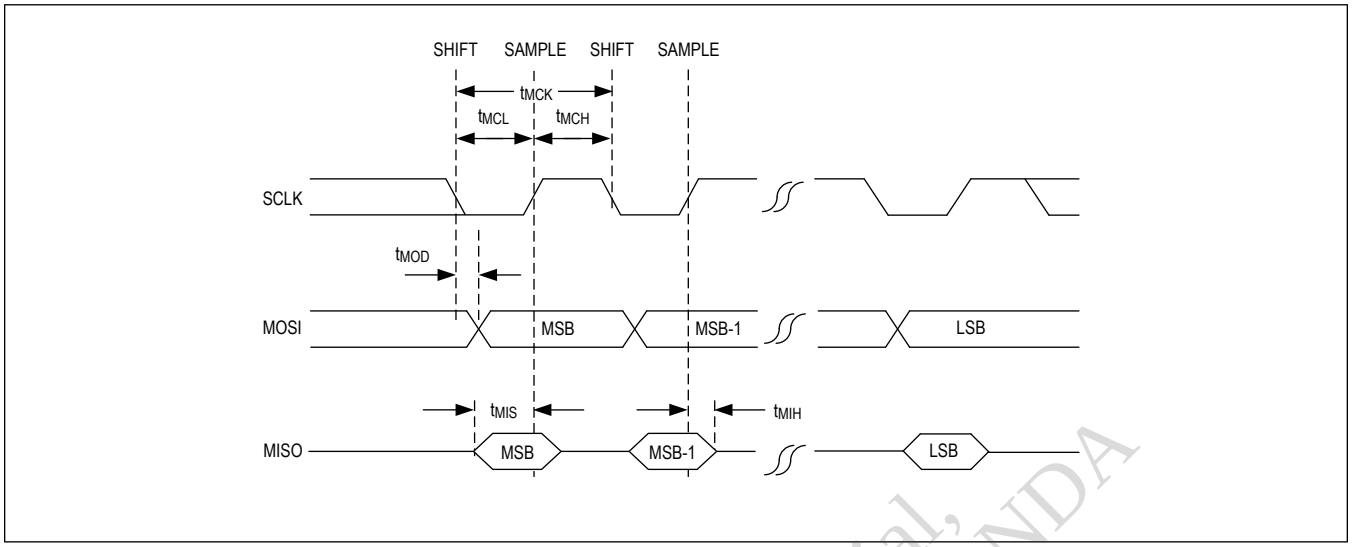

Figure 21. SPI Main Mode Timing Parameters

SPI Subordinate Mode Timing Parameters

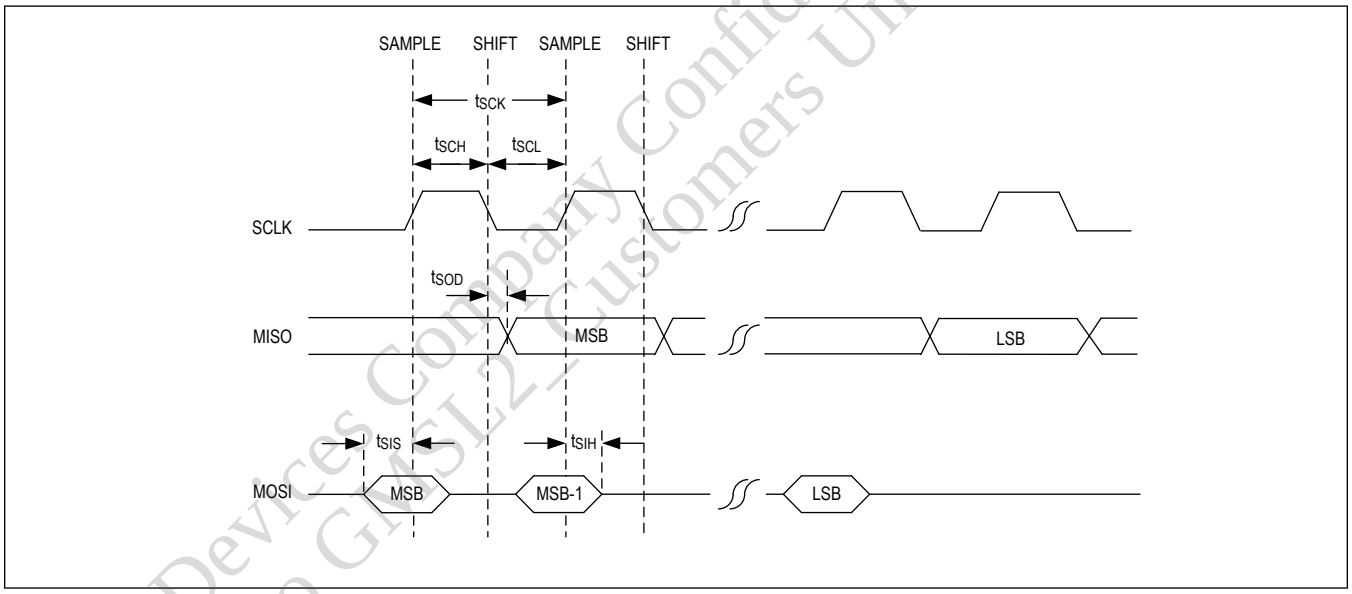

Figure 22. SPI Subordinate Mode Timing Parameters

Detailed Description

Additional Documentation

This data sheet contains electrical specifications, pin and functional descriptions, feature overviews, and register definitions. Designers must also have the following information to correctly design using this device:

- The **GMSL2 Channel Specification** contains physical layer requirements for the PCB traces, cables, and connectors

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that constitute the GMSL2 link.

- The **GMSL2 Hardware Design Guide** contains recommendations for PCB design, applications circuits, selection of external components, and guidelines for use of GMSL2 signal integrity tools.
- The **GMSL2 User Guide** contains detailed programming guidelines for GMSL2 device features.
- **Errata sheets** contain deviations from published device specifications and are specific to part number and revision ID.

Contact the factory to receive these documents and for additional guidance on MAX96712/B features.

Introduction

Analog Devices' GMSL2 serializers and deserializers provide sophisticated link management for high-speed, low bit-error-rate, bidirectional serial data transport. They support a comprehensive suite of display, camera, and communication interfaces over a single wire.

GMSL2 provides up to 6Gbps forward and 187.5Mbps reverse packetized data transmission over each fixed-speed link. The MAX96712/B's inputs can be aggregated such that incoming data from four remotely located sensors is combined and routed to any available combination of CSI outputs. With this capability, it is possible to transport data from four remote sensors to an SoC using a single CSI-2 port.

The following sections provide a brief overview of the device functions and features. Contact the factory for additional information and details on the configuration of each function and feature.

Product Overview

The MAX96712/B deserializer converts four GMSL2 or GMSL1 inputs to up to four independent MIPI CSI-2 C/D-PHY outputs containing a combined total of up to eight lanes. It also sends and receives control channel data, enabling full-duplex transmission of forward path video and bidirectional control data over low-cost 50Ω coax or 100Ω STP cables that meet the GMSL2 channel specification. In backward compatible GMSL1 mode, the MAX96712/B can be paired with 3.12Gbps or 1.5Gbps GMSL1 serializers or operate up to 3.12Gbps with GMSL2 serializers operated in GMSL1 mode.

The MAX96712/B has dual 4-lane or quad 2-lane CSI-2 v1.3 output ports which support data-rates of 80Mbps to 2.5Gbps per lane in D-PHY mode or 182Mbps to 5.7Gbps per lane in C-PHY mode. The number of active data lanes in each CSI-2 port is programmable with 4-lane ports providing one, two, three, or four lanes and 2-lane ports providing one or two lanes. Supported data types include RAW8/10/12/14/16/20, RGB565/666/888, YUV422 8/10-bit, user-defined, and generic long packet data types. Up to 16 virtual channels are supported in D-PHY mode while C-PHY mode provides up to 32 virtual channels, enabling flexible routing of separate data streams.

The MAX96712/B is intended to be paired with GMSL2 serializers or previous generation GMSL1 serializers. Several common multisensor use cases are supported with the MAX96712/B being particularly well suited to surround-view sensor systems that include four physically separate cameras or other sensors. The simplest conceptual system following this topology includes four independent sensors, each with a serializer, routed to the MAX96712/B's four GMSL inputs. The resulting CSI-2 streams from each sensor are then routed separately to the four independent CSI-2 C/D-PHY outputs, providing a system with four independent inputs and outputs where each input's data is uniquely routed to a dedicated output. This scenario is detailed in Figure 23.

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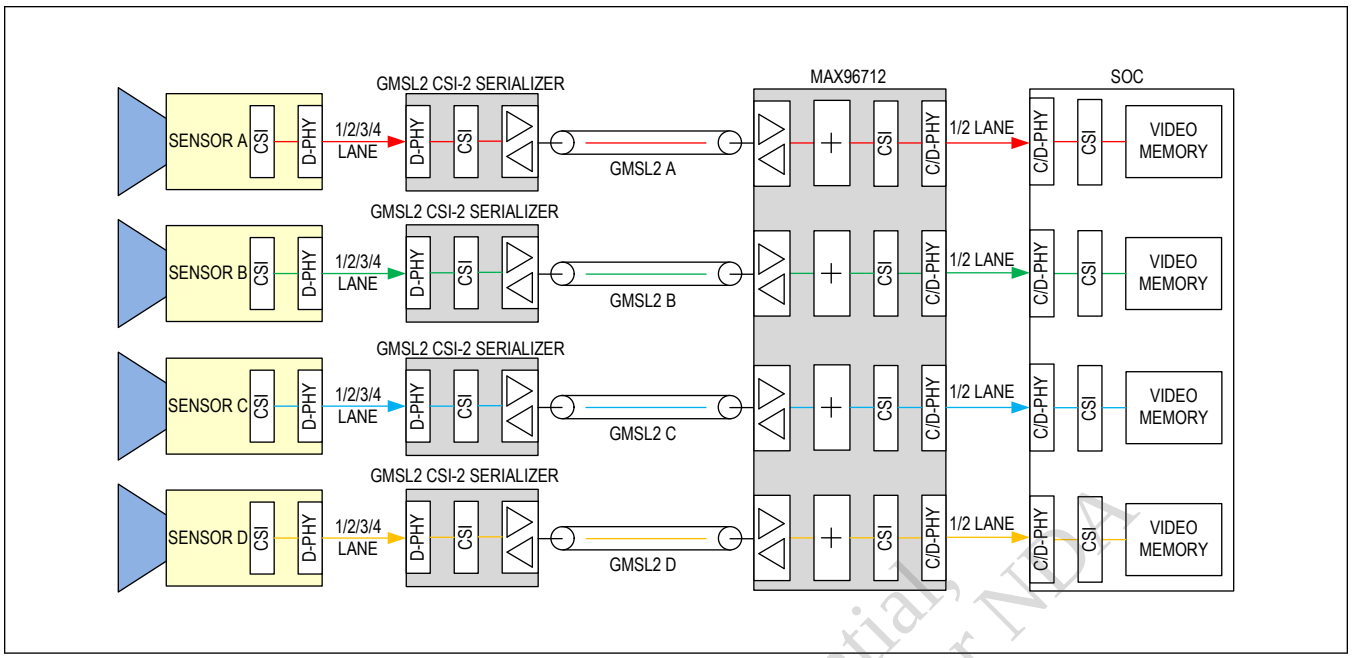

Figure 23. Four Independent Sensors with Dedicated CSI-2 Interfaces

A similar example is the case where each GMSL link streams data from more than one sensor. The MAX9295D serializer, for example, includes a pair of independent CSI-2 input ports. As a result, each remote sensor location using this device could interface to two independent sensors with multiple data types. In this case, the data from each pair of remotely located sensors is separated within a given link by appropriately mapping the virtual channel of each source. The total combined video throughput shared by each pair of remotely located sensors is 6Gbps (minus GMSL2 overhead), and each sensor can utilize a unique output format (GMSL2 only, may be limited by the number of available video pipes). An example of this system is shown in Figure 24. Each of the MAX96712/B's four GMSL inputs can be independently configured to create a system consisting of a hybrid of those shown in Figure 23 and Figure 24. In this case, some links support a single sensor while other links support multiple sensors, each of which has a unique output format. (This applies in GMSL2 mode only when multiple sensors utilize a common link).

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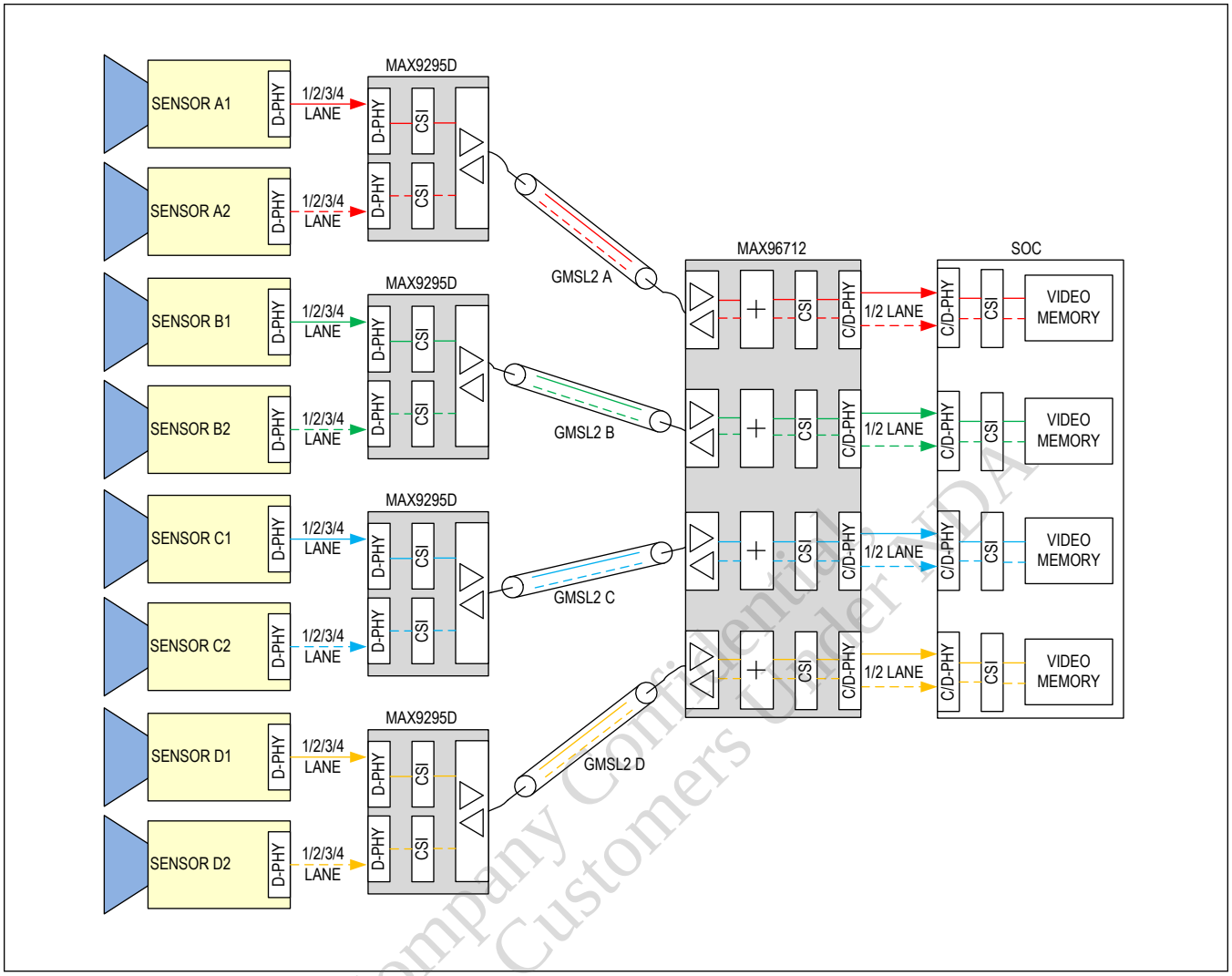

Figure 24. Four Independent Dual Sensors with Dedicated CSI-2 Interfaces

The MAX96712/B also supports data aggregation and replication. These features allow simultaneous streams from different sensors to be combined within a single CSI-2 output stream (aggregation) and then routed to multiple CSI-2 output ports (replication). Thus, data from several sensors can be combined into a single stream that connects to more than one SoC. The result is a more efficient utilization of SoC input resources, because the combined stream is transferred to a single CSI-2 port on each SoC.

The sensors can have different video timing and resolution. The SoC identifies the video source by reading each packet's virtual channel ID. If both sources initially use the same virtual channel, the MAX96712/B reassigns virtual channels so that separate streams can be identified by the SoC.

Figure 25 illustrates an example of four sensor streams combined by the MAX96712/B into a single CSI port that streams data from all sensors to the SoC.

Alternatively, partial aggregation is also possible. In this case, data from some sensors is combined within a common CSI stream while data from other sensors is concurrently routed to separate, independent CSI ports. (See Figure 26.) In general, any incoming stream with a unique virtual channel ID can be independently routed to any CSI output regardless of which GMSL input sources the data. Each CSI output can simultaneously stream many virtual channels, enabling a single CSI port to transfer data from a wide range of remote sensors in physically separate locations.

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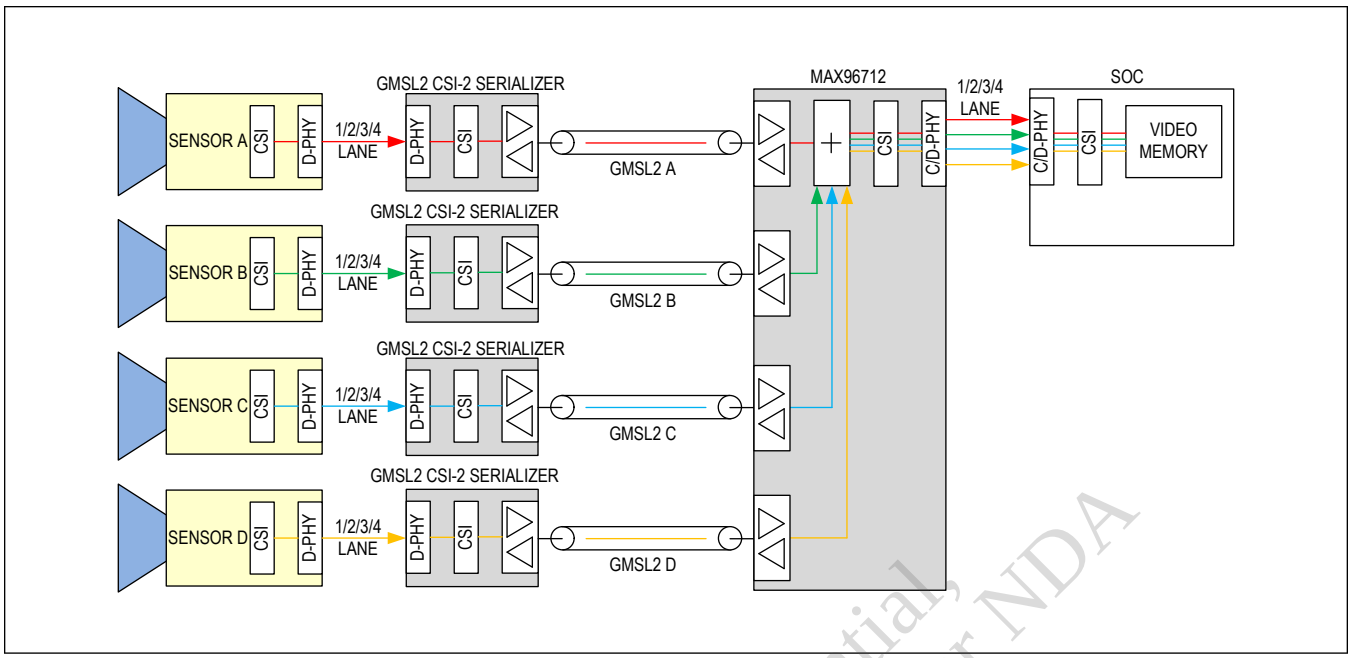

Figure 25. Four Independent Sensors Aggregated to a Single CSI-2 Output

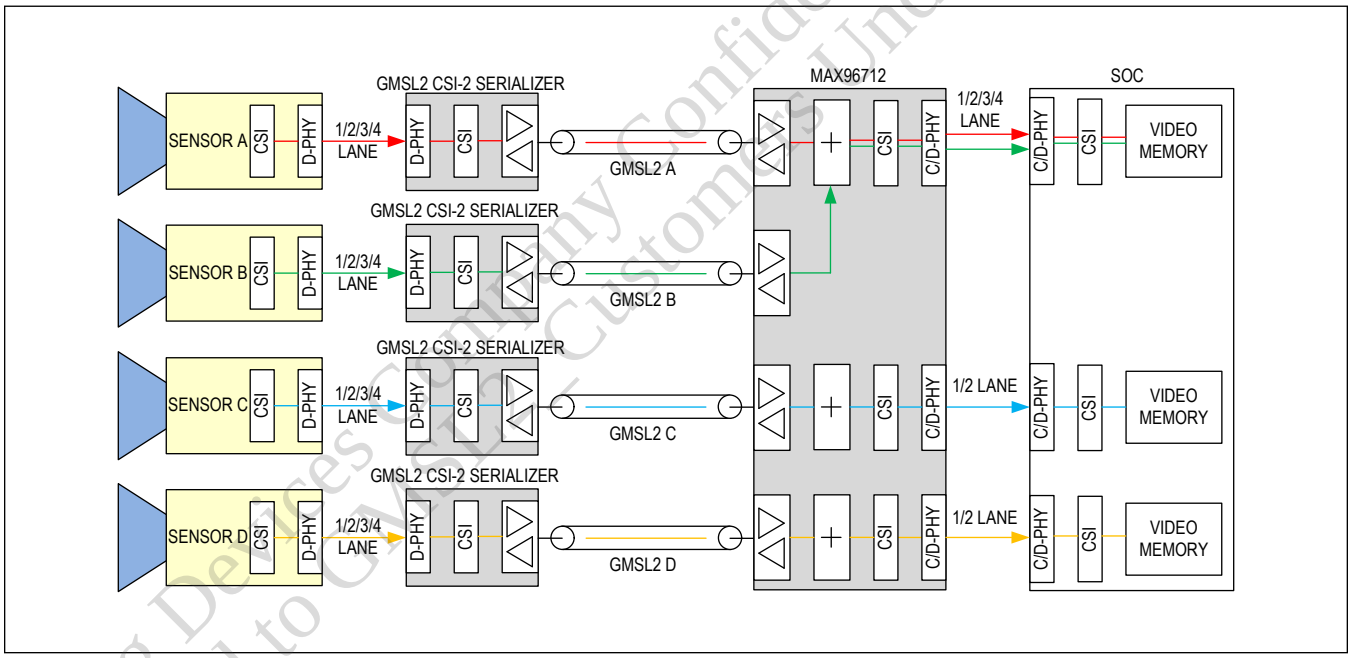

Figure 26. Four Independent Sensors Utilizing Partial Aggregation

Some applications require the video stream to be processed in parallel by multiple devices. In these cases, a single CSI-2 stream must be routed to multiple physical CSI-2 interfaces. The MAX96712/B accommodates this requirement with the ability to replicate the output of any of the CSI-2 controllers to multiple C/D-PHY outputs as shown in Figure 27.

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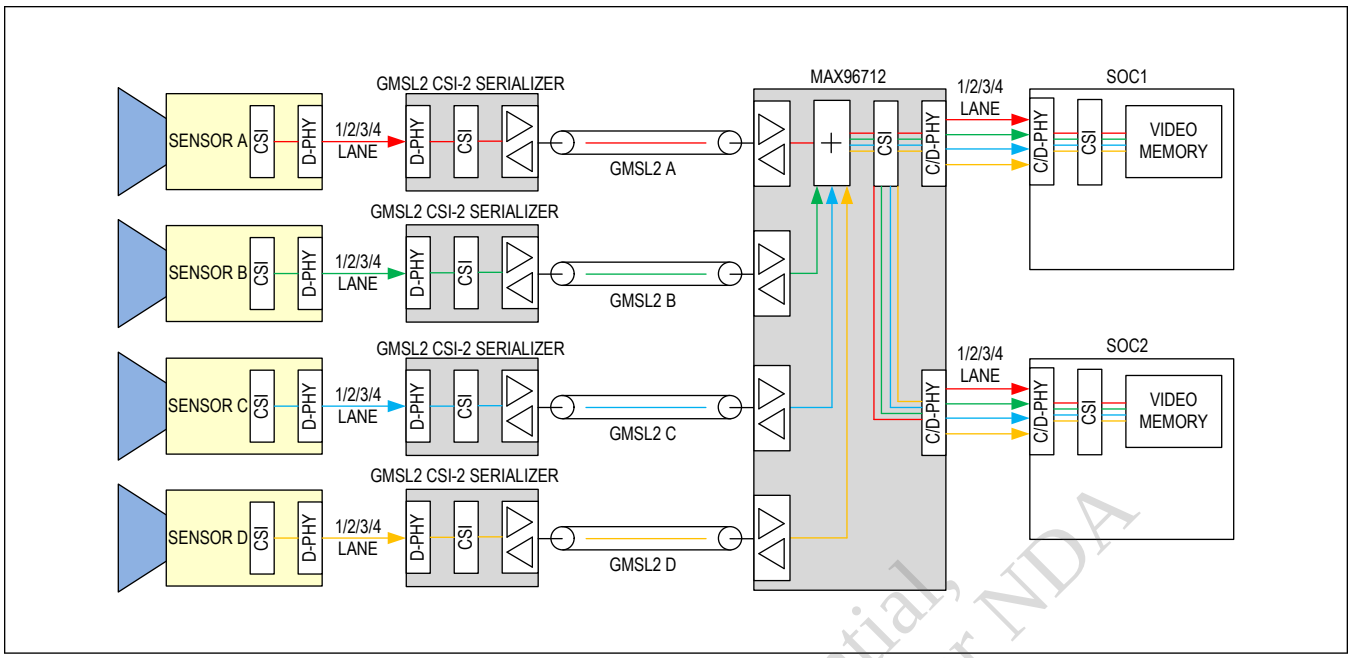

Figure 27. Four Independent Sensors Aggregated to a Single CSI-2 Stream and Replicated to Two PHY Outputs

The MAX96712/B's ability to simultaneously accommodate a variety of sensors with varied output formats extends to the GMSL link portion of the system. Each of the four links can independently accommodate a GMSL1 or GMSL2 serializer operating at any supported link rate. Each serializer can utilize any supported video input interface and format (within the constraints of the number of available video pipes). This enables a single MAX96712/B to simultaneously interface with up to four unique types of sensors, each utilizing a different serializer with its own link configuration and video interface. The incoming data streams can be aggregated, enabling a single CSI-2 port to transfer all video data regardless of the serializer and link configuration used by each of the sensors. Figure 28 illustrates an example of a mixed parallel GMSL1/CSI GMSL2 system with four sensors.

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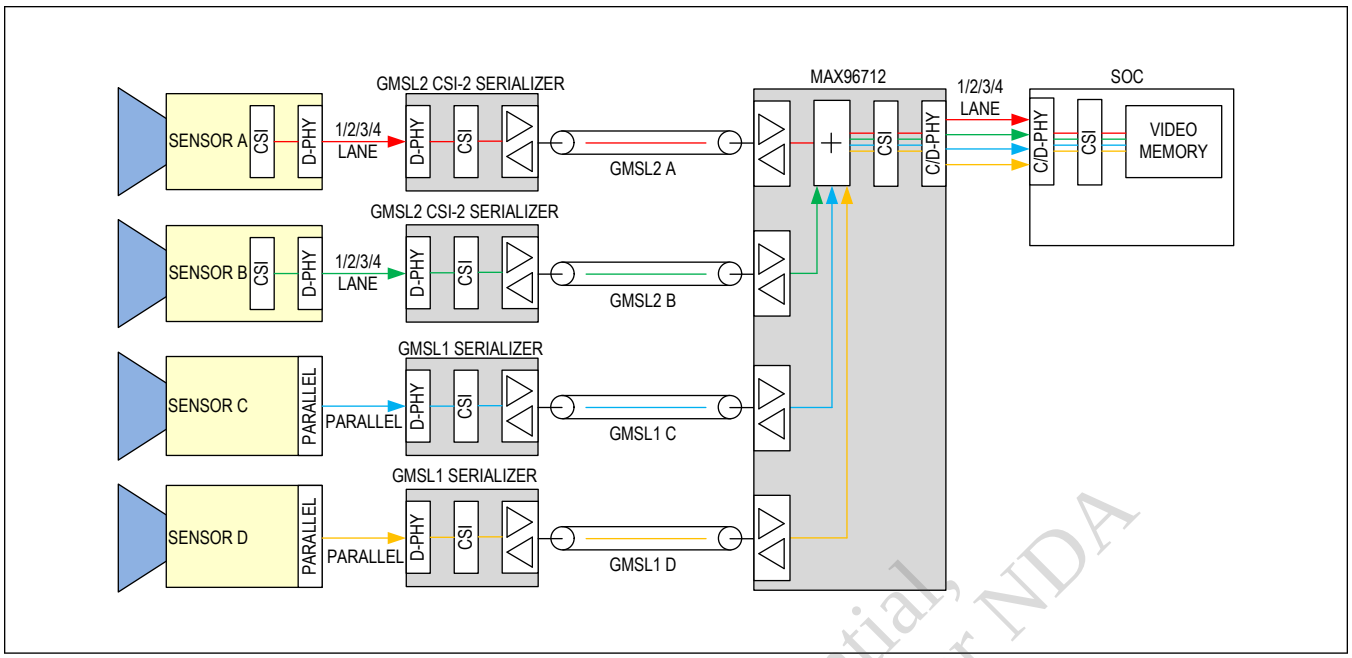

Figure 28. Four Independent Sensors with Mixed GMSL1/GMSL2 Links and Parallel/CSI-2 Video Ports

GMSL2 Overview

GMSL2 is a fixed-rate transmission medium designed to carry multiple types of communication channels concurrently. The link bit rate is based on a constant-frequency link clock generated from the 25MHz crystal oscillator or from an external reference frequency which is only supported with the MAX96712/22. B variants DO NOT support external oscillator. The link clock is not related to the video pixel clock beyond the natural constraint that the video bandwidth cannot exceed the available link bandwidth.

GMSL2 uses a packet-based protocol to seamlessly share the link bandwidth between communication channels in a flexible way. Bandwidth allocation is dynamic so that if a certain channel is not active, it does not consume any link bandwidth, and all the remaining active channels can share the full link bandwidth. Maximum packet size is limited to prevent a single channel from utilizing the link bandwidth for an extended time. In most cases, available link bandwidth exceeds the bandwidth requirement. Idle packets are used to fill in the unused link bandwidth. The same data protocol is used on forward and reverse channels, and for both video and control-channel data.

GMSL2 provides a flexible broadband data link that can transport high bandwidth bidirectional data between remotely located devices. The MAX96712/B is specifically designed to be an interface between multiple remotely located high resolution cameras or similar sensors and a centrally located processor with a particular focus on surround-view sensors. In addition to the core video/broadband streaming portion of the link, GMSL2 devices provide a variety of peripheral/auxiliary functions to enable flexible, robust system implementations.

Received video data is transferred to the SoC using an industry standard CSI-2 interface. Extensive signal routing options enable data from multiple remote sensors to be routed to a single video output port. A flexible video pattern generator providing common video test patterns and PRBS can be used to test downstream video devices to validate functionality of the CSI-2 interface.

GMSL2 supports a comprehensive suite of common embedded communication protocols. All devices utilize a primary I^2C/UART control-channel interface that an ECU uses to access serializer and deserializer registers, as well as peripheral devices. This access can be initiated from either end of the link. The MAX96712/B includes two additional I^2C/UART ports that can be used to access lower priority local register or to communicate with remote serializers and peripherals. Each GMSL link provides a dedicated control channel through which any one of the three I^2C/UART ports can communicate with the serializer or the peripherals connected to that link. Each link supports two additional tunneled pass-through I^2C/UART channels that are available for remote peripheral communication. The connectivity of the I^2C/UART ports can be

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configured independently for each of the GMSL links, enabling different I²C/UART ports to access the control channel and the tunnelled channels of each link.

Two SPI main/subordinate interfaces, each including two subordinate select pins, are included in the MAX96712/B. The SPI interfaces enable a host SPI main on one side of the GMSL2 link to control a peripheral SPI subordinate on the opposite side. The host can be located at either end of the link or can swap ends by reprogramming the GMSL2 devices as either a SPI main or a subordinate. The two SPI ports are fully independent and function exclusively as pass-through ports without access to serializer or deserializer registers.

All GMSL2 devices include a versatile suite of GPIO pins that work with the GMSL2 peripheral communication protocols. In general, the GPIOs function as user-defined inputs or outputs whose states can be either automatically forwarded across the link or controlled by register settings. GPIOs are typically used to tunnel low speed (<100Kbps) signals over the GMSL2 link. A GPIO tunnel can be set up in the forward or reverse direction.

GMSL2 provides extensive data integrity and safety features, including watermark generation/detection, CRC error detection for control and video data, and ECC protection of video memory. Watermark generation and detection verifies that the video image is not frozen. CRC error detection enables identification of errors in the video or control data streams. In the case of control channel CRC errors, automatic re-transmission of the flagged packet maximizes control channel speed and reliability. The internal video memory includes ECC protection to enable detection and correction of internally corrupted pixel data.

GMSL2 devices incorporate numerous link margin optimization and monitoring functions that ensure high link margin and robust functionality. Continuous (1Hz) adaptive equalization optimizes link margin to adapt to environmental changes and cable aging. An eye-opening monitor function provides continuous link margin diagnosis and includes various threshold alarm levels that trigger run-time alerts whenever link degradation is detected. PRBS checking verifies correct link and video channel operation.

Video Pipeline

The video channel transmits high bandwidth video data from a serializer to a deserializer. (Video data only flows in the forward direction.) The MAX96712/B supports a variety of common data types, including RAW8/10/12/14/16/20, RGB565/666/888, and YUV8/10-bit. The video channel offers extensive signal routing flexibility, enabling multiple cameras or other sensors to interface seamlessly with different C/D-PHY CSI output port configurations. It also includes several key safety features required in ASIL compliant systems (available only with GMSL2), and the internal memory associated with the video pipeline is ECC protected to ensure data integrity.

Video Pipes, Aggregation, and Replication

In GMSL2 mode, the transmission of video data is based on the concept of video pipes. Carrying data in pipes allows GMSL2 to bridge different digital video interfaces and perform watermark generation and detection.

A pipe carries a video stream(s) and video synchronization data. Each pipe operates in one of three modes. In all modes, a pipe can carry multiple concurrent video streams, with each stream having different virtual channels and data types.

Mode 1: Streams with constant bits per pixel (bpp) of up to 24bpp. The bpp of the streams must be the same.
Mode 2: Streams with 16, 14, 12, 10 or 8bpp. Streams less than 16bpp are padded with zeros.
Mode 3: Streams with two different bpp. The bpp of one stream must be twice the bpp of the other stream. The higher bpp stream maximum is 24bpp.

Mode 1 and Mode 3 carry data at full bandwidth but put more restrictions on bpp than Mode 2. Mode 2 allows streams with different bpp, but streams of less than 16bpp are carried using more bandwidth than necessary on the GMSL2 link because of zero padding. Mode 1 or Mode 3 are sufficient for most applications. Mode 2 requires less programming and is more convenient if the application does not require maximum link bandwidth.

The MAX96712/B has four GMSL input ports, each accommodating up to four independent pipes in GMSL2 mode. In GMSL1 mode, only a single, dedicated video pipe is available per link. These capabilities are consistent with those of other GMSL2 devices. To accommodate the greater number of GMSL inputs and incoming video streams, the MAX96712/B provides a total of eight internal video pipes that are shared by the four GMSL inputs as shown in Figure 29. Each internal pipe can be mapped to any one of the incoming GMSL video streams, and as a result, up to eight internal pipes can be mapped to a single GMSL2 input port. The combined total number of video pipes utilized by all connected serializers cannot exceed the eight internal pipes provided by the MAX96712/B. In GMSL1 mode, a total of four internal video pipes are available with fixed mapping between each GMSL1 input and a single internal pipe as shown in Figure

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29. In mixed GMSL1/GMSL2 systems, the GMSL1 input streams are routed to the dedicated GMSL1 pipe associated with each active GMSL1 input. Incoming GMSL2 streams can be routed to any of the available pipes not dedicated to an active GMSL1 input. In general, the content of any video pipe can route to any of the CSI output ports. The exception is that only pipes 0 to 3 are available sources for synchronous aggregation.

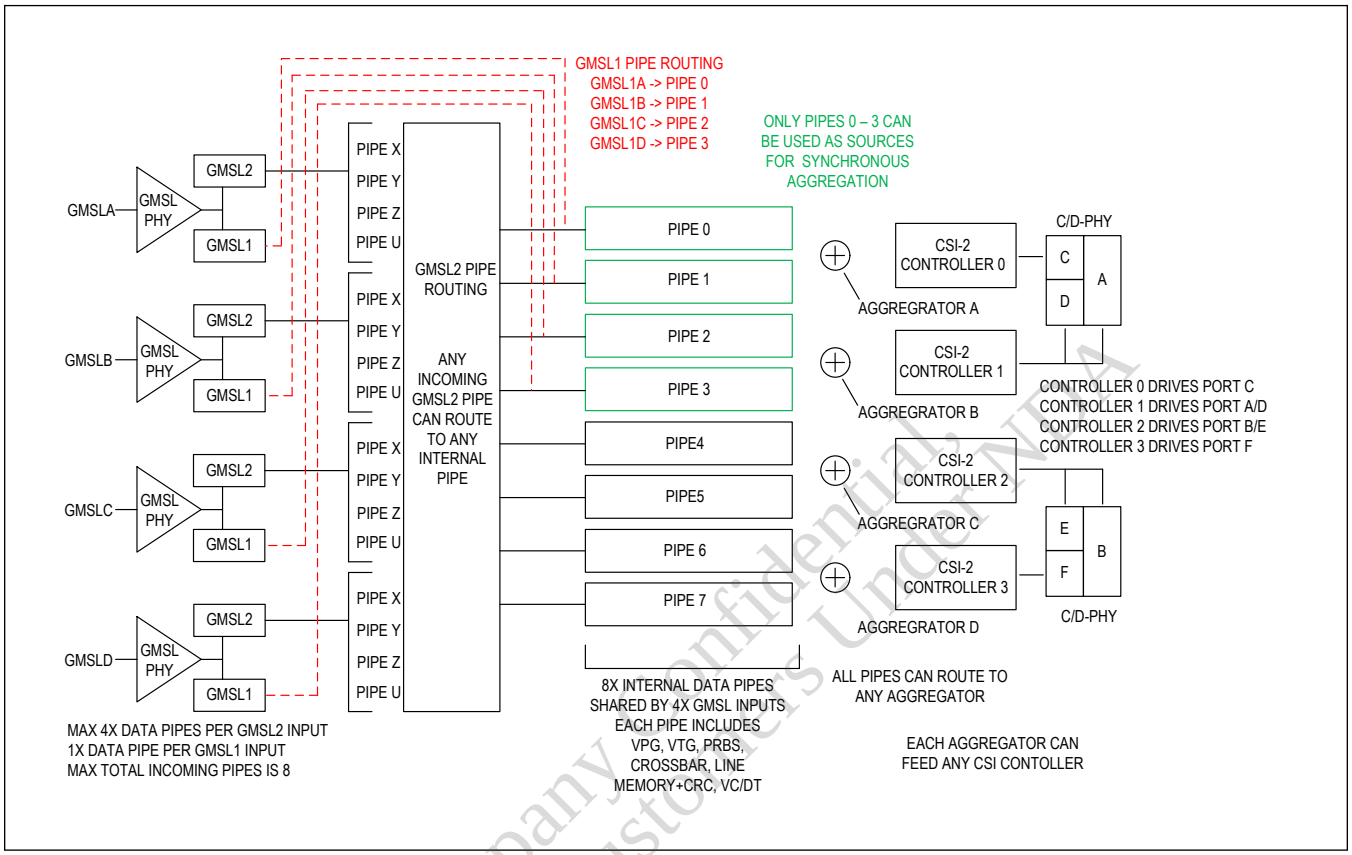

Figure 29. Video Pipes and Routing

In typical applications, a single camera requires either one or two pipes depending on whether it supports high dynamic range (HDR) imaging. For standard cameras using YUV422 formatted video, a single pipe is sufficient to transport all data. For HDR cameras using more complicated data formats, such as RAW16/8-bit embedded data and RAW12, a pair of pipes must be dedicated to carry the resulting video stream. The eight available internal pipes enable the MAX96712/B to dedicate two internal pipes to each of the four cameras in a high definition surroundview system that uses quad HDR cameras. The example shown in Figure 30 illustrates an application in which two links interface to HDR cameras (two dedicated pipes) while the other two links stream video from standard cameras (one dedicated pipe). GMSL1 operation limits each link to a single pipe, which reduces flexibility in handling certain types of sensor streams.

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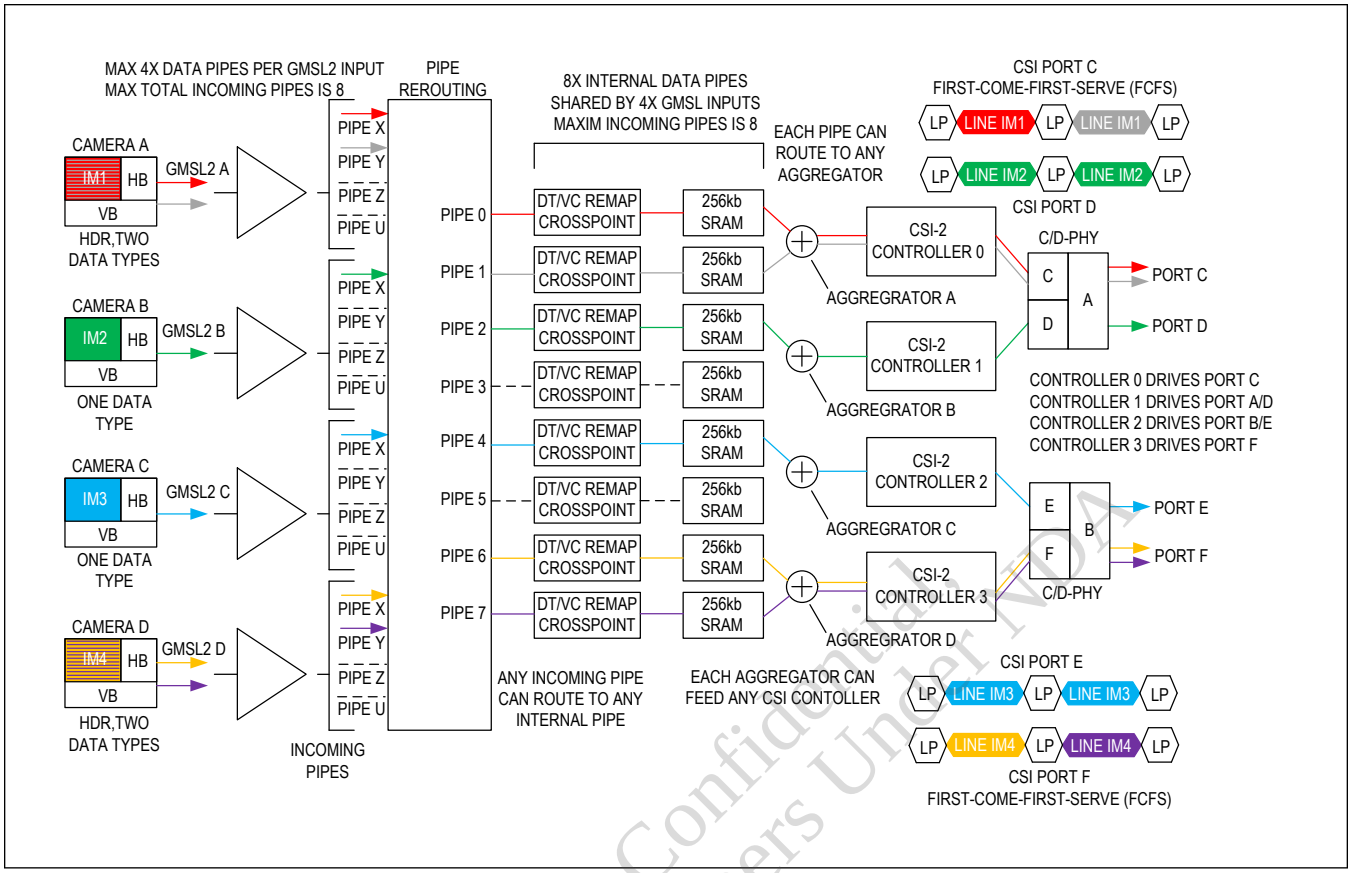

Figure 30. MAX96712/B Video Pipe Example with Partial FCFS Aggregation

When video data is received by one of the MAX96712/B's GMSL inputs, it is immediately forwarded to one of the internal video pipes. Note that a single pipe can carry many separate streams, provided that they comply with certain mode dependent format limitations. The channel ID of each incoming CSI stream can be reassigned if desired, and the order of the bits can optionally be remapped using the RX crosspoint switch. Video data then fills the dedicated line buffer associated with each pipe as controlled by the sync data.

Each line buffer can be routed to any one of the four aggregators, which can be used to combine data from multiple video pipes and/or virtual channels within a single CSI-2 stream. Only one aggregator can read data out of a given buffer. Once data is read, it cannot be read a second time by another aggregator. Up to eight pipes can be aggregated by one aggregator. Video data can be routed according to DT or VC based on the source CSI-2 packet's DT/VC, or it can be routed by a DT/VC assigned in the MAX96712/B. For example, data in pipe 0 with VC0 can be programmed to be read out by Aggregator A, while data in pipe 0 with VC1 can be programmed to be read out by Aggregator B. This maximizes data routing flexibility and enables multiple streams within a single pipe to be routed to separate CSI output ports.

Aggregated data is typically read out from line memory on a first come, first served (FCFS) basis as shown in Figure 30 and Figure 33. In this case, data from all eight video pipes is visible to the aggregators. The order in which the line memories reach filled status is the order in which they are read out. When a complete line of video data has filled the line memory, it is routed as specified by the aggregator to one of the CSI controllers for packet generation. In this case, the outgoing CSI data streams can be viewed as independent parallel streams that may have independent timing, although they may be effectively synchronized depending on the nature of the video sources used.

Alternatively, data can be aggregated in specific sequences corresponding to side-by-side (4WxH) or line-interleaved (Wx4H) output formats (see Figure 31). All data sources must use the same resolution and virtual channel assignment and must be precisely synchronized. The resulting output is a single stream consisting of a superframe that holds video data from all aggregated streams. The aggregators only have access to the content of video pipes 0 - 3, so any video

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content requiring synchronous aggregation must be routed using these pipes. Synchronous aggregation can effectively provide a single combined image output from multiple sensors, such as a single image surround view stream.

Side-by-side aggregation combines incoming streams from up to four sensors, resulting in a frame that has equal height and up to four times the width of a single sensor output. With side-by-side aggregation, the 4W horizontal resolution must not exceed the available video line memory depth. Line-interleaved aggregation alternates, in order, every line among as many as four sources, effectively creating an image that has equivalent width and up to four times the height of a single sensor output. In either case, the data rate corresponding to the aggregated video is equal to the data rate of a single sensor output multiplied by the number of combined streams. Figure 32 provides examples of video pipe configuration and data flow in line-interleaved and side-by-side synchronous aggregation modes.

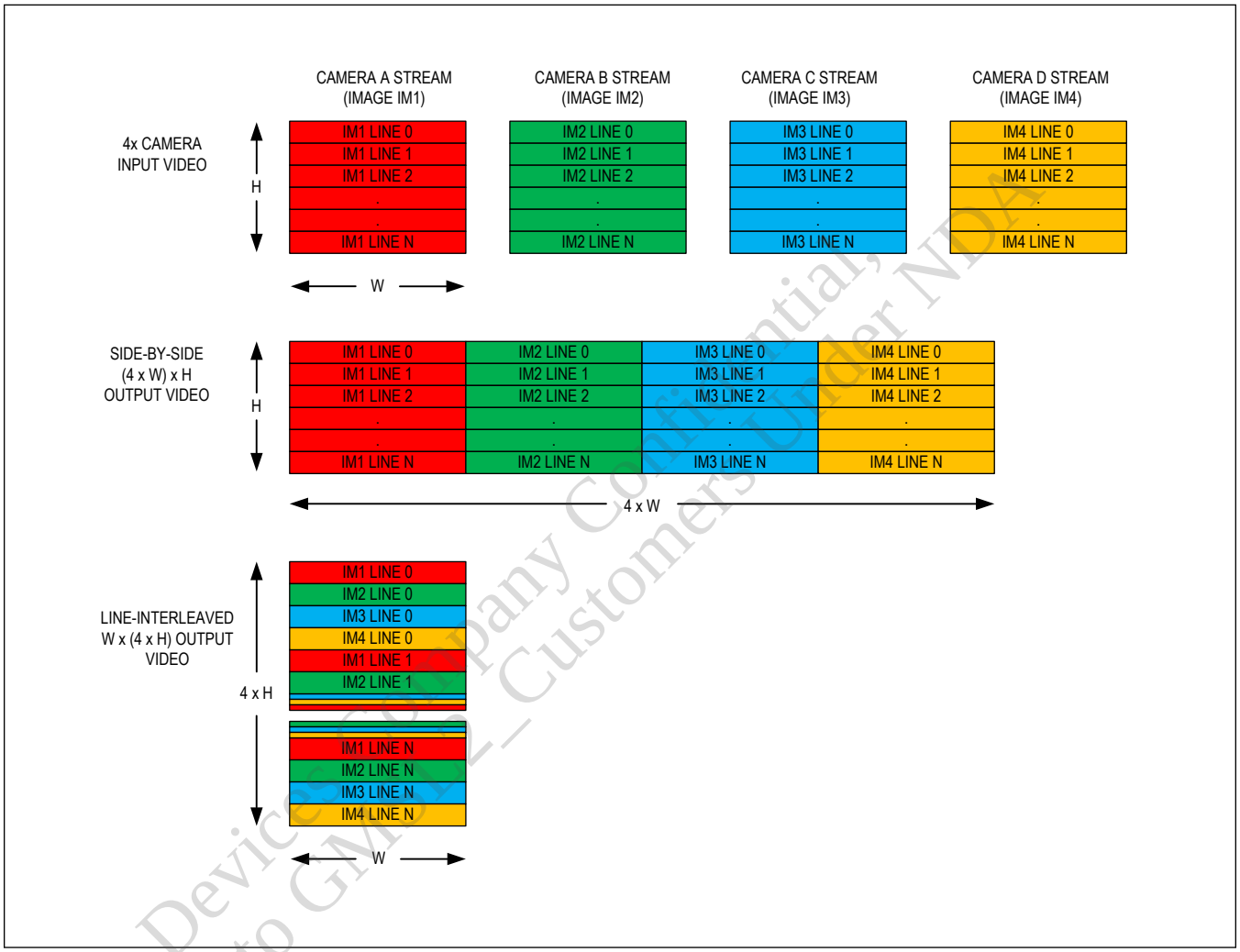

Figure 31. Side-by-Side and Line-Interleaved Synchronous Aggregation Frame Formats

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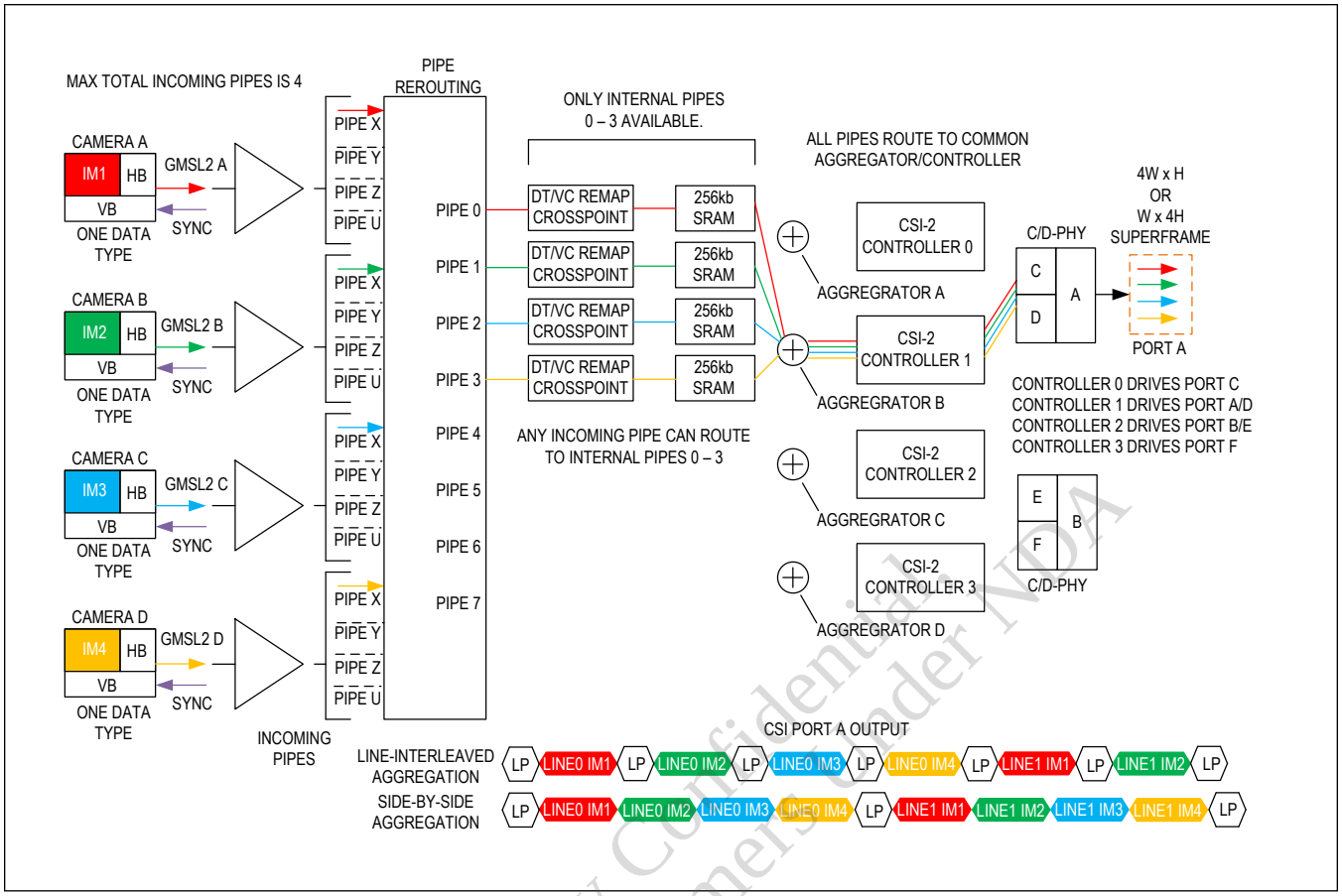

Figure 32. MAX96712/B Video Pipe Example with Synchronous Aggregation

Regardless of the type of aggregation used, the output of each CSI controller can drive one or more CSI ports depending on whether replication is used and how the CSI ports are configured. For example, CSI controller 1 can output packets on:

- PHY/D-PHY Port A and/or
- C-PHY/D-PHY Port B and/or
- C-PHY/D-PHY Ports C/D/E/F depending on the configuration

The MAX96712/B includes features that minimize the disruption resulting from one of the links failing in multilink systems that use aggregation. With systems using synchronous aggregation, the MAX96712/B masks the failed link's video data with 0s. This allows overall timing to continue as expected, enabling the remaining video streams to proceed uninterrupted. Similarly, with systems using FCFS aggregation, the video stream associated with a link that has failed is terminated at the end of a line to avoid a sudden disruption that may impact other streams using the same physical interface.

Figure 33 illustrates an example in which CSI controller 1 combines data from all four GMSL inputs with FCFS aggregation and then replicates the resulting output to CSI ports A and B. Note that a given PHY port can only accept packets from one controller. Data cannot be aggregated at the input of a PHY. All aggregation must be realized in the prior aggregation blocks. The CSI-2 port data rate needs to be programmed equal to or greater than the incoming data rate to prevent buffer overflow. Programming the output rate to be faster than the bandwidth of the incoming video increases packet spacing (LP time between packets).

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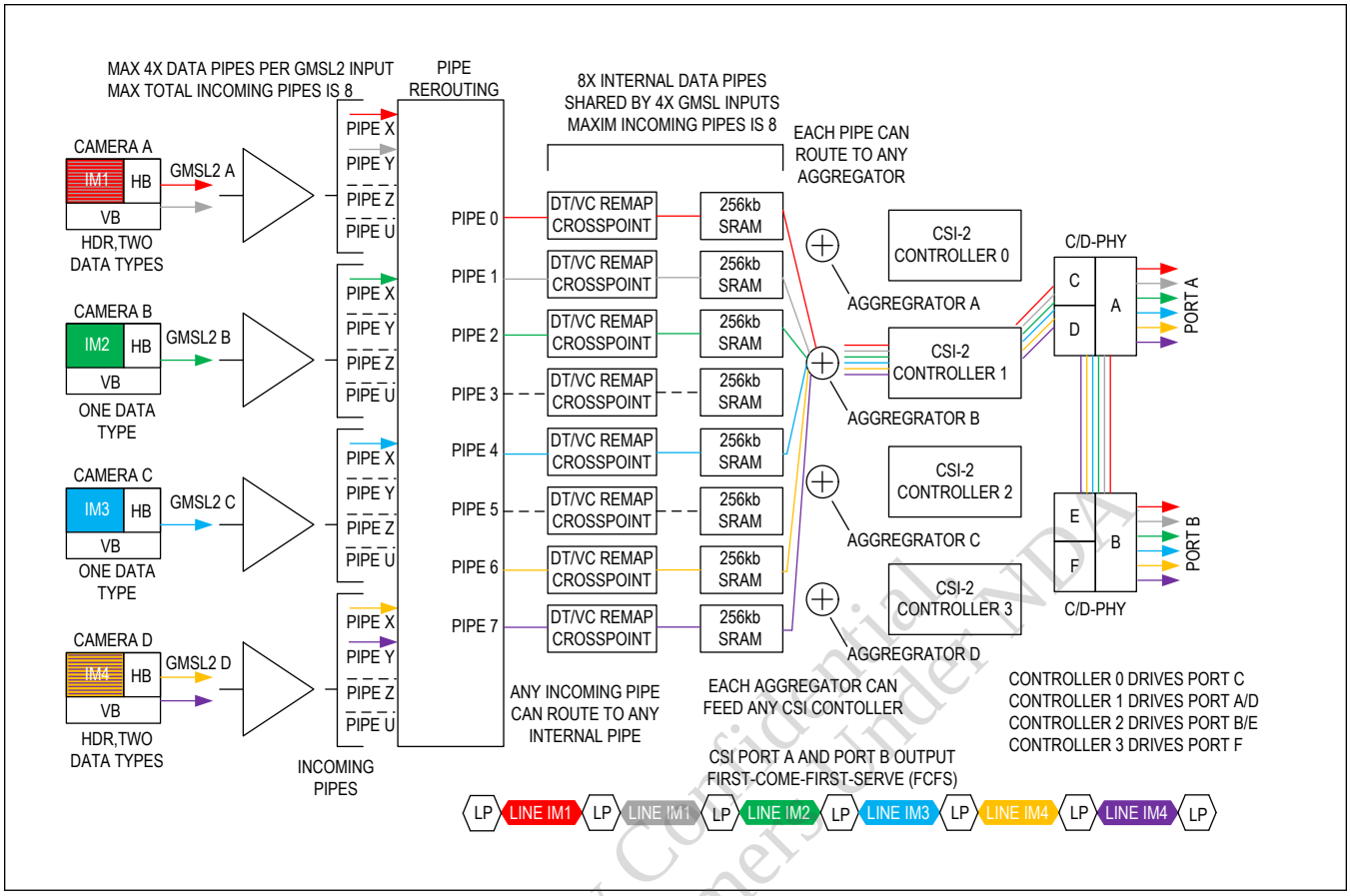

Figure 33. MAX96712/B Video Pipe Example with FCFS Aggregation and Replication

Video Crossbar

The incoming video stream or VPG output passes through a crossbar switch that enables arbitrary remapping of all bits in the video stream. A single bit can be remapped to multiple locations in the serial stream if desired. The default routing of the crossbar is such that no remapping occurs (crossbar function is completely transparent by default).

Watermarking

The watermarking block allows users to detect a frozen frame failure between the generator and the detector in a frame-based processing system. This feature specifically targets frozen frames caused by errors in safety-critical applications. It does not detect frozen frames that occur before the watermark generator or after the watermark detector. The MAX96712/B contains two watermark generators/detectors. This enables it to insert or detect a watermark concurrently on two safety critical video streams. The watermark generator inserts a time-varying watermark that is highly redundant and robust with respect to image processing and display stream compression. The watermark detector looks for this time-varying watermark. A failure to detect any of the generated watermarks indicates that a frozen frame failure has occurred between the generator and detector. In this error condition the watermark detector can generate an interrupt and/or blank the output video, returning the display to a safe-state in less than 500ms.

Video Line CRC

The MAX96712/B includes a GMSL video CRC error checker, which can be used in safety critical applications to guarantee the integrity of the video stream. The error checker utilizes a CRC32 polynomial function to generate a 32-bit CRC code for each received line of video data. This same CRC code is also generated on the serializer side of the link, and this code is transferred over the link to the MAX96712/B along with the corresponding video data. The MAX96712/B

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then compares the CRC received from the serializer with the CRC it has generated for a given line of video data. Any discrepancy in the CRC codes indicates an error in the video data.

Video Timing Monitor

The MAX96712/B provides optional monitoring of the video sync signals HS, VS, and DE, which are not readily available via the CSI-2 outputs. The sync signals can be derived from the content of any of the eight video pipes. In both GMSL2 and GMSL1 modes, the sync signals can be driven to MFP pins (VS=MFP4, HS=MFP13, DE=MFP14) for monitoring. In addition, the sync monitor HS, VS, and DE signals can be observed using the VID_HVD_DET registers.

Video Memory ECC Protection

The integrity of data propagating through the video pipeline's memory is guaranteed by ECC, which enables correction of 1-bit errors and detection of 1- or 2-bit errors per 32 bits of video data. This functionality provides protection of data that is not protected by the CRCs of the incoming GMSL stream or the outgoing CSI stream, eliminating the possibility that internally generated silent bit errors might corrupt the outgoing CSI-2 stream. The state of the ERRB pin can be used to detect the presence of errors. Intentional memory error injection is available for diagnostic purposes.

Control Channel and Side Channels

A µC or other controller can send and receive control and side-channel data over the GMSL2 serial link simultaneously with high-speed video data. The MAX96712/B supports the following interfaces:

1. 3x I^{2}C/UART
2. 2x SPI
3. 17x GPIO

Data from all interfaces tunnels through the GMSL2 link, but only one of the I^{2}C/UART interfaces can access remote serializer registers at a given time over any one of the links. All I^{2}C/UART ports offer concurrent access to local registers via arbitration. The default state of all I^{2}C/UART ports is specified by the power-up state of the I2CSEL/MFP13 pin. See *I^{2}C/UART* for further information.

Control and side-channel peripheral interfaces are accessed via multifunction GPIO pins (MFP pins). Multifunction pins have a default function and can be programmed to a variety of alternate functions after power-up. Due to a practical limit on the number of pins available on a given device, not all interfaces can be simultaneously supported. See the *Multifunction Pin Configuration* section and the *Pin Descriptions* for default and alternate multifunction pin functions as well as available combinations of interfaces.

I^{2}C/UART

The MAX96712/B includes three independent I^{2}C/UART interfaces. These interfaces are the only means by which local or remote (serializer) registers can be accessed. The operating mode of all three ports is set at power-up via the I2CSEL/MFP13 pin. Following power-up, the mode of each port can be independently changed by register programming. The main µC is typically located on the MAX96712/B side of the link, although this is not strictly required, and communication can be initiated by a device on either side of the link. For correct operation, the control channel of each of the MAX96712/B's links must be configured in the same mode as the serializer connected to that link (both I^{2}C or both UART; each link's control channel can use a different control channel port/mode with the constraint that each MAX96712/B UART port can only be routed to one link). Unlike GMSL1 devices, there is no I^{2}C-to-UART conversion capability. I^{2}C/UART outputs are open drain and require appropriately-sized external pullup resistors for proper operation.

Each of the three I^{2}C/UART ports can be used to access internal MAX96712/B registers, remote serializer registers, and remote peripheral registers. All three ports provide concurrent local register access. Each GMSL2 link provides a dedicated control channel through which any one of the ports can communicate with either a remote serializer connected to that link or with any remote peripherals connected to the serializer's control channel port. Each link's control channel can be independently assigned to any one of the three I^{2}C/UART ports. Each link includes an additional pair of tunneled pass-though channels for remote peripheral communication. For any given link, the tunneled pass-through channels can be assigned to the two I^{2}C/UART ports that are not routed to the control channel. Routing of the I^{2}C/UART ports to each link's control channel and tunneled channels is independent, enabling different combinations of local ports to access the control channel and the tunneled channels of each GMSL link.

All three ports provide simultaneous local access with lower indexed ports having the highest priority. In I^{2}C mode, a

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local port's local register access cannot be disconnected unless the port is disabled. Therefore, all active I²C ports have local register access at all times. For a port operating in UART mode, local register access can be disabled by forcing the port into bypass mode.

Remote serializer registers are visible only by means of the dedicated GMSL2 link control channel, which supports only a single port. Therefore, only one port at a time can access remote registers over a given link. By default, port 0 is routed to the control channel of each link. With appropriate configuration, port 1 or port 2 can also be routed to the control channel to support remote serializer register access. The two ports not routed to the control channel can be tunneled to the remote side of the link and used for peripheral communication by using the GMSL2 serializer's pass-through functions. Links operated in GMSL1 mode do not support the GMSL2 serializer pass-through tunnels. As a result, any links operated in GMSL1 mode provide only a single control channel with both serializer and peripheral register access. Note that a remote pass-through interface still provides local register access unless the port is configured as a UART in bypass mode. Therefore, the MAX96712/B's I²C device address is always present on every active I²C port. Figure 34 details the routing of the three I²C/UART ports.

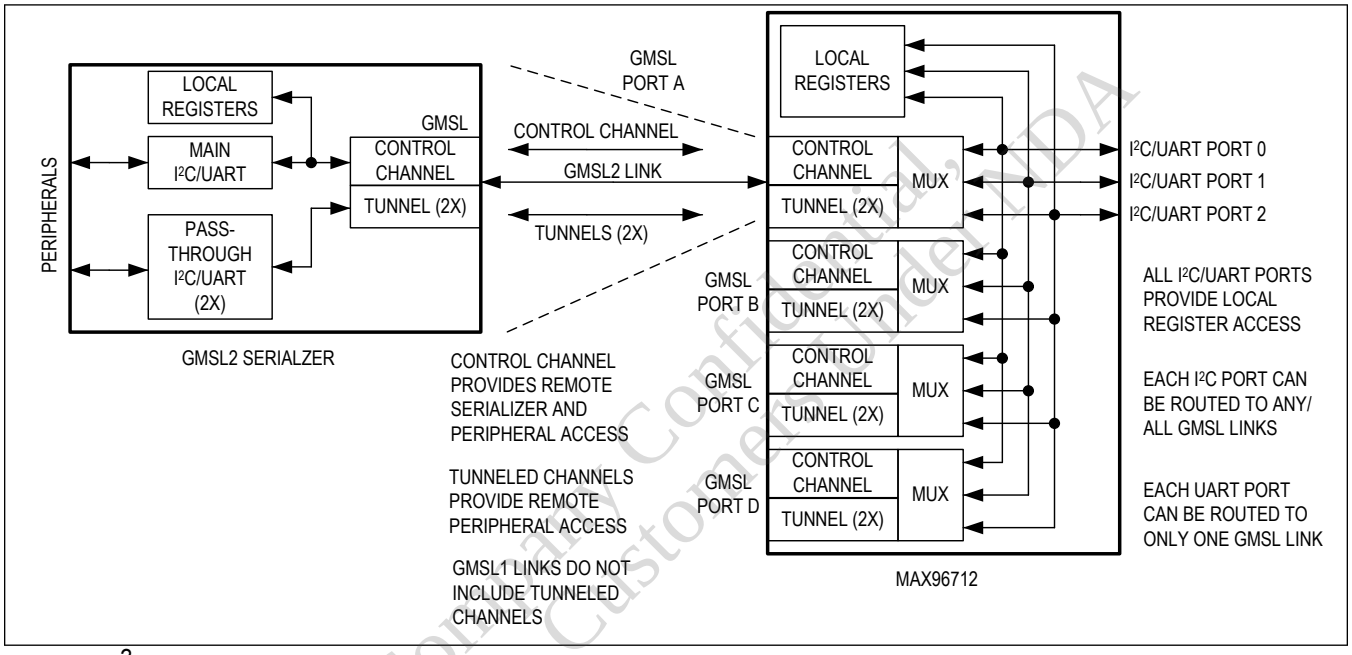

Figure 34. I²C/UART Control Routing

Each port's connectivity can be independently programmed for each of the four GMSL links. This enables different ports to access each link's control channel and tunneled channels. In addition, the tunneled channels can be enabled or disabled separately in each of the links, providing extensive flexibility in routing data from specific MAX96712/B ports to particular remote devices. This is especially useful in UART applications, which lack I²C's intrinsic multidevice support and are frequently limited to point-to-point communication between two devices. Ports operated in I²C mode can simultaneously communicate over any number of available GMSL links, while ports operated in UART mode can only communicate over one link at a time.

In UART mode, the MAX96712/B can either be configured to operate in base mode or bypass mode. In base mode, the host uses a special protocol that identifies the target device and register. Using this protocol, all UART ports provide concurrent local register access, and the UART port connected to a link's control channel can access remote serializer registers and protocol compliant remote peripheral registers associated with the link. In bypass mode, the serializer and deserializer ignore all control channel traffic, and the UART ports simply forward traffic across the link, effectively operating as pass-throughs. GMSL device register access is not possible in this case.

Each UART's mode is controlled by either the programmable shared local MS MFP function, a dedicated remote MS MFP function, or dedicated local control bits. When internal local registers are used to control the UART mode, each UART

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can be independently placed in either temporary or permanent bypass mode. In temporary bypass mode, the UART port maintains bypass mode as long as traffic is present on the port. After a user-defined period of idle activity, the bypass mode times out and the port returns to base mode. In permanent bypass mode, the timeout is disabled and the port remains in bypass mode until a reset returns it to base mode. When a port is in permanent bypass mode, subsequent GMSL device register access through the port is blocked until after a reset.

If either local or remote MS MFP functions control an external UART's mode, the UART mode responds immediately to the specified MS MFP state. When a remote MS MFP function sets the UART mode, the MS pin controls only the mode of the UART connected to the remote device through the dedicated GMSL control channel. Thus, it is possible that MS MFP functions in different remote devices can be used to control the modes of different MAX96712/B UART ports. A UART routed to a remote device as a remote pass-through does not change mode in response to the remote MS MFP function.

Any of the three UART ports can provide local access in addition to being connected to one of the GMSL link control channels. Thus, more than one port can operate as a control channel port that requires mode control. Depending on how UART mode control is realized, this could result in multiple ports relying on local MS MFP mode control. To meet this requirement, the shared local MS MFP function can be routed to all UART ports simultaneously.

When the user wishes to control only one UART's mode at a given time, great care must be taken in managing the routing of the local MS MFP. Otherwise, the modes of other UART ports could be inadvertently changed when not intended.

For details regarding operation of the I^{2}C/UART interfaces, see *Control Channel Programming*.

SPI

The MAX96712/B includes two independent SPI ports. SPI functionality is available only in links that use GMSL2 mode. These ports enable a host SPI main on one side of the GMSL2 link to control a peripheral SPI subordinate on the opposite side. Communication can be in either direction across the GMSL2 link. Each SPI port can communicate across one GMSL2 link at a time. The SPI clock range is 600kHz to 50MHz. Care must be taken to meet setup and hold time requirements when operating the interface at speeds higher than 20MHz. Table 14 includes recommended settings for the SPI interfaces for optimal performance at different clock speeds.

Although multiple SPI peripherals may be connected, it is recommended that only one be communicated with at a time. Contact the factory for guidance on configuring SPI connections.

Control Channel Latency

All control channels exhibit finite latency. Typical latency for each function is given in Table 5. For I^{2}C, which requires an immediate ACK from the receiver following each byte, clock stretching is used to temporarily pause communication as the ACK propagates through the control channel. All I^{2}C devices that communicate over the link must support clock stretching.

Table 5. Control Channel Latency

FUNCTION	FORWARD	REVERSE	NOTES
I^{2}C	< 10µs	< 10µs	
UART	< 10µs	< 10µs	
SPI	< 10µs	< 10µs	Round Trip

General Purpose Inputs and Outputs (GPIO)

GPIO are typically used to tunnel low speed (<100Kbps) signals over the GMSL2 link. A GPIO tunnel can be set up in the forward (serializer to deserializer) or reverse (deserializer to serializer) direction. GPIO transmissions are transition based. A GPIO packet is created and transmitted on the GMSL2 link when a rising or falling edge transition occurs at a GPI pin. The transition is regenerated at the corresponding GPO on the other end of the link.

Multifunction pins can be programmed as GPI (input), GPO (push-pull output or open-drain output, although some MFP pins only support open drain output) or GPIO (bidirectional input/output). Most GPIOs can also be programmed for 1MΩ or 40kΩ pullup or pulldown (or none). Although an internal pullup is provided, high-speed open-drain outputs require an appropriate value external pullup resistor to V_{DDIO}. Inputs cannot be left floating. Always ensure that every pin configured as an input has a pullup or pulldown programmed or is driven by another IC or external pullup/pulldown.

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A GPI on one side of the serial link can be mapped to either a single GPO or to multiple GPOs on the other side of the link. Each GPI is assigned a pin ID, with the destination GPO(s) on the other side of the link set to the same pin ID. By default, the ID mapping is GPIO0-GPIO0, GPIO1-GPIO1, GPIO2-GPIO2, etc. However, the GPIO mapping can be arbitrarily changed by register settings.

GPI transitions can be transmitted in two modes: delay-compensated and non-delay-compensated. When delay compensation is enabled, the GPI-to-GPO delay across the link is a precise, fixed value. Latency increases but jitter and skew decrease. The delay compensated mode's low skew is especially valuable when remotely located sensors must be precisely synchronized.

The state of each GPIO can be read or written by register either locally, using any of the three I^2C/UART ports, or remotely via the I^2C/UART interface that is routed to the GMSL2 control channel.

In non-delay-compensated mode, channel latency is not fixed. The GPI transition is sent as soon as possible based on priority and available link bandwidth. This variable delay is the result of multiple communication channels sharing the link. Non-delay-compensated mode can be used with signals tolerant to delay variation to minimize latency (i.e., µC interrupts).

GPI transitions are transmitted in the order they occur.

Typical GMSL2-only device delays for 6Gbps forward and 187Mbps reverse link rates are shown in Table 6.

Table 6. Typical GPIO Delays for Forward and Reverse Link Transmission

GPIO CHANNEL	DELAY COMPENSATION	DELAY
GPIO forwarding from serializer to deserializer (6Gbps forward channel)	0	720ns
	1	3.5µs
GPIO forwarding from deserializer to serializer (187Mbps reverse channel)	0	6µs
	1	15µs

GMSL2 Physical Layer

Maxim's GMSL2 family of serial links have transmitter and receiver capability enabled simultaneously, allowing full duplex operation on a single wire. A single cable between the serializer and deserializer delivers data being transmitted from each end of the link. Forward transmission is data being sent from the serializer to the deserializer. Reverse transmission is data being sent from the deserializer to the serializer.

Forward rate options are fixed at 3Gbps or 6Gbps, with defaults of 6Gbps in coax mode and 3Gbps in STP mode. Reverse data rate is fixed at 187.5Mbps.

Each of the MAX96712/B's four GMSL inputs can be independently configured for different link rates or GMSL2/GMSL1 operation.

Cabling Options

The MAX96712/B supports either 50Ω coax or 100Ω shielded-twisted pair (STP) cabling. Cable attenuation and return loss characteristics must stay within the requirements of the channel specification to achieve robust full-duplex link performance. These requirements vary with selected link rate. The available link rates and adaptive equalization enable support of a wide range of cabling options. Coax or STP mode and data rates are configured upon startup and determine which cabling option applies. In coax mode, use only the noninverted SIO pin. AC-couple and terminate the inverting SIO pin using the series connection of a 100nF capacitor and a 49.9Ω resistor. In STP configuration, both the noninverted and inverted SIO pins are enabled by default. Maximum cable length is limited by the frequency-dependent attenuation of the cable. Additionally, PCB and in-line connectors degrade the return loss characteristic of the cable assembly. The channel specification allows two inline connectors and provides detailed requirements for cable attenuation and return loss, as well as insertion loss and return loss requirements for PCB traces. In general, any physical channel implementation that is compliant with the channel specification can be used with reliable results. Contact the factory to receive the channel specification document.

GMSL2 Bandwidth Sharing

The GMSL forward bandwidth is shared between video, the I^2C/UART control channel, pass-through I^2C/UARTs, SPI, GPIOs, and various protocol specific data exchanges (i.e. info frames, sync, and acknowledgements). The reverse

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channel bandwidth is also shared with all of the above, with the exception of video packets, which cannot be transmitted over the reverse link.

The total link bandwidth used by all communication channels cannot exceed the fixed available link bandwidth.

GMSL2 offers considerable flexibility in how link bandwidth is shared between the various communication channels requesting the link for packet transmissions. This flexibility comes from packet-based transmission format and dynamic bandwidth allocation; if a certain channel is not active, it does not consume any link bandwidth, leaving the full link bandwidth available for all active communication channels to share. The packet-based protocol fulfills this sharing requirement. The maximum packet size is limited to prevent one single channel from monopolizing the link bandwidth and to ensure other channels are served.

The video and control channel packets can be assigned a priority level. There are four priority levels: low, normal, high, and urgent. The scheduler transmits the packet with the highest priority among the pending requests. Packets with stringent latency requirements can be assigned an increased priority.

GMSL2 Bandwidth Calculations

The GMSL2 forward link has a fixed link rate of 3Gbps or 6Gbps. The reverse link rate is fixed at 187.5Mbps. The GMSL2 protocol overhead is roughly 14%. This leaves approximately 2.6Gbps or 5.2Gbps of data throughput in the forward direction and 162Mbps in the reverse direction.

Worst-case applications must not exceed the available throughput of the forward and reverse links. Maxim's evaluation kit (EV kit) GUI includes a bandwidth (BW) calculator that estimates initial bandwidth requirements. Maxim offers other tools that are also useful for calculating link bandwidth utilization. Consult the factory for high-bandwidth use cases to ensure error free performance.

Table 7 provides rough estimates of the bandwidth utilization for each of the communication channels. Note that the video channel is available only in the forward link direction, and therefore bandwidth cannot be allocated to video in the reverse link. Bandwidth can be allocated to all other functions in both the forward and reverse directions.

Table 7. Forward and Reverse Link Bandwidth Utilization

DATA	APPROXIMATE BANDWIDTH UTILIZATION
Video	H x V x fps x bpp x (1+% blanking/100) x 1.14
I^2C	18 to 60 x I^2C clock rate, depending on available link bandwidth
UART	6 x UART bit rate, 5.5 x when parity bit enabled
SPI	2.5 x SPI rate
GPIO	60 x GPIO transition rate without delay compensation 80 x GPIO transition rate with delay compensation enabled

Definitions:

H = horizontal resolution

V = vertical resolution

fps = frames per second

bpp = bits per pixel

GMSL2 Minimum Blanking

The minimum horizontal blanking period needed by the CSI-2 serializers and deserializers is the maximum of either 40 pixels or 300ns + 370UI (where UI is defined as the period of CSI-2 lane rate). For most cases, 40 pixels is the larger number. The minimum vertical blanking period is one video line. The minimum vertical front porch is one video line. Recommended vertical back porch is one video line.

Minimum vertical back porch in Pixel mode is the maximum of:

- 40 pixels
- 300ns+ 370UI

Minimum vertical back porch in Tunneling mode is the maximum of:

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- 40 pixels
- 200 PCLK periods + 233ns, where PCLK = total MIPI data rate/24
- 300ns + 370UI

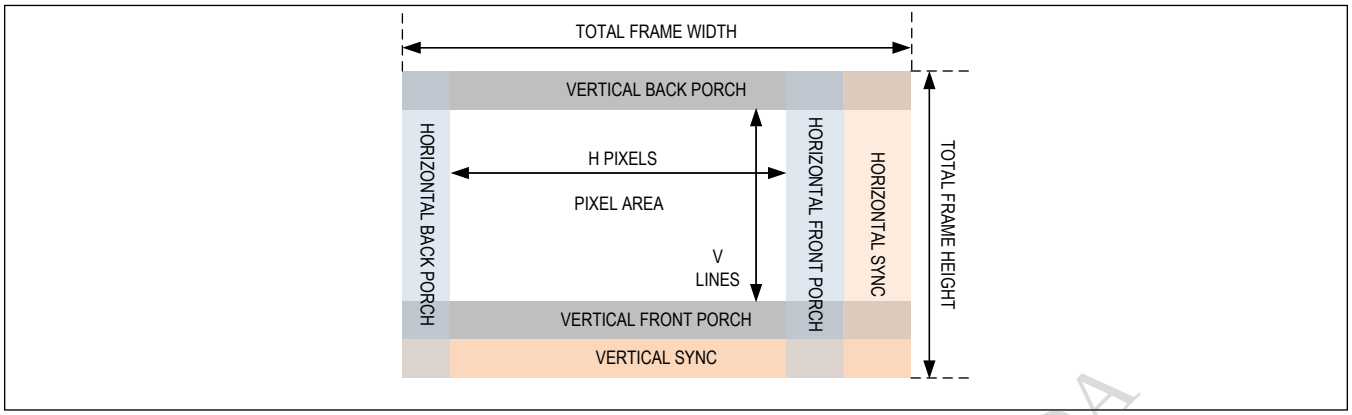

Figure 35. Video Timing

Eye Opening Monitor

The eye-opening monitor (EOM) enables GMSL2 parts to monitor the link margin on an active link and generate an interrupt if it falls below an acceptable level. For example, if a cable is damaged, the link can run error free but have less link margin than desired. The EOM allows the user to proactively react to deteriorating cable performance before any link errors occur. GMSL2 parts measure either the horizontal or the vertical eye opening of the equalizer's output. The measurement is activated automatically at a ~1Hz rate once a link is active. The EOM block compares the data sampled at the center of the eye with a sample offset in phase for the horizontal EOM or offset in voltage for the vertical EOM. The eye opening is then reported, and the EOM triggers an interrupt or reset if the opening falls below user-defined thresholds.

Video PRBS Generator/Checker

GMSL2 devices include built-in video PRBS generators/checkers for video link testing. For example, a serializer's PRBS generator can be used in conjunction with a deserializer's PRBS checker for testing the GMSL2 video channel that connects the two devices. In this case, the MAX96712/B's PRBS checker functionality compares the received PRBS stream with the predicted PRBS data to establish whether any errors are present.

The MAX96712/B also includes video PRBS generator functionality that enables the testing of downstream video devices that receive video via the MAX96712/B's CSI-2 output. This includes GMSL2 serializers that are connected in a loopback configuration with CSI and GMSL video paths being tested at the same time.

Note that all link bandwidth is not used by the video channel alone in GMSL2 mode, so it is possible to have a bit error on the link that does not cause a video PRBS error. Additional discussion of this functionality can be found in the *CSI Video Output Ports* section.

Link Error Generator

Each of the GMSL links includes a configurable error generator that injects errors into the outgoing data stream immediately prior to transmission. The deserializer injects errors into the reverse channel, and the serializer injects errors into the forward channel. The receiving device detects, counts, and flags the errors, enabling a thorough validation of the system's response to error conditions of varying severity.

AEQ (Adaptive Equalization)

The GMSL2 devices automatically adapt receiver characteristics to compensate for the insertion and return loss characteristics of the channel, which consists of the cables, connectors, and PCBs. This approach optimizes performance on any channel that meets the GMSL2 channel specification. The equalizer architecture helps guard GMSL2 links against the affects of noise, crosstalk, and reflections. Initial adaptation is performed during link lock. After the link is established,

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the AEQ continues running in the background, updating settings at a rate of ~1Hz to track temperature and voltage variations. The adaptation process optimizes the equalizer coefficients to maximize the eye opening by using the built in eye-opening monitor.

RoR (Reference over Reverse)

Reference Clock over Reverse channel (RoR) is a GMSL clock operating mode where the serializer receives its reference clock from the deserializer over the GMSL link. RoR eliminates the need for a crystal oscillator on the serializer side of the link.

In RoR mode, the serializer's timing reference is extracted from the signal sent on the reverse channel. The recovered clock coming from the deserializer is used by the serializer on-chip phase-locked loop (PLL) to synthesize the serializer output reference clock RCLKOUT.

RoR mode is enabled by default on the MAX96712/B. No register writes are required if desired register can be set to set to disable RoR mode.

The removal of the crystal oscillator in RoR provides several advantages:

- Reduced system cost
- Increased reliability
- Reduced board area
- Simplified board layout

MAX96712/B requires two registers to be written per PHY that is using RoR functionality.

SIOA = 0x148C = 0x20, 0x1498 = 0xC0

SIOB = 0x158C = 0x20, 0x1598 = 0xC0

SIOC = 0x168C = 0x20, 0x1698 = 0xC0

SIOD = 0x178C = 0x20, 0x1798 = 0xC0

GMSL1 Backwards Compatibility

The MAX96712/B is designed to pair with any GMSL1 serializer. However, the device does not support the entire range of features available across all GMSL1 serializers. GMSL1 backwards compatibility is only supported with forward link rates from 500Mbps to 3.12Gbps and a reverse link rate of 1Mbps. When paired with a GMSL2 serializer for GMSL1 operation, both devices must be configured to use GMSL1 compatibility mode. When the MAX96712/B is paired with a legacy GMSL1 only serializer, it must be configured for GMSL1 compatibility mode. The available forward link rate is then reduced to the rate limitations of the specified GMSL1 serializer.

Table 8 specifies the availability of common GMSL1/GMSL2 features in GMSL2 devices that are operated in GMSL1 mode. Note that some GMSL2 features, such as SPI, are only available in GMSL2 mode. As a result, they are never available in GMSL1 mode, regardless of the devices used. If a feature is not supported by both devices in a link, then it should be disabled. To utilize a feature, it must be enabled and configured consistently so that appropriate settings are applied to both ends of the link.

Most features specified in Table 8 can be enabled or disabled by appropriate register configurations and by the state of the CFG0 and CFG1 input pins at power-up. Hardware design of both serializer and deserializer subsystems must account for correct connection of configuration pins to achieve the desired settings. Interfacing coax interconnects to non-coax capable GMSL1 devices requires special hardware considerations to ensure reliable functionality. Contact the factory for additional information regarding general GMSL1 operation or GMSL1/GMSL2 device interoperability.

Table 8. Feature Availability in GMSL1 Mode

FEATURE NAME	GMSL2 SERIALIZER IN GMSL1 MODE	GMSL2 DESERIALIZER IN GMSL1 MODE
Coax	Yes	Yes
Bus Width Select (BWS)	Yes	Yes
High-Bandwidth Mode (HIBW)	Yes	Yes

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Table 8. Feature Availability in GMSL1 Mode (continued)

FEATURE NAME	GMSL2 SERIALIZER IN GMSL1 MODE	GMSL2 DESERIALIZER IN GMSL1 MODE
Data Rate Select (DRS) (Low-Speed Mode)	Yes	Yes
DBL (Double Mode)	Yes	Yes
HSYNC/VSYNC Encoding	Yes	Yes
Pixel CRC (6 bits per pixel)	Yes	Yes
Video Line CRC (32 bits per line)	Yes	Yes
Hamming Error Correction	No	No
I^2C to I^2C	Yes	Yes
UART to UART	Yes	Yes
UART to I^2C	No	No
Pass-Through I^2C Channels	No	No
I^2C Address Translation	Yes	Yes
SPI Control Channel	No	No
High-Immunity Mode	Yes	Yes
REV_FAST with HIBW Mode	Yes	Yes
Packet Control Channel with CRC	Yes	Yes
Packet CC Retransmission	Yes	Yes
Configuration Link	Yes	Yes
GPI to GPO on Reverse Channel	Yes	Yes
Frame Sync	Yes	Yes
Delay Compensated GPI/GPO	No	No
UART Base Mode	Yes	Yes
UART Bypass Mode	Yes	Yes
Spread Spectrum	Yes	Yes
Pre/De-emphasis	No	N/A
Legacy Programmable Equalization	N/A	No
GMSL1 Adaptive Equalization	N/A	Yes
Twisted-Pair Splitter Mode	No	N/A
Watermark	Yes	Yes
Video Timing Generator	Yes	No
Video Crossbar	Yes	Yes
PRBS	Yes	Yes
CNTL0,1,2,3 on Forward Channel	Yes	Yes
A/V Status Register Interrupt	No	No
HS/VS/DE Inversion	Yes	Yes
WS/SCK Inversion	Yes	N/A
Jitter-Filtering PLL	No	No
Sleep Mode	Yes	Yes
Line-Fault	Yes	Yes

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CSI Video Output Ports

The MAX96712/B includes a flexible CSI-2 compliant video output supporting both the D-PHY v1.2 and C-PHY v1.0 standards. The output includes a total of eight data lanes and four independent CSI-2 controllers. These can be configured as four 2-lane ports, which can be combined to alternatively provide two 4-lane ports or a combination of one 4-lane and two 2-lane ports. Each 4-lane port can consist of one, two, three, or four data lanes, while each 2-lane port includes either one or two active data lanes. Each D-PHY lane supports HS data rates from 80Mbps to 2.5Gbps, while each C-PHY lane supports HS data rates of 182Mbps to 5.7Gbps. To simplify signal routing, lanes within a given port can be arbitrarily assigned via lane swapping, and their polarity can be inverted if desired. Each CSI port is fully independent, and the user can separately configure or reset each port to suit the requirements of a given application.

Lane swapping registers need to be used to match pin mapping diagram MIPI_PHY3 (0x8A3) set to 0xE4.

Video Pattern Generator

The MAX96712/B includes a pair of flexible video pattern generators (VPG) that serve as a valuable tool for debugging video path functionality. Link lock is not required for VPG operation. Therefore, the VPG feature can be used even when the GMSL link is not functional. For optimal convenience, the VPGs are clocked based on the integrated 25MHz oscillator that provides global clock generation, eliminating the need for the user to provide a dedicated external clock for use with the VPG feature. Available PCLK frequencies are 25MHz, 75MHz, 150MHz, and 375MHz.

Each VPG supports a wide range of video resolutions and frame rates. Two video pattern options are available. The first option is a color gradient; the second option is a checkerboard pattern. All patterns are typically generated using 24b RGB color space. The outputs of the two generators can be synchronized if desired, and the resulting streams can be routed to any of the available C/D-PHY outputs. Aggregation and replication features can be used in conjunction with the VPG produced data streams.

Video PRBS Generator/Checker

In addition to the checkerboard and gradient video pattern generators, each of the internal video pipes includes a video PRBS generator/checker. The available sequences are PRBS7, PRBS9, and PRBS24 at PCLK frequencies of 25MHz, 75MHz, 150MHz, and 375MHz. As is the case for the gradient and checkerboard patterns, the PRBS sequences can be routed by the aggregation and replication capabilities of the MAX96712/B. They are also packetized into CSI-2 compliant streams at the CSI output. The video PRBS stream can be checked by a device located at the opposite end of the CSI-2 link or routed back to the MAX96712/B in a loopback configuration using a CSI-2 input serializer that drives one of the MAX96712/B's GMSL inputs. For more information on the video PRBS functionality, see *GMSL2 Overview*.

CSI Output Raw PRBS Generator

The MAX96712/B facilitates MIPI PHY characterization by enabling the generation of PRBS output streams in HS transmit mode directly from each C-PHY/D-PHY output lane. The available patterns are PRBS9, PRBS11, and PRBS18. The resulting output data is a continuous stream that is not packetized by the CSI-2 controllers.

CFG Latch at Power-up Pins

Voltage levels at the CFG0 and CFG1 pins are latched at power-up or upon a low-to-high transition of PWDNB. These levels set initial register values and functional modes that may not be easily programmed through I^2C or UART after the IC powers up. The CFG pins select device address, GMSL2 or GMSL1, serial rate, coax or STP, and high immunity mode. The user must identify the desired power-up state of the MAX96712/B and correspondingly select the values of the resistors connected to CFG0 and CFG1 according to Table 9 and Table 10.

The voltage level for each pin is set by an external precision resistor divider connected between V_{DDIO} and ground or, for some configurations, by a single resistor connected to V_{DDIO} or ground. Table 9 and Table 10 show the recommended resistor values to select each configuration. The voltage level at the CFG pins is latched about 1ms after all MAX96712/B supplies reach minimum levels required by the power-on-reset (PoR) circuit.

Table 9. CFG0 Input Map

CFG0 INPUT VOLTAGE (PERCENTAGE OF V_{DDIO}) (NOTES A, B)	SUGGESTED RESISTOR VALUES (±1% TOLERANCE) (NOTE C)	MAPPED CONFIGURATION (NOTE D)

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Table 9. CFG0 Input Map (continued)

MIN	TYP	MAX	R1 (Ω)	R2 (Ω)	DEVICE ADDRESS
0.0%	0.0%	11.7%	OPEN	10000	0x52
16.9%	20.2%	23.6%	80600	20500	0x54
28.8%	32.1%	35.5%	68100	32400	0x5A
40.7%	44.0%	47.4%	56200	44200	0x92
52.6%	56.0%	59.3%	44200	56200	0x96
64.5%	67.9%	71.2%	32400	68100	0x9A
76.4%	79.8%	83.1%	20500	80600	0xD2
88.3%	100%	100%	10000	OPEN	0xD6

Table 10. CFG1 Input Map

CFG1 INPUT VOLTAGE (PERCENTAGE of V_{DDIO}) (NOTES A, B)			SUGGESTED RESISTOR VALUES (±1% TOLERANCE) (NOTE C)		MAPPED CONFIGURATION (NOTES D, E)		
MIN	TYP	MAX	R1 (Ω)	R2 (Ω)	CXTP	GMSL1/GMSL2	HIM/ GMSL2 Rate
0.0%	0.0%	11.7%	OPEN	10000	COAX	GMSL2	6Gbps
16.9%	20.2%	23.6%	80600	20500		GMSL1	HIM Enabled
28.8%	32.1%	35.5%	68100	32400			HIM Disabled
40.7%	44.0%	47.4%	56200	44200	STP	GMSL2	6Gbps
52.6%	56.0%	59.3%	44200	56200			3Gbps
64.5%	67.9%	71.2%	32400	68100		GMSL1	HIM Enabled
76.4%	79.8%	83.1%	20500	80600			HIM Disabled
88.3%	100%	100%	10000	OPEN	COAX	GMSL2	3Gbps

Notes:

A) Voltage divider resistor tolerance, V_{DDIO} supply ripple, and external loading must not cause the CFG0 or CFG1 input voltage to exceed the maximum or minimum limits.

B) Until the input voltage is latched, any load on CFG0 or CFG1 (other than R1 and R2) must be ≥ 25 x (R1 + R2). Load capacitance (including R1 and R2) must be lumped load ≤ 10pF.

C) Each resistor in the voltage divider must be ≤100kΩ.

R1 connects to V_{DDIO}, R2 connects to GND.

D) DEVICE ADDRESS: Device Address

CXTP: Shielded twisted-pair (SIO_P, SIO_N) or coax (SIO_P) serial link.

GMSL1/GMSL2: GMSL1 or GMSL2 operating mode.

HIM applies when GMSL1 operating mode is selected. High Immunity mode for reverse control channel.

GMSL2 rate applies when GMSL2 operating mode is selected. 3Gbps or 6Gbps serial link bit rate. Reverse control channel rate is 187.5Mbps for both cases.

E) GMSL1 default BWS = 0 (24-bit).

Multifunction Pin Configuration

The MAX96712/B provides a wide range of peripheral I/O functions. These functions are mapped via register control to an array of multifunction pins (MFP). Each MFP has several possible functions, but only one can be used at a time.

In most cases, MFP pins can be used as generic I/O pins. However, a limited number of pins support only CMOS GPO functionality or open drain output functions. MFP13 is a special case. It defaults to GPO only, which is a useful

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debug feature that enables a toggling GPI on the opposite side of the link to be tunneled across the link with minimal programming. To enable input functionality of this pin, register bit ASIL_GPIO_EN must be written to a value of 1.

The various peripheral interfaces and other special functions are distributed between different pins, enabling the user to utilize a variety of interfaces and special functions simultaneously. Some functions require only a single MFP pin, but many are implemented across a group of MFPs. For example, ERRB is a single MFP while an SPI interface requires several pins. A user selects MFP functions to suit their use-case by programming the appropriate registers.

The *Pin Descriptions* show default and alternate functions for each MFP, listed in order of priority from highest to lowest. Table 11 also shows priority with highest priority on the left. A higher priority function must be disabled when a lower priority function is enabled, both by register writes.

Table 11. MFP Pin Function Map

PIN	LATCH ON POWER-UP	I²C/UART FSYNC	SPI	GMSL1 GPI MS LOCK ERRB	LINE-FAULT	MONITOR	GMSL1 CNTL	GPIO	SPEED GROUP
MFP0				MS	LMN6			GPIO0	D
MFP1				LOCK				GPIO1	D
MFP2		FSYNC		GPI1				GPIO2	D
MFP3				ERRB				GPIO3	D
MFP4		SDA2/RX2		GPI0		VS		GPIO4	D
MFP5			SCLK_0		LMN7			GPIO5	C
MFP6			MOSI_0		LMN0		CNTL1	GPIO6	C
MFP7			MISO_0		LMN1		CNTL2	GPIO7	C
MFP8		SDA1/ RX1(alt)	BNE_0/ SS1_0		LMN2		CNTL3	GPIO8	B
MFP9		SCL1/ TX1(alt)	RO_0/ SS2_0		LMN3		CNTL0	GPIO9	B
MFP10		FSYNC(alt)	SCLK_1	GPI2	LMN4			GPIO10	A
MFP11		SDA1/RX1	MOSI_1					GPIO11	A
MFP12		SCL1/TX1	MISO_1					GPIO12	A
MFP13	I2CSEL		BNE_1/ SS1_1			HS	CNTL4	GPO13 (GPIO13)	B
MFP14		SCL2/TX2	RO_1/ SS2_1	GPI3	LMN5	DE		GPIO14	B
MFP15		SDA/RX						ODO15/ GPI15	I²C
MFP16		SCL/TX						ODO16/ GPI16	I²C

The drive strength of most MFP outputs is adjustable. These MFPs are placed in one of four speed groups, each having an adjustable output transition time setting (TTS). Pins are grouped together according to the most frequently used functions available across multiple pins. Except for I²C/UART and GPI/ODO functions, whose transition times are fixed and specified as I²C speed group, the transition time of each speed group can be changed from the default value by register programming. When the speed group's transition time is changed, the transition time of all MFP's in the speed group is changed. Certain MFP functions override the TTS setting. For example, I²C/UART MFP functions automatically switch the MFP output driver to an open drain output whose speed corresponds to the I²C speed group.

Transition times depend on the transition time setting and V_{DDIO} supply voltage. Refer to Table 12 for typical rise and fall times for each TTS setting. The suggested TTS setting for each speed group at both common V_{DDIO} supply voltages is shown in Table 13. To change drive strength of a group of pins, find the desired I/O function in Table 11 and check the speed group with which it is associated. This is specified in the Speed Group column. The relevant register field for

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each speed group is called x_SPEED, where x is A, B, C, or D depending on the speed group. The register field can be programmed with one of the four possible TTS settings given in Table 12 to specify the transition time of a given group of pins. MFP pins associated exclusively with speed group I^2C have fixed output drive strength and, as a result, no register adjustment of TTS is available for these pins. MFP functions with dedicated open drain outputs, such as I^2C/UART, ERRB, and LOCK, automatically override the output driver configuration so that register control of drive strength is bypassed.

Table 12. MFP Pin Typical Output Rise and Fall Times

TRANSITION TIME SETTING (TTS)	RISE TIME (ns) (20% to 80%), C_L = 10pF		FALL TIME (ns) (80% to 20%), C_L = 10pF	
	V_{DDIO} = 1.8V	V_{DDIO} = 3.3V	V_{DDIO} = 1.8V	V_{DDIO} = 3.3V
00	1.0	0.6	0.8	0.5
01	2.1	1.1	2.0	1.1
10	4.0	2.3	4.3	2.9
11	8.8	5.0	10.1	5.1
I^2C	N/A	N/A	40	30

Table 13. Suggested MFP Pin Speed Settings

SPEED GROUP	SUGGESTED TTS	
	V_{DDIO} = 1.8V	V_{DDIO} = 3.3V
A	01	10
B	11	11
C	01	10
D	11	11

Speed Programming for SPI

The SPI interface can be used over a wide range of frequencies. The MAX96712/B provides flexible GPIO speed programming (see *Multifunction Pin Configuration*) to maintain timing margins while minimizing radiated EMI. Table 14 provides guidance on recommended speed settings for various SPI operating frequencies and V_{DDIO} supply voltages while Table 12 details the typical transition time associated with each available drive strength setting.

At lower frequencies, SPI data is typically latched on the opposite clock edge from which it is shifted, as shown in Figure 21 and Figure 22. However, to meet timing requirements at higher frequencies, the data must be latched on the same edge as the shift. Table 14 provides guidance for programming the latching clock edge.

Table 14. Recommended SPI Pin Programming

FREQUENCY (MHz)	V_{DDIO} (V)	LATCHING EDGE	RECOMMENDED TTS
< 12.5	1.7 to 2.24	Opposite From Shift	01
	2.25 to 3.6		10
12.5 to 25	1.7 to 2.24	Opposite From Shift	00
	2.25 to 3.6		01
25 to 50	1.7 to 2.24	Same As Shift	00
	2.25 to 3.6		01

Power-up and Link Start-up

GMSL2 ICs are in power-down mode when the PWDNB pin is low or when any of the power supplies are disabled. When in power-down mode, device configuration is reset to the default power-up state, and MFP pins are high impedance with internal 1MΩ pulldown.

The serializer and deserializer can power up in any order. After PWDNB is released and all power supplies have settled,

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each device starts its power-up sequence and performs the following operations:

1. Latch CFG and I2CSEL pin states and set internal registers accordingly. See Table 9 and Table 10.
2. Primary control channel (I^2C or UART) is functional on local side. Local device registers are writable and readable. Perform local configuration as needed to establish links.
3. Links are established based on default configuration specified by CFG1 pin power-up state, which specifies global configuration for all links.
4. Perform link calibration, equalizer adaptation, and data channel locking. LOCK pin is driven high when all enabled links are locked and ready. The status of individual links can be monitored by reading individual link lock status bits.
5. Control channel is available from/to remote side.
6. If using the internal V_{DD} regulator (V_{DD} = 1.2V), enable the regulator function as described in the *Power Supplies* section.

The entire link initialization process, from the time the last device's PWDNB input transitions from low to high, takes approximately 20ms nominally and 100ms maximum for any channels that meet the GMSL2 channel specification.

After each link is established, all devices associated with that link can be configured. This can be done locally or remotely over the control channel by a microcontroller on either side of the link.

Device Reset

There are three general reset options available through register writes:

1. RESET_ALL resets all blocks including all registers and digital and analog blocks. This is similar to driving the PWDNB pin low and then high. This bit is automatically cleared when written. **Note:** If Sleep mode is being used, do not use RESET_ALL as it returns the device to Sleep mode.
2. Setting RESET_LINK_x resets all GMSL PHY related logic as well as the data pipeline for the specified link (where x is A, B, C, or D). After this bit is set, all local control registers are still accessible. The link remains in RESET until the bit is cleared.
3. Setting RESET_ONESHOT_x resets all GMSL PHY related logic and the data pipeline for the associated link (where x is A, B, C, or D). The bit then automatically clears itself. This is similar to setting and then clearing one of the RESET_LINK_x bits.

When configuring a GMSL link, program registers that control operation of the desired GMSL link (i.e., CXTP_, GMSL2_) first, then issue a link reset using the associated RESET_LINK_x or RESET_ONESHOT_x bits.

Link and Video Lock

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GMSL2 Link Lock

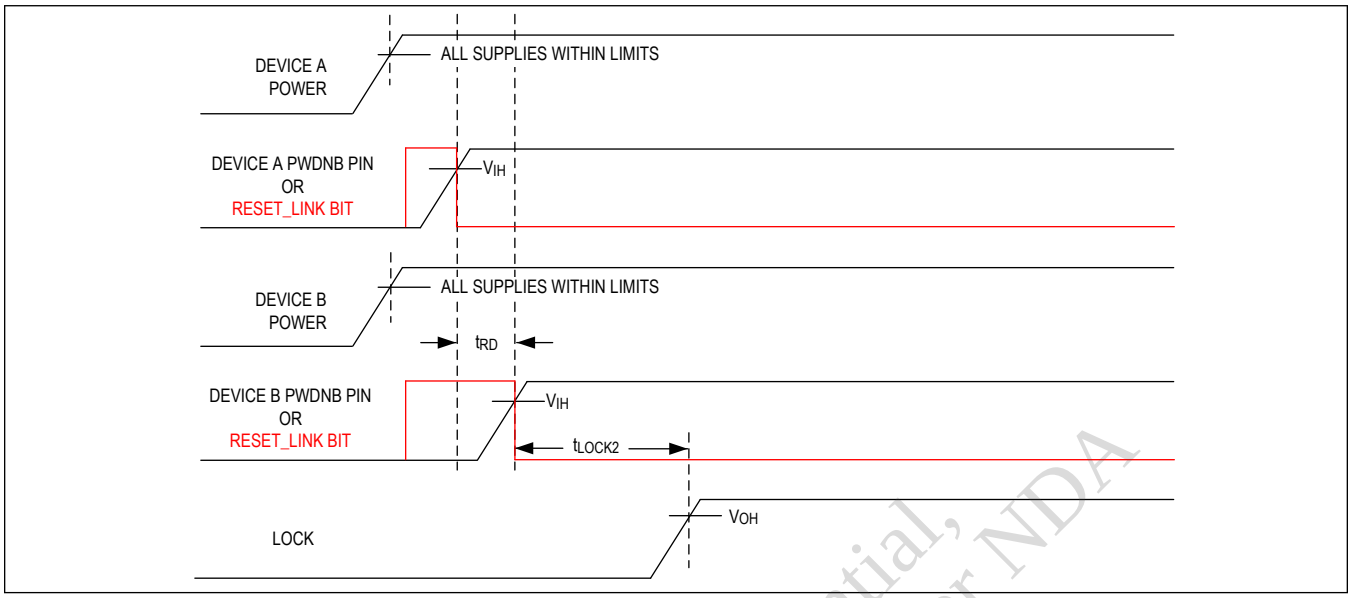

Figure 36. GMSL2 Lock Time

Figure 36 illustrates the sequence that is used to characterize GMSL2 link lock time. Device A is the first device (serializer or deserializer) to power-up or resume operation from a RESET_LINK

state. Device B is the device (deserializer or serializer) at the other end of the GMSL link.

Link lock indicates that the data receive paths are locked (forward channel in the deserializer, reverse channel in the serializer). Video and control channel functions (I^2C, GPIO) can be used immediately after link lock is asserted.

The device will establish single link GMSL2 connectivity and link lock automatically following power-up. This is an indication that the cable is plugged in and the system is up and running. Lock is obtained with no interaction between the µC and GMSL devices. Both serializers and deserializers have an open-drain LOCK output pin and a related status register.

The GMSL2 link uses the crystal as the reference clock for GMSL2 links, so a valid video input (PCLK) is not needed for the GMSL2 link to lock.

Notes:

1. The lock sequence is initiated by the release of the PWDNB pin or the RESET_LINK bit in either the serializer or the deserializer.
2. Lock time is measured from the later of PWDNB or RESET_LINK release in either the serializer or deserializer to LOCK being asserted.
3. The PWDNB/RESET_LINK states on the two sides of the link must have overlap when both devices are in PWDNB/RESET_LINK mode prior to the lock process starting.
4. If RESET_LINK is used to initiate lock, PWDNB is assumed to be high after power-up (normal operation).
5. If PWDNB is used to initiate the lock, RESET_LINK is assumed to be low after power-up (normal operation).
6. To achieve the specified lock time, time delay t_{RD} (delay between release of the PWDNB/RESET_LINK on the two devices) must be less than the threshold specified in Note 9. Contact the factory for guidance if this timing cannot be guaranteed.
7. Lock time and maximum allowed t_{RD} vary between different families of GMSL devices. They depend on the characteristics of both the serializer and the deserializer. The typical lock time of a specific link can be best estimated as the longer of the lock times specified in each device data sheet. Similarly, the maximum permissible t_{RD} for a specific link can be estimated as the smaller of the values specified in each device data sheet. For further guidance, contact the factory.

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8. If there is an instantaneous interruption to link lock, a period of 100ms following loss of lock should be provided to enable the link to automatically recover prior to any ECU initiated resets being issued. This will minimize any disruptions caused by a transient loss in connectivity.

Video Lock

Video lock indicates that the deserializer is receiving valid video data. After the GMSL2 link is locked, the deserializer video output PLL starts its locking sequence. The deserializer normally starts outputting video data several milliseconds after it asserts line lock, provided that it is receiving video packets from the serializer. Video lock status is typically read from a register.

Clocking

Reference Clock

GMSL2 devices require a reference clock source to generate the 6GHz line rate clock and associated internal clocks. Both serializers and deserializers are clocked via 25MHz crystals or external low jitter 25MHz clock sources with a frequency accuracy of ±200ppm.

Spread-Spectrum Clocking

Maxim's GMSL2 links provide exceptional electromagnetic interference (EMI) performance. Optional spread-spectrum clocking (SSC) is available to mitigate EMI emitted from devices and inter-connections and provide additional margin. SSC reduces peaks in the frequency spectrum by spreading the signal over a wider bandwidth. The spread has a 25kHz sawtooth modulation profile, programmable to deviate up to 2500ppm pk-pk.

Error and Fault Condition Monitoring

The MAX96712/B includes an open-drain, multipurpose error reporting and interrupt status output. The active-low ERRB pin is driven by the logical OR of a wide variety of error and event status indicators. Errors can be automatically forwarded across the link from the serializer, so certain serializer side errors, such as CSI-2 input CRC errors, can automatically be flagged by the MAX96712/B's LOCK output. The ability of each error condition to drive ERRB is maskable by register settings. Each error and event that can drive ERRB has a status flag within a sub-block of registers, so the reason for assertion of ERRB can be determined by reading the register status.

Line-Fault

GMSL2 devices include a novel line-fault detection circuit. It detects and reports open-circuit, short to battery, short to ground, and line-to-line short conditions on the GMSL interconnect. The line-fault monitor requires external resistors R_{EXT} and R_{PD} connected to the LMN pins as shown in Figure 37 and Figure 38. Note that these figures illustrate the connection scheme that is employed when the deserializer's line-fault detectors are used, which is typically the case in camera applications. The serializer's line fault detectors can alternatively be used and, in this case, the LMN connections and placement of R_{EXT} and R_{PD} are reversed between the serializer and deserializer sides of the link. Whether serializer or deserializer line-fault detectors should be used depends on the architecture of a given system. In general, the device that is used to detect line-fault should have a clear communication channel to the primary system controller module that does not depend on the integrity of the GMSL link. In both cases, a 49.9kΩ, 1% tolerance resistor (R_{PD}) is connected from each GMSL signal line to ground at the end of the link opposite the location of the line-fault detectors, while a 42.2kΩ (LMN0 with STP) or 48.7kΩ (LMN0 with coax, LMN1) 1% tolerance resistor (R_{EXT}) is connected from each GMSL signal line to the relevant LMN_ pin of the device whose line-fault detectors are utilized. Only the specified resistor values/tolerances should be used to ensure correct functionality. Note that R_{PD} and R_{EXT} are located on opposite sides of the link, so the line-fault detection must be considered in the design of both the serializer and deserializer portions of a system. Line-fault detection cannot be used in conjunction with power-over-cable (PoC), and it should not be used in applications in which there is a potential difference between the grounds at opposite ends of the link.

The MAX96712/B provides four pairs of line-fault detection inputs. The LMN functions are available as part of the MFP pin array. The presence of a fault condition can be flagged using the ERRB output. The line-fault monitor pins offer flexible connection and programming. Each line-fault input can be assigned to either polarity of the link when in STP mode. In coax mode, a single line fault input is required and, in this case, either of the available line-fault input functions within a given pair can be used. The unneeded line-fault function within each pair can be disabled, and the corresponding MFPs

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can be used for other functions in coax mode. In applications that do not require line-fault detection, line-fault inputs can be disabled and the corresponding MFPs can be used for alternate functions as needed. When using line-fault detection with STP interconnects, it is important to correctly associate each pair of pins to enable full functionality (LMN0 + LMN1, LMN2 + LMN3, LMN4 + LMN5, and LMN6 + LMN7).

The presence of a fault can be reported by the ERRB MFP function, as mentioned previously. A fault condition generates an interrupt that is forwarded across the link such that the ERRB output of the serializer flags a line-fault detected by the deserializer and vice-versa. In addition, the LFLT_INT bits flag the presence of a fault condition, enabling convenient register access. In the event of a fault, ERRB is driven low while LFLT_INT is written to a value of 1. Further details of a fault event are available in register fields LF_0 to LF_7, depending on which line-fault inputs are being used in a given application.

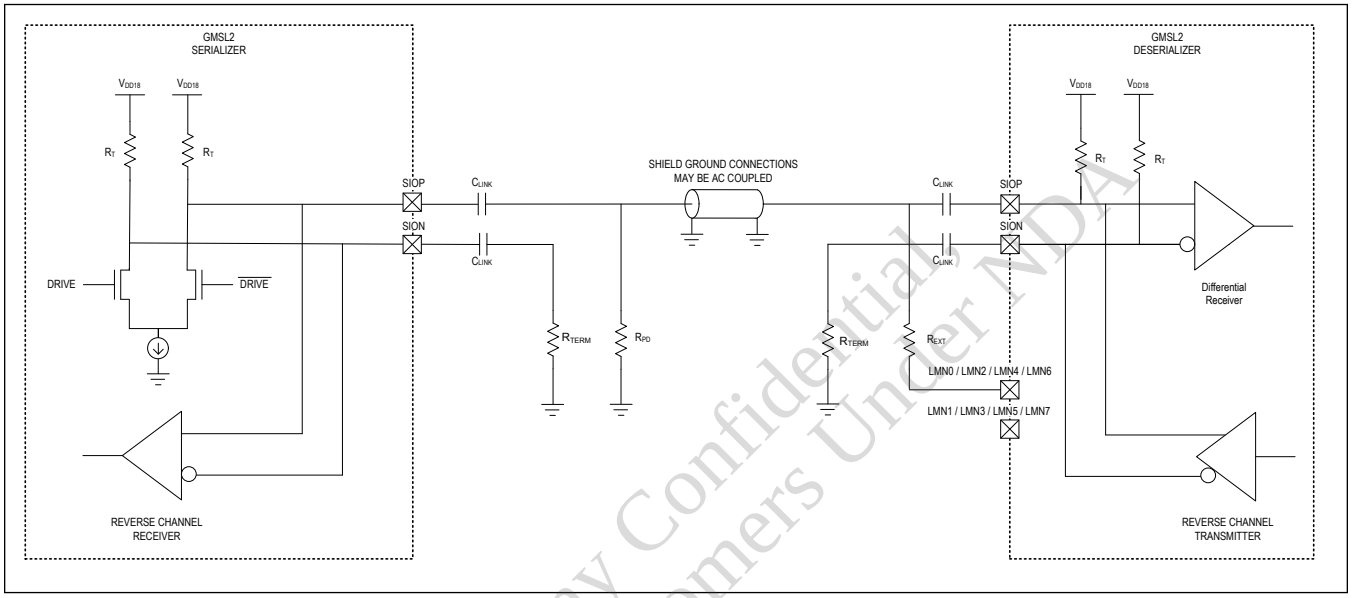

Figure 37. Typical GMSL1/2 Link Application Circuit for Coax Cable

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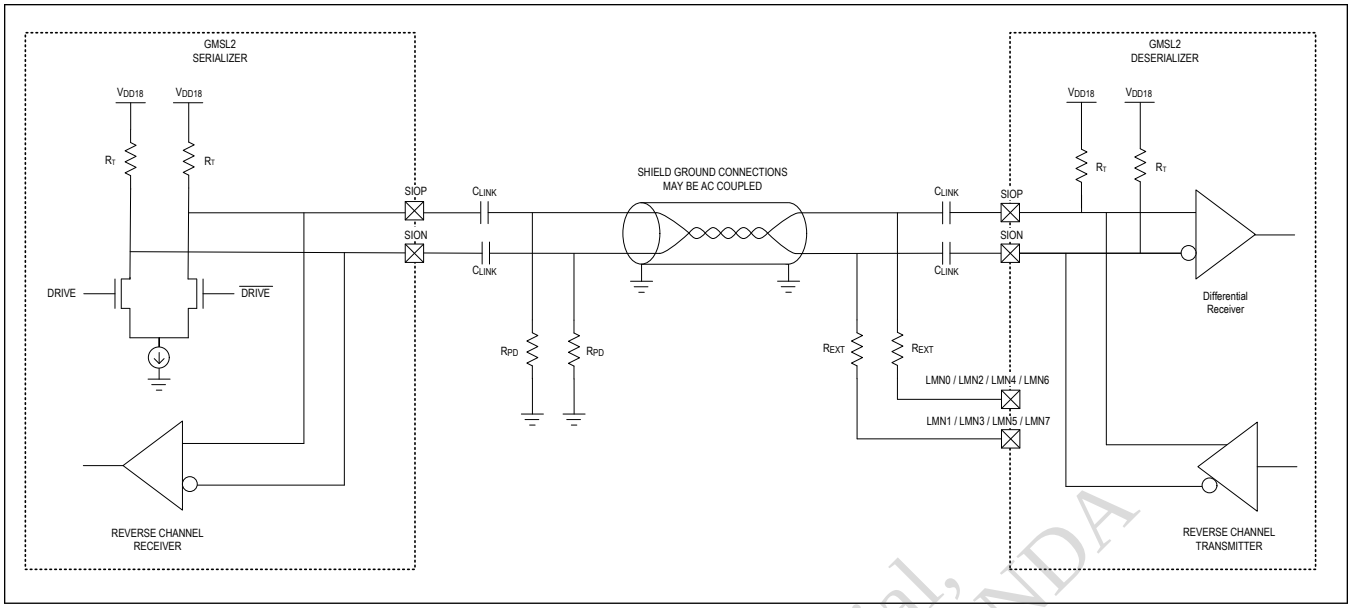

Figure 38. Typical GMSL1/2 Link Application Circuit for Twisted Pair

Power Supplies

The MAX96712/B provides flexible power supply configurations.

The 1V core supply can be provided directly or supplied by an internal regulator. To minimize power dissipation, connect 1.0V ±5% to V_{DD}. If V_{DD} < 1.1V and CAP_VDD < 1.05V, the regulator is automatically disabled at power-up and low-resistance switches connect V_{DD} to the internal supply rails. If using the internal regulator, connect 1.2V ±5% to V_{DD} and write REG_ENABLE = 1 and REG_MNL = 1 in order following power-up as part of the device initialization to enable the internal LDO.

The V_{DDIO} supply for the I/O pins can be 1.8V to 3.3V for flexibility in accommodating devices interfacing to the MAX96712/B. The allowable supply voltage range is 1.7V (1.8V -5%) to 3.6V (3.3V +9%).

V_{DD18} is the primary analog supply. Connect 1.8V ±5%.

V_{TERM} is the supply for the MIPI CSI C-PHY/D-PHY interface. Connect 1.2V ±5%.

Proper bypassing of all supplies is essential for optimal performance. In all cases, a decoupling capacitor should be placed as close as possible to each supply pin. See Table 3 for guidance regarding appropriate decoupling for each supply pin. See Table 2 for power supply tolerances and noise requirements. Contact the factory for guidance on sharing supplies and optimizing supply decoupling.

Power Supply Monitoring

Extensive power supply diagnostics capabilities are provided by the device. Undervoltage detection is included for all power supplies. Under voltage conditions on the V_{DD18}, V_{DDIO}, and V_{TERM} supply voltages can be indicated via either the ERRB pin or by reading the register field associated with the power supply undervoltage flag. An undervoltage condition on the V_{DD} supply, which can corrupt the register configuration, is detected by the power manager and results in a reset. Similarly, severe undervoltage conditions on V_{DDIO} or V_{DD18} also result in a reset. In the case of a reset, device configuration reverts to the power-up default state when the supplies have recovered, and the host device must initiate the power-on initialization procedure to return the device to full operation.

Overvoltage detection is also provided, although only for the internal V_{DD} supply voltage (CAP_VDD). As in the case of undervoltage events, an overvoltage situation can be reported by the ERRB pin in addition to a dedicated internal interrupt flag. No further action is taken by the power manager during an overvoltage situation. The device continues to operate normally, although it may sustain damage depending on the duration and magnitude of the overvoltage event.

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Standby and Sleep Mode

A power manager block is present in all GSML2 products. Its primary function is to monitor supply voltages and control Power-down (standby) and Sleep modes.

There are two ways to go into low power mode while all power supplies are active: asserting the PWDNB pin or invoking the sleep state. Both states offer very low power supply currents.

Asserting the PWDNB pin (active-low) places the device in Standby Power mode and resets the digital registers and configurations to their default power-up condition. Any supply dropping below its internal threshold settings also places the device in Power-down mode.

The sleep state provides preservation of critical register settings and configurations. The register table indicates which registers are retained. The device can be put into a sleep state through an I^2C/UART command. The resume state restores the device back to the pre-sleep condition without the need for additional register writes. A resume is invoked by an I^2C command or a low-frequency clock beacon transmitted from the main device over the GMSL2 link.

GPIOs are in Hi-Z during standby and sleep modes. The status of all GPIOs is retained in Sleep mode.

Note: If Sleep mode is being used, do not use RESET_ALL as it will return the device to Sleep mode instead of resetting all device values.

Thermal Management

Power consumption of the MAX96712/B varies based on the use case. Care must be taken by the user to provide sufficient heat dissipation with proper board design and cooling techniques. The package's exposed pad must be connected to the PCB ground plane by an array of vias. This approach simultaneously provides the lowest electrical and thermal impedances.

System thermal management must keep the operating junction temperature below 125°C to meet electrical specifications and avoid impacting device reliability.

Refer to Tutorial 4083 (*www.maximintegrated.com/thermal-tutorial*) for further guidance.

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Applications Information

Software Programming Model

GMSL automotive serializers and deserializers are designed to follow a general software programming model. Except for features that require in-operation control channel accesses, such as the ASIL safety measures and interrupt handling, the following programming model should be followed:

1. Set the impacted functional blocks to Disabled or Reset mode. A general method to place the part in IDLE state is to stop all side channel and video traffic followed by a register write (RESET_LINK=1) to stop the GMSL link.
2. It is required that the settings for each feature are fully configured before it is enabled.
3. Establish the link by setting RESET_LINK=0 and wait for link to lock.
4. Start video and side channel traffic.

If changing the configuration of a feature is required during operation of other features, disable the feature that will be reconfigured, change its settings, and re-enable it.

Control-Channel Programming

MAX96712/B internal registers can be accessed locally via any of the three available I^{2}C/UART ports. Lower indexed ports have higher priority in the case of simultaneous queries. By default, remote GMSL serializer register access is available via I^{2}C/UART port 0 only. However, the internal I^{2}C/UART routing mux enables any of the three ports to connect to the control channel, which thereby provides access to remote serializer registers. Only one of the three ports can access the control channel at a given time, and the other two I^{2}C/UART ports then function essentially as remote pass-throughs from the perspective of the serializer. See *I^{2}C/UART* for further details regarding the routing of I^{2}C/UART ports in the MAX96712/B. For multi-main configurations with microcontrollers connected to both the serializer and deserializer, bus contention can be avoided by using register settings to disable the remote control channel. In all cases, register addresses are 16-bits wide. Single or multiple data bytes can be written or read (by address autoincrements).

Device Address

Each device on the I^{2}C/UART control channel must have a unique address. This includes both peripherals and GMSL devices. The GMSL2 device address is set to one of several 7-bit addresses according to the voltage level of the CFG0 pin at power-up. See *CFG Latch at Power-up Pins* for further details. Note that device address can be changed after power-up by writing to the DEV_ADDR register.

I^{2}C Programming

Each device has an internal I^{2}C subordinate for register access. The internal registers can be written and read according to the I^{2}C protocol using the packet formats below. Each transmission consists of a START condition sent by a main, followed by the device's 7-bit subordinate address plus a R/W bit, register address bytes, one or more data bytes, and finally a STOP condition. SDA and SCL lines operate as both an input and an open-drain output. External pullup resistors are required on SDA and SCL.

Primary I^{2}C Host-to-GMSL2 Device Communication

The host I^{2}C main has access to GMSL2 serializer and deserializer registers. Any of the MAX96712/B's I^{2}C interfaces can be used to access local GMSL2 device registers. In the case of contention, the lower indexed port has precedence. Remote GMSL2 device registers can be accessed by any one of the three available ports. Only one port can access remote device registers via a given GMSL link at a time. By default, port 0 is configured to have remote device register access.

I^{2}C Write Packet Format

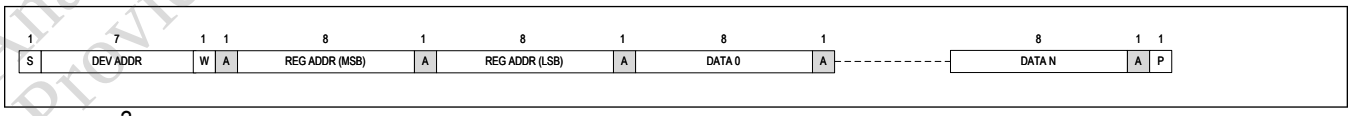

Figure 39. I^{2}C Write Packet Format

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I²C Read Packet Format

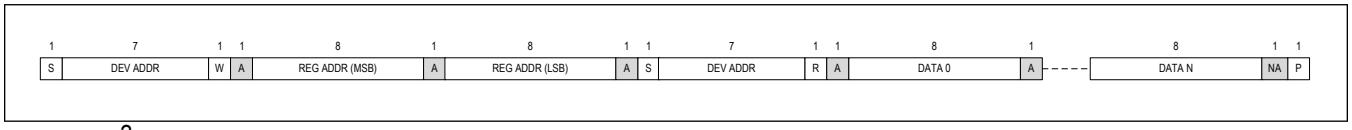

Figure 40. I²C Read Packet Format

Host-to-Peripheral Primary I²C and Pass-Through I²C Communication

When communicating between a host and peripheral, primary and pass-through I²C operation is the same. An I²C tunnel across the GMSL2 link connects the host's I²C main to the remote I²C subordinate. This logically connects separated I²C buses, enabling I²C transactions across the serial link to occur (with some delay) as if performed on the same physical I²C bus. The GMSL2 serializer and deserializer are intermediary devices; the host I²C main connects to a GMSL2 device I²C subordinate, and the peripheral I²C subordinate connects to a GMSL2 device I²C main.

For example, when the host I²C main transacts on one side of the link (local-side), the I²C subordinate of the local-side GMSL2 device forwards data to the other side (remote-side). Data is then received by the I²C main of the remote-side GMSL2 device, which in turn generates the same I²C transaction with the peripheral subordinate I²C. The remote-side GMSL2 device sends back any I²C data expected by the local-side.

The I²C interface uses clock stretching (holding SCL low) to account for timing differences between main and subordinate and to allow time for data to be forwarded and received across the serial link.

The host device can program GMSL2 device registers to independently configure the pass-through I²C/UART interfaces for communication over specified GMSL links as either I²C or UART.

UART Programming

When the primary I²C/UART interface is configured as UART, there are two operating modes: base and bypass.

UART Base Mode

Base mode is the means of µC communication with the serializer and deserializer in which internal registers in these devices can be accessed in addition to registers in peripheral devices. Base mode is enabled by default at power-up. In base mode, the µC is the host and can access the registers of both the serializer and deserializer from either side of the link using the GMSL2 UART packet protocol (see Figure 41). The µC can also communicate with compatible peripherals on the remote side when the remote side GMSL2 device's local control channel is enabled. The device addresses of the serializer and deserializer in this mode are programmable.

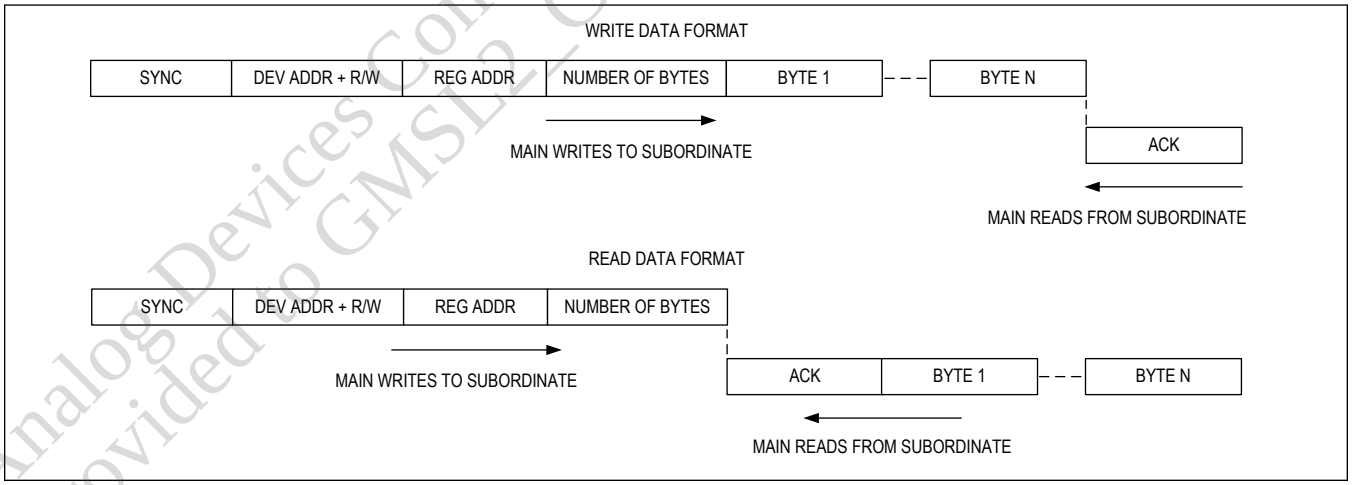

Figure 41. GMSL2 UART Protocol for Base Mode

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UART Bypass Mode

In bypass mode, the serializer/deserializer ignores UART commands from the µC, allowing the µC to communicate only with peripheral devices. The µC cannot access the serializer/deserializer registers in this mode, and as a result the addresses of the GMSL devices are not programmable. The UART transitions are simply sent over the GMSL link and routed directly to the attached peripherals. Ignoring UART transactions prevents inadvertent misprogramming of serializer and deserializer registers.

Switching Between UART Base and Bypass Modes

Selection of the UART mode can be specified by either register programming or appropriate control of the MS pin.

When register programmed, bypass mode is active only as long as there is UART activity. When there is no UART activity for a selected timeout, both devices exit bypass mode, and the bit is automatically cleared.

When set by the MS pin, a high pin level puts the device into bypass mode, and a low level puts the device in base mode. MS is set on-the-fly and is not latched on power-up.

UART Frame Format

Regular UART frames with an even parity bit are used to carry 1 byte of data each. A frame consists of a low start bit followed by 8 data bits, a parity bit, and a high stop bit. The parity bit is high if the number of ones in the 8 bits of data is odd, otherwise, the parity bit is low. There must be at least 1 high stop bit. If the next frame is in the same packet, there can be at most 4 high bits from the end of the stop bit to the beginning of the next start bit. Note that in the case of a parity bit error, the packet, starting from the frame with the error, is discarded. The start of each frame is always a high-to-low transition (i.e., the stop bit is high and the start bit is low). The phase of the internal UART bit clock is adjusted using the start bit of each frame. The framer calibrates the length of one UART bit in terms of the internal oscillator clock using the synchronization frame (i.e., the first frame of a UART packet transmission). In bypass mode, the parity bit is enabled by default, but the frames are not checked for parity errors. Either even or odd parity can be used. The parity bit is passed along with UART data transmissions; the recipient of the data must perform error checking. Optionally, the parity bit can be disabled before entering bypass mode. Note that the bit rate in bypass mode must be the same bit rate last used in base mode.

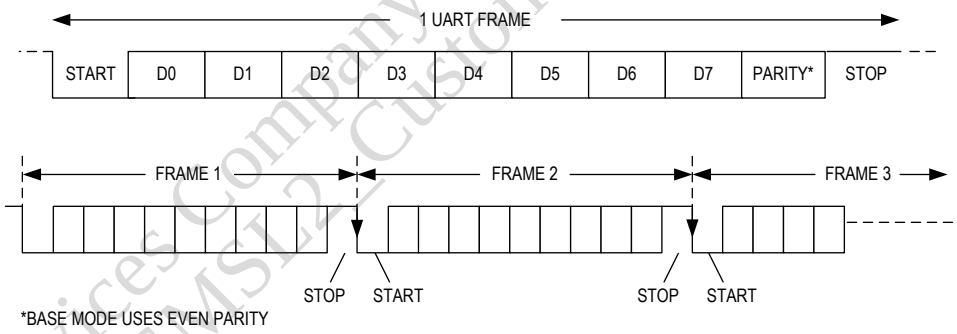

Figure 42. UART Data Format for Base Mode

Synchronization Frame

The serializer/deserializer must calibrate internal bit length counters with the UART bit rate for proper recovery of UART frames. A sync frame (a regular UART frame with the value 0x79) is sent as the first frame of each data packet from the µC and is used to calibrate the bit length in terms of the device's internal 150MHz clock. Sync frames must be properly detected before the subsequent frames of the packet can be correctly received. When the line stays high for at least 32 bits, the packet boundary is reset and the framer begins waiting for the next sync frame.

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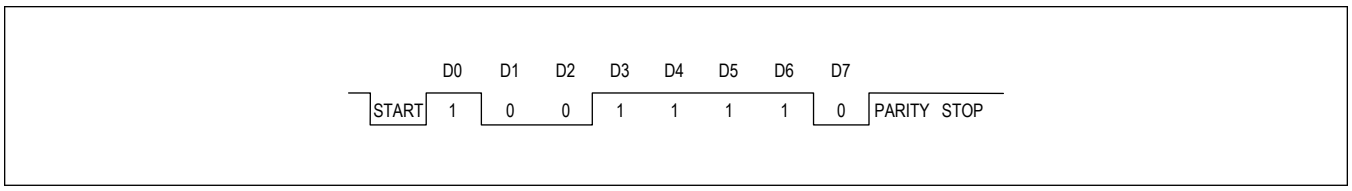

Figure 43. UART Synchronization Frame

Acknowledge Frame

When a packet is successfully received, the addressed device responds with an acknowledge frame to inform the µC that no errors are detected in the transmitted packet, and it is recognized as valid. This is sent after the last bit of a successfully recognized packet is received. The acknowledge frame is a regular UART frame (value 0xC3). Data written to the serializer/deserializer registers does not take effect until after the acknowledge byte is sent.

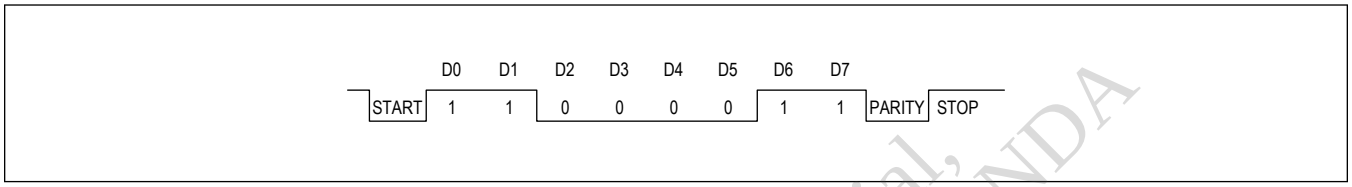

Figure 44. UART Acknowledge Frame

Write Packet

A write packet consists of a 5 byte packet header followed by 1 or more data bytes. A packet is recognized as a write packet when the LSB of the device address frame is 0. The addressed device responds with an acknowledge frame if no errors are detected while receiving the packet. Byte count indicates the number of data bytes to be written, and this number cannot be zero.

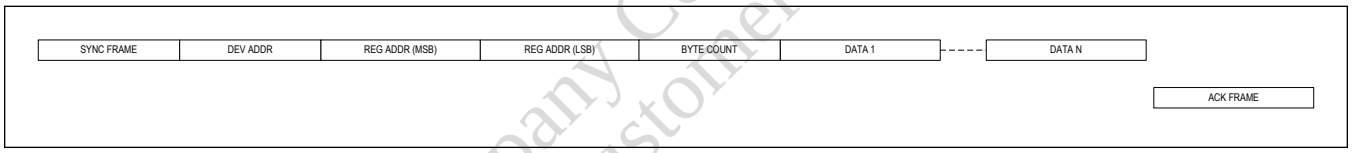

Figure 45. UART Write Packet Format

Read Packet

A read packet consists of 5 bytes. The LSB of the device address frame is 1 for read packets. If no errors are detected while receiving a valid read packet, the addressed device responds with an acknowledge frame followed by 1 or more data bytes. Byte count indicates the number of data bytes to be read, and this number cannot be zero.

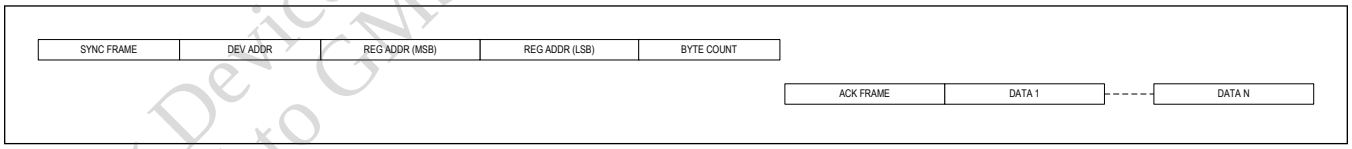

Figure 46. UART Read Packet Format

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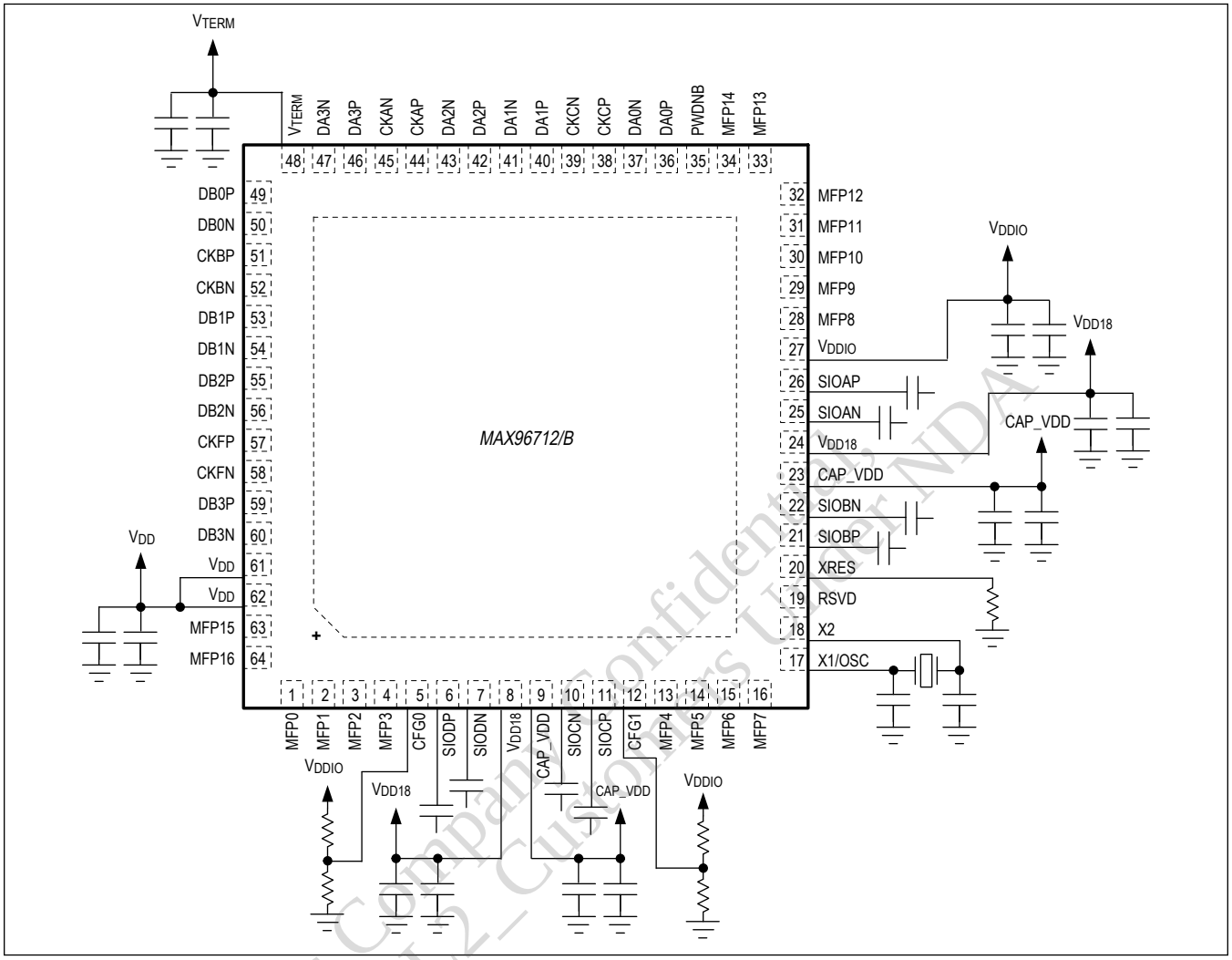
Typical Application Circuits



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Ordering Information

PART NUMBER	RoR	TEMP RANGE	PIN-PACKAGE
MAX96712GTB/V+		-40°C to +105°C	64 TQFN-EP
MAX96712GTB/V+T		-40°C to +105°C	64 TQFN-EP (Tape & Reel)
MAX96712GTB/VY+		-40°C to +105°C	64 TQFN-SW-EP
MAX96712GTB/VY+T		-40°C to +105°C	64 TQFN-SW-EP (Tape & Reel)
MAX96712BGTB/V+	X	-40°C to +105°C	64 TQFN-EP
MAX96712BGTB/V+T	X	-40°C to +105°C	64 TQFN-EP (Tape & Reel)
MAX96712BGTB/VY+	X	-40°C to +105°C	64 TQFN-SW-EP
MAX96712BGTB/VY+T	X	-40°C to +105°C	64 TQFN-SW-EP (Tape & Reel)

/V Denotes an Automotive Qualified Product.

+ Denotes a lead(Pb)-free/RoHS-compliant Package.

T Denotes tape-and-reel.

EP Denotes Exposed Pad.

Y Denotes Wettable Flank.

B Denotes RoR functionality

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Register Map

Reserved and Unused Register Bits

Not all register bits in the register space are shown in the register table. Any bit not explicitly defined in the register table should be treated as reserved and should not be modified. When a write is required to a register with both defined and undefined register bits, first read the register's contents, then create a new register value by only changing the defined bits, and finally, write the new byte to the register (Read/Replace/Write). In this document, default values are provided for read-only register bits. Read-only bit states are changed at power-up according to the actual state of the device. To avoid overwriting these bits, treat read-only bits as undefined.

Programming Notes

Lane swapping registers need to be used to match pin mapping diagram. Set MIPI_PHY3 (0x8A3) to 0xE4

For robust RoR performance, execute the following register writes during initialization:

- SIOA = 0x148C = 0x20, 0x1498 = 0xC0
- SIOB = 0x158C = 0x20, 0x1598 = 0xC0
- SIOC = 0x168C = 0x20, 0x1698 = 0xC0
- SIOD = 0x178C = 0x20, 0x1798 = 0xC0

For specified performance, execute the following register writes during initialization:

- Set bits [2:0] = 3'b000 in registers 0x1445, 0x1545, 0x1645, 0x1745
- Set bits [7:0] = 0x03 in registers 0x14D1, 0x15D1, 0x16D1, 0x17D1
- Set bits [7:0] = 0x10 in register 0x6C2

For any applications with at least one 6G link, execute the following register writes during initialization:

- Set Bit [2] = '1' in registers 0x1449, 0x1549, 0x1649, 0x1749

* Indicates the register is stored when entering Sleep mode and is restored upon exit.

ADDRESS	RESET	NAME	MSB							LSB
DEV										
0x00	0x90	REG0[7:0]	DEV_ADDR[6:0]							CFG_BLOCK
0x01	0x00	REG1[7:0]	IIC_SEL[1:0]		DIS_LOC_CC[1:0]		IIC_SEL_P2	DIS_LOC_CC_P2	ALT_IIC_SEL	FAILOVER
0x03	0xAA	REG3[7:0]	DIS_REM_CC_D[1:0]		DIS_REM_CC_C[1:0]		DIS_REM_CC_B[1:0]		DIS_REM_CC_A[1:0]	
0x04	0xFF	REG4[7:0]	VID_EN_7	VID_EN_6	VID_EN_5	VID_EN_4	VID_EN_3	VID_EN_2	VID_EN_1	VID_EN_0
0x05	0xC0	REG5[7:0]	LOCK_EN	ERRB_EN	LOCK_CFG	–	–	–	–	–
0x06	0xFF	REG6[7:0]	GMSL2_D	GMSL2_C	GMSL2_B	GMSL2_A	LINK_EN_D	LINK_EN_C	LINK_EN_B	LINK_EN_A
0x07	0x00	REG7[7:0]	CC_CROSSOVER_SEL[7:0]							
0x08	0x00	DEBUG_EXTRA_1[7:0]	PATGEN_SYNC	–	–	–	RSVD[3:0]			
0x09	0x00	DEBUG_EXTRA[7:0]	DEBUG_EXTRA[7:0]							
0x0A	0x00	CTRL12[7:0]	RSVD	RSVD	–	–	LOCKED_B	–	–	–

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ADDRESS	RESET	NAME	MSB							LSB
0x0B	0x00	CTRL13[7:0]	RSVD	RSVD	–	–	LOCKED_C	–	–	–
0x0C	0x00	CTRL14[7:0]	RSVD	RSVD	–	–	LOCKED_D	–	–	–
0x0D	0xA0	REG13[7:0]	DEV_ID[7:0]							
0x0E	0x0F	REG14[7:0]	DIS_LOCAL_WAKE_P2	–	AUTO_SLEEP_DIS	–	DIS_REM_CC_P2[3:0]			
0x10	0x22	REG26[7:0]	TX_RATE_PHYB[1:0]		RX_RATE_PHYB[1:0]		TX_RATE_PHYA[1:0]		RX_RATE_PHYA[1:0]	
0x11	0x22	REG27[7:0]	TX_RATE_PHYD[1:0]		RX_RATE_PHYD[1:0]		TX_RATE_PHYC[1:0]		RX_RATE_PHYC[1:0]	
TOP_CTRL										
0x12	0x00	PWR0[7:0]	VDDBAD_STATUS[2:0]			CMP_STATUS[4:0]				
0x13	0x00	PWR1[7:0]	RSVD	RESET_ALL	RSVD[5:0]					
0x17	0x10	CTRL0[7:0]	WAKE_EN_D	WAKE_EN_C	WAKE_EN_B	WAKE_EN_A	SLEEP	REG_ENABLE	DIS_LOCAL_WAKE[1:0]	
0x18	0x00	CTRL1[7:0]	RESET_LINK_D	RESET_LINK_C	RESET_LINK_B	RESET_LINK_A	RESET_ONESHOT_D	RESET_ONESHOT_C	RESET_ONESHOT_B	RESET_ONESHOT_A
0x19	0x84	CTRL2[7:0]	RSVD	RSVD	RSVD	REG_MNL	RSVD[1:0]		RSVD[1:0]	
0x1A	0x10	CTRL3[7:0]	RSVD	RSVD	RSVD[1:0]		LOCKED	ERROR	CMU_LOCKED	RSVD
0x22	0xAA	CTRL11[7:0]	RSVD	CXTP_D	RSVD	CXTP_C	RSVD	CXTP_B	RSVD	CXTP_A
0x23	0xA0	INTR0[7:0]	RSVD	RSVD	RSVD	–	AUTO_ERR_RST_EN	DEC_ERR_THR[2:0]		
0x24	0x00	INTR1[7:0]	PKT_CNT_EXP[3:0]				AUTO_CNT_RST_EN	PKT_CNT_THR[2:0]		
0x25	0x0F	INTR2[7:0]	RSVD	RSVD	RSVD	RSVD	DEC_ERR_OEN_D	DEC_ERR_OEN_C	DEC_ERR_OEN_B	DEC_ERR_OEN_A
0x26	0x00	INTR3[7:0]	RSVD	RSVD	RSVD	RSVD	DEC_ERR_FLAG_D	DEC_ERR_FLAG_C	DEC_ERR_FLAG_B	DEC_ERR_FLAG_A
0x27	0x07	INTR4[7:0]	EOM_ERR_OEN_D	EOM_ERR_OEN_C	EOM_ERR_OEN_B	EOM_ERR_OEN_A	RTTN_CRC_ERR_OEN	LFLT_INT_OEN	WM1_ERR_OEN	WM_ERR_OEN
0x28	0x00	INTR5[7:0]	EOM_ERR_FLAG_D	EOM_ERR_FLAG_C	EOM_ERR_FLAG_B	EOM_ERR_FLAG_A	RTTN_CRC_INT	LFLT_INT	WM1_ERR_FLAG	WM_ERR_FLAG
0x29	0xFD	INTR6[7:0]	G1_D_ERR_OEN	G1_C_ERR_OEN	G1_B_ERR_OEN	G1_A_ERR_OEN	LCRC_ERR_OEN	VPRBS_ERR_OEN	REM_ERR_OEN	FSYNC_ERR_OEN
0x2A	0x00	INTR7[7:0]	G1_D_ERR_FLAG	G1_C_ERR_FLAG	G1_B_ERR_FLAG	G1_A_ERR_FLAG	LCRC_ERR_FLAG	VPRBS_ERR_FLAG	REM_ERR_FLAG	FSYNC_ERR_FLAG

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ADDRESS	RESET	NAME	MSB							LSB
0x2B	0x00	INTR8[7:0]	RSVD	RSVD	RSVD	RSVD	IDLE_ERR_OEN_D	IDLE_ERR_OEN_C	IDLE_ERR_OEN_B	IDLE_ERR_OEN_A
0x2C	0x00	INTR9[7:0]	RSVD	RSVD	RSVD	RSVD	IDLE_ERR_FLAG_D	IDLE_ERR_FLAG_C	IDLE_ERR_FLAG_B	IDLE_ERR_FLAG_A
0x2D	0x0F	INTR10[7:0]	RT_CNT_OEN_D	RT_CNT_OEN_C	RT_CNT_OEN_B	RT_CNT_OEN_A	MAX_RT_OEN_D	MAX_RT_OEN_C	MAX_RT_OEN_B	MAX_RT_OEN_A
0x2E	0x00	INTR11[7:0]	RT_CNT_FLAG_D	RT_CNT_FLAG_C	RT_CNT_FLAG_B	RT_CNT_FLAG_A	MAX_RT_FLAG_D	MAX_RT_FLAG_C	MAX_RT_FLAG_B	MAX_RT_FLAG_A
0x2F	0x9F	INTR12[7:0]	ERR_TX_EN	MEM_ERR_OEN	–	ERR_TX_ID[4:0]				
0x30	0xDF	INTR13[7:0]	ERR_RX_EN_A	RSVD	–	ERR_RX_ID_A[4:0]				
0x31	0xDF	INTR14[7:0]	ERR_RX_EN_B	RSVD	–	ERR_RX_ID_B[4:0]				
0x32	0xDF	INTR15[7:0]	ERR_RX_EN_C	RSVD	–	ERR_RX_ID_C[4:0]				
0x33	0xDF	INTR16[7:0]	ERR_RX_EN_D	RSVD	–	ERR_RX_ID_D[4:0]				
0x35	0x00	CNT0[7:0]	DEC_ERR_A[7:0]							
0x36	0x00	CNT1[7:0]	DEC_ERR_B[7:0]							
0x37	0x00	CNT2[7:0]	DEC_ERR_C[7:0]							
0x38	0x00	CNT3[7:0]	DEC_ERR_D[7:0]							
0x39	0x00	CNT4[7:0]	IDLE_ERR_A[7:0]							
0x3A	0x00	CNT5[7:0]	IDLE_ERR_B[7:0]							
0x3B	0x00	CNT6[7:0]	IDLE_ERR_C[7:0]							
0x3C	0x00	CNT7[7:0]	IDLE_ERR_D[7:0]							
0x40	0x00	CNT8[7:0]	PKT_CNT_A[7:0]							
0x41	0x00	CNT9[7:0]	PKT_CNT_B[7:0]							
0x42	0x00	CNT10[7:0]	PKT_CNT_C[7:0]							
0x43	0x00	CNT11[7:0]	PKT_CNT_D[7:0]							
0x44	0x8F	VID_PXL_CRC_ERR_OEN[7:0]	MEM_ECC_ERR2_OEN	MEM_ECC_ERR1_OEN	–	–	VID_PXL_CRC_ERR_OEN_D	VID_PXL_CRC_ERR_OEN_C	VID_PXL_CRC_ERR_OEN_B	VID_PXL_CRC_ERR_OEN_A
0x45	0x00	VID_PXL_CRC_ERR_INT[7:0]	MEM_ECC_ERR2_INT	MEM_ECC_ERR1_INT	–	–	VID_PXL_CRC_ERR_D	VID_PXL_CRC_ERR_C	VID_PXL_CRC_ERR_B	VID_PXL_CRC_ERR_A
0x46	0xE7	PWR_STATUS_OEN[7:0]	VDDCMP_INT_OEN	RSVD	VDDBAD_INT_OEN	RSVD[4:0]				
0x47	0x00	PWR_STATUS_FLAG[7:0]	VDDCMP_INT_FLAG	RSVD	VDDBAD_INT_FLAG	–	–	–	–	–
0x48	0x05	PM_OV_STAT[7:0]	–	–	–	RSVD	RSVD[1:0]		OV_LEVEL[1:0]	

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ADDRESS	RESET	NAME	MSB							LSB
0x49	0x2F	VIDEO_MASKED_OEN[7:0]	–	–	CMP_VTERM_MASK	VDD_OV_OEN	VIDEO_MASKED_3_OEN	VIDEO_MASKED_2_OEN	VIDEO_MASKED_1_OEN	VIDEO_MASKED_0_OEN
0x4A	0x00	VIDEO_MASKED_FLAG[7:0]	–	–	CMP_VTERM_STATUS	VDD_OV_FLAG	VIDEO_MASKED_3_FLAG	VIDEO_MASKED_2_FLAG	VIDEO_MASKED_1_FLAG	VIDEO_MASKED_0_FLAG
0x4C	0x05	DEV_REV[7:0]	–	–	–	–	DEV_REV[3:0]			
CFGH_A VIDEO_X										
0x50	0x00	RX0[7:0]	–	–	–	–	–	–	STR_SEL[1:0]	
CFGH_A VIDEO_Y										
0x51	0x01	RX0[7:0]	–	–	–	–	–	–	STR_SEL[1:0]	
CFGH_A VIDEO_Z										
0x52	0x02	RX0[7:0]	–	–	–	–	–	–	STR_SEL[1:0]	
CFGH_A VIDEO_U										
0x53	0x03	RX0[7:0]	–	–	–	–	–	–	STR_SEL[1:0]	
CFGH_B VIDEO_X										
0x54	0x00	RX0[7:0]	–	–	–	–	–	–	STR_SEL_B[1:0]	
CFGH_B VIDEO_Y										
0x55	0x01	RX0[7:0]	–	–	–	–	–	–	STR_SEL_B[1:0]	
CFGH_B VIDEO_Z										
0x56	0x02	RX0[7:0]	–	–	–	–	–	–	STR_SEL_B[1:0]	
CFGH_B VIDEO_U										
0x57	0x03	RX0[7:0]	–	–	–	–	–	–	STR_SEL_B[1:0]	
CFGH_C VIDEO_X										
0x58	0x00	RX0[7:0]	–	–	–	–	–	–	STR_SEL_C[1:0]	
CFGH_C VIDEO_Y										
0x59	0x01	RX0[7:0]	–	–	–	–	–	–	STR_SEL_C[1:0]	
CFGH_C VIDEO_Z										
0x5A	0x02	RX0[7:0]	–	–	–	–	–	–	STR_SEL_C[1:0]	
CFGH_C VIDEO_U										
0x5B	0x03	RX0[7:0]	–	–	–	–	–	–	STR_SEL_C[1:0]	
CFGH_D VIDEO_X										
0x5C	0x00	RX0[7:0]	–	–	–	–	–	–	STR_SEL_D[1:0]	
CFGH_D VIDEO_Y										
0x5D	0x01	RX0[7:0]	–	–	–	–	–	–	STR_SEL_D[1:0]	
CFGH_D VIDEO_Z										
0x5E	0x02	RX0[7:0]	–	–	–	–	–	–	STR_SEL_D[1:0]	
CFGH_D VIDEO_U										
0x5F	0x03	RX0[7:0]	–	–	–	–	–	–	STR_SEL_D[1:0]	
CFGH_VIDEO_CRC										
0x60	0x00	CFGH_VIDEO_CRC0[7:0]	RX_CRC_EN_A_B[7:0]							

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ADDRESS	RESET	NAME	MSB							LSB
0x61	0x00	CFGH_VIDEO_CRC1[7:0]	RX_CRC_EN_C_D[7:0]							
CFGI_A INFOFR										
0x70	0xF0	TR0[7:0]	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		RSVD[1:0]	
0x71	0xB0	TR1[7:0]	BW_MULT[1:0]		BW_VAL[5:0]					
0x72	0x00	TR2[7:0]	–	–	–	–	–	TX_SRC_ID[2:0]		
0x73	0xFF	TR3[7:0]	RX_SRC_SEL[7:0]							
CFGI_B INFOFR										
0x74	0xF0	TR0[7:0]	TX_CRC_EN_B	RX_CRC_EN_B	RSVD[1:0]		PRIO_VAL_B[1:0]		RSVD[1:0]	
0x75	0xB0	TR1[7:0]	BW_MULT_B[1:0]		BW_VAL_B[5:0]					
0x76	0x00	TR2[7:0]	–	–	–	–	–	TX_SRC_ID_B[2:0]		
0x77	0xFF	TR3[7:0]	RX_SRC_SEL_B[7:0]							
CFGI_C INFOFR										
0x78	0xF0	TR0[7:0]	TX_CRC_EN_C	RX_CRC_EN_C	RSVD[1:0]		PRIO_VAL_C[1:0]		RSVD[1:0]	
0x79	0xB0	TR1[7:0]	BW_MULT_C[1:0]		BW_VAL_C[5:0]					
0x7A	0x00	TR2[7:0]	–	–	–	–	–	TX_SRC_ID_C[2:0]		
0x7B	0xFF	TR3[7:0]	RX_SRC_SEL_C[7:0]							
CFGI_D INFOFR										
0x7C	0xF0	TR0[7:0]	TX_CRC_EN_D	RX_CRC_EN_D	RSVD[1:0]		PRIO_VAL_D[1:0]		RSVD[1:0]	
0x7D	0xB0	TR1[7:0]	BW_MULT_D[1:0]		BW_VAL_D[5:0]					
0x7E	0x00	TR2[7:0]	–	–	–	–	–	TX_SRC_ID_D[2:0]		
0x7F	0xFF	TR3[7:0]	RX_SRC_SEL_D[7:0]							
CFGS SPI_0										
0x80	0xF0	TR0[7:0]	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0x81	0xB0	TR1[7:0]	BW_MULT[1:0]		BW_VAL[5:0]					
0x83	0x00	TR3[7:0]	–	–	–	–	–	TX_SRC_ID[2:0]		
0x84	0xFF	TR4[7:0]	RX_SRC_SEL[7:0]							
0x85	0x18	ARQ0[7:0]	–	RSVD	RSVD	ACK_SRC_ID	ARQ_EN	ARQ_EN	–	–
0x86	0x72	ARQ1[7:0]	–	MAX_RT[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
0x87	0x00	ARQ2[7:0]	MAX_RT_ERR	RT_CNT[6:0]						
CFGS SPI_1										
0x90	0xF0	TR0[7:0]	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		RSVD[1:0]	
0x91	0xB0	TR1[7:0]	BW_MULT[1:0]		BW_VAL[5:0]					
0x93	0x00	TR3[7:0]	–	–	–	–	–	TX_SRC_ID[2:0]		
0x94	0xFF	TR4[7:0]	RX_SRC_SEL[7:0]							
0x95	0x18	ARQ0[7:0]	–	RSVD	RSVD	RSVD	ARQ_EN	ARQ_EN	–	–

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ADDRESS	RESET	NAME	MSB							LSB
0x96	0x72	ARQ1[7:0]	–	MAX_RT[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
0x97	0x00	ARQ2[7:0]	MAX_RT_ERR	RT_CNT[6:0]						
CFGL_A GPIO										
0xA0	0xF0	TR0[7:0]	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		RSVD[1:0]	
0xA1	0xB0	TR1[7:0]	BW_MULT[1:0]		BW_VAL[5:0]					
0xA3	0x00	TR3[7:0]	–	–	–	–	–	TX_SRC_ID[2:0]		
0xA4	0xFF	TR4[7:0]	RX_SRC_SEL[7:0]							
0xA5	0x18	ARQ0[7:0]	–	RSVD	RSVD	RSVD	ARQ_EN	ARQ_EN	–	–
0xA6	0x72	ARQ1[7:0]	–	RSVD[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
0xA7	0x00	ARQ2[7:0]	MAX_RT_ERR	RT_CNT[6:0]						
CFGL_B GPIO										
0xA8	0xF0	TR0[7:0]	TX_CRC_EN_B	RX_CRC_EN_B	RSVD[1:0]		PRIO_VAL_B[1:0]		RSVD[1:0]	
0xA9	0xB0	TR1[7:0]	BW_MULT_B[1:0]		BW_VAL_B[5:0]					
0xAB	0x00	TR3[7:0]	–	–	–	–	–	TX_SRC_ID_B[2:0]		
0xAC	0xFF	TR4[7:0]	RX_SRC_SEL_B[7:0]							
0xAD	0x18	ARQ0[7:0]	–	RSVD	RSVD	RSVD	ARQ_EN_B	ARQ_EN	–	–
0xAE	0x72	ARQ1[7:0]	–	RSVD[2:0]			–	–	MAX_RT_ERR_OEN_B	RT_CNT_OEN_B
0xAF	0x00	ARQ2[7:0]	MAX_RT_ERR_B	RT_CNT_B[6:0]						
CFGL_C GPIO										
0xB0	0xF0	TR0[7:0]	TX_CRC_EN_C	RX_CRC_EN_C	RSVD[1:0]		PRIO_VAL_C[1:0]		RSVD[1:0]	
0xB1	0xB0	TR1[7:0]	BW_MULT_C[1:0]		BW_VAL_C[5:0]					
0xB3	0x00	TR3[7:0]	–	–	–	–	–	TX_SRC_ID_C[2:0]		
0xB4	0xFF	TR4[7:0]	RX_SRC_SEL_C[7:0]							
0xB5	0x18	ARQ0[7:0]	–	RSVD	RSVD	RSVD	ARQ_EN_C	ARQ_EN	–	–
0xB6	0x72	ARQ1[7:0]	–	RSVD[2:0]			–	–	MAX_RT_ERR_OEN_C	RT_CNT_OEN_C
0xB7	0x00	ARQ2[7:0]	MAX_RT_ERR_C	RT_CNT_C[6:0]						
CFGL_D GPIO										
0xB8	0xF0	TR0[7:0]	TX_CRC_EN_D	RX_CRC_EN_D	RSVD[1:0]		PRIO_VAL_D[1:0]		RSVD[1:0]	
0xB9	0xB0	TR1[7:0]	BW_MULT_D[1:0]		BW_VAL_D[5:0]					
0xBB	0x00	TR3[7:0]	–	–	–	–	–	TX_SRC_ID_D[2:0]		

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ADDRESS	RESET	NAME	MSB							LSB
0xBC	0xFF	TR4[7:0]	RX_SRC_SEL_D[7:0]							
0xBD	0x18	ARQ0[7:0]	–	RSVD	RSVD	RSVD	ARQ_EN_D	ARQ_EN	–	–
0xBE	0x72	ARQ1[7:0]	–	RSVD[2:0]			–	–	MAX_RT_ERR_OEN_D	RT_CNT_OEN_D
0xBF	0x00	ARQ2[7:0]	MAX_RT_ERR_D	RT_CNT_D[6:0]						
CC										
0xC7	0x66	I2C_7[7:0]	I2C_REGSLV_1_TIMED_OUT	I2C_INTREG_SLV_1_TO[2:0]			I2C_REGSLV_0_TIMED_OUT	I2C_INTREG_SLV_0_TO[2:0]		
0xC8	0x42	UART_0[7:0]	RSVD[1:0]		REM_MS_EN_0	LOC_MS_EN_0	BYPASS_DIS_PAR_0	BYPASS_TO_0[1:0]		BYPASS_EN_0
0xC9	0x96	UART_1[7:0]	BITLEN_LSB_0[7:0]							
0xCA	0x80	UART_2[7:0]	OUT_DELAY_0[1:0]		BITLEN_MSB_0[5:0]					
0xCB	0x42	UART_3[7:0]	ARB_TO_LEN_1[1:0]		REM_MS_EN_1	LOC_MS_EN_1	BYPASS_DIS_PAR_1	BYPASS_TO_1[1:0]		BYPASS_EN_1
0xCC	0x96	UART_4[7:0]	BITLEN_LSB_1[7:0]							
0xCD	0x80	UART_5[7:0]	OUT_DELAY_1[1:0]		BITLEN_MSB_1[5:0]					
0xCE	0x04	UART_6[7:0]	UART_2_LINK_SELECT[1:0]		GMSL1_UART_ARB_TO	GMSL1_UART_ARB_EN	UART_1_LINK_SELECT[1:0]		UART_0_LINK_SELECT[1:0]	
0xD0	0x00	UART_7[7:0]	–	–	UART_2_TX_OVERFLOW	UART_2_RX_OVERFLOW	UART_1_TX_OVERFLOW	UART_1_RX_OVERFLOW	UART_0_TX_OVERFLOW	UART_0_RX_OVERFLOW
0xD1	0x42	UART_8[7:0]	RSVD[1:0]		REM_MS_EN_2	LOC_MS_EN_2	BYPASS_DIS_PAR_2	BYPASS_TO_2[1:0]		BYPASS_EN_2
0xD2	0x96	UART_9[7:0]	BITLEN_LSB_2[7:0]							
0xD3	0x80	UART_10[7:0]	OUT_DELAY_2[1:0]		BITLEN_MSB_2[5:0]					
0xD4	0x06	I2C_8[7:0]	–	–	–	–	I2C_REGSLV_2_TIMED_OUT	I2C_INTREG_SLV_2_TO[2:0]		
LINE_FAULT										
0xE0	0x00	REG0[7:0]	PU_LF7	PU_LF6	PU_LF5	PU_LF4	PU_LF3	PU_LF2	PU_LF1	PU_LF0
0xE1	0x22	REG1[7:0]	–	LF_1[2:0]			–	LF_0[2:0]		
0xE2	0x22	REG2[7:0]	–	LF_3[2:0]			–	LF_2[2:0]		
0xE3	0x22	REG3[7:0]	–	LF_5[2:0]			–	LF_4[2:0]		
0xE4	0x22	REG4[7:0]	–	LF_7[2:0]			–	LF_6[2:0]		
0xE5	0x00	REG5[7:0]	LFLT_INT_FLAG[7:0]							
0xE6	0x00	REG6[7:0]	MASK_LF7	MASK_LF6	MASK_LF5	MASK_LF4	MASK_LF3	MASK_LF2	MASK_LF1	MASK_LF0

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ADDRESS	RESET	NAME	MSB							LSB
VIDEO_PIPE_SEL										
0xF0	0x62	VIDEO_PIPE_SEL_0[7:0]	VIDEO_PIPE_SEL_1[3:0]				VIDEO_PIPE_SEL_0[3:0]			
0xF1	0xEA	VIDEO_PIPE_SEL_1[7:0]	VIDEO_PIPE_SEL_3[3:0]				VIDEO_PIPE_SEL_2[3:0]			
0xF2	0x40	VIDEO_PIPE_SEL_2[7:0]	VIDEO_PIPE_SEL_5[3:0]				VIDEO_PIPE_SEL_4[3:0]			
0xF3	0xC8	VIDEO_PIPE_SEL_3[7:0]	VIDEO_PIPE_SEL_7[3:0]				VIDEO_PIPE_SEL_6[3:0]			
0xF4	0x0F	VIDEO_PIPE_EN[7:0]	VIDEO_PIPE_EN[7:0]							
HVD_GPIO_CTRL										
0xFA	0x00	HVD_GPIO_CTRL_0[7:0]	–	DE_EN	HS_EN	VS_EN	–	HVD_SEL[2:0]		
VID_RX 0										
0x100	0x32	VIDEO_RX0[7:0]	LCRC_ERR	RSVD	RSVD	SEQ_MISS_EN	RSVD	RSVD	LINE_CRC_EN	DIS_PKT_DET
0x103	0x40	VIDEO_RX3[7:0]	–	HD_TR_MODE	DLOCKED	VLOCKED	HLOCKED	DTRACKEN	VTRACKEN	HTRACKEN
0x106	0x02	VIDEO_RX6[7:0]	RSVD[2:0]			–	LIM_HEART	–	RSVD	RSVD
0x108	0x02	VIDEO_RX8[7:0]	VID_BLK_LEN_ERR	VID_LOCK	VID_PKT_DET	VID_SEQ_ERR	RSVD[3:0]			
0x10A	0x00	VIDEO_RX10[7:0]	–	MASK_VIDEO_DE	RSVD[5:0]					
VID_RX 1										
0x112	0x32	VIDEO_RX0[7:0]	LCRC_ERR	RSVD	RSVD	SEQ_MISS_EN	RSVD	RSVD	LINE_CRC_EN	DIS_PKT_DET
0x115	0x40	VIDEO_RX3[7:0]	–	HD_TR_MODE	DLOCKED	VLOCKED	HLOCKED	DTRACKEN	VTRACKEN	HTRACKEN
0x118	0x02	VIDEO_RX6[7:0]	RSVD[2:0]			–	LIM_HEART	–	RSVD	RSVD
0x11A	0x02	VIDEO_RX8[7:0]	VID_BLK_LEN_ERR	VID_LOCK	VID_PKT_DET	VID_SEQ_ERR	RSVD[3:0]			
0x11C	0x00	VIDEO_RX10[7:0]	–	MASK_VIDEO_DE	RSVD[5:0]					
VID_RX 2										
0x124	0x32	VIDEO_RX0[7:0]	LCRC_ERR	RSVD	RSVD	SEQ_MISS_EN	RSVD	RSVD	LINE_CRC_EN	DIS_PKT_DET
0x127	0x40	VIDEO_RX3[7:0]	–	HD_TR_MODE	DLOCKED	VLOCKED	HLOCKED	DTRACKEN	VTRACKEN	HTRACKEN
0x12A	0x02	VIDEO_RX6[7:0]	RSVD[2:0]			–	LIM_HEART	–	RSVD	RSVD
0x12C	0x02	VIDEO_RX8[7:0]	VID_BLK_LEN_ERR	VID_LOCK	VID_PKT_DET	VID_SEQ_ERR	RSVD[3:0]			

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ADDRESS	RESET	NAME	MSB							LSB
0x12E	0x00	VIDEO_RX10[7:0]	–	MASK_VIDEO_DE	RSVD[5:0]					
VID_RX 3										
0x136	0x32	VIDEO_RX0[7:0]	LCRC_ERR	RSVD	RSVD	SEQ_MISS_EN	RSVD	RSVD	LINE_CRC_EN	DIS_PKT_DET
0x139	0x40	VIDEO_RX3[7:0]	–	HD_TR_MODE	DLOCKED	VLOCKED	HLOCKED	DTRACKEN	VTRACKEN	HTRACKEN
0x13C	0x02	VIDEO_RX6[7:0]	RSVD[2:0]			–	LIM_HEART	–	RSVD	RSVD
0x13E	0x02	VIDEO_RX8[7:0]	VID_BLK_LEN_ERR	VID_LOCK	VID_PKT_DET	VID_SEQ_ERR	RSVD[3:0]			
0x140	0x00	VIDEO_RX10[7:0]	–	MASK_VIDEO_DE	RSVD[5:0]					
VID_RX 4										
0x148	0x32	VIDEO_RX0[7:0]	LCRC_ERR	RSVD	RSVD	SEQ_MISS_EN	RSVD	RSVD	LINE_CRC_EN	DIS_PKT_DET
0x14B	0x40	VIDEO_RX3[7:0]	–	HD_TR_MODE	DLOCKED	VLOCKED	HLOCKED	DTRACKEN	VTRACKEN	HTRACKEN
0x14E	0x02	VIDEO_RX6[7:0]	RSVD[2:0]			–	LIM_HEART	–	RSVD	RSVD
0x150	0x02	VIDEO_RX8[7:0]	VID_BLK_LEN_ERR	VID_LOCK	VID_PKT_DET	VID_SEQ_ERR	RSVD[3:0]			
0x152	0x00	VIDEO_RX10[7:0]	–	MASK_VIDEO_DE	RSVD[5:0]					
VID_RX 5										
0x160	0x32	VIDEO_RX0[7:0]	LCRC_ERR	RSVD	RSVD	SEQ_MISS_EN	RSVD	RSVD	LINE_CRC_EN	DIS_PKT_DET
0x163	0x40	VIDEO_RX3[7:0]	–	HD_TR_MODE	DLOCKED	VLOCKED	HLOCKED	DTRACKEN	VTRACKEN	HTRACKEN
0x166	0x02	VIDEO_RX6[7:0]	RSVD[2:0]			–	LIM_HEART	–	RSVD	RSVD
0x168	0x02	VIDEO_RX8[7:0]	VID_BLK_LEN_ERR	VID_LOCK	VID_PKT_DET	VID_SEQ_ERR	RSVD[3:0]			
0x16A	0x00	VIDEO_RX10[7:0]	–	MASK_VIDEO_DE	RSVD[5:0]					
VID_RX 6										
0x172	0x32	VIDEO_RX0[7:0]	LCRC_ERR	RSVD	RSVD	SEQ_MISS_EN	RSVD	RSVD	LINE_CRC_EN	DIS_PKT_DET
0x175	0x40	VIDEO_RX3[7:0]	–	HD_TR_MODE	DLOCKED	VLOCKED	HLOCKED	DTRACKEN	VTRACKEN	HTRACKEN
0x178	0x02	VIDEO_RX6[7:0]	RSVD[2:0]			–	LIM_HEART	–	RSVD	RSVD

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ADDRESS	RESET	NAME	MSB							LSB
0x17A	0x02	VIDEO_RX8[7:0]	VID_BLK_LEN_ERR	VID_LOCK	VID_PKT_DET	VID_SEQ_ERR	RSVD[3:0]			
0x17C	0x00	VIDEO_RX10[7:0]	–	MASK_VIDEO_DE	RSVD[5:0]					
VID_RX 7										
0x184	0x32	VIDEO_RX0[7:0]	LCRC_ERR	RSVD	RSVD	SEQ_MISS_EN	RSVD	RSVD	LINE_CRC_EN	DIS_PKT_DET
0x187	0x40	VIDEO_RX3[7:0]	–	HD_TR_MODE	DLOCKED	VLOCKED	HLOCKED	DTRACKEN	VTRACKEN	HTRACKEN
0x18A	0x02	VIDEO_RX6[7:0]	RSVD[2:0]			–	LIM_HEART	–	RSVD	RSVD
0x18C	0x02	VIDEO_RX8[7:0]	VID_BLK_LEN_ERR	VID_LOCK	VID_PKT_DET	VID_SEQ_ERR	RSVD[3:0]			
0x18E	0x00	VIDEO_RX10[7:0]	–	MASK_VIDEO_DE	RSVD[5:0]					
VRX__0 0										
0x1C0	0x00	CROSS_0[7:0]	–	CROSS0_I	CROSS0_F	CROSS0[4:0]				
0x1C1	0x01	CROSS_1[7:0]	–	CROSS1_I	CROSS1_F	CROSS1[4:0]				
0x1C2	0x02	CROSS_2[7:0]	–	CROSS2_I	CROSS2_F	CROSS2[4:0]				
0x1C3	0x03	CROSS_3[7:0]	–	CROSS3_I	CROSS3_F	CROSS3[4:0]				
0x1C4	0x04	CROSS_4[7:0]	–	CROSS4_I	CROSS4_F	CROSS4[4:0]				
0x1C5	0x05	CROSS_5[7:0]	–	CROSS5_I	CROSS5_F	CROSS5[4:0]				
0x1C6	0x06	CROSS_6[7:0]	–	CROSS6_I	CROSS6_F	CROSS6[4:0]				
0x1C7	0x07	CROSS_7[7:0]	–	CROSS7_I	CROSS7_F	CROSS7[4:0]				
0x1C8	0x08	CROSS_8[7:0]	–	CROSS8_I	CROSS8_F	CROSS8[4:0]				
0x1C9	0x09	CROSS_9[7:0]	–	CROSS9_I	CROSS9_F	CROSS9[4:0]				
0x1CA	0x0A	CROSS_10[7:0]	–	CROSS10_I	CROSS10_F	CROSS10[4:0]				
0x1CB	0x0B	CROSS_11[7:0]	–	CROSS11_I	CROSS11_F	CROSS11[4:0]				
0x1CC	0x0C	CROSS_12[7:0]	–	CROSS12_I	CROSS12_F	CROSS12[4:0]				
0x1CD	0x0D	CROSS_13[7:0]	–	CROSS13_I	CROSS13_F	CROSS13[4:0]				
0x1CE	0x0E	CROSS_14[7:0]	–	CROSS14_I	CROSS14_F	CROSS14[4:0]				

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ADDRESS	RESET	NAME	MSB							LSB
0x1CF	0x0F	CROSS_15[7:0]	–	CROSS15_I	CROSS15_F	CROSS15[4:0]				
0x1D0	0x10	CROSS_16[7:0]	–	CROSS16_I	CROSS16_F	CROSS16[4:0]				
0x1D1	0x11	CROSS_17[7:0]	–	CROSS17_I	CROSS17_F	CROSS17[4:0]				
0x1D2	0x12	CROSS_18[7:0]	–	CROSS18_I	CROSS18_F	CROSS18[4:0]				
0x1D3	0x13	CROSS_19[7:0]	–	CROSS19_I	CROSS19_F	CROSS19[4:0]				
0x1D4	0x14	CROSS_20[7:0]	–	CROSS20_I	CROSS20_F	CROSS20[4:0]				
0x1D5	0x15	CROSS_21[7:0]	–	CROSS21_I	CROSS21_F	CROSS21[4:0]				
0x1D6	0x16	CROSS_22[7:0]	–	CROSS22_I	CROSS22_F	CROSS22[4:0]				
0x1D7	0x17	CROSS_23[7:0]	–	CROSS23_I	CROSS23_F	CROSS23[4:0]				
0x1D8	0x18	CROSS_HS[7:0]	–	CROSS_HS_I	CROSS_HS_F	CROSS_HS[4:0]				
0x1D9	0x19	CROSS_VS[7:0]	–	CROSS_VS_I	CROSS_VS_F	CROSS_VS[4:0]				
0x1DA	0x1A	CROSS_DE[7:0]	–	CROSS_DE_I	CROSS_DE_F	CROSS_DE[4:0]				
0x1DB	0x00	PRBS_ERR[7:0]	VPRBS_ERR[7:0]							
0x1DC	0x80	VPRBS[7:0]	PATGEN_CLK_SRC	–	RSVD	VPRBS24_GENCHK_EN	VPRBS7_GENCHK_EN	VPRBS9_GENCHK_EN	DIS_GLITCH_FILT	VIDEO_LOCK
0x1DD	0x1B	CROSS_27[7:0]	ALT_CROSSBAR	CROSS27_I	CROSS27_F	CROSS27[4:0]				
0x1DE	0x1C	CROSS_28[7:0]	–	CROSS28_I	CROSS28_F	CROSS28[4:0]				
0x1DF	0x1D	CROSS_29[7:0]	–	CROSS29_I	CROSS29_F	CROSS29[4:0]				
VRX__0 1										
0x1E0	0x00	CROSS_0[7:0]	–	CROSS0_I	CROSS0_F	CROSS0[4:0]				
0x1E1	0x01	CROSS_1[7:0]	–	CROSS1_I	CROSS1_F	CROSS1[4:0]				
0x1E2	0x02	CROSS_2[7:0]	–	CROSS2_I	CROSS2_F	CROSS2[4:0]				
0x1E3	0x03	CROSS_3[7:0]	–	CROSS3_I	CROSS3_F	CROSS3[4:0]				
0x1E4	0x04	CROSS_4[7:0]	–	CROSS4_I	CROSS4_F	CROSS4[4:0]				
0x1E5	0x05	CROSS_5[7:0]	–	CROSS5_I	CROSS5_F	CROSS5[4:0]				
0x1E6	0x06	CROSS_6[7:0]	–	CROSS6_I	CROSS6_F	CROSS6[4:0]				

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ADDRESS	RESET	NAME	MSB							LSB
0x1E7	0x07	CROSS_7[7:0]	–	CROSS7_I	CROSS7_F	CROSS7[4:0]				
0x1E8	0x08	CROSS_8[7:0]	–	CROSS8_I	CROSS8_F	CROSS8[4:0]				
0x1E9	0x09	CROSS_9[7:0]	–	CROSS9_I	CROSS9_F	CROSS9[4:0]				
0x1EA	0x0A	CROSS_10[7:0]	–	CROSS10_I	CROSS10_F	CROSS10[4:0]				
0x1EB	0x0B	CROSS_11[7:0]	–	CROSS11_I	CROSS11_F	CROSS11[4:0]				
0x1EC	0x0C	CROSS_12[7:0]	–	CROSS12_I	CROSS12_F	CROSS12[4:0]				
0x1ED	0x0D	CROSS_13[7:0]	–	CROSS13_I	CROSS13_F	CROSS13[4:0]				
0x1EE	0x0E	CROSS_14[7:0]	–	CROSS14_I	CROSS14_F	CROSS14[4:0]				
0x1EF	0x0F	CROSS_15[7:0]	–	CROSS15_I	CROSS15_F	CROSS15[4:0]				
0x1F0	0x10	CROSS_16[7:0]	–	CROSS16_I	CROSS16_F	CROSS16[4:0]				
0x1F1	0x11	CROSS_17[7:0]	–	CROSS17_I	CROSS17_F	CROSS17[4:0]				
0x1F2	0x12	CROSS_18[7:0]	–	CROSS18_I	CROSS18_F	CROSS18[4:0]				
0x1F3	0x13	CROSS_19[7:0]	–	CROSS19_I	CROSS19_F	CROSS19[4:0]				
0x1F4	0x14	CROSS_20[7:0]	–	CROSS20_I	CROSS20_F	CROSS20[4:0]				
0x1F5	0x15	CROSS_21[7:0]	–	CROSS21_I	CROSS21_F	CROSS21[4:0]				
0x1F6	0x16	CROSS_22[7:0]	–	CROSS22_I	CROSS22_F	CROSS22[4:0]				
0x1F7	0x17	CROSS_23[7:0]	–	CROSS23_I	CROSS23_F	CROSS23[4:0]				
0x1F8	0x18	CROSS_HS[7:0]	–	CROSS_HS_I	CROSS_HS_F	CROSS_HS[4:0]				
0x1F9	0x19	CROSS_VS[7:0]	–	CROSS_VS_I	CROSS_VS_F	CROSS_VS[4:0]				
0x1FA	0x1A	CROSS_DE[7:0]	–	CROSS_DE_I	CROSS_DE_F	CROSS_DE[4:0]				
0x1FB	0x00	PRBS_ERR[7:0]	VPRBS_ERR[7:0]							
0x1FC	0x80	VPRBS[7:0]	PATGEN_CLK_SRC	–	RSVD	VPRBS24_GENCHK_EN	VPRBS7_GENCHK_EN	VPRBS9_GENCHK_EN	DIS_GLITCH_FILT	VIDEO_LOCK
0x1FD	0x1B	CROSS_27[7:0]	ALT_CROSSBAR	CROSS27_I	CROSS27_F	CROSS27[4:0]				
0x1FE	0x1C	CROSS_28[7:0]	–	CROSS28_I	CROSS28_F	CROSS28[4:0]				

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ADDRESS	RESET	NAME	MSB							LSB
0x1FF	0x1D	CROSS_29[7:0]	–	CROSS29_I	CROSS29_F	CROSS29[4:0]				
VRX__0 2										
0x200	0x00	CROSS_0[7:0]	–	CROSS0_I	CROSS0_F	CROSS0[4:0]				
0x201	0x01	CROSS_1[7:0]	–	CROSS1_I	CROSS1_F	CROSS1[4:0]				
0x202	0x02	CROSS_2[7:0]	–	CROSS2_I	CROSS2_F	CROSS2[4:0]				
0x203	0x03	CROSS_3[7:0]	–	CROSS3_I	CROSS3_F	CROSS3[4:0]				
0x204	0x04	CROSS_4[7:0]	–	CROSS4_I	CROSS4_F	CROSS4[4:0]				
0x205	0x05	CROSS_5[7:0]	–	CROSS5_I	CROSS5_F	CROSS5[4:0]				
0x206	0x06	CROSS_6[7:0]	–	CROSS6_I	CROSS6_F	CROSS6[4:0]				
0x207	0x07	CROSS_7[7:0]	–	CROSS7_I	CROSS7_F	CROSS7[4:0]				
0x208	0x08	CROSS_8[7:0]	–	CROSS8_I	CROSS8_F	CROSS8[4:0]				
0x209	0x09	CROSS_9[7:0]	–	CROSS9_I	CROSS9_F	CROSS9[4:0]				
0x20A	0x0A	CROSS_10[7:0]	–	CROSS10_I	CROSS10_F	CROSS10[4:0]				
0x20B	0x0B	CROSS_11[7:0]	–	CROSS11_I	CROSS11_F	CROSS11[4:0]				
0x20C	0x0C	CROSS_12[7:0]	–	CROSS12_I	CROSS12_F	CROSS12[4:0]				
0x20D	0x0D	CROSS_13[7:0]	–	CROSS13_I	CROSS13_F	CROSS13[4:0]				
0x20E	0x0E	CROSS_14[7:0]	–	CROSS14_I	CROSS14_F	CROSS14[4:0]				
0x20F	0x0F	CROSS_15[7:0]	–	CROSS15_I	CROSS15_F	CROSS15[4:0]				
0x210	0x10	CROSS_16[7:0]	–	CROSS16_I	CROSS16_F	CROSS16[4:0]				
0x211	0x11	CROSS_17[7:0]	–	CROSS17_I	CROSS17_F	CROSS17[4:0]				
0x212	0x12	CROSS_18[7:0]	–	CROSS18_I	CROSS18_F	CROSS18[4:0]				
0x213	0x13	CROSS_19[7:0]	–	CROSS19_I	CROSS19_F	CROSS19[4:0]				
0x214	0x14	CROSS_20[7:0]	–	CROSS20_I	CROSS20_F	CROSS20[4:0]				
0x215	0x15	CROSS_21[7:0]	–	CROSS21_I	CROSS21_F	CROSS21[4:0]				
0x216	0x16	CROSS_22[7:0]	–	CROSS22_I	CROSS22_F	CROSS22[4:0]				

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ADDRESS	RESET	NAME	MSB							LSB
0x217	0x17	CROSS_23[7:0]	–	CROSS23_I	CROSS23_F	CROSS23[4:0]				
0x218	0x18	CROSS_HS[7:0]	–	CROSS_HS_I	CROSS_HS_F	CROSS_HS[4:0]				
0x219	0x19	CROSS_VS[7:0]	–	CROSS_VS_I	CROSS_VS_F	CROSS_VS[4:0]				
0x21A	0x1A	CROSS_DE[7:0]	–	CROSS_DE_I	CROSS_DE_F	CROSS_DE[4:0]				
0x21B	0x00	PRBS_ERR[7:0]	VPRBS_ERR[7:0]							
0x21C	0x80	VPRBS[7:0]	PATGEN_CLK_SRC	–	RSVD	VPRBS24_GENCHK_EN	VPRBS7_GENCHK_EN	VPRBS9_GENCHK_EN	DIS_GLITCH_FILT	VIDEO_LOCK
0x21D	0x1B	CROSS_27[7:0]	ALT_CROSSBAR	CROSS27_I	CROSS27_F	CROSS27[4:0]				
0x21E	0x1C	CROSS_28[7:0]	–	CROSS28_I	CROSS28_F	CROSS28[4:0]				
0x21F	0x1D	CROSS_29[7:0]	–	CROSS29_I	CROSS29_F	CROSS29[4:0]				
VRX__0 3										
0x220	0x00	CROSS_0[7:0]	–	CROSS0_I	CROSS0_F	CROSS0[4:0]				
0x221	0x01	CROSS_1[7:0]	–	CROSS1_I	CROSS1_F	CROSS1[4:0]				
0x222	0x02	CROSS_2[7:0]	–	CROSS2_I	CROSS2_F	CROSS2[4:0]				
0x223	0x03	CROSS_3[7:0]	–	CROSS3_I	CROSS3_F	CROSS3[4:0]				
0x224	0x04	CROSS_4[7:0]	–	CROSS4_I	CROSS4_F	CROSS4[4:0]				
0x225	0x05	CROSS_5[7:0]	–	CROSS5_I	CROSS5_F	CROSS5[4:0]				
0x226	0x06	CROSS_6[7:0]	–	CROSS6_I	CROSS6_F	CROSS6[4:0]				
0x227	0x07	CROSS_7[7:0]	–	CROSS7_I	CROSS7_F	CROSS7[4:0]				
0x228	0x08	CROSS_8[7:0]	–	CROSS8_I	CROSS8_F	CROSS8[4:0]				
0x229	0x09	CROSS_9[7:0]	–	CROSS9_I	CROSS9_F	CROSS9[4:0]				
0x22A	0x0A	CROSS_10[7:0]	–	CROSS10_I	CROSS10_F	CROSS10[4:0]				
0x22B	0x0B	CROSS_11[7:0]	–	CROSS11_I	CROSS11_F	CROSS11[4:0]				
0x22C	0x0C	CROSS_12[7:0]	–	CROSS12_I	CROSS12_F	CROSS12[4:0]				
0x22D	0x0D	CROSS_13[7:0]	–	CROSS13_I	CROSS13_F	CROSS13[4:0]				
0x22E	0x0E	CROSS_14[7:0]	–	CROSS14_I	CROSS14_F	CROSS14[4:0]				

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ADDRESS	RESET	NAME	MSB							LSB
0x22F	0x0F	CROSS_15[7:0]	–	CROSS15_I	CROSS15_F	CROSS15[4:0]				
0x230	0x10	CROSS_16[7:0]	–	CROSS16_I	CROSS16_F	CROSS16[4:0]				
0x231	0x11	CROSS_17[7:0]	–	CROSS17_I	CROSS17_F	CROSS17[4:0]				
0x232	0x12	CROSS_18[7:0]	–	CROSS18_I	CROSS18_F	CROSS18[4:0]				
0x233	0x13	CROSS_19[7:0]	–	CROSS19_I	CROSS19_F	CROSS19[4:0]				
0x234	0x14	CROSS_20[7:0]	–	CROSS20_I	CROSS20_F	CROSS20[4:0]				
0x235	0x15	CROSS_21[7:0]	–	CROSS21_I	CROSS21_F	CROSS21[4:0]				
0x236	0x16	CROSS_22[7:0]	–	CROSS22_I	CROSS22_F	CROSS22[4:0]				
0x237	0x17	CROSS_23[7:0]	–	CROSS23_I	CROSS23_F	CROSS23[4:0]				
0x238	0x18	CROSS_HS[7:0]	–	CROSS_HS_I	CROSS_HS_F	CROSS_HS[4:0]				
0x239	0x19	CROSS_VS[7:0]	–	CROSS_VS_I	CROSS_VS_F	CROSS_VS[4:0]				
0x23A	0x1A	CROSS_DE[7:0]	–	CROSS_DE_I	CROSS_DE_F	CROSS_DE[4:0]				
0x23B	0x00	PRBS_ERR[7:0]	VPRBS_ERR[7:0]							
0x23C	0x80	VPRBS[7:0]	PATGEN_CLK_SRC	–	RSVD	VPRBS24_GENCHK_EN	VPRBS7_GENCHK_EN	VPRBS9_GENCHK_EN	DIS_GLITCH_FILT	VIDEO_LOCK
0x23D	0x1B	CROSS_27[7:0]	ALT_CROSSBAR	CROSS27_I	CROSS27_F	CROSS27[4:0]				
0x23E	0x1C	CROSS_28[7:0]	–	CROSS28_I	CROSS28_F	CROSS28[4:0]				
0x23F	0x1D	CROSS_29[7:0]	–	CROSS29_I	CROSS29_F	CROSS29[4:0]				
VRX__0 4										
0x240	0x00	CROSS_0[7:0]	–	CROSS0_I	CROSS0_F	CROSS0[4:0]				
0x241	0x01	CROSS_1[7:0]	–	CROSS1_I	CROSS1_F	CROSS1[4:0]				
0x242	0x02	CROSS_2[7:0]	–	CROSS2_I	CROSS2_F	CROSS2[4:0]				
0x243	0x03	CROSS_3[7:0]	–	CROSS3_I	CROSS3_F	CROSS3[4:0]				
0x244	0x04	CROSS_4[7:0]	–	CROSS4_I	CROSS4_F	CROSS4[4:0]				
0x245	0x05	CROSS_5[7:0]	–	CROSS5_I	CROSS5_F	CROSS5[4:0]				
0x246	0x06	CROSS_6[7:0]	–	CROSS6_I	CROSS6_F	CROSS6[4:0]				

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ADDRESS	RESET	NAME	MSB							LSB
0x247	0x07	CROSS_7[7:0]	–	CROSS7_I	CROSS7_F	CROSS7[4:0]				
0x248	0x08	CROSS_8[7:0]	–	CROSS8_I	CROSS8_F	CROSS8[4:0]				
0x249	0x09	CROSS_9[7:0]	–	CROSS9_I	CROSS9_F	CROSS9[4:0]				
0x24A	0x0A	CROSS_10[7:0]	–	CROSS10_I	CROSS10_F	CROSS10[4:0]				
0x24B	0x0B	CROSS_11[7:0]	–	CROSS11_I	CROSS11_F	CROSS11[4:0]				
0x24C	0x0C	CROSS_12[7:0]	–	CROSS12_I	CROSS12_F	CROSS12[4:0]				
0x24D	0x0D	CROSS_13[7:0]	–	CROSS13_I	CROSS13_F	CROSS13[4:0]				
0x24E	0x0E	CROSS_14[7:0]	–	CROSS14_I	CROSS14_F	CROSS14[4:0]				
0x24F	0x0F	CROSS_15[7:0]	–	CROSS15_I	CROSS15_F	CROSS15[4:0]				
0x250	0x10	CROSS_16[7:0]	–	CROSS16_I	CROSS16_F	CROSS16[4:0]				
0x251	0x11	CROSS_17[7:0]	–	CROSS17_I	CROSS17_F	CROSS17[4:0]				
0x252	0x12	CROSS_18[7:0]	–	CROSS18_I	CROSS18_F	CROSS18[4:0]				
0x253	0x13	CROSS_19[7:0]	–	CROSS19_I	CROSS19_F	CROSS19[4:0]				
0x254	0x14	CROSS_20[7:0]	–	CROSS20_I	CROSS20_F	CROSS20[4:0]				
0x255	0x15	CROSS_21[7:0]	–	CROSS21_I	CROSS21_F	CROSS21[4:0]				
0x256	0x16	CROSS_22[7:0]	–	CROSS22_I	CROSS22_F	CROSS22[4:0]				
0x257	0x17	CROSS_23[7:0]	–	CROSS23_I	CROSS23_F	CROSS23[4:0]				
0x258	0x18	CROSS_HS[7:0]	–	CROSS_HS_I	CROSS_HS_F	CROSS_HS[4:0]				
0x259	0x19	CROSS_VS[7:0]	–	CROSS_VS_I	CROSS_VS_F	CROSS_VS[4:0]				
0x25A	0x1A	CROSS_DE[7:0]	–	CROSS_DE_I	CROSS_DE_F	CROSS_DE[4:0]				
0x25B	0x00	PRBS_ERR[7:0]	VPRBS_ERR[7:0]							
0x25C	0x80	VPRBS[7:0]	PATGEN_CLK_SRC	–	RSVD	VPRBS24_GENCHK_EN	VPRBS7_GENCHK_EN	VPRBS9_GENCHK_EN	DIS_GLITCH_FILT	VIDEO_LOCK
0x25D	0x1B	CROSS_27[7:0]	ALT_CROSSBAR	CROSS27_I	CROSS27_F	CROSS27[4:0]				
0x25E	0x1C	CROSS_28[7:0]	–	CROSS28_I	CROSS28_F	CROSS28[4:0]				

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ADDRESS	RESET	NAME	MSB							LSB
0x25F	0x1D	CROSS_29[7:0]	–	CROSS29_I	CROSS29_F	CROSS29[4:0]				
VRX__0 5										
0x260	0x00	CROSS_0[7:0]	–	CROSS0_I	CROSS0_F	CROSS0[4:0]				
0x261	0x01	CROSS_1[7:0]	–	CROSS1_I	CROSS1_F	CROSS1[4:0]				
0x262	0x02	CROSS_2[7:0]	–	CROSS2_I	CROSS2_F	CROSS2[4:0]				
0x263	0x03	CROSS_3[7:0]	–	CROSS3_I	CROSS3_F	CROSS3[4:0]				
0x264	0x04	CROSS_4[7:0]	–	CROSS4_I	CROSS4_F	CROSS4[4:0]				
0x265	0x05	CROSS_5[7:0]	–	CROSS5_I	CROSS5_F	CROSS5[4:0]				
0x266	0x06	CROSS_6[7:0]	–	CROSS6_I	CROSS6_F	CROSS6[4:0]				
0x267	0x07	CROSS_7[7:0]	–	CROSS7_I	CROSS7_F	CROSS7[4:0]				
0x268	0x08	CROSS_8[7:0]	–	CROSS8_I	CROSS8_F	CROSS8[4:0]				
0x269	0x09	CROSS_9[7:0]	–	CROSS9_I	CROSS9_F	CROSS9[4:0]				
0x26A	0x0A	CROSS_10[7:0]	–	CROSS10_I	CROSS10_F	CROSS10[4:0]				
0x26B	0x0B	CROSS_11[7:0]	–	CROSS11_I	CROSS11_F	CROSS11[4:0]				
0x26C	0x0C	CROSS_12[7:0]	–	CROSS12_I	CROSS12_F	CROSS12[4:0]				
0x26D	0x0D	CROSS_13[7:0]	–	CROSS13_I	CROSS13_F	CROSS13[4:0]				
0x26E	0x0E	CROSS_14[7:0]	–	CROSS14_I	CROSS14_F	CROSS14[4:0]				
0x26F	0x0F	CROSS_15[7:0]	–	CROSS15_I	CROSS15_F	CROSS15[4:0]				
0x270	0x10	CROSS_16[7:0]	–	CROSS16_I	CROSS16_F	CROSS16[4:0]				
0x271	0x11	CROSS_17[7:0]	–	CROSS17_I	CROSS17_F	CROSS17[4:0]				
0x272	0x12	CROSS_18[7:0]	–	CROSS18_I	CROSS18_F	CROSS18[4:0]				
0x273	0x13	CROSS_19[7:0]	–	CROSS19_I	CROSS19_F	CROSS19[4:0]				
0x274	0x14	CROSS_20[7:0]	–	CROSS20_I	CROSS20_F	CROSS20[4:0]				
0x275	0x15	CROSS_21[7:0]	–	CROSS21_I	CROSS21_F	CROSS21[4:0]				
0x276	0x16	CROSS_22[7:0]	–	CROSS22_I	CROSS22_F	CROSS22[4:0]				

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ADDRESS	RESET	NAME	MSB							LSB
0x277	0x17	CROSS_23[7:0]	–	CROSS23_I	CROSS23_F	CROSS23[4:0]				
0x278	0x18	CROSS_HS[7:0]	–	CROSS_HS_I	CROSS_HS_F	CROSS_HS[4:0]				
0x279	0x19	CROSS_VS[7:0]	–	CROSS_VS_I	CROSS_VS_F	CROSS_VS[4:0]				
0x27A	0x1A	CROSS_DE[7:0]	–	CROSS_DE_I	CROSS_DE_F	CROSS_DE[4:0]				
0x27B	0x00	PRBS_ERR[7:0]	VPRBS_ERR[7:0]							
0x27C	0x80	VPRBS[7:0]	PATGEN_CLK_SRC	–	RSVD	VPRBS24_GENCHK_EN	VPRBS7_GENCHK_EN	VPRBS9_GENCHK_EN	DIS_GLITCH_FILT	VIDEO_LOCK
0x27D	0x1B	CROSS_27[7:0]	ALT_CROSSBAR	CROSS27_I	CROSS27_F	CROSS27[4:0]				
0x27E	0x1C	CROSS_28[7:0]	–	CROSS28_I	CROSS28_F	CROSS28[4:0]				
0x27F	0x1D	CROSS_29[7:0]	–	CROSS29_I	CROSS29_F	CROSS29[4:0]				
VRX__0 6										
0x280	0x00	CROSS_0[7:0]	–	CROSS0_I	CROSS0_F	CROSS0[4:0]				
0x281	0x01	CROSS_1[7:0]	–	CROSS1_I	CROSS1_F	CROSS1[4:0]				
0x282	0x02	CROSS_2[7:0]	–	CROSS2_I	CROSS2_F	CROSS2[4:0]				
0x283	0x03	CROSS_3[7:0]	–	CROSS3_I	CROSS3_F	CROSS3[4:0]				
0x284	0x04	CROSS_4[7:0]	–	CROSS4_I	CROSS4_F	CROSS4[4:0]				
0x285	0x05	CROSS_5[7:0]	–	CROSS5_I	CROSS5_F	CROSS5[4:0]				
0x286	0x06	CROSS_6[7:0]	–	CROSS6_I	CROSS6_F	CROSS6[4:0]				
0x287	0x07	CROSS_7[7:0]	–	CROSS7_I	CROSS7_F	CROSS7[4:0]				
0x288	0x08	CROSS_8[7:0]	–	CROSS8_I	CROSS8_F	CROSS8[4:0]				
0x289	0x09	CROSS_9[7:0]	–	CROSS9_I	CROSS9_F	CROSS9[4:0]				
0x28A	0x0A	CROSS_10[7:0]	–	CROSS10_I	CROSS10_F	CROSS10[4:0]				
0x28B	0x0B	CROSS_11[7:0]	–	CROSS11_I	CROSS11_F	CROSS11[4:0]				
0x28C	0x0C	CROSS_12[7:0]	–	CROSS12_I	CROSS12_F	CROSS12[4:0]				
0x28D	0x0D	CROSS_13[7:0]	–	CROSS13_I	CROSS13_F	CROSS13[4:0]				
0x28E	0x0E	CROSS_14[7:0]	–	CROSS14_I	CROSS14_F	CROSS14[4:0]				

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ADDRESS	RESET	NAME	MSB							LSB
0x28F	0x0F	CROSS_15[7:0]	–	CROSS15_I	CROSS15_F	CROSS15[4:0]				
0x290	0x10	CROSS_16[7:0]	–	CROSS16_I	CROSS16_F	CROSS16[4:0]				
0x291	0x11	CROSS_17[7:0]	–	CROSS17_I	CROSS17_F	CROSS17[4:0]				
0x292	0x12	CROSS_18[7:0]	–	CROSS18_I	CROSS18_F	CROSS18[4:0]				
0x293	0x13	CROSS_19[7:0]	–	CROSS19_I	CROSS19_F	CROSS19[4:0]				
0x294	0x14	CROSS_20[7:0]	–	CROSS20_I	CROSS20_F	CROSS20[4:0]				
0x295	0x15	CROSS_21[7:0]	–	CROSS21_I	CROSS21_F	CROSS21[4:0]				
0x296	0x16	CROSS_22[7:0]	–	CROSS22_I	CROSS22_F	CROSS22[4:0]				
0x297	0x17	CROSS_23[7:0]	–	CROSS23_I	CROSS23_F	CROSS23[4:0]				
0x298	0x18	CROSS_HS[7:0]	–	CROSS_HS_I	CROSS_HS_F	CROSS_HS[4:0]				
0x299	0x19	CROSS_VS[7:0]	–	CROSS_VS_I	CROSS_VS_F	CROSS_VS[4:0]				
0x29A	0x1A	CROSS_DE[7:0]	–	CROSS_DE_I	CROSS_DE_F	CROSS_DE[4:0]				
0x29B	0x00	PRBS_ERR[7:0]	VPRBS_ERR[7:0]							
0x29C	0x80	VPRBS[7:0]	PATGEN_CLK_SRC	–	RSVD	VPRBS24_GENCHK_EN	VPRBS7_GENCHK_EN	VPRBS9_GENCHK_EN	DIS_GLITCH_FILT	VIDEO_LOCK
0x29D	0x1B	CROSS_27[7:0]	ALT_CROSSBAR	CROSS27_I	CROSS27_F	CROSS27[4:0]				
0x29E	0x1C	CROSS_28[7:0]	–	CROSS28_I	CROSS28_F	CROSS28[4:0]				
0x29F	0x1D	CROSS_29[7:0]	–	CROSS29_I	CROSS29_F	CROSS29[4:0]				
VRX__0 7										
0x2A0	0x00	CROSS_0[7:0]	–	CROSS0_I	CROSS0_F	CROSS0[4:0]				
0x2A1	0x01	CROSS_1[7:0]	–	CROSS1_I	CROSS1_F	CROSS1[4:0]				
0x2A2	0x02	CROSS_2[7:0]	–	CROSS2_I	CROSS2_F	CROSS2[4:0]				
0x2A3	0x03	CROSS_3[7:0]	–	CROSS3_I	CROSS3_F	CROSS3[4:0]				
0x2A4	0x04	CROSS_4[7:0]	–	CROSS4_I	CROSS4_F	CROSS4[4:0]				
0x2A5	0x05	CROSS_5[7:0]	–	CROSS5_I	CROSS5_F	CROSS5[4:0]				
0x2A6	0x06	CROSS_6[7:0]	–	CROSS6_I	CROSS6_F	CROSS6[4:0]				

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ADDRESS	RESET	NAME	MSB							LSB
0x2A7	0x07	CROSS_7[7:0]	–	CROSS7_I	CROSS7_F	CROSS7[4:0]				
0x2A8	0x08	CROSS_8[7:0]	–	CROSS8_I	CROSS8_F	CROSS8[4:0]				
0x2A9	0x09	CROSS_9[7:0]	–	CROSS9_I	CROSS9_F	CROSS9[4:0]				
0x2AA	0x0A	CROSS_10[7:0]	–	CROSS10_I	CROSS10_F	CROSS10[4:0]				
0x2AB	0x0B	CROSS_11[7:0]	–	CROSS11_I	CROSS11_F	CROSS11[4:0]				
0x2AC	0x0C	CROSS_12[7:0]	–	CROSS12_I	CROSS12_F	CROSS12[4:0]				
0x2AD	0x0D	CROSS_13[7:0]	–	CROSS13_I	CROSS13_F	CROSS13[4:0]				
0x2AE	0x0E	CROSS_14[7:0]	–	CROSS14_I	CROSS14_F	CROSS14[4:0]				
0x2AF	0x0F	CROSS_15[7:0]	–	CROSS15_I	CROSS15_F	CROSS15[4:0]				
0x2B0	0x10	CROSS_16[7:0]	–	CROSS16_I	CROSS16_F	CROSS16[4:0]				
0x2B1	0x11	CROSS_17[7:0]	–	CROSS17_I	CROSS17_F	CROSS17[4:0]				
0x2B2	0x12	CROSS_18[7:0]	–	CROSS18_I	CROSS18_F	CROSS18[4:0]				
0x2B3	0x13	CROSS_19[7:0]	–	CROSS19_I	CROSS19_F	CROSS19[4:0]				
0x2B4	0x14	CROSS_20[7:0]	–	CROSS20_I	CROSS20_F	CROSS20[4:0]				
0x2B5	0x15	CROSS_21[7:0]	–	CROSS21_I	CROSS21_F	CROSS21[4:0]				
0x2B6	0x16	CROSS_22[7:0]	–	CROSS22_I	CROSS22_F	CROSS22[4:0]				
0x2B7	0x17	CROSS_23[7:0]	–	CROSS23_I	CROSS23_F	CROSS23[4:0]				
0x2B8	0x18	CROSS_HS[7:0]	–	CROSS_HS_I	CROSS_HS_F	CROSS_HS[4:0]				
0x2B9	0x19	CROSS_VS[7:0]	–	CROSS_VS_I	CROSS_VS_F	CROSS_VS[4:0]				
0x2BA	0x1A	CROSS_DE[7:0]	–	CROSS_DE_I	CROSS_DE_F	CROSS_DE[4:0]				
0x2BB	0x00	PRBS_ERR[7:0]	VPRBS_ERR[7:0]							
0x2BC	0x80	VPRBS[7:0]	PATGEN_CLK_SRC	–	RSVD	VPRBS24_GENCHK_EN	VPRBS7_GENCHK_EN	VPRBS9_GENCHK_EN	DIS_GLITCH_FILT	VIDEO_LOCK
0x2BD	0x1B	CROSS_27[7:0]	ALT_CROSSBAR	CROSS27_I	CROSS27_F	CROSS27[4:0]				
0x2BE	0x1C	CROSS_28[7:0]	–	CROSS28_I	CROSS28_F	CROSS28[4:0]				

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ADDRESS	RESET	NAME	MSB							LSB
0x2BF	0x1D	CROSS_29[7:0]	–	CROSS29_I	CROSS29_F	CROSS29[4:0]				
GPIO0 0										
0x300	0x83	GPIO_A[7:0]	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x301	0xA0	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x302	0x40	GPIO_C[7:0]	OVR_RES_CFG	RSVD	RSVD	GPIO_RX_ID[4:0]				
GPIO1 1										
0x303	0x84	GPIO_A[7:0]	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x304	0xA1	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x305	0x41	GPIO_C[7:0]	OVR_RES_CFG	RSVD	RSVD	GPIO_RX_ID[4:0]				
GPIO2 2										
0x306	0x81	GPIO_A[7:0]	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x307	0xA2	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x308	0x42	GPIO_C[7:0]	OVR_RES_CFG	RSVD	RSVD	GPIO_RX_ID[4:0]				
GPIO3 3										
0x309	0x81	GPIO_A[7:0]	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x30A	0x23	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x30B	0x43	GPIO_C[7:0]	OVR_RES_CFG	RSVD	RSVD	GPIO_RX_ID[4:0]				
GPIO4 4										
0x30C	0x81	GPIO_A[7:0]	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x30D	0xA4	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x30E	0x44	GPIO_C[7:0]	OVR_RES_CFG	RSVD	RSVD	GPIO_RX_ID[4:0]				
GPIO5 5										
0x310	0x81	GPIO_A[7:0]	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x311	0xA5	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x312	0x45	GPIO_C[7:0]	OVR_RES_CFG	RSVD	RSVD	GPIO_RX_ID[4:0]				
GPIO6 6										
0x313	0x83	GPIO_A[7:0]	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS

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ADDRESS	RESET	NAME	MSB							LSB
0x314	0xA6	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x315	0x46	GPIO_C[7:0]	OVR_RES_CFG	RSVD	RSVD	GPIO_RX_ID[4:0]				
GPIO7 7										
0x316	0x81	GPIO_A[7:0]	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x317	0xA7	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x318	0x47	GPIO_C[7:0]	OVR_RES_CFG	RSVD	RSVD	GPIO_RX_ID[4:0]				
GPIO8 8										
0x319	0x81	GPIO_A[7:0]	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x31A	0xA8	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x31B	0x48	GPIO_C[7:0]	OVR_RES_CFG	RSVD	RSVD	GPIO_RX_ID[4:0]				
GPIO9 9										
0x31C	0x81	GPIO_A[7:0]	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x31D	0xA9	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x31E	0x49	GPIO_C[7:0]	OVR_RES_CFG	RSVD	RSVD	GPIO_RX_ID[4:0]				
GPIO10 10										
0x320	0x81	GPIO_A[7:0]	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x321	0xAA	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x322	0x4A	GPIO_C[7:0]	OVR_RES_CFG	RSVD	RSVD	GPIO_RX_ID[4:0]				
GPIO11 11										
0x323	0x81	GPIO_A[7:0]	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x324	0x2B	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x325	0x4B	GPIO_C[7:0]	OVR_RES_CFG	RSVD	RSVD	GPIO_RX_ID[4:0]				
GPIO12 12										
0x326	0x81	GPIO_A[7:0]	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x327	0x2C	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x328	0x4C	GPIO_C[7:0]	OVR_RES_CFG	RSVD	RSVD	GPIO_RX_ID[4:0]				

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ADDRESS	RESET	NAME	MSB							LSB
GPIO13 13										
0x329	0x81	GPIO_A[7:0]	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x32A	0x2D	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x32B	0x4D	GPIO_C[7:0]	OVR_RES_CFG	RSVD	RSVD	GPIO_RX_ID[4:0]				
GPIO14 14										
0x32C	0x99	GPIO_A[7:0]	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x32D	0xAE	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x32E	0x4E	GPIO_C[7:0]	OVR_RES_CFG	RSVD	RSVD	GPIO_RX_ID[4:0]				
GPIO15 15										
0x330	0x19	GPIO_A[7:0]	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x331	0x0F	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]		RSVD	GPIO_TX_ID[4:0]				
0x332	0x4F	GPIO_C[7:0]	OVR_RES_CFG	RSVD	RSVD	GPIO_RX_ID[4:0]				
GPIO16 16										
0x333	0x19	GPIO_A[7:0]	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x334	0x10	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]		RSVD	GPIO_TX_ID[4:0]				
0x335	0x50	GPIO_C[7:0]	OVR_RES_CFG	RSVD	RSVD	GPIO_RX_ID[4:0]				
GPIO0_B 0										
0x337	0x00	GPIO_B[7:0]	RSVD	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
0x338	0x40	GPIO_C[7:0]	–	RSVD	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
GPIO0_B 1										
0x33A	0x01	GPIO_B[7:0]	RSVD	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
0x33B	0x41	GPIO_C[7:0]	–	RSVD	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
GPIO0_B 2										
0x33D	0x02	GPIO_B[7:0]	RSVD	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
0x33E	0x42	GPIO_C[7:0]	–	RSVD	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
GPIO0_B 3										
0x341	0x03	GPIO_B[7:0]	RSVD	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
0x342	0x43	GPIO_C[7:0]	–	RSVD	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				

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ADDRESS	RESET	NAME	MSB							LSB
GPIO0_B 4										
0x344	0x04	GPIO_B[7:0]	RSVD	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
0x345	0x44	GPIO_C[7:0]	–	RSVD	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
GPIO0_B 5										
0x347	0x05	GPIO_B[7:0]	RSVD	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
0x348	0x45	GPIO_C[7:0]	–	RSVD	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
GPIO0_B 6										
0x34A	0x06	GPIO_B[7:0]	RSVD	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
0x34B	0x46	GPIO_C[7:0]	–	RSVD	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
GPIO0_B 7										
0x34D	0x07	GPIO_B[7:0]	RSVD	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
0x34E	0x47	GPIO_C[7:0]	–	RSVD	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
GPIO0_B 8										
0x351	0x08	GPIO_B[7:0]	RSVD	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
0x352	0x48	GPIO_C[7:0]	–	RSVD	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
GPIO0_B 9										
0x354	0x09	GPIO_B[7:0]	RSVD	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
0x355	0x49	GPIO_C[7:0]	–	RSVD	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
GPIO0_B 10										
0x357	0x0A	GPIO_B[7:0]	RSVD	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
0x358	0x4A	GPIO_C[7:0]	–	RSVD	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
GPIO0_B 11										
0x35A	0x0B	GPIO_B[7:0]	RSVD	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
0x35B	0x4B	GPIO_C[7:0]	–	RSVD	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
GPIO0_B 12										
0x35D	0x0C	GPIO_B[7:0]	RSVD	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
0x35E	0x4C	GPIO_C[7:0]	–	RSVD	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
GPIO0_B 13										
0x361	0x0D	GPIO_B[7:0]	RSVD	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				

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ADDRESS	RESET	NAME	MSB							LSB
0x362	0x4D	GPIO_C[7:0]	–	RSVD	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
GPIO0_B 14										
0x364	0x0E	GPIO_B[7:0]	RSVD	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
0x365	0x4E	GPIO_C[7:0]	–	RSVD	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
GPIO0_B 15										
0x367	0x0F	GPIO_B[7:0]	RSVD	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
0x368	0x4F	GPIO_C[7:0]	–	RSVD	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
GPIO0_B 16										
0x36A	0x10	GPIO_B[7:0]	RSVD	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
0x36B	0x50	GPIO_C[7:0]	–	RSVD	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
GPIO0_C 0										
0x36D	0x00	GPIO_B[7:0]	RSVD	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
0x36E	0x40	GPIO_C[7:0]	–	RSVD	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
GPIO0_C 1										
0x371	0x01	GPIO_B[7:0]	RSVD	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
0x372	0x41	GPIO_C[7:0]	–	RSVD	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
GPIO0_C 2										
0x374	0x02	GPIO_B[7:0]	RSVD	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
0x375	0x42	GPIO_C[7:0]	–	RSVD	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
GPIO0_C 3										
0x377	0x03	GPIO_B[7:0]	RSVD	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
0x378	0x43	GPIO_C[7:0]	–	RSVD	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
GPIO0_C 4										
0x37A	0x04	GPIO_B[7:0]	RSVD	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
0x37B	0x44	GPIO_C[7:0]	–	RSVD	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
GPIO0_C 5										
0x37D	0x05	GPIO_B[7:0]	RSVD	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
0x37E	0x45	GPIO_C[7:0]	–	RSVD	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				

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ADDRESS	RESET	NAME	MSB							LSB
GPIO0_C 6										
0x381	0x06	GPIO_B[7:0]	RSVD	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
0x382	0x46	GPIO_C[7:0]	–	RSVD	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
GPIO0_C 7										
0x384	0x07	GPIO_B[7:0]	RSVD	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
0x385	0x47	GPIO_C[7:0]	–	RSVD	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
GPIO0_C 8										
0x387	0x08	GPIO_B[7:0]	RSVD	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
0x388	0x48	GPIO_C[7:0]	–	RSVD	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
GPIO0_C 9										
0x38A	0x09	GPIO_B[7:0]	RSVD	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
0x38B	0x49	GPIO_C[7:0]	–	RSVD	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
GPIO0_C 10										
0x38D	0x0A	GPIO_B[7:0]	RSVD	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
0x38E	0x4A	GPIO_C[7:0]	–	RSVD	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
GPIO0_C 11										
0x391	0x0B	GPIO_B[7:0]	RSVD	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
0x392	0x4B	GPIO_C[7:0]	–	RSVD	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
GPIO0_C 12										
0x394	0x0C	GPIO_B[7:0]	RSVD	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
0x395	0x4C	GPIO_C[7:0]	–	RSVD	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
GPIO0_C 13										
0x397	0x0D	GPIO_B[7:0]	RSVD	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
0x398	0x4D	GPIO_C[7:0]	–	RSVD	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
GPIO0_C 14										
0x39A	0x0E	GPIO_B[7:0]	RSVD	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
0x39B	0x4E	GPIO_C[7:0]	–	RSVD	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
GPIO0_C 15										
0x39D	0x0F	GPIO_B[7:0]	RSVD	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				

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ADDRESS	RESET	NAME	MSB							LSB
0x39E	0x4F	GPIO_C[7:0]	–	RSVD	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
GPIO0_C 16										
0x3A1	0x10	GPIO_B[7:0]	RSVD	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
0x3A2	0x50	GPIO_C[7:0]	–	RSVD	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
GPIO0_D 0										
0x3A4	0x00	GPIO_B[7:0]	RSVD	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
0x3A5	0x40	GPIO_C[7:0]	–	RSVD	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
GPIO0_D 1										
0x3A7	0x01	GPIO_B[7:0]	RSVD	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
0x3A8	0x41	GPIO_C[7:0]	–	RSVD	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
GPIO0_D 2										
0x3AA	0x02	GPIO_B[7:0]	RSVD	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
0x3AB	0x42	GPIO_C[7:0]	–	RSVD	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
GPIO0_D 3										
0x3AD	0x03	GPIO_B[7:0]	RSVD	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
0x3AE	0x43	GPIO_C[7:0]	–	RSVD	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
GPIO0_D 4										
0x3B1	0x04	GPIO_B[7:0]	RSVD	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
0x3B2	0x44	GPIO_C[7:0]	–	RSVD	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
GPIO0_D 5										
0x3B4	0x05	GPIO_B[7:0]	RSVD	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
0x3B5	0x45	GPIO_C[7:0]	–	RSVD	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
GPIO0_D 6										
0x3B7	0x06	GPIO_B[7:0]	RSVD	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
0x3B8	0x46	GPIO_C[7:0]	–	RSVD	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
GPIO0_D 7										
0x3BA	0x07	GPIO_B[7:0]	RSVD	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
0x3BB	0x47	GPIO_C[7:0]	–	RSVD	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				

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ADDRESS	RESET	NAME	MSB							LSB
GPIO0_D 8										
0x3BD	0x08	GPIO_B[7:0]	RSVD	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
0x3BE	0x48	GPIO_C[7:0]	–	RSVD	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
GPIO0_D 9										
0x3C1	0x09	GPIO_B[7:0]	RSVD	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
0x3C2	0x49	GPIO_C[7:0]	–	RSVD	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
GPIO0_D 10										
0x3C4	0x0A	GPIO_B[7:0]	RSVD	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
0x3C5	0x4A	GPIO_C[7:0]	–	RSVD	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
GPIO0_D 11										
0x3C7	0x0B	GPIO_B[7:0]	RSVD	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
0x3C8	0x4B	GPIO_C[7:0]	–	RSVD	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
GPIO0_D 12										
0x3CA	0x0C	GPIO_B[7:0]	RSVD	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
0x3CB	0x4C	GPIO_C[7:0]	–	RSVD	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
GPIO0_D 13										
0x3CD	0x0D	GPIO_B[7:0]	RSVD	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
0x3CE	0x4D	GPIO_C[7:0]	–	RSVD	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
GPIO0_D 14										
0x3D1	0x0E	GPIO_B[7:0]	RSVD	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
0x3D2	0x4E	GPIO_C[7:0]	–	RSVD	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
GPIO0_D 15										
0x3D4	0x0F	GPIO_B[7:0]	RSVD	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
0x3D5	0x4F	GPIO_C[7:0]	–	RSVD	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
GPIO0_D 16										
0x3D7	0x10	GPIO_B[7:0]	RSVD	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
0x3D8	0x50	GPIO_C[7:0]	–	RSVD	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
GPIO_MS_ID										
0x3F0	0x1D	MS_ID_A[7:0]	–	–	–	RX_MS_ID_A[4:0]				
0x3F1	0x1D	MS_ID_B[7:0]	–	–	–	RX_MS_ID_B[4:0]				

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ADDRESS	RESET	NAME	MSB							LSB
0x3F2	0x1D	MS_ID_C[7:0]	–	–	–	RX_MS_ID_C[4:0]				
0x3F3	0x1D	MS_ID_D[7:0]	–	–	–	RX_MS_ID_D[4:0]				
BACKTOP										
0x400	0x01	BACKTOP1[7:0]	CSIPLL3_LOCK	CSIPLL2_LOCK	CSIPLL1_LOCK	CSIPLL0_LOCK	LINE_SPL2	LINE_SPL0	RSVD	BACKTOP_EN
0x40A	0x00	BACKTOP11[7:0]	cmd_overflow3	cmd_overflow2	cmd_overflow1	cmd_overflow0	LMO_3	LMO_2	LMO_1	LMO_0
0x40B	0x02	BACKTOP12[7:0]	soft_bpp_0[4:0]					–	CSI_OUT_EN	RSVD
0x40C	0x00	BACKTOP13[7:0]	soft_vc_1[3:0]				soft_vc_0[3:0]			
0x40D	0x00	BACKTOP14[7:0]	soft_vc_3[3:0]				soft_vc_2[3:0]			
0x40E	0x00	BACKTOP15[7:0]	soft_dt_1_h[1:0]		soft_dt_0[5:0]					
0x40F	0x00	BACKTOP16[7:0]	soft_dt_2_h[3:0]				soft_dt_1_l[3:0]			
0x410	0x00	BACKTOP17[7:0]	soft_dt_3[5:0]						soft_dt_2_l[1:0]	
0x411	0x00	BACKTOP18[7:0]	soft_bpp_2_h[2:0]			soft_bpp_1[4:0]				
0x412	0x00	BACKTOP19[7:0]	–	soft_bpp_3[4:0]					soft_bpp_2_l[1:0]	
0x413	0x00	BACKTOP20[7:0]	phy0_csi_tx_dpll_fb_fraction_in_l[7:0]							
0x414	0x00	BACKTOP21[7:0]	bpp8dbl3	bpp8dbl2	bpp8dbl1	bpp8dbl0	phy0_csi_tx_dpll_fb_fraction_in_h[3:0]			
0x415	0x2F	BACKTOP22[7:0]	override_bpp_vc_dt_1	override_bpp_vc_dt_0	phy0_csi_tx_dpll_fb_fraction_predef_en	phy0_csi_tx_dpll_predef_freq[4:0]				
0x416	0x00	BACKTOP23[7:0]	phy1_csi_tx_dpll_fb_fraction_in_l[7:0]							
0x417	0x00	BACKTOP24[7:0]	bpp8dbl3_mode	bpp8dbl2_mode	bpp8dbl1_mode	bpp8dbl0_mode	phy1_csi_tx_dpll_fb_fraction_in_h[3:0]			
0x418	0x2F	BACKTOP25[7:0]	override_bpp_vc_dt_3	override_bpp_vc_dt_2	phy1_csi_tx_dpll_fb_fraction_predef_en	phy1_csi_tx_dpll_predef_freq[4:0]				
0x419	0x00	BACKTOP26[7:0]	phy2_csi_tx_dpll_fb_fraction_in_l[7:0]							
0x41A	0x00	BACKTOP27[7:0]	yuv_8_10_mux_mode3	yuv_8_10_mux_mode2	yuv_8_10_mux_mode1	yuv_8_10_mux_mode0	phy2_csi_tx_dpll_fb_fraction_in_h[3:0]			
0x41B	0x2F	BACKTOP28[7:0]	override_bpp_vc_dt_5	override_bpp_vc_dt_4	phy2_csi_tx_dpll_fb_fraction_predef_en	phy2_csi_tx_dpll_predef_freq[4:0]				

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ADDRESS	RESET	NAME	MSB							LSB
0x41C	0x00	BACKTOP29[7:0]	phy3_csi_tx_dpll_fb_fraction_in_l[7:0]							
0x41D	0x00	BACKTOP30[7:0]	override_bpp_vc_dt_7	override_bpp_vc_dt_6	bpp10dbl3_mode	bpp10dbl3	phy3_csi_tx_dpll_fb_fraction_in_h[3:0]			
0x41E	0x2F	BACKTOP31[7:0]	bpp10dbl2_mode	bpp10dbl2	phy3_csi_tx_dpll_fb_fraction_predef_en	phy3_csi_tx_dpll_predef_freq[4:0]				
0x41F	0x00	BACKTOP32[7:0]	bpp10dbl1_mode	bpp10dbl1	bpp10dbl0_mode	bpp10dbl0	bpp12dbl3	bpp12dbl2	bpp12dbl1	bpp12dbl0
BACKTOP_1										
0x420	0x00	BACKTOP1[7:0]	–	–	–	–	LINE_SPL6	LINE_SPL4	–	–
0x429	0x00	BACKTOP10[7:0]	DE_SEL7	DE_SEL6	DE_SEL5	DE_SEL4	LS_LE_EN7	LS_LE_EN6	LS_LE_EN5	LS_LE_EN4
0x42A	0x00	BACKTOP11[7:0]	cmd_overflow7	cmd_overflow6	cmd_overflow5	cmd_overflow4	LMO_7	LMO_6	LMO_5	LMO_4
0x42B	0x00	BACKTOP12[7:0]	soft_bpp_4[4:0]					–	–	–
0x42C	0x00	BACKTOP13[7:0]	soft_vc_5[3:0]				soft_vc_4[3:0]			
0x42D	0x00	BACKTOP14[7:0]	soft_vc_7[3:0]				soft_vc_6[3:0]			
0x42E	0x00	BACKTOP15[7:0]	soft_dt_5_h[1:0]		soft_dt_4[5:0]					
0x42F	0x00	BACKTOP16[7:0]	soft_dt_6_h[3:0]				soft_dt_5_l[3:0]			
0x430	0x00	BACKTOP17[7:0]	soft_dt_7[5:0]						soft_dt_6_l[1:0]	
0x431	0x00	BACKTOP18[7:0]	soft_bpp_6_h[2:0]			soft_bpp_5[4:0]				
0x432	0x00	BACKTOP19[7:0]	–	soft_bpp_7[4:0]					soft_bpp_6_l[1:0]	
0x434	0x00	BACKTOP21[7:0]	bpp8dbl7	bpp8dbl6	bpp8dbl5	bpp8dbl4	–	–	–	–
0x435	0x01	BACKTOP22[7:0]	–	–	–	–	n_vs_block[3:0]			
0x436	0x00	BACKTOP23[7:0]	dis_vs7	dis_vs6	dis_vs5	dis_vs4	dis_vs3	dis_vs2	dis_vs1	dis_vs0
0x437	0x00	BACKTOP24[7:0]	bpp8dbl7_mode	bpp8dbl6_mode	bpp8dbl5_mode	bpp8dbl4_mode	–	–	–	–
0x438	0x00	BACKTOP25[7:0]	mem_err7	mem_err6	mem_err5	mem_err4	mem_err3	mem_err2	mem_err1	mem_err0
0x43A	0x00	BACKTOP27[7:0]	yuv_8_10_mux_mode7	yuv_8_10_mux_mode6	yuv_8_10_mux_mode5	yuv_8_10_mux_mode4	–	–	–	–
0x43D	0x00	BACKTOP30[7:0]	–	–	bpp10dbl7_mode	bpp10dbl7	–	–	–	–

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ADDRESS	RESET	NAME	MSB							LSB
0x43E	0x00	BACKTOP31[7:0]	bpp10dbl6_mode	bpp10dbl6	–	–	–	–	–	–
0x43F	0x00	BACKTOP32[7:0]	bpp10dbl5_mode	bpp10dbl5	bpp10dbl4_mode	bpp10dbl4	bpp12dbl7	bpp12dbl6	bpp12dbl5	bpp12dbl4
FSYNC										
0x4A0	0x0D	FSYNC_0[7:0]	RSVD	RSVD	FSYNC_OUT_PIN	EN_VS_GEN	FSYNC_MODE[1:0]		FSYNC_METH[1:0]	
0x4A1	0x00	FSYNC_1[7:0]	RSVD[1:0]		RSVD[1:0]		FSYNC_PER_DIV[3:0]			
0x4A2	0x81	FSYNC_2[7:0]	MST_LINK_SEL[2:0]			K_VAL_SIGN	K_VAL[3:0]			
0x4A3	0x00	FSYNC_3[7:0]	P_VAL_L[7:0]							
0x4A4	0x00	FSYNC_4[7:0]	–	–	P_VAL_SIGN	P_VAL_H[4:0]				
0x4A5	0x00	FSYNC_5[7:0]	FSYNC_PERIOD_L[7:0]							
0x4A6	0x00	FSYNC_6[7:0]	FSYNC_PERIOD_M[7:0]							
0x4A7	0x00	FSYNC_7[7:0]	FSYNC_PERIOD_H[7:0]							
0x4A8	0x00	FSYNC_8[7:0]	FRM_DIFF_ERR_THR_L[7:0]							
0x4A9	0x0F	FSYNC_9[7:0]	–	–	–	FRM_DIFF_ERR_THR_H[4:0]				
0x4AA	0x00	FSYNC_10[7:0]	OVLP_WINDOW_L[7:0]							
0x4AB	0x00	FSYNC_11[7:0]	EN_FSIN_LAST	–	–	OVLP_WINDOW_H[4:0]				
0x4AF	0x9F	FSYNC_15[7:0]	FS_GPIO_TYPE	FS_USE_XTAL	–	AUTO_FS_LINKS	FS_LINK_3	FS_LINK_2	FS_LINK_1	FS_LINK_0
0x4B0	0x00	FSYNC_16[7:0]	FSYNC_ERR_CNT[7:0]							
0x4B1	0xF0	FSYNC_17[7:0]	FSYNC_TX_ID[4:0]					FSYNC_ERR_THR[2:0]		
0x4B2	0x00	FSYNC_18[7:0]	CALC_FRM_LEN_L[7:0]							
0x4B3	0x00	FSYNC_19[7:0]	CALC_FRM_LEN_M[7:0]							
0x4B4	0x00	FSYNC_20[7:0]	CALC_FRM_LEN_H[7:0]							
0x4B5	0x00	FSYNC_21[7:0]	FRM_DIFF_L[7:0]							
0x4B6	0x00	FSYNC_22[7:0]	FSYNC_LOSS_OF_LOCK	FSYNC_LOCKED	FRM_DIFF_H[5:0]					
0x4B7	0x00	FSYNC_23[7:0]	RSVD	RSVD	–	–	RSVD	RSVD	RSVD	RSVD

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ADDRESS	RESET	NAME	MSB							LSB
SPI_0										
0x4E0	0x08	SPI_0[7:0]	SPI_LOC_ID[1:0]		SPI_CC_TRG_ID[1:0]		SPI_IGNR_ID	SPI_CC_EN	MST_SLVN	SPI_EN
0x4E1	0x1D	SPI_1[7:0]	SPI_LOC_N[5:0]						RSVD[1:0]	
0x4E2	0x03	SPI_2[7:0]	REQ_HOLD_OFF[2:0]			FULL_SCK_SETUP	SPI_MOD3_F	SPI_MOD3	SPIM_SS2_ACT_H	SPIM_SS1_ACT_H
0x4E3	0x00	SPI_3[7:0]	SPIM_SS_DLY_CLKS[7:0]							
0x4E4	0x00	SPI_4[7:0]	SPIM_SCK_LO_CLKS[7:0]							
0x4E5	0x00	SPI_5[7:0]	SPIM_SCK_HI_CLKS[7:0]							
0x4E6	0x00	SPI_6[7:0]	–	–	BNE	SPIS_RWN	SS_IO_EN_2	SS_IO_EN_1	BNE_IO_EN	RWN_IO_EN
0x4E7	0x00	SPI_7[7:0]	SPI_RX_OVRFLW	SPI_TX_OVRFLW	–	SPIS_BYTE_CNT[4:0]				
0x4E8	0x00	SPI_8[7:0]	REQ_HOLD_OFF_TO[7:0]							
0x4E9	0x0	SPI_9[7:0]							SPI_0_LINK_SELECT[1:0]	
SPI_1										
0x4F0	0x08	SPI_0[7:0]	SPI_LOC_ID_1[1:0]		SPI_CC_TRG_ID_1[1:0]		SPI_IGNR_ID_1	SPI_CC_EN_1	MST_SLVN_1	SPI_EN_1
0x4F1	0x1D	SPI_1[7:0]	SPI_LOC_N_1[5:0]						RSVD[1:0]	
0x4F2	0x03	SPI_2[7:0]	REQ_HOLD_OFF_1[2:0]			FULL_SCK_SETUP_1	SPI_MOD3_F_1	SPI_MOD3_1	SPIM_SS2_ACT_H_1	SPIM_SS1_ACT_H_1
0x4F3	0x00	SPI_3[7:0]	SPIM_SS_DLY_CLKS_1[7:0]							
0x4F4	0x00	SPI_4[7:0]	SPIM_SCK_LO_CLKS_1[7:0]							
0x4F5	0x00	SPI_5[7:0]	SPIM_SCK_HI_CLKS_1[7:0]							
0x4F6	0x00	SPI_6[7:0]	–	–	BNE_1	SPIS_RWN_1	SS_IO_EN_2_1	SS_IO_EN_1_1	BNE_IO_EN_1	RWN_IO_EN_1
0x4F7	0x00	SPI_7[7:0]	SPI_RX_OVRFLW_1	SPI_TX_OVRFLW_1	–	SPIS_BYTE_CNT_1[4:0]				
0x4F8	0x00	SPI_8[7:0]	REQ_HOLD_OFF_TO_1[7:0]							
0x4F9	0x1	SPI_9[7:0]							SPI_1_LINK_SELECT[1:0]	
CFGC_A CC_0										
0x500	0xF0	TR0[7:0]	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0x501	0xB0	TR1[7:0]	BW_MULT[1:0]		BW_VAL[5:0]					
0x503	0x00	TR3[7:0]	–	–	–	–	–	TX_SRC_ID[2:0]		
0x504	0xFF	TR4[7:0]	RX_SRC_SEL[7:0]							
0x505	0x18	ARQ0[7:0]	–	RSVD	RSVD	RSVD	RSVD	DIS_DBL_ACK_RETX	–	–
0x506	0x72	ARQ1[7:0]	–	RSVD[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN

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0x507	0x00	ARQ2[7:0]	MAX_RT_ERR	RT_CNT[6:0]						
CFGC_B CC_0										
0x510	0xF0	TR0[7:0]	TX_CRC_EN_B	RX_CRC_EN_B	RSVD[1:0]		PRIO_VAL_B[1:0]		PRIO_CFG_B[1:0]	
0x511	0xB0	TR1[7:0]	BW_MULT_B[1:0]		BW_VAL_B[5:0]					
0x513	0x00	TR3[7:0]	–	–	–	–	–	TX_SRC_ID_B[2:0]		
0x514	0xFF	TR4[7:0]	RX_SRC_SEL_B[7:0]							
0x515	0x18	ARQ0[7:0]	–	RSVD	RSVD	RSVD	RSVD	DIS_DBL_ACK_RETX_B	–	–
0x516	0x72	ARQ1[7:0]	–	RSVD[2:0]			–	–	MAX_RT_ERR_OEN_B	RT_CNT_OEN_B
0x517	0x00	ARQ2[7:0]	MAX_RT_ERR_B	RT_CNT_B[6:0]						
CFGC_C CC_0										
0x520	0xF0	TR0[7:0]	TX_CRC_EN_C	RX_CRC_EN_C	RSVD[1:0]		PRIO_VAL_C[1:0]		PRIO_CFG_C[1:0]	
0x521	0xB0	TR1[7:0]	BW_MULT_C[1:0]		BW_VAL_C[5:0]					
0x523	0x00	TR3[7:0]	–	–	–	–	–	TX_SRC_ID_C[2:0]		
0x524	0xFF	TR4[7:0]	RX_SRC_SEL_C[7:0]							
0x525	0x18	ARQ0[7:0]	–	RSVD	RSVD	RSVD	RSVD	DIS_DBL_ACK_RETX_C	–	–
0x526	0x72	ARQ1[7:0]	–	RSVD[2:0]			–	–	MAX_RT_ERR_OEN_C	RT_CNT_OEN_C
0x527	0x00	ARQ2[7:0]	MAX_RT_ERR_C	RT_CNT_C[6:0]						
CFGC_D CC_0										
0x530	0xF0	TR0[7:0]	TX_CRC_EN_D	RX_CRC_EN_D	RSVD[1:0]		PRIO_VAL_D[1:0]		PRIO_CFG_D[1:0]	
0x531	0xB0	TR1[7:0]	BW_MULT_D[1:0]		BW_VAL_D[5:0]					
0x533	0x00	TR3[7:0]	–	–	–	–	–	TX_SRC_ID_D[2:0]		
0x534	0xFF	TR4[7:0]	RX_SRC_SEL_D[7:0]							
0x535	0x18	ARQ0[7:0]	–	RSVD	RSVD	RSVD	RSVD	DIS_DBL_ACK_RETX_D	–	–
0x536	0x72	ARQ1[7:0]	–	RSVD[2:0]			–	–	MAX_RT_ERR_OEN_D	RT_CNT_OEN_D
0x537	0x00	ARQ2[7:0]	MAX_RT_ERR_D	RT_CNT_D[6:0]						
CFGC_A CC_1										
0x560	0xF0	TR0[7:0]	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0x561	0xB0	TR1[7:0]	BW_MULT[1:0]		BW_VAL[5:0]					

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ADDRESS	RESET	NAME	MSB							LSB
0x563	0x00	TR3[7:0]	–	–	–	–	–	TX_SRC_ID[2:0]		
0x564	0xFF	TR4[7:0]	RX_SRC_SEL[7:0]							
0x565	0x18	ARQ0[7:0]	–	RSVD	RSVD	RSVD	RSVD	DIS_DBL_ACK_RETX	–	–
0x566	0x72	ARQ1[7:0]	–	RSVD[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
0x567	0x00	ARQ2[7:0]	MAX_RT_ERR	RT_CNT[6:0]						
CFGC_B CC_1										
0x570	0xF0	TR0[7:0]	TX_CRC_EN_B	RX_CRC_EN_B	RSVD[1:0]		PRIO_VAL_B[1:0]		PRIO_CFG_B[1:0]	
0x571	0xB0	TR1[7:0]	BW_MULT_B[1:0]		BW_VAL_B[5:0]					
0x573	0x00	TR3[7:0]	–	–	–	–	–	TX_SRC_ID_B[2:0]		
0x574	0xFF	TR4[7:0]	RX_SRC_SEL_B[7:0]							
0x575	0x18	ARQ0[7:0]	–	RSVD	RSVD	RSVD	RSVD	DIS_DBL_ACK_RETX_B	–	–
0x576	0x72	ARQ1[7:0]	–	RSVD[2:0]			–	–	MAX_RT_ERR_OEN_B	RT_CNT_OEN_B
0x577	0x00	ARQ2[7:0]	MAX_RT_ERR_B	RT_CNT_B[6:0]						
CFGC_C CC_1										
0x580	0xF0	TR0[7:0]	TX_CRC_EN_C	RX_CRC_EN_C	RSVD[1:0]		PRIO_VAL_C[1:0]		PRIO_CFG_C[1:0]	
0x581	0xB0	TR1[7:0]	BW_MULT_C[1:0]		BW_VAL_C[5:0]					
0x583	0x00	TR3[7:0]	–	–	–	–	–	TX_SRC_ID_C[2:0]		
0x584	0xFF	TR4[7:0]	RX_SRC_SEL_C[7:0]							
0x585	0x18	ARQ0[7:0]	–	RSVD	RSVD	RSVD	RSVD	DIS_DBL_ACK_RETX_C	–	–
0x586	0x72	ARQ1[7:0]	–	RSVD[2:0]			–	–	MAX_RT_ERR_OEN_C	RT_CNT_OEN_C
0x587	0x00	ARQ2[7:0]	MAX_RT_ERR_C	RT_CNT_C[6:0]						
CFGC_D CC_1										
0x590	0xF0	TR0[7:0]	TX_CRC_EN_D	RX_CRC_EN_D	RSVD[1:0]		PRIO_VAL_D[1:0]		PRIO_CFG_D[1:0]	
0x591	0xB0	TR1[7:0]	BW_MULT_D[1:0]		BW_VAL_D[5:0]					
0x593	0x00	TR3[7:0]	–	–	–	–	–	TX_SRC_ID_D[2:0]		
0x594	0xFF	TR4[7:0]	RX_SRC_SEL_D[7:0]							
0x595	0x18	ARQ0[7:0]	–	RSVD	RSVD	RSVD	RSVD	DIS_DBL_ACK_RETX_D	–	–

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0x596	0x72	ARQ1[7:0]	–	RSVD[2:0]			–	–	MAX_RT_ERR_OEN_D	RT_CNT_OEN_D
0x597	0x00	ARQ2[7:0]	MAX_RT_ERR_D	RT_CNT_D[6:0]						
CFGC_A CC_2										
0x5A0	0xF0	TR0[7:0]	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0x5A1	0xB0	TR1[7:0]	BW_MULT[1:0]		BW_VAL[5:0]					
0x5A3	0x00	TR3[7:0]	–	–	–	–	–	TX_SRC_ID[2:0]		
0x5A4	0xFF	TR4[7:0]	RX_SRC_SEL[7:0]							
0x5A5	0x18	ARQ0[7:0]	–	RSVD	RSVD	RSVD	RSVD	DIS_DBL_ACK_RETX	–	–
0x5A6	0x72	ARQ1[7:0]	–	RSVD[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
0x5A7	0x00	ARQ2[7:0]	MAX_RT_ERR	RT_CNT[6:0]						
CFGC_B CC_2										
0x5B0	0xF0	TR0[7:0]	TX_CRC_EN_B	RX_CRC_EN_B	RSVD[1:0]		PRIO_VAL_B[1:0]		PRIO_CFG_B[1:0]	
0x5B1	0xB0	TR1[7:0]	BW_MULT_B[1:0]		BW_VAL_B[5:0]					
0x5B3	0x00	TR3[7:0]	–	–	–	–	–	TX_SRC_ID_B[2:0]		
0x5B4	0xFF	TR4[7:0]	RX_SRC_SEL_B[7:0]							
0x5B5	0x18	ARQ0[7:0]	–	RSVD	RSVD	RSVD	RSVD	DIS_DBL_ACK_RETX_B	–	–
0x5B6	0x72	ARQ1[7:0]	–	RSVD[2:0]			–	–	MAX_RT_ERR_OEN_B	RT_CNT_OEN_B
0x5B7	0x00	ARQ2[7:0]	MAX_RT_ERR_B	RT_CNT_B[6:0]						
CFGC_C CC_2										
0x5C0	0xF0	TR0[7:0]	TX_CRC_EN_C	RX_CRC_EN_C	RSVD[1:0]		PRIO_VAL_C[1:0]		PRIO_CFG_C[1:0]	
0x5C1	0xB0	TR1[7:0]	BW_MULT_C[1:0]		BW_VAL_C[5:0]					
0x5C3	0x00	TR3[7:0]	–	–	–	–	–	TX_SRC_ID_C[2:0]		
0x5C4	0xFF	TR4[7:0]	RX_SRC_SEL_C[7:0]							
0x5C5	0x18	ARQ0[7:0]	–	RSVD	RSVD	RSVD	RSVD	DIS_DBL_ACK_RETX_C	–	–
0x5C6	0x72	ARQ1[7:0]	–	RSVD[2:0]			–	–	MAX_RT_ERR_OEN_C	RT_CNT_OEN_C
0x5C7	0x00	ARQ2[7:0]	MAX_RT_ERR_C	RT_CNT_C[6:0]						

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ADDRESS	RESET	NAME	MSB							LSB
CFGC_D CC_2										
0x5D0	0xF0	TR0[7:0]	TX_CRC_EN_D	RX_CRC_EN_D	RSVD[1:0]		PRIO_VAL_D[1:0]		PRIO_CFG_D[1:0]	
0x5D1	0xB0	TR1[7:0]	BW_MULT_D[1:0]		BW_VAL_D[5:0]					
0x5D3	0x00	TR3[7:0]	–	–	–	–	–	TX_SRC_ID_D[2:0]		
0x5D4	0xFF	TR4[7:0]	RX_SRC_SEL_D[7:0]							
0x5D5	0x18	ARQ0[7:0]	–	RSVD	RSVD	RSVD	RSVD	DIS_DBL_ACK_RETX_D	–	–
0x5D6	0x72	ARQ1[7:0]	–	RSVD[2:0]			–	–	MAX_RT_ERR_OEN_D	RT_CNT_OEN_D
0x5D7	0x00	ARQ2[7:0]	MAX_RT_ERR_D	RT_CNT_D[6:0]						
CC_G2P0_A										
0x640	0x26	I2C_0[7:0]	–	–	SLV_SH_P0_A[1:0]		–	SLV_TO_P0_A[2:0]		
0x641	0x56	I2C_1[7:0]	RSVD	MST_BT_P0_A[2:0]			–	MST_TO_P0_A[2:0]		
0x642	0x00	I2C_2[7:0]	SRC_A_P0_A[6:0]							–
0x643	0x00	I2C_3[7:0]	DST_A_P0_A[6:0]							–
0x644	0x00	I2C_4[7:0]	SRC_B_P0_A[6:0]							–
0x645	0x00	I2C_5[7:0]	DST_B_P0_A[6:0]							–
CC_G2P0_B										
0x650	0x26	I2C_0[7:0]	–	–	SLV_SH_P0_B[1:0]		–	SLV_TO_P0_B[2:0]		
0x651	0x56	I2C_1[7:0]	RSVD	MST_BT_P0_B[2:0]			–	MST_TO_P0_B[2:0]		
0x652	0x00	I2C_2[7:0]	SRC_A_P0_B[6:0]							–
0x653	0x00	I2C_3[7:0]	DST_A_P0_B[6:0]							–
0x654	0x00	I2C_4[7:0]	SRC_B_P0_B[6:0]							–
0x655	0x00	I2C_5[7:0]	DST_B_P0_B[6:0]							–
CC_G2P0_C										
0x660	0x26	I2C_0[7:0]	–	–	SLV_SH_P0_C[1:0]		–	SLV_TO_P0_C[2:0]		
0x661	0x56	I2C_1[7:0]	RSVD	MST_BT_P0_C[2:0]			–	MST_TO_P0_C[2:0]		
0x662	0x00	I2C_2[7:0]	SRC_A_P0_C[6:0]							–
0x663	0x00	I2C_3[7:0]	DST_A_P0_C[6:0]							–
0x664	0x00	I2C_4[7:0]	SRC_B_P0_C[6:0]							–
0x665	0x00	I2C_5[7:0]	DST_B_P0_C[6:0]							–
CC_G2P0_D										
0x670	0x26	I2C_0[7:0]	–	–	SLV_SH_P0_D[1:0]		–	SLV_TO_P0_D[2:0]		
0x671	0x56	I2C_1[7:0]	RSVD	MST_BT_P0_D[2:0]			–	MST_TO_P0_D[2:0]		
0x672	0x00	I2C_2[7:0]	SRC_A_P0_D[6:0]							–
0x673	0x00	I2C_3[7:0]	DST_A_P0_D[6:0]							–
0x674	0x00	I2C_4[7:0]	SRC_B_P0_D[6:0]							–
0x675	0x00	I2C_5[7:0]	DST_B_P0_D[6:0]							–
CC_G2P1_A										
0x680	0x26	I2C_0[7:0]	–	–	SLV_SH_P1_A[1:0]		–	SLV_TO_P1_A[2:0]		

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0x681	0x56	I2C_1[7:0]	RSVD	MST_BT_P1_A[2:0]		–	MST_TO_P1_A[2:0]		
0x682	0x00	I2C_2[7:0]	SRC_A_P1_A[6:0]						–
0x683	0x00	I2C_3[7:0]	DST_A_P1_A[6:0]						–
0x684	0x00	I2C_4[7:0]	SRC_B_P1_A[6:0]						–
0x685	0x00	I2C_5[7:0]	DST_B_P1_A[6:0]						–
CC_G2P2_A									
0x688	0x26	I2C_0[7:0]	–	–	SLV_SH_P2_A[1:0]	–	SLV_TO_P2_A[2:0]		
0x689	0x56	I2C_1[7:0]	RSVD	MST_BT_P2_A[2:0]		–	MST_TO_P2_A[2:0]		
0x68A	0x00	I2C_2[7:0]	SRC_A_P2_A[6:0]						–
0x68B	0x00	I2C_3[7:0]	DST_A_P2_A[6:0]						–
0x68C	0x00	I2C_4[7:0]	SRC_B_P2_A[6:0]						–
0x68D	0x00	I2C_5[7:0]	DST_B_P2_A[6:0]						–
CC_G2P1_B									
0x690	0x26	I2C_0[7:0]	–	–	SLV_SH_P1_B[1:0]	–	SLV_TO_P1_B[2:0]		
0x691	0x56	I2C_1[7:0]	RSVD	MST_BT_P1_B[2:0]		–	MST_TO_P1_B[2:0]		
0x692	0x00	I2C_2[7:0]	SRC_A_P1_B[6:0]						–
0x693	0x00	I2C_3[7:0]	DST_A_P1_B[6:0]						–
0x694	0x00	I2C_4[7:0]	SRC_B_P1_B[6:0]						–
0x695	0x00	I2C_5[7:0]	DST_B_P1_B[6:0]						–
CC_G2P2_B									
0x698	0x26	I2C_0[7:0]	–	–	SLV_SH_P2_B[1:0]	–	SLV_TO_P2_B[2:0]		
0x699	0x56	I2C_1[7:0]	RSVD	MST_BT_P2_B[2:0]		–	MST_TO_P2_B[2:0]		
0x69A	0x00	I2C_2[7:0]	SRC_A_P2_B[6:0]						–
0x69B	0x00	I2C_3[7:0]	DST_A_P2_B[6:0]						–
0x69C	0x00	I2C_4[7:0]	SRC_B_P2_B[6:0]						–
0x69D	0x00	I2C_5[7:0]	DST_B_P2_B[6:0]						–
CC_G2P1_C									
0x6A0	0x26	I2C_0[7:0]	–	–	SLV_SH_P1_C[1:0]	–	SLV_TO_P1_C[2:0]		
0x6A1	0x56	I2C_1[7:0]	RSVD	MST_BT_P1_C[2:0]		–	MST_TO_P1_C[2:0]		
0x6A2	0x00	I2C_2[7:0]	SRC_A_P1_C[6:0]						–
0x6A3	0x00	I2C_3[7:0]	DST_A_P1_C[6:0]						–
0x6A4	0x00	I2C_4[7:0]	SRC_B_P1_C[6:0]						–
0x6A5	0x00	I2C_5[7:0]	DST_B_P1_C[6:0]						–
CC_G2P2_C									
0x6A8	0x26	I2C_0[7:0]	–	–	SLV_SH_P2_C[1:0]	–	SLV_TO_P2_C[2:0]		
0x6A9	0x56	I2C_1[7:0]	RSVD	MST_BT_P2_C[2:0]		–	MST_TO_P2_C[2:0]		
0x6AA	0x00	I2C_2[7:0]	SRC_A_P2_C[6:0]						–
0x6AB	0x00	I2C_3[7:0]	DST_A_P2_C[6:0]						–
0x6AC	0x00	I2C_4[7:0]	SRC_B_P2_C[6:0]						–
0x6AD	0x00	I2C_5[7:0]	DST_B_P2_C[6:0]						–
CC_G2P1_D									
0x6B0	0x26	I2C_0[7:0]	–	–	SLV_SH_P1_D[1:0]	–	SLV_TO_P1_D[2:0]		

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0x6B1	0x56	I2C_1[7:0]	RSVD	MST_BT_P1_D[2:0]			–	MST_TO_P1_D[2:0]		
0x6B2	0x00	I2C_2[7:0]	SRC_A_P1_D[6:0]							–
0x6B3	0x00	I2C_3[7:0]	DST_A_P1_D[6:0]							–
0x6B4	0x00	I2C_4[7:0]	SRC_B_P1_D[6:0]							–
0x6B5	0x00	I2C_5[7:0]	DST_B_P1_D[6:0]							–
CC_G2P2_D										
0x6B8	0x26	I2C_0[7:0]	–	–	SLV_SH_P2_D[1:0]		–	SLV_TO_P2_D[2:0]		
0x6B9	0x56	I2C_1[7:0]	RSVD	MST_BT_P2_D[2:0]			–	MST_TO_P2_D[2:0]		
0x6BA	0x00	I2C_2[7:0]	SRC_A_P2_D[6:0]							–
0x6BB	0x00	I2C_3[7:0]	DST_A_P2_D[6:0]							–
0x6BC	0x00	I2C_4[7:0]	SRC_B_P2_D[6:0]							–
0x6BD	0x00	I2C_5[7:0]	DST_B_P2_D[6:0]							–
CMU										
0x6C2	0x00	CMU2[7:0]	RSVD	RSVD[2:0]			RSVD	RSVD[1:0]		RSVD
0x6C4	0x00	CMU4[7:0]	A_SPEED[1:0]		B_SPEED[1:0]		C_SPEED[1:0]		D_SPEED[1:0]	
MISC										
0x6DF	0x60	DP_ORSTB_CTL[7:0]	–	DP_RST_MIPI3	DP_RST_STABLE	DP_RST_MIPI2	DP_RST_MIPI	DP_RST_VP	DP_RST_FS	DP_RST_CC
MIPI_TX_EXT 0										
0x800	0x00	MIPI_TX_EXT 0[7:0]	MAP_SRC_0_H[2:0]			MAP_DST_0_H[2:0]			–	–
0x801	0x00	MIPI_TX_EXT 1[7:0]	MAP_SRC_1_H[2:0]			MAP_DST_1_H[2:0]			–	–
0x802	0x00	MIPI_TX_EXT 2[7:0]	MAP_SRC_2_H[2:0]			MAP_DST_2_H[2:0]			–	–
0x803	0x00	MIPI_TX_EXT 3[7:0]	MAP_SRC_3_H[2:0]			MAP_DST_3_H[2:0]			–	–
0x804	0x00	MIPI_TX_EXT 4[7:0]	MAP_SRC_4_H[2:0]			MAP_DST_4_H[2:0]			–	–
0x805	0x00	MIPI_TX_EXT 5[7:0]	MAP_SRC_5_H[2:0]			MAP_DST_5_H[2:0]			–	–
0x806	0x00	MIPI_TX_EXT 6[7:0]	MAP_SRC_6_H[2:0]			MAP_DST_6_H[2:0]			–	–
0x807	0x00	MIPI_TX_EXT 7[7:0]	MAP_SRC_7_H[2:0]			MAP_DST_7_H[2:0]			–	–
0x808	0x00	MIPI_TX_EXT 8[7:0]	MAP_SRC_8_H[2:0]			MAP_DST_8_H[2:0]			–	–
0x809	0x00	MIPI_TX_EXT 9[7:0]	MAP_SRC_9_H[2:0]			MAP_DST_9_H[2:0]			–	–
0x80A	0x00	MIPI_TX_EXT 10[7:0]	MAP_SRC_10_H[2:0]			MAP_DST_10_H[2:0]			–	–
0x80B	0x00	MIPI_TX_EXT 11[7:0]	MAP_SRC_11_H[2:0]			MAP_DST_11_H[2:0]			–	–
0x80C	0x00	MIPI_TX_EXT 12[7:0]	MAP_SRC_12_H[2:0]			MAP_DST_12_H[2:0]			–	–

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0x80D	0x00	MIPI_TX_EXT 13[7:0]	MAP_SRC_13_H[2:0]			MAP_DST_13_H[2:0]			–	–
0x80E	0x00	MIPI_TX_EXT 14[7:0]	MAP_SRC_14_H[2:0]			MAP_DST_14_H[2:0]			–	–
0x80F	0x00	MIPI_TX_EXT 15[7:0]	MAP_SRC_15_H[2:0]			MAP_DST_15_H[2:0]			–	–
MIPI_TX_EXT 1										
0x810	0x00	MIPI_TX_EXT 0[7:0]	MAP_SRC_0_H[2:0]			MAP_DST_0_H[2:0]			–	–
0x811	0x00	MIPI_TX_EXT 1[7:0]	MAP_SRC_1_H[2:0]			MAP_DST_1_H[2:0]			–	–
0x812	0x00	MIPI_TX_EXT 2[7:0]	MAP_SRC_2_H[2:0]			MAP_DST_2_H[2:0]			–	–
0x813	0x00	MIPI_TX_EXT 3[7:0]	MAP_SRC_3_H[2:0]			MAP_DST_3_H[2:0]			–	–
0x814	0x00	MIPI_TX_EXT 4[7:0]	MAP_SRC_4_H[2:0]			MAP_DST_4_H[2:0]			–	–
0x815	0x00	MIPI_TX_EXT 5[7:0]	MAP_SRC_5_H[2:0]			MAP_DST_5_H[2:0]			–	–
0x816	0x00	MIPI_TX_EXT 6[7:0]	MAP_SRC_6_H[2:0]			MAP_DST_6_H[2:0]			–	–
0x817	0x00	MIPI_TX_EXT 7[7:0]	MAP_SRC_7_H[2:0]			MAP_DST_7_H[2:0]			–	–
0x818	0x00	MIPI_TX_EXT 8[7:0]	MAP_SRC_8_H[2:0]			MAP_DST_8_H[2:0]			–	–
0x819	0x00	MIPI_TX_EXT 9[7:0]	MAP_SRC_9_H[2:0]			MAP_DST_9_H[2:0]			–	–
0x81A	0x00	MIPI_TX_EXT 10[7:0]	MAP_SRC_10_H[2:0]			MAP_DST_10_H[2:0]			–	–
0x81B	0x00	MIPI_TX_EXT 11[7:0]	MAP_SRC_11_H[2:0]			MAP_DST_11_H[2:0]			–	–
0x81C	0x00	MIPI_TX_EXT 12[7:0]	MAP_SRC_12_H[2:0]			MAP_DST_12_H[2:0]			–	–
0x81D	0x00	MIPI_TX_EXT 13[7:0]	MAP_SRC_13_H[2:0]			MAP_DST_13_H[2:0]			–	–
0x81E	0x00	MIPI_TX_EXT 14[7:0]	MAP_SRC_14_H[2:0]			MAP_DST_14_H[2:0]			–	–
0x81F	0x00	MIPI_TX_EXT 15[7:0]	MAP_SRC_15_H[2:0]			MAP_DST_15_H[2:0]			–	–
MIPI_TX_EXT 2										
0x820	0x00	MIPI_TX_EXT 0[7:0]	MAP_SRC_0_H[2:0]			MAP_DST_0_H[2:0]			–	–
0x821	0x00	MIPI_TX_EXT 1[7:0]	MAP_SRC_1_H[2:0]			MAP_DST_1_H[2:0]			–	–
0x822	0x00	MIPI_TX_EXT 2[7:0]	MAP_SRC_2_H[2:0]			MAP_DST_2_H[2:0]			–	–
0x823	0x00	MIPI_TX_EXT 3[7:0]	MAP_SRC_3_H[2:0]			MAP_DST_3_H[2:0]			–	–

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0x824	0x00	MIPI_TX_EXT 4[7:0]	MAP_SRC_4_H[2:0]			MAP_DST_4_H[2:0]			–	–
0x825	0x00	MIPI_TX_EXT 5[7:0]	MAP_SRC_5_H[2:0]			MAP_DST_5_H[2:0]			–	–
0x826	0x00	MIPI_TX_EXT 6[7:0]	MAP_SRC_6_H[2:0]			MAP_DST_6_H[2:0]			–	–
0x827	0x00	MIPI_TX_EXT 7[7:0]	MAP_SRC_7_H[2:0]			MAP_DST_7_H[2:0]			–	–
0x828	0x00	MIPI_TX_EXT 8[7:0]	MAP_SRC_8_H[2:0]			MAP_DST_8_H[2:0]			–	–
0x829	0x00	MIPI_TX_EXT 9[7:0]	MAP_SRC_9_H[2:0]			MAP_DST_9_H[2:0]			–	–
0x82A	0x00	MIPI_TX_EXT 10[7:0]	MAP_SRC_10_H[2:0]			MAP_DST_10_H[2:0]			–	–
0x82B	0x00	MIPI_TX_EXT 11[7:0]	MAP_SRC_11_H[2:0]			MAP_DST_11_H[2:0]			–	–
0x82C	0x00	MIPI_TX_EXT 12[7:0]	MAP_SRC_12_H[2:0]			MAP_DST_12_H[2:0]			–	–
0x82D	0x00	MIPI_TX_EXT 13[7:0]	MAP_SRC_13_H[2:0]			MAP_DST_13_H[2:0]			–	–
0x82E	0x00	MIPI_TX_EXT 14[7:0]	MAP_SRC_14_H[2:0]			MAP_DST_14_H[2:0]			–	–
0x82F	0x00	MIPI_TX_EXT 15[7:0]	MAP_SRC_15_H[2:0]			MAP_DST_15_H[2:0]			–	–
MIPI_TX_EXT 3										
0x830	0x00	MIPI_TX_EXT 0[7:0]	MAP_SRC_0_H[2:0]			MAP_DST_0_H[2:0]			–	–
0x831	0x00	MIPI_TX_EXT 1[7:0]	MAP_SRC_1_H[2:0]			MAP_DST_1_H[2:0]			–	–
0x832	0x00	MIPI_TX_EXT 2[7:0]	MAP_SRC_2_H[2:0]			MAP_DST_2_H[2:0]			–	–
0x833	0x00	MIPI_TX_EXT 3[7:0]	MAP_SRC_3_H[2:0]			MAP_DST_3_H[2:0]			–	–
0x834	0x00	MIPI_TX_EXT 4[7:0]	MAP_SRC_4_H[2:0]			MAP_DST_4_H[2:0]			–	–
0x835	0x00	MIPI_TX_EXT 5[7:0]	MAP_SRC_5_H[2:0]			MAP_DST_5_H[2:0]			–	–
0x836	0x00	MIPI_TX_EXT 6[7:0]	MAP_SRC_6_H[2:0]			MAP_DST_6_H[2:0]			–	–
0x837	0x00	MIPI_TX_EXT 7[7:0]	MAP_SRC_7_H[2:0]			MAP_DST_7_H[2:0]			–	–
0x838	0x00	MIPI_TX_EXT 8[7:0]	MAP_SRC_8_H[2:0]			MAP_DST_8_H[2:0]			–	–
0x839	0x00	MIPI_TX_EXT 9[7:0]	MAP_SRC_9_H[2:0]			MAP_DST_9_H[2:0]			–	–
0x83A	0x00	MIPI_TX_EXT 10[7:0]	MAP_SRC_10_H[2:0]			MAP_DST_10_H[2:0]			–	–
0x83B	0x00	MIPI_TX_EXT 11[7:0]	MAP_SRC_11_H[2:0]			MAP_DST_11_H[2:0]			–	–

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0x83C	0x00	MIPI_TX_EXT 12[7:0]	MAP_SRC_12_H[2:0]			MAP_DST_12_H[2:0]			–	–
0x83D	0x00	MIPI_TX_EXT 13[7:0]	MAP_SRC_13_H[2:0]			MAP_DST_13_H[2:0]			–	–
0x83E	0x00	MIPI_TX_EXT 14[7:0]	MAP_SRC_14_H[2:0]			MAP_DST_14_H[2:0]			–	–
0x83F	0x00	MIPI_TX_EXT 15[7:0]	MAP_SRC_15_H[2:0]			MAP_DST_15_H[2:0]			–	–
MIPI_TX_EXT 4										
0x840	0x00	MIPI_TX_EXT 0[7:0]	MAP_SRC_0_H[2:0]			MAP_DST_0_H[2:0]			–	–
0x841	0x00	MIPI_TX_EXT 1[7:0]	MAP_SRC_1_H[2:0]			MAP_DST_1_H[2:0]			–	–
0x842	0x00	MIPI_TX_EXT 2[7:0]	MAP_SRC_2_H[2:0]			MAP_DST_2_H[2:0]			–	–
0x843	0x00	MIPI_TX_EXT 3[7:0]	MAP_SRC_3_H[2:0]			MAP_DST_3_H[2:0]			–	–
0x844	0x00	MIPI_TX_EXT 4[7:0]	MAP_SRC_4_H[2:0]			MAP_DST_4_H[2:0]			–	–
0x845	0x00	MIPI_TX_EXT 5[7:0]	MAP_SRC_5_H[2:0]			MAP_DST_5_H[2:0]			–	–
0x846	0x00	MIPI_TX_EXT 6[7:0]	MAP_SRC_6_H[2:0]			MAP_DST_6_H[2:0]			–	–
0x847	0x00	MIPI_TX_EXT 7[7:0]	MAP_SRC_7_H[2:0]			MAP_DST_7_H[2:0]			–	–
0x848	0x00	MIPI_TX_EXT 8[7:0]	MAP_SRC_8_H[2:0]			MAP_DST_8_H[2:0]			–	–
0x849	0x00	MIPI_TX_EXT 9[7:0]	MAP_SRC_9_H[2:0]			MAP_DST_9_H[2:0]			–	–
0x84A	0x00	MIPI_TX_EXT 10[7:0]	MAP_SRC_10_H[2:0]			MAP_DST_10_H[2:0]			–	–
0x84B	0x00	MIPI_TX_EXT 11[7:0]	MAP_SRC_11_H[2:0]			MAP_DST_11_H[2:0]			–	–
0x84C	0x00	MIPI_TX_EXT 12[7:0]	MAP_SRC_12_H[2:0]			MAP_DST_12_H[2:0]			–	–
0x84D	0x00	MIPI_TX_EXT 13[7:0]	MAP_SRC_13_H[2:0]			MAP_DST_13_H[2:0]			–	–
0x84E	0x00	MIPI_TX_EXT 14[7:0]	MAP_SRC_14_H[2:0]			MAP_DST_14_H[2:0]			–	–
0x84F	0x00	MIPI_TX_EXT 15[7:0]	MAP_SRC_15_H[2:0]			MAP_DST_15_H[2:0]			–	–
MIPI_TX_EXT 5										
0x850	0x00	MIPI_TX_EXT 0[7:0]	MAP_SRC_0_H[2:0]			MAP_DST_0_H[2:0]			–	–
0x851	0x00	MIPI_TX_EXT 1[7:0]	MAP_SRC_1_H[2:0]			MAP_DST_1_H[2:0]			–	–
0x852	0x00	MIPI_TX_EXT 2[7:0]	MAP_SRC_2_H[2:0]			MAP_DST_2_H[2:0]			–	–

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0x853	0x00	MIPI_TX_EXT 3[7:0]	MAP_SRC_3_H[2:0]			MAP_DST_3_H[2:0]			–	–
0x854	0x00	MIPI_TX_EXT 4[7:0]	MAP_SRC_4_H[2:0]			MAP_DST_4_H[2:0]			–	–
0x855	0x00	MIPI_TX_EXT 5[7:0]	MAP_SRC_5_H[2:0]			MAP_DST_5_H[2:0]			–	–
0x856	0x00	MIPI_TX_EXT 6[7:0]	MAP_SRC_6_H[2:0]			MAP_DST_6_H[2:0]			–	–
0x857	0x00	MIPI_TX_EXT 7[7:0]	MAP_SRC_7_H[2:0]			MAP_DST_7_H[2:0]			–	–
0x858	0x00	MIPI_TX_EXT 8[7:0]	MAP_SRC_8_H[2:0]			MAP_DST_8_H[2:0]			–	–
0x859	0x00	MIPI_TX_EXT 9[7:0]	MAP_SRC_9_H[2:0]			MAP_DST_9_H[2:0]			–	–
0x85A	0x00	MIPI_TX_EXT 10[7:0]	MAP_SRC_10_H[2:0]			MAP_DST_10_H[2:0]			–	–
0x85B	0x00	MIPI_TX_EXT 11[7:0]	MAP_SRC_11_H[2:0]			MAP_DST_11_H[2:0]			–	–
0x85C	0x00	MIPI_TX_EXT 12[7:0]	MAP_SRC_12_H[2:0]			MAP_DST_12_H[2:0]			–	–
0x85D	0x00	MIPI_TX_EXT 13[7:0]	MAP_SRC_13_H[2:0]			MAP_DST_13_H[2:0]			–	–
0x85E	0x00	MIPI_TX_EXT 14[7:0]	MAP_SRC_14_H[2:0]			MAP_DST_14_H[2:0]			–	–
0x85F	0x00	MIPI_TX_EXT 15[7:0]	MAP_SRC_15_H[2:0]			MAP_DST_15_H[2:0]			–	–
MIPI_TX_EXT 6										
0x860	0x00	MIPI_TX_EXT 0[7:0]	MAP_SRC_0_H[2:0]			MAP_DST_0_H[2:0]			–	–
0x861	0x00	MIPI_TX_EXT 1[7:0]	MAP_SRC_1_H[2:0]			MAP_DST_1_H[2:0]			–	–
0x862	0x00	MIPI_TX_EXT 2[7:0]	MAP_SRC_2_H[2:0]			MAP_DST_2_H[2:0]			–	–
0x863	0x00	MIPI_TX_EXT 3[7:0]	MAP_SRC_3_H[2:0]			MAP_DST_3_H[2:0]			–	–
0x864	0x00	MIPI_TX_EXT 4[7:0]	MAP_SRC_4_H[2:0]			MAP_DST_4_H[2:0]			–	–
0x865	0x00	MIPI_TX_EXT 5[7:0]	MAP_SRC_5_H[2:0]			MAP_DST_5_H[2:0]			–	–
0x866	0x00	MIPI_TX_EXT 6[7:0]	MAP_SRC_6_H[2:0]			MAP_DST_6_H[2:0]			–	–
0x867	0x00	MIPI_TX_EXT 7[7:0]	MAP_SRC_7_H[2:0]			MAP_DST_7_H[2:0]			–	–
0x868	0x00	MIPI_TX_EXT 8[7:0]	MAP_SRC_8_H[2:0]			MAP_DST_8_H[2:0]			–	–
0x869	0x00	MIPI_TX_EXT 9[7:0]	MAP_SRC_9_H[2:0]			MAP_DST_9_H[2:0]			–	–
0x86A	0x00	MIPI_TX_EXT 10[7:0]	MAP_SRC_10_H[2:0]			MAP_DST_10_H[2:0]			–	–

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0x86B	0x00	MIPI_TX_EXT 11[7:0]	MAP_SRC_11_H[2:0]			MAP_DST_11_H[2:0]			–	–
0x86C	0x00	MIPI_TX_EXT 12[7:0]	MAP_SRC_12_H[2:0]			MAP_DST_12_H[2:0]			–	–
0x86D	0x00	MIPI_TX_EXT 13[7:0]	MAP_SRC_13_H[2:0]			MAP_DST_13_H[2:0]			–	–
0x86E	0x00	MIPI_TX_EXT 14[7:0]	MAP_SRC_14_H[2:0]			MAP_DST_14_H[2:0]			–	–
0x86F	0x00	MIPI_TX_EXT 15[7:0]	MAP_SRC_15_H[2:0]			MAP_DST_15_H[2:0]			–	–
MIPI_TX_EXT 7										
0x870	0x00	MIPI_TX_EXT 0[7:0]	MAP_SRC_0_H[2:0]			MAP_DST_0_H[2:0]			–	–
0x871	0x00	MIPI_TX_EXT 1[7:0]	MAP_SRC_1_H[2:0]			MAP_DST_1_H[2:0]			–	–
0x872	0x00	MIPI_TX_EXT 2[7:0]	MAP_SRC_2_H[2:0]			MAP_DST_2_H[2:0]			–	–
0x873	0x00	MIPI_TX_EXT 3[7:0]	MAP_SRC_3_H[2:0]			MAP_DST_3_H[2:0]			–	–
0x874	0x00	MIPI_TX_EXT 4[7:0]	MAP_SRC_4_H[2:0]			MAP_DST_4_H[2:0]			–	–
0x875	0x00	MIPI_TX_EXT 5[7:0]	MAP_SRC_5_H[2:0]			MAP_DST_5_H[2:0]			–	–
0x876	0x00	MIPI_TX_EXT 6[7:0]	MAP_SRC_6_H[2:0]			MAP_DST_6_H[2:0]			–	–
0x877	0x00	MIPI_TX_EXT 7[7:0]	MAP_SRC_7_H[2:0]			MAP_DST_7_H[2:0]			–	–
0x878	0x00	MIPI_TX_EXT 8[7:0]	MAP_SRC_8_H[2:0]			MAP_DST_8_H[2:0]			–	–
0x879	0x00	MIPI_TX_EXT 9[7:0]	MAP_SRC_9_H[2:0]			MAP_DST_9_H[2:0]			–	–
0x87A	0x00	MIPI_TX_EXT 10[7:0]	MAP_SRC_10_H[2:0]			MAP_DST_10_H[2:0]			–	–
0x87B	0x00	MIPI_TX_EXT 11[7:0]	MAP_SRC_11_H[2:0]			MAP_DST_11_H[2:0]			–	–
0x87C	0x00	MIPI_TX_EXT 12[7:0]	MAP_SRC_12_H[2:0]			MAP_DST_12_H[2:0]			–	–
0x87D	0x00	MIPI_TX_EXT 13[7:0]	MAP_SRC_13_H[2:0]			MAP_DST_13_H[2:0]			–	–
0x87E	0x00	MIPI_TX_EXT 14[7:0]	MAP_SRC_14_H[2:0]			MAP_DST_14_H[2:0]			–	–
0x87F	0x00	MIPI_TX_EXT 15[7:0]	MAP_SRC_15_H[2:0]			MAP_DST_15_H[2:0]			–	–
MIPI_PHY										
0x8A0	0x04	MIPI_PHY0[7:0]	force_csi_out_en	force_clk3_en	force_clk0_en	phy_1x4b_22	phy_1x4a_22	phy_2x4	RSVD	phy_4x2
0x8A1	0x00	MIPI_PHY1[7:0]	t_hs_przero[1:0]		t_hs_prep[1:0]		t_clk_trail[1:0]		t_clk_przero[1:0]	

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0x8A2	0xF4	MIPI_PHY2[7:0]	phy_Stdby_n[3:0]				t_lpx[1:0]		t_hs_trail[1:0]	
0x8A3	0x4E	MIPI_PHY3[7:0]	phy1_lane_map[3:0]				phy0_lane_map[3:0]			
0x8A4	0xE4	MIPI_PHY4[7:0]	phy3_lane_map[3:0]				phy2_lane_map[3:0]			
0x8A5	0x00	MIPI_PHY5[7:0]	t_clk_prep[1:0]		phy1_pol_map[2:0]			phy0_pol_map[2:0]		
0x8A6	0x00	MIPI_PHY6[7:0]	–	–	phy3_pol_map[2:0]			phy2_pol_map[2:0]		
0x8A8	0x00	MIPI_PHY8[7:0]	t_lpxesc[2:0]			RSVD	RSVD	RSVD	RSVD	RSVD
0x8A9	0x00	MIPI_PHY9[7:0]	phy_cp0[4:0]					–	RSVD	RSVD
0x8AA	0x02	MIPI_PHY10[7:0]	phy_cp1[4:0]					–	RSVD	RSVD
0x8AB	0x00	MIPI_PHY11[7:0]	phy_cp_err[3:0]				–	–	RSVD	–
0x8AD	0x00	MIPI_PHY13[7:0]	–	–	t_t3_prebegin[5:0]					
0x8AE	0x01	MIPI_PHY14[7:0]	–	t_t3_post[4:0]					t_t3_prep[1:0]	
0x8C0	0x00	MIPI_PRBS_0[7:0]	MIPI_PRBS_EN_P1_LN1[1:0]		MIPI_PRBS_EN_P1_LN0[1:0]		MIPI_PRBS_EN_P0_LN1[1:0]		MIPI_PRBS_EN_P0_LN0[1:0]	
0x8C1	0x00	MIPI_PRBS_1[7:0]	MIPI_PRBS_EN_P3_LN1[1:0]		MIPI_PRBS_EN_P3_LN0[1:0]		MIPI_PRBS_EN_P2_LN1[1:0]		MIPI_PRBS_EN_P2_LN0[1:0]	
0x8C3	0xF2	MIPI_PRBS_3[7:0]	RSVD	RSVD	RSVD	RSVD	–	–	MIPI_CUSTOM_SEED_2[1:0]	
0x8C4	0x78	MIPI_PRBS_4[7:0]	MIPI_CUSTOM_SEED_1[7:0]							
0x8C5	0x9A	MIPI_PRBS_5[7:0]	MIPI_CUSTOM_SEED_0[7:0]							
0x8C6	0x0F	MIPI_PHY_15[7:0]	Force_Video_Mask[3:0]				Auto_Mask_En[3:0]			
0x8C7	0x0F	MIPI_PHY_16[7:0]	RSVD	–	–	–	Video_Mask_Restart_En[3:0]			
0x8C9	0x00	MIPI_PHY_18[7:0]	–	–	–	–	RST_MIPITX_LOC[3:0]			
0x8D0	0x00	MIPI_PHY_19[7:0]	csi2_tx1_pkt_cnt[3:0]				csi2_tx0_pkt_cnt[3:0]			
0x8D1	0x00	MIPI_PHY_20[7:0]	csi2_tx3_pkt_cnt[3:0]				csi2_tx2_pkt_cnt[3:0]			
0x8D2	0x00	MIPI_PHY_21[7:0]	phy1_pkt_cnt[3:0]				phy0_pkt_cnt[3:0]			
0x8D3	0x00	MIPI_PHY_22[7:0]	phy3_pkt_cnt[3:0]				phy2_pkt_cnt[3:0]			
MIPI_TX 0										
0x901	0x00	MIPI_TX1[7:0]	MODE[7:0]							
0x902	0x00	MIPI_TX2[7:0]	STATUS[7:0]							

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ADDRESS	RESET	NAME	MSB							LSB
0x903	0x00	MIPI_TX3[7:0]	DESKEW_INIT[7:0]							
0x904	0x00	MIPI_TX4[7:0]	DESKEW_PER[7:0]							
0x905	0x71	MIPI_TX5[7:0]	CSI2_T_PRE[7:0]							
0x906	0x19	MIPI_TX6[7:0]	CSI2_T_POST[7:0]							
0x907	0x1C	MIPI_TX7[7:0]	CSI2_TX_GAP[7:0]							
0x908	0x00	MIPI_TX8[7:0]	CSI2_TWAKEUP_L[7:0]							
0x909	0x01	MIPI_TX9[7:0]	CSI2_TWAKEUP_M[7:0]							
0x90A	0xC0	MIPI_TX10[7:0]	CSI2_LANE_CNT[1:0]		CSI2_CPHY_EN	csi2_vcx_en	–	CSI2_TWAKEUP_H[2:0]		
0x90B	0x00	MIPI_TX11[7:0]	MAP_EN_L[7:0]							
0x90C	0x00	MIPI_TX12[7:0]	MAP_EN_H[7:0]							
0x90D	0x00	MIPI_TX13[7:0]	MAP_SRC_0[7:0]							
0x90E	0x00	MIPI_TX14[7:0]	MAP_DST_0[7:0]							
0x90F	0x00	MIPI_TX15[7:0]	MAP_SRC_1[7:0]							
0x910	0x00	MIPI_TX16[7:0]	MAP_DST_1[7:0]							
0x911	0x00	MIPI_TX17[7:0]	MAP_SRC_2[7:0]							
0x912	0x00	MIPI_TX18[7:0]	MAP_DST_2[7:0]							
0x913	0x00	MIPI_TX19[7:0]	MAP_SRC_3[7:0]							
0x914	0x00	MIPI_TX20[7:0]	MAP_DST_3[7:0]							
0x915	0x00	MIPI_TX21[7:0]	MAP_SRC_4[7:0]							
0x916	0x00	MIPI_TX22[7:0]	MAP_DST_4[7:0]							
0x917	0x00	MIPI_TX23[7:0]	MAP_SRC_5[7:0]							
0x918	0x00	MIPI_TX24[7:0]	MAP_DST_5[7:0]							
0x919	0x00	MIPI_TX25[7:0]	MAP_SRC_6[7:0]							
0x91A	0x00	MIPI_TX26[7:0]	MAP_DST_6[7:0]							
0x91B	0x00	MIPI_TX27[7:0]	MAP_SRC_7[7:0]							
0x91C	0x00	MIPI_TX28[7:0]	MAP_DST_7[7:0]							
0x91D	0x00	MIPI_TX29[7:0]	MAP_SRC_8[7:0]							

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ADDRESS	RESET	NAME	MSB							LSB
0x91E	0x00	MIPI_TX30[7:0]	MAP_DST_8[7:0]							
0x91F	0x00	MIPI_TX31[7:0]	MAP_SRC_9[7:0]							
0x920	0x00	MIPI_TX32[7:0]	MAP_DST_9[7:0]							
0x921	0x00	MIPI_TX33[7:0]	MAP_SRC_10[7:0]							
0x922	0x00	MIPI_TX34[7:0]	MAP_DST_10[7:0]							
0x923	0x00	MIPI_TX35[7:0]	MAP_SRC_11[7:0]							
0x924	0x00	MIPI_TX36[7:0]	MAP_DST_11[7:0]							
0x925	0x00	MIPI_TX37[7:0]	MAP_SRC_12[7:0]							
0x926	0x00	MIPI_TX38[7:0]	MAP_DST_12[7:0]							
0x927	0x00	MIPI_TX39[7:0]	MAP_SRC_13[7:0]							
0x928	0x00	MIPI_TX40[7:0]	MAP_DST_13[7:0]							
0x929	0x00	MIPI_TX41[7:0]	MAP_SRC_14[7:0]							
0x92A	0x00	MIPI_TX42[7:0]	MAP_DST_14[7:0]							
0x92B	0x00	MIPI_TX43[7:0]	MAP_SRC_15[7:0]							
0x92C	0x00	MIPI_TX44[7:0]	MAP_DST_15[7:0]							
0x92D	0x00	MIPI_TX45[7:0]	MAP_DPHY_DEST_3[1:0]		MAP_DPHY_DEST_2[1:0]		MAP_DPHY_DEST_1[1:0]		MAP_DPHY_DEST_0[1:0]	
0x92E	0x00	MIPI_TX46[7:0]	MAP_DPHY_DEST_7[1:0]		MAP_DPHY_DEST_6[1:0]		MAP_DPHY_DEST_5[1:0]		MAP_DPHY_DEST_4[1:0]	
0x92F	0x00	MIPI_TX47[7:0]	MAP_DPHY_DEST_11[1:0]		MAP_DPHY_DEST_10[1:0]		MAP_DPHY_DEST_9[1:0]		MAP_DPHY_DEST_8[1:0]	
0x930	0x00	MIPI_TX48[7:0]	MAP_DPHY_DEST_15[1:0]		MAP_DPHY_DEST_14[1:0]		MAP_DPHY_DEST_13[1:0]		MAP_DPHY_DEST_12[1:0]	
0x931	0x00	MIPI_TX49[7:0]	MAP_CON[7:0]							
0x932	0x00	MIPI_TX50[7:0]	SKEW_PER_SEL[7:0]							
0x933	0x00	MIPI_TX51[7:0]	–	–	–	ALT2_MEM_MAP8	MODE_DT	ALT_MEM_MAP10	ALT_MEM_MAP8	ALT_MEM_MAP12
0x934	0x00	MIPI_TX52[7:0]	video_masked_latched[3:0]				video_masked[3:0]			
MIPI_TX 1										
0x941	0x00	MIPI_TX1[7:0]	MODE[7:0]							

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ADDRESS	RESET	NAME	MSB							LSB
0x942	0x00	MIPI_TX2[7:0]	STATUS[7:0]							
0x943	0x00	MIPI_TX3[7:0]	DESKEW_INIT[7:0]							
0x944	0x00	MIPI_TX4[7:0]	DESKEW_PER[7:0]							
0x945	0x71	MIPI_TX5[7:0]	CSI2_T_PRE[7:0]							
0x946	0x19	MIPI_TX6[7:0]	CSI2_T_POST[7:0]							
0x947	0x1C	MIPI_TX7[7:0]	CSI2_TX_GAP[7:0]							
0x948	0x00	MIPI_TX8[7:0]	CSI2_TWAKEUP_L[7:0]							
0x949	0x01	MIPI_TX9[7:0]	CSI2_TWAKEUP_M[7:0]							
0x94A	0xC0	MIPI_TX10[7:0]	CSI2_LANE_CNT[1:0]		CSI2_CPHY_EN	csi2_vcx_en	–	CSI2_TWAKEUP_H[2:0]		
0x94B	0x00	MIPI_TX11[7:0]	MAP_EN_L[7:0]							
0x94C	0x00	MIPI_TX12[7:0]	MAP_EN_H[7:0]							
0x94D	0x00	MIPI_TX13[7:0]	MAP_SRC_0[7:0]							
0x94E	0x00	MIPI_TX14[7:0]	MAP_DST_0[7:0]							
0x94F	0x00	MIPI_TX15[7:0]	MAP_SRC_1[7:0]							
0x950	0x00	MIPI_TX16[7:0]	MAP_DST_1[7:0]							
0x951	0x00	MIPI_TX17[7:0]	MAP_SRC_2[7:0]							
0x952	0x00	MIPI_TX18[7:0]	MAP_DST_2[7:0]							
0x953	0x00	MIPI_TX19[7:0]	MAP_SRC_3[7:0]							
0x954	0x00	MIPI_TX20[7:0]	MAP_DST_3[7:0]							
0x955	0x00	MIPI_TX21[7:0]	MAP_SRC_4[7:0]							
0x956	0x00	MIPI_TX22[7:0]	MAP_DST_4[7:0]							
0x957	0x00	MIPI_TX23[7:0]	MAP_SRC_5[7:0]							
0x958	0x00	MIPI_TX24[7:0]	MAP_DST_5[7:0]							
0x959	0x00	MIPI_TX25[7:0]	MAP_SRC_6[7:0]							
0x95A	0x00	MIPI_TX26[7:0]	MAP_DST_6[7:0]							
0x95B	0x00	MIPI_TX27[7:0]	MAP_SRC_7[7:0]							
0x95C	0x00	MIPI_TX28[7:0]	MAP_DST_7[7:0]							
0x95D	0x00	MIPI_TX29[7:0]	MAP_SRC_8[7:0]							

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ADDRESS	RESET	NAME	MSB							LSB
0x95E	0x00	MIPI_TX30[7:0]	MAP_DST_8[7:0]							
0x95F	0x00	MIPI_TX31[7:0]	MAP_SRC_9[7:0]							
0x960	0x00	MIPI_TX32[7:0]	MAP_DST_9[7:0]							
0x961	0x00	MIPI_TX33[7:0]	MAP_SRC_10[7:0]							
0x962	0x00	MIPI_TX34[7:0]	MAP_DST_10[7:0]							
0x963	0x00	MIPI_TX35[7:0]	MAP_SRC_11[7:0]							
0x964	0x00	MIPI_TX36[7:0]	MAP_DST_11[7:0]							
0x965	0x00	MIPI_TX37[7:0]	MAP_SRC_12[7:0]							
0x966	0x00	MIPI_TX38[7:0]	MAP_DST_12[7:0]							
0x967	0x00	MIPI_TX39[7:0]	MAP_SRC_13[7:0]							
0x968	0x00	MIPI_TX40[7:0]	MAP_DST_13[7:0]							
0x969	0x00	MIPI_TX41[7:0]	MAP_SRC_14[7:0]							
0x96A	0x00	MIPI_TX42[7:0]	MAP_DST_14[7:0]							
0x96B	0x00	MIPI_TX43[7:0]	MAP_SRC_15[7:0]							
0x96C	0x00	MIPI_TX44[7:0]	MAP_DST_15[7:0]							
0x96D	0x00	MIPI_TX45[7:0]	MAP_DPHY_DEST_3[1:0]		MAP_DPHY_DEST_2[1:0]		MAP_DPHY_DEST_1[1:0]		MAP_DPHY_DEST_0[1:0]	
0x96E	0x00	MIPI_TX46[7:0]	MAP_DPHY_DEST_7[1:0]		MAP_DPHY_DEST_6[1:0]		MAP_DPHY_DEST_5[1:0]		MAP_DPHY_DEST_4[1:0]	
0x96F	0x00	MIPI_TX47[7:0]	MAP_DPHY_DEST_11[1:0]		MAP_DPHY_DEST_10[1:0]		MAP_DPHY_DEST_9[1:0]		MAP_DPHY_DEST_8[1:0]	
0x970	0x00	MIPI_TX48[7:0]	MAP_DPHY_DEST_15[1:0]		MAP_DPHY_DEST_14[1:0]		MAP_DPHY_DEST_13[1:0]		MAP_DPHY_DEST_12[1:0]	
0x971	0x00	MIPI_TX49[7:0]	MAP_CON[7:0]							
0x972	0x00	MIPI_TX50[7:0]	SKEW_PER_SEL[7:0]							
0x973	0x00	MIPI_TX51[7:0]	–	–	–	ALT2_MEM_MAP8	MODE_DT	ALT_MEM_MAP10	ALT_MEM_MAP8	ALT_MEM_MAP12
0x974	0x00	MIPI_TX52[7:0]	video_masked_latched[3:0]				video_masked[3:0]			
MIPI_TX 2										
0x981	0x00	MIPI_TX1[7:0]	MODE[7:0]							

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ADDRESS	RESET	NAME	MSB							LSB
0x982	0x00	MIPI_TX2[7:0]	STATUS[7:0]							
0x983	0x00	MIPI_TX3[7:0]	DESKEW_INIT[7:0]							
0x984	0x00	MIPI_TX4[7:0]	DESKEW_PER[7:0]							
0x985	0x71	MIPI_TX5[7:0]	CSI2_T_PRE[7:0]							
0x986	0x19	MIPI_TX6[7:0]	CSI2_T_POST[7:0]							
0x987	0x1C	MIPI_TX7[7:0]	CSI2_TX_GAP[7:0]							
0x988	0x00	MIPI_TX8[7:0]	CSI2_TWAKEUP_L[7:0]							
0x989	0x01	MIPI_TX9[7:0]	CSI2_TWAKEUP_M[7:0]							
0x98A	0xC0	MIPI_TX10[7:0]	CSI2_LANE_CNT[1:0]		CSI2_CPHY_EN	csi2_vcx_en	–	CSI2_TWAKEUP_H[2:0]		
0x98B	0x00	MIPI_TX11[7:0]	MAP_EN_L[7:0]							
0x98C	0x00	MIPI_TX12[7:0]	MAP_EN_H[7:0]							
0x98D	0x00	MIPI_TX13[7:0]	MAP_SRC_0[7:0]							
0x98E	0x00	MIPI_TX14[7:0]	MAP_DST_0[7:0]							
0x98F	0x00	MIPI_TX15[7:0]	MAP_SRC_1[7:0]							
0x990	0x00	MIPI_TX16[7:0]	MAP_DST_1[7:0]							
0x991	0x00	MIPI_TX17[7:0]	MAP_SRC_2[7:0]							
0x992	0x00	MIPI_TX18[7:0]	MAP_DST_2[7:0]							
0x993	0x00	MIPI_TX19[7:0]	MAP_SRC_3[7:0]							
0x994	0x00	MIPI_TX20[7:0]	MAP_DST_3[7:0]							
0x995	0x00	MIPI_TX21[7:0]	MAP_SRC_4[7:0]							
0x996	0x00	MIPI_TX22[7:0]	MAP_DST_4[7:0]							
0x997	0x00	MIPI_TX23[7:0]	MAP_SRC_5[7:0]							
0x998	0x00	MIPI_TX24[7:0]	MAP_DST_5[7:0]							
0x999	0x00	MIPI_TX25[7:0]	MAP_SRC_6[7:0]							
0x99A	0x00	MIPI_TX26[7:0]	MAP_DST_6[7:0]							
0x99B	0x00	MIPI_TX27[7:0]	MAP_SRC_7[7:0]							
0x99C	0x00	MIPI_TX28[7:0]	MAP_DST_7[7:0]							
0x99D	0x00	MIPI_TX29[7:0]	MAP_SRC_8[7:0]							

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ADDRESS	RESET	NAME	MSB							LSB
0x99E	0x00	MIPI_TX30[7:0]	MAP_DST_8[7:0]							
0x99F	0x00	MIPI_TX31[7:0]	MAP_SRC_9[7:0]							
0x9A0	0x00	MIPI_TX32[7:0]	MAP_DST_9[7:0]							
0x9A1	0x00	MIPI_TX33[7:0]	MAP_SRC_10[7:0]							
0x9A2	0x00	MIPI_TX34[7:0]	MAP_DST_10[7:0]							
0x9A3	0x00	MIPI_TX35[7:0]	MAP_SRC_11[7:0]							
0x9A4	0x00	MIPI_TX36[7:0]	MAP_DST_11[7:0]							
0x9A5	0x00	MIPI_TX37[7:0]	MAP_SRC_12[7:0]							
0x9A6	0x00	MIPI_TX38[7:0]	MAP_DST_12[7:0]							
0x9A7	0x00	MIPI_TX39[7:0]	MAP_SRC_13[7:0]							
0x9A8	0x00	MIPI_TX40[7:0]	MAP_DST_13[7:0]							
0x9A9	0x00	MIPI_TX41[7:0]	MAP_SRC_14[7:0]							
0x9AA	0x00	MIPI_TX42[7:0]	MAP_DST_14[7:0]							
0x9AB	0x00	MIPI_TX43[7:0]	MAP_SRC_15[7:0]							
0x9AC	0x00	MIPI_TX44[7:0]	MAP_DST_15[7:0]							
0x9AD	0x00	MIPI_TX45[7:0]	MAP_DPHY_DEST_3[1:0]		MAP_DPHY_DEST_2[1:0]		MAP_DPHY_DEST_1[1:0]		MAP_DPHY_DEST_0[1:0]	
0x9AE	0x00	MIPI_TX46[7:0]	MAP_DPHY_DEST_7[1:0]		MAP_DPHY_DEST_6[1:0]		MAP_DPHY_DEST_5[1:0]		MAP_DPHY_DEST_4[1:0]	
0x9AF	0x00	MIPI_TX47[7:0]	MAP_DPHY_DEST_11[1:0]		MAP_DPHY_DEST_10[1:0]		MAP_DPHY_DEST_9[1:0]		MAP_DPHY_DEST_8[1:0]	
0x9B0	0x00	MIPI_TX48[7:0]	MAP_DPHY_DEST_15[1:0]		MAP_DPHY_DEST_14[1:0]		MAP_DPHY_DEST_13[1:0]		MAP_DPHY_DEST_12[1:0]	
0x9B1	0x00	MIPI_TX49[7:0]	MAP_CON[7:0]							
0x9B2	0x00	MIPI_TX50[7:0]	SKEW_PER_SEL[7:0]							
0x9B3	0x00	MIPI_TX51[7:0]	–	–	–	ALT2_MEM_MAP8	MODE_DT	ALT_MEM_MAP10	ALT_MEM_MAP8	ALT_MEM_MAP12
0x9B4	0x00	MIPI_TX52[7:0]	video_masked_latched[3:0]				video_masked[3:0]			
MIPI_TX 3										
0x9C1	0x00	MIPI_TX1[7:0]	MODE[7:0]							

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ADDRESS	RESET	NAME	MSB							LSB
0x9C2	0x00	MIPI_TX2[7:0]	STATUS[7:0]							
0x9C3	0x00	MIPI_TX3[7:0]	DESKEW_INIT[7:0]							
0x9C4	0x00	MIPI_TX4[7:0]	DESKEW_PER[7:0]							
0x9C5	0x71	MIPI_TX5[7:0]	CSI2_T_PRE[7:0]							
0x9C6	0x19	MIPI_TX6[7:0]	CSI2_T_POST[7:0]							
0x9C7	0x1C	MIPI_TX7[7:0]	CSI2_TX_GAP[7:0]							
0x9C8	0x00	MIPI_TX8[7:0]	CSI2_TWAKEUP_L[7:0]							
0x9C9	0x01	MIPI_TX9[7:0]	CSI2_TWAKEUP_M[7:0]							
0x9CA	0xC0	MIPI_TX10[7:0]	CSI2_LANE_CNT[1:0]		CSI2_CPHY_EN	csi2_vcx_en	–	CSI2_TWAKEUP_H[2:0]		
0x9CB	0x00	MIPI_TX11[7:0]	MAP_EN_L[7:0]							
0x9CC	0x00	MIPI_TX12[7:0]	MAP_EN_H[7:0]							
0x9CD	0x00	MIPI_TX13[7:0]	MAP_SRC_0[7:0]							
0x9CE	0x00	MIPI_TX14[7:0]	MAP_DST_0[7:0]							
0x9CF	0x00	MIPI_TX15[7:0]	MAP_SRC_1[7:0]							
0x9D0	0x00	MIPI_TX16[7:0]	MAP_DST_1[7:0]							
0x9D1	0x00	MIPI_TX17[7:0]	MAP_SRC_2[7:0]							
0x9D2	0x00	MIPI_TX18[7:0]	MAP_DST_2[7:0]							
0x9D3	0x00	MIPI_TX19[7:0]	MAP_SRC_3[7:0]							
0x9D4	0x00	MIPI_TX20[7:0]	MAP_DST_3[7:0]							
0x9D5	0x00	MIPI_TX21[7:0]	MAP_SRC_4[7:0]							
0x9D6	0x00	MIPI_TX22[7:0]	MAP_DST_4[7:0]							
0x9D7	0x00	MIPI_TX23[7:0]	MAP_SRC_5[7:0]							
0x9D8	0x00	MIPI_TX24[7:0]	MAP_DST_5[7:0]							
0x9D9	0x00	MIPI_TX25[7:0]	MAP_SRC_6[7:0]							
0x9DA	0x00	MIPI_TX26[7:0]	MAP_DST_6[7:0]							
0x9DB	0x00	MIPI_TX27[7:0]	MAP_SRC_7[7:0]							
0x9DC	0x00	MIPI_TX28[7:0]	MAP_DST_7[7:0]							
0x9DD	0x00	MIPI_TX29[7:0]	MAP_SRC_8[7:0]							

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ADDRESS	RESET	NAME	MSB							LSB
0x9DE	0x00	MIPI_TX30[7:0]	MAP_DST_8[7:0]							
0x9DF	0x00	MIPI_TX31[7:0]	MAP_SRC_9[7:0]							
0x9E0	0x00	MIPI_TX32[7:0]	MAP_DST_9[7:0]							
0x9E1	0x00	MIPI_TX33[7:0]	MAP_SRC_10[7:0]							
0x9E2	0x00	MIPI_TX34[7:0]	MAP_DST_10[7:0]							
0x9E3	0x00	MIPI_TX35[7:0]	MAP_SRC_11[7:0]							
0x9E4	0x00	MIPI_TX36[7:0]	MAP_DST_11[7:0]							
0x9E5	0x00	MIPI_TX37[7:0]	MAP_SRC_12[7:0]							
0x9E6	0x00	MIPI_TX38[7:0]	MAP_DST_12[7:0]							
0x9E7	0x00	MIPI_TX39[7:0]	MAP_SRC_13[7:0]							
0x9E8	0x00	MIPI_TX40[7:0]	MAP_DST_13[7:0]							
0x9E9	0x00	MIPI_TX41[7:0]	MAP_SRC_14[7:0]							
0x9EA	0x00	MIPI_TX42[7:0]	MAP_DST_14[7:0]							
0x9EB	0x00	MIPI_TX43[7:0]	MAP_SRC_15[7:0]							
0x9EC	0x00	MIPI_TX44[7:0]	MAP_DST_15[7:0]							
0x9ED	0x00	MIPI_TX45[7:0]	MAP_DPHY_DEST_3[1:0]		MAP_DPHY_DEST_2[1:0]		MAP_DPHY_DEST_1[1:0]		MAP_DPHY_DEST_0[1:0]	
0x9EE	0x00	MIPI_TX46[7:0]	MAP_DPHY_DEST_7[1:0]		MAP_DPHY_DEST_6[1:0]		MAP_DPHY_DEST_5[1:0]		MAP_DPHY_DEST_4[1:0]	
0x9EF	0x00	MIPI_TX47[7:0]	MAP_DPHY_DEST_11[1:0]		MAP_DPHY_DEST_10[1:0]		MAP_DPHY_DEST_9[1:0]		MAP_DPHY_DEST_8[1:0]	
0x9F0	0x00	MIPI_TX48[7:0]	MAP_DPHY_DEST_15[1:0]		MAP_DPHY_DEST_14[1:0]		MAP_DPHY_DEST_13[1:0]		MAP_DPHY_DEST_12[1:0]	
0x9F1	0x00	MIPI_TX49[7:0]	MAP_CON[7:0]							
0x9F2	0x00	MIPI_TX50[7:0]	SKEW_PER_SEL[7:0]							
0x9F3	0x00	MIPI_TX51[7:0]	–	–	–	ALT2_MEM_MAP8	MODE_DT	ALT_MEM_MAP10	ALT_MEM_MAP8	ALT_MEM_MAP12
0x9F4	0x00	MIPI_TX52[7:0]	video_masked_latched[3:0]				video_masked[3:0]			
MIPI_TX 4										
0xA0B	0x00	MIPI_TX11[7:0]	MAP_EN_L[7:0]							

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0xA0C	0x00	MIPI_TX12[7:0]	MAP_EN_H[7:0]							
0xA0D	0x00	MIPI_TX13[7:0]	MAP_SRC_0[7:0]							
0xA0E	0x00	MIPI_TX14[7:0]	MAP_DST_0[7:0]							
0xA0F	0x00	MIPI_TX15[7:0]	MAP_SRC_1[7:0]							
0xA10	0x00	MIPI_TX16[7:0]	MAP_DST_1[7:0]							
0xA11	0x00	MIPI_TX17[7:0]	MAP_SRC_2[7:0]							
0xA12	0x00	MIPI_TX18[7:0]	MAP_DST_2[7:0]							
0xA13	0x00	MIPI_TX19[7:0]	MAP_SRC_3[7:0]							
0xA14	0x00	MIPI_TX20[7:0]	MAP_DST_3[7:0]							
0xA15	0x00	MIPI_TX21[7:0]	MAP_SRC_4[7:0]							
0xA16	0x00	MIPI_TX22[7:0]	MAP_DST_4[7:0]							
0xA17	0x00	MIPI_TX23[7:0]	MAP_SRC_5[7:0]							
0xA18	0x00	MIPI_TX24[7:0]	MAP_DST_5[7:0]							
0xA19	0x00	MIPI_TX25[7:0]	MAP_SRC_6[7:0]							
0xA1A	0x00	MIPI_TX26[7:0]	MAP_DST_6[7:0]							
0xA1B	0x00	MIPI_TX27[7:0]	MAP_SRC_7[7:0]							
0xA1C	0x00	MIPI_TX28[7:0]	MAP_DST_7[7:0]							
0xA1D	0x00	MIPI_TX29[7:0]	MAP_SRC_8[7:0]							
0xA1E	0x00	MIPI_TX30[7:0]	MAP_DST_8[7:0]							
0xA1F	0x00	MIPI_TX31[7:0]	MAP_SRC_9[7:0]							
0xA20	0x00	MIPI_TX32[7:0]	MAP_DST_9[7:0]							
0xA21	0x00	MIPI_TX33[7:0]	MAP_SRC_10[7:0]							
0xA22	0x00	MIPI_TX34[7:0]	MAP_DST_10[7:0]							
0xA23	0x00	MIPI_TX35[7:0]	MAP_SRC_11[7:0]							
0xA24	0x00	MIPI_TX36[7:0]	MAP_DST_11[7:0]							

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ADDRESS	RESET	NAME	MSB							LSB
0xA25	0x00	MIPI_TX37[7:0]	MAP_SRC_12[7:0]							
0xA26	0x00	MIPI_TX38[7:0]	MAP_DST_12[7:0]							
0xA27	0x00	MIPI_TX39[7:0]	MAP_SRC_13[7:0]							
0xA28	0x00	MIPI_TX40[7:0]	MAP_DST_13[7:0]							
0xA29	0x00	MIPI_TX41[7:0]	MAP_SRC_14[7:0]							
0xA2A	0x00	MIPI_TX42[7:0]	MAP_DST_14[7:0]							
0xA2B	0x00	MIPI_TX43[7:0]	MAP_SRC_15[7:0]							
0xA2C	0x00	MIPI_TX44[7:0]	MAP_DST_15[7:0]							
0xA2D	0x00	MIPI_TX45[7:0]	MAP_DPHY_DEST_3[1:0]		MAP_DPHY_DEST_2[1:0]		MAP_DPHY_DEST_1[1:0]		MAP_DPHY_DEST_0[1:0]	
0xA2E	0x00	MIPI_TX46[7:0]	MAP_DPHY_DEST_7[1:0]		MAP_DPHY_DEST_6[1:0]		MAP_DPHY_DEST_5[1:0]		MAP_DPHY_DEST_4[1:0]	
0xA2F	0x00	MIPI_TX47[7:0]	MAP_DPHY_DEST_11[1:0]		MAP_DPHY_DEST_10[1:0]		MAP_DPHY_DEST_9[1:0]		MAP_DPHY_DEST_8[1:0]	
0xA30	0x00	MIPI_TX48[7:0]	MAP_DPHY_DEST_15[1:0]		MAP_DPHY_DEST_14[1:0]		MAP_DPHY_DEST_13[1:0]		MAP_DPHY_DEST_12[1:0]	
0xA31	0x00	MIPI_TX49[7:0]	–	–	–	–	MODE_DT	ALT_MEM_MAP10	ALT_MEM_MAP8	ALT_MEM_MAP12
MIPI_TX 5										
0xA4B	0x00	MIPI_TX11[7:0]	MAP_EN_L[7:0]							
0xA4C	0x00	MIPI_TX12[7:0]	MAP_EN_H[7:0]							
0xA4D	0x00	MIPI_TX13[7:0]	MAP_SRC_0[7:0]							
0xA4E	0x00	MIPI_TX14[7:0]	MAP_DST_0[7:0]							
0xA4F	0x00	MIPI_TX15[7:0]	MAP_SRC_1[7:0]							
0xA50	0x00	MIPI_TX16[7:0]	MAP_DST_1[7:0]							
0xA51	0x00	MIPI_TX17[7:0]	MAP_SRC_2[7:0]							
0xA52	0x00	MIPI_TX18[7:0]	MAP_DST_2[7:0]							
0xA53	0x00	MIPI_TX19[7:0]	MAP_SRC_3[7:0]							
0xA54	0x00	MIPI_TX20[7:0]	MAP_DST_3[7:0]							
0xA55	0x00	MIPI_TX21[7:0]	MAP_SRC_4[7:0]							

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ADDRESS	RESET	NAME	MSB							LSB
0xA56	0x00	MIPI_TX22[7:0]	MAP_DST_4[7:0]							
0xA57	0x00	MIPI_TX23[7:0]	MAP_SRC_5[7:0]							
0xA58	0x00	MIPI_TX24[7:0]	MAP_DST_5[7:0]							
0xA59	0x00	MIPI_TX25[7:0]	MAP_SRC_6[7:0]							
0xA5A	0x00	MIPI_TX26[7:0]	MAP_DST_6[7:0]							
0xA5B	0x00	MIPI_TX27[7:0]	MAP_SRC_7[7:0]							
0xA5C	0x00	MIPI_TX28[7:0]	MAP_DST_7[7:0]							
0xA5D	0x00	MIPI_TX29[7:0]	MAP_SRC_8[7:0]							
0xA5E	0x00	MIPI_TX30[7:0]	MAP_DST_8[7:0]							
0xA5F	0x00	MIPI_TX31[7:0]	MAP_SRC_9[7:0]							
0xA60	0x00	MIPI_TX32[7:0]	MAP_DST_9[7:0]							
0xA61	0x00	MIPI_TX33[7:0]	MAP_SRC_10[7:0]							
0xA62	0x00	MIPI_TX34[7:0]	MAP_DST_10[7:0]							
0xA63	0x00	MIPI_TX35[7:0]	MAP_SRC_11[7:0]							
0xA64	0x00	MIPI_TX36[7:0]	MAP_DST_11[7:0]							
0xA65	0x00	MIPI_TX37[7:0]	MAP_SRC_12[7:0]							
0xA66	0x00	MIPI_TX38[7:0]	MAP_DST_12[7:0]							
0xA67	0x00	MIPI_TX39[7:0]	MAP_SRC_13[7:0]							
0xA68	0x00	MIPI_TX40[7:0]	MAP_DST_13[7:0]							
0xA69	0x00	MIPI_TX41[7:0]	MAP_SRC_14[7:0]							
0xA6A	0x00	MIPI_TX42[7:0]	MAP_DST_14[7:0]							
0xA6B	0x00	MIPI_TX43[7:0]	MAP_SRC_15[7:0]							
0xA6C	0x00	MIPI_TX44[7:0]	MAP_DST_15[7:0]							
0xA6D	0x00	MIPI_TX45[7:0]	MAP_DPHY_DEST_3[1:0]		MAP_DPHY_DEST_2[1:0]		MAP_DPHY_DEST_1[1:0]		MAP_DPHY_DEST_0[1:0]	
0xA6E	0x00	MIPI_TX46[7:0]	MAP_DPHY_DEST_7[1:0]		MAP_DPHY_DEST_6[1:0]		MAP_DPHY_DEST_5[1:0]		MAP_DPHY_DEST_4[1:0]	

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0xA6F	0x00	MIPI_TX47[7:0]	MAP_DPHY_DEST_11[1:0]		MAP_DPHY_DEST_10[1:0]		MAP_DPHY_DEST_9[1:0]		MAP_DPHY_DEST_8[1:0]	
0xA70	0x00	MIPI_TX48[7:0]	MAP_DPHY_DEST_15[1:0]		MAP_DPHY_DEST_14[1:0]		MAP_DPHY_DEST_13[1:0]		MAP_DPHY_DEST_12[1:0]	
0xA71	0x00	MIPI_TX49[7:0]	–	–	–	–	MODE_DT	ALT_MEM_MAP10	ALT_MEM_MAP8	ALT_MEM_MAP12
MIPI_TX 6										
0xA8B	0x00	MIPI_TX11[7:0]	MAP_EN_L[7:0]							
0xA8C	0x00	MIPI_TX12[7:0]	MAP_EN_H[7:0]							
0xA8D	0x00	MIPI_TX13[7:0]	MAP_SRC_0[7:0]							
0xA8E	0x00	MIPI_TX14[7:0]	MAP_DST_0[7:0]							
0xA8F	0x00	MIPI_TX15[7:0]	MAP_SRC_1[7:0]							
0xA90	0x00	MIPI_TX16[7:0]	MAP_DST_1[7:0]							
0xA91	0x00	MIPI_TX17[7:0]	MAP_SRC_2[7:0]							
0xA92	0x00	MIPI_TX18[7:0]	MAP_DST_2[7:0]							
0xA93	0x00	MIPI_TX19[7:0]	MAP_SRC_3[7:0]							
0xA94	0x00	MIPI_TX20[7:0]	MAP_DST_3[7:0]							
0xA95	0x00	MIPI_TX21[7:0]	MAP_SRC_4[7:0]							
0xA96	0x00	MIPI_TX22[7:0]	MAP_DST_4[7:0]							
0xA97	0x00	MIPI_TX23[7:0]	MAP_SRC_5[7:0]							
0xA98	0x00	MIPI_TX24[7:0]	MAP_DST_5[7:0]							
0xA99	0x00	MIPI_TX25[7:0]	MAP_SRC_6[7:0]							
0xA9A	0x00	MIPI_TX26[7:0]	MAP_DST_6[7:0]							
0xA9B	0x00	MIPI_TX27[7:0]	MAP_SRC_7[7:0]							
0xA9C	0x00	MIPI_TX28[7:0]	MAP_DST_7[7:0]							
0xA9D	0x00	MIPI_TX29[7:0]	MAP_SRC_8[7:0]							
0xA9E	0x00	MIPI_TX30[7:0]	MAP_DST_8[7:0]							
0xA9F	0x00	MIPI_TX31[7:0]	MAP_SRC_9[7:0]							

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ADDRESS	RESET	NAME	MSB							LSB
0xAA0	0x00	MIPI_TX32[7:0]	MAP_DST_9[7:0]							
0xAA1	0x00	MIPI_TX33[7:0]	MAP_SRC_10[7:0]							
0xAA2	0x00	MIPI_TX34[7:0]	MAP_DST_10[7:0]							
0xAA3	0x00	MIPI_TX35[7:0]	MAP_SRC_11[7:0]							
0xAA4	0x00	MIPI_TX36[7:0]	MAP_DST_11[7:0]							
0xAA5	0x00	MIPI_TX37[7:0]	MAP_SRC_12[7:0]							
0xAA6	0x00	MIPI_TX38[7:0]	MAP_DST_12[7:0]							
0xAA7	0x00	MIPI_TX39[7:0]	MAP_SRC_13[7:0]							
0xAA8	0x00	MIPI_TX40[7:0]	MAP_DST_13[7:0]							
0xAA9	0x00	MIPI_TX41[7:0]	MAP_SRC_14[7:0]							
0xAAA	0x00	MIPI_TX42[7:0]	MAP_DST_14[7:0]							
0xAAB	0x00	MIPI_TX43[7:0]	MAP_SRC_15[7:0]							
0xAAC	0x00	MIPI_TX44[7:0]	MAP_DST_15[7:0]							
0xAAD	0x00	MIPI_TX45[7:0]	MAP_DPHY_DEST_3[1:0]		MAP_DPHY_DEST_2[1:0]		MAP_DPHY_DEST_1[1:0]		MAP_DPHY_DEST_0[1:0]	
0xAAE	0x00	MIPI_TX46[7:0]	MAP_DPHY_DEST_7[1:0]		MAP_DPHY_DEST_6[1:0]		MAP_DPHY_DEST_5[1:0]		MAP_DPHY_DEST_4[1:0]	
0xAAF	0x00	MIPI_TX47[7:0]	MAP_DPHY_DEST_11[1:0]		MAP_DPHY_DEST_10[1:0]		MAP_DPHY_DEST_9[1:0]		MAP_DPHY_DEST_8[1:0]	
0xAB0	0x00	MIPI_TX48[7:0]	MAP_DPHY_DEST_15[1:0]		MAP_DPHY_DEST_14[1:0]		MAP_DPHY_DEST_13[1:0]		MAP_DPHY_DEST_12[1:0]	
0xAB1	0x00	MIPI_TX49[7:0]	–	–	–	–	MODE_DT	ALT_MEM_MAP10	ALT_MEM_MAP8	ALT_MEM_MAP12
MIPI_TX 7										
0xACB	0x00	MIPI_TX11[7:0]	MAP_EN_L[7:0]							
0xACC	0x00	MIPI_TX12[7:0]	MAP_EN_H[7:0]							
0xACD	0x00	MIPI_TX13[7:0]	MAP_SRC_0[7:0]							
0xACE	0x00	MIPI_TX14[7:0]	MAP_DST_0[7:0]							
0xACF	0x00	MIPI_TX15[7:0]	MAP_SRC_1[7:0]							
0xAD0	0x00	MIPI_TX16[7:0]	MAP_DST_1[7:0]							

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0xAD1	0x00	MIPI_TX17[7:0]	MAP_SRC_2[7:0]							
0xAD2	0x00	MIPI_TX18[7:0]	MAP_DST_2[7:0]							
0xAD3	0x00	MIPI_TX19[7:0]	MAP_SRC_3[7:0]							
0xAD4	0x00	MIPI_TX20[7:0]	MAP_DST_3[7:0]							
0xAD5	0x00	MIPI_TX21[7:0]	MAP_SRC_4[7:0]							
0xAD6	0x00	MIPI_TX22[7:0]	MAP_DST_4[7:0]							
0xAD7	0x00	MIPI_TX23[7:0]	MAP_SRC_5[7:0]							
0xAD8	0x00	MIPI_TX24[7:0]	MAP_DST_5[7:0]							
0xAD9	0x00	MIPI_TX25[7:0]	MAP_SRC_6[7:0]							
0xADA	0x00	MIPI_TX26[7:0]	MAP_DST_6[7:0]							
0xADB	0x00	MIPI_TX27[7:0]	MAP_SRC_7[7:0]							
0xADC	0x00	MIPI_TX28[7:0]	MAP_DST_7[7:0]							
0xADD	0x00	MIPI_TX29[7:0]	MAP_SRC_8[7:0]							
0xADE	0x00	MIPI_TX30[7:0]	MAP_DST_8[7:0]							
0xADF	0x00	MIPI_TX31[7:0]	MAP_SRC_9[7:0]							
0xAE0	0x00	MIPI_TX32[7:0]	MAP_DST_9[7:0]							
0xAE1	0x00	MIPI_TX33[7:0]	MAP_SRC_10[7:0]							
0xAE2	0x00	MIPI_TX34[7:0]	MAP_DST_10[7:0]							
0xAE3	0x00	MIPI_TX35[7:0]	MAP_SRC_11[7:0]							
0xAE4	0x00	MIPI_TX36[7:0]	MAP_DST_11[7:0]							
0xAE5	0x00	MIPI_TX37[7:0]	MAP_SRC_12[7:0]							
0xAE6	0x00	MIPI_TX38[7:0]	MAP_DST_12[7:0]							
0xAE7	0x00	MIPI_TX39[7:0]	MAP_SRC_13[7:0]							
0xAE8	0x00	MIPI_TX40[7:0]	MAP_DST_13[7:0]							
0xAE9	0x00	MIPI_TX41[7:0]	MAP_SRC_14[7:0]							

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ADDRESS	RESET	NAME	MSB							LSB
0xAEA	0x00	MIPI_TX42[7:0]	MAP_DST_14[7:0]							
0xAEB	0x00	MIPI_TX43[7:0]	MAP_SRC_15[7:0]							
0xAEC	0x00	MIPI_TX44[7:0]	MAP_DST_15[7:0]							
0xAED	0x00	MIPI_TX45[7:0]	MAP_DPHY_DEST_3[1:0]		MAP_DPHY_DEST_2[1:0]		MAP_DPHY_DEST_1[1:0]		MAP_DPHY_DEST_0[1:0]	
0xAEE	0x00	MIPI_TX46[7:0]	MAP_DPHY_DEST_7[1:0]		MAP_DPHY_DEST_6[1:0]		MAP_DPHY_DEST_5[1:0]		MAP_DPHY_DEST_4[1:0]	
0xAEF	0x00	MIPI_TX47[7:0]	MAP_DPHY_DEST_11[1:0]		MAP_DPHY_DEST_10[1:0]		MAP_DPHY_DEST_9[1:0]		MAP_DPHY_DEST_8[1:0]	
0xAF0	0x00	MIPI_TX48[7:0]	MAP_DPHY_DEST_15[1:0]		MAP_DPHY_DEST_14[1:0]		MAP_DPHY_DEST_13[1:0]		MAP_DPHY_DEST_12[1:0]	
0xAF1	0x00	MIPI_TX49[7:0]	–	–	–	–	MODE_DT	ALT_MEM_MAP10	ALT_MEM_MAP8	ALT_MEM_MAP12
GMSL1 A										
0xB02	0x03	GMSL1_2[7:0]	–	–	–	–	–	–	RSVD[1:0]	
0xB04	0x03	GMSL1_4[7:0]	–	–	PRBSEN	CC_PORT_SEL[1:0]		–	RSVD	FWDCCEN
0xB05	0x39	GMSL1_5[7:0]	I2CMETHOD	NO_REM_MST	HVTR_MODE	EN_EQ	EQTUNE[3:0]			
0xB06	0x6F	GMSL1_6[7:0]	HIGHIMM	MAX_RT_EN	I2C_RT_EN	GPI_COMP_EN	GPI_RT_EN	HV_SRC[2:0]		
0xB07	0x00	GMSL1_7[7:0]	DBL	DRS	BWS	–	HIBW	HVEN	–	PXL_CRC
0xB08	0x21	GMSL1_8[7:0]	GPI_SEL[1:0]		GPI_EN	EN_FSYNC_TX	–	PKTCC_EN	CC_CRC_LENGTH[1:0]	
0xB0D	0x00	GMSL1_D[7:0]	I2C_LOC_ACK	RSVD	–	–	–	HS_TRACK_FSYNC	RSVD	RSVD
0xB0E	0x00	GMSL1_E[7:0]	DET_THR[7:0]							
0xB0F	0x09	GMSL1_F[7:0]	–	EN_DE_FILT	EN_HS_FILT	EN_VS_FILT	DE_EN	–	–	PRBS_TYPE
0xB10	0x02	GMSL1_10[7:0]	RCEG_TYPE[1:0]		RCEG_BOUND	RCEG_ERR_NUM[3:0]				RCEG_EN
0xB11	0xF0	GMSL1_11[7:0]	RCEG_ERR_RATE[3:0]				RCEG_LO_BST_PRB[1:0]		RCEG_LO_BST_LEN[1:0]	
0xB12	0x52	GMSL1_12[7:0]	UNDERBST_DET_EN	CC_CRC_ERR_EN	LINE_CRC_LOC[1:0]		LINE_CRC_EN_GMSL1	–	MAX_RT_ERR_EN	RCEG_ERR_PER_EN
0xB13	0xC0	GMSL1_13[7:0]	EOM_EN_G1	EOM_PER_MODE_G1	EOM_MAN_TRG_REQ_G1	EOM_MIN_THR_G1[4:0]				

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0xB14	0x80	GMSL1_14[7:0]	AEQ_EN	AEQ_PER_MODE	AEQ_MAN_TRG_REQ	EOM_PER_THR[4:0]				
0xB15	0x00	GMSL1_15[7:0]	DET_ERR[7:0]							
0xB16	0x00	GMSL1_16[7:0]	PRBS_ERR[7:0]							
0xB17	0x00	GMSL1_17[7:0]	RSVD	MAX_RT_ERR_I2C	PRBS_OK	GPI_IN	MAX_RT_ERR_GPI	–	–	–
0xB18	0x00	GMSL1_18[7:0]	CC_RETR_CNT[7:0]							
0xB19	0x00	GMSL1_19[7:0]	CC_CRC_ERRCNT[7:0]							
0xB1A	0x00	GMSL1_1A[7:0]	RCEG_ERR_CNT[7:0]							
0xB1B	0x00	GMSL1_1B[7:0]	–	–	–	–	–	LINE_CRC_ERR	–	–
0xB1C	0x00	GMSL1_1C[7:0]	–	–	EOM_EYE_WIDTH[5:0]					
0xB1D	0x00	GMSL1_1D[7:0]	–	–	–	UNDER BOOST_DET	AEQ_BST[3:0]			
0xB20	0x00	GMSL1_20[7:0]	CRC_VALUE_0[7:0]							
0xB21	0x00	GMSL1_21[7:0]	CRC_VALUE_1[7:0]							
0xB22	0x00	GMSL1_22[7:0]	CRC_VALUE_2[7:0]							
0xB23	0x00	GMSL1_23[7:0]	CRC_VALUE_3[7:0]							
0xB96	0x01	GMSL1_96[7:0]	CONV_GMSL1_DATATYPE[4:0]					RSVD	CONV_GMSL1_EN	RSVD
0xBA7	0x05	GMSL1_A7[7:0]	RSVD	SHIFT_VID_HVD	RSVD	–	RSVD[3:0]			
0xBCB	0x00	GMSL1_CB[7:0]	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	LOCKED_G1
0xBD1	0x00	GMSL1_D1[7:0]	CNTL_OUT_ORD[2:0]			CNTL_OUT_EN[4:0]				
GMSL1 B										
0xC02	0x03	GMSL1_2[7:0]	–	–	–	–	–	–	RSVD[1:0]	
0xC04	0x03	GMSL1_4[7:0]	–	–	PRBSEN	CC_PORT_SEL[1:0]		–	RSVD	FWDCCEN
0xC05	0x39	GMSL1_5[7:0]	I2CMETHOD	NO_REM_MST	HVTR_MODE	EN_EQ	EQTUNE[3:0]			
0xC06	0x6F	GMSL1_6[7:0]	HIGHIMM	MAX_RT_EN	I2C_RT_EN	GPI_COMP_EN	GPI_RT_EN	HV_SRC[2:0]		

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ADDRESS	RESET	NAME	MSB							LSB
0xC07	0x00	GMSL1_7[7:0]	DBL	DRS	BWS	–	HIBW	HVEN	–	PXL_CRC
0xC08	0x21	GMSL1_8[7:0]	GPI_SEL[1:0]		GPI_EN	EN_FSYNC_TX	–	PKTCC_EN	CC_CRC_LENGTH[1:0]	
0xC0D	0x00	GMSL1_D[7:0]	I2C_LOC_ACK	RSVD	–	–	–	HS_TRACK_FSYNC	RSVD	RSVD
0xC0E	0x00	GMSL1_E[7:0]	DET_THR[7:0]							
0xC0F	0x09	GMSL1_F[7:0]	–	EN_DE_FILT	EN_HS_FILT	EN_VS_FILT	DE_EN	–	–	PRBS_TYPE
0xC10	0x02	GMSL1_10[7:0]	RCEG_TYPE[1:0]		RCEG_BOUND	RCEG_ERR_NUM[3:0]				RCEG_EN
0xC11	0xF0	GMSL1_11[7:0]	RCEG_ERR_RATE[3:0]				RCEG_LO_BST_PRB[1:0]		RCEG_LO_BST_LEN[1:0]	
0xC12	0x52	GMSL1_12[7:0]	UNDERBST_DET_EN	CC_CRC_ERR_EN	LINE_CRC_LOC[1:0]		LINE_CRC_EN_GMSL1	–	MAX_RT_ERR_EN	RCEG_ERR_PER_EN
0xC13	0xC0	GMSL1_13[7:0]	EOM_EN_G1	EOM_PER_MODE_G1	EOM_MAN_TRG_REQ_G1	EOM_MIN_THR_G1[4:0]				
0xC14	0x80	GMSL1_14[7:0]	AEQ_EN	AEQ_PER_MODE	AEQ_MAN_TRG_REQ	EOM_PER_THR[4:0]				
0xC15	0x00	GMSL1_15[7:0]	DET_ERR[7:0]							
0xC16	0x00	GMSL1_16[7:0]	PRBS_ERR[7:0]							
0xC17	0x00	GMSL1_17[7:0]	RSVD	MAX_RT_ERR_I2C	PRBS_OK	GPI_IN	MAX_RT_ERR_GPI	–	–	–
0xC18	0x00	GMSL1_18[7:0]	CC_RETR_CNT[7:0]							
0xC19	0x00	GMSL1_19[7:0]	CC_CRC_ERRCNT[7:0]							
0xC1A	0x00	GMSL1_1A[7:0]	RCEG_ERR_CNT[7:0]							
0xC1B	0x00	GMSL1_1B[7:0]	–	–	–	–	–	LINE_CRC_ERR	–	–
0xC1C	0x00	GMSL1_1C[7:0]	–	–	EOM_EYE_WIDTH[5:0]					
0xC1D	0x00	GMSL1_1D[7:0]	–	–	–	UNDERBOOST_DET	AEQ_BST[3:0]			
0xC20	0x00	GMSL1_20[7:0]	CRC_VALUE_0[7:0]							
0xC21	0x00	GMSL1_21[7:0]	CRC_VALUE_1[7:0]							
0xC22	0x00	GMSL1_22[7:0]	CRC_VALUE_2[7:0]							

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ADDRESS	RESET	NAME	MSB							LSB
0xC23	0x00	GMSL1_23[7:0]	CRC_VALUE_3[7:0]							
0xC96	0x01	GMSL1_96[7:0]	CONV_GMSL1_DATATYPE[4:0]					RSVD	CONV_GMSL1_EN	RSVD
0xCA7	0x05	GMSL1_A7[7:0]	RSVD	SHIFT_VID_HVD	RSVD	–	RSVD[3:0]			
0xCCB	0x00	GMSL1_CB[7:0]	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	LOCKED_G1
0xCD1	0x00	GMSL1_D1[7:0]	CNTL_OUT_ORD[2:0]			CNTL_OUT_EN[4:0]				
GMSL1 C										
0xD02	0x03	GMSL1_2[7:0]	–	–	–	–	–	–	RSVD[1:0]	
0xD04	0x03	GMSL1_4[7:0]	–	–	PRBSEN	CC_PORT_SEL[1:0]		–	RSVD	FWDCCEN
0xD05	0x39	GMSL1_5[7:0]	I2CMETHOD	NO_REM_MST	HVTR_MODE	EN_EQ	EQTUNE[3:0]			
0xD06	0x6F	GMSL1_6[7:0]	HIGHIMM	MAX_RT_EN	I2C_RT_EN	GPI_COMP_EN	GPI_RT_EN	HV_SRC[2:0]		
0xD07	0x00	GMSL1_7[7:0]	DBL	DRS	BWS	–	HIBW	HVEN	–	PXL_CRC
0xD08	0x21	GMSL1_8[7:0]	GPI_SEL[1:0]		GPI_EN	EN_FSYNC_TX	–	PKTCC_EN	CC_CRC_LENGTH[1:0]	
0xD0D	0x00	GMSL1_D[7:0]	I2C_LOC_ACK	RSVD	–	–	–	HS_TRACK_FSYNC	RSVD	RSVD
0xD0E	0x00	GMSL1_E[7:0]	DET_THR[7:0]							
0xD0F	0x09	GMSL1_F[7:0]	–	EN_DE_FILT	EN_HS_FILT	EN_VS_FILT	DE_EN	–	–	PRBS_TYPE
0xD10	0x02	GMSL1_10[7:0]	RCEG_TYPE[1:0]		RCEG_BOUND	RCEG_ERR_NUM[3:0]				RCEG_EN
0xD11	0xF0	GMSL1_11[7:0]	RCEG_ERR_RATE[3:0]				RCEG_LO_BST_PRB[1:0]		RCEG_LO_BST_LEN[1:0]	
0xD12	0x52	GMSL1_12[7:0]	UNDERBST_DET_EN	CC_CRC_ERR_EN	LINE_CRC_LOC[1:0]		LINE_CRC_EN_GMSL1	–	MAX_RT_ERR_EN	RCEG_ERR_PER_EN
0xD13	0xC0	GMSL1_13[7:0]	EOM_EN_G1	EOM_PER_MODE_G1	EOM_MAN_TRG_REQ_G1	EOM_MIN_THR_G1[4:0]				
0xD14	0x80	GMSL1_14[7:0]	AEQ_EN	AEQ_PER_MODE	AEQ_MAN_TRG_REQ	EOM_PER_THR[4:0]				
0xD15	0x00	GMSL1_15[7:0]	DET_ERR[7:0]							
0xD16	0x00	GMSL1_16[7:0]	PRBS_ERR[7:0]							

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ADDRESS	RESET	NAME	MSB							LSB
0xD17	0x00	GMSL1_17[7:0]	RSVD	MAX_RT_ERR_I2C	PRBS_OK	GPI_IN	MAX_RT_ERR_GPI	–	–	–
0xD18	0x00	GMSL1_18[7:0]	CC_RETR_CNT[7:0]							
0xD19	0x00	GMSL1_19[7:0]	CC_CRC_ERRCNT[7:0]							
0xD1A	0x00	GMSL1_1A[7:0]	RCEG_ERR_CNT[7:0]							
0xD1B	0x00	GMSL1_1B[7:0]	–	–	–	–	–	LINE_CRC_ERR	–	–
0xD1C	0x00	GMSL1_1C[7:0]	–	–	EOM_EYE_WIDTH[5:0]					
0xD1D	0x00	GMSL1_1D[7:0]	–	–	–	UNDER BOOST_DET	AEQ_BST[3:0]			
0xD20	0x00	GMSL1_20[7:0]	CRC_VALUE_0[7:0]							
0xD21	0x00	GMSL1_21[7:0]	CRC_VALUE_1[7:0]							
0xD22	0x00	GMSL1_22[7:0]	CRC_VALUE_2[7:0]							
0xD23	0x00	GMSL1_23[7:0]	CRC_VALUE_3[7:0]							
0xD96	0x01	GMSL1_96[7:0]	CONV_GMSL1_DATATYPE[4:0]					RSVD	CONV_GMSL1_EN	RSVD
0xDA7	0x05	GMSL1_A7[7:0]	RSVD	SHIFT_VID_HVD	RSVD	–	RSVD[3:0]			
0xDCB	0x00	GMSL1_CB[7:0]	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	LOCKED_G1
0xDD1	0x00	GMSL1_D1[7:0]	CNTL_OUT_ORD[2:0]			CNTL_OUT_EN[4:0]				
GMSL1 D										
0xE02	0x03	GMSL1_2[7:0]	–	–	–	–	–	–	RSVD[1:0]	
0xE04	0x03	GMSL1_4[7:0]	–	–	PRBSEN	CC_PORT_SEL[1:0]		–	RSVD	FWDCCEN
0xE05	0x39	GMSL1_5[7:0]	I2CMETHOD	NO_REM_MST	HVTR_MODE	EN_EQ	EQTUNE[3:0]			
0xE06	0x6F	GMSL1_6[7:0]	HIGHIMM	MAX_RT_EN	I2C_RT_EN	GPI_COMP_EN	GPI_RT_EN	HV_SRC[2:0]		
0xE07	0x00	GMSL1_7[7:0]	DBL	DRS	BWS	–	HIBW	HVEN	–	PXL_CRC
0xE08	0x21	GMSL1_8[7:0]	GPI_SEL[1:0]		GPI_EN	EN_FSYNC_TX	–	PKTCC_EN	CC_CRC_LENGTH[1:0]	
0xE0D	0x00	GMSL1_D[7:0]	I2C_LOC_ACK	RSVD	–	–	–	HS_TRACK_FSYNC	RSVD	RSVD

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0xE0E	0x00	GMSL1_E[7:0]	DET_THR[7:0]							
0xE0F	0x09	GMSL1_F[7:0]	–	EN_DE_FILT	EN_HS_FILT	EN_VS_FILT	DE_EN	–	–	PRBS_TYPE
0xE10	0x02	GMSL1_10[7:0]	RCEG_TYPE[1:0]		RCEG_BOUND	RCEG_ERR_NUM[3:0]				RCEG_EN
0xE11	0xF0	GMSL1_11[7:0]	RCEG_ERR_RATE[3:0]				RCEG_LO_BST_PRB[1:0]		RCEG_LO_BST_LEN[1:0]	
0xE12	0x52	GMSL1_12[7:0]	UNDERBST_DET_EN	CC_CRC_ERR_EN	LINE_CRC_LOC[1:0]		LINE_CRC_EN_GMSL1	–	MAX_RT_ERR_EN	RCEG_ERR_PER_EN
0xE13	0xC0	GMSL1_13[7:0]	EOM_EN_G1	EOM_PER_MODE_G1	EOM_MAN_TRG_REQ_G1	EOM_MIN_THR_G1[4:0]				
0xE14	0x80	GMSL1_14[7:0]	AEQ_EN	AEQ_PER_MODE	AEQ_MAN_TRG_REQ	EOM_PER_THR[4:0]				
0xE15	0x00	GMSL1_15[7:0]	DET_ERR[7:0]							
0xE16	0x00	GMSL1_16[7:0]	PRBS_ERR[7:0]							
0xE17	0x00	GMSL1_17[7:0]	RSVD	MAX_RT_ERR_I2C	PRBS_OK	GPI_IN	MAX_RT_ERR_GPI	–	–	–
0xE18	0x00	GMSL1_18[7:0]	CC_RETR_CNT[7:0]							
0xE19	0x00	GMSL1_19[7:0]	CC_CRC_ERRCNT[7:0]							
0xE1A	0x00	GMSL1_1A[7:0]	RCEG_ERR_CNT[7:0]							
0xE1B	0x00	GMSL1_1B[7:0]	–	–	–	–	–	LINE_CRC_ERR	–	–
0xE1C	0x00	GMSL1_1C[7:0]	–	–	EOM_EYE_WIDTH[5:0]					
0xE1D	0x00	GMSL1_1D[7:0]	–	–	–	UNDERBOOST_DET	AEQ_BST[3:0]			
0xE20	0x00	GMSL1_20[7:0]	CRC_VALUE_0[7:0]							
0xE21	0x00	GMSL1_21[7:0]	CRC_VALUE_1[7:0]							
0xE22	0x00	GMSL1_22[7:0]	CRC_VALUE_2[7:0]							
0xE23	0x00	GMSL1_23[7:0]	CRC_VALUE_3[7:0]							
0xE96	0x01	GMSL1_96[7:0]	CONV_GMSL1_DATATYPE[4:0]					RSVD	CONV_GMSL1_EN	RSVD
0xEA7	0x05	GMSL1_A7[7:0]	RSVD	SHIFT_VID_HVD	RSVD	–	RSVD[3:0]			

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0xECB	0x00	GMSL1_CB[7:0]	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	LOCKED_G1
0xED1	0x00	GMSL1_D1[7:0]	CNTL_OUT_ORD[2:0]			CNTL_OUT_EN[4:0]				
GMSL A										
0x1001	0x00	TX1[7:0]	RSVD	–	–	ERRG_EN	–	–	RSVD	RSVD
0x1002	0x20	TX2[7:0]	ERRG_CNT[1:0]		ERRG_RATE[1:0]		ERRG_BURST[2:0]			ERRG_PER
0x1003	0x44	TX3[7:0]	RSVD[1:0]		–	–	–	TIMEOUT[2:0]		
0x1004	0x00	RX0[7:0]	PKT_CNT_LBW[1:0]		–	RSVD	PKT_CNT_SEL[3:0]			
0x1008	0x41	GPIOA[7:0]	RSVD	RSVD	GPIO_FWD_CDLY[5:0]					
0x1009	0x88	GPIOB[7:0]	GPIO_TX_WNDW[1:0]		GPIO_REV_CDLY[5:0]					
GMSL B										
0x1011	0x00	TX1[7:0]	RSVD	–	–	ERRG_EN	–	–	RSVD	RSVD
0x1012	0x20	TX2[7:0]	ERRG_CNT[1:0]		ERRG_RATE[1:0]		ERRG_BURST[2:0]			ERRG_PER
0x1013	0x44	TX3[7:0]	RSVD[1:0]		–	–	–	TIMEOUT[2:0]		
0x1014	0x00	RX0[7:0]	PKT_CNT_LBW[1:0]		–	RSVD	PKT_CNT_SEL[3:0]			
0x1018	0x41	GPIOA[7:0]	RSVD	RSVD	GPIO_FWD_CDLY[5:0]					
0x1019	0x88	GPIOB[7:0]	GPIO_TX_WNDW[1:0]		GPIO_REV_CDLY[5:0]					
GMSL C										
0x1021	0x00	TX1[7:0]	RSVD	–	–	ERRG_EN	–	–	RSVD	RSVD
0x1022	0x20	TX2[7:0]	ERRG_CNT[1:0]		ERRG_RATE[1:0]		ERRG_BURST[2:0]			ERRG_PER
0x1023	0x44	TX3[7:0]	RSVD[1:0]		–	–	–	TIMEOUT[2:0]		
0x1024	0x00	RX0[7:0]	PKT_CNT_LBW[1:0]		–	RSVD	PKT_CNT_SEL[3:0]			
0x1028	0x41	GPIOA[7:0]	RSVD	RSVD	GPIO_FWD_CDLY[5:0]					
0x1029	0x88	GPIOB[7:0]	GPIO_TX_WNDW[1:0]		GPIO_REV_CDLY[5:0]					
GMSL D										
0x1031	0x00	TX1[7:0]	RSVD	–	–	ERRG_EN	–	–	RSVD	RSVD
0x1032	0x20	TX2[7:0]	ERRG_CNT[1:0]		ERRG_RATE[1:0]		ERRG_BURST[2:0]			ERRG_PER
0x1033	0x44	TX3[7:0]	RSVD[1:0]		–	–	–	TIMEOUT[2:0]		
0x1034	0x00	RX0[7:0]	PKT_CNT_LBW[1:0]		–	RSVD	PKT_CNT_SEL[3:0]			
0x1038	0x41	GPIOA[7:0]	RSVD	RSVD	GPIO_FWD_CDLY[5:0]					
0x1039	0x88	GPIOB[7:0]	GPIO_TX_WNDW[1:0]		GPIO_REV_CDLY[5:0]					
VRX_PATGEN_0 0										
0x1050	0x03	PATGEN_0[7:0]	GEN_VS	GEN_HS	GEN_DE	VS_INV	HS_INV	DE_INV	VTG_MODE[1:0]	

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ADDRESS	RESET	NAME	MSB							LSB
0x1051	0x00	PATGEN_1[7:0]	GRAD_MODE	–	PATGEN_MODE[1:0]		–	–	–	VS_TRIG
0x1052	0x00	VS_DLY_2[7:0]	VS_DLY_2[7:0]							
0x1053	0x00	VS_DLY_1[7:0]	VS_DLY_1[7:0]							
0x1054	0x00	VS_DLY_0[7:0]	VS_DLY_0[7:0]							
0x1055	0x00	VS_HIGH_2[7:0]	VS_HIGH_2[7:0]							
0x1056	0x00	VS_HIGH_1[7:0]	VS_HIGH_1[7:0]							
0x1057	0x00	VS_HIGH_0[7:0]	VS_HIGH_0[7:0]							
0x1058	0x00	VS_LOW_2[7:0]	VS_LOW_2[7:0]							
0x1059	0x00	VS_LOW_1[7:0]	VS_LOW_1[7:0]							
0x105A	0x00	VS_LOW_0[7:0]	VS_LOW_0[7:0]							
0x105B	0x00	V2H_2[7:0]	V2H_2[7:0]							
0x105C	0x00	V2H_1[7:0]	V2H_1[7:0]							
0x105D	0x00	V2H_0[7:0]	V2H_0[7:0]							
0x105E	0x00	HS_HIGH_1[7:0]	HS_HIGH_1[7:0]							
0x105F	0x00	HS_HIGH_0[7:0]	HS_HIGH_0[7:0]							
0x1060	0x00	HS_LOW_1[7:0]	HS_LOW_1[7:0]							
0x1061	0x00	HS_LOW_0[7:0]	HS_LOW_0[7:0]							
0x1062	0x00	HS_CNT_1[7:0]	HS_CNT_1[7:0]							
0x1063	0x00	HS_CNT_0[7:0]	HS_CNT_0[7:0]							
0x1064	0x00	V2D_2[7:0]	V2D_2[7:0]							
0x1065	0x00	V2D_1[7:0]	V2D_1[7:0]							
0x1066	0x00	V2D_0[7:0]	V2D_0[7:0]							
0x1067	0x00	DE_HIGH_1[7:0]	DE_HIGH_1[7:0]							
0x1068	0x00	DE_HIGH_0[7:0]	DE_HIGH_0[7:0]							
0x1069	0x00	DE_LOW_1[7:0]	DE_LOW_1[7:0]							
0x106A	0x00	DE_LOW_0[7:0]	DE_LOW_0[7:0]							
0x106B	0x00	DE_CNT_1[7:0]	DE_CNT_1[7:0]							

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ADDRESS	RESET	NAME	MSB							LSB
0x106C	0x00	DE_CNT_0[7:0]	DE_CNT_0[7:0]							
0x106D	0x00	GRAD_INCR[7:0]	GRAD_INCR[7:0]							
0x106E	0x00	CHKR_COLOR_A_L[7:0]	CHKR_COLOR_A_L[7:0]							
0x106F	0x00	CHKR_COLOR_A_M[7:0]	CHKR_COLOR_A_M[7:0]							
0x1070	0x00	CHKR_COLOR_A_H[7:0]	CHKR_COLOR_A_H[7:0]							
0x1071	0x00	CHKR_COLOR_B_L[7:0]	CHKR_COLOR_B_L[7:0]							
0x1072	0x00	CHKR_COLOR_B_M[7:0]	CHKR_COLOR_B_M[7:0]							
0x1073	0x00	CHKR_COLOR_B_H[7:0]	CHKR_COLOR_B_H[7:0]							
0x1074	0x00	CHKR_RPT_A[7:0]	CHKR_RPT_A[7:0]							
0x1075	0x00	CHKR_RPT_B[7:0]	CHKR_RPT_B[7:0]							
0x1076	0x00	CHKR_ALT[7:0]	CHKR_ALT[7:0]							
VRX_PATGEN_0 1										
0x1080	0x03	PATGEN_0[7:0]	GEN_VS	GEN_HS	GEN_DE	VS_INV	HS_INV	DE_INV	VTG_MODE[1:0]	
0x1081	0x00	PATGEN_1[7:0]	GRAD_MODE	–	PATGEN_MODE[1:0]		–	–	–	VS_TRIG
0x1082	0x00	VS_DLY_2[7:0]	VS_DLY_2[7:0]							
0x1083	0x00	VS_DLY_1[7:0]	VS_DLY_1[7:0]							
0x1084	0x00	VS_DLY_0[7:0]	VS_DLY_0[7:0]							
0x1085	0x00	VS_HIGH_2[7:0]	VS_HIGH_2[7:0]							
0x1086	0x00	VS_HIGH_1[7:0]	VS_HIGH_1[7:0]							
0x1087	0x00	VS_HIGH_0[7:0]	VS_HIGH_0[7:0]							
0x1088	0x00	VS_LOW_2[7:0]	VS_LOW_2[7:0]							
0x1089	0x00	VS_LOW_1[7:0]	VS_LOW_1[7:0]							
0x108A	0x00	VS_LOW_0[7:0]	VS_LOW_0[7:0]							
0x108B	0x00	V2H_2[7:0]	V2H_2[7:0]							
0x108C	0x00	V2H_1[7:0]	V2H_1[7:0]							
0x108D	0x00	V2H_0[7:0]	V2H_0[7:0]							

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ADDRESS	RESET	NAME	MSB							LSB
0x108E	0x00	HS_HIGH_1[7:0]	HS_HIGH_1[7:0]							
0x108F	0x00	HS_HIGH_0[7:0]	HS_HIGH_0[7:0]							
0x1090	0x00	HS_LOW_1[7:0]	HS_LOW_1[7:0]							
0x1091	0x00	HS_LOW_0[7:0]	HS_LOW_0[7:0]							
0x1092	0x00	HS_CNT_1[7:0]	HS_CNT_1[7:0]							
0x1093	0x00	HS_CNT_0[7:0]	HS_CNT_0[7:0]							
0x1094	0x00	V2D_2[7:0]	V2D_2[7:0]							
0x1095	0x00	V2D_1[7:0]	V2D_1[7:0]							
0x1096	0x00	V2D_0[7:0]	V2D_0[7:0]							
0x1097	0x00	DE_HIGH_1[7:0]	DE_HIGH_1[7:0]							
0x1098	0x00	DE_HIGH_0[7:0]	DE_HIGH_0[7:0]							
0x1099	0x00	DE_LOW_1[7:0]	DE_LOW_1[7:0]							
0x109A	0x00	DE_LOW_0[7:0]	DE_LOW_0[7:0]							
0x109B	0x00	DE_CNT_1[7:0]	DE_CNT_1[7:0]							
0x109C	0x00	DE_CNT_0[7:0]	DE_CNT_0[7:0]							
0x109D	0x00	GRAD_INCR[7:0]	GRAD_INCR[7:0]							
0x109E	0x00	CHKR_COLOR_A_L[7:0]	CHKR_COLOR_A_L[7:0]							
0x109F	0x00	CHKR_COLOR_A_M[7:0]	CHKR_COLOR_A_M[7:0]							
0x10A0	0x00	CHKR_COLOR_A_H[7:0]	CHKR_COLOR_A_H[7:0]							
0x10A1	0x00	CHKR_COLOR_B_L[7:0]	CHKR_COLOR_B_L[7:0]							
0x10A2	0x00	CHKR_COLOR_B_M[7:0]	CHKR_COLOR_B_M[7:0]							
0x10A3	0x00	CHKR_COLOR_B_H[7:0]	CHKR_COLOR_B_H[7:0]							
0x10A4	0x00	CHKR_RPT_A[7:0]	CHKR_RPT_A[7:0]							
0x10A5	0x00	CHKR_RPT_B[7:0]	CHKR_RPT_B[7:0]							
0x10A6	0x00	CHKR_ALT[7:0]	CHKR_ALT[7:0]							
VID_PXL_CRC_ERR										
0x11D0	0x00	CNT_AX[7:0]	VID_PXL_CRC_ERR_AX[7:0]							

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ADDRESS	RESET	NAME	MSB							LSB
0x11D1	0x00	CNT_AY[7:0]	VID_PXL_CRC_ERR_AY[7:0]							
0x11D2	0x00	CNT_AZ[7:0]	VID_PXL_CRC_ERR_AZ[7:0]							
0x11E0	0x00	CNT_AU[7:0]	VID_PXL_CRC_ERR_AU[7:0]							
0x11E1	0x00	CNT_BX[7:0]	VID_PXL_CRC_ERR_BX[7:0]							
0x11E2	0x00	CNT_BY[7:0]	VID_PXL_CRC_ERR_BY[7:0]							
0x11E3	0x00	CNT_BZ[7:0]	VID_PXL_CRC_ERR_BZ[7:0]							
0x11E4	0x00	CNT_BU[7:0]	VID_PXL_CRC_ERR_BU[7:0]							
0x11E5	0x00	CNT_CX[7:0]	VID_PXL_CRC_ERR_CX[7:0]							
0x11E6	0x00	CNT_CY[7:0]	VID_PXL_CRC_ERR_CY[7:0]							
0x11E7	0x00	CNT_CZ[7:0]	VID_PXL_CRC_ERR_CZ[7:0]							
0x11E8	0x00	CNT_CU[7:0]	VID_PXL_CRC_ERR_CU[7:0]							
0x11E9	0x00	CNT_DX[7:0]	VID_PXL_CRC_ERR_DX[7:0]							
0x11EA	0x00	CNT_DY[7:0]	VID_PXL_CRC_ERR_DY[7:0]							
0x11EB	0x00	CNT_DZ[7:0]	VID_PXL_CRC_ERR_DZ[7:0]							
0x11EC	0x00	CNT_DU[7:0]	VID_PXL_CRC_ERR_DU[7:0]							
VID_HVD_DET										
0x11F0	0x00	DE_DET[7:0]	DE_DET_7	DE_DET_6	DE_DET_5	DE_DET_4	DE_DET_3	DE_DET_2	DE_DET_1	DE_DET_0
0x11F1	0x00	HS_DET[7:0]	HS_DET_7	HS_DET_6	HS_DET_5	HS_DET_4	HS_DET_3	HS_DET_2	HS_DET_1	HS_DET_0
0x11F2	0x00	VS_DET[7:0]	VS_DET_7	VS_DET_6	VS_DET_5	VS_DET_4	VS_DET_3	VS_DET_2	VS_DET_1	VS_DET_0
0x11F3	0x00	HS_POL[7:0]	HS_POL_7	HS_POL_6	HS_POL_5	HS_POL_4	HS_POL_3	HS_POL_2	HS_POL_1	HS_POL_0
0x11F4	0x00	VS_POL[7:0]	VS_POL_7	VS_POL_6	VS_POL_5	VS_POL_4	VS_POL_3	VS_POL_2	VS_POL_1	VS_POL_0
WM										
0x1200	0x00	WM_0[7:0]	WM_LEN	WM_MODE[2:0]			WM_DET[1:0]		–	WM_EN
0x1201	0x59	WM_1[7:0]	RSVD[1:0]		WM_KO[1:0]		RSVD[3:0]			
0x1202	0x50	WM_2[7:0]	–	RSVD[2:0]			HsyncPol	VsyncPol	WM_NPFILT[1:0]	
0x1203	0x14	WM_3[7:0]	–	WM_TH[6:0]						
0x1204	0x10	WM_4[7:0]	–	–	RSVD[1:0]		RSVD	–	WM_MASKMODE[1:0]	
0x1205	0x00	WM_5[7:0]	–	–	–	–	–	RSVD	WM_DETOUT	WM_ERROR
0x1206	0x00	WM_6[7:0]	WM_TIMER[7:0]							
0x121E	0x00	WM_WREN_0[7:0]	WM_WREN_L[7:0]							
0x121F	0x00	WM_WREN_1[7:0]	WM_WREN_H[7:0]							
WM1										
0x1220	0x00	WM_0[7:0]	WM1_LEN	WM1_MODE[2:0]			WM1_DET[1:0]		–	WM1_EN
0x1221	0x59	WM_1[7:0]	RSVD[1:0]		WM1_KO[1:0]		RSVD[3:0]			

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ADDRESS	RESET	NAME	MSB							LSB
0x1222	0x50	WM_2[7:0]	–	RSVD[2:0]			HsyncPol1	VsyncPol1	RSVD[1:0]	
0x1224	0x10	WM_4[7:0]	–	–	WM1_YUV_IN[1:0]		WM1_COLORADJ	–	WM1_MASKMODE[1:0]	
0x1225	0x00	WM_5[7:0]	–	–	–	–	–	RSVD	WM1_DETOUT	WM1_ERROR
0x1226	0x00	WM_6[7:0]	WM1_TIMER[7:0]							
0x123E	0x00	WM_WREN_0[7:0]	WM1_WREN_L[7:0]							
0x123F	0x00	WM_WREN_1[7:0]	WM1_WREN_H[7:0]							
MEM_ECC										
0x1250	0x00	MEM_ECC0[7:0]	MEM_ECC_ERR2_THR[2:0]			MEM_ECC_ERR1_THR[2:0]			RESET_MEM_ECC_ERR2_CNT	RESET_MEM_ECC_ERR1_CNT
0x1251	0x00	MEM_ECC1[7:0]	MEM_ECC_ERR1_CNT[7:0]							
0x1252	0x00	MEM_ECC2[7:0]	MEM_ECC_ERR2_CNT[7:0]							
0x1253	0x00	MEM_ECC_ERR_DEBUG[7:0]	–	–	–	–	–	–	MEM_INJ_E2A	MEM_INJ_E1A
0x1254	0x00	MEM_ECC_ERR_FLAG[7:0]	BACKTOP8_ECC_ERR_FLAG	BACKTOP7_ECC_ERR_FLAG	BACKTOP6_ECC_ERR_FLAG	BACKTOP5_ECC_ERR_FLAG	BACKTOP4_ECC_ERR_FLAG	BACKTOP3_ECC_ERR_FLAG	BACKTOP2_ECC_ERR_FLAG	BACKTOP1_ECC_ERR_FLAG
SPARE_SIGNALS										
0x12A1	0x00	SPARE_DIGITAL[7:0]	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RESET_MEM_FLUSH	BACKTOP_ECC_ERR_SEL
RLMS A										
0x1403	0x0A	RLMS3[7:0]	AdaptEn	RSVD	RSVD	RSVD	RSVD	–	RSVD[1:0]	
0x1404	0x4B	RLMS4[7:0]	EOM_CHK_AMOUNT[3:0]				EOM_CHK_THR[1:0]		EOM_PER_MODE	EOM_EN
0x1405	0x10	RLMS5[7:0]	EOM_MAN_TRG_REQ	EOM_MIN_THR[6:0]						
0x1406	0x80	RLMS6[7:0]	EOM_PV_MODE	EOM_RST_THR[6:0]						
0x1407	0x00	RLMS7[7:0]	EOM_DONE	EOM[6:0]						
0x1434	0x00	RLMS34[7:0]	EyeMonPerCntL[7:0]							
0x1435	0x00	RLMS35[7:0]	EyeMonPerCntH[7:0]							
0x1437	0x00	RLMS37[7:0]	–	RSVD	RSVD	EyeMonDone	EyeMonCntClr	EyeMonStart	EyeMonPh	EyeMonDPol
0x1438	0x00	RLMS38[7:0]	EyeMonErrCntL[7:0]							

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ADDRESS	RESET	NAME	MSB							LSB
0x1439	0x00	RLMS39[7:0]	EyeMonErrCntH[7:0]							
0x143A	0x00	RLMS3A[7:0]	EyeMonValCntL[7:0]							
0x143B	0x00	RLMS3B[7:0]	EyeMonValCntH[7:0]							
0x143D	0x01	RLMS3D[7:0]	ErrChPh[6:0]							ErrChPh TogEn
0x143E	0xB3	RLMS3E[7:0]	ErrChPh SecTA	ErrChPhSec[6:0]						
0x143F	0x72	RLMS3F[7:0]	ErrChPh PriTA	ErrChPhPri[6:0]						
0x1445	0x01	RLMS45[7:0]	RSVD	RSVD	–	–	–	RSVD[2:0]		
0x1449	0x71	RLMS49[7:0]	–	RSVD	RSVD	RSVD	RSVD	ErrChPw rUp	–	RSVD
0x1458	0x28	RLMS58[7:0]	–	ErrChVTh1[6:0]						
0x1459	0x68	RLMS59[7:0]	–	ErrChVTh0[6:0]						
0x1464	0x00	RLMS64[7:0]	–	–	–	–	–	RSVD	TxSSCMode[1:0]	
0x1470	0x01	RLMS70[7:0]	–	TxSSCFrqCtrl[6:0]						
0x1471	0x02	RLMS71[7:0]	–	TxSSCCenSprSt[5:0]						TxSSCE n
0x1472	0xCF	RLMS72[7:0]	TxSSCPreSclL[7:0]							
0x1473	0x00	RLMS73[7:0]	–	–	–	–	–	TxSSCPreSclH[2:0]		
0x1474	0x00	RLMS74[7:0]	TxSSCPhL[7:0]							
0x1475	0x00	RLMS75[7:0]	–	TxSSCPhH[6:0]						
0x1476	0x00	RLMS76[7:0]	–	–	–	–	–	–	TxSSCPhQuad[1:0]	
0x1495	0x69	RLMS95[7:0]	TxAmpl ManEn	RSVD	TxAmplMan[5:0]					
0x1498	0x40	RLMS98[7:0]	RSVD	RSVD	RSVD[2:0]			Rxhpf_cnt[2:0]		
0x14A4	0xBD	RLMSA4[7:0]	AEQ_PER_MULT[1:0]	AEQ_PER[5:0]						
0x14AC	0xCD	RLMSAC[7:0]	ErrChPh SecTAF R3G	ErrChPhSecFR3G[6:0]						
0x14AD	0x0D	RLMSAD[7:0]	ErrChPh PriTAFR 3G	ErrChPhPriFR3G[6:0]						
0x14B6	0xBB	RLMSB6[7:0]	ErrChPh SecTAS RG1875	ErrChPhSecSRG1875[6:0]						
0x14B7	0x7A	RLMSB7[7:0]	ErrChPh PriTASR G1875	ErrChPhPriSRG1875[6:0]						
0x14C4	0x40	RLMSC4[7:0]	RevTrfM anEn	RevTrfMan[2:0]			–	RevFast	–	–
0x14C5	0x40	RLMSC5[7:0]	RevLen ManEn	RevFLenMan[6:0]						
0x14D1	0x88	RLMSD1[7:0]	RSVD[2:0]			RSVD[2:0]			RSVD	RSVD
RLMS B										
0x1503	0x0A	RLMS3[7:0]	AdaptEn	RSVD	RSVD	RSVD	RSVD	–	RSVD[1:0]	

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ADDRESS	RESET	NAME	MSB							LSB
0x1504	0x4B	RLMS4[7:0]	EOM_CHK_AMOUNT[3:0]				EOM_CHK_THR[1:0]		EOM_PER_MODE	EOM_EN
0x1505	0x10	RLMS5[7:0]	EOM_MAN_TRG_REQ	EOM_MIN_THR[6:0]						
0x1506	0x80	RLMS6[7:0]	EOM_PV_MODE	EOM_RST_THR[6:0]						
0x1507	0x00	RLMS7[7:0]	EOM_DONE	EOM[6:0]						
0x1534	0x00	RLMS34[7:0]	EyeMonPerCntL[7:0]							
0x1535	0x00	RLMS35[7:0]	EyeMonPerCntH[7:0]							
0x1537	0x00	RLMS37[7:0]	–	RSVD	RSVD	EyeMonDone	EyeMonCntClr	EyeMonStart	EyeMonPh	EyeMonDPol
0x1538	0x00	RLMS38[7:0]	EyeMonErrCntL[7:0]							
0x1539	0x00	RLMS39[7:0]	EyeMonErrCntH[7:0]							
0x153A	0x00	RLMS3A[7:0]	EyeMonValCntL[7:0]							
0x153B	0x00	RLMS3B[7:0]	EyeMonValCntH[7:0]							
0x153D	0x01	RLMS3D[7:0]	ErrChPh[6:0]							ErrChPhTogEn
0x153E	0xB3	RLMS3E[7:0]	ErrChPhSecTA	ErrChPhSec[6:0]						
0x153F	0x72	RLMS3F[7:0]	ErrChPhPriTA	ErrChPhPri[6:0]						
0x1545	0x01	RLMS45[7:0]	RSVD	RSVD	–	–	–	RSVD[2:0]		
0x1549	0x71	RLMS49[7:0]	–	RSVD	RSVD	RSVD	RSVD	ErrChPwrUp	–	RSVD
0x1558	0x28	RLMS58[7:0]	–	ErrChVTh1[6:0]						
0x1559	0x68	RLMS59[7:0]	–	ErrChVTh0[6:0]						
0x1564	0x00	RLMS64[7:0]	–	–	–	–	–	RSVD	TxSSCMode[1:0]	
0x1570	0x01	RLMS70[7:0]	–	TxSSCFrqCtrl[6:0]						
0x1571	0x02	RLMS71[7:0]	–	TxSSCCenSprSt[5:0]						TxSSCEn
0x1572	0xCF	RLMS72[7:0]	TxSSCPreSclL[7:0]							
0x1573	0x00	RLMS73[7:0]	–	–	–	–	–	TxSSCPreSclH[2:0]		
0x1574	0x00	RLMS74[7:0]	TxSSCPhL[7:0]							
0x1575	0x00	RLMS75[7:0]	–	TxSSCPhH[6:0]						
0x1576	0x00	RLMS76[7:0]	–	–	–	–	–	–	TxSSCPhQuad[1:0]	
0x1595	0x69	RLMS95[7:0]	TxAmplManEn	RSVD	TxAmplMan[5:0]					
0x1598	0x40	RLMS98[7:0]	RSVD	RSVD	RSVD[2:0]			Rxhpf_cnt[2:0]		
0x15A4	0xBD	RLMSA4[7:0]	AEQ_PER_MULT[1:0]	AEQ_PER[5:0]						
0x15AC	0xCD	RLMSAC[7:0]	ErrChPhSecTAFR3G	ErrChPhSecFR3G[6:0]						

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ADDRESS	RESET	NAME	MSB							LSB
0x15AD	0x0D	RLMSAD[7:0]	ErrChPhPriTAFR3G	ErrChPhPriFR3G[6:0]						
0x15B6	0xBB	RLMSB6[7:0]	ErrChPhSecTASRG1875	ErrChPhSecSRG1875[6:0]						
0x15B7	0x7A	RLMSB7[7:0]	ErrChPhPriTASRG1875	ErrChPhPriSRG1875[6:0]						
0x15C4	0x40	RLMSC4[7:0]	RevTrfManEn	RevTrfMan[2:0]			–	RevFast	–	–
0x15C5	0x40	RLMSC5[7:0]	RevLenManEn	RevFLenMan[6:0]						
0x15D1	0x88	RLMSD1[7:0]	RSVD[2:0]			RSVD[2:0]			RSVD	RSVD
RLMS C										
0x1603	0x0A	RLMS3[7:0]	AdaptEn	RSVD	RSVD	RSVD	RSVD	–	RSVD[1:0]	
0x1604	0x4B	RLMS4[7:0]	EOM_CHK_AMOUNT[3:0]				EOM_CHK_THR[1:0]		EOM_PER_MODE	EOM_EN
0x1605	0x10	RLMS5[7:0]	EOM_MAN_TRG_REQ	EOM_MIN_THR[6:0]						
0x1606	0x80	RLMS6[7:0]	EOM_PV_MODE	EOM_RST_THR[6:0]						
0x1607	0x00	RLMS7[7:0]	EOM_DONE	EOM[6:0]						
0x1634	0x00	RLMS34[7:0]	EyeMonPerCntL[7:0]							
0x1635	0x00	RLMS35[7:0]	EyeMonPerCntH[7:0]							
0x1637	0x00	RLMS37[7:0]	–	RSVD	RSVD	EyeMonDone	EyeMonCntClr	EyeMonStart	EyeMonPh	EyeMonDPol
0x1638	0x00	RLMS38[7:0]	EyeMonErrCntL[7:0]							
0x1639	0x00	RLMS39[7:0]	EyeMonErrCntH[7:0]							
0x163A	0x00	RLMS3A[7:0]	EyeMonValCntL[7:0]							
0x163B	0x00	RLMS3B[7:0]	EyeMonValCntH[7:0]							
0x163D	0x01	RLMS3D[7:0]	ErrChPh[6:0]							ErrChPhTogEn
0x163E	0xB3	RLMS3E[7:0]	ErrChPhSecTA	ErrChPhSec[6:0]						
0x163F	0x72	RLMS3F[7:0]	ErrChPhPriTA	ErrChPhPri[6:0]						
0x1645	0x01	RLMS45[7:0]	RSVD	RSVD	–	–	–	RSVD[2:0]		
0x1649	0x71	RLMS49[7:0]	–	RSVD	RSVD	RSVD	RSVD	ErrChPwrUp	–	RSVD
0x1658	0x28	RLMS58[7:0]	–	ErrChVTh1[6:0]						
0x1659	0x68	RLMS59[7:0]	–	ErrChVTh0[6:0]						
0x1664	0x00	RLMS64[7:0]	–	–	–	–	–	RSVD	TxSSCMode[1:0]	
0x1670	0x01	RLMS70[7:0]	–	TxSSCFrqCtrl[6:0]						

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ADDRESS	RESET	NAME	MSB							LSB
0x1671	0x02	RLMS71[7:0]	–	TxSSCCenSprSt[5:0]						TxSSCEn
0x1672	0xCF	RLMS72[7:0]	TxSSCPreSclL[7:0]							
0x1673	0x00	RLMS73[7:0]	–	–	–	–	–	TxSSCPreSclH[2:0]		
0x1674	0x00	RLMS74[7:0]	TxSSCPhL[7:0]							
0x1675	0x00	RLMS75[7:0]	–	TxSSCPhH[6:0]						
0x1676	0x00	RLMS76[7:0]	–	–	–	–	–	–	TxSSCPhQuad[1:0]	
0x1695	0x69	RLMS95[7:0]	TxAmplManEn	RSVD	TxAmplMan[5:0]					
0x1698	0x40	RLMS98[7:0]	RSVD	RSVD	RSVD[2:0]			Rxhpf_cnt[2:0]		
0x16A4	0xBD	RLMSA4[7:0]	AEQ_PER_MULT[1:0]		AEQ_PER[5:0]					
0x16AC	0xCD	RLMSAC[7:0]	ErrChPhSecTAFR3G	ErrChPhSecFR3G[6:0]						
0x16AD	0x0D	RLMSAD[7:0]	ErrChPhPriTAFR3G	ErrChPhPriFR3G[6:0]						
0x16B6	0xBB	RLMSB6[7:0]	ErrChPhSecTASRG1875	ErrChPhSecSRG1875[6:0]						
0x16B7	0x7A	RLMSB7[7:0]	ErrChPhPriTASRG1875	ErrChPhPriSRG1875[6:0]						
0x16C4	0x40	RLMSC4[7:0]	RevTrfManEn	RevTrfMan[2:0]			–	RevFast	–	–
0x16C5	0x40	RLMSC5[7:0]	RevLenManEn	RevFLenMan[6:0]						
0x16D1	0x88	RLMSD1[7:0]	RSVD[2:0]			RSVD[2:0]			RSVD	RSVD
RLMS D										
0x1703	0x0A	RLMS3[7:0]	AdaptEn	RSVD	RSVD	RSVD	RSVD	–	RSVD[1:0]	
0x1704	0x4B	RLMS4[7:0]	EOM_CHK_AMOUNT[3:0]				EOM_CHK_THR[1:0]		EOM_PER_MODE	EOM_EN
0x1705	0x10	RLMS5[7:0]	EOM_MAN_TRG_REQ	EOM_MIN_THR[6:0]						
0x1706	0x80	RLMS6[7:0]	EOM_PV_MODE	EOM_RST_THR[6:0]						
0x1707	0x00	RLMS7[7:0]	EOM_DONE	EOM[6:0]						
0x1734	0x00	RLMS34[7:0]	EyeMonPerCntL[7:0]							
0x1735	0x00	RLMS35[7:0]	EyeMonPerCntH[7:0]							
0x1737	0x00	RLMS37[7:0]	–	RSVD	RSVD	EyeMonDone	EyeMonCntClr	EyeMonStart	EyeMonPh	EyeMonDPol
0x1738	0x00	RLMS38[7:0]	EyeMonErrCntL[7:0]							
0x1739	0x00	RLMS39[7:0]	EyeMonErrCntH[7:0]							
0x173A	0x00	RLMS3A[7:0]	EyeMonValCntL[7:0]							

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ADDRESS	RESET	NAME	MSB							LSB
0x173B	0x00	RLMS3B[7:0]	EyeMonValCntH[7:0]							
0x173D	0x01	RLMS3D[7:0]	ErrChPh[6:0]							ErrChPh TogEn
0x173E	0xB3	RLMS3E[7:0]	ErrChPh SecTA	ErrChPhSec[6:0]						
0x173F	0x72	RLMS3F[7:0]	ErrChPh PriTA	ErrChPhPri[6:0]						
0x1745	0x01	RLMS45[7:0]	RSVD	RSVD	–	–	–	RSVD[2:0]		
0x1749	0x71	RLMS49[7:0]	–	RSVD	RSVD	RSVD	RSVD	ErrChPw rUp	–	RSVD
0x1758	0x28	RLMS58[7:0]	–	ErrChVTh1[6:0]						
0x1759	0x68	RLMS59[7:0]	–	ErrChVTh0[6:0]						
0x1764	0x00	RLMS64[7:0]	–	–	–	–	–	RSVD	TxSSCMode[1:0]	
0x1770	0x01	RLMS70[7:0]	–	TxSSCFrqCtrl[6:0]						
0x1771	0x02	RLMS71[7:0]	–	TxSSCCenSprSt[5:0]						TxSSCE n
0x1772	0xCF	RLMS72[7:0]	TxSSCPreSclL[7:0]							
0x1773	0x00	RLMS73[7:0]	–	–	–	–	–	TxSSCPreSclH[2:0]		
0x1774	0x00	RLMS74[7:0]	TxSSCPhL[7:0]							
0x1775	0x00	RLMS75[7:0]	–	TxSSCPhH[6:0]						
0x1776	0x00	RLMS76[7:0]	–	–	–	–	–	–	TxSSCPhQuad[1:0]	
0x1795	0x69	RLMS95[7:0]	TxAmpl ManEn	RSVD	TxAmplMan[5:0]					
0x1798	0x40	RLMS98[7:0]	RSVD	RSVD	RSVD[2:0]			Rxhpf_cnt[2:0]		
0x17A4	0xBD	RLMSA4[7:0]	AEQ_PER_MULT[1:0]	AEQ_PER[5:0]						
0x17AC	0xCD	RLMSAC[7:0]	ErrChPh SecTAF R3G	ErrChPhSecFR3G[6:0]						
0x17AD	0x0D	RLMSAD[7:0]	ErrChPh PriTAFR 3G	ErrChPhPriFR3G[6:0]						
0x17B6	0xBB	RLMSB6[7:0]	ErrChPh SecTAS RG1875	ErrChPhSecSRG1875[6:0]						
0x17B7	0x7A	RLMSB7[7:0]	ErrChPh PriTASR G1875	ErrChPhPriSRG1875[6:0]						
0x17C4	0x40	RLMSC4[7:0]	RevTrfM anEn	RevTrfMan[2:0]			–	RevFast	–	–
0x17C5	0x40	RLMSC5[7:0]	RevLen ManEn	RevFLenMan[6:0]						
0x17D1	0x88	RLMSD1[7:0]	RSVD[2:0]			RSVD[2:0]			RSVD	RSVD
DPLL CSI1										
0x1C00	0xF5	DPLL_0[7:0]	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	config_s oft_rst_n

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ADDRESS	RESET	NAME	MSB							LSB
DPLL CSI2										
0x1D00	0xF5	DPLL_0[7:0]	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	config_soft_rst_n
DPLL CSI3										
0x1E00	0xF5	DPLL_0[7:0]	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	config_soft_rst_n
DPLL CSI4										
0x1F00	0xF5	DPLL_0[7:0]	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	config_soft_rst_n

Register Details

REG0 (0x0)

BIT	7	6	5	4	3	2	1	0
Field	DEV_ADDR[6:0]							CFG_BLOCK
Reset	0b1001000							0b0
Access Type	Write, Read							Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DEV_ADDR	7:1	Device Address Default address is set by the CFG0 pin at power-up. Refer to data sheet discussion of the CFG0 pin for further information. Address can be changed following power-up by updating the contents of this register.	0b0000000: I²C write/read address is 0x00/0x01 0b0000001: I²C write/read address is 0x02/0x03 ... ... 0b1001000: I²C write/read address is 0x90/0x91 0b1001010: I²C write/read address is 0x94/0x95 0b1001100: I²C write/read address is 0x98/0x99 0b1101000: I²C write/read address is 0xD0/0xD1 0b1101010: I²C write/read address is 0xD4/0xD5 0b1101100: I²C write/read address is 0xD8/0xD9 0b0101000: I²C write/read address is 0x50/0x51 0b0101010: I²C write/read address is 0x54/0x55 ... ... 0b1111111: I²C write/read address is 0xFE/0xFF
CFG_BLOCK	0	Configuration Block When set, all registers become non-writable (read-only). This bit can be used to freeze the chip configuration.	0b0: Not blocked 0b1: Blocked

REG1 (0x1)

BIT	7	6	5	4	3	2	1	0
Field	IIC_SEL[1:0]		DIS_LOC_CC[1:0]		IIC_SEL_P2	DIS_LOC_CC_P2	ALT_IIC_SEL	FAILOVER
Reset	0x0		0b00		0x0	0x0	0x0	0x0
Access Type	Write, Read		Write, Read		Write, Read	Write, Read	Write, Read	Write, Read

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BITFIELD	BITS	DESCRIPTION	DECODE
IIC_SEL	7:6	Selects control channel port type for Ports 1 and 0. Bit 0 selects type of Port 0 (RX0/SDA0, TX0/SCL0) Bit 1 selects type of Port 1 (RX1/SDA1, TX1/SCL1) Bits are set according to the latched CFG pin value at power-up. See bit 3 for selection control for Port 2.	0bX0: Port 0 UART 0bX1: Port 0 I^2C 0b0X: Port 1 UART 0b1X: Port 1 I^2C
DIS_LOC_CC	5:4	Disables control channel connection to I^2C/UART Ports 1 and 0 Bit 4 controls Port 0. Bit 5 controls Port 1. See bit 2 for control of control channel Port 2.	0bx0: Port 0 Rx/SDA and Tx/SCL connected to control channel 0bx1: Port 0 Rx/SDA and Tx/SCL disconnected from control channel 0b0x: Port 1 Rx1/SDA1 and Tx1/SCL1 connected to control channel 0b1x: Port 1 Rx1/SDA1 and Tx1/SCL1 disconnected from control channel
IIC_SEL_P2	3	Selects Port 2 control channel port type. Selects type for Port 2 (RX2/SDA2, TX2/SCL2). Bit is set according to the latched CFG pin value at power-up. See bits [7:6] for selection control for Ports 1 and 0.	0b0: UART 0b1: I^2C
DIS_LOC_CC_P2	2	Disables control channel connection to Port 2. See bits [5:4] for control of control channel for Ports 1 and 0.	0b0: Enable 0b1: Disable
ALT_IIC_SEL	1	Selects whether or not to use the alternate I^2C pins for I^2C Port 1. When set, the original Port 1 I^2C pins revert to GPIO's.	0b0: Disable selection of alternative I^2C pins for use as I^2C Port 1 0b1: Enable selection of alternative I^2C pins for use as I^2C Port 1
FAILOVER	0	I^2C and UART Port 0 failover to Port 1. When set to 1, this control bit provides a failover multiplexing of Port 0 I^2C/UART I/O onto Port 1. The purpose of this control bit is to provide redundancy for Port 0. If a primary controller connected to Port 0 is disabled, a secondary controller connected to Port 0 can assume the primary controller's duties through Port 1.	0b0: Disable failover multiplexing of Port 0 to Port 1 0b1: Enable failover multiplexing of Port 0 to Port 1

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REG3 (0x3)

BIT	7	6	5	4	3	2	1	0
Field	DIS_REM_CC_D[1:0]		DIS_REM_CC_C[1:0]		DIS_REM_CC_B[1:0]		DIS_REM_CC_A[1:0]	
Reset	0b10		0b10		0b10		0b10	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
DIS_REM_CC_D	7:6	Disable GMSL2 remote control channel link from each CC port to Link D Bit 0 disables the connection from Port 0. Bit 1 disables the connection from Port 1.	0b0: Remote control channel enabled 0b1: Remote control channel disabled
DIS_REM_CC_C	5:4	Disable GMSL2 remote control channel link from each CC port to Link C Bit 0 disables the connection from Port 0. Bit 1 disables the connection from Port 1.	0b0: Remote control channel enabled 0b1: Remote control channel disabled
DIS_REM_CC_B	3:2	Disable GMSL2 remote control channel link from each CC port to Link B Bit 0 disables the connection from Port 0. Bit 1 disables the connection from Port 1.	0b0: Remote control channel enabled 0b1: Remote control channel disabled
DIS_REM_CC_A	1:0	Disable GMSL2 remote control channel link from each CC port to Link A Bit 0 disables the connection from Port 0. Bit 1 disables the connection from Port 1.	0b0: Remote control channel enabled 0b1: Remote control channel disabled

REG4 (0x4)

BIT	7	6	5	4	3	2	1	0
Field	VID_EN_7	VID_EN_6	VID_EN_5	VID_EN_4	VID_EN_3	VID_EN_2	VID_EN_1	VID_EN_0
Reset	0b1	0b1	0b1	0b1	0b1	0b1	0b1	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
VID_EN_7	7	Video Enable	0b0: Video transmit Channel 7 disabled 0b1: Video transmit Channel 7 enabled
VID_EN_6	6	Video Enable	0b0: Video transmit Channel 6 disabled 0b1: Video transmit Channel 6 enabled
VID_EN_5	5	Video Enable	0b0: Video transmit Channel 5 disabled 0b1: Video transmit Channel 5 enabled
VID_EN_4	4	Video Enable	0b0: Video transmit Channel 4 disabled 0b1: Video transmit Channel 4 enabled
VID_EN_3	3	Video Enable	0b0: Video transmit Channel 3 disabled 0b1: Video transmit Channel 3 enabled
VID_EN_2	2	Video Enable	0b0: Video transmit Channel 2 disabled 0b1: Video transmit Channel 2 enabled
VID_EN_1	1	Video Enable	0b0: Video transmit Channel 1 disabled 0b1: Video transmit Channel 1 enabled
VID_EN_0	0	Video Enable	0b0: Video transmit Channel 0 disabled 0b1: Video transmit Channel 0 enabled

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REG5 (0x5)

BIT	7	6	5	4	3	2	1	0
Field	LOCK_EN	ERRB_EN	LOCK_CFG	–	–	–	–	–
Reset	0x1	0x1	0b0	–	–	–	–	–
Access Type	Write, Read	Write, Read	Write, Read	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
LOCK_EN	7	Enables LOCK output to GPIO	0b0: LOCK output disabled 0b1: LOCK output enabled
ERRB_EN	6	Enables ERRB output to GPIO	0b0: ERRB output disabled 0b1: ERRB output enabled
LOCK_CFG	5	Configures LOCK pin behavior	0b0: GMSL2 link locked 0b1: GMSL2 link locked and MIPI output started

REG6 (0x6)

BIT	7	6	5	4	3	2	1	0
Field	GMSL2_D	GMSL2_C	GMSL2_B	GMSL2_A	LINK_EN_D	LINK_EN_C	LINK_EN_B	LINK_EN_A
Reset	0b1	0b1	0b1	0b1	0x1	0x1	0x1	0x1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
GMSL2_D	7	GMSL1/GMSL2 Selection for Link D Bit is set according to the latched CFG1 pin value at power-up	0b0: GMSL1 0b1: GMSL2
GMSL2_C	6	GMSL1/GMSL2 Selection for Link C Bit is set according to the latched CFG1 pin value at power-up	0b0: GMSL1 0b1: GMSL2
GMSL2_B	5	GMSL1/GMSL2 Selection for Link B Bit is set according to the latched CFG1 pin value at power-up	0b0: GMSL1 0b1: GMSL2
GMSL2_A	4	GMSL1/GMSL2 Selection for Link A Bit is set according to the latched CFG1 pin value at power-up	0b0: GMSL1 0b1: GMSL2
LINK_EN_D	3	Enables Link D	0b0: Disable link D 0b1: Enable link D
LINK_EN_C	2	Enables Link C	0b0: Disable link C 0b1: Enable link C
LINK_EN_B	1	Enables Link B	0b0: Disable link B 0b1: Enable link B
LINK_EN_A	0	Enables Link A	0b0: Disable link A 0b1: Enable link A

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REG7 (0x7)

BIT	7	6	5	4	3	2	1	0
Field	CC_CROSSOVER_SEL[7:0]							
Reset	0x0							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
CC_CROSSOVER_SEL	7:0	Control Channel Port Crossover Selector Bit pairs in this register select whether control channel port crossover is disabled or enabled between Port 0 and Port 1 or Port 0 and Port 2 The primary microcontroller must be connected to I^{2}C/UART Port 0. The secondary microcontroller(s) should be connected to I^{2}C/UART Port 1 or Port 2. Each of the links is controlled by a set of two bits in the bitfield. Note that these bit sets are not contiguous. The description of each link's pair of bits is as follows: Link A bit[4], bit[0]: 00—No Crossover 10—Enable Crossover between Port 0 and Port 1 01—Enable Crossover between Port 0 and Port 2 Link B bit[5], bit[1]: 00—No Crossover 10—Enable Crossover between Port 0 and Port 1 01—Enable Crossover between Port 0 and Port 2 Link C bit[6], bit[2] 00—No Crossover 10—Enable Crossover between Port 0 and Port 1 01—Enable Crossover between Port 0 and Port 2 Link D bit[7], bit[3]: 00—No Crossover 10—Enable Crossover between Port 0 and Port 1 01—Enable Crossover between Port 0 and Port 2	0bXXX0XXX0: Link A—No Crossover 0bXXX1XXX0: Link A—Enable Crossover between Port 0 and Port 1 0bXXX0XXX1: Link A—Enable Crossover between Port 0 and Port 2 0bXX0XXX0X: Link B—No Crossover 0bXX1XXX0X: Link B—Enable Crossover between Port 0 and Port 1 0bXX0XXX1X: Link B—Enable Crossover between Port 0 and Port 2 0bX0XXX0XX: Link C—No Crossover 0bX1XXX0XX: Link C—Enable Crossover between Port 0 and Port 1 0bX0XXX1XX: Link C—Enable Crossover between Port 0 and Port 2 0b0XXX0XXX: Link D—No Crossover 0b1XXX0XXX: Link D—Enable Crossover between Port 0 and Port 1 0b0XXX1XXX: Link D—Enable Crossover between Port 0 and Port 2

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DEBUG_EXTRA_1 (0x8)

BIT	7	6	5	4	3	2	1	0
Field	PATGEN_SYNC	–	–	–	RSVD[3:0]			
Reset	0x0	–	–	–	0x0			
Access Type	Write, Read	–	–	–				

BITFIELD	BITS	DESCRIPTION	DECODE
PATGEN_SYNC	7	Synchronizes multiple pattern generators.	0b0: Do not synchronize 0b1: Synchronize

DEBUG_EXTRA (0x9)

BIT	7	6	5	4	3	2	1	0
Field	DEBUG_EXTRA[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DEBUG_EXTRA	7:0	Pattern CLK Frequency Register Bits[1:0] set the video pattern PCLK frequency. Bits[7:2] are reserved. Note that bit[1] works in conjunction with the corresponding PATGEN_CLK_SRC bitfield to set the PCLK frequency. A PATGEN_CLK_SRC bit is present in the VPRBS register of each of the eight VRX blocks. See registers 0x1DC, 0x1FC, 0x21C, 0x23C, 0x25C, 0x27C, 0x29C, and 0x2BC.	0bXXXXXX00: 25MHz 0bXXXXXX01: 75MHz 0bXXXXXX10: 150MHz (when PATGEN_CLK_SRC = 0b0) 0bXXXXXX11: 375MHz (when PATGEN_CLK_SRC = 0b1)

CTRL12 (0xA)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	–	–	LOCKED_B	–	–	–
Reset	0b0	0b0	–	–	0b0	–	–	–
Access Type			–	–	Read Only	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
LOCKED_B	3	GMSL2 Link Locked (bidirectional)	0b0: GMSL2 link not locked 0b1: GMSL2 link locked

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CTRL13 (0xB)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	–	–	LOCKED_C	–	–	–
Reset	0b0	0b0	–	–	0b0	–	–	–
Access Type			–	–	Read Only	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
LOCKED_C	3	GMSL2 Link Locked (bidirectional)	0b0: GMSL2 link not locked 0b1: GMSL2 link locked

CTRL14 (0xC)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	–	–	LOCKED_D	–	–	–
Reset	0b0	0b0	–	–	0b0	–	–	–
Access Type			–	–	Read Only	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
LOCKED_D	3	GMSL2 Link Locked (bidirectional)	0b0: GMSL2 link not locked 0b1: GMSL2 link locked

REG13 (0xD)

BIT	7	6	5	4	3	2	1	0
Field	DEV_ID[7:0]							
Reset	0xA0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
DEV_ID	7:0	Device Identifier	0xA0: MAX96712 and MAX96712B

REG14 (0xE)

BIT	7	6	5	4	3	2	1	0
Field	DIS_LOCAL_WAKE_P2	–	AUTO_SLEEP_DIS	–	DIS_REM_CC_P2[3:0]			
Reset	0b0	–	0b0	–	0b1111			
Access Type	Write, Read	–	Write, Read	–	Write, Read			

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BITFIELD	BITS	DESCRIPTION	DECODE
DIS_LOCAL_WAKE_P2	7	Disables wake-up by local µC from SDA_RX pin on Port 2. Bit [7] - Controls the local wake-up for Port 2 See the DIS_LOCAL_WAKE bitfield in the description for the TOP_CTRL/CTRL0 register (Address 0x17) for Port 1 and 0 local wake-up control.	0b0: Local wake-up enabled 0b1: Local wake-up disabled
AUTO_SLEEP_DIS	5	Disables the 8ms auto-sleep timeout after wake-up.	0b0: 8ms auto-sleep enabled 0b1: 8ms auto-sleep disabled
DIS_REM_CC_P2	3:0	Disables GMSL2 remote control channel link from CC Port 2 for all Links (A, B, C, and D) Bit 0 disables the Port 2 connection to Link A. Bit 1 disables the Port 2 connection to Link B. Bit 2 disables the Port 2 connection to Link C. Bit 3 disables the Port 2 connection to Link D.	0bXXX0: Remote control channel enabled— Link A 0bXXX1: Remote control channel disabled— Link A 0bXX0X: Remote control channel enabled— Link B 0bXX1X: Remote control channel disabled— Link B 0bX0XX: Remote control channel enabled— Link C 0bX1XX: Remote control channel disabled— Link C 0b0XXX: Remote control channel enabled— Link D 0b1XXX: Remote control channel disabled— Link D

REG26 (0x10)

BIT	7	6	5	4	3	2	1	0
Field	TX_RATE_PHYB[1:0]		RX_RATE_PHYB[1:0]		TX_RATE_PHYA[1:0]		RX_RATE_PHYA[1:0]	
Reset	0x0		0x2		0x0		0x2	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_RATE_PHYB	7:6	Transmitter Rate (when changed, becomes active after next link reset)	0b00: 187.5Mbps 0b01: Reserved 0b10: Reserved 0b11: Reserved
RX_RATE_PHYB	5:4	Receiver Rate (when changed, becomes active after next link reset) Default value is set by CFG1 pin at power-up: 6Gbps when CXTP = 1 (coax cable) and 3Gbps when CXTP = 0 (twisted-pair cable)	0b00: Reserved 0b01: 3Gbps 0b10: 6Gbps 0b11: Reserved
TX_RATE_PHYA	3:2	Transmitter Rate (when changed, becomes active after next link reset)	0b00: 187.5Mbps 0b01: Reserved 0b10: Reserved 0b11: Reserved
RX_RATE_PHYA	1:0	Receiver Rate (when changed, becomes active after next link reset) Default value is set by CFG1 pin at power-up: 6Gbps when CXTP = 1 (coax cable) and 3Gbps when CXTP = 0 (twisted-pair cable)	0b00: Reserved 0b01: 3Gbps 0b10: 6Gbps 0b11: Reserved

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REG27 (0x11)

BIT	7	6	5	4	3	2	1	0
Field	TX_RATE_PHYD[1:0]		RX_RATE_PHYD[1:0]		TX_RATE_PHYC[1:0]		RX_RATE_PHYC[1:0]	
Reset	0x0		0x2		0x0		0x2	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_RATE_PHYD	7:6	Transmitter Rate (when changed, becomes active after next link reset)	0b00: 187.5Mbps 0b01: Reserved 0b10: Reserved 0b11: Reserved
RX_RATE_PHYD	5:4	Receiver Rate (when changed, becomes active after next link reset) Default value is set by CFG1 pin at power-up: 6Gbps when CXTP = 1 (coax cable) and 3Gbps when CXTP = 0 (twisted-pair cable)	0b00: Reserved 0b01: 3Gbps 0b10: 6Gbps 0b11: Reserved
TX_RATE_PHYC	3:2	Transmitter Rate (when changed, becomes active after next link reset)	0b00: 187.5Mbps 0b01: Reserved 0b10: Reserved 0b11: Reserved
RX_RATE_PHYC	1:0	Receiver Rate (when changed, becomes active after next link reset) Default value is set by CFG1 pin at power-up: 6Gbps when CXTP = 1 (coax cable) and 3Gbps when CXTP = 0 (twisted-pair cable)	0b00: Reserved 0b01: 3Gbps 0b10: 6Gbps 0b11: Reserved

PWR0 (0x12)

BIT	7	6	5	4	3	2	1	0
Field	VDDBAD_STATUS[2:0]			CMP_STATUS[4:0]				
Reset	0x0			0x0				
Access Type	Read Only			Read Only				

BITFIELD	BITS	DESCRIPTION	DECODE
VDDBAD_STATUS	7:5	Switched 1V supply comparator status bits	0bXX1: Latched high when CAP_VDD < 0.82V 0bX1X: Latched high when CAP_VDD < 0.82V 0bX00: CAP_VDD > 0.82V 0b1XX: Reserved
CMP_STATUS	4:0	V_{DD18}, V_{DDIO}, and CAP_VDD supply voltage comparator status bits	0bXXXX0: Latched low when V_{DD18} < 1.617V 0bXXX0X: Latched low when switched V_{DDIO} supply < 1.617V 0bXX0XX: Latched low when CAP_VDD < 0.82V 0bX0XXX: Reserved 0b0XXXX: Reserved 0bXX111: All supplies are at expected levels

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PWR1 (0x13)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RESET_ALL	RSVD[5:0]					
Reset	0b0	0b0	0x0					
Access Type		Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
RESET_ALL	6	Device Reset Writing 1 to this bit resets the device. All blocks and registers are reset to defaults. This is equivalent to toggling the PWDNB pin. The bit is cleared when written.	0b0: No action 0b1: Activate chip reset

CTRL0 (0x17)

BIT	7	6	5	4	3	2	1	0
Field	WAKE_EN_D	WAKE_EN_C	WAKE_EN_B	WAKE_EN_A	SLEEP	REG_ENABLE	DIS_LOCAL_WAKE[1:0]	
Reset	0b0	0b0	0b0	0b1	0b0	0x0	0b0	
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
WAKE_EN_D	7	Enable wake-up by remote chip connected to Link D.	0b0: Link D remote wake-up disabled 0b1: Link D remote wake-up enabled
WAKE_EN_C	6	Enable wake-up by remote chip connected to Link C	0b0: Link C remote wake-up disabled 0b1: Link C remote wake-up enabled
WAKE_EN_B	5	Enable wake-up by remote chip connected to Link B	0b0: Link B remote wake-up disabled 0b1: Link B remote wake-up enabled
WAKE_EN_A	4	Enable wake-up by remote chip connected to Link A	0b0: Link A remote wake-up disabled 0b1: Link A remote wake-up enabled
SLEEP	3	Activates sleep mode.	0b0: Sleep mode disabled 0b1: Sleep mode enabled
REG_ENABLE	2	V_{DD} LDO Regulator Enable Works in conjunction with bitfield REG_MNL (0x19). Enable function is available when REG_MNL = 1. If REG_MNL = 0, manual control using REG_ENABLE is not available.	0b0: V_{DD} LDO regulator disabled (bypassed) when REG_MNL = 1 0b1: V_{DD} LDO regulator enabled when REG_ENABLE = 1 and REG_MNL = 1. When V_{DD} = 1.2V, first set REG_ENABLE = 1, and then write REG_MNL = 1
DIS_LOCAL_WAKE	1:0	Disables wake-up by local µC from SDA_RX pin for Ports 1 and 0 bit [1] - Controls the local wake-up for Port 1 bit [0] - Controls the local wake-up for Port 0 See the description for DEV_REG14 (at address 0xE) for Port 2 local wake-up control.	0bX0: Local wake-up enabled—Port 0 0bX1: Local wake-up disabled—Port 0 0b0X: Local wake-up enabled—Port 1 0b1X: Local wake-up disabled—Port 1

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CTRL1 (0x18)

BIT	7	6	5	4	3	2	1	0
Field	RESET_LINK_D	RESET_LINK_C	RESET_LINK_B	RESET_LINK_A	RESET_ONESHOT_D	RESET_ONESHOT_C	RESET_ONESHOT_B	RESET_ONESHOT_A
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write Clears All, Read	Write Clears All, Read	Write Clears All, Read	Write Clears All, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RESET_LINK_D	7	Link D Reset Resets whole data path (keep register settings). Write 1 to activate reset, write 0 to release reset.	0b0: Release link reset 0b1: Activate link reset
RESET_LINK_C	6	Link C Reset Resets whole data path (keep register settings). Write 1 to activate reset, write 0 to release reset.	0b0: Release link reset 0b1: Activate link reset
RESET_LINK_B	5	Link B Reset Resets whole data path (keep register settings). Write 1 to activate reset, write 0 to release reset.	0b0: Release link reset 0b1: Activate link reset
RESET_LINK_A	4	Link A Reset Resets whole data path (keep register settings). Write 1 to activate reset, write 0 to release reset.	0b0: Release link reset 0b1: Activate link reset
RESET_ONESHOT_D	3	Link D One-Shot Reset Resets whole data path (keep register settings) one shot. Write 1 to activate reset, bit self-clears and automatically releases reset.	0b0: No action 0b1: Reset data path
RESET_ONESHOT_C	2	Link C One-Shot Reset Resets whole data path (keep register settings) one shot. Write 1 to activate reset, bit self-clears and automatically releases reset.	0b0: No action 0b1: Reset data path

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BITFIELD	BITS	DESCRIPTION	DECODE
RESET_ONE SHOT_B	1	Link B One-Shot Reset Resets whole data path (keep register settings) one shot. Write 1 to activate reset, bit self-clears and automatically releases reset.	0b0: No action 0b1: Reset data path
RESET_ONE SHOT_A	0	Link A One-Shot Reset Resets whole data path (keep register settings) one shot. Write 1 to activate reset, bit self-clears and automatically releases reset.	0b0: No action 0b1: Reset data path

CTRL2 (0x19)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	REG_MNL	RSVD[1:0]		RSVD[1:0]	
Reset	0x1	0b0	0x0	0b0	0x1		0x0	
Access Type				Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
REG_MNL	4	Enables V_{DD} LDO regulator manual on/bypass control via REG_ENABLE bitfield (0x10).	0b0: V_{DD} LDO regulator range sensing on. 0b1: V_{DD} LDO regulator range sensing off. V_{DD} LDO regulator on/bypass state controlled by REG_ENABLE. When V_{DD} = 1.2V, enable V_{DD} LDO regulator by first setting REG_ENABLE = 1 and then setting REG_MNL = 1.

CTRL3 (0x1A)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD[1:0]		LOCKED	ERROR	CMU_LOC KED	RSVD
Reset	0b0	0b0	0x1		0b0	0b0	0b0	0x0
Access Type					Read Only	Read Only	Read Only	

BITFIELD	BITS	DESCRIPTION	DECODE
LOCKED	3	GMSL2 link lock (bidirectional)—Link A only	0b0: GMSL2 link not locked 0b1: GMSL2 link locked
ERROR	2	Reflects error status (inverse of ERRB pin value)	0b0: ERRB not asserted (ERRB pin = 1) 0b1: ERRB asserted (ERRB pin = 0)
CMU_LOCK ED	1	Clock Multiplier Unit (CMU) lock	0b0: CMU not locked 0b1: CMU locked

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CTRL11 (0x22)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	CXTP_D	RSVD	CXTP_C	RSVD	CXTP_B	RSVD	CXTP_A
Reset	0b1	0b0	0b1	0b0	0b1	0b0	0b1	0b0
Access Type		Write, Read		Write, Read		Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CXTP_D	6	Coax/Twisted-Pair Cable Select for Link D Bit is set according to the latched CFG1 pin value at power-up.	0b0: Shielded twisted-pair drive 0b1: Coax drive
CXTP_C	4	Coax/Twisted-Pair Cable Select for Link C Bit is set according to the latched CFG1 pin value at power-up.	0b0: Shielded twisted-pair drive 0b1: Coax drive
CXTP_B	2	Coax/Twisted-Pair Cable Select for Link B Bit is set according to the latched CFG1 pin value at power-up.	0b0: Shielded twisted-pair drive 0b1: Coax drive
CXTP_A	0	Coax/Twisted-Pair Cable Select for Link A Bit is set according to the latched CFG1 pin value at power-up.	0b0: Shielded twisted-pair drive 0b1: Coax drive

INTR0 (0x23)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	–	AUTO_ERR_RST_EN	DEC_ERR_THR[2:0]		
Reset	0x1	0x0	0x1	–	0b0	0x0		
Access Type				–	Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
AUTO_ERR_RST_EN	3	Automatically resets DEC_ERR_A (0x35), DEC_ERR_B (0x36), DEC_ERR_C (0x37) DEC_ERR_D (0x38) and IDLE_ERR_A (0x39), IDLE_ERR_B (0x3A), IDLE_ERR_C (0x3B), IDLE_ERR_D (0x3C) bitfields after ERRB pin is asserted for 1µs.	0b0: Auto reset disabled 0b1: Auto reset enabled

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BITFIELD	BITS	DESCRIPTION	DECODE
DEC_ERR_THR	2:0	Decoding and Idle Error Reporting Threshold DEC_ERR_FLAG_A (0x26) is asserted when DEC_ERR_A (0x35) ≥ DEC_ERR_THR. DEC_ERR_FLAG_B (0x26) is asserted when DEC_ERR_B (0x36) ≥ DEC_ERR_THR. DEC_ERR_FLAG_C (0x26) is asserted when DEC_ERR_C (0x37) ≥ DEC_ERR_THR. DEC_ERR_FLAG_D (0x26) is asserted when DEC_ERR_D (0x38) ≥ DEC_ERR_THR. IDLE_ERR_FLAG_A (0x2C) is asserted when IDLE_ERR_A (0x39) ≥ DEC_ERR_THR. IDLE_ERR_FLAG_B (0x2C) is asserted when IDLE_ERR_B (0x3A) ≥ DEC_ERR_THR. IDLE_ERR_FLAG_C (0x2C) is asserted when IDLE_ERR_C (0x3B) ≥ DEC_ERR_THR. IDLE_ERR_FLAG_D (0x2C) is asserted when IDLE_ERR_D (0x3C) ≥ DEC_ERR_THR.	0b000: 1 error 0b001: 2 errors 0b010: 4 errors 0b011: 8 errors 0b100: 16 errors 0b101: 32 errors 0b110: 64 errors 0b111: 128 errors

INTR1 (0x24)

BIT	7	6	5	4	3	2	1	0
Field	PKT_CNT_EXP[3:0]				AUTO_CNT_RST_EN	PKT_CNT_THR[2:0]		
Reset	0x0				0b0	0x0		
Access Type	Write, Read				Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
PKT_CNT_EXP	7:4	Packet Count Multiplier Exponent See the description of PKT_CNT_x (0x40—0x43) bitfield.	0xX: PKT_CNT_x exponent
AUTO_CNT_RST_EN	3	Automatically resets PKT_CNT_x bitfield (0x40—0x43) after ERRB pin is asserted for 1µs.	0b0: Do not automatically reset PKT_CNT_x register after ERRB pin is asserted for 1µs 0b1: Automatically reset PKT_CNT_x register after ERRB pin is asserted for 1µs

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BITFIELD	BITS	DESCRIPTION	DECODE
PKT_CNT_THR	2:0	Packet Count Reporting Threshold PKT_CNT_FLAG_A (0x2C) is asserted when PKT_CNT_A (0x40) ≥ PKT_CNT_THR. PKT_CNT_FLAG_B (0x2C) is asserted when PKT_CNT_B (0x41) ≥ PKT_CNT_THR. PKT_CNT_FLAG_C (0x2C) is asserted when PKT_CNT_C (0x42) ≥ PKT_CNT_THR. PKT_CNT_FLAG_D (0x2C) is asserted when PKT_CNT_D (0x43) ≥ PKT_CNT_THR.	0b000: 1 packet 0b001: 2 packets 0b010: 4 packets 0b011: 8 packets 0b100: 16 packets 0b101: 32 packets 0b110: 64 packets 0b111: 128 packets

INTR2 (0x25)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	DEC_ERR_OEN_D	DEC_ERR_OEN_C	DEC_ERR_OEN_B	DEC_ERR_OEN_A
Reset	0b0	0b0	0b0	0b0	0b1	0b1	0b1	0b1
Access Type					Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DEC_ERR_OEN_D	3	Enables reporting of decoding errors (DEC_ERR_FLAG_D—0x26) at ERRB pin.	0b0: Disable reporting of decoding errors (DEC_ERR_FLAG_D) at ERRB pin 0b1: Enable reporting of decoding errors (DEC_ERR_FLAG_D) at ERRB pin
DEC_ERR_OEN_C	2	Enables reporting of decoding errors (DEC_ERR_FLAG_C—0x26) at ERRB pin.	0b0: Disable reporting of decoding errors (DEC_ERR_FLAG_C) at ERRB pin 0b1: Enable reporting of decoding errors (DEC_ERR_FLAG_C) at ERRB pin
DEC_ERR_OEN_B	1	Enables reporting of decoding errors (DEC_ERR_FLAG_B—0x26) at ERRB pin.	0b0: Disable reporting of decoding errors (DEC_ERR_FLAG_B) at ERRB pin 0b1: Enable reporting of decoding errors (DEC_ERR_FLAG_B) at ERRB pin
DEC_ERR_OEN_A	0	Enables reporting of decoding errors (DEC_ERR_FLAG_A—0x26) at ERRB pin.	0b0: Disable reporting of decoding errors (DEC_ERR_FLAG_A) at ERRB pin 0b1: Enable reporting of decoding errors (DEC_ERR_FLAG_A) at ERRB pin

INTR3 (0x26)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	DEC_ERR_FLAG_D	DEC_ERR_FLAG_C	DEC_ERR_FLAG_B	DEC_ERR_FLAG_A
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type					Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
DEC_ERR_FLAG_D	3	Decoding error flag for Link D, asserted when DEC_ERR_D ≥ DEC_ERR_THR.	0b0: DEC_ERR_D < DEC_ERR_THR 0b1: DEC_ERR_D ≥ DEC_ERR_THR

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BITFIELD	BITS	DESCRIPTION	DECODE
DEC_ERR_FLAG_C	2	Decoding error flag for Link C, asserted when DEC_ERR_C ≥ DEC_ERR_THR.	0b0: DEC_ERR_C < DEC_ERR_THR 0b1: DEC_ERR_C ≥ DEC_ERR_THR
DEC_ERR_FLAG_B	1	Decoding error flag for Link B, asserted when DEC_ERR_B ≥ DEC_ERR_THR.	0b0: DEC_ERR_B < DEC_ERR_THR 0b1: DEC_ERR_B ≥ DEC_ERR_THR
DEC_ERR_FLAG_A	0	Decoding error flag for Link A, asserted when DEC_ERR_A ≥ DEC_ERR_THR.	0b0: DEC_ERR_A < DEC_ERR_THR 0b1: DEC_ERR_A ≥ DEC_ERR_THR

INTR4 (0x27)

BIT	7	6	5	4	3	2	1	0
Field	EOM_ERR_OEN_D	EOM_ERR_OEN_C	EOM_ERR_OEN_B	EOM_ERR_OEN_A	RTTN_CRC_ERR_OEN	LFLT_INT_OEN	WM1_ERR_OEN	WM_ERR_OEN
Reset	0b0	0b0	0b0	0b0	0b0	0x1	0b1	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_ERR_OEN_D	7	Enables reporting of eye-opening monitor error (EOM_ERR_FLAG_D—0x28) for Link D at ERRB pin.	0b0: Disable reporting of eye-opening monitor error (EOM_ERR_FLAG_D) for Link D at ERRB pin 0b1: Enable reporting of eye-opening monitor error (EOM_ERR_FLAG_D) for Link D at ERRB pin
EOM_ERR_OEN_C	6	Enables reporting of eye-opening monitor error (EOM_ERR_FLAG_C—0x28) for Link C at ERRB pin.	0b0: Disable reporting of eye-opening monitor error (EOM_ERR_FLAG_C) for Link C at ERRB pin 0b1: Enable reporting of eye-opening monitor error (EOM_ERR_FLAG_C) for Link C at ERRB pin
EOM_ERR_OEN_B	5	Enables reporting of eye-opening monitor error (EOM_ERR_FLAG_B—0x28) for Link B at ERRB pin.	0b0: Disable reporting of eye-opening monitor error (EOM_ERR_FLAG_B) for Link B at ERRB pin 0b1: Enable reporting of eye-opening monitor error (EOM_ERR_FLAG_B) for Link B at ERRB pin
EOM_ERR_OEN_A	4	Enables reporting of eye-opening monitor error (EOM_ERR_FLAG_A0x28) for Link A at ERRB pin.	0b0: Disable reporting of eye-opening monitor error (EOM_ERR_FLAG_A) for Link A at ERRB pin 0b1: Enable reporting of eye-opening monitor error (EOM_ERR_FLAG_A) for Link A at ERRB pin
RTTN_CRC_ERR_OEN	3	Enables reporting of retention restoration CRC error (RTTN_CRC_ERR_FLAG) at ERRB pin.	0b0: Disable reporting of retention restoration CRC error (RTTN_CRC_ERR_FLAG) at ERRB pin 0b1: Enable reporting of retention restoration CRC error (RTTN_CRC_ERR_FLAG) at ERRB pin
LFLT_INT_OEN	2	Enable reporting of line fault interrupt (LFLT_INT) at ERRB pin	0b0: Disable reporting of line fault interrupt (LFLT_INT) at ERRB pin 0b1: Enable reporting of line fault interrupt (LFLT_INT) at ERRB pin
WM1_ERR_OEN	1	Enables reporting of watermark errors (WM1_ERR_FLAG) at ERRB pin.	0b0: Disable reporting of watermark errors (WM1_ERR_FLAG) at ERRB pin 0b1: Enable reporting of watermark errors (WM1_ERR_FLAG) at ERRB pin
WM_ERR_OEN	0	Enables reporting of watermark errors (WM_ERR_FLAG) at ERRB pin.	0b0: Disable reporting of watermark errors (WM_ERR_FLAG) at ERRB pin 0b1: Enable reporting of watermark errors (WM_ERR_FLAG) at ERRB pin

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INTR5 (0x28)

BIT	7	6	5	4	3	2	1	0
Field	EOM_ERR_FLAG_D	EOM_ERR_FLAG_C	EOM_ERR_FLAG_B	EOM_ERR_FLAG_A	RTTN_CRC_INT	LFLT_INT	WM1_ERR_FLAG	WM_ERR_FLAG
Reset	0b0	0b0	0b0	0b0	0x0	0x0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_ERR_FLAG_D	7	Link D Eye-opening Threshold Status Indicates whether or not eye-opening is below configured threshold for Link D.	0b0: Eye-opening is above configured threshold for Link D 0b1: Eye-opening is below configured threshold for Link D
EOM_ERR_FLAG_C	6	Link C Eye-opening Threshold Status Indicates whether or not eye-opening is below configured threshold for Link C.	0b0: Eye-opening is above configured threshold for Link C 0b1: Eye-opening is below configured threshold for Link C
EOM_ERR_FLAG_B	5	Link B Eye-opening Threshold Status Indicates whether or not eye-opening is below configured threshold for Link B.	0b0: Eye-opening is above configured threshold for Link B 0b1: Eye-opening is below configured threshold for Link B
EOM_ERR_FLAG_A	4	Link A Eye-opening Threshold Status Indicates whether or not eye-opening is below configured threshold for Link A.	0b0: Eye-opening is above configured threshold for Link A 0b1: Eye-opening is below configured threshold for Link A
RTTN_CRC_INT	3	Retention Memory Restore CRC Error Interrupt Asserted when an error is detected in the CRC calculation during a retention memory restore. Reading this register bit will clear the retention CRC error register.	0b0: No error detected in the CRC calculation during a retention memory restore. 0b1: An error was detected in the CRC calculation during a retention memory restore.
LFLT_INT	2	Line Fault Interrupt Asserted when either one of line fault monitors indicates a fault status. ***See LF_0 and LF_1 registers for more info.***	0b0: No fault status indicated for either line fault monitor 0b1: One (or both) of the line fault monitors indicate a fault status.
WM1_ERR_FLAG	1	Watermark Error Flag (watermark detector 1) Asserted when a watermark error is detected by watermark detector 1.	0b0: No watermark error detected 0b1: Watermark error detected
WM_ERR_FLAG	0	Watermark Error Flag (watermark detector 0) Asserted when a watermark error is detected by watermark detector 0.	0b0: No watermark error detected 0b1: Watermark error detected

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INTR6 (0x29)

BIT	7	6	5	4	3	2	1	0
Field	G1_D_ERR_OEN	G1_C_ERR_OEN	G1_B_ERR_OEN	G1_A_ERR_OEN	LCRC_ERR_OEN	VPRBS_ERR_OEN	REM_ERR_OEN	FSYNC_ERR_OEN
Reset	0x1	0x1	0x1	0x1	0b1	0b1	0b0	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
G1_D_ERR_OEN	7	Enables reporting of GMSL1 Link D errors (G1_D_ERR_FLAG) at ERRB pin.	0b0: Disable GMSL1 Link D error reporting (G1_D_ERR_FLAG) at ERRB pin 0b1: Enable GMSL1 Link D error reporting (G1_D_ERR_FLAG) at ERRB pin
G1_C_ERR_OEN	6	Enables reporting of GMSL1 Link C errors (G1_C_ERR_FLAG) at ERRB pin.	0b0: Disable GMSL1 Link C error reporting (G1_C_ERR_FLAG) at ERRB pin 0b1: Enable GMSL1 Link C error reporting (G1_C_ERR_FLAG) at ERRB pin
G1_B_ERR_OEN	5	Enables reporting of GMSL1 Link B errors (G1_B_ERR_FLAG) at ERRB pin.	0b0: Disable GMSL1 Link B error reporting (G1_B_ERR_FLAG) at ERRB pin 0b1: Enable GMSL1 Link B error reporting (G1_B_ERR_FLAG) at ERRB pin
G1_A_ERR_OEN	4	Enables reporting of GMSL1 Link A errors (G1_A_ERR_FLAG) at ERRB pin.	0b0: Disable GMSL1 Link A error reporting (G1_A_ERR_FLAG) at ERRB pin 0b1: Enable GMSL1 Link A error reporting (G1_A_ERR_FLAG) at ERRB pin
LCRC_ERR_OEN	3	Enables reporting of video line CRC errors (LCRC_ERR_FLAG—0x2A) at ERRB pin.	0b0: Disable video line CRC error reporting (LCRC_ERR_FLAG) at ERRB pin 0b1: Enable video line CRC error reporting (LCRC_ERR_FLAG) at ERRB pin
VPRBS_ERR_OEN	2	Enables reporting of video PRBS errors (VPRBS_ERR_FLAG—0x2A) at ERRB pin.	0b0: Disable video PRBS error reporting (VPRBS_ERR_FLAG) at ERRB pin 0b1: Enable video PRBS error reporting (VPRBS_ERR_FLAG) at ERRB pin
REM_ERR_OEN	1	Enables reporting of remote error status (REM_ERR—0x2A) at ERRB pin.	0b0: Disable remote error status (REM_ERR) reporting at ERRB pin 0b1: Enable remote error status (REM_ERR) reporting at ERRB pin
FSYNC_ERR_OEN	0	Enables reporting of frame sync errors (FSYNC_ERR_FLAG—0x2A) at ERRB pin.	0b0: Disable frame sync error reporting (FSYNC_ERR_FLAG) at ERRB pin 0b1: Enable frame sync error reporting (FSYNC_ERR_FLAG) at ERRB pin

INTR7 (0x2A)

BIT	7	6	5	4	3	2	1	0
Field	G1_D_ERR_FLAG	G1_C_ERR_FLAG	G1_B_ERR_FLAG	G1_A_ERR_FLAG	LCRC_ERR_FLAG	VPRBS_ERR_FLAG	REM_ERR_FLAG	FSYNC_ERR_FLAG
Reset	0x0	0x0	0x0	0x0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

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BITFIELD	BITS	DESCRIPTION	DECODE
G1_D_ERR_FLAG	7	GMSL1 Link D Error Flag When PRBS test is enabled, this bit is asserted if at least one PRBS error has been detected. When PRBS test is not enabled, this flag is asserted when any of these conditions is true: 1. The number of detected decoding errors is greater than the detected error threshold (DET_ERR (0xB15) > DET_THR (0xC0E)). 2. The measured eye-opening is less than or equal to the eye-opening threshold (EOM_EYE_WIDTH (0xC1C) ≤ EOM_MIN_THR_G1 (0xB13)). 3. The adaptive EQ has detected an under boost. 4. A video line CRC error is detected. 5. The maximum retransmission count in PKTCC communication has been exceeded. 6. A CRC errors was detected in PKTCC communication.	0b0: No error detected 0b1: Error detected
G1_C_ERR_FLAG	6	GMSL1 Link C Error Flag When PRBS test is enabled, this bit is asserted if at least one PRBS error has been detected. When PRBS test is not enabled, this flag is asserted when any of these conditions is true: 1. The number of detected decoding errors is greater than the detected error threshold (DET_ERR (0xB15) > DET_THR (0xC0E)). 2. The measured eye-opening is less than or equal to the eye-opening threshold (EOM_EYE_WIDTH (0xC1C) ≤ EOM_MIN_THR_G1 (0xB13)). 3. The adaptive EQ has detected an under boost. 4. A video line CRC error is detected. 5. The maximum retransmission count in PKTCC communication has been exceeded. 6. A CRC errors was detected in PKTCC communication.	0b0: No error detected 0b1: Error detected

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BITFIELD	BITS	DESCRIPTION	DECODE
G1_B_ERR_FLAG	5	GMSL1 Link B Error Flag When PRBS test is enabled, this bit is asserted if at least one PRBS error has been detected. When PRBS test is not enabled, this flag is asserted when any of these conditions is true: 1. The number of detected decoding errors is greater than the detected error threshold (DET_ERR (0xB15) > DET_THR (0xC0E)). 2. The measured eye-opening is less than or equal to the eye-opening threshold (EOM_EYE_WIDTH (0xC1C) ≤ EOM_MIN_THR_G1 (0xB13)). 3. The adaptive EQ has detected an under boost. 4. A video line CRC error is detected. 5. The maximum retransmission count in PKTCC communication has been exceeded. 6. A CRC errors was detected in PKTCC communication.	0b0: No error detected 0b1: Error detected
G1_A_ERR_FLAG	4	GMSL1 Link A Error Flag When PRBS test is enabled, this bit is asserted if at least one PRBS error has been detected. When PRBS test is not enabled, this flag is asserted when any of these conditions is true: 1. The number of detected decoding errors is greater than the detected error threshold (DET_ERR (0xB15) > DET_THR (0xC0E)). 2. The measured eye-opening is less than or equal to the eye-opening threshold (EOM_EYE_WIDTH (0xC1C) ≤ EOM_MIN_THR_G1 (0xB13)). 3. The adaptive EQ has detected an under boost. 4. A video line CRC error is detected. 5. The maximum retransmission count in PKTCC communication has been exceeded. 6. A CRC errors was detected in PKTCC communication.	0b0: No error detected 0b1: Error detected

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BITFIELD	BITS	DESCRIPTION	DECODE
LCRC_ERR_FLAG	3	Video Line CRC Error Flag Assert when a video line CRC error is detected.	0b0: No video line CRC error detected 0b1: Video line CRC error detected
VPRBS_ERR_FLAG	2	Video PRBS Error Flag Asserted when VPRBS_ERR (0x1D8) > 0.	0b0: VPRBS_ERR ≤ 0 0b1: VPRBS_ERR > 0
REM_ERR_FLAG	1	Receives remote side error status (inverse of remote side ERRB pin level).	0b0: No remote side error status received 0b1: Remote side error status received
FSYNC_ERR_FLAG	0	Frame Sync Error Flag Asserted when FSYNC_ERR_CNT (0x4B0) ≥ FSYNC_ERR_THR (0x4B1).	0b0: FSYNC_ERR_CNT < FSYNC_ERR_THR 0b1: FSYNC_ERR_CNT ≥ FSYNC_ERR_THR

INTR8 (0x2B)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	IDLE_ERR_OEN_D	IDLE_ERR_OEN_C	IDLE_ERR_OEN_B	IDLE_ERR_OEN_A
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type					Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
IDLE_ERR_OEN_D	3	Enables reporting of Idle word errors (IDLE_ERR_FLAG_D) at ERRB pin.	0b0: Disable idle word error reporting (IDLE_ERR_FLAG_D) at ERRB pin 0b1: Enable idle word error reporting (IDLE_ERR_FLAG_D) at ERRB pin
IDLE_ERR_OEN_C	2	Enables reporting of idle word errors (IDLE_ERR_FLAG_C) at ERRB pin.	0b0: Disable idle word error reporting (IDLE_ERR_FLAG_C) at ERRB pin 0b1: Enable idle word error reporting (IDLE_ERR_FLAG_C) at ERRB pin
IDLE_ERR_OEN_B	1	Enables reporting of idle word errors (IDLE_ERR_FLAG_B) at ERRB pin.	0b0: Disable idle word error reporting (IDLE_ERR_FLAG_B) at ERRB pin 0b1: Enable idle word error reporting (IDLE_ERR_FLAG_B) at ERRB pin
IDLE_ERR_OEN_A	0	Enables reporting of idle word errors (IDLE_ERR_FLAG_A) at ERRB pin.	0b0: Disable idle word error reporting (IDLE_ERR_FLAG_A) at ERRB pin 0b1: Enable idle word error reporting (IDLE_ERR_FLAG_A) at ERRB pin

INTR9 (0x2C)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	IDLE_ERR_FLAG_D	IDLE_ERR_FLAG_C	IDLE_ERR_FLAG_B	IDLE_ERR_FLAG_A
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type					Read Only	Read Only	Read Only	Read Only

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BITFIELD	BITS	DESCRIPTION	DECODE
IDLE_ERR_FLAG_D	3	Idle Word Error Flag D Asserted when IDLE_ERR_D (0x3C) ≥ DEC_ERR_THR (0x23).	0b0: IDLE_ERR_D < DEC_ERR_THR 0b1: IDLE_ERR_D ≥ DEC_ERR_THR
IDLE_ERR_FLAG_C	2	Idle Word Error Flag C Asserted when IDLE_ERR_C (0x3B) ≥ DEC_ERR_THR.	0b0: IDLE_ERR_C < DEC_ERR_THR 0b1: IDLE_ERR_C ≥ DEC_ERR_THR
IDLE_ERR_FLAG_B	1	Idle Word Error Flag B Asserted when IDLE_ERR_B (x3A0 ≥ DEC_ERR_THR (0x23).	0b0: IDLE_ERR_B < DEC_ERR_THR 0b1: IDLE_ERR_B ≥ DEC_ERR_THR
IDLE_ERR_FLAG_A	0	Idle Word Error Flag A Asserted when IDLE_ERR_A (0x39) ≥ DEC_ERR_THR (0x23).	0b0: IDLE_ERR_A < DEC_ERR_THR 0b1: IDLE_ERR_A ≥ DEC_ERR_THR

INTR10 (0x2D)

BIT	7	6	5	4	3	2	1	0
Field	RT_CNT_OEN_D	RT_CNT_OEN_C	RT_CNT_OEN_B	RT_CNT_OEN_A	MAX_RT_OEN_D	MAX_RT_OEN_C	MAX_RT_OEN_B	MAX_RT_OEN_A
Reset	0b0	0b0	0b0	0b0	0b1	0b1	0b1	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RT_CNT_OEN_D	7	Enables reporting of combined ARQ retransmission event flag (RT_CNT_FLAG_D—0x2E) at ERRB pin.	0b0: Disable reporting of combined ARQ retransmission event flag (RT_CNT_FLAG_D) at ERRB pin 0b1: Enable reporting of combined ARQ retransmission event flag (RT_CNT_FLAG_D) at ERRB pin
RT_CNT_OEN_C	6	Enables reporting of combined ARQ retransmission event flag (RT_CNT_FLAG_C—0x2E) at ERRB pin.	0b0: Disable reporting of combined ARQ retransmission event flag (RT_CNT_FLAG_C) at ERRB pin 0b1: Enable reporting of combined ARQ retransmission event flag (RT_CNT_FLAG_C) at ERRB pin
RT_CNT_OEN_B	5	Enables reporting of combined ARQ retransmission event flag (RT_CNT_FLAG_B—0x2E) at ERRB pin.	0b0: Disable reporting of combined ARQ retransmission event flag (RT_CNT_FLAG_B) at ERRB pin 0b1: Enable reporting of combined ARQ retransmission event flag (RT_CNT_FLAG_B) at ERRB pin
RT_CNT_OEN_A	4	Enables reporting of combined ARQ retransmission event flag (RT_CNT_FLAG_A—0x2E) at ERRB pin.	0b0: Disable reporting of combined ARQ retransmission event flag (RT_CNT_FLAG_A) at ERRB pin 0b1: Enable reporting of combined ARQ retransmission event flag (RT_CNT_FLAG_A) at ERRB pin

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BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_OEN_D	3	Enables reporting of combined ARQ maximum retransmission limit error flag (MAX_RT_FLAG_D—0x2E) at ERRB pin.	0b0: Disable reporting of combined ARQ maximum retransmission limit error flag (MAX_RT_FLAG_D) at ERRB pin 0b1: Enable reporting of combined ARQ maximum retransmission limit error flag (MAX_RT_FLAG_D) at ERRB pin
MAX_RT_OEN_C	2	Enables reporting of combined ARQ maximum retransmission limit error flag (MAX_RT_FLAG_C—0x2E) at ERRB pin.	0b0: Disable reporting of combined ARQ maximum retransmission limit error flag (MAX_RT_FLAG_C) at ERRB pin 0b1: Enable reporting of combined ARQ maximum retransmission limit error flag (MAX_RT_FLAG_C) at ERRB pin
MAX_RT_OEN_B	1	Enables reporting of combined ARQ maximum retransmission limit error flag (MAX_RT_FLAG_B—0x2E) at ERRB pin.	0b0: Disable reporting of combined ARQ maximum retransmission limit error flag (MAX_RT_FLAG_B) at ERRB pin 0b1: Enable reporting of combined ARQ maximum retransmission limit error flag (MAX_RT_FLAG_B) at ERRB pin
MAX_RT_OEN_A	0	Enables reporting of combined ARQ maximum retransmission limit error flag (MAX_RT_FLAG_A—0x2E) at ERRB pin.	0b0: Disable reporting of combined ARQ maximum retransmission limit error flag (MAX_RT_FLAG_A) at ERRB pin 0b1: Enable reporting of combined ARQ maximum retransmission limit error flag (MAX_RT_FLAG_A) at ERRB pin

INTR11 (0x2E)

BIT	7	6	5	4	3	2	1	0
Field	RT_CNT_FLAG_D	RT_CNT_FLAG_C	RT_CNT_FLAG_B	RT_CNT_FLAG_A	MAX_RT_FLAG_D	MAX_RT_FLAG_C	MAX_RT_FLAG_B	MAX_RT_FLAG_A
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
RT_CNT_FLAG_D	7	Combined ARQ Retransmission Event Flag D Asserted when any of the selected channels have done at least one ARQ retransmission. Selection is done by each channel's RT_CNT_OEN_D (0x2D) register bit.	0b0: None of the selected channels have done at least one ARQ retransmission 0b1: One or more of the selected channels has done at least one ARQ retransmission
RT_CNT_FLAG_C	6	Combined ARQ Retransmission Event Flag C Asserted when any of the selected channels have done at least one ARQ retransmission. Selection is done by each channel's RT_CNT_OEN_C (0x2D) register bit.	0b0: None of the selected channels have done at least one ARQ retransmission 0b1: One or more of the selected channels has done at least one ARQ retransmission
RT_CNT_FLAG_B	5	Combined ARQ Retransmission Event Flag B Asserted when any of the selected channels have done at least one ARQ retransmission. Selection is done by each channel's RT_CNT_OEN_B (0x2D) register bit.	0b0: None of the selected channels have done at least one ARQ retransmission 0b1: One or more of the selected channels has done at least one ARQ retransmission

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BITFIELD	BITS	DESCRIPTION	DECODE
RT_CNT_FLAG_A	4	Combined ARQ Retransmission Event Flag A Asserted when any of the selected channels have done at least one ARQ retransmission. Selection is done by each channel's RT_CNT_OEN_A (0x2D) register bit.	0b0: None of the selected channels have done at least one ARQ retransmission 0b1: One or more of the selected channels has done at least one ARQ retransmission
MAX_RT_FLAG_D	3	Combined ARQ Maximum Retransmission Limit Error Flag D Asserted when any of the selected channel's ARQ retransmission limit is reached. Selection is done by each channel's MAX_RT_ERR_OEN_D (0x2D) register bit.	0b0: None of the selected channels have reached the maximum retry limit 0b1: One or more of the selected channels has reached the maximum retry limit
MAX_RT_FLAG_C	2	Combined ARQ Maximum Retransmission Limit Error Flag C Asserted when any of the selected channel's ARQ retransmission limit is reached. Selection is done by each channel's MAX_RT_ERR_OEN_C (0x2D) register bit.	0b0: None of the selected channels have reached the maximum retry limit 0b1: One or more of the selected channels has reached the maximum retry limit
MAX_RT_FLAG_B	1	Combined ARQ Maximum Retransmission Limit Error Flag B Asserted when any of the selected channel's ARQ retransmission limit is reached. Selection is done by each channel's MAX_RT_ERR_OEN_B (0x2D) register bit.	0b0: None of the selected channels have reached the maximum retry limit 0b1: One or more of the selected channels has reached the maximum retry limit
MAX_RT_FLAG_A	0	Combined ARQ Maximum Retransmission Limit Error Flag A Asserted when any of the selected channel's ARQ retransmission limit is reached. Selection is done by each channel's MAX_RT_ERR_OEN_A (0x2D) register bit.	0b0: None of the selected channels have reached the maximum retry limit 0b1: One or more of the selected channels has reached the maximum retry limit

INTR12 (0x2F)

BIT	7	6	5	4	3	2	1	0
Field	ERR_TX_EN	MEM_ERR_OEN	–	ERR_TX_ID[4:0]				
Reset	0b1	0b0	–	0x1F				
Access Type	Write, Read	Write, Read	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_TX_EN	7	Transmits local error status (inverse of ERRB pin level) to remote side through GPIO channel.	0b0: Do not transmit local error status to remote side through GPIO channel 0b1: Transmit local error status to remote side through GPIO channel
MEM_ERR_OEN	6	Enables reporting of line memory read/write errors at ERRB pin.	0b0: Disable MEM_ERR error reporting at ERRB pin 0b1: Enable MEM_ERR error reporting at ERRB pin
ERR_TX_ID	4:0	GPIO ID used for transmitting ERR_TX.	0bXXXXX: GPIO ID used for transmitting ERR_TX

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INTR13 (0x30)

BIT	7	6	5	4	3	2	1	0
Field	ERR_RX_EN_A	RSVD	–	ERR_RX_ID_A[4:0]				
Reset	0b1	0b1	–	0x1F				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_RX_EN_A	7	Receives remote error status (inverse of ERRB pin level) through GPIO channel for GMSL2 Link A.	0b0: Do not receive remote error status through GPIO channel for GMSL2 Link A 0b1: Receive remote error status through GPIO channel for GMSL2 Link A
ERR_RX_ID_A	4:0	GPIO ID used for receiving ERR_RX for GMSL2 Link A.	0bXXXXX: GPIO ID used for receiving ERR_RX Link A

INTR14 (0x31)

BIT	7	6	5	4	3	2	1	0
Field	ERR_RX_EN_B	RSVD	–	ERR_RX_ID_B[4:0]				
Reset	0b1	0b1	–	0x1F				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_RX_EN_B	7	Receives remote error status (inverse of ERRB pin level) through GPIO channel for GMSL2 Link B.	0b0: Do not receive remote error status through GPIO channel for GMSL2 Link B 0b1: Receive remote error status through GPIO channel for GMSL2 Link B
ERR_RX_ID_B	4:0	GPIO ID used for receiving ERR_RX for GMSL2 Link B.	0bXXXXX: GPIO ID used for receiving ERR_RX Link B

INTR15 (0x32)

BIT	7	6	5	4	3	2	1	0
Field	ERR_RX_EN_C	RSVD	–	ERR_RX_ID_C[4:0]				
Reset	0b1	0b1	–	0x1F				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_RX_EN_C	7	Receives remote error status (inverse of ERRB pin level) through GPIO channel for GMSL2 Link C.	0b0: Do not receive remote error status through GPIO channel for GMSL2 Link C 0b1: Receive remote error status through GPIO channel for GMSL2 Link C
ERR_RX_ID_C	4:0	GPIO ID used for receiving ERR_RX for GMSL2 link C	0bXXXXX: GPIO ID used for receiving ERR_RX link C

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INTR16 (0x33)

BIT	7	6	5	4	3	2	1	0
Field	ERR_RX_EN_D	RSVD	–	ERR_RX_ID_D[4:0]				
Reset	0b1	0b1	–	0x1F				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_RX_EN_D	7	Receives remote error status (inverse of ERRB pin level) through GPIO channel for GMSL2 Link D.	0b0: Do not receive remote error status through GPIO channel for GMSL2 Link D 0b1: Receive remote error status through GPIO channel for GMSL2 Link D
ERR_RX_ID_D	4:0	GPIO ID used for receiving ERR_RX for GMSL2 link D	0bXXXXX: GPIO ID used for receiving ERR_RX link D

CNT0 (0x35)

BIT	7	6	5	4	3	2	1	0
Field	DEC_ERR_A[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
DEC_ERR_A	7:0	The number of decoding (disparity) errors detected at Link A Reset after reading or with the rising edge of LOCK.	0xXX: Number of Link A decoding errors detected

CNT1 (0x36)

BIT	7	6	5	4	3	2	1	0
Field	DEC_ERR_B[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
DEC_ERR_B	7:0	The number of decoding (disparity) errors detected at Link B Reset after reading or with the rising edge of LOCK.	0xXX: Number of Link B decoding errors detected

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CNT2 (0x37)

BIT	7	6	5	4	3	2	1	0
Field	DEC_ERR_C[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
DEC_ERR_C	7:0	The number of decoding (disparity) errors detected at Link C Reset after reading or with the rising edge of LOCK.	0xXX: Number of Link C decoding errors detected

CNT3 (0x38)

BIT	7	6	5	4	3	2	1	0
Field	DEC_ERR_D[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
DEC_ERR_D	7:0	The number of decoding (disparity) errors detected at Link D Reset after reading or with the rising edge of LOCK.	0xXX: Number of Link D decoding errors detected

CNT4 (0x39)

BIT	7	6	5	4	3	2	1	0
Field	IDLE_ERR_A[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
IDLE_ERR_A	7:0	The number of idle word errors detected at Link A Reset after reading or with the rising edge of LOCK.	0xXX: Number of idle word errors detected

CNT5 (0x3A)

BIT	7	6	5	4	3	2	1	0
Field	IDLE_ERR_B[7:0]							
Reset	0x00							
Access Type	Read Clears All							

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BITFIELD	BITS	DESCRIPTION	DECODE
IDLE_ERR_B	7:0	The number of idle word errors detected at Link B Reset after reading or with the rising edge of LOCK.	0xXX: Number of idle word errors detected

CNT6 (0x3B)

BIT	7	6	5	4	3	2	1	0
Field	IDLE_ERR_C[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
IDLE_ERR_C	7:0	The number of idle word errors detected at Link C Reset after reading or with the rising edge of LOCK.	0xXX: Number of idle word errors detected

CNT7 (0x3C)

BIT	7	6	5	4	3	2	1	0
Field	IDLE_ERR_D[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
IDLE_ERR_D	7:0	Number of idle word errors detected at Link D Reset after reading or with the rising edge of LOCK.	0xXX: Number of idle word errors detected

CNT8 (0x40)

BIT	7	6	5	4	3	2	1	0
Field	PKT_CNT_A[7:0]							
Reset	0x00							
Access Type	Read Clears All							

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BITFIELD	BITS	DESCRIPTION	DECODE
PKT_CNT_A	7:0	The Number of Received Packets of a Selected Type at Link A Packet type is selected with the associated PKT_CNT_SEL bitfield (0x1004). Reported packet count is a scaled value, such that actual packet count is ≥ PKT_CNT_A x ($2^{PKT_CNT_EXP}$) and < (PKT_CNT_A + 1) x ($2^{PKT_CNT_EXP}$). (PKT_CNT_EXP bitfield is at 0x24.) When maximum value is reported, packet count is greater or equal to the reported value.	0xXX: Scaled number of received packets

CNT9 (0x41)

BIT	7	6	5	4	3	2	1	0
Field	PKT_CNT_B[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
PKT_CNT_B	7:0	The Number of Received Packets of a Selected Type at Link B Packet type is selected with the associated PKT_CNT_SEL bitfield (0x1014). Reported packet count is a scaled value, such that actual packet count is ≥ PKT_CNT_B x ($2^{PKT_CNT_EXP}$) and < (PKT_CNT_B + 1) x ($2^{PKT_CNT_EXP}$). (PKT_CNT_EXP bitfield is at 0x24.) When maximum value is reported, packet count is greater or equal to the reported value.	0xXX: Scaled number of received packets

CNT10 (0x42)

BIT	7	6	5	4	3	2	1	0
Field	PKT_CNT_C[7:0]							
Reset	0x00							
Access Type	Read Clears All							

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BITFIELD	BITS	DESCRIPTION	DECODE
PKT_CNT_C	7:0	The Number of Received Packets of a Selected Type at Link C Packet type is selected with the associated PKT_CNT_SEL bitfield (0x1024). Reported packet count is a scaled value, such that actual packet count is ≥ PKT_CNT_C x ($2^{PKT_CNT_EXP}$) and < (PKT_CNT_C + 1) x ($2^{PKT_CNT_EXP}$). (PKT_CNT_EXP bitfield is at 0x24.) When maximum value is reported, packet count is greater or equal to the reported value.	0xXX: Scaled number of received packets

CNT11 (0x43)

BIT	7	6	5	4	3	2	1	0
Field	PKT_CNT_D[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
PKT_CNT_D	7:0	The Number of Received Packets of a Selected Typeat Link D Packet type is selected with the associated PKT_CNT_SEL bitfield (0x1034). Reported packet count is a scaled value, such that actual packet count is ≥ PKT_CNT_D x ($2^{PKT_CNT_EXP}$) and < (PKT_CNT_D + 1) x ($2^{PKT_CNT_EXP}$). (PKT_CNT_EXP bitfield is at 0x24.) When maximum value is reported, packet count is greater or equal to the reported value.	0xXX: Scaled number of received packets

VID_PXL_CRC_ERR_OEN (0x44)

BIT	7	6	5	4	3	2	1	0
Field	MEM_ECC_ERR2_OEN	MEM_ECC_ERR1_OEN	–	–	VID_PXL_CRC_ERR_OEN_D	VID_PXL_CRC_ERR_OEN_C	VID_PXL_CRC_ERR_OEN_B	VID_PXL_CRC_ERR_OEN_A
Reset	0x1	0x0	–	–	0x1	0x1	0x1	0x1
Access Type	Write, Read	Write, Read	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MEM_ECC_ERR2_OEN	7	Enables reporting of memory ECC 2-bit uncorrectable errors at ERRB pin.	0b0: Disable reporting of 2b ECC memory errors 0b1: Enable reporting of 2b ECC memory errors

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BITFIELD	BITS	DESCRIPTION	DECODE
MEM_ECC_ERR1_OEN	6	Enables reporting of memory ECC 1-bit correctable errors at ERRB pin.	0b0: Disable reporting of 1b ECC memory errors 0b1: Enable reporting of 1b ECC memory errors
VID_PXL_CRC_ERR_OEN_D	3	Video Pixel CRC Error Counter Interrupt Output Enable	0b0: Disable video pixel CRC error counter interrupt output 0b1: Enable video pixel CRC error counter interrupt output
VID_PXL_CRC_ERR_OEN_C	2	Video Pixel CRC Error Counter Interrupt Output Enable	0b0: Disable video pixel CRC error counter interrupt output 0b1: Enable video pixel CRC error counter interrupt output
VID_PXL_CRC_ERR_OEN_B	1	Video Pixel CRC Error Counter Interrupt Output Enable	0b0: Disable video pixel CRC error counter interrupt output 0b1: Enable video pixel CRC error counter interrupt output
VID_PXL_CRC_ERR_OEN_A	0	Video Pixel CRC Error Counter Interrupt Output Enable	0b0: Disable video pixel CRC error counter interrupt output 0b1: Enable video pixel CRC error counter interrupt output

VID_PXL_CRC_ERR_INT (0x45)

BIT	7	6	5	4	3	2	1	0
Field	MEM_ECC_ERR2_INT	MEM_ECC_ERR1_INT	–	–	VID_PXL_CRC_ERR_D	VID_PXL_CRC_ERR_C	VID_PXL_CRC_ERR_B	VID_PXL_CRC_ERR_A
Reset	0b0	0b0	–	–	0x0	0x0	0x0	0x0
Access Type	Read Only	Read Only	–	–	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
MEM_ECC_ERR2_INT	7	Decoding Error Flag for 2-bit Uncorrectable Memory ECC Errors Asserted when MEM_ECC_ERR2_CNT (0x1252) ≥ MEM_ECC_ERR2_THR (0x1250).	0b0: 2b ECC memory error not detected 0b1: 2b ECC memory error detected
MEM_ECC_ERR1_INT	6	Decoding Error Flag for 1-bit Correctable Memory ECC Errors Asserted when MEM_ECC_ERR1_CNT (0x1251) ≥ MEM_ECC_ERR1_THR (0x1250).	0b0: 1b ECC memory error not detected 0b1: 1b ECC memory error detected
VID_PXL_CRC_ERR_D	3	Video Pixel CRC Error Counter Interrupt	0b0: No video pixel CRC error counter interrupt detected 0b1: Video pixel CRC error counter interrupt detected
VID_PXL_CRC_ERR_C	2	Video Pixel CRC Error Counter Interrupt	0b0: No video pixel CRC error counter interrupt detected 0b1: Video pixel CRC error counter interrupt detected
VID_PXL_CRC_ERR_B	1	Video Pixel CRC Error Counter Interrupt	0b0: No video pixel CRC error counter interrupt detected 0b1: Video pixel CRC error counter interrupt detected

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BITFIELD	BITS	DESCRIPTION	DECODE
VID_PXL_CRC_ERR_A	0	Video Pixel CRC Error Counter Interrupt	0b0: No video pixel CRC error counter interrupt detected 0b1: Video pixel CRC error counter interrupt detected

PWR_STATUS_OEN (0x46)

BIT	7	6	5	4	3	2	1	0
Field	VDDCMP_INT_OEN	RSVD	VDDBAD_INT_OEN	RSVD[4:0]				
Reset	0x1	0x1	0x1	0x07				
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
VDDCMP_INT_OEN	7	Enables reporting of V_{DD} comparator interrupt (VDDCMP_INT_FLAG) at ERRB pin	0b0: ERRB reporting disabled 0b1: ERRB reporting enabled
VDDBAD_INT_OEN	5	Enables reporting of VDDBAD interrupt (VDDBAD_INT_FLAG) at ERRB pin	0b0: ERRB reporting disabled 0b1: ERRB reporting enabled

PWR_STATUS_FLAG (0x47)

BIT	7	6	5	4	3	2	1	0
Field	VDDCMP_INT_FLAG	RSVD	VDDBAD_INT_FLAG	–	–	–	–	–
Reset	0x0	0x0	0x0	–	–	–	–	–
Access Type	Read Clears All		Read Clears All	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
VDDCMP_INT_FLAG	7	Combined V_{DD} Comparator Output Flag. See CMP_STATUS for details of error states that drive this flag. To clear, first read CMP_STATUS and then read VDDCMP_INT_FLAG.	0b0: No V_{DD} comparator error 0b1: V_{DD} comparator error state asserted
VDDBAD_INT_FLAG	5	Combined V_{DD} Bad Indicator. See VDDBAD_STATUS for details for error states that drive this flag. To clear, first read VDDBAD_STATUS and then read VDDBAD_INT_FLAG.	0b0: No V_{DD} bad error 0b1: V_{DD} bad error state asserted

PM_OV_STAT (0x48)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	RSVD	RSVD[1:0]		OV_LEVEL[1:0]	
Reset	–	–	–	0x0	0x1		0x1	
Access Type	–	–	–				Write, Read	

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BITFIELD	BITS	DESCRIPTION	DECODE
OV_LEVEL	1:0	V_{DD_sw} overvoltage comparator trip level V_{trip_ov}	0x0: 1.12 0x1: 1.14 0x2: 1.17 0x3: 1.20

VIDEO_MASKED_OEN (0x49)

BIT	7	6	5	4	3	2	1	0
Field	–	–	CMP_VTERM_MASK	VDD_OV_OEN	VIDEO_MASKED_3_OEN	VIDEO_MASKED_2_OEN	VIDEO_MASKED_1_OEN	VIDEO_MASKED_0_OEN
Reset	–	–	0x1	0x0	0x1	0x1	0x1	0x1
Access Type	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CMP_VTERM_MASK	5	Select V_{DD} comparator V_{TERM} status to drive VDDCMP error flag and ERRB pin	0b0: Disable V_{TERM} comparator error reporting 0b1: Enable V_{TERM} comparator error reporting
VDD_OV_OEN	4	Enable V_{DD} overvoltage status on ERRB	0b0: Do not enable V_{DD} overvoltage status 0b1: Enable V_{DD} overvoltage status
VIDEO_MASKED_3_OEN	3	Enable Video Masked 3 status on ERRB	0b0: Disable reporting of Video Masked 3 Interrupt at ERRB pin 0b1: Enable reporting of Video Masked 3 Interrupt at ERRB pin
VIDEO_MASKED_2_OEN	2	Enable Video Masked 2 status on ERRB	0b0: Disable reporting of Video Masked 2 Interrupt at ERRB pin 0b1: Enable reporting of Video Masked 2 Interrupt at ERRB pin
VIDEO_MASKED_1_OEN	1	Enable Video Masked 1 status on ERRB	0b0: Disable reporting of Video Masked 1 Interrupt at ERRB pin 0b1: Enable reporting of Video Masked 1 Interrupt at ERRB pin
VIDEO_MASKED_0_OEN	0	Enable Video Masked 0 status on ERRB	0b0: Disable reporting of Video Masked 0 Interrupt at ERRB pin 0b1: Enable reporting of Video Masked 0 Interrupt at ERRB pin

VIDEO_MASKED_FLAG (0x4A)

BIT	7	6	5	4	3	2	1	0
Field	–	–	CMP_VTERM_STATUS	VDD_OV_FLAG	VIDEO_MASKED_3_FLAG	VIDEO_MASKED_2_FLAG	VIDEO_MASKED_1_FLAG	VIDEO_MASKED_0_FLAG
Reset	–	–	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	–	–	Read Only	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

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BITFIELD	BITS	DESCRIPTION	DECODE
CMP_VTERM_STATUS	5	Power Manager V_{TERM} Comparator Status. Latched low when switched V_{TERM} supply < 1V. Cleared when the CMP_STATUS word (register 0x12) is read and the switched V_{TERM} supply is > 1V.	0b0: V_{TERM} < 1V (latched low, read to clear) 0b1: V_{TERM} > 1V
VDD_OV_FLAG	4	V_{DD} Overvoltage Indication. This bit is sticky. It is set when V_{DD} is over the overvoltage threshold. It is cleared when read. See OV_LEVEL register for overvoltage threshold value.	0b0: V_{DD_sw} overvoltage condition not detected 0b1: V_{DD_sw} overvoltage condition detected (latched, read to clear)
VIDEO_MASKED_3_FLAG	3	Sticky Status value for Video Masked 3. Flag will be set if any of the video pipes used in Controller 3 synchronous aggregation lose video lock. See video_masked registers in MIPI_TX_x registers to determine which video pipe has been masked.	0b0: Video not masked in Controller 3 synchronous aggregation 0b1: Video masked in at least one pipe in Controller 3 synchronous aggregation
VIDEO_MASKED_2_FLAG	2	Sticky Status value for Video Masked 2. Flag will be set if any of the video pipes used in Controller 2 synchronous aggregation lose video lock. See video_masked registers in MIPI_TX_x registers to determine which video pipe has been masked.	0b0: Video not masked in Controller 2 synchronous aggregation 0b1: Video masked in at least one pipe in Controller 2 synchronous aggregation
VIDEO_MASKED_1_FLAG	1	Sticky Status value for Video Masked 1. Flag will be set if any of the video pipes used in Controller 1 synchronous aggregation lose video lock. See video_masked registers in MIPI_TX_x registers to determine which video pipe has been masked.	0b0: Video not masked in Controller 1 synchronous aggregation 0b1: Video masked in at least one pipe in Controller 1 synchronous aggregation
VIDEO_MASKED_0_FLAG	0	Sticky Status value for Video Masked 0. Flag will be set if any of the video pipes used in Controller 0 synchronous aggregation lose video lock. See video_masked registers in MIPI_TX_x registers to determine which video pipe has been masked.	0b0: Video not masked in Controller 0 synchronous aggregation 0b1: Video masked in at least one pipe in Controller 0 synchronous aggregation

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DEV_REV (0x4C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	DEV_REV[3:0]			
Reset	–	–	–	–	0x5			
Access Type	–	–	–	–	Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
DEV_REV	3:0	Device Revision A1 -0 A2 -1 B1 -2 C1 -3 D1 -4 E1 -5	0xX: Device revision number

RX0 (0x50)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	STR_SEL[1:0]	
Reset	–	–	–	–	–	–	0x0	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
STR_SEL	1:0	Receives packets with selected stream ID.	0bXX: Receive packets with this stream ID

RX0 (0x51)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	STR_SEL[1:0]	
Reset	–	–	–	–	–	–	0x1	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
STR_SEL	1:0	Receives packets with selected stream ID.	0bXX: Receive packets with this stream ID

RX0 (0x52)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	STR_SEL[1:0]	
Reset	–	–	–	–	–	–	0x2	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
STR_SEL	1:0	Receives packets with selected stream ID.	0bXX: Receive packets with this stream ID

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RX0 (0x53)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	STR_SEL[1:0]	
Reset	–	–	–	–	–	–	0x3	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
STR_SEL	1:0	Receives packets with selected stream ID.	0bXX: Receive packets with this stream ID

RX0 (0x54)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	STR_SEL_B[1:0]	
Reset	–	–	–	–	–	–	0x0	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
STR_SEL_B	1:0	Receives packets with selected stream ID.	0bXX: Receive packets with this stream ID

RX0 (0x55)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	STR_SEL_B[1:0]	
Reset	–	–	–	–	–	–	0x1	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
STR_SEL_B	1:0	Receives packets with selected stream ID.	0bXX: Receive packets with this stream ID

RX0 (0x56)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	STR_SEL_B[1:0]	
Reset	–	–	–	–	–	–	0x2	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
STR_SEL_B	1:0	Receives packets with selected stream ID.	0bXX: Receive packets with this stream ID

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RX0 (0x57)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	STR_SEL_B[1:0]	
Reset	–	–	–	–	–	–	0x3	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
STR_SEL_B	1:0	Receives packets with selected stream ID.	0bXX: Receive packets with this stream ID

RX0 (0x58)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	STR_SEL_C[1:0]	
Reset	–	–	–	–	–	–	0x0	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
STR_SEL_C	1:0	Receives packets with selected stream ID.	0bXX: Receive packets with this stream ID

RX0 (0x59)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	STR_SEL_C[1:0]	
Reset	–	–	–	–	–	–	0x1	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
STR_SEL_C	1:0	Receives packets with selected stream ID.	0bXX: Receive packets with this stream ID

RX0 (0x5A)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	STR_SEL_C[1:0]	
Reset	–	–	–	–	–	–	0x2	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
STR_SEL_C	1:0	Receives packets with selected stream ID.	0bXX: Receive packets with this stream ID

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RX0 (0x5B)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	STR_SEL_C[1:0]	
Reset	–	–	–	–	–	–	0x3	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
STR_SEL_C	1:0	Receives packets with selected stream ID.	0bXX: Receive packets with this stream ID

RX0 (0x5C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	STR_SEL_D[1:0]	
Reset	–	–	–	–	–	–	0x0	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
STR_SEL_D	1:0	Receives packets with selected stream ID.	0bXX: Receive packets with this stream ID

RX0 (0x5D)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	STR_SEL_D[1:0]	
Reset	–	–	–	–	–	–	0x1	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
STR_SEL_D	1:0	Receives packets with selected stream ID.	0bXX: Receive packets with this stream ID

RX0 (0x5E)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	STR_SEL_D[1:0]	
Reset	–	–	–	–	–	–	0x2	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
STR_SEL_D	1:0	Receives packets with selected stream ID.	0bXX: Receive packets with this stream ID

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RX0 (0x5F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	STR_SEL_D[1:0]	
Reset	–	–	–	–	–	–	0x3	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
STR_SEL_D	1:0	Receives packets with selected stream ID.	0bXX: Receive packets with this stream ID

CFGH_VIDEO_CRC0 (0x60)

BIT	7	6	5	4	3	2	1	0
Field	RX_CRC_EN_A_B[7:0]							
Reset	0b0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_CRC_EN_A_B	7:0	Received Packet CRC Enable for Ports A and B Each bit enables CRC for one pipe within a GMSL link as described below. Setting a given bit indicates that packets received at the corresponding port/pipe have appended CRC and CRC checking must be performed at each packet. bit 0: RX_CRC_EN_A_VIDEO_X bit 1: RX_CRC_EN_A_VIDEO_Y bit 2: RX_CRC_EN_A_VIDEO_Z bit 3: RX_CRC_EN_A_VIDEO_U bit 4: RX_CRC_EN_B_VIDEO_X bit 5: RX_CRC_EN_B_VIDEO_Y bit 6: RX_CRC_EN_B_VIDEO_Z bit 7: RX_CRC_EN_B_VIDEO_U	0bXXXXXXX0: No CRC on received packets—RX_CRC_EN_A_VIDEO_X 0bXXXXXXX1: Received packets have CRC and checking is enabled—RX_CRC_EN_A_VIDEO_X 0bXXXXXX0X: No CRC on received packets—RX_CRC_EN_A_VIDEO_Y 0bXXXXXX1X: Received packets have CRC and checking is enabled— RX_CRC_EN_A_VIDEO_Y ... ... 0b0XXXXXXX: No CRC on received packets—RX_CRC_EN_B_VIDEO_U 0b1XXXXXXX: Received packets have CRC and checking is enabled— RX_CRC_EN_B_VIDEO_U

CFGH_VIDEO_CRC1 (0x61)

BIT	7	6	5	4	3	2	1	0
Field	RX_CRC_EN_C_D[7:0]							
Reset	0b0							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
RX_CRC_EN_C_D	7:0	Received Packet CRC Enable for Ports C and D Each bit enables CRC for one pipe within a GMSL link as described below. Setting a given bit indicates that packets received at the corresponding port/pipe have appended CRC and CRC checking must be performed at each packet. bit 0: RX_CRC_EN_C_VIDEO_X bit 1: RX_CRC_EN_C_VIDEO_Y bit 2: RX_CRC_EN_C_VIDEO_Z bit 3: RX_CRC_EN_C_VIDEO_U bit 4: RX_CRC_EN_D_VIDEO_X bit 5: RX_CRC_EN_D_VIDEO_Y bit 6: RX_CRC_EN_D_VIDEO_Z bit 7: RX_CRC_EN_D_VIDEO_U	0bXXXXXXX0: No CRC on received packets—RX_CRC_EN_C_VIDEO_X 0bXXXXXXX1: Received packets have CRC and checking is enabled—RX_CRC_EN_C_VIDEO_X 0bXXXXXX0X: No CRC on received packets—RX_CRC_EN_C_VIDEO_Y 0bXXXXXX1X: Received packets have CRC and checking is enabled— RX_CRC_EN_C_VIDEO_Y ... ... 0b0XXXXXXX: No CRC on received packets—RX_CRC_EN_D_VIDEO_U 0b1XXXXXXX: Received packets have CRC and checking is enabled— RX_CRC_EN_D_VIDEO_U

TR0 (0x70)

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		RSVD[1:0]	
Reset	0b1	0b1	0x3		0x0		0x0	
Access Type	Write, Read	Write, Read	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN	7	When set, calculates and appends CRC to each packet transmitted from this port.	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled
RX_CRC_EN	6	When set, indicates that packets received at this port have appended CRC, and CRC checking should be performed at each packet.	0b0: Receive CRC disabled 0b1: Receive CRC enabled
PRIO_VAL	3:2	Sets the priority for this channel's packet requests.	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority

TR1 (0x71)

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT[1:0]		BW_VAL[5:0]					
Reset	0x2		0x30					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT	7:6	Channel bandwidth-allocation multiplication factor.	0b00: Multiply BW_VAL by 1 0b01: Multiply BW_VAL by 4 0b10: Multiply BW_VAL by 16 0b11: Multiply BW_VAL by 16

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BITFIELD	BITS	DESCRIPTION	DECODE
BW_VAL	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL x BW_MULT/10 as a percentage of total link bandwidth.	0bXXXXXX: Channel base-bandwidth value

TR2 (0x72)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TX_SRC_ID[2:0]		
Reset	–	–	–	–	–	0x0		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID	2:0	Source identifier used in packets transmitted from this port. Default value is set by CFG0 pin.	0bXXX: Source ID for packets from this channel

TR3 (0x73)

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL	7:0	Receives packets from selected sources Each bit indicates whether packets with that source ID should be received or not. For example, when RX_SRC_SEL = 00001001, then packets with source ID equal to 0 and 3 will be received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received ... ... 0xFF: Packets from all source IDs received

TR0 (0x74)

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN_B	RX_CRC_EN_B	RSVD[1:0]		PRIO_VAL_B[1:0]		RSVD[1:0]	
Reset	0b1	0b1	0x3		0x0		0x0	
Access Type	Write, Read	Write, Read			Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN_B	7	When set, calculates and appends CRC to each packet transmitted from this port.	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled

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BITFIELD	BITS	DESCRIPTION	DECODE
RX_CRC_EN_B	6	When set, indicates that packets received at this port have appended CRC, and CRC checking should be performed at each packet.	0b0: Receive CRC disabled 0b1: Receive CRC enabled
PRIO_VAL_B	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority

TR1 (0x75)

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT_B[1:0]		BW_VAL_B[5:0]					
Reset	0x2		0x30					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT_B	7:6	Channel bandwidth-allocation multiplication factor.	0b00: Multiply BW_VAL_B by 1 0b01: Multiply BW_VAL_B by 4 0b10: Multiply BW_VAL_B by 16 0b11: Multiply BW_VAL_B by 16
BW_VAL_B	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL_B x BW_MULT_B/10 as a percentage of total link bandwidth	0bXXXXXX: Channel base-bandwidth value

TR2 (0x76)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TX_SRC_ID_B[2:0]		
Reset	–	–	–	–	–	0x0		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID_B	2:0	Source identifier used in packets transmitted from this port. Default value is set by CFG0 pin.	0bXXX: Source ID for packets from this channel

TR3 (0x77)

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL_B[7:0]							
Reset	0xFF							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL_B	7:0	Receives packets from selected sources Each bit indicates whether packets with that source ID should be received or not. For example, when RX_SRC_SEL_B = 00001001, then packets with source ID equal to 0 and 3 will be received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received ... ... 0xFF: Packets from all source IDs received

TR0 (0x78)

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN_C	RX_CRC_EN_C	RSVD[1:0]		PRIO_VAL_C[1:0]		RSVD[1:0]	
Reset	0b1	0b1	0x3		0x0		0x0	
Access Type	Write, Read	Write, Read			Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN_C	7	When set, calculates and appends CRC to each packet transmitted from this port.	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled
RX_CRC_EN_C	6	When set, indicates that packets received at this port have appended CRC, and CRC checking should be performed at each packet.	0b0: Receive CRC disabled 0b1: Receive CRC enabled
PRIO_VAL_C	3:2	Sets the priority for this channel's packet requests.	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority

TR1 (0x79)

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT_C[1:0]		BW_VAL_C[5:0]					
Reset	0x2		0x30					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT_C	7:6	Channel bandwidth-allocation multiplication factor	0b00: Multiply BW_VAL_C by 1 0b01: Multiply BW_VAL_C by 4 0b10: Multiply BW_VAL_C by 16 0b11: Multiply BW_VAL_C by 16
BW_VAL_C	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL_C x BW_MULT_C/10 as a percentage of total link bandwidth	0bXXXXXX: Channel base-bandwidth value

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TR2 (0x7A)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TX_SRC_ID_C[2:0]		
Reset	–	–	–	–	–	0x0		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID_C	2:0	Source identifier used in packets transmitted from this port. Default value is set by CFG0 pin.	0bXXX: Source ID for packets from this channel

TR3 (0x7B)

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL_C[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL_C	7:0	Receives packets from selected sources Each bit indicates whether packets with that source ID should be received or not. For example, when RX_SRC_SEL_C = 00001001, then packets with source ID equal to 0 and 3 will be received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received ... ... 0xFF: Packets from all source IDs received

TR0 (0x7C)

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN_D	RX_CRC_EN_D	RSVD[1:0]		PRIO_VAL_D[1:0]		RSVD[1:0]	
Reset	0b1	0b1	0x3		0x0		0x0	
Access Type	Write, Read	Write, Read			Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN_D	7	When set, calculates and appends CRC to each packet transmitted from this port	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled
RX_CRC_EN_D	6	When set, indicates that packets received at this port have appended CRC, and CRC checking should be performed at each packet.	0b0: Receive CRC disabled 0b1: Receive CRC enabled
PRIO_VAL_D	3:2	Sets the priority for this channel's packet requests.	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority

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TR1 (0x7D)

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT_D[1:0]		BW_VAL_D[5:0]					
Reset	0x2		0x30					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT_D	7:6	Channel bandwidth-allocation multiplication factor	0b00: Multiply BW_VAL_D by 1 0b01: Multiply BW_VAL_D by 4 0b10: Multiply BW_VAL_D by 16 0b11: Multiply BW_VAL_D by 16
BW_VAL_D	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL_D x BW_MULT_D/10 as a percentage of total link bandwidth	0bXXXXXX: Channel base-bandwidth value

TR2 (0x7E)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TX_SRC_ID_D[2:0]		
Reset	–	–	–	–	–	0x0		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID_D	2:0	Source identifier used in packets transmitted from this port. Default value is set by CFG0 pin.	0bXXX: Source ID for packets from this channel

TR3 (0x7F)

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL_D[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL_D	7:0	Receives packets from selected sources Each bit indicates whether packets with that source ID should be received or not. For example, when RX_SRC_SEL_D = 00001001, then packets with source ID equal to 0 and 3 will be received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received ... ... 0xFF: Packets from all source IDs received

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TR0 (0x80)

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
Reset	0b1	0b1	0x3		0x0		0x0	
Access Type	Write, Read	Write, Read			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN	7	When set, calculate and append CRC to each packet transmitted from this port.	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled
RX_CRC_EN	6	When set, indicates that packets received at this port have appended CRC, and CRC checking should be performed at each packet.	0b0: Receive CRC disabled 0b1: Receive CRC enabled
PRIO_VAL	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG	1:0	Adjust the priority used for this channel.	0b00: Current channel priority is used 0b01: Increase current channel priority 0b10: Decrease current channel priority 0b11: Reset to channel PRIO_VAL[1:0] setting

TR1 (0x81)

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT[1:0]		BW_VAL[5:0]					
Reset	0x2		0x30					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT	7:6	Channel bandwidth-allocation multiplication factor.	0b00: Multiply BW_VAL by 1 0b01: Multiply BW_VAL by 4 0b10: Multiply BW_VAL by 16 0b11: Multiply BW_VAL by 16
BW_VAL	5:0	Channel bandwidth allocation base. Fair bandwidth use ratio = BW_VAL x BW_MULT/10 as a percentage of total link bandwidth.	0bXXXXXX: Channel base-bandwidth value

TR3 (0x83)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TX_SRC_ID[2:0]		
Reset	–	–	–	–	–	0x0		
Access Type	–	–	–	–	–	Write, Read		

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BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID	2:0	Source identifier used in packets transmitted from this port. Default value is set by CFG0 pin.	0bXXX: Source ID for packets from this channel

TR4 (0x84)

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL	7:0	Receives packets from selected sources Each bit indicates whether packets with that source ID should be received or not. For example, when RX_SRC_SEL = 00001001, then packets with source ID equal to 0 and 3 will be received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received ... ... 0xFF: Packets from all source IDs received

ARQ0 (0x85)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	RSVD	ACK_SRC_ID	ARQ_EN	ARQ_EN	–	–
Reset	–	0b0	0b0	0b1	0b1	0b0	–	–
Access Type	–			Write, Read	Write, Read	Write, Read	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
ACK_SRC_ID	4	Selects what to use as SRC_ID in transmitted acknowledge packets	0b0: Use SRC_ID of the received data packet 0b1: Use TX_SRC_ID register
ARQ_EN	3	Enable ARQ	0b0: ARQ disabled 0b1: ARQ enabled
ARQ_EN	2	Disables retransmission due to receiving same ACK twice	0b0: Enabled 0b1: Disabled

ARQ1 (0x86)

BIT	7	6	5	4	3	2	1	0
Field	–	MAX_RT[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
Reset	–	0x7			–	–	0b1	0b0
Access Type	–	Write, Read			–	–	Write, Read	Write, Read

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BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT	6:4	Maximum Retransmit Limit ARQ will stop retransmission after trying retransmit for this many times for a single packet.	0bXXX: Maximum retransmit limit
MAX_RT_ERR_OEN	1	Enables reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR—0x87) for this channel at ERRB pin.	0b0: ARQ maximum retransmit limit errors reporting at ERRB pin disabled 0b1: ARQ maximum retransmit limit errors reporting at ERRB pin enabled
RT_CNT_OEN	0	Enables reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT (0x87) of this channel is greater than 0.	0b0: ARQ retransmission count reporting at ERRB pin disabled 0b1: ARQ retransmission count reporting at ERRB pin enabled

ARQ2 (0x87)

BIT	7	6	5	4	3	2	1	0
Field	MAX_RT_ERR	RT_CNT[6:0]						
Reset	0b0	0x0						
Access Type	Read Clears All	Read Clears All						

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR	7	Reached maximum retransmit limit (MAX_RT—0x86) for one packet in this channel.	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT	6:0	Total retransmission count in this channel.	0bXXXXXXX: Count of retransmissions for this channel

TR0 (0x90)

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		RSVD[1:0]	
Reset	0b1	0b1	0x3		0x0		0x0	
Access Type	Write, Read	Write, Read			Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN	7	When set, calculates and appends CRC to each packet transmitted from this port.	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled
RX_CRC_EN	6	When set, indicates that packets received at this port have appended CRC, and CRC checking should be performed at each packet.	0b0: Receive CRC disabled 0b1: Receive CRC enabled
PRIO_VAL	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority

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TR1 (0x91)

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT[1:0]		BW_VAL[5:0]					
Reset	0x2		0x30					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT	7:6	Channel bandwidth-allocation multiplication factor	0b00: Multiply BW_VAL by 1 0b01: Multiply BW_VAL by 4 0b10: Multiply BW_VAL by 16 0b11: Multiply BW_VAL by 16
BW_VAL	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL x BW_MULT/10 as a percentage of total link bandwidth	0bXXXXXX: Channel base-bandwidth value

TR3 (0x93)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TX_SRC_ID[2:0]		
Reset	–	–	–	–	–	0x0		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID	2:0	Source identifier used in packets transmitted from this port. Default value is set by CFG0 pin.	0bXXX: Source ID for packets from this channel

TR4 (0x94)

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL	7:0	Receives packets from selected sources Each bit indicates whether packets with that source ID should be received or not. For example, when RX_SRC_SEL = 00001001, then packets with source ID equal to 0 and 3 will be received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received ... ... 0xFF: Packets from all source IDs received

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ARQ0 (0x95)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	RSVD	RSVD	ARQ_EN	ARQ_EN	–	–
Reset	–	0b0	0b0	0b1	0b1	0b0	–	–
Access Type	–				Write, Read	Write, Read	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
ARQ_EN	3	Enables ARQ	0b0: ARQ disabled 0b1: ARQ enabled
ARQ_EN	2	Disables retransmission due to receiving same ACK twice	0b0: Enabled 0b1: Disabled

ARQ1 (0x96)

BIT	7	6	5	4	3	2	1	0
Field	–	MAX_RT[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
Reset	–	0x7			–	–	0b1	0b0
Access Type	–	Write, Read			–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT	6:4	Maximum Retransmit Limit ARQ will stop retransmission after trying retransmit for this many times for a single packet.	0bXXX: Maximum retransmit limit
MAX_RT_ERR_OEN	1	Enables reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR—0x97) for this channel at ERRB pin	0b0: ARQ maximum retransmit limit errors reporting at ERRB pin disabled 0b1: ARQ maximum retransmit limit errors reporting at ERRB pin enabled
RT_CNT_OEN	0	Enables reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT (0x97) of this channel is greater than 0.	0b0: ARQ retransmission count reporting at ERRB pin disabled 0b1: ARQ retransmission count reporting at ERRB pin enabled

ARQ2 (0x97)

BIT	7	6	5	4	3	2	1	0
Field	MAX_RT_ERR	RT_CNT[6:0]						
Reset	0b0	0x0						
Access Type	Read Clears All	Read Clears All						

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR	7	Reached maximum retransmit limit (MAX_RT) for one packet in this channel	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT	6:0	Total retransmission count in this channel	0bXXXXXXX: Count of retransmissions for this channel

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TR0 (0xA0)

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		RSVD[1:0]	
Reset	0b1	0b1	0x3		0x0		0x0	
Access Type	Write, Read	Write, Read			Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN	7	When set, calculates and appends CRC to each packet transmitted from this port.	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled
RX_CRC_EN	6	When set, indicates that packets received at this port have appended CRC and CRC checking should be performed at each packet.	0b0: Receive CRC disabled 0b1: Receive CRC enabled
PRIO_VAL	3:2	Sets the priority for this channel's packet requests.	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority

TR1 (0xA1)

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT[1:0]		BW_VAL[5:0]					
Reset	0x2		0x30					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT	7:6	Channel bandwidth-allocation multiplication factor	0b00: Multiply BW_VAL by 1 0b01: Multiply BW_VAL by 4 0b10: Multiply BW_VAL by 16 0b11: Multiply BW_VAL by 16
BW_VAL	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL x BW_MULT/10 as a percentage of total link bandwidth	0bXXXXXX: Channel base-bandwidth value

TR3 (0xA3)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TX_SRC_ID[2:0]		
Reset	–	–	–	–	–	0x0		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID	2:0	Source identifier used in packets transmitted from this port. Default value is set by CFG0 pin.	0bXXX: Source ID for packets from this channel

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TR4 (0xA4)

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL	7:0	Receives packets from selected sources. Each bit indicates whether packets with that source ID should be received or not. For example, when RX_SRC_SEL = 00001001, then packets with source ID equal to 0 and 3 will be received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received ... ... 0xFF: Packets from all source IDs received

ARQ0 (0xA5)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	RSVD	RSVD	ARQ_EN	ARQ_EN	–	–
Reset	–	0b0	0b0	0b1	0b1	0b0	–	–
Access Type	–				Write, Read	Write, Read	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
ARQ_EN	3	Enables ARQ	0b0: ARQ disabled 0b1: ARQ enabled
ARQ_EN	2	Disables retransmission due to receiving same ACK twice	0b0: Enabled 0b1: Disabled

ARQ1 (0xA6)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
Reset	–	0x7			–	–	0b1	0b0
Access Type	–				–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR_OEN	1	Enables reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR—0xA7) for this channel at ERRB pin	0b0: ARQ maximum retransmit limit errors reporting at ERRB pin disabled 0b1: ARQ maximum retransmit limit errors reporting at ERRB pin enabled
RT_CNT_OEN	0	Enables reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT (0xA7) of this channel is greater than 0.	0b0: ARQ retransmission count reporting at ERRB pin disabled 0b1: ARQ retransmission count reporting at ERRB pin enabled

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ARQ2 (0xA7)

BIT	7	6	5	4	3	2	1	0
Field	MAX_RT_ERR	RT_CNT[6:0]						
Reset	0b0	0x0						
Access Type	Read Clears All	Read Clears All						

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR	7	Reached maximum retransmit limit (MAX_RT—0xA6) for one packet in this channel	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT	6:0	Total retransmission count in this channel	0bXXXXXXX: Count of retransmissions for this channel

TR0 (0xA8)

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN_B	RX_CRC_EN_B	RSVD[1:0]		PRIO_VAL_B[1:0]		RSVD[1:0]	
Reset	0b1	0b1	0x3		0x0		0x0	
Access Type	Write, Read	Write, Read			Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN_B	7	When set, calculates and appends CRC to each packet transmitted from this port.	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled
RX_CRC_EN_B	6	When set, indicates that packets received at this port have appended CRC, and CRC checking should be performed at each packet.	0b0: Receive CRC disabled 0b1: Receive CRC enabled
PRIO_VAL_B	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority

TR1 (0xA9)

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT_B[1:0]		BW_VAL_B[5:0]					
Reset	0x2		0x30					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT_B	7:6	Channel bandwidth-allocation multiplication factor.	0b00: Multiply BW_VAL_B by 1 0b01: Multiply BW_VAL_B by 4 0b10: Multiply BW_VAL_B by 16 0b11: Multiply BW_VAL_B by 16

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BITFIELD	BITS	DESCRIPTION	DECODE
BW_VAL_B	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL_B x BW_MULT_B/10 as a percentage of total link bandwidth	0bXXXXXX: Channel base-bandwidth value

TR3 (0xAB)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TX_SRC_ID_B[2:0]		
Reset	–	–	–	–	–	0x0		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID_B	2:0	Source identifier used in packets transmitted from this port. Default value is set by CFG0 pin.	0bXXX: Source ID for packets from this channel

TR4 (0xAC)

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL_B[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL_B	7:0	Receives packets from selected sources. Each bit indicates whether packets with that source ID should be received or not. For example, when RX_SRC_SEL_B = 00001001, then packets with source ID equal to 0 and 3 will be received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received ... ... 0xFF: Packets from all source IDs received

ARQ0 (0xAD)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	RSVD	RSVD	ARQ_EN_B	ARQ_EN	–	–
Reset	–	0b0	0b0	0b1	0b1	0b0	–	–
Access Type	–				Write, Read	Write, Read	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
ARQ_EN_B	3	Enables ARQ	0b0: ARQ disabled 0b1: ARQ enabled
ARQ_EN	2	Disables retransmission due to receiving same ACK twice	0b0: Enabled 0b1: Disabled

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ARQ1 (0xAE)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD[2:0]			–	–	MAX_RT_ERR_OEN_B	RT_CNT_OEN_B
Reset	–	0x7			–	–	0b1	0b0
Access Type	–				–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR_OEN_B	1	Enables reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR_B—0xAF) for this channel at ERRB pin	0b0: ARQ maximum retransmit limit errors reporting at ERRB pin disabled 0b1: ARQ maximum retransmit limit errors reporting at ERRB pin enabled
RT_CNT_OEN_B	0	Enables reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT_B (0xAF) of this channel is greater than 0.	0b0: ARQ retransmission count reporting at ERRB pin disabled 0b1: ARQ retransmission count reporting at ERRB pin enabled

ARQ2 (0xAF)

BIT	7	6	5	4	3	2	1	0
Field	MAX_RT_ERR_B	RT_CNT_B[6:0]						
Reset	0b0	0x0						
Access Type	Read Clears All	Read Clears All						

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR_B	7	Reached maximum retransmit limit (MAX_RT_B—0xAE) for one packet in this channel.	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT_B	6:0	Total retransmission count in this channel.	0bXXXXXXX: Count of retransmissions for this channel

TR0 (0xB0)

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN_C	RX_CRC_EN_C	RSVD[1:0]		PRIO_VAL_C[1:0]		RSVD[1:0]	
Reset	0b1	0b1	0x3		0x0		0x0	
Access Type	Write, Read	Write, Read			Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN_C	7	When set, calculates and appends CRC to each packet transmitted from this port.	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled
RX_CRC_EN_C	6	When set, indicates that packets received at this port have appended CRC, and CRC checking should be performed at each packet.	0b0: Receive CRC disabled 0b1: Receive CRC enabled

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BITFIELD	BITS	DESCRIPTION	DECODE
PRIO_VAL_C	3:2	Sets the priority for this channel's packet requests.	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority

TR1 (0xB1)

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT_C[1:0]		BW_VAL_C[5:0]					
Reset	0x2		0x30					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT_C	7:6	Channel bandwidth-allocation multiplication factor.	0b00: Multiply BW_VAL_C by 1 0b01: Multiply BW_VAL_C by 4 0b10: Multiply BW_VAL_C by 16 0b11: Multiply BW_VAL_C by 16
BW_VAL_C	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL_C x BW_MULT_C/10 as a percentage of total link bandwidth	0bXXXXXX: Channel base-bandwidth value

TR3 (0xB3)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TX_SRC_ID_C[2:0]		
Reset	–	–	–	–	–	0x0		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID_C	2:0	Source identifier used in packets transmitted from this port. Default value is set by CFG0 pin.	0bXXX: Source ID for packets from this channel

TR4 (0xB4)

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL_C[7:0]							
Reset	0xFF							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL_C	7:0	Receives packets from selected sources. Each bit indicates whether packets with that source ID should be received or not. For example, when RX_SRC_SEL_C = 00001001, then packets with source ID equal to 0 and 3 will be received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received ... ... 0xFF: Packets from all source IDs received

ARQ0 (0xB5)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	RSVD	RSVD	ARQ_EN_C	ARQ_EN	–	–
Reset	–	0b0	0b0	0b1	0b1	0b0	–	–
Access Type	–				Write, Read	Write, Read	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
ARQ_EN_C	3	Enables ARQ	0b0: ARQ disabled 0b1: ARQ enabled
ARQ_EN	2	Disables retransmission due to receiving same ACK twice	0b0: Enabled 0b1: Disabled

ARQ1 (0xB6)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD[2:0]			–	–	MAX_RT_ERR_OEN_C	RT_CNT_OEN_C
Reset	–	0x7			–	–	0b1	0b0
Access Type	–				–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR_OEN_C	1	Enables reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR_C—0xB7) for this channel at ERRB pin	0b0: ARQ maximum retransmit limit errors reporting at ERRB pin disabled 0b1: ARQ maximum retransmit limit errors reporting at ERRB pin enabled
RT_CNT_OEN_C	0	Enables reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT_C (0xB7) of this channel is greater than 0.	0b0: ARQ retransmission count reporting at ERRB pin disabled 0b1: ARQ retransmission count reporting at ERRB pin enabled

ARQ2 (0xB7)

BIT	7	6	5	4	3	2	1	0
Field	MAX_RT_ERR_C	RT_CNT_C[6:0]						
Reset	0b0	0x0						
Access Type	Read Clears All	Read Clears All						

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BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR_C	7	Reached maximum retransmit limit (MAX_RT_C—0xB6) for one packet in this channel.	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT_C	6:0	Total retransmission count in this channel.	0bXXXXXXX: Count of retransmissions for this channel

TR0 (0xB8)

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN_D	RX_CRC_EN_D	RSVD[1:0]		PRIO_VAL_D[1:0]		RSVD[1:0]	
Reset	0b1	0b1	0x3		0x0		0x0	
Access Type	Write, Read	Write, Read			Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN_D	7	When set, calculates and appends CRC to each packet transmitted from this port.	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled
RX_CRC_EN_D	6	When set, indicates that packets received at this port have appended CRC, and CRC checking should be performed at each packet.	0b0: Receive CRC disabled 0b1: Receive CRC enabled
PRIO_VAL_D	3:2	Sets the priority for this channel's packet requests.	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority

TR1 (0xB9)

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT_D[1:0]		BW_VAL_D[5:0]					
Reset	0x2		0x30					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT_D	7:6	Channel bandwidth-allocation multiplication factor.	0b00: Multiply BW_VAL_D by 1 0b01: Multiply BW_VAL_D by 4 0b10: Multiply BW_VAL_D by 16 0b11: Multiply BW_VAL_D by 16
BW_VAL_D	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL_D x BW_MULT_D/10 as a percentage of total link bandwidth	0bXXXXXX: Channel base-bandwidth value

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TR3 (0xBB)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TX_SRC_ID_D[2:0]		
Reset	–	–	–	–	–	0x0		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID_D	2:0	Source identifier used in packets transmitted from this port. Default value is set by CFG0 pin.	0bXXX: Source ID for packets from this channel

TR4 (0xBC)

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL_D[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL_D	7:0	Receives packets from selected sources. Each bit indicates whether packets with that source ID should be received or not. For example, when RX_SRC_SEL_D = 00001001, then packets with source ID equal to 0 and 3 will be received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received ... ... 0xFF: Packets from all source IDs received

ARQ0 (0xBD)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	RSVD	RSVD	ARQ_EN_D	ARQ_EN	–	–
Reset	–	0b0	0b0	0b1	0b1	0b0	–	–
Access Type	–				Write, Read	Write, Read	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
ARQ_EN_D	3	Enables ARQ	0b0: ARQ disabled 0b1: ARQ enabled
ARQ_EN	2	Disables retransmission due to receiving same ACK twice.	0b0: Enabled 0b1: Disabled

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ARQ1 (0xBE)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD[2:0]			–	–	MAX_RT_ERR_OEN_D	RT_CNT_OEN_D
Reset	–	0x7			–	–	0b1	0b0
Access Type	–				–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR_OEN_D	1	Enables reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR_D—0xBF) for this channel at ERRB pin	0b0: ARQ maximum retransmit limit errors reporting at ERRB pin disabled 0b1: ARQ maximum retransmit limit errors reporting at ERRB pin enabled
RT_CNT_OEN_D	0	Enables reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT_D (0xBF) of this channel is greater than 0.	0b0: ARQ retransmission count reporting at ERRB pin disabled 0b1: ARQ retransmission count reporting at ERRB pin enabled

ARQ2 (0xBF)

BIT	7	6	5	4	3	2	1	0
Field	MAX_RT_ERR_D	RT_CNT_D[6:0]						
Reset	0b0	0x0						
Access Type	Read Clears All	Read Clears All						

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR_D	7	Reached maximum retransmit limit (MAX_RT_D—0xBE) for one packet in this channel.	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT_D	6:0	Total retransmission count in this channel.	0bXXXXXXX: Count of retransmissions for this channel

I2C_7 (0xC7)

BIT	7	6	5	4	3	2	1	0
Field	I2C_REGSLV_1_TIMED_OUT	I2C_INTREG_SLV_1_TO[2:0]			I2C_REGSLV_0_TIMED_OUT	I2C_INTREG_SLV_0_TO[2:0]		
Reset	0x0	0x6			0x0	0x6		
Access Type	Read Only	Write, Read			Read Only	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
I2C_REGSLV_1_TIMED_OUT	7	Internal I^{2}C-to-register subordinate for Port 1 has timed out while waiting for the main or the internal register access FSM.	0b0: Internal I^{2}C-to-register subordinate for Port 1 has not timed out 0b1: Internal I^{2}C-to-register subordinate for Port 1 has timed out

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BITFIELD	BITS	DESCRIPTION	DECODE
I2C_INTREG_SLV_1_TO	6:4	I^{2}C-to-Internal Register Subordinate 1 Timeout Setting Internal register I^{2}C Subordinate 1 times out after the configured duration if it does not receive any response from the external main or internal register FSM. This subordinate serves I^{2}C Port 1.	0b000: 1ms 0b001: 2ms 0b010: 4ms 0b011: 8ms 0b100: 16ms 0b101: 32ms 0b110: 35ms 0b111: Disabled
I2C_REGSLV_0_TIMED_OUT	3	Internal I^{2}C-to-register subordinate for Port 0 has timed out while waiting for the main or the internal register access FSM.	0b0: Internal I^{2}C-to-register subordinate for Port 0 has not timed out 0b1: Internal I^{2}C-to-register subordinate for Port 0 has timed out
I2C_INTREG_SLV_0_TO	2:0	I^{2}C-to-Internal Register Subordinate 0 Timeout Setting Internal register I^{2}C Subordinate 0 times out after the configured duration if it does not receive any response from the external main or internal register FSM. This subordinate serves I^{2}C Port 0.	0b000: 1ms 0b001: 2ms 0b010: 4ms 0b011: 8ms 0b100: 16ms 0b101: 32ms 0b110: 35ms 0b111: Disabled

UART_0 (0xC8)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		REM_MS_EN_0	LOC_MS_EN_0	BYPASS_DIS_PAR_0	BYPASS_TO_0[1:0]		BYPASS_EN_0
Reset	0x1		0x0	0x0	0x0	0x1		0x0
Access Type			Write, Read	Write, Read	Write, Read	Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
REM_MS_EN_0	5	Enables UART Port 0 bypass mode control by remote GPIO pin. When set, remote chip's GPIO is used as MS pin (UART mode select). When MS is high, chip is in bypass mode, otherwise, chip is in base mode.	0b0: UART bypass mode not controlled by remote MS pin 0b1: UART bypass mode controlled by remote MS pin
LOC_MS_EN_0	4	Enables UART Port 0 bypass mode control by local GPIO pin. Set to use GPIO0 pin as MS pin (UART mode select). When MS is high, chip is in bypass mode, otherwise, chip is in base mode.	0b0: UART bypass mode not controlled by local MS pin 0b1: UART bypass mode controlled by local MS pin
BYPASS_DIS_PAR_0	3	Does not receive and send parity bit in bypass mode (for UART Port 0)	0b0: Receive and send parity bit in bypass mode 0b1: Do not receive and send parity bit in bypass mode
BYPASS_TO_0	2:1	UART Port 0 Soft-Bypass Timeout Duration	0b00: 2ms 0b01: 8ms 0b10: 32ms 0b11: Reserved

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BITFIELD	BITS	DESCRIPTION	DECODE
BYPASS_EN_0	0	Enables UART Port 0 soft-bypass mode. Bypass mode remains active as long as there is UART activity. When there is no UART activity for selected duration (configured by BYPASS_TO_0 bitfield), device exits bypass mode and the bit is automatically cleared.	0b0: UART soft-bypass mode disabled 0b1: UART soft-bypass mode enabled

UART_1 (0xC9)

BIT	7	6	5	4	3	2	1	0
Field	BITLEN_LSB_0[7:0]							
Reset	0x96							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
BITLEN_LSB_0	7:0	UART Port 0 detected bit length, low 8 bits	0xXX: UART Port 0 detected bit length, low 8 bits

UART_2 (0xCA)

BIT	7	6	5	4	3	2	1	0
Field	OUT_DELAY_0[1:0]		BITLEN_MSB_0[5:0]					
Reset	0x2		0x0					
Access Type	Write, Read		Read Only					

BITFIELD	BITS	DESCRIPTION	DECODE
OUT_DELAY_0	7:6	UART Port 0 Initial Output Delay In base mode, first received UART byte of a packet (SYNC or ACK frame) is delayed by the configured number of bit times in order to output the UART frames of the same packet back-to-back on the remote side.	0b00: 0 bits 0b01: 4 bits 0b10: 8 bits 0b11: 1 bit
BITLEN_MSB_0	5:0	UART Port 0 detected bit length, high 6 bits	0bXXXXXX: UART Port 0 detected bit length, high 6 bits

UART_3 (0xCB)

BIT	7	6	5	4	3	2	1	0
Field	ARB_TO_LEN_1[1:0]		REM_MS_EN_1	LOC_MS_EN_1	BYPASS_DIS_PAR_1	BYPASS_TO_1[1:0]		BYPASS_EN_1
Reset	0x1		0x0	0x0	0x0	0x1		0x0
Access Type	Write, Read		Write, Read	Write, Read	Write, Read	Write, Read		Write, Read

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BITFIELD	BITS	DESCRIPTION	DECODE
ARB_TO_LEN_1	7:6	UART Port 1 Rx Source Arbitration Timeout Duration UART Rx processes packets from a single UART source at any time. When UART Rx does not receive any UART packets for this duration, it will select the next UART source according to the source ID of the next following received packet.	0bXX: Arbitration timeout duration
REM_MS_EN_1	5	Enables UART Port 1 bypass mode control by remote GPIO pin. When set, remote chip's GPIO is used as MS pin (UART mode select). When MS is High, chip is in bypass mode, otherwise, chip is in base mode.	0b0: UART bypass mode not controlled by remote MS pin 0b1: UART bypass mode controlled by remote MS pin
LOC_MS_EN_1	4	Enables UART Port 1 bypass mode control by local GPIO pin. Set to use GPIO0 pin as MS pin (UART mode select). When MS is high, chip is in bypass mode, otherwise chip is in base mode.	0b0: UART bypass mode not controlled by local MS pin 0b1: UART bypass mode controlled by local MS pin
BYPASS_DIS_PAR_1	3	Does not receive and send parity bit in bypass mode (for UART Port 1)	0b0: Receive and send parity bit in bypass mode 0b1: Do not receive and send parity bit in bypass mode
BYPASS_TO_1	2:1	UART Port 1 Soft-Bypass Timeout Duration	0b00: 2ms 0b01: 8ms 0b10: 32ms 0b11: Reserved
BYPASS_EN_1	0	Enables UART Port 1 Soft-Bypass Mode Bypass mode remains active as long as there is UART activity. When there is no UART activity for selected duration (configured by BYPASS_TO_1 bitfield), device exits bypass mode and the bit is automatically cleared.	0b0: UART soft-bypass mode disabled 0b1: UART soft-bypass mode enabled

UART_4 (0xCC)

BIT	7	6	5	4	3	2	1	0
Field	BITLEN_LSB_1[7:0]							
Reset	0x96							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
BITLEN_LSB_1	7:0	UART Port 1 detected bit length, low 8 bits	0xXX: UART Port 1 detected bit length, low 8 bits

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UART_5 (0xCD)

BIT	7	6	5	4	3	2	1	0
Field	OUT_DELAY_1[1:0]		BITLEN_MSB_1[5:0]					
Reset	0x2		0x0					
Access Type	Write, Read		Read Only					

BITFIELD	BITS	DESCRIPTION	DECODE
OUT_DELAY_1	7:6	UART Port 1 Initial Output Delay In base mode, first received UART byte of a packet (SYNC or ACK frame) is delayed by the configured number of bit times in order to output the UART frames of the same packet back-to-back on the remote side.	0b00: 0 bits 0b01: 4 bits 0b10: 8 bits 0b11: 1 bit
BITLEN_MSB_1	5:0	UART Port 1 detected bit length, high 6 bits	0bXXXXXX: UART Port 1 detected bit length, high 6 bits

UART_6 (0xCE)

BIT	7	6	5	4	3	2	1	0
Field	UART_2_LINK_SELECT[1:0]		GMSL1_UART_ARB_TO	GMSL1_UART_ARB_EN	UART_1_LINK_SELECT[1:0]		UART_0_LINK_SELECT[1:0]	
Reset	0x0		0x0	0x0	0x1		0x0	
Access Type	Write, Read		Write, Read	Write, Read	Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
UART_2_LINK_SELECT	7:6	UART Port 2 Link Connection Select Note that the GMSL2 UART connections are point-to-point only (this is different from GMSL1 operation). In mixed link operation (i.e. some links enabled for GMSL1 and other links enabled for GMSL2), a UART port will be considered dedicated to GMSL2 if the UART Port 2 link connection decode above matches a link which is enabled for GMSL2 operation. Otherwise, the UART port will operate in GMSL1 mode. See REG6 (0x6) of the DEV register block.	0b00: Link A 0b01: Link B 0b10: Link C 0b11: Link D
GMSL1_UART_ARB_TO	5	GMSL1 UART Arbitration Timeout Value	0b0: 256µs 0b1: 4ms
GMSL1_UART_ARB_EN	4	UART Arbitration Enable on GMSL1 Forward Control Channel Links	0b0: UART arbitration not enabled on GMSL1 forward control channel links 0b1: UART arbitration enabled on GMSL1 forward control channel links

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BITFIELD	BITS	DESCRIPTION	DECODE
UART_1_LINK_SELECT	3:2	UART Port 1 Link Connection Select Note that the GMSL2 UART connections are point-to-point only (this is different from GMSL1 operation). In mixed link operation (i.e. some links enabled for GMSL1 and other links enabled for GMSL2), a UART port will be considered dedicated to GMSL2 if the UART Port 1 link connection decode above matches a link which is enabled for GMSL2 operation. Otherwise, the UART port will operate in GMSL1 mode. See REG6 (0x6) of the DEV register block.	0b00: Link A 0b01: Link B 0b10: Link C 0b11: Link D
UART_0_LINK_SELECT	1:0	UART Port 0 Link Connection Select Note that the GMSL2 UART connections are point-to-point only (this is different from GMSL1 operation). In mixed link operation (i.e. some links enabled for GMSL1 and other links enabled for GMSL2) a UART port will be considered dedicated to GMSL2 if the UART Port 0 link connection decode above matches a link which is enabled for GMSL2 operation. Otherwise, the UART port will operate in GMSL1 mode. See REG6 (0x6) of the DEV register block.	0b00: Link A 0b01: Link B 0b10: Link C 0b11: Link D

UART_7 (0xD0)

BIT	7	6	5	4	3	2	1	0
Field	–	–	UART_2_TX_OVERFLOW	UART_2_RX_OVERFLOW	UART_1_TX_OVERFLOW	UART_1_RX_OVERFLOW	UART_0_TX_OVERFLOW	UART_0_RX_OVERFLOW
Reset	–	–	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	–	–	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
UART_2_TX_OVERFLOW	5	UART Port 2 Tx Overflow	0b0: No overflow 0b1: Overflow
UART_2_RX_OVERFLOW	4	UART Port 2 Rx Overflow	0b0: No overflow 0b1: Overflow
UART_1_TX_OVERFLOW	3	UART Port 1 Tx Overflow	0b0: No overflow 0b1: Overflow
UART_1_RX_OVERFLOW	2	UART Port 1 Rx Overflow	0b0: No overflow 0b1: Overflow

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BITFIELD	BITS	DESCRIPTION	DECODE
UART_0_TX_OVERFLOW	1	UART Port 0 Tx Overflow	0b0: No overflow 0b1: Overflow
UART_0_RX_OVERFLOW	0	UART Port 0 Rx Overflow	0b0: No overflow 0b1: Overflow

UART_8 (0xD1)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		REM_MS_EN_2	LOC_MS_EN_2	BYPASS_DIS_PAR_2	BYPASS_TO_2[1:0]		BYPASS_EN_2
Reset	0x1		0x0	0x0	0x0	0x1		0x0
Access Type			Write, Read	Write, Read	Write, Read	Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
REM_MS_EN_2	5	Enable UART Port 2 bypass mode control by remote GPIO pin. When set, remote chip's GPIO is used as MS pin (UART mode select). When MS is high, chip is in bypass mode. Otherwise, chip is in base mode.	0b0: UART bypass mode not controlled by remote MS pin 0b1: UART bypass mode controlled by remote MS pin
LOC_MS_EN_2	4	Enable UART Port 2 bypass mode control by local GPIO pin. Set to use GPIO0 pin as MS pin (UART mode select). When MS is high, chip is in bypass mode. Otherwise, chip is in base mode.	0b0: UART bypass mode not controlled by local MS pin 0b1: UART bypass mode controlled by local MS pin
BYPASS_DIS_PAR_2	3	Does not receive and send parity bit in bypass mode (for UART Port 2)	0b0: Receive and send parity bit in bypass mode 0b1: Do not receive and send parity bit in bypass mode
BYPASS_TO_2	2:1	UART Port 2 Soft-Bypass Timeout Duration	0b00: 2ms 0b01: 8ms 0b10: 32ms 0b11: Reserved
BYPASS_EN_2	0	Enable UART Port 2 Soft-Bypass Mode Bypass mode remains active as long as there is UART activity. When there is no UART activity for selected duration (configured by BYPASS_TO_2 bitfield), device exits bypass mode and the bit is automatically cleared.	0b0: UART soft-bypass mode disabled 0b1: UART soft-bypass mode enabled

UART_9 (0xD2)

BIT	7	6	5	4	3	2	1	0
Field	BITLEN_LSB_2[7:0]							
Reset	0x96							
Access Type	Read Only							

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BITFIELD	BITS	DESCRIPTION	DECODE
BITLEN_LSB_2	7:0	UART Port 2 detected bit length, low 8 bits	0xXX: UART Port 2 detected bit length, low 8 bits

UART_10 (0xD3)

BIT	7	6	5	4	3	2	1	0
Field	OUT_DELAY_2[1:0]		BITLEN_MSB_2[5:0]					
Reset	0x2		0x0					
Access Type	Write, Read		Read Only					

BITFIELD	BITS	DESCRIPTION	DECODE
OUT_DELAY_2	7:6	UART Port 2 initial output delay In base mode, first received UART byte of a packet (SYNC or ACK frame) is delayed by the configured number of bit times in order to output the UART frames of the same packet back-to-back on the remote side.	0b00: 0 bits 0b01: 4 bits 0b10: 8 bits 0b11: 1 bit
BITLEN_MSB_2	5:0	UART Port 2 detected bit length, high 6 bits	0bXXXXXX: UART Port 2 detected bit length, high 6 bits

I2C_8 (0xD4)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	I2C_REGSLV_2_TIMED_OUT	I2C_INTREG_SLV_2_TO[2:0]		
Reset	–	–	–	–	0x0	0x6		
Access Type	–	–	–	–	Read Only	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
I2C_REGSLV_2_TIMED_OUT	3	Internal I^2C-to-register subordinate for Port 2 has timed out while waiting for the main or the internal register access FSM.	0b0: Internal I^2C-to-register subordinate for Port 2 has not timed out 0b1: Internal I^2C-to-register subordinate for Port 2 has timed out
I2C_INTREG_SLV_2_TO	2:0	I^2C-to-Internal Register Subordinate 2 Timeout Setting Internal register I^2C Subordinate 2 times out after the configured duration if it does not receive any response from the external main or internal register FSM. This subordinate serves I^2C Port 2.	0b000: 1ms 0b001: 2ms 0b010: 4ms 0b011: 8ms 0b100: 16ms 0b101: 32ms 0b110: 35ms 0b111: Disabled

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REG0 (0xE0)

BIT	7	6	5	4	3	2	1	0
Field	PU_LF7	PU_LF6	PU_LF5	PU_LF4	PU_LF3	PU_LF2	PU_LF1	PU_LF0
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
PU_LF7	7	Power-Up Line Fault Monitor 7	0b0: Line fault monitor 7 disabled 0b1: Line fault monitor 7 enabled
PU_LF6	6	Power-Up Line Fault Monitor 6	0b0: Line fault monitor 6 disabled 0b1: Line fault monitor 6 enabled
PU_LF5	5	Power-Up Line Fault Monitor 5	0b0: Line fault monitor 5 disabled 0b1: Line fault monitor 5 enabled
PU_LF4	4	Power-Up Line Fault Monitor 4	0b0: Line fault monitor 4 disabled 0b1: Line fault monitor 4 enabled
PU_LF3	3	Power-Up Line Fault Monitor 3	0b0: Line fault monitor 3 disabled 0b1: Line fault monitor 3 enabled
PU_LF2	2	Power-Up Line Fault Monitor 2	0b0: Line fault monitor 2 disabled 0b1: Line fault monitor 2 enabled
PU_LF1	1	Power-Up Line Fault Monitor 1	0b0: Line fault monitor 1 disabled 0b1: Line fault monitor 1 enabled
PU_LF0	0	Power-Up Line Fault Monitor 0	0b0: Line fault monitor 0 disabled 0b1: Line fault monitor 0 enabled

REG1 (0xE1)

BIT	7	6	5	4	3	2	1	0
Field	–	LF_1[2:0]			–	LF_0[2:0]		
Reset	–	0x2			–	0x2		
Access Type	–	Read Only			–	Read Only		

BITFIELD	BITS	DESCRIPTION	DECODE
LF_1	6:4	Line Fault Status of Wire Connected to LMN1 Pin	0b000: Short to battery 0b001: Short to GND 0b010: Normal Operation 0b011: Line Open 0b1XX: Line-to-line short
LF_0	2:0	Line Fault Status of Wire Connected to LMN0 Pin	0b000: Short to battery 0b001: Short to GND 0b010: Normal Operation 0b011: Line Open 0b1XX: Line-to-line short

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REG2 (0xE2)

BIT	7	6	5	4	3	2	1	0
Field	–	LF_3[2:0]			–	LF_2[2:0]		
Reset	–	0x2			–	0x2		
Access Type	–	Read Only			–	Read Only		

BITFIELD	BITS	DESCRIPTION	DECODE
LF_3	6:4	Line Fault Status of Wire Connected to LMN3 Pin	0b000: Short to battery 0b001: Short to GND 0b010: Normal Operation 0b011: Line Open 0b1XX: Line-to-line short
LF_2	2:0	Line Fault Status of Wire Connected to LMN2 Pin	0b000: Short to battery 0b001: Short to GND 0b010: Normal Operation 0b011: Line Open 0b1XX: Line-to-line short

REG3 (0xE3)

BIT	7	6	5	4	3	2	1	0
Field	–	LF_5[2:0]			–	LF_4[2:0]		
Reset	–	0x2			–	0x2		
Access Type	–	Read Only			–	Read Only		

BITFIELD	BITS	DESCRIPTION	DECODE
LF_5	6:4	Line Fault Status of Wire Connected to LMN5 Pin	0b000: Short to battery 0b001: Short to GND 0b010: Normal Operation 0b011: Line Open 0b1XX: Line-to-line short
LF_4	2:0	Line Fault Status of Wire Connected to LMN4 Pin	0b000: Short to battery 0b001: Short to GND 0b010: Normal Operation 0b011: Line Open 0b1XX: Line-to-line short

REG4 (0xE4)

BIT	7	6	5	4	3	2	1	0
Field	–	LF_7[2:0]			–	LF_6[2:0]		
Reset	–	0x2			–	0x2		
Access Type	–	Read Only			–	Read Only		

BITFIELD	BITS	DESCRIPTION	DECODE
LF_7	6:4	Line Fault Status of Wire Connected to LMN7 Pin	0b000: Short to battery 0b001: Short to GND 0b010: Normal Operation 0b011: Line Open 0b1XX: Line-to-line short

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BITFIELD	BITS	DESCRIPTION	DECODE
LF_6	2:0	Line Fault Status of Wire Connected to LMN6 Pin	0b000: Short to battery 0b001: Short to GND 0b010: Normal Operation 0b011: Line Open 0b1XX: Line-to-line short

REG5 (0xE5)

BIT	7	6	5	4	3	2	1	0
Field	LFLT_INT_FLAG[7:0]							
Reset								
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
LFLT_INT_FLAG	7:0	Latched Line Fault Monitor Error Flags Each bit corresponds to one of the line fault monitor status indicators as detailed in the decode. A line fault is flagged if a given line fault detector is enabled via the PU_LF* bits and the associated LF_* status indicator has a value other than 0b010. Routing of the LFLT_INT_FLAG flags to ERRB is controlled via the MASK_LF* bits. Read LFLT_INT_FLAG register to clear the latched error flag.	0bxxxxxxx0: No Error, Line Fault Monitor 0 0bxxxxxxx1: Error, Line Fault Monitor 0 0bxxxxxx0x: No Error, Line Fault Monitor 1 0bxxxxxx1x: Error, Line Fault Monitor 1 0bxxxxx0xx: No Error, Line Fault Monitor 2 0bxxxxx1xx: Error, Line Fault Monitor 2 0bxxxx0xxx: No Error, Line Fault Monitor 3 0bxxxx1xxx: Error, Line Fault Monitor 3 0bxxx0xxxx: No Error, Line Fault Monitor 4 0bxxx1xxxx: Error, Line Fault Monitor 4 0bxx0xxxxx: No Error, Line Fault Monitor 5 0bxx1xxxxx: Error, Line Fault Monitor 5 0bx0xxxxxx: No Error, Line Fault Monitor 6 0bx1xxxxxx: Error, Line Fault Monitor 6 0b0xxxxxxx: No Error, Line Fault Monitor 7 0b1xxxxxxx: Error, Line Fault Monitor 7

REG6 (0xE6)

BIT	7	6	5	4	3	2	1	0
Field	MASK_LF7	MASK_LF6	MASK_LF5	MASK_LF4	MASK_LF3	MASK_LF2	MASK_LF1	MASK_LF0
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MASK_LF7	7	Mask Line Fault Monitor 7 Interrupt	0b0: Line fault monitor 7 interrupt enabled 0b1: Line fault monitor 7 interrupt masked
MASK_LF6	6	Mask Line Fault Monitor 6 Interrupt	0b0: Line fault monitor 6 interrupt enabled 0b1: Line fault monitor 6 interrupt masked
MASK_LF5	5	Mask Line Fault Monitor 5 Interrupt	0b0: Line fault monitor 5 interrupt enabled 0b1: Line fault monitor 5 interrupt masked
MASK_LF4	4	Mask Line Fault Monitor 4 Interrupt	0b0: Line fault monitor 4 interrupt enabled 0b1: Line fault monitor 4 interrupt masked
MASK_LF3	3	Mask Line Fault Monitor 3 Interrupt	0b0: Line fault monitor 3 interrupt enabled 0b1: Line fault monitor 3 interrupt masked
MASK_LF2	2	Mask Line Fault Monitor 2 Interrupt	0b0: Line fault monitor 2 interrupt enabled 0b1: Line fault monitor 2 interrupt masked

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BITFIELD	BITS	DESCRIPTION	DECODE
MASK_LF1	1	Mask Line Fault Monitor 1 Interrupt	0b0: Line fault monitor 1 interrupt enabled 0b1: Line fault monitor 1 interrupt masked
MASK_LF0	0	Mask Line Fault Monitor 0 Interrupt	0b0: Line fault monitor 0 interrupt enabled 0b1: Line fault monitor 0 interrupt masked

VIDEO_PIPE_SEL_0 (0xF0)

BIT	7	6	5	4	3	2	1	0
Field	VIDEO_PIPE_SEL_1[3:0]				VIDEO_PIPE_SEL_0[3:0]			
Reset	0x6				0x2			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
VIDEO_PIPE_SEL_1	7:4	Video Pipe 1 Input Selection Control bits [7:6]: GMSL2 Phy Link selection for Pipe 1 bits [5:4]: Input Pipe selection for Pipe 1	Bits [7:6] 0b00: GMSL2 PHY A 0b01: GMSL2 PHY B 0b10: GMSL2 PHY C 0b11: GMSL2 PHY D Bits [5:4] 0b00: Pipe X 0b01: Pipe Y 0b10: Pipe Z 0b11: Pipe U
VIDEO_PIPE_SEL_0	3:0	Video Pipe 0 Input Selection Control bits [3:2]: GMSL2 Phy Link selection for Pipe 0 bits [1:0]: Input Pipe selection for Pipe 0	Bits [3:2] 0b00: GMSL2 PHY A 0b01: GMSL2 PHY B 0b10: GMSL2 PHY C 0b11: GMSL2 PHY D Bits [1:0] 0b00: Pipe X 0b01: Pipe Y 0b10: Pipe Z 0b11: Pipe U

VIDEO_PIPE_SEL_1 (0xF1)

BIT	7	6	5	4	3	2	1	0
Field	VIDEO_PIPE_SEL_3[3:0]				VIDEO_PIPE_SEL_2[3:0]			
Reset	0xe				0xa			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
VIDEO_PIPE_SEL_3	7:4	Video Pipe 3 Selection bits [7:6]: GMSL2 Phy Link selection for Pipe 3 bits [5:4]: Input Pipe selection for Pipe 3	Bits [7:6] 0b00: GMSL2 PHY A 0b01: GMSL2 PHY B 0b10: GMSL2 PHY C 0b11: GMSL2 PHY D Bits [5:4] 0b00: Pipe X 0b01: Pipe Y 0b10: Pipe Z 0b11: Pipe U

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BITFIELD	BITS	DESCRIPTION	DECODE
VIDEO_PIPE_SEL_2	3:0	Video Pipe 2 Selection bits [3:2]: GMSL2 Phy Link selection for Pipe 2 bits [1:0]: Input Pipe selection for Pipe 2	Bits [3:2] 0b00: GMSL2 PHY A 0b01: GMSL2 PHY B 0b10: GMSL2 PHY C 0b11: GMSL2 PHY D Bits [1:0] 0b00: Pipe X 0b01: Pipe Y 0b10: Pipe Z 0b11: Pipe U

VIDEO_PIPE_SEL_2 (0xF2)

BIT	7	6	5	4	3	2	1	0
Field	VIDEO_PIPE_SEL_5[3:0]				VIDEO_PIPE_SEL_4[3:0]			
Reset	0x4				0x0			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
VIDEO_PIPE_SEL_5	7:4	Video Pipe 5 Selection bits [7:6]: GMSL2 Phy Link selection for Pipe 5 bits [5:4]: Input Pipe selection for Pipe 5	Bits [7:6] 0b00: GMSL2 PHY A 0b01: GMSL2 PHY B 0b10: GMSL2 PHY C 0b11: GMSL2 PHY D Bits [5:4] 0b00: Pipe X 0b01: Pipe Y 0b10: Pipe Z 0b11: Pipe U
VIDEO_PIPE_SEL_4	3:0	Video Pipe 4 Selection bits [3:2]: GMSL2 Phy Link selection for Pipe 4 bits [1:0]: Input Pipe selection for Pipe 4	Bits [3:2] 0b00: GMSL2 PHY A 0b01: GMSL2 PHY B 0b10: GMSL2 PHY C 0b11: GMSL2 PHY D Bits [1:0] 0b00: Pipe X 0b01: Pipe Y 0b10: Pipe Z 0b11: Pipe U

VIDEO_PIPE_SEL_3 (0xF3)

BIT	7	6	5	4	3	2	1	0
Field	VIDEO_PIPE_SEL_7[3:0]				VIDEO_PIPE_SEL_6[3:0]			
Reset	0xc				0x8			
Access Type	Write, Read				Write, Read			

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BITFIELD	BITS	DESCRIPTION	DECODE
VIDEO_PIPE_SEL_7	7:4	Video Pipe 7 Selection bits [7:6]: GMSL2 Phy Link selection for Pipe 7 bits [5:4]: Input Pipe selection for Pipe 7	Bits [7:6] 0b00: GMSL2 PHY A 0b01: GMSL2 PHY B 0b10: GMSL2 PHY C 0b11: GMSL2 PHY D Bits [5:4] 0b00: Pipe X 0b01: Pipe Y 0b10: Pipe Z 0b11: Pipe U
VIDEO_PIPE_SEL_6	3:0	Video Pipe 6 Selection bits [3:2]: GMSL2 Phy Link selection for Pipe 6 bits [1:0]: Input Pipe selection for Pipe 6	Bits [3:2] 0b00: GMSL2 PHY A 0b01: GMSL2 PHY B 0b10: GMSL2 PHY C 0b11: GMSL2 PHY D Bits [1:0] 0b00: Pipe X 0b01: Pipe Y 0b10: Pipe Z 0b11: Pipe U

VIDEO_PIPE_EN (0xF4)

BIT	7	6	5	4	3	2	1	0
Field	VIDEO_PIPE_EN[7:0]							
Reset	0x0F							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VIDEO_PIPE_EN	7:0	Video Pipe Enable Register	0bXXXXXXX0: Disable Pipe 0 0bXXXXXXX1: Enable Pipe 0 0bXXXXXX0X: Disable Pipe 1 0bXXXXXX1X: Enable Pipe 1 0bXXXXX0XX: Disable Pipe 2 0bXXXXX1XX: Enable Pipe 2 0bXXXX0XXX: Disable Pipe 3 0bXXXX1XXX: Enable Pipe 3 0bXXX0XXXX: Disable Pipe 4 0bXXX1XXXX: Enable Pipe 4 0bXX0XXXXX: Disable Pipe 5 0bXX1XXXXX: Enable Pipe 5 0bX0XXXXXX: Disable Pipe 6 0bX1XXXXXX: Enable Pipe 6 0b0XXXXXXX: Disable Pipe 7 0b1XXXXXXX: Enable Pipe 7

HVD_GPIO_CTRL_0 (0xFA)

BIT	7	6	5	4	3	2	1	0
Field	–	DE_EN	HS_EN	VS_EN	–	HVD_SEL[2:0]		
Reset	–	0x0	0x0	0x0	–	0x0		
Access Type	–	Write, Read	Write, Read	Write, Read	–	Write, Read		

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BITFIELD	BITS	DESCRIPTION	DECODE
DE_EN	6	DE Enable Enables DE to be muxed out to GPIO.	0b0: Disable multiplexing of DE out to GPIO 0b1: Enable mulitplexing of DE out to GPIO
HS_EN	5	HS Enable Enables HS to be muxed out to GPIO.	0b0: Disable multiplexing of HS out to GPIO 0b1: Enable multiplexing of HS out to GPIO
VS_EN	4	Enable VS Enables VS to be muxed out to GPIO.	0b0: Disable multiplexing of VS out to GPIO 0b1: Enable multiplexing of VS out to GPIO
HVD_SEL	2:0	HVD Select Selects 1 of 8 pipes to view HS, VS, and/or DE	0b000: Select Pipe 0 0b001: Select Pipe 1 0b010: Select Pipe 2 0b011: Select Pipe 3 0b100: Select Pipe 4 0b101: Select Pipe 5 0b110: Select Pipe 6 0b111: Select Pipe 7

VIDEO_RX0 (0x100, 0x112, 0x124, 0x136, 0x148, 0x160, 0x172, 0x184)

BIT	7	6	5	4	3	2	1	0
Field	LCRC_ERR	RSVD	RSVD	SEQ_MISS_EN	RSVD	RSVD	LINE_CRC_EN	DIS_PKT_DET
Reset	0x0	0b0	0b1	0b1	0b0	0b0	0b1	0b0
Access Type	Read Clears All			Write, Read			Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LCRC_ERR	7	Video Line CRC Error Flag Asserted when a video line CRC error is detected	0b0: No video line CRC error detected 0b1: Video line CRC error detected
SEQ_MISS_EN	4	Video sequence miss detection enable	0b0: Disable Video Sequence Miss Detection 0b1: Video Sequence Miss Detection Enabled (Default)
LINE_CRC_EN	1	Video Line CRC Enable	0b0: Disable video line CRC 0b1: Enable video line CRC
DIS_PKT_DET	0	Disable Packet Detector If the video is restarted with a different BPP when the packet detector is disabled, toggle this register or the video receive enable register to make sure the video link restarts.	0b0: Enable packet detect (default) 0b1: Disable packet detect

VIDEO_RX3 (0x103, 0x115, 0x127, 0x139, 0x14B, 0x163, 0x175, 0x187)

BIT	7	6	5	4	3	2	1	0
Field	–	HD_TR_MODE	DLOCKED	VLOCKED	HLOCKED	DTRACKEN	VTRACKEN	HTRACKEN
Reset	–	0b1	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	Write, Read	Read Only	Read Only	Read Only	Write, Read	Write, Read	Write, Read

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BITFIELD	BITS	DESCRIPTION	DECODE
HD_TR_MODE	6	HD Tracking Mode HS and DE tracking enables full periodic pattern.	0b0: Allow only partial periodic HS, DE 0b1: Allow partial periodic and full periodic HS, DE
DLOCKED	5	DE Tracking Locked	0b0: DE tracking not locked 0b1: DE tracking locked
VLOCKED	4	VS Tracking Locked	0b0: VS tracking unlocked 0b1: VS tracking locked
HLOCKED	3	HS Tracking Locked	0b0: HS tracking unlocked 0b1: HS tracking locked
DTRACKEN	2	DE Tracking Enable (disable if FSYNC = 1) The system observes DE pulses and when it locks on the pattern, it can compensate for a limited number of missing pulses or suppress glitches.	0b0: DE tracking disabled (default) 0b1: DE tracking enabled
VTRACKEN	1	VSYNC tracking enable (disable if FSYNC = 1). The system observes VS pulses and when it locks on the pattern, it can compensate for a limited number of missing pulses or suppress glitches.	0b0: VSYNC tracking disabled (default) 0b1: VSYNC tracking enabled
HTRACKEN	0	HSYNC tracking enable (disable if FSYNC = 1). The system observes HS pulses and when it locks on the pattern, it can compensate for a limited number of missing pulses or suppress glitches.	0b0: HSYNC tracking disabled (default) 0b1: HSYNC tracking enabled

VIDEO_RX6 (0x106, 0x118, 0x12A, 0x13C, 0x14E, 0x166, 0x178, 0x18A)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[2:0]			–	LIM_HEART	–	RSVD	RSVD
Reset	0x0			–	0b0	–	0b1	0b0
Access Type				–	Write, Read	–		

BITFIELD	BITS	DESCRIPTION
LIM_HEART	3	If enabled, there is a 10ms timeout to detect loss of video lock. If disabled, there is a 100us timeout to detect loss of video lock. Set to 10ms timeout if Heartbeat is disabled (LIM_HEART = 1 on Serializer) Use together with SEQ_MISS_EN and DIS_PKT_DET registers in Deserializer. Embedded Data should use the heartbeat to ensure loss of video lock timeout does not occur.

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VIDEO_RX8 (0x108, 0x11A, 0x12C, 0x13E, 0x150, 0x168, 0x17A, 0x18C)

BIT	7	6	5	4	3	2	1	0
Field	VID_BLK_LEN_ERR	VID_LOCK	VID_PKT_DET	VID_SEQ_ERR	RSVD[3:0]			
Reset	0b0	0b0	0b0	0b0	0x2			
Access Type	Read Clears All	Read Only	Read Only	Read Clears All				

BITFIELD	BITS	DESCRIPTION	DECODE
VID_BLK_LEN_ERR	7	Video Rx block length error detected.	0b0: No video Rx block length error detected 0b1: Video Rx block length error detected
VID_LOCK	6	Video pipeline locked	0b0: Video pipeline not locked 0b1: Video pipeline locked
VID_PKT_DET	5	Video Rx sufficient packet throughput detection.	0b0: Insufficient packet throughput 0b1: Sufficient packet throughput
VID_SEQ_ERR	4	Video Rx sequence error detection.	0b0: No video Rx sequence error detected 0b1: Video Rx sequence error detected

VIDEO_RX10 (0x10A, 0x11C, 0x12E, 0x140, 0x152, 0x16A, 0x17C, 0x18E)

BIT	7	6	5	4	3	2	1	0
Field	–	MASK_VIDEO_DE	RSVD[5:0]					
Reset	–	0b0	0x00					
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
MASK_VIDEO_DE	6	Mask video when DE is low	0b0: Do not mask video with DE 0b1: Mask video with DE

CROSS_0 (0x1C0, 0x1E0, 0x200, 0x220, 0x240, 0x260, 0x280, 0x2A0)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS0_I	CROSS0_F	CROSS0[4:0]				
Reset	–	0x0	0x0	0x00				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS0_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS0_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS0	4:0	Maps incoming bit position set by this field to the outgoing bit position 0	0bXXXXX: Incoming bit position

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CROSS_1 (0x1C1, 0x1E1, 0x201, 0x221, 0x241, 0x261, 0x281, 0x2A1)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS1_I	CROSS1_F	CROSS1[4:0]				
Reset	–	0x0	0x0	0x01				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS1_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS1_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS1	4:0	Maps incoming bit position set by this field to the outgoing bit position 1	0bXXXXX: Incoming bit position

CROSS_2 (0x1C2, 0x1E2, 0x202, 0x222, 0x242, 0x262, 0x282, 0x2A2)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS2_I	CROSS2_F	CROSS2[4:0]				
Reset	–	0x0	0x0	0x02				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS2_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS2_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS2	4:0	Maps incoming bit position set by this field to the outgoing bit position 2	0bXXXXX: Incoming bit position

CROSS_3 (0x1C3, 0x1E3, 0x203, 0x223, 0x243, 0x263, 0x283, 0x2A3)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS3_I	CROSS3_F	CROSS3[4:0]				
Reset	–	0x0	0x0	0x03				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS3_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS3_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS3	4:0	Maps incoming bit position set by this field to the outgoing bit position 3	0bXXXXX: Incoming bit position

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CROSS_4 (0x1C4, 0x1E4, 0x204, 0x224, 0x244, 0x264, 0x284, 0x2A4)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS4_I	CROSS4_F	CROSS4[4:0]				
Reset	–	0x0	0x0	0x04				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS4_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS4_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS4	4:0	Maps incoming bit position set by this field to the outgoing bit position 4	0bXXXXX: Incoming bit position

CROSS_5 (0x1C5, 0x1E5, 0x205, 0x225, 0x245, 0x265, 0x285, 0x2A5)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS5_I	CROSS5_F	CROSS5[4:0]				
Reset	–	0x0	0x0	0x05				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS5_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS5_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS5	4:0	Maps incoming bit position set by this field to the outgoing bit position 5	0bXXXXX: Incoming bit position

CROSS_6 (0x1C6, 0x1E6, 0x206, 0x226, 0x246, 0x266, 0x286, 0x2A6)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS6_I	CROSS6_F	CROSS6[4:0]				
Reset	–	0x0	0x0	0x06				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS6_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS6_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS6	4:0	Maps incoming bit position set by this field to the outgoing bit position 6	0bXXXXX: Incoming bit position

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CROSS_7 (0x1C7, 0x1E7, 0x207, 0x227, 0x247, 0x267, 0x287, 0x2A7)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS7_I	CROSS7_F	CROSS7[4:0]				
Reset	–	0x0	0x0	0x07				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS7_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS7_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS7	4:0	Maps incoming bit position set by this field to the outgoing bit position 7	0bXXXXX: Incoming bit position

CROSS_8 (0x1C8, 0x1E8, 0x208, 0x228, 0x248, 0x268, 0x288, 0x2A8)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS8_I	CROSS8_F	CROSS8[4:0]				
Reset	–	0x0	0x0	0x08				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS8_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS8_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS8	4:0	Maps incoming bit position set by this field to the outgoing bit position 8	0bXXXXX: Incoming bit position

CROSS_9 (0x1C9, 0x1E9, 0x209, 0x229, 0x249, 0x269, 0x289, 0x2A9)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS9_I	CROSS9_F	CROSS9[4:0]				
Reset	–	0x0	0x0	0x09				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS9_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS9_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS9	4:0	Maps incoming bit position set by this field to the outgoing bit position 9	0bXXXXX: Incoming bit position

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CROSS_10 (0x1CA, 0x1EA, 0x20A, 0x22A, 0x24A, 0x26A, 0x28A, 0x2AA)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS10_I	CROSS10_F	CROSS10[4:0]				
Reset	–	0x0	0x0	0x0A				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS10_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS10_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS10	4:0	Maps incoming bit position set by this field to the outgoing bit position 10	0bXXXXX: Incoming bit position

CROSS_11 (0x1CB, 0x1EB, 0x20B, 0x22B, 0x24B, 0x26B, 0x28B, 0x2AB)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS11_I	CROSS11_F	CROSS11[4:0]				
Reset	–	0x0	0x0	0x0B				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS11_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS11_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS11	4:0	Maps incoming bit position set by this field to the outgoing bit position 11	0bXXXXX: Incoming bit position

CROSS_12 (0x1CC, 0x1EC, 0x20C, 0x22C, 0x24C, 0x26C, 0x28C, 0x2AC)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS12_I	CROSS12_F	CROSS12[4:0]				
Reset	–	0x0	0x0	0x0C				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS12_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS12_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS12	4:0	Maps incoming bit position set by this field to the outgoing bit position 12	0bXXXXX: Incoming bit position

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CROSS_13 (0x1CD, 0x1ED, 0x20D, 0x22D, 0x24D, 0x26D, 0x28D, 0x2AD)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS13_I	CROSS13_F	CROSS13[4:0]				
Reset	–	0x0	0x0	0x0D				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS13_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS13_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS13	4:0	Maps incoming bit position set by this field to the outgoing bit position 13	0bXXXXX: Incoming bit position

CROSS_14 (0x1CE, 0x1EE, 0x20E, 0x22E, 0x24E, 0x26E, 0x28E, 0x2AE)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS14_I	CROSS14_F	CROSS14[4:0]				
Reset	–	0x0	0x0	0x0E				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS14_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS14_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS14	4:0	Maps incoming bit position set by this field to the outgoing bit position 14	0bXXXXX: Incoming bit position

CROSS_15 (0x1CF, 0x1EF, 0x20F, 0x22F, 0x24F, 0x26F, 0x28F, 0x2AF)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS15_I	CROSS15_F	CROSS15[4:0]				
Reset	–	0x0	0x0	0x0F				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS15_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS15_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS15	4:0	Maps incoming bit position set by this field to the outgoing bit position 15	0bXXXXX: Incoming bit position

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CROSS_16 (0x1D0, 0x1F0, 0x210, 0x230, 0x250, 0x270, 0x290, 0x2B0)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS16_I	CROSS16_F	CROSS16[4:0]				
Reset	–	0x0	0x0	0x10				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS16_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS16_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS16	4:0	Maps incoming bit position set by this field to the outgoing bit position 16	0bXXXXX: Incoming bit position

CROSS_17 (0x1D1, 0x1F1, 0x211, 0x231, 0x251, 0x271, 0x291, 0x2B1)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS17_I	CROSS17_F	CROSS17[4:0]				
Reset	–	0x0	0x0	0x11				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS17_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS17_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS17	4:0	Maps incoming bit position set by this field to the outgoing bit position 17	0bXXXXX: Incoming bit position

CROSS_18 (0x1D2, 0x1F2, 0x212, 0x232, 0x252, 0x272, 0x292, 0x2B2)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS18_I	CROSS18_F	CROSS18[4:0]				
Reset	–	0x0	0x0	0x12				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS18_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS18_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS18	4:0	Maps incoming bit position set by this field to the outgoing bit position 18	0bXXXXX: Incoming bit position

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CROSS_19 (0x1D3, 0x1F3, 0x213, 0x233, 0x253, 0x273, 0x293, 0x2B3)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS19_I	CROSS19_F	CROSS19[4:0]				
Reset	–	0x0	0x0	0x13				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS19_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS19_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS19	4:0	Maps incoming bit position set by this field to the outgoing bit position 19	0bXXXXX: Incoming bit position

CROSS_20 (0x1D4, 0x1F4, 0x214, 0x234, 0x254, 0x274, 0x294, 0x2B4)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS20_I	CROSS20_F	CROSS20[4:0]				
Reset	–	0x0	0x0	0x14				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS20_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS20_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS20	4:0	Maps incoming bit position set by this field to the outgoing bit position 20	0bXXXXX: Incoming bit position

CROSS_21 (0x1D5, 0x1F5, 0x215, 0x235, 0x255, 0x275, 0x295, 0x2B5)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS21_I	CROSS21_F	CROSS21[4:0]				
Reset	–	0x0	0x0	0x15				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS21_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS21_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS21	4:0	Maps incoming bit position set by this field to the outgoing bit position 21	0bXXXXX: Incoming bit position

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CROSS_22 (0x1D6, 0x1F6, 0x216, 0x236, 0x256, 0x276, 0x296, 0x2B6)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS22_I	CROSS22_F	CROSS22[4:0]				
Reset	–	0x0	0x0	0x16				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS22_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS22_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS22	4:0	Maps incoming bit position set by this field to the outgoing bit position 22	0bXXXXX: Incoming bit position

CROSS_23 (0x1D7, 0x1F7, 0x217, 0x237, 0x257, 0x277, 0x297, 0x2B7)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS23_I	CROSS23_F	CROSS23[4:0]				
Reset	–	0x0	0x0	0x17				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS23_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS23_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS23	4:0	Maps incoming bit position set by this field to the outgoing bit position 23	0bXXXXX: Incoming bit position

CROSS_HS (0x1D8, 0x1F8, 0x218, 0x238, 0x258, 0x278, 0x298, 0x2B8)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS_HS_I	CROSS_HS_F	CROSS_HS[4:0]				
Reset	–	0x0	0x0	0x18				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS_HS_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS_HS_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS_HS	4:0	Maps selected internal signal to Cross X	0bXXXXX: Incoming bit position

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CROSS_VS (0x1D9, 0x1F9, 0x219, 0x239, 0x259, 0x279, 0x299, 0x2B9)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS_VS_I	CROSS_VS_F	CROSS_VS[4:0]				
Reset	–	0x0	0x0	0x19				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS_VS_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS_VS_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS_VS	4:0	Maps selected internal signal to Cross X	0bXXXXX: Incoming bit position

CROSS_DE (0x1DA, 0x1FA, 0x21A, 0x23A, 0x25A, 0x27A, 0x29A, 0x2BA)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS_DE_I	CROSS_DE_F	CROSS_DE[4:0]				
Reset	–	0x0	0x0	0x1A				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS_DE_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS_DE_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS_DE	4:0	Maps selected internal signal to Cross X	0bXXXXX: Incoming bit position

PRBS_ERR (0x1DB, 0x1FB, 0x21B, 0x23B, 0x25B, 0x27B, 0x29B, 0x2BB)

BIT	7	6	5	4	3	2	1	0
Field	VPRBS_ERR[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
VPRBS_ERR	7:0	Video PRBS error counter, clears on read	0xXX: Number of video PRBS errors since last read

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VPRBS (0x1DC, 0x1FC, 0x21C, 0x23C, 0x25C, 0x27C, 0x29C, 0x2BC)

BIT	7	6	5	4	3	2	1	0
Field	PATGEN_CLK_SRC	–	RSVD	VPRBS24_GENCHK_EN	VPRBS7_GENCHK_EN	VPRBS9_GENCHK_EN	DIS_GLITCH_FILT	VIDEO_LOCK
Reset	0x1	–	0b0	0b0	0b0	0b0	0x0	0b0
Access Type	Write, Read	–		Write, Read	Write, Read	Write, Read	Write, Read	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
PATGEN_CLK_SRC	7	Pattern generator clock source for video PRBS7, PRBS9, PRBS24, checkerboard, and gradient patterns. 0 = 150MHz, 1 = 375MHz (default).	0b0: 150MHz 0b1: 375MHz (default)
VPRBS24_GENCHK_EN	4	Enables video PRBS24 generator/checker	0b0: Video PRBS24 generator/checker disabled 0b1: Video PRBS24 generator/checker enabled
VPRBS7_GENCHK_EN	3	Enables video PRBS7 generator/checker	0b0: Video PRBS7 generator/checker disabled 0b1: Video PRBS7 generator/checker enabled
VPRBS9_GENCHK_EN	2	Enables video PRBS9 generator/checker	0b0: Video PRBS9 generator/checker disabled 0b1: Video PRBS9 generator/checker enabled
DIS_GLITCH_FILT	1	Disables HS, VS, and DE glitch filtering	0b0: Glitch filter enabled 0b1: Glitch filter disabled
VIDEO_LOCK	0	Video channel is locked and outputting valid video data	0b0: Video channel is not locked 0b1: Video channel is locked

CROSS_27 (0x1DD, 0x1FD, 0x21D, 0x23D, 0x25D, 0x27D, 0x29D, 0x2BD)

BIT	7	6	5	4	3	2	1	0
Field	ALT_CROSSBAR	CROSS27_I	CROSS27_F	CROSS27[4:0]				
Reset	0x0	0x0	0x0	0x1B				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
ALT_CROSSBAR	7	Selects whether to use the crossbar in the VRX block or the alternative crossbar in the RDP.	0b0: Use crossbar in VRX block 0b1: Use crossbar in RDP
CROSS27_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS27_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS27	4:0	Maps selected internal signal to Cross X	0bXXXXX: Incoming bit position

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CROSS_28 (0x1DE, 0x1FE, 0x21E, 0x23E, 0x25E, 0x27E, 0x29E, 0x2BE)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS28_I	CROSS28_F	CROSS28[4:0]				
Reset	–	0x0	0x0	0x1C				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS28_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS28_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS28	4:0	Maps selected internal signal to Cross X	0bXXXXX: Incoming bit position

CROSS_29 (0x1DF, 0x1FF, 0x21F, 0x23F, 0x25F, 0x27F, 0x29F, 0x2BF)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS29_I	CROSS29_F	CROSS29[4:0]				
Reset	–	0x0	0x0	0x1D				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS29_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS29_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS29	4:0	Maps selected internal signal to Cross X	0bXXXXX: Incoming bit position

GPIO_A (0x300)

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0x0	0x0	0b0	0b0	0b0	0b1	0b1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	GPIO_REV_CDLY_AJitter minimization compensation enable Note: In delay compensation mode, a fixed delay is guaranteed once the link is locked. But each link reset could change the delay between two values which are 1.7us apart. Note: Use GPIO_REV_CDLY to adjust comp time.	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled

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BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Enable/disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x301)

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x2		0b1	0x00				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x302)

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	RSVD	GPIO_RX_ID[4:0]				
Reset	0x0	0b1	0b0	0x00				
Access Type	Write, Read			Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG (0x300) and PULL_UPDN_SEL (0x301) are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

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GPIO_A (0x303)

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0x0	0x0	0b0	0b0	0b1	0b0	0b0
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Enable/disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x304)

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x2		0b1	0x01				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

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GPIO_C (0x305)

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	RSVD	GPIO_RX_ID[4:0]				
Reset	0x0	0b1	0b0	0x01				
Access Type	Write, Read			Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG (0x303) and PULL_UPDN_SEL (0x304) are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x306)

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0x0	0x0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Enable/disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

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GPIO_B (0x307)

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x2		0b1	0x02				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x308)

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	RSVD	GPIO_RX_ID[4:0]				
Reset	0x0	0b1	0b0	0x02				
Access Type	Write, Read			Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG (0x306) and PULL_UPDN_SEL (0x307) are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x309)

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0x0	0x0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1

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BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Enable/disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x30A)

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x0		0b1	0x03				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x30B)

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	RSVD	GPIO_RX_ID[4:0]				
Reset	0x0	0b1	0b0	0x03				
Access Type	Write, Read			Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG (0x309) and PULL_UPDN_SEL (0x30A) are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

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GPIO_A (0x30C)

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0x0	0x0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Enable/disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x30D)

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x2		0b1	0x04				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

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GPIO_C (0x30E)

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	RSVD	GPIO_RX_ID[4:0]				
Reset	0x0	0b1	0b0	0x04				
Access Type	Write, Read			Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG (0x30C) and PULL_UPDN_SEL (0x30D) are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x310)

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0x0	0x0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Enable/disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

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GPIO_B (0x311)

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x2		0b1	0x05				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x312)

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	RSVD	GPIO_RX_ID[4:0]				
Reset	0x0	0b1	0b0	0x05				
Access Type	Write, Read			Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG (0x310) and PULL_UPDN_SEL (0x311) are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x313)

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0x0	0x0	0b0	0b0	0b0	0b1	0b1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1

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BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Enable/disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x314)

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x2		0b1	0x06				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x315)

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	RSVD	GPIO_RX_ID[4:0]				
Reset	0x0	0b1	0b0	0x06				
Access Type	Write, Read			Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG (0x313) and PULL_UPDN_SEL (0x314) are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

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GPIO_A (0x316)

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0x0	0x0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Enable/disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x317)

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x2		0b1	0x07				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

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GPIO_C (0x318)

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	RSVD	GPIO_RX_ID[4:0]				
Reset	0x0	0b1	0b0	0x07				
Access Type	Write, Read			Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG (0x316) and PULL_UPDN_SEL (0x317) are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x319)

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0x0	0x0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Enable/disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

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GPIO_B (0x31A)

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x2		0b1	0x08				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x31B)

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	RSVD	GPIO_RX_ID[4:0]				
Reset	0x0	0b1	0b0	0x08				
Access Type	Write, Read			Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG (0x319) and PULL_UPDN_SEL (0x31A) are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x31C)

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0x0	0x0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1

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BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Enable/disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x31D)

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x2		0b1	0x09				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x31E)

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	RSVD	GPIO_RX_ID[4:0]				
Reset	0x0	0b1	0b0	0x09				
Access Type	Write, Read			Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG (0x31C) and PULL_UPDN_SEL (0x31D) are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

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GPIO_A (0x320)

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0x0	0x0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Enable/disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x321)

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x2		0b1	0x0A				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

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GPIO_C (0x322)

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	RSVD	GPIO_RX_ID[4:0]				
Reset	0x0	0b1	0b0	0x0A				
Access Type	Write, Read			Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG (0x320) and PULL_UPDN_SEL (0x321) are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x323)

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0x0	0x0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Enable/disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

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GPIO_B (0x324)

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x0		0b1	0x0B				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x325)

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	RSVD	GPIO_RX_ID[4:0]				
Reset	0x0	0b1	0b0	0x0B				
Access Type	Write, Read			Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG (0x323) and PULL_UPDN_SEL (0x324) are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x326)

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0x0	0x0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1

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BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Enable/disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x327)

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x0		0b1	0x0C				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x328)

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	RSVD	GPIO_RX_ID[4:0]				
Reset	0x0	0b1	0b0	0x0C				
Access Type	Write, Read			Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG (0x326) and PULL_UPDN_SEL (0x327) are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

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GPIO_A (0x329)

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0x0	0x0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Enable/disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x32A)

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x0		0b1	0x0D				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

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GPIO_C (0x32B)

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	RSVD	GPIO_RX_ID[4:0]				
Reset	0x0	0b1	0b0	0x0D				
Access Type	Write, Read			Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG (0x329) and PULL_UPDN_SEL (0x32A) are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x32C)

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0x0	0x0	0b1	0b1	0b0	0b0	0b1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Enable/disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

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GPIO_B (0x32D)

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x2		0b1	0x0E				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x32E)

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	RSVD	GPIO_RX_ID[4:0]				
Reset	0x0	0b1	0b0	0x0E				
Access Type	Write, Read			Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG (0x32C) and PULL_UPDN_SEL (0x32D) are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x330)

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b0	0x0	0x0	0b1	0b1	0b0	0b0	0b1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1

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BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Enable/disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x331)

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		RSVD	GPIO_TX_ID[4:0]				
Reset	0x0		0b0	0x0F				
Access Type	Write, Read			Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x332)

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	RSVD	GPIO_RX_ID[4:0]				
Reset	0x0	0b1	0b0	0x0F				
Access Type	Write, Read			Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG (0x330) and PULL_UPDN_SEL (0x331) are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

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GPIO_A (0x333)

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b0	0x0	0x0	0b1	0b1	0b0	0b0	0b1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Enable/disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x334)

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		RSVD	GPIO_TX_ID[4:0]				
Reset	0x0		0b0	0x10				
Access Type	Write, Read			Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x335)

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	RSVD	GPIO_RX_ID[4:0]				
Reset	0x0	0b1	0b0	0x10				
Access Type	Write, Read			Write, Read				

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BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES-CFG (0x333) and PULL_UPDN_SEL (0x334) are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x337)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
Reset	0x0	0x0	0b0	0x00				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_B	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_B	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_B	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x338)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
Reset	–	0b1	0b0	0x00				
Access Type	–		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_B	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_B	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

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GPIO_B (0x33A)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
Reset	0x0	0x0	0b0	0x01				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_B	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_B	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_B	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x33B)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
Reset	–	0b1	0b0	0x01				
Access Type	–		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_B	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_B	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x33D)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
Reset	0x0	0x0	0b0	0x02				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_B	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_B	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission

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BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_TX_ID_B	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x33E)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
Reset	–	0b1	0b0	0x02				
Access Type	–		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_B	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_B	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x341)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
Reset	0x0	0x0	0b0	0x03				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_B	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_B	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_B	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x342)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
Reset	–	0b1	0b0	0x03				
Access Type	–		Write, Read	Write, Read				

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BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_B	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_B	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x344)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
Reset	0x0	0x0	0b0	0x04				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_B	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_B	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_B	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x345)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
Reset	–	0b1	0b0	0x04				
Access Type	–		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_B	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_B	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x347)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
Reset	0x0	0x0	0b0	0x05				
Access Type		Write, Read	Write, Read	Write, Read				

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BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_B	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_B	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_B	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x348)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
Reset	–	0b1	0b0	0x05				
Access Type	–		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_B	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_B	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x34A)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
Reset	0x0	0x0	0b0	0x06				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_B	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_B	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_B	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

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GPIO_C (0x34B)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
Reset	–	0b1	0b0	0x06				
Access Type	–		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_B	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_B	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x34D)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
Reset	0x0	0x0	0b0	0x07				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_B	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_B	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_B	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x34E)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
Reset	–	0b1	0b0	0x07				
Access Type	–		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_B	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_B	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

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GPIO_B (0x351)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
Reset	0x0	0x0	0b0	0x08				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_B	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_B	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_B	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x352)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
Reset	–	0b1	0b0	0x08				
Access Type	–		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_B	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_B	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x354)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
Reset	0x0	0x0	0b0	0x09				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_B	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_B	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission

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BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_TX_ID_B	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x355)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
Reset	–	0b1	0b0	0x09				
Access Type	–		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_B	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_B	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x357)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
Reset	0x0	0x0	0b0	0x0a				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_B	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_B	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_B	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x358)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
Reset	–	0b1	0b0	0x0a				
Access Type	–		Write, Read	Write, Read				

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BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_B	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_B	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x35A)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
Reset	0x0	0x0	0b0	0x0b				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_B	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_B	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_B	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x35B)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
Reset	–	0b1	0b0	0x0b				
Access Type	–		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_B	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_B	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x35D)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
Reset	0x0	0x0	0b0	0x0c				
Access Type		Write, Read	Write, Read	Write, Read				

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BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_B	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_B	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_B	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x35E)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
Reset	–	0b1	0b0	0x0c				
Access Type	–		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_B	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_B	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x361)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
Reset	0x0	0x0	0b0	0x0d				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_B	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_B	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_B	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

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GPIO_C (0x362)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
Reset	–	0b1	0b0	0x0d				
Access Type	–		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_B	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_B	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x364)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
Reset	0x0	0x0	0b0	0x0e				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_B	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_B	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_B	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x365)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
Reset	–	0b1	0b0	0x0e				
Access Type	–		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_B	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_B	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

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GPIO_B (0x367)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
Reset	0x0	0x0	0b0	0x0F				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_B	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_B	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_B	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x368)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
Reset	–	0b1	0b0	0x0F				
Access Type	–		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_B	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_B	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x36A)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
Reset	0x0	0x0	0b0	0x10				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_B	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_B	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission

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BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_TX_ID_B	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x36B)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
Reset	–	0b1	0b0	0x10				
Access Type	–		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_B	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_B	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x36D)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
Reset	0x0	0x0	0b0	0x00				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_C	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_C	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_C	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x36E)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
Reset	–	0b1	0b0	0x00				
Access Type	–		Write, Read	Write, Read				

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BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_C	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_C	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x371)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
Reset	0x0	0x0	0b0	0x01				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_C	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_C	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_C	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x372)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
Reset	–	0b1	0b0	0x01				
Access Type	–		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_C	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_C	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x374)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
Reset	0x0	0x0	0b0	0x02				
Access Type		Write, Read	Write, Read	Write, Read				

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BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_C	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_C	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_C	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x375)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
Reset	–	0b1	0b0	0x02				
Access Type	–		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_C	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_C	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x377)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
Reset	0x0	0x0	0b0	0x03				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_C	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_C	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_C	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

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GPIO_C (0x378)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
Reset	–	0b1	0b0	0x03				
Access Type	–		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_C	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_C	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x37A)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
Reset	0x0	0x0	0b0	0x04				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_C	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_C	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_C	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x37B)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
Reset	–	0b1	0b0	0x04				
Access Type	–		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_C	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_C	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

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GPIO_B (0x37D)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
Reset	0x0	0x0	0b0	0x05				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_C	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_C	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_C	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x37E)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
Reset	–	0b1	0b0	0x05				
Access Type	–		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_C	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_C	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x381)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
Reset	0x0	0x0	0b0	0x06				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_C	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_C	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission

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BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_TX_ID_C	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x382)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
Reset	–	0b1	0b0	0x06				
Access Type	–		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_C	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_C	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x384)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
Reset	0x0	0x0	0b0	0x07				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_C	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_C	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_C	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x385)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
Reset	–	0b1	0b0	0x07				
Access Type	–		Write, Read	Write, Read				

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BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_C	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_C	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x387)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
Reset	0x0	0x0	0b0	0x08				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_C	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_C	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_C	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x388)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
Reset	–	0b1	0b0	0x08				
Access Type	–		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_C	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_C	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x38A)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
Reset	0x0	0x0	0b0	0x09				
Access Type		Write, Read	Write, Read	Write, Read				

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BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_C	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_C	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_C	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x38B)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
Reset	–	0b1	0b0	0x09				
Access Type	–		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_C	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_C	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x38D)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
Reset	0x0	0x0	0b0	0x0a				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_C	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_C	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_C	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

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GPIO_C (0x38E)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
Reset	–	0b1	0b0	0x0a				
Access Type	–		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_C	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_C	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x391)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
Reset	0x0	0x0	0b0	0x0b				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_C	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_C	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_C	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x392)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
Reset	–	0b1	0b0	0x0b				
Access Type	–		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_C	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_C	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

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GPIO_B (0x394)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
Reset	0x0	0x0	0b0	0x0c				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_C	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_C	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_C	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x395)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
Reset	–	0b1	0b0	0x0c				
Access Type	–		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_C	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_C	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x397)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
Reset	0x0	0x0	0b0	0x0d				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_C	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_C	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission

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BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_TX_ID_C	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x398)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
Reset	–	0b1	0b0	0x0d				
Access Type	–		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_C	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_C	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x39A)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
Reset	0x0	0x0	0b0	0x0e				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_C	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_C	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_C	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x39B)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
Reset	–	0b1	0b0	0x0e				
Access Type	–		Write, Read	Write, Read				

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BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_C	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_C	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x39D)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
Reset	0x0	0x0	0b0	0x0f				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_C	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_C	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_C	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x39E)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
Reset	–	0b1	0b0	0x0f				
Access Type	–		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_C	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_C	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x3A1)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
Reset	0x0	0x0	0b0	0x10				
Access Type		Write, Read	Write, Read	Write, Read				

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BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_C	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_C	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_C	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x3A2)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
Reset	–	0b1	0b0	0x10				
Access Type	–		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_C	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_C	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x3A4)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
Reset	0x0	0x0	0b0	0x00				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_D	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_D	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_D	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

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GPIO_C (0x3A5)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
Reset	–	0b1	0b0	0x00				
Access Type	–		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_D	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_D	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x3A7)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
Reset	0x0	0x0	0b0	0x01				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_D	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_D	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_D	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x3A8)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
Reset	–	0b1	0b0	0x01				
Access Type	–		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_D	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_D	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

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GPIO_B (0x3AA)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
Reset	0x0	0x0	0b0	0x02				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_D	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_D	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_D	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x3AB)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
Reset	–	0b1	0b0	0x02				
Access Type	–		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_D	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_D	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x3AD)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
Reset	0x0	0x0	0b0	0x03				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_D	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_D	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission

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BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_TX_ID_D	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x3AE)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
Reset	–	0b1	0b0	0x03				
Access Type	–		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_D	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_D	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x3B1)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
Reset	0x0	0x0	0b0	0x04				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_D	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_D	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_D	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x3B2)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
Reset	–	0b1	0b0	0x04				
Access Type	–		Write, Read	Write, Read				

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BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_D	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_D	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x3B4)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
Reset	0x0	0x0	0b0	0x05				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_D	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_D	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_D	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x3B5)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
Reset	–	0b1	0b0	0x05				
Access Type	–		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_D	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_D	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x3B7)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
Reset	0x0	0x0	0b0	0x06				
Access Type		Write, Read	Write, Read	Write, Read				

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BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_D	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_D	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_D	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x3B8)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
Reset	–	0b1	0b0	0x06				
Access Type	–		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_D	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_D	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x3BA)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
Reset	0x0	0x0	0b0	0x07				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_D	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_D	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_D	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

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GPIO_C (0x3BB)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
Reset	–	0b1	0b0	0x07				
Access Type	–		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_D	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_D	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x3BD)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
Reset	0x0	0x0	0b0	0x08				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_D	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_D	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_D	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x3BE)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
Reset	–	0b1	0b0	0x08				
Access Type	–		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_D	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_D	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

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GPIO_B (0x3C1)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
Reset	0x0	0x0	0b0	0x09				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_D	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_D	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_D	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x3C2)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
Reset	–	0b1	0b0	0x09				
Access Type	–		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_D	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_D	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x3C4)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
Reset	0x0	0x0	0b0	0x0a				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_D	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_D	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission

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BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_TX_ID_D	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x3C5)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
Reset	–	0b1	0b0	0x0a				
Access Type	–		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_D	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_D	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x3C7)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
Reset	0x0	0x0	0b0	0x0b				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_D	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_D	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_D	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x3C8)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
Reset	–	0b1	0b0	0x0b				
Access Type	–		Write, Read	Write, Read				

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BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_D	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_D	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x3CA)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
Reset	0x0	0x0	0b0	0x0c				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_D	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_D	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_D	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x3CB)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
Reset	–	0b1	0b0	0x0c				
Access Type	–		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_D	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_D	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x3CD)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
Reset	0x0	0x0	0b0	0x0d				
Access Type		Write, Read	Write, Read	Write, Read				

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BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_D	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_D	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_D	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x3CE)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
Reset	–	0b1	0b0	0x0d				
Access Type	–		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_D	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_D	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x3D1)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
Reset	0x0	0x0	0b0	0x0e				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_D	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_D	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_D	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

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GPIO_C (0x3D2)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
Reset	–	0b1	0b0	0x0e				
Access Type	–		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_D	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_D	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x3D4)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
Reset	0x0	0x0	0b0	0x0f				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_D	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_D	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_D	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x3D5)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
Reset	–	0b1	0b0	0x0f				
Access Type	–		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_D	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_D	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

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GPIO_B (0x3D7)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
Reset	0x0	0x0	0b0	0x10				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_D	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_D	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_D	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x3D8)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
Reset	–	0b1	0b0	0x10				
Access Type	–		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_D	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_D	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

MS_ID_A (0x3F0)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	RX_MS_ID_A[4:0]				
Reset	–	–	–	0x1D				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
RX_MS_ID_A	4:0	GPIO ID for remote MS pin for Link A	0bXXXXX: This GPIO transmit ID

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MS_ID_B (0x3F1)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	RX_MS_ID_B[4:0]				
Reset	–	–	–	0x1D				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
RX_MS_ID_B	4:0	GPIO ID for remote MS pin for Link B	0bXXXXX: This GPIO transmit ID

MS_ID_C (0x3F2)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	RX_MS_ID_C[4:0]				
Reset	–	–	–	0x1D				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
RX_MS_ID_C	4:0	GPIO ID for remote MS pin for Link C	0bXXXXX: This GPIO transmit ID

MS_ID_D (0x3F3)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	RX_MS_ID_D[4:0]				
Reset	–	–	–	0x1D				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
RX_MS_ID_D	4:0	GPIO ID for remote MS pin for Link D	0bXXXXX: This GPIO transmit ID

BACKTOP1 (0x400)

BIT	7	6	5	4	3	2	1	0
Field	CSIPLL3_LOCK	CSIPLL2_LOCK	CSIPLL1_LOCK	CSIPLL0_LOCK	LINE_SPL2	LINE_SPL0	RSVD	BACKTOP_EN
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b1
Access Type	Read Only	Read Only	Read Only	Read Only	Write, Read	Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CSIPLL3_LOCK	7	CSIPLL3 lock	0b0: PLL not locked 0b1: PLL locked
CSIPLL2_LOCK	6	CSIPLL2 lock	0b0: PLL not locked 0b1: PLL locked

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BITFIELD	BITS	DESCRIPTION	DECODE
CSIPLL1_LOCK	5	CSIPLL1 lock	0b0: PLL not locked 0b1: PLL locked
CSIPLL0_LOCK	4	CSIPLL0 lock	0b0: CSI2 0 PLL not locked 0b1: CSI2 0 PLL locked
LINE_SPL2	3	Enables line-based distribution to line memories for Video Pipe 2	0b0: Disable 0b1: Enable
LINE_SPL0	2	Enables line-based distribution to line memories for Video Pipe 0	0b0: Disable 0b1: Enable
BACKTOP_EN	0	Backtop write logic enable	0b0: Disable writes to BACKTOP register block 0b1: Enable writes to BACKTOP register block

BACKTOP11 (0x40A)

BIT	7	6	5	4	3	2	1	0
Field	cmd_overflow3	cmd_overflow2	cmd_overflow1	cmd_overflow0	LMO_3	LMO_2	LMO_1	LMO_0
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
cmd_overflow3	7	Pipe 3 command FIFO overflow	0b0: No overflow 0b1: Overflow
cmd_overflow2	6	Pipe 2 command FIFO overflow	0b0: No overflow 0b1: Overflow
cmd_overflow1	5	Pipe 1 command FIFO overflow	0b0: No overflow 0b1: Overflow
cmd_overflow0	4	Pipe 0 command FIFO overflow	0b0: No overflow 0b1: Overflow
LMO_3	3	Pipe 3 line memory overflow sticky register	0b0: No overflow 0b1: Overflow
LMO_2	2	Pipe 2 line memory overflow sticky register	0b0: No overflow 0b1: Overflow
LMO_1	1	Pipe 1 line memory overflow sticky register	0b0: No overflow 0b1: Overflow
LMO_0	0	Pipe 0 line memory overflow sticky register	0b0: No overflow 0b1: Overflow

BACKTOP12 (0x40B)

BIT	7	6	5	4	3	2	1	0
Field	soft_bpp_0[4:0]					–	CSI_OUT_EN	RSVD
Reset	0x00					–	0b1	0b0
Access Type	Write, Read					–	Write, Read	

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BITFIELD	BITS	DESCRIPTION	DECODE
soft_bpp_0	7:3	Pipe 0 BPP software-override: Software-override video data BPP.	0x8: Datatypes = 0x2A, 0x10-12, 0x31-37 0xA: Datatypes = 0x2B 0xC: Datatypes = 0x2C 0xE: Datatypes = 0x2D 0x10: Datatypes = 0x22, 0x1E, 0x2E 0x12: Datatypes = 0x23 0x14: Datatypes = 0x1F, 0x2F 0x18: Datatypes = 0x24, 0x30 All other values: Reserved
CSI_OUT_EN	1	Enables MIPI CSI output	0b0: CSI output disabled 0x1: CSI output enabled

BACKTOP13 (0x40C)

BIT	7	6	5	4	3	2	1	0
Field	soft_vc_1[3:0]				soft_vc_0[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
soft_vc_1	7:4	Pipe 1 VC software-override	0xX: Software-defined virtual channel for Pipe 1
soft_vc_0	3:0	Pipe 0 VC software-override	0xX: Software-defined virtual channel for Pipe 0

BACKTOP14 (0x40D)

BIT	7	6	5	4	3	2	1	0
Field	soft_vc_3[3:0]				soft_vc_2[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
soft_vc_3	7:4	Pipe 3 VC software-override	0xX: Software-defined virtual channel for Pipe 3
soft_vc_2	3:0	Pipe 2 VC software-override	0xX: Software-defined virtual channel for Pipe 2

BACKTOP15 (0x40E)

BIT	7	6	5	4	3	2	1	0
Field	soft_dt_1_h[1:0]		soft_dt_0[5:0]					
Reset	0x0		0x00					
Access Type	Write, Read		Write, Read					

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BITFIELD	BITS	DESCRIPTION	DECODE
soft_dt_1_h	7:6	Pipe 1 DT (high bits) software-override bitfield. Works together with soft_dt_1_l in BACKTOP16 register (0x40F).	0x10: GENERIC8 0x11: GENERIC8 0x12: EMBEDDED 0x1E: YUV422 8-bit 0x1F: YUV422 10-bit 0x22: RGB565 0x23: RGB666 0x24: RGB888 0x2A: RAW8 0x2B: RAW10 0x2C: RAW12 0x2D: RAW14 0x2E: RAW16 0x2F: RAW20 0x30: YUV422 12-bit 0x31: UDP8 0x32: UDP8 0x33: UDP8 0x34: UDP8 0x35: UDP8 0x36: UDP8 0x37: UDP8
soft_dt_0	5:0	Pipe 0 DT software-override.	0x10: GENERIC8 0x11: GENERIC8 0x12: EMBEDDED 0x1E: YUV422 8-bit 0x1F: YUV422 10-bit 0x22: RGB565 0x23: RGB666 0x24: RGB888 0x2A: RAW8 0x2B: RAW10 0x2C: RAW12 0x2D: RAW14 0x2E: RAW16 0x2F: RAW20 0x30: YUV422 12-bit 0x31: UDP8 0x32: UDP8 0x33: UDP8 0x34: UDP8 0x35: UDP8 0x36: UDP8 0x37: UDP8

BACKTOP16 (0x40F)

BIT	7	6	5	4	3	2	1	0
Field	soft_dt_2_h[3:0]				soft_dt_1_l[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

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BITFIELD	BITS	DESCRIPTION	DECODE
soft_dt_2_h	7:4	Pipe 2 DT (high bits) software-override bitfield. Works together with soft_dt_2_l in BACKTOP17 register (0x410).	0x10: GENERIC8 0x11: GENERIC8 0x12: EMBEDDED 0x1E: YUV422 8-bit 0x1F: YUV422 10-bit 0x22: RGB565 0x23: RGB666 0x24: RGB888 0x2A: RAW8 0x2B: RAW10 0x2C: RAW12 0x2D: RAW14 0x2E: RAW16 0x2F: RAW20 0x30: YUV422 12-bit 0x31: UDP8 0x32: UDP8 0x33: UDP8 0x34: UDP8 0x35: UDP8 0x36: UDP8 0x37: UDP8
soft_dt_1_l	3:0	Pipe 1 DT (low bits) software-override bitfield. Works together with soft_dt_1_h in BACKTOP16 register (0x40E).	0x10: GENERIC8 0x11: GENERIC8 0x12: EMBEDDED 0x1E: YUV422 8-bit 0x1F: YUV422 10-bit 0x22: RGB565 0x23: RGB666 0x24: RGB888 0x2A: RAW8 0x2B: RAW10 0x2C: RAW12 0x2D: RAW14 0x2E: RAW16 0x2F: RAW20 0x30: YUV422 12-bit 0x31: UDP8 0x32: UDP8 0x33: UDP8 0x34: UDP8 0x35: UDP8 0x36: UDP8 0x37: UDP8

BACKTOP17 (0x410)

BIT	7	6	5	4	3	2	1	0
Field	soft_dt_3[5:0]						soft_dt_2_l[1:0]	
Reset	0x00						0x0	
Access Type	Write, Read						Write, Read	

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BITFIELD	BITS	DESCRIPTION	DECODE
soft_dt_3	7:2	Pipe 3 DT software-override	0x10: GENERIC8 0x11: GENERIC8 0x12: EMBEDDED 0x1E: YUV422 8-bit 0x1F: YUV422 10-bit 0x22: RGB565 0x23: RGB666 0x24: RGB888 0x2A: RAW8 0x2B: RAW10 0x2C: RAW12 0x2D: RAW14 0x2E: RAW16 0x2F: RAW20 0x30: YUV422 12-bit 0x31: UDP8 0x32: UDP8 0x33: UDP8 0x34: UDP8 0x35: UDP8 0x36: UDP8 0x37: UDP8
soft_dt_2_l	1:0	Pipe 2 DT (low bits) software-override. Works together with soft_dt_2_h in BACKTOP16 register (0x40F).	0x10: GENERIC8 0x11: GENERIC8 0x12: EMBEDDED 0x1E: YUV422 8-bit 0x1F: YUV422 10-bit 0x22: RGB565 0x23: RGB666 0x24: RGB888 0x2A: RAW8 0x2B: RAW10 0x2C: RAW12 0x2D: RAW14 0x2E: RAW16 0x2F: RAW20 0x30: YUV422 12-bit 0x31: UDP8 0x32: UDP8 0x33: UDP8 0x34: UDP8 0x35: UDP8 0x36: UDP8 0x37: UDP8

BACKTOP18 (0x411)

BIT	7	6	5	4	3	2	1	0
Field	soft_bpp_2_h[2:0]			soft_bpp_1[4:0]				
Reset	0x0			0x00				
Access Type	Write, Read			Write, Read				

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BITFIELD	BITS	DESCRIPTION	DECODE
soft_bpp_2_h	7:5	Pipe 2 BPP (high bits) software-override bitfield: Works together with soft_bpp_2_l in BACKTOP19 register (0x412).	0bXX: High bits of software-defined BPP for Pipe 2
soft_bpp_1	4:0	Pipe 1 BPP software-override bitfield: Software override video data BPP.	0x8: Datatypes = 0x2A, 0x10-12, 0x31-37 0xA: Datatypes = 0x2B 0xC: Datatypes = 0x2C 0xE: Datatypes = 0x2D 0x10: Datatypes = 0x22, 0x1E, 0x2E 0x12: Datatypes = 0x23 0x14: Datatypes = 0x1F, 0x2F 0x18: Datatypes = 0x24, 0x30

BACKTOP19 (0x412)

BIT	7	6	5	4	3	2	1	0
Field	–	soft_bpp_3[4:0]					soft_bpp_2_l[1:0]	
Reset	–	0x00					0x0	
Access Type	–	Write, Read					Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
soft_bpp_3	6:2	Pipe 3 BPP software-override bitfield: Software override video data BPP.	0x8: Datatypes = 0x2A, 0x10-12, 0x31-37 0xA: Datatypes = 0x2B 0xC: Datatypes = 0x2C 0xE: Datatypes = 0x2D 0x10: Datatypes = 0x22, 0x1E, 0x2E 0x12: Datatypes = 0x23 0x14: Datatypes = 0x1F, 0x2F 0x18: Datatypes = 0x24, 0x30 0bXX: New BPP for Pipe 4
soft_bpp_2_l	1:0	Pipe 2 BPP software-override register: Software override video data BPP (low bits). Works together with soft_bpp_2_h in BACKTOP18 register (0x412).	0bXX: Low bits of software-defined BPP for Pipe 2

BACKTOP20 (0x413)

BIT	7	6	5	4	3	2	1	0
Field	phy0_csi_tx_dpll_fb_fraction_in_l[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
phy0_csi_tx_dpll_fb_fraction_in_l	7:0	Low byte of software-override value for CSI PHY0 frequency fine tuning	0xXX: PHY frequency fine tuning override low byte

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BACKTOP21 (0x414)

BIT	7	6	5	4	3	2	1	0
Field	bpp8dbl3	bpp8dbl2	bpp8dbl1	bpp8dbl0	phy0_csi_tx_dpll_fb_fraction_in_h[3:0]			
Reset	0b0	0b0	0b0	0b0	0x0			
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
bpp8dbl3	7	Pipe 3 BPP8 double-pixel register: BPP = 8 processed as 16-bit color	0b0: Disable process BPP = 8 as 16-bit color 0b1: Enable process BPP = 8 as 16-bit color
bpp8dbl2	6	Pipe 2 BPP8 double-pixel register: BPP = 8 processed as 16-bit color	0b0: Disable process BPP = 8 as 16-bit color 0b1: Enable process BPP = 8 as 16-bit color
bpp8dbl1	5	Pipe 1 BPP8 double-pixel register: BPP = 8 processed as 16-bit color	0b0: Disable process BPP = 8 as 16-bit color 0b1: Enable process BPP = 8 as 16-bit color
bpp8dbl0	4	Pipe 0 BPP8 double-pixel register: BPP = 8 processed as 16-bit color	0b0: Disable process BPP = 8 as 16-bit color 0b1: Enable process BPP = 8 as 16-bit color
phy0_csi_tx_dpll_fb_fraction_in_h	3:0	High nibble of software-override value for CSI PHY0 frequency fine tuning	0xX: PHY0 frequency fine tuning override high nibble

BACKTOP22 (0x415)

BIT	7	6	5	4	3	2	1	0
Field	override_bpp_vc_dt_1	override_bpp_vc_dt_0	phy0_csi_tx_dpll_fb_fraction_predef_en	phy0_csi_tx_dpll_predef_freq[4:0]				
Reset	0b0	0b0	0b1	0x0F				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
override_bpp_vc_dt_1	7	Pipe 1 software-override enable bitfield	0b0: Disable 0b1: Enable
override_bpp_vc_dt_0	6	Pipe 0 software-override enable bitfield	0b0: Disable 0b1: Enable
phy0_csi_tx_dpll_fb_fraction_predef_en	5	MIPI PHY0 software-override disable for frequency fine tuning	0b0: Enable software override for frequency fine tuning 0b1: Disable software override for frequency fine tuning
phy0_csi_tx_dpll_predef_freq	4:0	MIPI PHY0 DPLL frequency bitfield: Set DPLL frequency on multiple of 100MHz. DPHY: Clock frequency is half, data rate is equivalent bps/lane. CPHY: 2.28bits/symbol.	DPHY data rate/lane 0x02: 200MHz DPLL, 200Mbps/lane ... 0x19: 2500MHz DPLL, 2.5Gbps/lane CPHY data rate/trio 0x02: 200MHz DPLL,456Mbps/lane ... 0x19: 2500MHz DPLL, 5.7Gbps/lane

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BACKTOP23 (0x416)

BIT	7	6	5	4	3	2	1	0
Field	phy1_csi_tx_dpll_fb_fraction_in_l[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
phy1_csi_tx_dpll_fb_fraction_in_l	7:0	Low byte of software-override value for CSI PHY1 frequency fine tuning	0xXX: PHY1 frequency fine tuning override low byte

BACKTOP24 (0x417)

BIT	7	6	5	4	3	2	1	0
Field	bpp8dbl3_mode	bpp8dbl2_mode	bpp8dbl1_mode	bpp8dbl0_mode	phy1_csi_tx_dpll_fb_fraction_in_h[3:0]			
Reset	0b0	0b0	0b0	0b0	0x0			
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
bpp8dbl3_mode	7	Pipe 3 BPP8 double-pixel mode register: 8-bit alternate bit mapping to rams	0b0: Alternative bit mapping not selected 0b1: Alternative bit mapping selected
bpp8dbl2_mode	6	Pipe 2 BPP8 double-pixel mode register: 8-bit alternate bit mapping to rams	0b0: Alternative bit mapping not selected 0b1: Alternative bit mapping selected
bpp8dbl1_mode	5	Pipe 1 BPP8 double-pixel mode register: 8-bit alternate bit mapping to rams	0b0: Alternative bit mapping not selected 0b1: Alternative bit mapping selected
bpp8dbl0_mode	4	Pipe 0 BPP8 double-pixel mode register: 8-bit alternate bit mapping to rams	0b0: Alternative bit mapping not selected 0b1: Alternative bit mapping selected
phy1_csi_tx_dpll_fb_fraction_in_h	3:0	High nibble of software-override value for CSI PHY1 frequency fine tuning	0xX: PHY1 frequency fine tuning override high nibble

BACKTOP25 (0x418)

BIT	7	6	5	4	3	2	1	0
Field	override_bpp_vc_dt_3	override_bpp_vc_dt_2	phy1_csi_tx_dpll_fb_fraction_predef_en	phy1_csi_tx_dpll_predef_freq[4:0]				
Reset	0b0	0b0	0b1	0x0F				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
override_bpp_vc_dt_3	7	Pipe 3 software-override enable bitfield	0b0: Disable 0b1: Enable
override_bpp_vc_dt_2	6	Pipe 2 software-override enable bitfield	0b0: Disable 0b1: Enable

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BITFIELD	BITS	DESCRIPTION	DECODE
phy1_csi_tx_dpll_fb_fraction_predef_en	5	MIPI PHY1 software-override disable for frequency fine tuning	0b0: Enable software override for frequency fine tuning 0b1: Disable software override for frequency fine tuning
phy1_csi_tx_dpll_predef_freq	4:0	MIPI PHY1 DPLL frequency bitfield: Set DPLL frequency on multiple of 100MHz. DPHY: Clock frequency is half; data rate is equivalent bps/lane. CPHY: 2.28bits/symbol.	DPHY data rate/lane 0x02: 200MHz DPLL, 200Mbps/lane ... 0x19: 2500MHz DPLL, 2.5Gbps/lane CPHY data rate/trio 0x02: 200MHz DPLL,456Mbps/lane ... 0x19: 2500MHz DPLL, 5.7Gbps/lane

BACKTOP26 (0x419)

BIT	7	6	5	4	3	2	1	0
Field	phy2_csi_tx_dpll_fb_fraction_in_l[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
phy2_csi_tx_dpll_fb_fraction_in_l	7:0	Low byte of software-override value for CSI PHY2 frequency fine tuning	0xXX: PHY2 frequency fine tuning override low byte

BACKTOP27 (0x41A)

BIT	7	6	5	4	3	2	1	0
Field	yuv_8_10_mux_mode3	yuv_8_10_mux_mode2	yuv_8_10_mux_mode1	yuv_8_10_mux_mode0	phy2_csi_tx_dpll_fb_fraction_in_h[3:0]			
Reset	0x0	0x0	0x0	0x0	0x0			
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
yuv_8_10_mux_mode3	7	Pipe 3 YUV422 8-bit and 10-bit mux	0b0: Disable 8-/10-bit mux 0b1: Enable 8-/10-bit mux
yuv_8_10_mux_mode2	6	Pipe 2 YUV422 8-bit and 10-bit mux	0b0: Disable 8-/10-bit mux 0b1: Enable 8-/10-bit mux
yuv_8_10_mux_mode1	5	Pipe 1 YUV422 8-bit and 10-bit mux	0b0: Disable 8-/10-bit mux 0b1: Enable 8-/10-bit mux
yuv_8_10_mux_mode0	4	Pipe 0 YUV422 8-bit and 10-bit mux	0b0: Disable 8-/10-bit mux 0b1: Enable 8-/10-bit mux
phy2_csi_tx_dpll_fb_fraction_in_h	3:0	High nibble of software-override value for CSI PHY2 frequency fine tuning	0xX: PHY2 frequency fine tuning override high nibble

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BACKTOP28 (0x41B)

BIT	7	6	5	4	3	2	1	0
Field	override_bpp_vc_dt_5	override_bpp_vc_dt_4	phy2_csi_tx_dpll_fb_fraction_predef_en	phy2_csi_tx_dpll_predef_freq[4:0]				
Reset	0b0	0b0	0b1	0x0F				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
override_bpp_vc_dt_5	7	Pipe 5 software-override enable for BPP, VC, and DT	0b0: Disable 0b1: Enable
override_bpp_vc_dt_4	6	Pipe 4 software-override enable for BPP, VC, and DT	0b0: Disable 0b1: Enable
phy2_csi_tx_dpll_fb_fraction_predef_en	5	MIPI PHY2 software-override disable for frequency fine tuning	0b0: Enable software override for frequency fine tuning 0b1: Disable software override for frequency fine tuning
phy2_csi_tx_dpll_predef_freq	4:0	MIPI PHY2 DPLL frequency register: Set DPLL frequency on multiple of 100MHz. DPHY: Clock frequency is half; data rate is equivalent bps/lane. CPHY: 2.28bits/symbol.	DPHY data rate/lane 0x02: 200MHz DPLL, 200Mbps/lane ... 0x19: 2500MHz DPLL, 2.5Gbps/lane CPHY data rate/trio 0x02: 200MHz DPLL,456Mbps/lane ... 0x19: 2500MHz DPLL, 5.7Gbps/lane

BACKTOP29 (0x41C)

BIT	7	6	5	4	3	2	1	0
Field	phy3_csi_tx_dpll_fb_fraction_in_l[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
phy3_csi_tx_dpll_fb_fraction_in_l	7:0	Low byte of software-override value for CSI PHY3 frequency fine tuning	0xXX: PHY3 frequency fine tuning override low byte

BACKTOP30 (0x41D)

BIT	7	6	5	4	3	2	1	0
Field	override_bpp_vc_dt_7	override_bpp_vc_dt_6	bpp10dbl3_mode	bpp10dbl3	phy3_csi_tx_dpll_fb_fraction_in_h[3:0]			
Reset	0b0	0b0	0b0	0b0	0x0			
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read			

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BITFIELD	BITS	DESCRIPTION	DECODE
override_bpp_vc_dt_7	7	Pipe 7 software-override enable for BPP, VC, and DT	0b0: Disable 0b1: Enable
override_bpp_vc_dt_6	6	Pipe 6 software-override enable for BPP, VC, and DT	0b0: Disable 0b1: Enable
bpp10dbl3_mode	5	Pipe 3 BPP10 double-pixel mode register: 10-bit alternate bit mapping to rams	0b0: Alternative bit mapping not selected 0b1: Alternative bit mapping selected
bpp10dbl3	4	Pipe 3 BPP10 double-pixel register: BPP = 10 processed as 20-bit color	0b0: Disable process BPP = 10 as 20-bit color 0b1: Enable process BPP = 10 as 20-bit color
phy3_csi_tx_dpll_fb_fraction_in_h	3:0	High nibble of software-override value for CSI PHY3 frequency fine tuning	0xX: PHY3 frequency fine tuning override high nibble

BACKTOP31 (0x41E)

BIT	7	6	5	4	3	2	1	0
Field	bpp10dbl2_mode	bpp10dbl2	phy3_csi_tx_dpll_fb_fraction_predef_en	phy3_csi_tx_dpll_predef_freq[4:0]				
Reset	0b0	0b0	0b1	0x0F				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
bpp10dbl2_mode	7	Pipe 2 BPP10 double-pixel mode register: 10-bit alternate bit mapping to rams	0b0: Alternative bit mapping not selected 0b1: Alternative bit mapping selected
bpp10dbl2	6	Pipe 2 BPP10 double-pixel register: BPP = 10 processed as 20-bit color	0b0: Disable process BPP = 10 as 20-bit color 0b1: Enable process BPP = 10 as 20-bit color
phy3_csi_tx_dpll_fb_fraction_predef_en	5	MIPI PHY3 software-override disable for frequency fine tuning	0b0: Enable software override for frequency fine tuning 0b1: Disable software override for frequency fine tuning
phy3_csi_tx_dpll_predef_freq	4:0	MIPI PHY3 DPLL frequency register: Set DPLL frequency on multiple of 100MHz. DPHY: Clock frequency is half; data rate is equivalent bps/lane. CPHY: 2.28bits/symbol.	DPHY data rate/lane 0x02: 200MHz DPLL, 200Mbps/lane ... 0x19: 2500MHz DPLL, 2.5Gbps/lane CPHY data rate/trio 0x02: 200MHz DPLL,456Mbps/lane ... 0x19: 2500MHz DPLL, 5.7Gbps/lane

BACKTOP32 (0x41F)

BIT	7	6	5	4	3	2	1	0
Field	bpp10dbl1_mode	bpp10dbl1	bpp10dbl0_mode	bpp10dbl0	bpp12dbl3	bpp12dbl2	bpp12dbl1	bpp12dbl0
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

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BITFIELD	BITS	DESCRIPTION	DECODE
bpp10dbl1_mode	7	Pipe 1 BPP10 double-pixel mode register: 10-bit alternate bit mapping to rams	0b0: Alternative bit mapping not selected 0b1: Alternative bit mapping selected
bpp10dbl1	6	Pipe 1 BPP10 double-pixel register: BPP = 10 processed as 20-bit color	0b0: Disable process BPP = 10 as 20-bit color 0b1: Enable process BPP = 10 as 20-bit color
bpp10dbl0_mode	5	Pipe 0 BPP10 double-pixel mode register: 10-bit alternate bit mapping to rams	0b0: Alternative bit mapping not selected 0b1: Alternative bit mapping selected
bpp10dbl0	4	Pipe 0 BPP10 double-pixel register: BPP = 10 processed as 20-bit color	0b0: Disable process BPP = 10 as 20-bit color 0b1: Enable process BPP = 10 as 20-bit color
bpp12dbl3	3	Pipe 3 BPP12 double-pixel register: BPP = 12 processed as 24-bit color	0b0: Disable process BPP = 12 as 24-bit color 0b1: Enable process BPP = 12 as 24-bit color
bpp12dbl2	2	Pipe 2 BPP12 double-pixel register: BPP = 12 processed as 24-bit color	0b0: Disable process BPP = 12 as 24-bit color 0b1: Enable process BPP = 12 as 24-bit color
bpp12dbl1	1	Pipe 1 BPP12 double-pixel register: BPP = 12 processed as 24-bit color	0b0: Disable process BPP = 12 as 24-bit color 0b1: Enable process BP P= 12 as 24-bit color
bpp12dbl0	0	Pipe 0 BPP12 double-pixel register: BPP = 12 processed as 24-bit color	0b0: Disable process BPP = 12 as 24-bit color 0b1: Enable process BPP = 12 as 24-bit color

BACKTOP1 (0x420)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	LINE_SPL6	LINE_SPL4	–	–
Reset	–	–	–	–	0b0	0b0	–	–
Access Type	–	–	–	–	Write, Read	Write, Read	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
LINE_SPL6	3	Enables line-based distribution to line memories for Video Pipe 6	0b0: Disable 0b1: Enable
LINE_SPL4	2	Enables line-based distribution to line memories for Video Pipe 4	0b0: Disable 0b1: Enable

BACKTOP10 (0x429)

BIT	7	6	5	4	3	2	1	0
Field	DE_SEL7	DE_SEL6	DE_SEL5	DE_SEL4	LS_LE_EN7	LS_LE_EN6	LS_LE_EN5	LS_LE_EN4
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DE_SEL7	7	Uses HS for creation of long packets instead of DE	0b0: Use DE for creation of long packets 0b1: Use HS for creation of long packets
DE_SEL6	6	Uses HS for creation of long packets instead of DE	0b0: Use DE for creation of long packets 0b1: Use HS for creation of long packets
DE_SEL5	5	Uses HS for creation of long packets instead of DE	0b0: Use DE for creation of long packets 0b1: Use HS for creation of long packets
DE_SEL4	4	Uses HS for creation of long packets instead of DE	0b0: Use DE for creation of long packets 0b1: Use HS for creation of long packets
LS_LE_EN7	3	Enables line start line end short packets	0b0: Disable line start line end short packets 0b1: Enable line start line end short packets

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BITFIELD	BITS	DESCRIPTION	DECODE
LS_LE_EN6	2	Enables line start line end short packets	0b0: Disable line start line end short packets 0b1: Enable line start line end short packets
LS_LE_EN5	1	Enables line start line end short packets	0b0: Disable line start line end short packets 0b1: Enable line start line end short packets
LS_LE_EN4	0	Enables line start line end short packets	0b0: Disable line start line end short packets 0b1: Enable line start line end short packets

BACKTOP11 (0x42A)

BIT	7	6	5	4	3	2	1	0
Field	cmd_overflow7	cmd_overflow6	cmd_overflow5	cmd_overflow4	LMO_7	LMO_6	LMO_5	LMO_4
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
cmd_overflow7	7	Pipe 7 command FIFO overflow	0b0: No overflow 0b1: Overflow
cmd_overflow6	6	Pipe 6 command FIFO overflow	0b0: No overflow 0b1: Overflow
cmd_overflow5	5	Pipe 5 command FIFO overflow	0b0: No overflow 0b1: Overflow
cmd_overflow4	4	Pipe 4 command FIFO overflow	0b0: No overflow 0b1: Overflow
LMO_7	3	Pipe 7 line memory overflow sticky bitfield	0b0: No overflow 0b1: Overflow
LMO_6	2	Pipe 6 line memory overflow sticky bitfield	0b0: No overflow 0b1: Overflow
LMO_5	1	Pipe 5 line memory overflow sticky bitfield	0b0: No overflow 0b1: Overflow
LMO_4	0	Pipe 4 line memory overflow sticky bitfield	0b0: No overflow 0b1: Overflow

BACKTOP12 (0x42B)

BIT	7	6	5	4	3	2	1	0
Field	soft_bpp_4[4:0]					–	–	–
Reset	0x00					–	–	–
Access Type	Write, Read					–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
soft_bpp_4	7:3	Pipe 4 BPP software-override: Software override video data BPP.	0x8: Datatypes = 0x2A, 0x10-12, 0x31-37 0xA: Datatypes = 0x2B 0xC: Datatypes = 0x2C 0xE: Datatypes = 0x2D 0x10: Datatypes = 0x22, 0x1E, 0x2E, 0x12: Datatypes = 0x23 0x14: Datatypes = 0x1F, 0x2F 0x18: Datatypes = 0x24, 0x30

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BACKTOP13 (0x42C)

BIT	7	6	5	4	3	2	1	0
Field	soft_vc_5[3:0]				soft_vc_4[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
soft_vc_5	7:4	Pipe 5 VC software-override	0xX: Software-defined virtual channel for Pipe 5
soft_vc_4	3:0	Pipe 4 VC software-override	0xX: Software-defined virtual channel for Pipe 4

BACKTOP14 (0x42D)

BIT	7	6	5	4	3	2	1	0
Field	soft_vc_7[3:0]				soft_vc_6[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
soft_vc_7	7:4	Pipe 7 VC software-override	0xX: Software-defined virtual channel for Pipe 7
soft_vc_6	3:0	Pipe 6 VC software-override	0xX: Software-defined virtual channel for Pipe 6

BACKTOP15 (0x42E)

BIT	7	6	5	4	3	2	1	0
Field	soft_dt_5_h[1:0]		soft_dt_4[5:0]					
Reset	0x0		0x00					
Access Type	Write, Read		Write, Read					

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BITFIELD	BITS	DESCRIPTION	DECODE
soft_dt_5_h	7:6	Pipe 5 DT software-override (high nibble). Works together with soft_dt_5_l.	0x10: GENERIC8 0x11: GENERIC8 0x12: EMBEDDED 0x1E: YUV422 8-bit 0x1F: YUV422 10-bit 0x22: RGB565 0x23: RGB666 0x24: RGB888 0x2A: RAW8 0x2B: RAW10 0x2C: RAW12 0x2D: RAW14 0x2E: RAW16 0x2F: RAW20 0x30: YUV422 12-bit 0x31: UDP8 0x32: UDP8 0x33: UDP8 0x34: UDP8 0x35: UDP8 0x36: UDP8 0x37: UDP8
soft_dt_4	5:0	Pipe 4 DT software-override	0x10: GENERIC8 0x11: GENERIC8 0x12: EMBEDDED 0x1E: YUV422 8-bit 0x1F: YUV422 10-bit 0x22: RGB565 0x23: RGB666 0x24: RGB888 0x2A: RAW8 0x2B: RAW10 0x2C: RAW12 0x2D: RAW14 0x2E: RAW16 0x2F: RAW20 0x30: YUV422 12-bit 0x31: UDP8 0x32: UDP8 0x33: UDP8 0x34: UDP8 0x35: UDP8 0x36: UDP8 0x37: UDP8

BACKTOP16 (0x42F)

BIT	7	6	5	4	3	2	1	0
Field	soft_dt_6_h[3:0]				soft_dt_5_l[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

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BITFIELD	BITS	DESCRIPTION	DECODE
soft_dt_6_h	7:4	Pipe 6 DT software-override (high nibble). Works together with soft_dt_6_l.	0x10: GENERIC8 0x11: GENERIC8 0x12: EMBEDDED 0x1E: YUV422 8-bit 0x1F: YUV422 10-bit 0x22: RGB565 0x23: RGB666 0x24: RGB888 0x2A: RAW8 0x2B: RAW10 0x2C: RAW12 0x2D: RAW14 0x2E: RAW16 0x2F: RAW20 0x30: YUV422 12-bit 0x31: UDP8 0x32: UDP8 0x33: UDP8 0x34: UDP8 0x35: UDP8 0x36: UDP8 0x37: UDP8
soft_dt_5_l	3:0	Pipe 5 DT software-override (low nibble)	0xXX: Low bits of software-defined data type for Pipeline 5

BACKTOP17 (0x430)

BIT	7	6	5	4	3	2	1	0
Field	soft_dt_7[5:0]						soft_dt_6_l[1:0]	
Reset	0x00						0x0	
Access Type	Write, Read						Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
soft_dt_7	7:2	Pipe 7 DT software-override	0x10: GENERIC8 0x11: GENERIC8 0x12: EMBEDDED 0x1E: YUV422 8-bit 0x1F: YUV422 10-bit 0x22: RGB565 0x23: RGB666 0x24: RGB888 0x2A: RAW8 0x2B: RAW10 0x2C: RAW12 0x2D: RAW14 0x2E: RAW16 0x2F: RAW20 0x30: YUV422 12-bit 0x31: UDP8 0x32: UDP8 0x33: UDP8 0x34: UDP8 0x35: UDP8 0x36: UDP8 0x37: UDP8

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BITFIELD	BITS	DESCRIPTION	DECODE
soft_dt_6_l	1:0	Pipe 6 DT software-override (low nibble)	0xXX: Low bits of software-defined data type for Pipeline 6

BACKTOP18 (0x431)

BIT	7	6	5	4	3	2	1	0
Field	soft_bpp_6_h[2:0]			soft_bpp_5[4:0]				
Reset	0x0			0x00				
Access Type	Write, Read			Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
soft_bpp_6_h	7:5	Pipe 6 BPP software-override (high bits): Software-override video data BPP. Works together with soft_bpp_6_l.	0x8: Datatypes = 0x2A, 0x10-12, 0x31-37 0xA: Datatypes = 0x2B 0xC: Datatypes = 0x2C 0xE: Datatypes = 0x2D 0x10: Datatypes = 0x22, 0x1E, 0x2E, 0x12: Datatypes = 0x23 0x14: Datatypes = 0x1F, 0x2F 0x18: Datatypes = 0x24, 0x30
soft_bpp_5	4:0	Pipe 5 BPP software-override: Software override video data BPP.	0x8: Datatypes = 0x2A, 0x10-12, 0x31-37 0xA: Datatypes = 0x2B 0xC: Datatypes = 0x2C 0xE: Datatypes = 0x2D 0x10: Datatypes = 0x22, 0x1E, 0x2E, 0x12: Datatypes = 0x23 0x14: Datatypes = 0x1F, 0x2F 0x18: Datatypes = 0x24, 0x30

BACKTOP19 (0x432)

BIT	7	6	5	4	3	2	1	0
Field	–	soft_bpp_7[4:0]					soft_bpp_6_l[1:0]	
Reset	–	0x00					0x0	
Access Type	–	Write, Read					Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
soft_bpp_7	6:2	Pipe 7 BPP software-override: Software override video data BPP.	0x8: Datatypes = 0x2A, 0x10-12, 0x31-37 0xA: Datatypes = 0x2B 0xC: Datatypes = 0x2C 0xE: Datatypes = 0x2D 0x10: Datatypes = 0x22, 0x1E, 0x2E, 0x12: Datatypes = 0x23 0x14: Datatypes = 0x1F, 0x2F 0x18: Datatypes = 0x24, 0x30
soft_bpp_6_l	1:0	Pipe 6 BPP software-override (low nibble): Software override video data BPP	0bXX: Low bits of software-defined BPP

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BACKTOP21 (0x434)

BIT	7	6	5	4	3	2	1	0
Field	bpp8dbl7	bpp8dbl6	bpp8dbl5	bpp8dbl4	–	–	–	–
Reset	0b0	0b0	0b0	0b0	–	–	–	–
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
bpp8dbl7	7	Pipe 7 BPP8 double-pixel: BPP = 8 processed as 16-bit color	0b0: Disable process BPP = 8 as 16-bit color 0b1: Enable process BPP = 8 as 16-bit color
bpp8dbl6	6	Pipe 6 BPP8 double-pixel: BPP = 8 processed as 16-bit color	0b0: Disable process BPP = 8 as 16-bit color 0b1: Enable process BPP = 8 as 16-bit color
bpp8dbl5	5	Pipe 5 BPP8 double-pixel: BPP = 8 processed as 16-bit color	0b0: Disable process BPP = 8 as 16-bit color 0b1: Enable process BPP = 8 as 16-bit color
bpp8dbl4	4	Pipe 4 BPP8 double-pixel: BPP = 8 processed as 16-bit color	0b0: Disable process BPP = 8 as 16-bit color 0b1: Enable process BPP = 8 as 16-bit color

BACKTOP22 (0x435)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	n_vs_block[3:0]			
Reset	–	–	–	–	0b1			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
n_vs_block	3:0	Frame block: Block the first 1-15 frames after video lock	0x0: All frames out 0x1: Block the first frame . . . 0xF: Block the first 15 frames

BACKTOP23 (0x436)

BIT	7	6	5	4	3	2	1	0
Field	dis_vs7	dis_vs6	dis_vs5	dis_vs4	dis_vs3	dis_vs2	dis_vs1	dis_vs0
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
dis_vs7	7	Pipe 7 disable VS: Disable the transmission of VS to MIPI output.	0b0: Enable VS out 0b1: Disable VS out
dis_vs6	6	Pipe 6 disable VS: Disable the transmission of VS to MIPI output.	0b0: Enable VS out 0b1: Disable VS out
dis_vs5	5	Pipe 5 disable VS: Disable the transmission of VS to MIPI output.	0b0: Enable VS out 0b1: Disable VS out

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BITFIELD	BITS	DESCRIPTION	DECODE
dis_vs4	4	Pipe 4 disable VS: Disable the transmission of VS to MIPI output.	0b0: Enable VS out 0b1: Disable VS out
dis_vs3	3	Pipe 3 disable VS: Disable the transmission of VS to MIPI output.	0b0: Enable VS out 0b1: Disable VS out
dis_vs2	2	Pipe 2 disable VS: Disable the transmission of VS to MIPI output.	0b0: Enable VS out 0b1: Disable VS out
dis_vs1	1	Pipe 1 disable VS: Disable the transmission of VS to MIPI output.	0b0: Enable VS out 0b1: Disable VS out
dis_vs0	0	Pipe 0 disable VS: Disable the transmission of VS to MIPI output.	0b0: Enable VS out 0b1: Disable VS out

BACKTOP24 (0x437)

BIT	7	6	5	4	3	2	1	0
Field	bpp8dbl7_mode	bpp8dbl6_mode	bpp8dbl5_mode	bpp8dbl4_mode	–	–	–	–
Reset	0b0	0b0	0b0	0b0	–	–	–	–
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
bpp8dbl7_mode	7	Pipe 7 BPP8 double-pixel mode: 8-bit alternate bit mapping to memory	0b0: Alternative bit mapping not selected 0b1: Alternative bit mapping selected
bpp8dbl6_mode	6	Pipe 6 BPP8 double-pixel mode: 8-bit alternate bit mapping to memory	0b0: Alternative bit mapping not selected 0b1: Alternative bit mapping selected
bpp8dbl5_mode	5	Pipe 5 BPP8 double-pixel mode: 8-bit alternate bit mapping to memory	0b0: Alternative bit mapping not selected 0b1: Alternative bit mapping selected
bpp8dbl4_mode	4	Pipe 4 BPP8 double-pixel mode: 8-bit alternate bit mapping to memory	0b0: Alternative bit mapping not selected 0b1: Alternative bit mapping selected

BACKTOP25 (0x438)

BIT	7	6	5	4	3	2	1	0
Field	mem_err7	mem_err6	mem_err5	mem_err4	mem_err3	mem_err2	mem_err1	mem_err0
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
mem_err7	7	Pipe 7 line memory error	0b0: No MEM error 0b1: MEM error detected
mem_err6	6	Pipe 6 line memory error	0b0: No MEM error 0b1: MEM error detected
mem_err5	5	Pipe 5 line memory error	0b0: No MEM error 0b1: MEM error detected

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BITFIELD	BITS	DESCRIPTION	DECODE
mem_err4	4	Pipe 4 line memory error	0b0: No MEM error 0b1: MEM error detected
mem_err3	3	Pipe 3 line memory error	0b0: No MEM error 0b1: MEM error detected
mem_err2	2	Pipe 2 line memory error	0b0: No MEM error 0b1: MEM error detected
mem_err1	1	Pipe1 line memory error	0b0: No MEM error 0b1: MEM error detected
mem_err0	0	Pipe 0 line memory error	0b0: No MEM error 0b1: MEM error detected

BACKTOP27 (0x43A)

BIT	7	6	5	4	3	2	1	0
Field	yuv_8_10_mux_mode7	yuv_8_10_mux_mode6	yuv_8_10_mux_mode5	yuv_8_10_mux_mode4	–	–	–	–
Reset	0x0	0x0	0x0	0x0	–	–	–	–
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
yuv_8_10_mux_mode7	7	Pipe 7 YUV422 8-bit and 10-bit mux	0b0: Disable 8-/10-bit mux 0b1: Enable 8-/10-bit mux
yuv_8_10_mux_mode6	6	Pipe 6 YUV422 8-bit and 10-bit mux	0b0: Disable 8-/10-bit mux 0b1: Enable 8-/10-bit mux
yuv_8_10_mux_mode5	5	Pipe 5 YUV422 8-bit and 10-bit mux	0b0: Disable 8-/10-bit mux 0b1: Enable 8-/10-bit mux
yuv_8_10_mux_mode4	4	Pipe 4 YUV422 8-bit and 10-bit mux	0b0: Disable 8-/10-bit mux 0b1: Enable 8-/10-bit mux

BACKTOP30 (0x43D)

BIT	7	6	5	4	3	2	1	0
Field	–	–	bpp10dbl7_mode	bpp10dbl7	–	–	–	–
Reset	–	–	0b0	0b0	–	–	–	–
Access Type	–	–	Write, Read	Write, Read	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
bpp10dbl7_mode	5	Pipe 7 BPP10 double-pixel mode: 10-bit alternate bit mapping to memory	0b0: Alternative bit mapping not selected 0b1: Alternative bit mapping selected
bpp10dbl7	4	Pipe 7 BPP10 double-pixel: BPP = 10 processed as 20-bit color	0b0: Disable process BPP = 10 as 20-bit color 0b1: Enable process BPP = 10 as 20-bit color

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BACKTOP31 (0x43E)

BIT	7	6	5	4	3	2	1	0
Field	bpp10dbl6_mode	bpp10dbl6	–	–	–	–	–	–
Reset	0b0	0b0	–	–	–	–	–	–
Access Type	Write, Read	Write, Read	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
bpp10dbl6_mode	7	Pipe 6 BPP10 double-pixel mode: 10-bit write map alternate mode to memory	0b0: Alternative bit mapping not selected 0b1: Alternative bit mapping selected
bpp10dbl6	6	Pipe 6 BPP10 double-pixel: BPP = 10 processed as 20-bit color	0b0: Disable process BPP = 10 as 20-bit color 0b1: Enable process BPP = 10 as 20-bit color

BACKTOP32 (0x43F)

BIT	7	6	5	4	3	2	1	0
Field	bpp10dbl5_mode	bpp10dbl5	bpp10dbl4_mode	bpp10dbl4	bpp12dbl7	bpp12dbl6	bpp12dbl5	bpp12dbl4
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
bpp10dbl5_mode	7	Pipe 5 BPP10 double-pixel mode: 10-bit write map alternate mode to memory	0b0: Alternative bit mapping not selected 0b1: Alternative bit mapping selected
bpp10dbl5	6	Pipe 5 BPP10 double-pixel: BPP = 10 processed as 20-bit color	0b0: Disable process BPP = 10 as 20-bit color 0b1: Enable process BPP = 10 as 20-bit color
bpp10dbl4_mode	5	Pipe 4 BPP10 double-pixel mode: 10-bit write map alternate mode to memory	0b0: Alternative bit mapping not selected 0b1: Alternative bit mapping selected
bpp10dbl4	4	Pipe 4 BPP10 double-pixel: BPP = 10 processed as 20-bit color	0b0: Disable process BPP = 10 as 20-bit color 0b1: Enable process BPP = 10 as 20-bit color
bpp12dbl7	3	Pipe 7 BPP12 double-pixel: BPP = 12 processed as 24-bit color	0b0: Disable process BPP = 12 as 24-bit color 0b1: Enable process BPP = 12 as 24-bit color
bpp12dbl6	2	Pipe 6 BPP12 double-pixel: BPP = 12 processed as 24-bit color	0b0: Disable process BPP = 12 as 24-bit color 0b1: Enable process BPP = 12 as 24-bit color
bpp12dbl5	1	Pipe 5 BPP12 double-pixel: BPP = 12 processed as 24-bit color	0b0: Disable process BPP = 12 as 24-bit color 0b1: Enable process BPP = 12 as 24-bit color
bpp12dbl4	0	Pipe 4 BPP12 double-pixel: BPP = 12 processed as 24bit color	0b0: Disable process BPP = 12 as 24-bit color 0b1: Enable process BPP = 12 as 24-bit color

FSYNC_0 (0x4A0)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	FSYNC_OUT_PIN	EN_VS_GEN	FSYNC_MODE[1:0]		FSYNC_METH[1:0]	
Reset	0x0	0x0	0b0	0x0	0x3		0x1	
Access Type			Write, Read	Write, Read	Write, Read		Write, Read	

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BITFIELD	BITS	DESCRIPTION	DECODE
FSYNC_OUT_PIN	5	Selects pin to output frame sync signal (effective only when FSYNC_METH = 01)	0b0: MFP2 0b1: MFP10
EN_VS_GEN	4	Selects whether or not VS is generated internally by the frame sync generator (not effective when FSYNC_MODE = 11)	0b0: VS is not generated internally by the frame sync generator 0b1: VS is generated internally by the frame sync generator
FSYNC_MODE	3:2	Frame Synchronization Mode	0b00: Frame sync generation is on. GPIO is not used as FSYNC input or output 0b01: Frame sync generation is on. GPIO is used as FSYNC output and drives a subordinate device 0b10: Frame sync generation is off. GPIO is used as FSYNC input driven by a main device for GMSL1 links. Any enabled GPIO input can be used as FSYNC input for GMSL2 links. 0b11: Frame sync generation is off. GPIO is not used as FSYNC input or output
FSYNC_METH	1:0	Frame Synchronization Method	0b00: Manual 0b01: Semi-auto 0b10: Auto 0b11: Reserved

FSYNC_1 (0x4A1)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		RSVD[1:0]		FSYNC_PER_DIV[3:0]			
Reset	0x0		0x0		0x0			
Access Type					Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
FSYNC_PER_DIV	3:0	Frame sync transmission period in terms of VSYNC periods	0x0: 1 0x1: 2 0x2: 3 0x3: 6 0x4: 8 0x5: 10 0x6: 12 0x7: 16 0x8: 20 0x9: 24 0xA: 32 0xB: 48 0xC: 64 0xD: 80 0xE: 96 0xF: 128

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FSYNC_2 (0x4A2)

BIT	7	6	5	4	3	2	1	0
Field	MST_LINK_SEL[2:0]			K_VAL_SIGN	K_VAL[3:0]			
Reset	0x4			0x0	0x1			
Access Type	Write, Read			Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
MST_LINK_SEL	7:5	Main link select for frame sync generation	0b000: Video 0 0b001: Video 1 0b010: Video 2 0b011: Video 3 0b100: Auto select 0b101: Auto select 0b110: Auto select 0b111: Auto select
K_VAL_SIGN	4	Sign bit of K_VAL	0b0: K_VAL is positive 0b1: K_VAL is negative
K_VAL	3:0	Desired frame sync margin with respect to either the VSYNC of the slowest link in automatic mode or the VSYNC of the main link in semi-automatic mode.	0x0: 0.85µs 0x1: 1.71µs 0x2: 2.56µs 0x3: 3.41µs 0x4: 4.27µs 0x5: 5.12µs 0x6: 5.97µs 0x7: 6.83µs 0x8: 8.53µs 0x9: 10.24µs 0xA: 11.95µs 0xB: 13.65µs 0xC: 17.07µs 0xD: 20.48µs 0xE: 23.89µs 0xF: 27.31µs

FSYNC_3 (0x4A3)

BIT	7	6	5	4	3	2	1	0
Field	P_VAL_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
P_VAL_L	7:0	Low byte of desired frame sync margin in terms of PCLK cycles with respect to the VSYNC of the slowest link in automatic mode or with respect to the VSYNC of the main link in semi-automatic mode	0bXXXXXXXX: Low byte of desired frame sync margin

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FSYNC_4 (0x4A4)

BIT	7	6	5	4	3	2	1	0
Field	–	–	P_VAL_SIGN	P_VAL_H[4:0]				
Reset	–	–	0x0	0x00				
Access Type	–	–	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
P_VAL_SIGN	5	Sign bit of P_VAL	0b0: P_VAL is positive 0b1: P_VAL is negative
P_VAL_H	4:0	High bits of desired frame sync margin in terms of PCLK cycles with respect to the VSYNC of the slowest link in automatic mode or with respect to the VSYNC of the main link in semi-automatic mode	0bXXXXX: High bits of desired frame sync margin

FSYNC_5 (0x4A5)

BIT	7	6	5	4	3	2	1	0
Field	FSYNC_PERIOD_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
FSYNC_PERIOD_L	7:0	Low byte of frame sync period in terms of pixel clock (effective when FSYNC_METH = 00 and FSYNC_MODE = 0x)	0xXX: Low byte of number of PLCK cycles in FSYNC period

FSYNC_6 (0x4A6)

BIT	7	6	5	4	3	2	1	0
Field	FSYNC_PERIOD_M[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
FSYNC_PERIOD_M	7:0	Middle byte of frame sync period in terms of pixel clock (effective when FSYNC_METH = 00 and FSYNC_MODE = 0x)	0xXX: Middle byte of number of PLCK cycles in FSYNC period

FSYNC_7 (0x4A7)

BIT	7	6	5	4	3	2	1	0
Field	FSYNC_PERIOD_H[7:0]							
Reset	0x00							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
FSYNC_PERIOD_H	7:0	High byte of frame sync period in terms of pixel clock (effective when FSYNC_METH = 00 and FSYNC_MODE = 0x)	0xXX: High byte of number of PLCK cycles in FSYNC period

FSYNC_8 (0x4A8)

BIT	7	6	5	4	3	2	1	0
Field	FRM_DIFF_ERR_THR_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
FRM_DIFF_ERR_THR_L	7:0	Low byte of the error threshold for the difference between the earliest and latest VSYNCs in terms of PCLK cycles (default is 40µs for 96MHz PCLK) (disabled when all 13 bits are 0's)	0xXX: Low byte of number of PLCK cycles in VSYNC error threshold

FSYNC_9 (0x4A9)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	FRM_DIFF_ERR_THR_H[4:0]				
Reset	–	–	–	0x0F				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
FRM_DIFF_ERR_THR_H	4:0	High bits of the error threshold for the difference between the earliest and latest VSYNCs in terms of PCLK cycles (default is 40µs for 96MHz PCLK) (disabled when all 13 bits are 0's)	0bXXXXX: High bits of number of PLCK cycles in VSYNC error threshold

FSYNC_10 (0x4AA)

BIT	7	6	5	4	3	2	1	0
Field	OVLP_WINDOW_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
OVLP_WINDOW_L	7:0	Low byte of the overlap window value in terms of PCLK cycles (default is 60µs for 96MHz PCLK) (disabled when all 13 bits are 0's)	0xXX: Low byte of number of PCLK cycles in the VSYNC-FSYNC overlap window

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FSYNC_11 (0x4AB)

BIT	7	6	5	4	3	2	1	0
Field	EN_FSIN_LAST	–	–	OVLP_WINDOW_H[4:0]				
Reset	0x0	–	–	0x00				
Access Type	Write, Read	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
EN_FSIN_LAST	7	When set to 0, FSIN can occur anywhere with respect to VS rising edges When set to 1, FSIN should occur after all VS rising edges	0b0: FSIN can occur anywhere with respect to VS rising edges 0b1: FSIN occurs after all rising edges
OVLP_WINDOW_H	4:0	High bits of the overlap window value in terms of PCLK cycles (default is 60µs for 96MHz PCLK) (disabled when all 13 bits are 0's)	0bXXXXX: High bits of number of PCLK cycles in the VSYNC-FSYNC overlap window

FSYNC_15 (0x4AF)

BIT	7	6	5	4	3	2	1	0
Field	FS_GPIO_TYPE	FS_USE_XTAL	–	AUTO_FS_LINKS	FS_LINK_3	FS_LINK_2	FS_LINK_1	FS_LINK_0
Reset	0x1	0x0	–	0x1	0x1	0x1	0x1	0x1
Access Type	Write, Read	Write, Read	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
FS_GPIO_TYPE	7	Selects the type of FSYNC signal to output from GPIO	0b0: GSML1 type 0b1: GMSL2 type
FS_USE_XTAL	6	Uses crystal oscillator clock for generating frame sync signal	0b0: Disabled 0b1: Enabled
AUTO_FS_LINKS	4	Selects how links are selected for frame sync generation	0b0: Include links selected by FS_LINK_x register bits in frame sync generation 0b1: Include all enabled links in frame sync generation
FS_LINK_3	3	Includes Video Pipe 3 in frame sync generation This is used only if AUTO_FS_LINKS = 0	0b0: Do not include Video Pipe 3 in frame sync generation 0b1: Include Video Pipe 3 in frame sync generation
FS_LINK_2	2	Includes Video Pipe 2 in frame sync generation This is used only if AUTO_FS_LINKS = 0	0b0: Do not include Video Pipe 2 in frame sync generation 0b1: Include Video Pipe 2 in frame sync generation
FS_LINK_1	1	Includes Video Pipe 1 in frame sync generation This is used only if AUTO_FS_LINKS = 0	0b0: Do not include Video Pipe 1 in frame sync generation 0b1: Include Video Pipe 1 in frame sync generation
FS_LINK_0	0	Includes Video Pipe 0 in frame sync generation This is used only if AUTO_FS_LINKS = 0	0b0: Do not include Video Pipe 0 in frame sync generation 0b1: Include Video Pipe 0 in frame sync generation

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FSYNC_16 (0x4B0)

BIT	7	6	5	4	3	2	1	0
Field	FSYNC_ERR_CNT[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
FSYNC_ERR_CNT	7:0	Frame Sync Error Counter (resets to 0 when read or when FSYNC_LOCKED (0x4b6) goes high)	0xXX: Number of frame sync errors detected since last error counter reset

FSYNC_17 (0x4B1)

BIT	7	6	5	4	3	2	1	0
Field	FSYNC_TX_ID[4:0]					FSYNC_ERR_THR[2:0]		
Reset	0x1E					0x0		
Access Type	Write, Read					Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
FSYNC_TX_ID	7:3	GPIO ID used for transmitting FSYNC signal	0bXXXXX: GPIO ID associated with FSYNC transmission
FSYNC_ERR_THR	2:0	Frame sync error reporting threshold. FSYNC_ERR_FLAG is asserted when FSYNC_ERR_CNT ≥ FSYNC_ERR_THR.	0b000: 1 error 0b001: 2 errors 0b010: 4 errors 0b011: 8 errors 0b100: 16 errors 0b101: 32 errors 0b110: 64 errors 0b111: 128 errors

FSYNC_18 (0x4B2)

BIT	7	6	5	4	3	2	1	0
Field	CALC_FRM_LEN_L[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
CALC_FRM_LEN_L	7:0	Low byte of calculated VS period of main link in terms of pixel clock in automatic or semi-automatic synchronization mode (Use when FSYNC_METH = 10 and FSYNC_MODE = 0x)	0xXX: Low byte of number of PCLKs in VS period in main link auto or semi-auto synchronization mode.

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FSYNC_19 (0x4B3)

BIT	7	6	5	4	3	2	1	0
Field	CALC_FRM_LEN_M[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
CALC_FRM_LEN_M	7:0	Middle byte of calculated VS period of main link in terms of pixel clock in automatic or semi-automatic synchronization mode (Use when FSYNC_METH = 10 and FSYNC_MODE = 0x)	0xXX: Middle byte of number of PCLKs in VS period in main link auto or semi-auto synchronization mode

FSYNC_20 (0x4B4)

BIT	7	6	5	4	3	2	1	0
Field	CALC_FRM_LEN_H[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
CALC_FRM_LEN_H	7:0	High byte of calculated VS period of main link in terms of pixel clock in automatic or semi-automatic synchronization mode (Use when FSYNC_METH = 10 and FSYNC_MODE = 0x)	0xXX: High byte of number of PCLKs in VS period in main link auto or semi-auto synchronization mode

FSYNC_21 (0x4B5)

BIT	7	6	5	4	3	2	1	0
Field	FRM_DIFF_L[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
FRM_DIFF_L	7:0	Low byte of the difference between the fastest and the slowest frame in terms of main PCLK cycles	0xXX: Low byte of the difference between the fastest and the slowest frame

FSYNC_22 (0x4B6)

BIT	7	6	5	4	3	2	1	0
Field	FSYNC_LOSS_OF_LOCK	FSYNC_LOCKED	FRM_DIFF_H[5:0]					
Reset	0x0	0x0	0x00					
Access Type	Read Clears All	Read Only	Read Only					

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BITFIELD	BITS	DESCRIPTION	DECODE
FSYNC_LOSS_OF_LOCK	7	Frame Synchronization Lost Lock This bit is set to 1 when frame synchronization loses lock, it is cleared when read.	0b0: Frame synchronization loss of lock has not been detected or has been cleared by a previous read operation 0b1: Frame synchronization loss of lock has been detected
FSYNC_LOCKED	6	Frame Synchronization Lock	0b0: Frame synchronization is not locked 0b1: Frame synchronization is locked
FRM_DIFF_H	5:0	High bits of the difference between the fastest and the slowest frame in terms of main PCLK cycles	0bXXXXX: High bits of the difference between the fastest and the slowest frame

FSYNC_23 (0x4B7)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	–	–	RSVD	RSVD	RSVD	RSVD
Reset	0x0	0x0	–	–	0x0	0x0	0x0	0x0
Access Type			–	–				

SPI_0 (0x4E0)

BIT	7	6	5	4	3	2	1	0
Field	SPI_LOC_ID[1:0]		SPI_CC_TRG_ID[1:0]		SPI_IGNR_ID	SPI_CC_EN	MST_SLVN	SPI_EN
Reset	0x0		0x0		0x1	0x0	0x0	0x0
Access Type	Write, Read		Write, Read		Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SPI_LOC_ID	7:6	Program to local ID if packets are filtered based on header ID.	0bXX: Program to local ID
SPI_CC_TRG_ID	5:4	ID for GMSL2 header when in SPI CC bridge mode	0bXX: ID for GMSL2 header
SPI_IGNR_ID	3	Indicates whether to accept all packets regardless of header ID	0b0: Accept only packets with designated ID 0b1: Accept all packets regardless of header ID
SPI_CC_EN	2	Enables CC to SPI bridge function	0b0: Disable CC to SPI bridge function 0b1: Enable CC to SPI bridge function
MST_SLVN	1	Selects whether this chip is SPI main or SPI subordinate	0b0: Chip is on the near side of the GMSL2 link (near the µC), internal SPI subordinate is enabled 0b1: Chip is on the far side of the GMSL2 link (away from the µC), internal SPI main is enabled
SPI_EN	0	Enables SPI channel	0b0: Disable SPI channel 0b1: Enable SPI channel

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SPI_1 (0x4E1)

BIT	7	6	5	4	3	2	1	0
Field	SPI_LOC_N[5:0]						RSVD[1:0]	
Reset	0x07						0x1	
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SPI_LOC_N	7:2	Maximum packet size ((2N + 1) bytes) for GMSL2 SPI packets. If this is programmed to a value more than 7, ARQ of the SPI channel must be disabled.	0b000000: Packet size is 1 byte 0b000001: Packet size is 3 bytes . . . 0b111110: Packet size is 125 bytes 0b111111: Packet size is 127 bytes

SPI_2 (0x4E2)

BIT	7	6	5	4	3	2	1	0
Field	REQ_HOLD_OFF[2:0]			FULL_SCK_SETUP	SPI_MOD3_F	SPI_MOD3	SPIM_SS2_ACT_H	SPIM_SS1_ACT_H
Reset	0x0			0x0	0x0	0x0	0x1	0x1
Access Type	Write, Read			Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
REQ_HOLD_OFF	7:5	Holds off GMSL2 request until this number of extra bytes are received on SPI port.	0bXXX: Number of extra bytes received on SPI port
FULL_SCK_SETUP	4	Samples MISO after full SCK period, rather than only half SCK period as per defacto spec	0b0: Sample MISO after half SCK period 0b1: Sample MISO after full SCK period
SPI_MOD3_F	3	Suppresses extra SCK prior to SS deassertion	0b0: Do not suppress extra SCK prior to SS deassertion 0b1: Suppress extra SCK prior to SS deassertion
SPI_MOD3	2	Enables SPI mode 3	0b0: Disable SPI mode 3 0b1: Enable SPI mode 3
SPIM_SS2_ACT_H	1	Subordinate Select 2 (SS2) polarity	0b0: Active low 0b1: Active high
SPIM_SS1_ACT_H	0	Subordinate Select 1 (SS1) polarity	0b0: Active low 0b1: Active high

SPI_3 (0x4E3)

BIT	7	6	5	4	3	2	1	0
Field	SPIM_SS_DLY_CLKS[7:0]							
Reset	0x00							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
SPIM_SS_DLY_CLKS	7:0	Number of 300MHz clocks to delay between: 1. Assertion of SS and start of SCK pulses 2. End of SCK pulses and deassertion of SS 3. Deassertion of SS and reassertion of SS (if necessary)	0xXX: Number of clocks delays

SPI_4 (0x4E4)

BIT	7	6	5	4	3	2	1	0
Field	SPIM_SCK_LO_CLKS[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SPIM_SCK_LO_CLKS	7:0	Number of 300MHz clocks for SCK low time	0xXX: Number of clocks for SCK low time

SPI_5 (0x4E5)

BIT	7	6	5	4	3	2	1	0
Field	SPIM_SCK_HI_CLKS[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SPIM_SCK_HI_CLKS	7:0	Number of 300MHz clocks for SCK high time	0xXX: Number of clocks for SCK high time

SPI_6 (0x4E6)

BIT	7	6	5	4	3	2	1	0
Field	–	–	BNE	SPIS_RWN	SS_IO_EN_2	SS_IO_EN_1	BNE_IO_EN	RWN_IO_EN
Reset	–	–	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	–	–	Read Only	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
BNE	5	BNE indicates the buffer not empty status.	0b0: Buffer is empty 0b1: Buffer is not empty
SPIS_RWN	4	Works in conjunction with RWN_IO_EN (Bit 0, this register) to act as a Rd/WrN control when GPIO is not available for that purpose. When RWN_IO_EN is set to 1 (GPIO enabled), SPIS_RWN is ignored. When RWN_IO_EN is set to 0 (GPIO disabled), SPIS_RWN indicates either a read or a write function.	0b0: Write 0b1: Read

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BITFIELD	BITS	DESCRIPTION	DECODE
SS_IO_EN_2	3	Enables GPIO for use as Subordinate Select 2 output	0b0: Disable GPIO for use as Subordinate Select 2 output 0b1: Enable GPIO for use as Subordinate Select 2 output
SS_IO_EN_1	2	Enables GPIO for use as Subordinate Select 1 output	0b0: Disable GPIO for use as Subordinate Select 1 output 0b1: Enable GPIO for use as Subordinate Select 1 output
BNE_IO_EN	1	Enables GPIO for use as Rx buffer not empty output for SPI data available status	0b0: Disable GPIO for use as Rx buffer not empty output 0b1: Enable GPIO for use as Rx buffer not empty output
RWN_IO_EN	0	Enables GPIO for use as Rd/WrN input for control of SPI data movement. See description of SPIS_RWN (bit 4, this register) for alternative when GPIO is disabled.	0b0: Disable GPIO for use as Rd/WrN input 0b1: Enable GPIO for use as Rd/WrN input

SPI_7 (0x4E7)

BIT	7	6	5	4	3	2	1	0
Field	SPI_RX_OVRFLW	SPI_TX_OVRFLW	–	SPIS_BYTE_CNT[4:0]				
Reset	0b0	0b0	–	0x0				
Access Type	Read Clears All	Read Clears All	–	Read Only				

BITFIELD	BITS	DESCRIPTION	DECODE
SPI_RX_OVRFLW	7	Status flag indicating buffer overflow was detected on GMSL2 Rx buffer.	0b0: No buffer overflow detected 0b1: Buffer overflow detected
SPI_TX_OVRFLW	6	Status flag indicating buffer overflow was detected on GMSL2 Tx buffer	0b0: No buffer overflow detected 0b1: Buffer overflow detected
SPIS_BYTE_CNT	4:0	Number of SPI data bytes available for reading from Rx buffer.	0bXXXXX: Number of SPI data bytes available for reading from Rx buffer

SPI_8 (0x4E8)

BIT	7	6	5	4	3	2	1	0
Field	REQ_HOLD_OFF_TO[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
REQ_HOLD_OFF_TO	7:0	Timeout delay (in 100nS increments) for GMSL2 request hold off (0 is disable).	0xXX: Number of 100nS delay increments for GMSL2 request hold off

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SPI_9 (0x4E9)

BIT		1	0
Field		SPI_0_LINK_SELECT[1:0]	
Reset		0x00	
Access Type		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
SPI_0_LINK_SELECT	1:0	Selects link connection for SPI Port 0	0b00: Selects GMSL2 Link A 0b01: Selects GMSL2 Link B 0b10: Selects GMSL2 Link C 0b11: Selects GMSL2 Link D

SPI_0 (0x4F0)

BIT	7	6	5	4	3	2	1	0
Field	SPI_LOC_ID_1[1:0]		SPI_CC_TRG_ID_1[1:0]		SPI_IGNR_ID_1	SPI_CC_EN_1	MST_SLVN_1	SPI_EN_1
Reset	0x0		0x0		0x1	0x0	0x0	0x0
Access Type	Write, Read		Write, Read		Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SPI_LOC_ID_1	7:6	Programs to local ID if packets are to be filtered based on the header ID.	0bXX: Program to local ID
SPI_CC_TRG_ID_1	5:4	ID for GMSL2 header when in SPI CC bridge mode	0bXX: GMSL2 header ID
SPI_IGNR_ID_1	3	Indicates whether all packets are to be accepted regardless of header ID.	0b0: Accept only packets with designated ID 0b1: Accept all packets regardless of ID
SPI_CC_EN_1	2	Enables CC to SPI bridge function	0b0: CC to SPI bridge function disabled 0b1: CC to SPI bridge function enabled
MST_SLVN_1	1	Selects whether this chip is SPI main or SPI subordinate	0b0: Chip is on the near side of the GMSL2 link (near the µC), internal SPI subordinate is enabled 0b1: Chip is on the far side of the GMSL2 link (away from the µC), internal SPI main is enabled
SPI_EN_1	0	Enables SPI channel	0b0: Disable SPI channel 0b1: Enable SPI channel

SPI_1 (0x4F1)

BIT	7	6	5	4	3	2	1	0
Field	SPI_LOC_N_1[5:0]						RSVD[1:0]	
Reset	0x07						0x1	
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
SPI_LOC_N_1	7:2	Maximum packet size ((2N + 1) bytes) for GMSL2 SPI packets. If this is programmed to a value more than 7, ARQ of the SPI channel must be disabled.	0b000000: Packet size is 1 byte 0b000001: Packet size is 3 bytes . . . 0b111110: Packet size is 125 bytes 0b111111: Packet size is 127 bytes

SPI_2 (0x4F2)

BIT	7	6	5	4	3	2	1	0
Field	REQ_HOLD_OFF_1[2:0]			FULL_SCK_SETUP_1	SPI_MOD3_F_1	SPI_MOD3_1	SPIM_SS2_ACT_H_1	SPIM_SS1_ACT_H_1
Reset	0x0			0x0	0x0	0x0	0x1	0x1
Access Type	Write, Read			Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
REQ_HOLD_OFF_1	7:5	Holds off GMSL2 request until this number of extra bytes are received on SPI port.	0bXX: Number of extra bytes received on SPI port
FULL_SCK_SETUP_1	4	Samples MISO after full SCK period, rather than only half SCK period as per defacto spec	0b0: Sample MISO after half SCK period 0b1: Sample MISO after full SCK period
SPI_MOD3_F_1	3	Suppresses extra SCK prior to SS deassertion	0b0: Do not suppress extra SCK prior to SS deassertion 0b1: Suppress extra SCK prior to SS deassertion
SPI_MOD3_1	2	Enables SPI mode 3	0b0: Disable SPI mode 3 0b1: Enable SPI mode 3
SPIM_SS2_ACT_H_1	1	Subordinate Select 2 (SS2) polarity	0b0: Active low 0b1: Active high
SPIM_SS1_ACT_H_1	0	Subordinate Select 1 (SS1) polarity	0b0: Active low 0b1: Active high

SPI_3 (0x4F3)

BIT	7	6	5	4	3	2	1	0
Field	SPIM_SS_DLY_CLKS_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SPIM_SS_DLY_CLKS_1	7:0	Number of 300MHz clocks to delay between: 1. Assertion of SS and start of SCK pulses 2. End of SCK pulses and deassertion of SS 3. Deassertion of SS and reassertion of SS (if necessary)	0xXX: Number of clocks delays

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SPI_4 (0x4F4)

BIT	7	6	5	4	3	2	1	0
Field	SPIM_SCK_LO_CLKS_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SPIM_SCK_LO_CLKS_1	7:0	Number of 300MHz clocks for SCK low time	0xXX: Number of clocks for SCK low time

SPI_5 (0x4F5)

BIT	7	6	5	4	3	2	1	0
Field	SPIM_SCK_HI_CLKS_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SPIM_SCK_HI_CLKS_1	7:0	Number of 300MHz clocks for SCK high time	0xXX: Number of clocks for SCK high time

SPI_6 (0x4F6)

BIT	7	6	5	4	3	2	1	0
Field	–	–	BNE_1	SPIS_RWN_1	SS_IO_EN_2_1	SS_IO_EN_1_1	BNE_IO_EN_1	RWN_IO_EN_1
Reset	–	–	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	–	–	Read Only	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
BNE_1	5	BNE_1 indicates the buffer not empty status.	0b0: Buffer is empty 0b1: Buffer is not empty
SPIS_RWN_1	4	Works in conjunction with RWN_IO_EN_1 (Bit 0, this register) to act as a Rd/WrN control when GPIO is not available for that purpose. When RWN_IO_EN is set to 1 (GPIO enabled), SPIS_RWN is ignored. When RWN_IO_EN is set to 0 (GPIO disabled), SPIS_RWN indicates either a read or a write function.	0b0: Write 0b1: Read
SS_IO_EN_2_1	3	Enables GPIO for use as subordinate select 2 output	0b0: Disable GPIO for use as subordinate select 2 output 0b1: Enable GPIO for use as subordinate select 2 output
SS_IO_EN_1_1	2	Enables GPIO for use as subordinate select 1 output	0b0: Disable GPIO for use as subordinate select 1 output 0b1: Enable GPIO for use as subordinate select 1 output

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BITFIELD	BITS	DESCRIPTION	DECODE
BNE_IO_EN_1	1	Enables GPIO for use as Rx buffer not empty output for SPI data available status	0b0: Disable GPIO for use as Rx buffer not empty output 0b1: Enable GPIO for use as Rx buffer not empty output
RWN_IO_EN_1	0	Enables GPIO for use as Rd/WrN input for control of SPI data movement control. See description of SPIS_RWN_1 (bit 4, this register) for alternative when GPIO is disabled.	0b0: Disable GPIO for use as Rd/WrN input 0b1: Enable GPIO for use as Rd/WrN input

SPI_7 (0x4F7)

BIT	7	6	5	4	3	2	1	0
Field	SPI_RX_OVRFLW_1	SPI_TX_OVRFLW_1	–	SPIS_BYTE_CNT_1[4:0]				
Reset	0b0	0b0	–	0x0				
Access Type	Read Clears All	Read Clears All	–	Read Only				

BITFIELD	BITS	DESCRIPTION	DECODE
SPI_RX_OVRFLW_1	7	Status flag indicating buffer overflow was detected on GMSL2 Rx buffer.	0b0: No buffer overflow detected 0b1: Buffer overflow detected
SPI_TX_OVRFLW_1	6	Status flag indicating buffer overflow was detected on GMSL2 Tx buffer	0b0: No buffer overflow detected 0b1: Buffer overflow detected
SPIS_BYTE_CNT_1	4:0	Number of SPI data bytes available for reading from Rx buffer.	0bXXXXX: Number of SPI data bytes available for reading from Rx buffer

SPI_8 (0x4F8)

BIT	7	6	5	4	3	2	1	0
Field	REQ_HOLD_OFF_TO_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
REQ_HOLD_OFF_TO_1	7:0	Timeout delay (in 100nS increments) for GMSL2 request hold off (0 is disable).	0xXX: Number of 100nS delay increments for GMSL2 request hold off

SPI_9 (0x4F9)

BIT		1	0
Field		SPI_1_LINK_SELECT[1:0]	
Reset		0x01	
Access Type		Write, Read	

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BITFIELD	BITS	DESCRIPTION	DECODE
SPI_1_LINK_SELECT	1:0	Selects link connection for SPI Port 1	0b00: Selects GMSL2 link A 0b01: Selects GMSL2 link B 0b10: Selects GMSL2 link C 0b11: Selects GMSL2 link D

TR0 (0x500, 0x560)

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
Reset	0b1	0b1	0x3		0x0		0x0	
Access Type	Write, Read	Write, Read			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN	7	When set, calculates and appends CRC to each packet transmitted from this port	0b0: Do not calculate and append CRC to each packet 0b1: Calculate and append CRC to each packet
RX_CRC_EN	6	When set, indicates that packets received at this port have appended CRC, and CRC checking should be performed at each packet.	0b0: Do not perform CRC check at each packet 0b1: Perform CRC check at each packet
PRIO_VAL	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG	1:0	Adjusts the priority to be used for requests from this channel	0b00: Priority from Tx adapter is used 0b01: Priority from Tx adapter is increased 0b10: Priority from Tx adapter is decreased 0b11: Priority in PRIO_VAL register is used

TR1 (0x501, 0x561)

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT[1:0]		BW_VAL[5:0]					
Reset	0x2		0x30					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT	7:6	Channel bandwidth-allocation multiplication factor	0b00: Multiply BW_VAL by 1 0b01: Multiply BW_VAL by 4 0b10: Multiply BW_VAL by 16 0b11: Multiply BW_VAL by 16
BW_VAL	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL x BW_MULT/10 as a percentage of total link bandwidth	0bXXXXXX: Channel base-bandwidth value

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TR3 (0x503, 0x563)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TX_SRC_ID[2:0]		
Reset	–	–	–	–	–	0x0		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID	2:0	Source identifier used in packets transmitted from this port. Default value is set by CFG0 pin.	0bXXX: Source ID for packets from this channel

TR4 (0x504, 0x564)

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL	7:0	Receives packets from selected sources Each bit indicates whether packets with that source ID should be received or not. For example, when RX_SRC_SEL = 00001001, then packets with source ID equal to 0 and 3 will be received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received . . . 0xFF: Packets from all source IDs received

ARQ0 (0x505, 0x565)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	RSVD	RSVD	RSVD	DIS_DBL_ACK_RETX	–	–
Reset	–	0b0	0b0	0b1	0b1	0b0	–	–
Access Type	–					Write, Read	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
DIS_DBL_ACK_RETX	2	Disables retransmission due to receiving same ACK twice	0b0: Enabled 0b1: Disabled

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ARQ1 (0x506, 0x566)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
Reset	–	0x7			–	–	0b1	0b0
Access Type	–				–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR_OEN	1	Enables reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR—ARQ2 register) for this channel at ERRB pin	0b0: Disable reporting of ARQ maximum retransmission limit errors 0b1: Enable reporting of ARQ maximum retransmission limit errors
RT_CNT_OEN	0	Enables reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT of this channel is greater than 0.	0b0: Disable reporting of ARQ retransmission event 0b1: Enable reporting of ARQ retransmission event

ARQ2 (0x507, 0x567)

BIT	7	6	5	4	3	2	1	0
Field	MAX_RT_ERR	RT_CNT[6:0]						
Reset	0b0	0x0						
Access Type	Read Clears All	Read Clears All						

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR	7	Reached maximum retransmit limit (MAX_RT—ARQ1) for one packet in this channel	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT	6:0	Total retransmission count in this channel	0bXXXXXXX: Count of retransmission for this channel

TR0 (0x510)

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN_B	RX_CRC_EN_B	RSVD[1:0]		PRIO_VAL_B[1:0]		PRIO_CFG_B[1:0]	
Reset	0b1	0b1	0x3		0x0		0x0	
Access Type	Write, Read	Write, Read			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN_B	7	When set, calculates and appends CRC to each packet transmitted from this port	0b0: Do not calculate and append CRC to each packet 0b1: Calculate and append CRC to each packet
RX_CRC_EN_B	6	When set, indicates that packets received at this port have appended CRC, and CRC checking should be performed at each packet.	0b0: Do not perform CRC check at each packet 0b1: Perform CRC check at each packet

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BITFIELD	BITS	DESCRIPTION	DECODE
PRIO_VAL_B	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG_B	1:0	Adjusts the priority to be used for requests from this channel	00: Priority from Tx adapter is used 01: Priority from Tx adapter is increased 10: Priority from Tx adapter is decreased 11: Priority in PRIO_VAL register is used

TR1 (0x511)

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT_B[1:0]		BW_VAL_B[5:0]					
Reset	0x2		0x30					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT_B	7:6	Channel bandwidth-allocation multiplication factor	0b00: Multiply BW_VAL_B by 1 0b01: Multiply BW_VAL_B by 4 0b10: Multiply BW_VAL_B by 16 0b11: Multiply BW_VAL_B by 16
BW_VAL_B	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL_B x BW_MULT_B/10 as a percentage of total link bandwidth	0bXXXXXX: Channel base-bandwidth value

TR3 (0x513)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TX_SRC_ID_B[2:0]		
Reset	–	–	–	–	–	0x0		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID_B	2:0	Source identifier used in packets transmitted from this port. Default value is set by CFG0 pin.	0bXXX: Source ID for packets from this channel

TR4 (0x514)

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL_B[7:0]							
Reset	0xFF							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL_B	7:0	Received Packets from Selected Sources Each bit indicates whether packets with that source ID should be received or not. For example, when RX_SRC_SEL_B = 00001001, then packets with source ID equal to 0 and 3 will be received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received . . . 0xFF: Packets from all source IDs received

ARQ0 (0x515)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	RSVD	RSVD	RSVD	DIS_DBL_ACK_RETX_B	–	–
Reset	–	0b0	0b0	0b1	0b1	0b0	–	–
Access Type	–					Write, Read	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
DIS_DBL_ACK_RETX_B	2	Disables retransmission due to receiving same ACK twice	0b0: Enabled 0b1: Disabled

ARQ1 (0x516)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD[2:0]			–	–	MAX_RT_ERR_OEN_B	RT_CNT_OEN_B
Reset	–	0x7			–	–	0b1	0b0
Access Type	–				–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR_OEN_B	1	Enables reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR_B—0x517) for this channel at ERRB pin	0b0: Disable reporting of ARQ maximum retransmission limit errors 0b1: Enable reporting of ARQ maximum retransmission limit errors
RT_CNT_OEN_B	0	Enables reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT_B—0x517 of this channel is greater than 0.	0b0: Disable reporting of ARQ retransmission event 0b1: Enable reporting of ARQ retransmission event

ARQ2 (0x517)

BIT	7	6	5	4	3	2	1	0
Field	MAX_RT_ERR_B	RT_CNT_B[6:0]						
Reset	0b0	0x0						
Access Type	Read Clears All	Read Clears All						

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BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR_B	7	Reached maximum retransmit limit (MAX_RT_B—(0x516) for one packet in this channel	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT_B	6:0	Total retransmission count in this channel	0bXXXXXXX: Count of retransmission for this channel

TR0 (0x520)

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN_C	RX_CRC_EN_C	RSVD[1:0]		PRIO_VAL_C[1:0]		PRIO_CFG_C[1:0]	
Reset	0b1	0b1	0x3		0x0		0x0	
Access Type	Write, Read	Write, Read			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN_C	7	When set, calculates and appends CRC to each packet transmitted from this port	0b0: Do not calculate and append CRC to each packet 0b1: Calculate and append CRC to each packet
RX_CRC_EN_C	6	When set, indicates that packets received at this port have appended CRC, and CRC checking should be performed at each packet.	0b0: Do not perform CRC check at each packet 0b1: Perform CRC check at each packet
PRIO_VAL_C	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG_C	1:0	Adjusts the priority to be used for requests from this channel	0b00: Priority from Tx adapter is used 0b01: Priority from Tx adapter is increased 0b10: Priority from Tx adapter is decreased 0b11: Priority in PRIO_VAL register is used

TR1 (0x521)

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT_C[1:0]		BW_VAL_C[5:0]					
Reset	0x2		0x30					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT_C	7:6	Channel bandwidth-allocation multiplication factor	0b00: Multiply BW_VAL_C by 1 0b01: Multiply BW_VAL_C by 4 0b10: Multiply BW_VAL_C by 16 0b11: Multiply BW_VAL_C by 16
BW_VAL_C	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL_C x BW_MULT_C/10 as a percentage of total link bandwidth	0bXXXXXX: Channel base-bandwidth value

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TR3 (0x523)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TX_SRC_ID_C[2:0]		
Reset	–	–	–	–	–	0x0		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID_C	2:0	Source identifier used in packets transmitted from this port. Default value is set by CFG0 pin.	0bXXX: Source ID for packets from this channel

TR4 (0x524)

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL_C[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL_C	7:0	Received packets from selected sources Each bit indicates whether packets with that source ID should be received or not. For example, when RX_SRC_SEL_C = 00001001, then packets with source ID equal to 0 and 3 will be received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received . . . 0xFF: Packets from all source IDs received

ARQ0 (0x525)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	RSVD	RSVD	RSVD	DIS_DBL_ACK_RETX_C	–	–
Reset	–	0b0	0b0	0b1	0b1	0b0	–	–
Access Type	–					Write, Read	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
DIS_DBL_ACK_RETX_C	2	Disables retransmission due to receiving same ACK twice	0b0: Enabled 0b1: Disabled

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ARQ1 (0x526)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD[2:0]			–	–	MAX_RT_ERR_OEN_C	RT_CNT_OEN_C
Reset	–	0x7			–	–	0b1	0b0
Access Type	–				–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR_OEN_C	1	Enables reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR_C—0x527) for this channel at ERRB pin	0b0: Disable reporting of ARQ maximum retransmission limit errors 0b1: Enable reporting of ARQ maximum retransmission limit errors
RT_CNT_OEN_C	0	Enables reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT_C (0x527) of this channel is greater than 0.	0b0: Disable reporting of ARQ retransmission event 0b1: Enable reporting of ARQ retransmission event

ARQ2 (0x527)

BIT	7	6	5	4	3	2	1	0
Field	MAX_RT_ERR_C	RT_CNT_C[6:0]						
Reset	0b0	0x0						
Access Type	Read Clears All	Read Clears All						

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR_C	7	Reached maximum retransmit limit (MAX_RT_C—0x526) for one packet in this channel	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT_C	6:0	Total retransmission count in this channel	0bXXXXXXX: Count of retransmission for this channel

TR0 (0x530)

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN_D	RX_CRC_EN_D	RSVD[1:0]		PRIO_VAL_D[1:0]		PRIO_CFG_D[1:0]	
Reset	0b1	0b1	0x3		0x0		0x0	
Access Type	Write, Read	Write, Read			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN_D	7	When set, calculates and appends CRC to each packet transmitted from this port	0b0: Do not calculate and append CRC to each packet 0b1: Calculate and append CRC to each packet
RX_CRC_EN_D	6	When set, indicates that packets received at this port have appended CRC, and CRC checking should be performed at each packet.	0b0: Do not perform CRC check at each packet 0b1: Perform CRC check at each packet

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BITFIELD	BITS	DESCRIPTION	DECODE
PRIO_VAL_D	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG_D	1:0	Adjusts the priority to be used for requests from this channel	0b00: Priority from Tx adapter is used 0b01: Priority from Tx adapter is increased 0b10: Priority from Tx adapter is decreased 0b11: Priority in PRIO_VAL register is used

TR1 (0x531)

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT_D[1:0]		BW_VAL_D[5:0]					
Reset	0x2		0x30					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT_D	7:6	Channel bandwidth-allocation multiplication factor	0b00: Multiply BW_VAL_D by 1 0b01: Multiply BW_VAL_D by 4 0b10: Multiply BW_VAL_D by 16 0b11: Multiply BW_VAL_D by 16
BW_VAL_D	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL_D x BW_MULT_D/10 as a percentage of total link bandwidth	0bXXXXXX: Channel base-bandwidth value

TR3 (0x533)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TX_SRC_ID_D[2:0]		
Reset	–	–	–	–	–	0x0		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID_D	2:0	Source identifier used in packets transmitted from this port. Default value is set by CFG0 pin.	0bXXX: Source ID for packets from this channel

TR4 (0x534)

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL_D[7:0]							
Reset	0xFF							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL_D	7:0	Received packets from selected sources Each bit indicates whether packets with that source ID should be received or not. For example, when RX_SRC_SEL_D = 00001001, then packets with source ID equal to 0 and 3 will be received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received . . . 0xFF: Packets from all source IDs received

ARQ0 (0x535)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	RSVD	RSVD	RSVD	DIS_DBL_ACK_RETX_D	–	–
Reset	–	0b0	0b0	0b1	0b1	0b0	–	–
Access Type	–					Write, Read	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
DIS_DBL_ACK_RETX_D	2	Disables retransmission due to receiving same ACK twice	0b0: Enabled 0b1: Disabled

ARQ1 (0x536)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD[2:0]			–	–	MAX_RT_ERR_OEN_D	RT_CNT_OEN_D
Reset	–	0x7			–	–	0b1	0b0
Access Type	–				–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR_OEN_D	1	Enables reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR_D—0x537) for this channel at ERRB pin	0b0: Disable reporting of ARQ maximum retransmission limit errors 0b1: Enable reporting of ARQ maximum retransmission limit errors
RT_CNT_OEN_D	0	Enables reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT_D (0x537) of this channel is greater than 0.	0b0: Disable reporting of ARQ retransmission event 0b1: Enable reporting of ARQ retransmission event

ARQ2 (0x537)

BIT	7	6	5	4	3	2	1	0
Field	MAX_RT_ERR_D	RT_CNT_D[6:0]						
Reset	0b0	0x0						
Access Type	Read Clears All	Read Clears All						

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BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR_D	7	Reached maximum retransmit limit (MAX_RT_D—0x536) for one packet in this channel	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT_D	6:0	Total retransmission count in this channel	0bXXXXXXX: Count of retransmission for this channel

TR0 (0x570)

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN_B	RX_CRC_EN_B	RSVD[1:0]		PRIO_VAL_B[1:0]		PRIO_CFG_B[1:0]	
Reset	0b1	0b1	0x3		0x0		0x0	
Access Type	Write, Read	Write, Read			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN_B	7	When set, calculates and appends CRC to each packet transmitted from this port	0b0: Do not calculate and append CRC to each packet 0b1: Calculate and append CRC to each packet
RX_CRC_EN_B	6	When set, indicates that packets received at this port have appended CRC, and CRC checking should be performed at each packet.	0b0: Do not perform CRC check at each packet 0b1: Perform CRC check at each packet
PRIO_VAL_B	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG_B	1:0	Adjust the priority to be used for requests from this channel	0b00: Priority from Tx adapter is used 0b01: Priority from Tx adapter is increased 0b10: Priority from Tx adapter is decreased 0b11: Priority in PRIO_VAL register is used

TR1 (0x571)

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT_B[1:0]		BW_VAL_B[5:0]					
Reset	0x2		0x30					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT_B	7:6	Channel bandwidth-allocation multiplication factor	0b00: Multiply BW_VAL_B by 1 0b01: Multiply BW_VAL_B by 4 0b10: Multiply BW_VAL_B by 16 0b11: Multiply BW_VAL_B by 16
BW_VAL_B	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL_B x BW_MULT_B/10 as a percentage of total link bandwidth	0bXXXXXX: Channel base-bandwidth value

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TR3 (0x573)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TX_SRC_ID_B[2:0]		
Reset	–	–	–	–	–	0x0		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID_B	2:0	Source identifier used in packets transmitted from this port. Default value is set by CFG0 pin.	0bXXX: Source ID for packets from this channel

TR4 (0x574)

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL_B[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL_B	7:0	Receives packets from selected sources Each bit indicates whether packets with that source ID should be received or not. For example, when RX_SRC_SEL_B = 00001001, then packets with source ID equal to 0 and 3 will be received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received . . . 0xFF: Packets from all source IDs received

ARQ0 (0x575)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	RSVD	RSVD	RSVD	DIS_DBL_ACK_RETX_B	–	–
Reset	–	0b0	0b0	0b1	0b1	0b0	–	–
Access Type	–					Write, Read	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
DIS_DBL_ACK_RETX_B	2	Disables retransmission due to receiving same ACK twice	0b0: Enabled 0b1: Disabled

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ARQ1 (0x576)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD[2:0]			–	–	MAX_RT_ERR_OEN_B	RT_CNT_OEN_B
Reset	–	0x7			–	–	0b1	0b0
Access Type	–				–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR_OEN_B	1	Enables reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR—0x577) for this channel at ERRB pin	0b0: Disable reporting of ARQ maximum retransmission limit errors 0b1: Enable reporting of ARQ maximum retransmission limit errors
RT_CNT_OEN_B	0	Enables reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT (0x577) of this channel is greater than 0.	0b0: Disable reporting of ARQ retransmission event 0b1: Enable reporting of ARQ retransmission event

ARQ2 (0x577)

BIT	7	6	5	4	3	2	1	0
Field	MAX_RT_ERR_B	RT_CNT_B[6:0]						
Reset	0b0	0x0						
Access Type	Read Clears All	Read Clears All						

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR_B	7	Reached maximum retransmit limit (MAX_RT_B—0x576) for one packet in this channel	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT_B	6:0	Total retransmission count in this channel	0bXXXXXXX: Count of retransmission for this channel

TR0 (0x580)

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN_C	RX_CRC_EN_C	RSVD[1:0]		PRIO_VAL_C[1:0]		PRIO_CFG_C[1:0]	
Reset	0b1	0b1	0x3		0x0		0x0	
Access Type	Write, Read	Write, Read			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN_C	7	When set, calculate and append CRC to each packet transmitted from this port	0b0: Do not calculate and append CRC to each packet 0b1: Calculate and append CRC to each packet
RX_CRC_EN_C	6	When set, indicates that packets received at this port have appended CRC, and CRC checking should be performed at each packet.	0b0: Do not perform CRC check at each packet 0b1: Perform CRC check at each packet

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BITFIELD	BITS	DESCRIPTION	DECODE
PRIO_VAL_C	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG_C	1:0	Adjust the priority to be used for requests from this channel	0b00: Priority from Tx adapter is used 0b01: Priority from Tx adapter is increased 0b10: Priority from Tx adapter is decreased 0b11: Priority in PRIO_VAL register is used

TR1 (0x581)

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT_C[1:0]		BW_VAL_C[5:0]					
Reset	0x2		0x30					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT_C	7:6	Channel bandwidth-allocation multiplication factor	0b00: Multiply BW_VAL_C by 1 0b01: Multiply BW_VAL_C by 4 0b10: Multiply BW_VAL_C by 16 0b11: Multiply BW_VAL_C by 16
BW_VAL_C	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL_C x BW_MULT_C/10 as a percentage of total link bandwidth	0bXXXXXX: Channel base-bandwidth value

TR3 (0x583)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TX_SRC_ID_C[2:0]		
Reset	–	–	–	–	–	0x0		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID_C	2:0	Source identifier used in packets transmitted from this port. Default value is set by CFG0 pin.	0bXXX: Source ID for packets from this channel

TR4 (0x584)

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL_C[7:0]							
Reset	0xFF							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL_C	7:0	Receive packets from selected sources Each bit indicates whether packets with that source ID should be received or not. For example, when RX_SRC_SEL_C = 00001001, then packets with source ID equal to 0 and 3 will be received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received . . . 0xFF: Packets from all source IDs received

ARQ0 (0x585)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	RSVD	RSVD	RSVD	DIS_DBL_ACK_RETX_C	–	–
Reset	–	0b0	0b0	0b1	0b1	0b0	–	–
Access Type	–					Write, Read	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
DIS_DBL_ACK_RETX_C	2	Disable retransmission due to receiving same ACK twice	0b0: Enabled 0b1: Disabled

ARQ1 (0x586)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD[2:0]			–	–	MAX_RT_ERR_OEN_C	RT_CNT_OEN_C
Reset	–	0x7			–	–	0b1	0b0
Access Type	–				–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR_OEN_C	1	Enable reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR_C—0X587) for this channel at ERRB pin	0b0: Disable reporting of ARQ maximum retransmission limit errors 0b1: Enable reporting of ARQ maximum retransmission limit errors
RT_CNT_OEN_C	0	Enable reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT_C (0x587) of this channel is greater than 0.	0b0: Disable reporting of ARQ retransmission event 0b1: Enable reporting of ARQ retransmission event

ARQ2 (0x587)

BIT	7	6	5	4	3	2	1	0
Field	MAX_RT_ERR_C	RT_CNT_C[6:0]						
Reset	0b0	0x0						
Access Type	Read Clears All	Read Clears All						

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BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR_C	7	Reached maximum retransmit limit (MAX_RT_C—0x586) for one packet in this channel	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT_C	6:0	Total retransmission count in this channel	0bXXXXXXX: Count of retransmission for this channel

TR0 (0x590)

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN_D	RX_CRC_EN_D	RSVD[1:0]		PRIO_VAL_D[1:0]		PRIO_CFG_D[1:0]	
Reset	0b1	0b1	0x3		0x0		0x0	
Access Type	Write, Read	Write, Read			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN_D	7	When set, calculate and append CRC to each packet transmitted from this port	0b0: Do not calculate and append CRC to each packet 0b1: Calculate and append CRC to each packet
RX_CRC_EN_D	6	When set, indicates that packets received at this port have appended CRC, and CRC checking should be performed at each packet.	0b0: Do not perform CRC check at each packet 0b1: Perform CRC check at each packet
PRIO_VAL_D	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG_D	1:0	Adjust the priority to be used for requests from this channel	0b00: Priority from Tx adapter is used 0b01: Priority from Tx adapter is increased 0b10: Priority from Tx adapter is decreased 0b11: Priority in PRIO_VAL register is used

TR1 (0x591)

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT_D[1:0]		BW_VAL_D[5:0]					
Reset	0x2		0x30					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT_D	7:6	Channel bandwidth-allocation multiplication factor	0b00: Multiply BW_VAL_D by 1 0b01: Multiply BW_VAL_D by 4 0b10: Multiply BW_VAL_D by 16 0b11: Multiply BW_VAL_D by 16
BW_VAL_D	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL_D x BW_MULT_D/10 as a percentage of total link bandwidth	0bXXXXXX: Channel base-bandwidth value

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TR3 (0x593)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TX_SRC_ID_D[2:0]		
Reset	–	–	–	–	–	0x0		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID_D	2:0	Source identifier used in packets transmitted from this port. Default value is set by CFG0 pin.	0bXXX: Source ID for packets from this channel

TR4 (0x594)

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL_D[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL_D	7:0	Received packets from selected sources Each bit indicates whether packets with that source ID should be received or not. For example, when RX_SRC_SEL_D = 00001001, then packets with source ID equal to 0 and 3 will be received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received . . . 0xFF: Packets from all source IDs received

ARQ0 (0x595)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	RSVD	RSVD	RSVD	DIS_DBL_ACK_RETX_D	–	–
Reset	–	0b0	0b0	0b1	0b1	0b0	–	–
Access Type	–					Write, Read	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
DIS_DBL_ACK_RETX_D	2	Disables retransmission due to receiving same ACK twice	0b0: Enabled 0b1: Disabled

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ARQ1 (0x596)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD[2:0]			–	–	MAX_RT_ERR_OEN_D	RT_CNT_OEN_D
Reset	–	0x7			–	–	0b1	0b0
Access Type	–				–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR_OEN_D	1	Enables reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR—0x597) for this channel at ERRB pin	0b0: Disable reporting of ARQ maximum retransmission limit errors 0b1: Enable reporting of ARQ maximum retransmission limit errors
RT_CNT_OEN_D	0	Enables reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT_D (0x597) of this channel is greater than 0.	0b0: Disable reporting of ARQ retransmission event 0b1: Enable reporting of ARQ retransmission event

ARQ2 (0x597)

BIT	7	6	5	4	3	2	1	0
Field	MAX_RT_ERR_D	RT_CNT_D[6:0]						
Reset	0b0	0x0						
Access Type	Read Clears All	Read Clears All						

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR_D	7	Reached maximum retransmit limit (MAX_RT_D—0x596) for one packet in this channel	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT_D	6:0	Total retransmission count in this channel	0bXXXXXXX: Count of retransmission for this channel

TR0 (0x5A0)

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
Reset	0b1	0b1	0x3		0x0		0x0	
Access Type	Write, Read	Write, Read			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN	7	When set, calculate and append CRC to each packet transmitted from this port	0b0: Do not calculate and append CRC to each packet 0b1: Calculate and append CRC to each packet
RX_CRC_EN	6	When set, indicates that packets received at this port have appended CRC, and CRC checking should be performed at each packet.	0b0: Do not perform CRC check at each packet 0b1: Perform CRC check at each packet

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BITFIELD	BITS	DESCRIPTION	DECODE
PRIO_VAL	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG	1:0	Adjusts the priority to be used for requests from this channel.	0b00: Priority from Tx adapter is used 0b01: Priority from Tx adapter is increased 0b10: Priority from Tx adapter is decreased 0b11: Priority in PRIO_VAL register is used

TR1 (0x5A1)

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT[1:0]		BW_VAL[5:0]					
Reset	0x2		0x30					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT	7:6	Channel bandwidth-allocation multiplication factor	0b00: Multiply BW_VAL by 1 0b01: Multiply BW_VAL by 4 0b10: Multiply BW_VAL by 16 0b11: Multiply BW_VAL by 16
BW_VAL	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL x BW_MULT/10 as a percentage of total link bandwidth	0bXXXXXX: Channel base-bandwidth value

TR3 (0x5A3)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TX_SRC_ID[2:0]		
Reset	–	–	–	–	–	0x0		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID	2:0	Source identifier used in packets transmitted from this port. Default value is set by CFG0 pin.	0bXXX: Source ID for packets from this channel

TR4 (0x5A4)

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL[7:0]							
Reset	0xFF							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL	7:0	Received packets from selected sources Each bit indicates whether packets with that source ID should be received or not. For example, when RX_SRC_SEL = 00001001, then packets with source ID equal to 0 and 3 will be received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received . . . 0xFF: Packets from all source IDs received

ARQ0 (0x5A5)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	RSVD	RSVD	RSVD	DIS_DBL_ACK_RETX	–	–
Reset	–	0b0	0b0	0b1	0b1	0b0	–	–
Access Type	–					Write, Read	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
DIS_DBL_ACK_RETX	2	Disables retransmission due to receiving same ACK twice	0b0: Enabled 0b1: Disabled

ARQ1 (0x5A6)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
Reset	–	0x7			–	–	0b1	0b0
Access Type	–				–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR_OEN	1	Enables reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR) for this channel at ERRB pin	0b0: Disable reporting of ARQ maximum retransmission limit errors 0b1: Enable reporting of ARQ maximum retransmission limit errors
RT_CNT_OEN	0	Enables reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT of this channel is greater than 0.	0b0: Disable reporting of ARQ retransmission event 0b1: Enable reporting of ARQ retransmission event

ARQ2 (0x5A7)

BIT	7	6	5	4	3	2	1	0
Field	MAX_RT_ERR	RT_CNT[6:0]						
Reset	0b0	0x0						
Access Type	Read Clears All	Read Clears All						

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BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR	7	Reached maximum retransmit limit (MAX_RT) for one packet in this channel	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT	6:0	Total retransmission count in this channel	0bXXXXXXX: Count of retransmission for this channel

TR0 (0x5B0)

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN_B	RX_CRC_EN_B	RSVD[1:0]		PRIO_VAL_B[1:0]		PRIO_CFG_B[1:0]	
Reset	0b1	0b1	0x3		0x0		0x0	
Access Type	Write, Read	Write, Read			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN_B	7	When set, calculates and appends CRC to each packet transmitted from this port	0b0: Do not calculate and append CRC to each packet 0b1: Calculate and append CRC to each packet
RX_CRC_EN_B	6	When set, indicates that packets received at this port have appended CRC, and CRC checking should be performed at each packet.	0b0: Do not perform CRC check at each packet 0b1: Perform CRC check at each packet
PRIO_VAL_B	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG_B	1:0	Adjusts the priority to be used for requests from this channel	0b00: Priority from Tx adapter is used 0b01: Priority from Tx adapter is increased 0b10: Priority from Tx adapter is decreased 0b11: Priority in PRIO_VAL register is used

TR1 (0x5B1)

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT_B[1:0]		BW_VAL_B[5:0]					
Reset	0x2		0x30					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT_B	7:6	Channel bandwidth-allocation multiplication factor	0b00: Multiply BW_VAL_B by 1 0b01: Multiply BW_VAL_B by 4 0b10: Multiply BW_VAL_B by 16 0b11: Multiply BW_VAL_B by 16
BW_VAL_B	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL_B x BW_MULT_B/10 as a percentage of total link bandwidth	0bXXXXXX: Channel base-bandwidth value

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TR3 (0x5B3)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TX_SRC_ID_B[2:0]		
Reset	–	–	–	–	–	0x0		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID_B	2:0	Source identifier used in packets transmitted from this port. Default value is set by CFG0 pin.	0bXXX: Source ID for packets from this channel

TR4 (0x5B4)

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL_B[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL_B	7:0	Receives packets from selected sources Each bit indicates whether packets with that source ID should be received or not. For example, when RX_SRC_SEL_B = 00001001, then packets with source ID equal to 0 and 3 will be received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received . . . 0xFF: Packets from all source IDs received

ARQ0 (0x5B5)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	RSVD	RSVD	RSVD	DIS_DBL_ACK_RETX_B	–	–
Reset	–	0b0	0b0	0b1	0b1	0b0	–	–
Access Type	–					Write, Read	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
DIS_DBL_ACK_RETX_B	2	Disables retransmission due to receiving same ACK twice	0b0: Enabled 0b1: Disabled

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ARQ1 (0x5B6)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD[2:0]			–	–	MAX_RT_ERR_OEN_B	RT_CNT_OEN_B
Reset	–	0x7			–	–	0b1	0b0
Access Type	–				–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR_OEN_B	1	Enables reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR_B—0x5B7) for this channel at ERRB pin	0b0: Disable reporting of ARQ maximum retransmission limit errors 0b1: Enable reporting of ARQ maximum retransmission limit errors
RT_CNT_OEN_B	0	Enables reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT_B (0x5B7) of this channel is greater than 0.	0b0: Disable reporting of ARQ retransmission event 0b1: Enable reporting of ARQ retransmission event

ARQ2 (0x5B7)

BIT	7	6	5	4	3	2	1	0
Field	MAX_RT_ERR_B	RT_CNT_B[6:0]						
Reset	0b0	0x0						
Access Type	Read Clears All	Read Clears All						

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR_B	7	Reached maximum retransmit limit (MAX_RT_B—0x5B6) for one packet in this channel	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT_B	6:0	Total retransmission count in this channel	0xXXXXXXX: Count of retransmission for this channel

TR0 (0x5C0)

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN_C	RX_CRC_EN_C	RSVD[1:0]		PRIO_VAL_C[1:0]		PRIO_CFG_C[1:0]	
Reset	0b1	0b1	0x3		0x0		0x0	
Access Type	Write, Read	Write, Read			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN_C	7	When set, calculate and append CRC to each packet transmitted from this port	0b0: Do not calculate and append CRC to each packet 0b1: Calculate and append CRC to each packet
RX_CRC_EN_C	6	When set, indicates that packets received at this port have appended CRC, and CRC checking should be performed at each packet.	0b0: Do not perform CRC check at each packet 0b1: Perform CRC check at each packet

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BITFIELD	BITS	DESCRIPTION	DECODE
PRIO_VAL_C	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG_C	1:0	Adjusts the priority to be used for requests from this channel	0b00: Priority from Tx adapter is used 0b01: Priority from Tx adapter is increased 0b10: Priority from Tx adapter is decreased 0b11: Priority in PRIO_VAL register is used

TR1 (0x5C1)

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT_C[1:0]		BW_VAL_C[5:0]					
Reset	0x2		0x30					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT_C	7:6	Channel bandwidth-allocation multiplication factor	0b00: Multiply BW_VAL_C by 1 0b01: Multiply BW_VAL_C by 4 0b10: Multiply BW_VAL_C by 16 0b11: Multiply BW_VAL_C by 16
BW_VAL_C	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL_C x BW_MULT_C/10 as a percentage of total link bandwidth	0bXXXXXX: Channel base-bandwidth value

TR3 (0x5C3)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TX_SRC_ID_C[2:0]		
Reset	–	–	–	–	–	0x0		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID_C	2:0	Source identifier used in packets transmitted from this port. Default value is set by CFG0 pin.	0bXXX: Source ID for packets from this channel

TR4 (0x5C4)

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL_C[7:0]							
Reset	0xFF							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL_C	7:0	Received packets from selected sources Each bit indicates whether packets with that source ID should be received or not. For example, when RX_SRC_SEL_C = 00001001, then packets with source ID equal to 0 and 3 will be received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received . . . 0xFF: Packets from all source IDs received

ARQ0 (0x5C5)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	RSVD	RSVD	RSVD	DIS_DBL_ACK_RETX_C	–	–
Reset	–	0b0	0b0	0b1	0b1	0b0	–	–
Access Type	–					Write, Read	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
DIS_DBL_ACK_RETX_C	2	Disables retransmission due to receiving same ACK twice	0b0: Enabled 0b1: Disabled

ARQ1 (0x5C6)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD[2:0]			–	–	MAX_RT_ERR_OEN_C	RT_CNT_OEN_C
Reset	–	0x7			–	–	0b1	0b0
Access Type	–				–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR_OEN_C	1	Enables reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR_C—0c5C7) for this channel at ERRB pin	0b0: Disable reporting of ARQ maximum retransmission limit errors 0b1: Enable reporting of ARQ maximum retransmission limit errors
RT_CNT_OEN_C	0	Enables reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT_C (0x5C7) of this channel is greater than 0.	0b0: Disable reporting of ARQ retransmission event 0b1: Enable reporting of ARQ retransmission event

ARQ2 (0x5C7)

BIT	7	6	5	4	3	2	1	0
Field	MAX_RT_ERR_C	RT_CNT_C[6:0]						
Reset	0b0	0x0						
Access Type	Read Clears All	Read Clears All						

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BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR_C	7	Reached maximum retransmit limit (MAX_RT_C—0x5C6) for one packet in this channel	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT_C	6:0	Total retransmission count in this channel	0xXXXXXXX: Count of retransmission for this channel

TR0 (0x5D0)

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN_D	RX_CRC_EN_D	RSVD[1:0]		PRIO_VAL_D[1:0]		PRIO_CFG_D[1:0]	
Reset	0b1	0b1	0x3		0x0		0x0	
Access Type	Write, Read	Write, Read			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN_D	7	When set, calculate and append CRC to each packet transmitted from this port	0b0: Do not calculate and append CRC to each packet 0b1: Calculate and append CRC to each packet
RX_CRC_EN_D	6	When set, indicates that packets received at this port have appended CRC, and CRC checking should be performed at each packet.	0b0: Do not perform CRC check at each packet 0b1: Perform CRC check at each packet
PRIO_VAL_D	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG_D	1:0	Adjusts the priority to be used for requests from this channel	0b00: Priority from Tx adapter is used 0b01: Priority from Tx adapter is increased 0b10: Priority from Tx adapter is decreased 0b11: Priority in PRIO_VAL register is used

TR1 (0x5D1)

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT_D[1:0]		BW_VAL_D[5:0]					
Reset	0x2		0x30					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT_D	7:6	Channel bandwidth-allocation multiplication factor	0b00: Multiply BW_VAL_D by 1 0b01: Multiply BW_VAL_D by 4 0b10: Multiply BW_VAL_D by 16 0b11: Multiply BW_VAL_D by 16
BW_VAL_D	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL_D x BW_MULT_D/10 as a percentage of total link bandwidth	0bXXXXXX: Channel base-bandwidth value

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TR3 (0x5D3)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TX_SRC_ID_D[2:0]		
Reset	–	–	–	–	–	0x0		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID_D	2:0	Source identifier used in packets transmitted from this port. Default value is set by CFG0 pin.	0bXXX: Source ID for packets from this channel

TR4 (0x5D4)

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL_D[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL_D	7:0	Received packets from selected sources Each bit indicates whether packets with that source ID should be received or not. For example, when RX_SRC_SEL_D = 00001001, then packets with source ID equal to 0 and 3 will be received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received . . . 0xFF: Packets from all source IDs received

ARQ0 (0x5D5)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	RSVD	RSVD	RSVD	DIS_DBL_ACK_RETX_D	–	–
Reset	–	0b0	0b0	0b1	0b1	0b0	–	–
Access Type	–					Write, Read	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
DIS_DBL_ACK_RETX_D	2	Disables retransmission due to receiving same ACK twice	0b0: Enabled 0b1: Disabled

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ARQ1 (0x5D6)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD[2:0]			–	–	MAX_RT_ERR_OEN_D	RT_CNT_OEN_D
Reset	–	0x7			–	–	0b1	0b0
Access Type	–				–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR_OEN_D	1	Enables reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR_D—0x5D7) for this channel at ERRB pin	0b0: Disable reporting of ARQ maximum retransmission limit errors 0b1: Enable reporting of ARQ maximum retransmission limit errors
RT_CNT_OEN_D	0	Enables reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT_D (0x5D7) of this channel is greater than 0.	0b0: Disable reporting of ARQ retransmission event 0b1: Enable reporting of ARQ retransmission event

ARQ2 (0x5D7)

BIT	7	6	5	4	3	2	1	0
Field	MAX_RT_ERR_D	RT_CNT_D[6:0]						
Reset	0b0	0x0						
Access Type	Read Clears All	Read Clears All						

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR_D	7	Reached maximum retransmit limit (MAX_RT_D—5D6) for one packet in this channel.	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT_D	6:0	Total retransmission count in this channel	0xXXXXXXX: Count of retransmission for this channel

I2C_0 (0x640)

BIT	7	6	5	4	3	2	1	0
Field	–	–	SLV_SH_P0_A[1:0]		–	SLV_TO_P0_A[2:0]		
Reset	–	–	0x2		–	0x6		
Access Type	–	–	Write, Read		–	Write, Read		

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BITFIELD	BITS	DESCRIPTION	DECODE
SLV_SH_P0_A	5:4	Link A GMSL1 AND GMSL2 I²C-to-I²C Subordinate Setup and Hold Time Setting (setup, hold) Configures the interval between SDA and SCL transitions when driven by the internal I²C subordinate. Set this according to the I²C speed mode. This setting applies only to I²C Port 0 for GMSL2. This setting applies to all I²C Ports for GMSL1.	0b00: Fast-mode Plus 0b01: Fast-mode 0b10: Standard-mode 0b11: Reserved
SLV_TO_P0_A	2:0	Link A GMSL1 AND GMSL2 I²C-to-I²C Subordinate Timeout Setting Internal I²C subordinate times out after the configured duration if it does not receive any response while waiting for a packet from the remote device. This setting applies only to I²C Port 0 for GMSL2. This setting applies to all I²C Ports for GMSL1.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_1 (0x641)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	MST_BT_P0_A[2:0]			–	MST_TO_P0_A[2:0]		
Reset	0x0	0x5			–	0x6		
Access Type		Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
MST_BT_P0_A	6:4	Link A GMSL1 AND GMSL2 I²C-to-I²C Main Bit Rate Setting Configures the I²C bit rate used by the internal I²C main (in the device on the remote side from the external I²C main). This setting applies only to I²C Port 0 for GMSL2 Link A This setting applies to all I²C Ports for GMSL1 Link A. Set this according to the I²C speed mode: Fast-mode Plus = 101 to 111 Fast-mode = 010 to 101 Standard-mode = 000 to 010	3b000: 9.92Kbps - Set for I²C Standard-mode speed 3b001: 33.2Kbps - Set for I²C Standard-mode speed 3b010: 99.2Kbps - Set for I²C Standard or Fast-mode speed 3b011: 123Kbps - Set for I²C Fast-mode speed 3b100: 203Kbps - Set for I²C Fast-mode speed 3b101: 397Kbps - Set for I²C Fast or Fast-mode Plus speed 3b110: 625Kbps - Set for I²C Fast or Fast-mode Plus speed 3b111: 980Kbps - Set for I²C Fast-mode Plus speed

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BITFIELD	BITS	DESCRIPTION	DECODE
MST_TO_P0_A	2:0	Link A GMSL1 AND GMSL2 I²C-to-I²C Main Timeout Setting Internal I²C main times out after the configured duration if it does not receive any response while waiting for a packet from the remote device. This setting applies only to I²C Port 0 for GMSL2. This setting applies to all I²C Ports for GMSL1.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_2 (0x642)

BIT	7	6	5	4	3	2	1	0
Field	SRC_A_P0_A[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_A_P0_A	7:1	Link A GMSL1 AND GMSL2 I²C Address Translator Source A When I²C device address matches SRC_A_P0_A, internal I²C main (on the remote side) replaces the device address by DST_A_P0_A. This setting applies only to I²C Port 0 for GMSL2. This setting applies to all I²C Ports for GMSL1.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 . . . 0b1111111: Write/read device address is 0xFE/0xFF

I2C_3 (0x643)

BIT	7	6	5	4	3	2	1	0
Field	DST_A_P0_A[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

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BITFIELD	BITS	DESCRIPTION	DECODE
DST_A_P0_A	7:1	Link A GMSL1 AND GMSL2 I²C Address Translator Destination A This setting applies only to I²C Port 0 for GMSL2. This setting applies to all I²C Ports for GMSL1. See the description of SRC_A_P0_A.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 . . . 0b1111111: Write/read device address is 0xFE/0xFF

I2C_4 (0x644)

BIT	7	6	5	4	3	2	1	0
Field	SRC_B_P0_A[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_B_P0_A	7:1	Link A GMSL1 AND GMSL2 I²C Address Translator Source B When I²C device address matches SRC_B_P0_A, internal I²C main (on the remote side) replaces the device address by DST_B_P0_A. This setting applies only to I²C Port 0 for GMSL2. This setting applies to all I²C Ports for GMSL1.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 . . . 0b1111111: Write/read device address is 0xFE/0xFF

I2C_5 (0x645)

BIT	7	6	5	4	3	2	1	0
Field	DST_B_P0_A[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_B_P0_A	7:1	Link A GMSL1 AND GMSL2 I²C Address Translator Destination B This setting applies only to I²C Port 0 for GMSL2. This setting applies to all I²C Ports for GMSL1. See the description of SRC_B_P0_A.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 . . . 0b1111111: Write/read device address is 0xFE/0xFF

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I2C_0 (0x650)

BIT	7	6	5	4	3	2	1	0
Field	–	–	SLV_SH_P0_B[1:0]		–	SLV_TO_P0_B[2:0]		
Reset	–	–	0x2		–	0x6		
Access Type	–	–	Write, Read		–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
SLV_SH_P0_B	5:4	Link B GMSL1 AND GMSL2 I^{2}C-to-I^{2}C Subordinate Setup and Hold Time Setting (setup, hold) Configures the interval between SDA and SCL transitions when driven by the internal I^{2}C subordinate. Set this according to the I^{2}C speed mode. This setting applies only to I^{2}C Port 0 for GMSL2. This setting applies to all I^{2}C Ports for GMSL1.	0b00: Fast-mode Plus 0b01: Fast-mode 0b10: Standard-mode 0b11: Reserved
SLV_TO_P0_B	2:0	Link B GMSL1 AND GMSL2 I^{2}C-to-I^{2}C Subordinate Timeout Setting Internal I^{2}C subordinate times out after the configured duration if it does not receive any response while waiting for a packet from the remote device. This setting applies only to I^{2}C Port 0 for GMSL2. This setting applies to all I^{2}C Ports for GMSL1.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_1 (0x651)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	MST_BT_P0_B[2:0]			–	MST_TO_P0_B[2:0]		
Reset	0x0	0x5			–	0x6		
Access Type		Write, Read			–	Write, Read		

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BITFIELD	BITS	DESCRIPTION	DECODE
MST_BT_P0_B	6:4	Link B GMSL1 **AND** GMSL2 I²C-to-I²C Main Bit Rate Setting Configures the I²C bit rate used by the internal I²C main (in the device on the remote side from the external I²C main). This setting applies only to I²C Port 0 for GMSL2 Link B. This setting applies to all I²C Ports for GMSL1 Link B. Set this according to the I²C speed mode: Fast-mode Plus = 101 to 111 Fast-mode = 010 to 101 Standard-mode = 000 to 010	3b000: 9.92Kbps - Set for I²C Standard-mode speed 3b001: 33.2Kbps - Set for I²C Standard-mode speed 3b010: 99.2Kbps - Set for I²C Standard or Fast-mode speed 3b011: 123Kbps - Set for I²C Fast-mode speed 3b100: 203Kbps - Set for I²C Fast-mode speed 3b101: 397Kbps - Set for I²C Fast or Fast-mode Plus speed 3b110: 625Kbps - Set for I²C Fast or Fast-mode Plus speed 3b111: 980Kbps - Set for I²C Fast-mode Plus speed
MST_TO_P0_B	2:0	Link B GMSL1 AND GMSL2 I²C-to-I²C Main Timeout Setting Internal I²C main times out after the configured duration if it does not receive any response while waiting for a packet from the remote device. This setting applies only to I²C Port 0 for GMSL2. This setting applies to all I²C Ports for GMSL1.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_2 (0x652)

BIT	7	6	5	4	3	2	1	0
Field	SRC_A_P0_B[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_A_P0_B	7:1	Link B GMSL1 AND GMSL2 I²C Address Translator Source A When I²C device address matches SRC_A_P0_B, internal I²C main (on the remote side) replaces the device address by DST_A_P0_B. This setting applies only to I²C Port 0 for GMSL2. This setting applies to all I²C Ports for GMSL1.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 . . . 0b1111111: Write/read device address is 0xFE/0xFF

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I2C_3 (0x653)

BIT	7	6	5	4	3	2	1	0
Field	DST_A_P0_B[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_A_P0_B	7:1	Link B GMSL1 AND GMSL2 I^{2}C Address Translator Destination A. This setting applies only to I^{2}C Port 0 for GMSL2. This setting applies to all I^{2}C Ports for GMSL1. See the description of SRC_A_P0_B.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 . . . 0b1111111: Write/read device address is 0xFE/0xFF

I2C_4 (0x654)

BIT	7	6	5	4	3	2	1	0
Field	SRC_B_P0_B[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_B_P0_B	7:1	Link B GMSL1 AND GMSL2 I^{2}C Address Translator Source B When I^{2}C device address matches SRC_B_P0_B, internal I^{2}C main (on the remote side) replaces the device address by DST_B_P0_B. This setting applies only to I^{2}C Port 0 for GMSL2. This setting applies to all I^{2}C Ports for GMSL1.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 . . . 0b1111111: Write/read device address is 0xFE/0xFF

I2C_5 (0x655)

BIT	7	6	5	4	3	2	1	0
Field	DST_B_P0_B[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

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BITFIELD	BITS	DESCRIPTION	DECODE
DST_B_P0_B	7:1	Link B GMSL1 AND GMSL2 I²C Address Translator Destination B This setting applies only to I²C Port 0 for GMSL2. This setting applies to all I²C Ports for GMSL1. See the description of SRC_B_P0_B.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 . . . 0b1111111: Write/read device address is 0xFE/0xFF

I2C_0 (0x660)

BIT	7	6	5	4	3	2	1	0
Field	–	–	SLV_SH_P0_C[1:0]		–	SLV_TO_P0_C[2:0]		
Reset	–	–	0x2		–	0x6		
Access Type	–	–	Write, Read		–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
SLV_SH_P0_C	5:4	Link C GMSL1 AND GMSL2 I²C-to-I²C Subordinate Setup and Hold Time Setting (setup, hold). Configures the interval between SDA and SCL transitions when driven by the internal I²C subordinate. Set this according to the I²C speed mode. This setting applies only to I²C Port 0 for GMSL2. This setting applies to all I²C Ports for GMSL1.	0b00: Fast-mode Plus 0b01: Fast-mode 0b10: Standard-mode 0b11: Reserved
SLV_TO_P0_C	2:0	Link C GMSL1 AND GMSL2 I²C-to-I²C Subordinate Timeout Setting Internal I²C subordinate times out after the configured duration if it does not receive any response while waiting for a packet from the remote device. This setting applies only to I²C Port 0 for GMSL2. This setting applies to all I²C Ports for GMSL1.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

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I2C_1 (0x661)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	MST_BT_P0_C[2:0]			–	MST_TO_P0_C[2:0]		
Reset	0x0	0x5			–	0x6		
Access Type		Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
MST_BT_P0_C	6:4	Link C GMSL1 AND GMSL2 I²C-to-I²C Main Bit Rate Setting Configures the I²C bit rate used by the internal I²C main (in the device on the remote side from the external I²C main). This setting applies only to I²C Port 0 for GMSL2 Link C. This setting applies to all I²C Ports for GMSL1 Link C. Set this according to the I²C speed mode: Fast-mode Plus = 101 to 111 Fast-mode = 010 to 101 Standard-mode = 000 to 010	3b000: 9.92Kbps - Set for I²C Standard-mode speed 3b001: 33.2Kbps - Set for I²C Standard-mode speed 3b010: 99.2Kbps - Set for I²C Standard or Fast-mode speed 3b011: 123Kbps - Set for I²C Fast-mode speed 3b100: 203Kbps - Set for I²C Fast-mode speed 3b101: 397Kbps - Set for I²C Fast or Fast-mode Plus speed 3b110: 625Kbps - Set for I²C Fast or Fast-mode Plus speed 3b111: 980Kbps - Set for I²C Fast-mode Plus speed
MST_TO_P0_C	2:0	Link C GMSL1 AND GMSL2 I²C-to-I²C Main Timeout Setting Internal I²C main times out after the configured duration if it does not receive any response while waiting for a packet from the remote device. This setting applies only to I²C Port 0 for GMSL2. This setting applies to all I²C Ports for GMSL1.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_2 (0x662)

BIT	7	6	5	4	3	2	1	0
Field	SRC_A_P0_C[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

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BITFIELD	BITS	DESCRIPTION	DECODE
SRC_A_P0_C	7:1	Link C GMSL1 AND GMSL2 I²C Address Translator Source A When I²C device address matches SRC_A_P0_C, internal I²C main (on the remote side) replaces the device address by DST_A_P0_C. This setting applies only to I²C Port 0 for GMSL2. This setting applies to all I²C Ports for GMSL1.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 . . . 0b1111111: Write/read device address is 0xFE/0xFF

I2C_3 (0x663)

BIT	7	6	5	4	3	2	1	0
Field	DST_A_P0_C[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_A_P0_C	7:1	Link C GMSL1 AND GMSL2 I²C Address Translator Destination A This setting applies only to I²C Port 0 for GMSL2. This setting applies to all I²C Ports for GMSL1. See the description of SRC_A_P0_C.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 . . . 0b1111111: Write/read device address is 0xFE/0xFF

I2C_4 (0x664)

BIT	7	6	5	4	3	2	1	0
Field	SRC_B_P0_C[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

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BITFIELD	BITS	DESCRIPTION	DECODE
SRC_B_P0_C	7:1	Link C GMSL1 AND GMSL2 I²C Address Translator Source B When I²C device address matches SRC_B_P0_C, internal I²C main (on the remote side) replaces the device address by DST_B_P0_C. This setting applies only to I²C Port 0 for GMSL2. This setting applies to all I²C Ports for GMSL1.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 . . . 0b1111111: Write/read device address is 0xFE/0xFF

I2C_5 (0x665)

BIT	7	6	5	4	3	2	1	0
Field	DST_B_P0_C[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_B_P0_C	7:1	Link C GMSL1 AND GMSL2 I²C Address Translator Destination B This setting applies only to I²C Port 0 for GMSL2. This setting applies to all I²C Ports for GMSL1. See the description of SRC_B_P0_C.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 . . . 0b1111111: Write/read device address is 0xFE/0xFF

I2C_0 (0x670)

BIT	7	6	5	4	3	2	1	0
Field	–	–	SLV_SH_P0_D[1:0]		–	SLV_TO_P0_D[2:0]		
Reset	–	–	0x2		–	0x6		
Access Type	–	–	Write, Read		–	Write, Read		

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BITFIELD	BITS	DESCRIPTION	DECODE
SLV_SH_P0_D	5:4	Link D GMSL1 AND GMSL2 I²C-to-I²C Subordinate Setup and Hold Time Setting (setup, hold) Configures the interval between SDA and SCL transitions when driven by the internal I²C subordinate. Set this according to the I²C speed mode. This setting applies only to I²C Port 0 for GMSL2. This setting applies to all I²C Ports for GMSL1.	0b00: Fast-mode Plus 0b01: Fast-mode 0b10: Standard-mode 0b11: Reserved
SLV_TO_P0_D	2:0	Link D GMSL1 AND GMSL2 I²C-to-I²C Subordinate Timeout Setting Internal I²C subordinate times out after the configured duration if it does not receive any response while waiting for a packet from the remote device. This setting applies only to I²C Port 0 for GMSL2. This setting applies to all I²C Ports for GMSL1.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_1 (0x671)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	MST_BT_P0_D[2:0]			–	MST_TO_P0_D[2:0]		
Reset	0x0	0x5			–	0x6		
Access Type		Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
MST_BT_P0_D	6:4	Link D GMSL1 AND GMSL2 I²C-to-I²C Main Bit Rate Setting Configures the I²C bit rate used by the internal I²C main (in the device on the remote side from the external I²C main). This setting applies only to I²C Port 0 for GMSL2 Link D. This setting applies to all I²C Ports for GMSL1 Link D. Set this according to the I²C speed mode: Fast-mode Plus = 101 to 111 Fast-mode = 010 to 101 Standard-mode = 000 to 010	3b000: 9.92Kbps - Set for I²C Standard-mode speed 3b001: 33.2Kbps - Set for I²C Standard-mode speed 3b010: 99.2Kbps - Set for I²C Standard or Fast-mode speed 3b011: 123Kbps - Set for I²C Fast-mode speed 3b100: 203Kbps - Set for I²C Fast-mode speed 3b101: 397Kbps - Set for I²C Fast or Fast-mode Plus speed 3b110: 625Kbps - Set for I²C Fast or Fast-mode Plus speed 3b111: 980Kbps - Set for I²C Fast-mode Plus speed

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BITFIELD	BITS	DESCRIPTION	DECODE
MST_TO_P0_D	2:0	Link D GMSL1 AND GMSL2 I²C-to-I²C Main Timeout Setting Internal I²C main times out after the configured duration if it does not receive any response while waiting for a packet from the remote device. This setting applies only to I²C Port 0 for GMSL2. This setting applies to all I²C Ports for GMSL1.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_2 (0x672)

BIT	7	6	5	4	3	2	1	0
Field	SRC_A_P0_D[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_A_P0_D	7:1	Link D GMSL1 AND GMSL2 I²C Address Translator Source A. When I²C device address matches SRC_A_P0_D, internal I²C main (on the remote side) replaces the device address by DST_A_P0_D. This setting applies only to I²C Port 0 for GMSL2. This setting applies to all I²C Ports for GMSL1.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 . . . 0b1111111: Write/read device address is 0xFE/0xFF

I2C_3 (0x673)

BIT	7	6	5	4	3	2	1	0
Field	DST_A_P0_D[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

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BITFIELD	BITS	DESCRIPTION	DECODE
DST_A_P0_D	7:1	Link D GMSL1 AND GMSL2 I²C Address Translator Destination A This setting applies only to I²C Port 0 for GMSL2. This setting applies to all I²C Ports for GMSL1. See the description of SRC_A_P0_D.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 . . . 0b1111111: Write/read device address is 0xFE/0xFF

I2C_4 (0x674)

BIT	7	6	5	4	3	2	1	0
Field	SRC_B_P0_D[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_B_P0_D	7:1	Link D GMSL1 AND GMSL2 I²C Address Translator Source B When I²C device address main SRC_B_P0_D, internal I²C main (on the remote side) replaces the device address by DST_B_P0_D. This setting applies only to I²C Port 0 for GMSL2. This setting applies to all I²C Ports for GMSL1.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 . . . 0b1111111: Write/read device address is 0xFE/0xFF

I2C_5 (0x675)

BIT	7	6	5	4	3	2	1	0
Field	DST_B_P0_D[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_B_P0_D	7:1	Link D GMSL1 AND GMSL2 I²C address translator destination B. This setting applies only to I²C Port 0 for GMSL2. This setting applies to all I²C Ports for GMSL1. See the description of SRC_B_P0_D.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 . . . 0b1111111: Write/read device address is 0xFE/0xFF

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I2C_0 (0x680)

BIT	7	6	5	4	3	2	1	0
Field	–	–	SLV_SH_P1_A[1:0]		–	SLV_TO_P1_A[2:0]		
Reset	–	–	0x2		–	0x6		
Access Type	–	–	Write, Read		–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
SLV_SH_P1_A	5:4	GMSL2 I²C-to-I²C Subordinate Setup and Hold Time Setting (setup, hold) Configures the interval between SDA and SCL transitions when driven by the internal I²C subordinate. Set this according to the I²C speed mode. This setting applies only to I²C Port 1 for GMSL2 Link A.	0b00: Fast-mode Plus 0b01: Fast-mode 0b10: Standard-mode 0b11: Reserved
SLV_TO_P1_A	2:0	GMSL2 I²C-to-I²C Subordinate Timeout Setting Internal GMSL2 I²C subordinate times out after the configured duration if it does not receive any response while waiting for a packet from the remote device. This setting applies only to I²C Port 1 for GMSL2 Link A.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_1 (0x681)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	MST_BT_P1_A[2:0]			–	MST_TO_P1_A[2:0]		
Reset	0x0	0x5			–	0x6		
Access Type		Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
MST_BT_P1_A	6:4	GMSL2 I²C-to-I²C Main Bit Rate Setting Configures the I²C bit rate used by the internal I²C main (in the device on the remote side from the external I²C main). This setting applies only to I²C Port 1 for GMSL2 Link A. Set this according to the I²C speed mode: Fast-mode Plus = 101 to 111 Fast-mode = 010 to 101 Standard-mode = 000 to 010	3b000: 9.92Kbps - Set for I²C Standard-mode speed 3b001: 33.2Kbps - Set for I²C Standard-mode speed 3b010: 99.2Kbps - Set for I²C Standard or Fast-mode speed 3b011: 123Kbps - Set for I²C Fast-mode speed 3b100: 203Kbps - Set for I²C Fast-mode speed 3b101: 397Kbps - Set for I²C Fast or Fast-mode Plus speed 3b110: 625Kbps - Set for I²C Fast or Fast-mode Plus speed 3b111: 980Kbps - Set for I²C Fast-mode Plus speed

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BITFIELD	BITS	DESCRIPTION	DECODE
MST_TO_P1_A	2:0	GMSL2 I²C-to-I²C Main Timeout Setting Internal GMSL2 I²C main times out after the configured duration if it does not receive any response while waiting for a packet from the remote device. This setting applies only to I²C Port 1 for GMSL2 Link A.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_2 (0x682)

BIT	7	6	5	4	3	2	1	0
Field	SRC_A_P1_A[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_A_P1_A	7:1	GMSL2 I²C Address Translator Source A. When I²C device address matches SRC_A_P1_A, internal I²C main (on the remote side) replaces the device address by DST_A_P1_A. This setting applies only to I²C Port 1 for GMSL2 Link A.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 . . . 0b1111111: Write/read device address is 0xFE/0xFF

I2C_3 (0x683)

BIT	7	6	5	4	3	2	1	0
Field	DST_A_P1_A[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_A_P1_A	7:1	GMSL2 I²C Address Translator Destination A. This setting applies only to I²C Port 1 for GMSL2 Link A. See the description of SRC_A_P1_A	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 . . . 0b1111111: Write/read device address is 0xFE/0xFF

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I2C_4 (0x684)

BIT	7	6	5	4	3	2	1	0
Field	SRC_B_P1_A[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_B_P1_A	7:1	GMSL2 I²C Address Translator Source B When I²C device address matches SRC_B_P1_A, internal I²C main (on the remote side) replaces the device address by DST_B_P1_A. This setting applies only to I²C Port 1 for GMSL2 Link A.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 . . . 0b1111111: Write/read device address is 0xFE/0xFF

I2C_5 (0x685)

BIT	7	6	5	4	3	2	1	0
Field	DST_B_P1_A[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_B_P1_A	7:1	GMSL2 I²C Address Translator Destination B. This setting applies only to I²C Port 1 for GMSL2 Link A. See the description of SRC_B_P1_A.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 . . . 0b1111111: Write/read device address is 0xFE/0xFF

I2C_0 (0x688)

BIT	7	6	5	4	3	2	1	0
Field	–	–	SLV_SH_P2_A[1:0]		–	SLV_TO_P2_A[2:0]		
Reset	–	–	0x2		–	0x6		
Access Type	–	–	Write, Read		–	Write, Read		

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BITFIELD	BITS	DESCRIPTION	DECODE
SLV_SH_P2_A	5:4	GMSL2 I²C-to-I²C Subordinate Setup and Hold Time Setting (setup, hold) Configures the interval between SDA and SCL transitions when driven by the internal I²C subordinate. Set this according to the I²C speed mode. This setting applies only to I²C Port 2 for GMSL2 Link A.	0b00: Fast-mode Plus 0b01: Fast-mode 0b10: Standard-mode 0b11: Reserved
SLV_TO_P2_A	2:0	GMSL2 I²C-to-I²C Subordinate Timeout Setting Internal GMSL2 I²C subordinate times out after the configured duration if it does not receive any response while waiting for a packet from the remote device. This setting applies only to I²C Port 2 for GMSL2 Link A.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_1 (0x689)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	MST_BT_P2_A[2:0]			–	MST_TO_P2_A[2:0]		
Reset	0x0	0x5			–	0x6		
Access Type		Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
MST_BT_P2_A	6:4	GMSL2 I²C-to-I²C Main Bit Rate Setting Configures the I²C bit rate used by the internal I²C main (in the device on the remote side from the external I²C main). This setting applies only to I²C Port 2 for GMSL2 Link A. Set this according to the I²C speed mode: Fast-mode Plus = 101 to 111 Fast-mode = 010 to 101 Standard-mode = 000 to 010	3b000: 9.92Kbps - Set for I²C Standard-mode speed 3b001: 33.2Kbps - Set for I²C Standard-mode speed 3b010: 99.2Kbps - Set for I²C Standard or Fast-mode speed 3b011: 123Kbps - Set for I²C Fast-mode speed 3b100: 203Kbps - Set for I²C Fast-mode speed 3b101: 397Kbps - Set for I²C Fast or Fast-mode Plus speed 3b110: 625Kbps - Set for I²C Fast or Fast-mode Plus speed 3b111: 980Kbps - Set for I²C Fast-mode Plus speed
MST_TO_P2_A	2:0	GMSL2 I²C-to-I²C Main Timeout Setting Internal GMSL2 I²C main times out after the configured duration if it does not receive any response while waiting for a packet from the remote device. This setting applies only to I²C Port 2 for GMSL2 Link A.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

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I2C_2 (0x68A)

BIT	7	6	5	4	3	2	1	0
Field	SRC_A_P2_A[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_A_P2_A	7:1	GMSL2 I²C Address Translator Source A When I²C device address matches SRC_A_P2_A, internal I²C main (on the remote side) replaces the device address by DST_A_P2_A. This setting applies only to I²C Port 2 for GMSL2 Link A.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 . . . 0b1111111: Write/read device address is 0xFE/0xFF

I2C_3 (0x68B)

BIT	7	6	5	4	3	2	1	0
Field	DST_A_P2_A[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_A_P2_A	7:1	GMSL2 I²C Address Translator Destination A. This setting applies only to I²C Port 2 for GMSL2 Link A. See the description of SRC_A_P2_A.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 . . . 0b1111111: Write/read device address is 0xFE/0xFF

I2C_4 (0x68C)

BIT	7	6	5	4	3	2	1	0
Field	SRC_B_P2_A[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

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BITFIELD	BITS	DESCRIPTION	DECODE
SRC_B_P2_A	7:1	GMSL2 I²C Address Translator Source B When I²C device address matches SRC_B_P2_A, internal I²C main (on the remote side) replaces the device address by DST_B_P2_A. This setting applies only to I²C Port 2 for GMSL2 Link A.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 . . . 0b1111111: Write/read device address is 0xFE/0xFF

I2C_5 (0x68D)

BIT	7	6	5	4	3	2	1	0
Field	DST_B_P2_A[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_B_P2_A	7:1	GMSL2 I²C Address Translator Destination B. This setting applies only to I²C Port 2 for GMSL2 Link A. See the description of SRC_B_P2_A.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 . . . 0b1111111: Write/read device address is 0xFE/0xFF

I2C_0 (0x690)

BIT	7	6	5	4	3	2	1	0
Field	–	–	SLV_SH_P1_B[1:0]		–	SLV_TO_P1_B[2:0]		
Reset	–	–	0x2		–	0x6		
Access Type	–	–	Write, Read		–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
SLV_SH_P1_B	5:4	GMSL2 I²C-to-I²C Subordinate Setup and Hold Time Setting (setup, hold) Configures the interval between SDA and SCL transitions when driven by the internal I²C subordinate. Set this according to the I²C speed mode. This setting applies only to I²C Port 1 for GMSL2 Link B.	0b00: Fast-mode Plus 0b01: Fast-mode 0b10: Standard-mode 0b11: Reserved

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BITFIELD	BITS	DESCRIPTION	DECODE
SLV_TO_P1_B	2:0	GMSL2 I²C-to-I²C Subordinate Timeout Setting Internal GMSL2 I²C subordinate times out after the configured duration if it does not receive any response while waiting for a packet from the remote device. This setting applies only to I²C Port 1 for GMSL2 Link B.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_1 (0x691)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	MST_BT_P1_B[2:0]			–	MST_TO_P1_B[2:0]		
Reset	0x0	0x5			–	0x6		
Access Type		Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
MST_BT_P1_B	6:4	GMSL2 I²C-to-I²C Main Bit Rate Setting Configures the I²C bit rate used by the internal I²C main (in the device on the remote side from the external I²C main). This setting applies only to I²C Port 1 for GMSL2 Link B. Set this according to the I²C speed mode: Fast-mode Plus = 101 to 111 Fast-mode = 010 to 101 Standard-mode = 000 to 010	3b000: 9.92Kbps - Set for I²C Standard-mode speed 3b001: 33.2Kbps - Set for I²C Standard-mode speed 3b010: 99.2Kbps - Set for I²C Standard or Fast-mode speed 3b011: 123Kbps - Set for I²C Fast-mode speed 3b100: 203Kbps - Set for I²C Fast-mode speed 3b101: 397Kbps - Set for I²C Fast or Fast-mode Plus speed 3b110: 625Kbps - Set for I²C Fast or Fast-mode Plus speed 3b111: 980Kbps - Set for I²C Fast-mode Plus speed
MST_TO_P1_B	2:0	GMSL2 I²C-to-I²C Main Timeout Setting Internal GMSL2 I²C main times out after the configured duration if it does not receive any response while waiting for a packet from the remote device. This setting applies only to I²C Port 1 for GMSL2 Link B.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_2 (0x692)

BIT	7	6	5	4	3	2	1	0
Field	SRC_A_P1_B[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

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BITFIELD	BITS	DESCRIPTION	DECODE
SRC_A_P1_B	7:1	GMSL2 I²C Address Translator Source A. When I²C device address matches SRC_A_P1_B, internal I²C main (on the remote side) replaces the device address by DST_A_P1_B This setting applies only to I²C Port 1 for GMSL2 Link B.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 . . . 0b1111111: Write/read device address is 0xFE/0xFF

I2C_3 (0x693)

BIT	7	6	5	4	3	2	1	0
Field	DST_A_P1_B[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_A_P1_B	7:1	GMSL2 I²C Address Translator Destination A. This setting applies only to I²C Port 1 for GMSL2 Link B. See the description of SRC_A_P1_B.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 . . . 0b1111111: Write/read device address is 0xFE/0xFF

I2C_4 (0x694)

BIT	7	6	5	4	3	2	1	0
Field	SRC_B_P1_B[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_B_P1_B	7:1	GMSL2 I²C Address Translator Source B. When I²C device address matches SRC_B_P1_B, internal I²C main (on the remote side) replaces the device address by DST_B_P1_B. This setting applies only to I²C Port 1 for GMSL2 Link B.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 . . . 0b1111111: Write/read device address is 0xFE/0xFF

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I2C_5 (0x695)

BIT	7	6	5	4	3	2	1	0
Field	DST_B_P1_B[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_B_P1_B	7:1	GMSL2 I²C Address Translator Destination B. This setting applies only to I²C Port 1 for GMSL2 Link B. See the description of SRC_B_P1_B.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 . . . 0b1111111: Write/read device address is 0xFE/0xFF

I2C_0 (0x698)

BIT	7	6	5	4	3	2	1	0
Field	–	–	SLV_SH_P2_B[1:0]		–	SLV_TO_P2_B[2:0]		
Reset	–	–	0x2		–	0x6		
Access Type	–	–	Write, Read		–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
SLV_SH_P2_B	5:4	GMSL2 I²C-to-I²C Subordinate Setup and Hold Time Setting (setup, hold) Configures the interval between SDA and SCL transitions when driven by the internal I²C subordinate. Set this according to the I²C speed mode. This setting applies only to I²C Port 2 for GMSL2 Link B.	0b00: Fast-mode Plus 0b01: Fast-mode 0b10: Standard-mode 0b11: Reserved
SLV_TO_P2_B	2:0	GMSL2 I²C-to-I²C Subordinate Timeout Setting Internal GMSL2 I²C subordinate times out after the configured duration if it does not receive any response while waiting for a packet from the remote device. This setting applies only to I²C Port 2 for GMSL2 Link B.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

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I2C_1 (0x699)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	MST_BT_P2_B[2:0]			–	MST_TO_P2_B[2:0]		
Reset	0x0	0x5			–	0x6		
Access Type		Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
MST_BT_P2_B	6:4	GMSL2 I²C-to-I²C Main Bit Rate Setting Configures the I²C bit rate used by the internal I²C main (in the device on the remote side from the external I²C main). This setting applies only to I²C Port 2 for GMSL2 Link B. Set this according to the I²C speed mode: Fast-mode Plus = 101 to 111 Fast-mode = 010 to 101 Standard-mode = 000 to 010	3b000: 9.92Kbps - Set for I²C Standard-mode speed 3b001: 33.2Kbps - Set for I²C Standard-mode speed 3b010: 99.2Kbps - Set for I²C Standard or Fast-mode speed 3b011: 123Kbps - Set for I²C Fast-mode speed 3b100: 203Kbps - Set for I²C Fast-mode speed 3b101: 397Kbps - Set for I²C Fast or Fast-mode Plus speed 3b110: 625Kbps - Set for I²C Fast or Fast-mode Plus speed 3b111: 980Kbps - Set for I²C Fast-mode Plus speed
MST_TO_P2_B	2:0	GMSL2 I²C-to-I²C Main Timeout Setting Internal GMSL2 I²C main times out after the configured duration if it does not receive any response while waiting for a packet from the remote device. This setting applies only to I²C Port 2 for GMSL2 Link B.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_2 (0x69A)

BIT	7	6	5	4	3	2	1	0
Field	SRC_A_P2_B[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_A_P2_B	7:1	GMSL2 I²C Address Translator Source A. When I²C device address matches SRC_A_P2_B, internal I²C main (on the remote side) replaces the device address by DST_A_P2_B This setting applies only to I²C Port 2 for GMSL2 Link B.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 . . . 0b1111111: Write/read device address is 0xFE/0xFF

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I2C_3 (0x69B)

BIT	7	6	5	4	3	2	1	0
Field	DST_A_P2_B[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_A_P2_B	7:1	GMSL2 I^{2}C Address Translator Destination A. This setting applies only to I^{2}C Port 2 for GMSL2 Link B. See the description of SRC_A_P2_B.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 . . . 0b1111111: Write/read device address is 0xFE/0xFF

I2C_4 (0x69C)

BIT	7	6	5	4	3	2	1	0
Field	SRC_B_P2_B[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_B_P2_B	7:1	GMSL2 I^{2}C Address Translator Source B When I^{2}C device address matches SRC_B_P2_B, internal I^{2}C main (on the remote side) replaces the device address by DST_B_P2_B. This setting applies only to I^{2}C Port 2 for GMSL2 Link B.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 . . . 0b1111111: Write/read device address is 0xFE/0xFF

I2C_5 (0x69D)

BIT	7	6	5	4	3	2	1	0
Field	DST_B_P2_B[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

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BITFIELD	BITS	DESCRIPTION	DECODE
DST_B_P2_B	7:1	GMSL2 I²C Address Translator Destination B. This setting applies only to I²C Port 2 for GMSL2 Link B. See the description of SRC_B_P2_B.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 . . . 0b1111111: Write/read device address is 0xFE/0xFF

I2C_0 (0x6A0)

BIT	7	6	5	4	3	2	1	0
Field	–	–	SLV_SH_P1_C[1:0]		–	SLV_TO_P1_C[2:0]		
Reset	–	–	0x2		–	0x6		
Access Type	–	–	Write, Read		–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
SLV_SH_P1_C	5:4	GMSL2 I²C-to-I²C Subordinate Setup and Hold Time Setting (setup, hold) Configures the interval between SDA and SCL transitions when driven by the internal I²C subordinate. Set this according to the I²C speed mode. This setting applies only to I²C Port 1 for GMSL2 Link C.	0b00: Fast-mode Plus 0b01: Fast-mode 0b10: Standard-mode 0b11: Reserved
SLV_TO_P1_C	2:0	GMSL2 I²C-to-I²C Subordinate Timeout Setting Internal GMSL2 I²C subordinate times out after the configured duration if it does not receive any response while waiting for a packet from the remote device. This setting applies only to I²C Port 1 for GMSL2 Link C.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_1 (0x6A1)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	MST_BT_P1_C[2:0]			–	MST_TO_P1_C[2:0]		
Reset	0x0	0x5			–	0x6		
Access Type		Write, Read			–	Write, Read		

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BITFIELD	BITS	DESCRIPTION	DECODE
MST_BT_P1_C	6:4	GMSL2 I²C-to-I²C Main Bit Rate Setting Configures the I²C bit rate used by the internal I²C main (in the device on the remote side from the external I²C main). This setting applies only to I²C Port 1 for GMSL2 Link C. Set this according to the I²C speed mode: Fast-mode Plus = 101 to 111 Fast-mode = 010 to 101 Standard-mode = 000 to 010	3b000: 9.92Kbps - Set for I²C Standard-mode speed 3b001: 33.2Kbps - Set for I²C Standard-mode speed 3b010: 99.2Kbps - Set for I²C Standard or Fast-mode speed 3b011: 123Kbps - Set for I²C Fast-mode speed 3b100: 203Kbps - Set for I²C Fast-mode speed 3b101: 397Kbps - Set for I²C Fast or Fast-mode Plus speed 3b110: 625Kbps - Set for I²C Fast or Fast-mode Plus speed 3b111: 980Kbps - Set for I²C Fast-mode Plus speed
MST_TO_P1_C	2:0	GMSL2 I²C-to-I²C Main Timeout Setting Internal GMSL2 I²C main times out after the configured duration if it does not receive any response while waiting for a packet from the remote device. This setting applies only to I²C Port 1 for GMSL2 Link C.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_2 (0x6A2)

BIT	7	6	5	4	3	2	1	0
Field	SRC_A_P1_C[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_A_P1_C	7:1	GMSL2 I²C Address Translator Source A. When I²C device address matches SRC_A_P1_C, the internal I²C main (on the remote side) replaces the device address by DST_A_P1_C. This setting applies only to I²C Port 1 for GMSL2 Link C.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 . . . 0b1111111: Write/read device address is 0xFE/0xFF

I2C_3 (0x6A3)

BIT	7	6	5	4	3	2	1	0
Field	DST_A_P1_C[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

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BITFIELD	BITS	DESCRIPTION	DECODE
DST_A_P1_C	7:1	GMSL2 I²C Address Translator Destination A. This setting applies only to I²C Port 1 for GMSL2 Link C. See the description of SRC_A_P1_C.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 . . . 0b1111111: Write/read device address is 0xFE/0xFF

I2C_4 (0x6A4)

BIT	7	6	5	4	3	2	1	0
Field	SRC_B_P1_C[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_B_P1_C	7:1	GMSL2 I²C Address Translator Source B. When I²C device address matches SRC_B_P1_C, internal I²C main (on the remote side) replaces the device address by DST_B_P1_C. This setting applies only to I²C Port 1 for GMSL2 Link C.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 . . . 0b1111111: Write/read device address is 0xFE/0xFF

I2C_5 (0x6A5)

BIT	7	6	5	4	3	2	1	0
Field	DST_B_P1_C[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_B_P1_C	7:1	GMSL2 I²C Address Translator Destination B. This setting applies only to I²C Port 1 for GMSL2 Link C. See the description of SRC_B_P1_C.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 . . . 0b1111111: Write/read device address is 0xFE/0xFF

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I2C_0 (0x6A8)

BIT	7	6	5	4	3	2	1	0
Field	–	–	SLV_SH_P2_C[1:0]		–	SLV_TO_P2_C[2:0]		
Reset	–	–	0x2		–	0x6		
Access Type	–	–	Write, Read		–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
SLV_SH_P2_C	5:4	GMSL2 I²C-to-I²C Subordinate Setup and Hold Time Setting (setup, hold) Configures the interval between SDA and SCL transitions when driven by the internal I²C subordinate. Set this according to the I²C speed mode. This setting applies only to I²C Port 2 for GMSL2 Link C.	0b00: Fast-mode Plus 0b01: Fast-mode 0b10: Standard-mode 0b11: Reserved
SLV_TO_P2_C	2:0	GMSL2 I²C-to-I²C Subordinate Timeout Setting Internal GMSL2 I²C subordinate times out after the configured duration if it does not receive any response while waiting for a packet from the remote device. This setting applies only to I²C Port 2 for GMSL2 Link C.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_1 (0x6A9)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	MST_BT_P2_C[2:0]			–	MST_TO_P2_C[2:0]		
Reset	0x0	0x5			–	0x6		
Access Type		Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
MST_BT_P2_C	6:4	GMSL2 I²C-to-I²C Main Bit Rate Setting Configures the I²C bit rate used by the internal I²C main (in the device on the remote side from the external I²C main). This setting applies only to I²C Port 2 for GMSL2 Link C. Set this according to the I²C speed mode: Fast-mode Plus = 101 to 111 Fast-mode = 010 to 101 Standard-mode = 000 to 010	3b000: 9.92Kbps - Set for I²C Standard-mode speed 3b001: 33.2Kbps - Set for I²C Standard-mode speed 3b010: 99.2Kbps - Set for I²C Standard or Fast-mode speed 3b011: 123Kbps - Set for I²C Fast-mode speed 3b100: 203Kbps - Set for I²C Fast-mode speed 3b101: 397Kbps - Set for I²C Fast or Fast-mode Plus speed 3b110: 625Kbps - Set for I²C Fast or Fast-mode Plus speed 3b111: 980Kbps - Set for I²C Fast-mode Plus speed

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BITFIELD	BITS	DESCRIPTION	DECODE
MST_TO_P2_C	2:0	GMSL2 I²C-to-I²C Main Timeout Setting Internal GMSL2 I²C main times out after the configured duration if it does not receive any response while waiting for a packet from the remote device. This setting applies only to I²C Port 2 for GMSL2 Link C.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_2 (0x6AA)

BIT	7	6	5	4	3	2	1	0
Field	SRC_A_P2_C[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_A_P2_C	7:1	GMSL2 I²C Address Translator Source A. When I²C device address matches SRC_A_P2_C, internal I²C main (on the remote side) replaces the device address by DST_A_P2_C. This setting applies only to I²C Port 2 for GMSL2 Link C.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 . . . 0b1111111: Write/read device address is 0xFE/0xFF

I2C_3 (0x6AB)

BIT	7	6	5	4	3	2	1	0
Field	DST_A_P2_C[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_A_P2_C	7:1	GMSL2 I²C Address Translator Destination A. This setting applies only to I²C Port 2 for GMSL2 Link C. See the description of SRC_A_P2_C.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 . . . 0b1111111: Write/read device address is 0xFE/0xFF

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I2C_4 (0x6AC)

BIT	7	6	5	4	3	2	1	0
Field	SRC_B_P2_C[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_B_P2_C	7:1	GMSL2 I²C Address Translator Source B. When I²C device address matches SRC_B_P2_C, internal I²C main (on the remote side) replaces the device address by DST_B_P2_C. This setting applies only to I²C Port 2 for GMSL2 Link C.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 . . . 0b1111111: Write/read device address is 0xFE/0xFF

I2C_5 (0x6AD)

BIT	7	6	5	4	3	2	1	0
Field	DST_B_P2_C[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_B_P2_C	7:1	GMSL2 I²C address translator destination B. This setting applies only to I²C Port 2 for GMSL2 Link C. See the description of SRC_B_P2_C.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 . . . 0b1111111: Write/read device address is 0xFE/0xFF

I2C_0 (0x6B0)

BIT	7	6	5	4	3	2	1	0
Field	–	–	SLV_SH_P1_D[1:0]		–	SLV_TO_P1_D[2:0]		
Reset	–	–	0x2		–	0x6		
Access Type	–	–	Write, Read		–	Write, Read		

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BITFIELD	BITS	DESCRIPTION	DECODE
SLV_SH_P1_D	5:4	GMSL2 I²C-to-I²C Subordinate Setup and Hold Time Setting (setup, hold) Configures the interval between SDA and SCL transitions when driven by the internal I²C subordinate. Set this according to the I²C speed mode. This setting applies only to I²C Port 1 for GMSL2 Link D.	0b00: Fast-mode Plus 0b01: Fast-mode 0b10: Standard-mode 0b11: Reserved
SLV_TO_P1_D	2:0	GMSL2 I²C-to-I²C Subordinate Timeout Setting Internal GMSL2 I²C subordinate times out after the configured duration if it does not receive any response while waiting for a packet from the remote device. This setting applies only to I²C Port 1 for GMSL2 Link D.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_1 (0x6B1)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	MST_BT_P1_D[2:0]			–	MST_TO_P1_D[2:0]		
Reset	0x0	0x5			–	0x6		
Access Type		Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
MST_BT_P1_D	6:4	GMSL2 I²C-to-I²C Main Bit Rate Setting Configures the I²C bit rate used by the internal I²C main (in the device on the remote side from the external I²C main). This setting applies only to I²C Port 1 for GMSL2 Link D. Set this according to the I²C speed mode: Fast-mode Plus = 101 to 111 Fast-mode = 010 to 101 Standard-mode = 000 to 010	3b000: 9.92Kbps - Set for I²C Standard-mode speed 3b001: 33.2Kbps - Set for I²C Standard-mode speed 3b010: 99.2Kbps - Set for I²C Standard or Fast-mode speed 3b011: 123Kbps - Set for I²C Fast-mode speed 3b100: 203Kbps - Set for I²C Fast-mode speed 3b101: 397Kbps - Set for I²C Fast or Fast-mode Plus speed 3b110: 625Kbps - Set for I²C Fast or Fast-mode Plus speed 3b111: 980Kbps - Set for I²C Fast-mode Plus speed
MST_TO_P1_D	2:0	GMSL2 I²C-to-I²C Main Timeout Setting Internal GMSL2 I²C main times out after the configured duration if it does not receive any response while waiting for a packet from the remote device. This setting applies only to I²C Port 1 for GMSL2 Link D.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

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I2C_2 (0x6B2)

BIT	7	6	5	4	3	2	1	0
Field	SRC_A_P1_D[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_A_P1_D	7:1	GMSL2 I^{2}C Address Translator Source A When I^{2}C device address matches SRC_A_P1_D, internal I^{2}C main (on the remote side) replaces the device address by DST_A_P1_D. This setting applies only to I^{2}C Port 1 for GMSL2 Link D.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 . . . 0b1111111: Write/read device address is 0xFE/0xFF

I2C_3 (0x6B3)

BIT	7	6	5	4	3	2	1	0
Field	DST_A_P1_D[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_A_P1_D	7:1	GMSL2 I^{2}C Address Translator Destination A This setting applies only to I^{2}C Port 1 for GMSL2 Link D. See the description of SRC_A_P1_D.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 . . . 0b1111111: Write/read device address is 0xFE/0xFF

I2C_4 (0x6B4)

BIT	7	6	5	4	3	2	1	0
Field	SRC_B_P1_D[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

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BITFIELD	BITS	DESCRIPTION	DECODE
SRC_B_P1_D	7:1	GMSL2 I²C Address Translator Source B When I²C device address matches SRC_B_P1_D, internal I²C main (on the remote side) replaces the device address by DST_B_P1_D. This setting applies only to I²C Port 1 for GMSL2 Link D.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 . . . 0b1111111: Write/read device address is 0xFE/0xFF

I2C_5 (0x6B5)

BIT	7	6	5	4	3	2	1	0
Field	DST_B_P1_D[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_B_P1_D	7:1	GMSL2 I²C Address Translator Destination B This setting applies only to I²C Port 1 for GMSL2 Link D. See the description of SRC_B_P1_D.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 . . . 0b1111111: Write/read device address is 0xFE/0xFF

I2C_0 (0x6B8)

BIT	7	6	5	4	3	2	1	0
Field	–	–	SLV_SH_P2_D[1:0]		–	SLV_TO_P2_D[2:0]		
Reset	–	–	0x2		–	0x6		
Access Type	–	–	Write, Read		–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
SLV_SH_P2_D	5:4	GMSL2 I²C-to-I²C Subordinate Setup and Hold Time Setting (setup, hold) Configures the interval between SDA and SCL transitions when driven by the internal I²C subordinate. Set this according to the I²C speed mode. This setting applies only to I²C Port 2 for GMSL2 Link D.	0b00: Fast-mode Plus 0b01: Fast-mode 0b10: Standard-mode 0b11: Reserved

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BITFIELD	BITS	DESCRIPTION	DECODE
SLV_TO_P2_D	2:0	GMSL2 I²C-to-I²C Subordinate Timeout Setting Internal GMSL2 I²C subordinate times out after the configured duration if it does not receive any response while waiting for a packet from the remote device. This setting applies only to I²C Port 2 for GMSL2 Link D.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_1 (0x6B9)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	MST_BT_P2_D[2:0]			–	MST_TO_P2_D[2:0]		
Reset	0x0	0x5			–	0x6		
Access Type		Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
MST_BT_P2_D	6:4	GMSL2 I²C-to-I²C Main Bit Rate Setting Configures the I²C bit rate used by the internal I²C main (in the device on the remote side from the external I²C main). This setting applies only to I²C Port 2 for GMSL2 Link D. Set this according to the I²C speed mode: Fast-mode Plus = 101 to 111 Fast-mode = 010 to 101 Standard-mode = 000 to 010	3b000: 9.92Kbps - Set for I²C Standard-mode speed 3b001: 33.2Kbps - Set for I²C Standard-mode speed 3b010: 99.2Kbps - Set for I²C Standard or Fast-mode speed 3b011: 123Kbps - Set for I²C Fast-mode speed 3b100: 203Kbps - Set for I²C Fast-mode speed 3b101: 397Kbps - Set for I²C Fast or Fast-mode Plus speed 3b110: 625Kbps - Set for I²C Fast or Fast-mode Plus speed 3b111: 980Kbps - Set for I²C Fast-mode Plus speed
MST_TO_P2_D	2:0	GMSL2 I²C-to-I²C Main Timeout Setting Internal GMSL2 I²C main times out after the configured duration if it does not receive any response while waiting for a packet from the remote device. This setting applies only to I²C Port 2 for GMSL2 Link D.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_2 (0x6BA)

BIT	7	6	5	4	3	2	1	0
Field	SRC_A_P2_D[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

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BITFIELD	BITS	DESCRIPTION	DECODE
SRC_A_P2_D	7:1	GMSL2 I²C Address Translator Source A When I²C device address matches SRC_A_P2_D, internal I²C main (on the remote side) replaces the device address by DST_A_P2_D. This setting applies only to I²C Port 2 for GMSL2 Link D.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 . . . 0b1111111: Write/read device address is 0xFE/0xFF

I2C_3 (0x6BB)

BIT	7	6	5	4	3	2	1	0
Field	DST_A_P2_D[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_A_P2_D	7:1	GMSL2 I²C Address Translator Destination A. This setting applies only to I²C Port 2 for GMSL2 Link D. See the description of SRC_A_P2_D.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 . . . 0b1111111: Write/read device address is 0xFE/0xFF

I2C_4 (0x6BC)

BIT	7	6	5	4	3	2	1	0
Field	SRC_B_P2_D[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_B_P2_D	7:1	GMSL2 I²C Address Translator Source B When I²C device address matches SRC_B_P2_D, internal I²C main (on the remote side) replaces the device address by DST_B_P2_D. This setting applies only to I²C Port 2 for GMSL2 Link D.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 . . . 0b1111111: Write/read device address is 0xFE/0xFF

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I2C_5 (0x6BD)

BIT	7	6	5	4	3	2	1	0
Field	DST_B_P2_D[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_B_P2_D	7:1	GMSL2 I^{2}C Address Translator Destination B This setting applies only to I^{2}C Port 2 for GMSL2 Link D. See the description of SRC_B_P2_D.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 . . . 0b1111111: Write/read device address is 0xFE/0xFF

CMU2 (0x6C2)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD[2:0]			RSVD	RSVD[1:0]		RSVD
Reset	0x0	0x00			0x00	0x00		0x00
Access Type	Write, Read	Write, Read			Write, Read	Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	Reserved	Must write value of 0.
RSVD	6:4	Reserved	Must write value of 1.
RSVD	3	Reserved	Must write value of 0.
RSVD	2:1	Reserved	Must write value of 0.
RSVD	0	Reserved	Must write value of 0.

CMU4 (0x6C4)

BIT	7	6	5	4	3	2	1	0
Field	A_SPEED[1:0]		B_SPEED[1:0]		C_SPEED[1:0]		D_SPEED[1:0]	
Reset	0b00		0b00		0b00		0b00	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
A_SPEED	7:6	GPIO Slew Rate for MFP10 to MFP12 First value in the table is the typical rise/fall time for V_{DDIO} = 1.8V, second value is for V_{DDIO} = 3.3V.	0b00: 2ns, 1ns 0011: 4ns, 2ns 0b10: 8ns, 4ns 0b11: 16ns, 8ns

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BITFIELD	BITS	DESCRIPTION	DECODE
B_SPEED	5:4	GPIO Slew Rate for MFP8, MFP9, MFP13, and MFP14 First value in the table is the typical rise/fall time for V_{DDIO} = 1.8V, second value is for V_{DDIO} = 3.3V.	0b00: 2ns, 1ns 0b01: 4ns, 2ns 0b10: 8ns, 4ns 0b11: 16ns, 8ns
C_SPEED	3:2	GPIO Slew Rate for MFP5 to MFP7 First value in the table is the typical rise/fall time for V_{DDIO} = 1.8V, second value is for V_{DDIO} = 3.3V.	0b00: 2ns, 1ns 0b01: 4ns, 2ns 0b10: 8ns, 4ns 0b11: 16ns, 8ns
D_SPEED	1:0	GPIO Slew Rate for MFP0 to MFP4 First value in the table is the typical rise/fall time for V_{DDIO} = 1.8V, second value is for V_{DDIO} = 3.3V.	0b00: 2ns, 1ns 0b01: 4ns, 2ns 0b10: 8ns, 4ns 0b11: 16ns, 8ns

DP_ORSTB_CTL (0x6DF)

BIT	7	6	5	4	3	2	1	0
Field	–	DP_RST_MIPI3	DP_RST_STABLE	DP_RST_MIPI2	DP_RST_MIPI	DP_RST_VP	DP_RST_FS	DP_RST_CC
Reset	–	0x1	0x1	0x0	0x0	0x0	0x0	0x0
Access Type	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DP_RST_MIPI3	6	Selects RST mode CMD FIFO read pointer	0b0: Rev B behavior – CMD FIFO read pointer is not reset automatically when video lock is lost 0b1: (Default) Rev C behavior – CMD FIFO read pointer is reset automatically when video lock is lost
DP_RST_STABLE	5	Selects RST mode	0b0: Do not prevent reset glitches when changing reset behavior between individualized resets (Rev C behavior) vs. non-individualized resets (Rev B behavior) 0b1: (Default) Prevent reset glitches when changing reset behavior between individualized resets (Rev C behavior) vs. non-individualized resets (Rev B behavior)
DP_RST_MIPI2	4	Selects RST mode to MIPI controllers.	0b0: (Default) Rev B behavior – All MIPI controllers will be reset during any one-shot reset or link reset 0b1: Rev C behavior – Each MIPI controller can be reset automatically based on the associated GMSL PHY and Video Pipe reset during a one-shot reset or link reset
DP_RST_MIPI	3	Selects RST mode to MIPI controllers.	0b0: (Default) Rev B behavior – All MIPI controllers will be reset during any one-shot reset or link reset 0b1: Rev C behavior – Each MIPI controller can be reset individually based on RST_MIPITX_LOC[3:0] (0x8C9)

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BITFIELD	BITS	DESCRIPTION	DECODE
DP_RST_VP	2	Selects RST mode to video_rx, vrx blocks.	0b0: (Default) Rev B behavior – All video pipes will be reset during any one-shot reset or link reset 0b1: Rev C behavior – Each video pipe will be reset individually based on the associated GMSL PHY reset during a one-shot reset or link reset
DP_RST_FS	1	Selects reset mode to frame sync block	0b0: (Default) Rev B behavior – Frame sync block will be reset during any one-shot reset or link reset 0b1: Rev C behavior – The internal frame sync block will not be reset during a one-shot reset or link reset
DP_RST_CC	0	Selects reset mode for iic_mux_uart blocks	0b0: (Default) Rev B behavior – All I^2C/UART ports will be reset during any one-shot reset or link reset 0b1: Rev C behavior – Each I^2C/UART port will be reset individually based on the associated GMSL PHY reset during a one-shot reset or link reset

MIPI_TX_EXT0 (0x800, 0x810, 0x820, 0x830, 0x840, 0x850, 0x860, 0x870)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_0_H[2:0]			MAP_DST_0_H[2:0]			–	–
Reset	0x0			0x0			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_0_H	7:5	Video Pipe Extended VC Source Mapping register 0: Most Significant 3 bits of Virtual Channel (VC) Source Mapping register, MAP_SRC_0, for use in VC extended mode. See MAP_SRC_0 register associated with this Video Pipe. Incoming Video streams whose VC and Data Type match this setting are mapped to the VC and Data Type programmed in MAP_DST_0_H. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source part of the 0th mapping pair.	0bXXX: MS 3 bits of VC mapping for MAP_SRC_0

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BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_0_H	4:2	Video Pipe Extended VC Destination Mapping register 0: Most Significant 3 bits of Virtual Channel (VC) Destination mapping register, MAP_DST_0, for use in VC extended mode. See MAP_DST_0 register associated with this Video Pipe. This setting provides the corresponding destination map associated with the MAP_SRC_0_H register. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination part of the 0th mapping pair.	0bXXX: MS 3 bits of VC destination mapping for MAP_DST_0

MIPI_TX_EXT1 (0x801, 0x811, 0x821, 0x831, 0x841, 0x851, 0x861, 0x871)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_1_H[2:0]			MAP_DST_1_H[2:0]			–	–
Reset	0x0			0x0			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_1_H	7:5	Video Pipe Extended VC Source Mapping register 1: Most Significant 3 bits of Virtual Channel (VC) Source Mapping register, MAP_SRC_1, for use in VC extended mode. See MAP_SRC_1 register associated with this Video Pipe. Incoming Video streams whose VC and Data Type match this setting are mapped to the VC and Data Type programmed in MAP_DST_1_H. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source part of the 1st mapping pair.	0bXXX: MS 3 bits of VC mapping for MAP_SRC_1

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BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_1_H	4:2	Video Pipe Extended VC Destination Mapping register 1: Most Significant 3 bits of Virtual Channel (VC) Destination mapping register, MAP_DST_1, for use in VC extended mode. See MAP_DST_1 register associated with this Video Pipe. This setting provides the corresponding destination map associated with the MAP_SRC_1_H register. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination part of the 1st mapping pair.	0bXXX: MS 3 bits of VC destination mapping for MAP_DST_1

MIPI_TX_EXT2 (0x802, 0x812, 0x822, 0x832, 0x842, 0x852, 0x862, 0x872)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_2_H[2:0]			MAP_DST_2_H[2:0]			–	–
Reset	0x0			0x0			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_2_H	7:5	Video Pipe Extended VC Source Mapping register 2: Most Significant 3 bits of Virtual Channel (VC) Source Mapping register, MAP_SRC_2, for use in VC extended mode. See MAP_SRC_2 register associated with this Video Pipe. Incoming Video streams whose VC and Data Type match this setting are mapped to the VC and Data Type programmed in MAP_DST_2_H. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source part of the 2nd mapping pair.	0bXXX: MS 3 bits of VC mapping for MAP_SRC_2

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BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_2_H	4:2	Video Pipe Extended VC Destination Mapping register 2: Most Significant 3 bits of Virtual Channel (VC) Destination mapping register, MAP_DST_2, for use in VC extended mode. See MAP_DST_2 register associated with this Video Pipe. This setting provides the corresponding destination map associated with the MAP_SRC_2_H register. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination part of the 2nd mapping pair.	0bXXX: MS 3 bits of VC destination mapping for MAP_DST_2

MIPI_TX_EXT3 (0x803, 0x813, 0x823, 0x833, 0x843, 0x853, 0x863, 0x873)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_3_H[2:0]			MAP_DST_3_H[2:0]			–	–
Reset	0x0			0x0			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_3_H	7:5	Video Pipe Extended VC Source Mapping register 3: Most Significant 3 bits of Virtual Channel (VC) Source Mapping register, MAP_SRC_3, for use in VC extended mode. See MAP_SRC_3 register associated with this Video Pipe. Incoming Video streams whose VC and Data Type match this setting are mapped to the VC and Data Type programmed in MAP_DST_3_H. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source part of the 3rd mapping pair.	0bXXX: MS 3 bits of VC mapping for MAP_SRC_3

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BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_3_H	4:2	Video Pipe Extended VC Destination Mapping register 3: Most Significant 3 bits of Virtual Channel (VC) Destination mapping register, MAP_DST_3, for use in VC extended mode. See MAP_DST_3 register associated with this Video Pipe. This setting provides the corresponding destination map associated with the MAP_SRC_3_H register. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination part of the 3rd mapping pair.	0bXXX: MS 3 bits of VC destination mapping for MAP_DST_3

MIPI_TX_EXT4 (0x804, 0x814, 0x824, 0x834, 0x844, 0x854, 0x864, 0x874)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_4_H[2:0]			MAP_DST_4_H[2:0]			–	–
Reset	0x0			0x0			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_4_H	7:5	Video Pipe Extended VC Source Mapping register 4: Most Significant 3 bits of Virtual Channel (VC) Source Mapping register, MAP_SRC_4, for use in VC extended mode. See MAP_SRC_4 register associated with this Video Pipe. Incoming Video streams whose VC and Data Type match this setting are mapped to the VC and Data Type programmed in MAP_DST_4_H. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source part of the 4th mapping pair.	0bXXX: MS 3 bits of VC mapping for MAP_SRC_4

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BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_4_H	4:2	Video Pipe Extended VC Destination Mapping register 4: Most Significant 3 bits of Virtual Channel (VC) Destination mapping register, MAP_DST_4, for use in VC extended mode. See MAP_DST_4 register associated with this Video Pipe. This setting provides the corresponding destination map associated with the MAP_SRC_4_H register. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination part of the 4th mapping pair.	0bXXX: MS 3 bits of VC destination mapping for MAP_DST_4

MIPI_TX_EXT5 (0x805, 0x815, 0x825, 0x835, 0x845, 0x855, 0x865, 0x875)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_5_H[2:0]			MAP_DST_5_H[2:0]			–	–
Reset	0x0			0x0			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_5_H	7:5	Video Pipe Extended VC Source Mapping register 5: Most Significant 3 bits of Virtual Channel (VC) Source Mapping register, MAP_SRC_5, for use in VC extended mode. See MAP_SRC_5 register associated with this Video Pipe. Incoming Video streams whose VC and Data Type match this setting are mapped to the VC and Data Type programmed in MAP_DST_5_H. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source part of the 5th mapping pair.	0bXXX: MS 3 bits of VC mapping for MAP_SRC_5

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BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_5_H	4:2	Video Pipe Extended VC Destination Mapping register 5: Most Significant 3 bits of Virtual Channel (VC) Destination mapping register, MAP_DST_5, for use in VC extended mode. See MAP_DST_5 register associated with this Video Pipe. This setting provides the corresponding destination map associated with the MAP_SRC_5_H register. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination part of the 5th mapping pair.	0bXXX: MS 3 bits of VC destination mapping for MAP_DST_5

MIPI_TX_EXT6 (0x806, 0x816, 0x826, 0x836, 0x846, 0x856, 0x866, 0x876)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_6_H[2:0]			MAP_DST_6_H[2:0]			–	–
Reset	0x0			0x0			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_6_H	7:5	Video Pipe Extended VC Source Mapping register 6: Most Significant 3 bits of Virtual Channel (VC) Source Mapping register, MAP_SRC_6, for use in VC extended mode. See MAP_SRC_6 register associated with this Video Pipe. Incoming Video streams whose VC and Data Type match this setting are mapped to the VC and Data Type programmed in MAP_DST_6_H. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source part of the 6th mapping pair.	0bXXX: MS 3 bits of VC mapping for MAP_SRC_6

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BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_6_H	4:2	Video Pipe Extended VC Destination Mapping register 6: Most Significant 3 bits of Virtual Channel (VC) Destination mapping register, MAP_DST_6, for use in VC extended mode. See MAP_DST_6 register associated with this Video Pipe. This setting provides the corresponding destination map associated with the MAP_SRC_6_H register. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination part of the 6th mapping pair.	0bXXX: MS 3 bits of VC destination mapping for MAP_DST_6

MIPI_TX_EXT7 (0x807, 0x817, 0x827, 0x837, 0x847, 0x857, 0x867, 0x877)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_7_H[2:0]			MAP_DST_7_H[2:0]			–	–
Reset	0x0			0x0			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_7_H	7:5	Video Pipe Extended VC Source Mapping register 7: Most Significant 3 bits of Virtual Channel (VC) Source Mapping register, MAP_SRC_7, for use in VC extended mode. See MAP_SRC_7 register associated with this Video Pipe. Incoming Video streams whose VC and Data Type match this setting are mapped to the VC and Data Type programmed in MAP_DST_7_H. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source part of the 7th mapping pair.	0bXXX: MS 3 bits of VC mapping for MAP_SRC_7

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BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_7_H	4:2	Video Pipe Extended VC Destination Mapping register 7: Most Significant 3 bits of Virtual Channel (VC) Destination mapping register, MAP_DST_7, for use in VC extended mode. See MAP_DST_7 register associated with this Video Pipe. This setting provides the corresponding destination map associated with the MAP_SRC_7_H register. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination part of the 7th mapping pair.	0bXXX: MS 3 bits of VC destination mapping for MAP_DST_7

MIPI_TX_EXT8 (0x808, 0x818, 0x828, 0x838, 0x848, 0x858, 0x868, 0x878)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_8_H[2:0]			MAP_DST_8_H[2:0]			–	–
Reset	0x0			0x0			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_8_H	7:5	Video Pipe Extended VC Source Mapping register 8: Most Significant 3 bits of Virtual Channel (VC) Source Mapping register, MAP_SRC_8, for use in VC extended mode. See MAP_SRC_8 register associated with this Video Pipe. Incoming Video streams whose VC and Data Type match this setting are mapped to the VC and Data Type programmed in MAP_DST_8_H. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source part of the 8th mapping pair.	0bXXX: MS 3 bits of VC mapping for MAP_SRC_8

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BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_8_H	4:2	Video Pipe Extended VC Destination Mapping register 8: Most Significant 3 bits of Virtual Channel (VC) Destination mapping register, MAP_DST_8, for use in VC extended mode. See MAP_DST_8 register associated with this Video Pipe. This setting provides the corresponding destination map associated with the MAP_SRC_8_H register. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination part of the 8th mapping pair.	0XXX: MS 3 bits of VC destination mapping for MAP_DST_8

MIPI_TX_EXT9 (0x809, 0x819, 0x829, 0x839, 0x849, 0x859, 0x869, 0x879)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_9_H[2:0]			MAP_DST_9_H[2:0]			–	–
Reset	0x0			0x0			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_9_H	7:5	Video Pipe Extended VC Source Mapping register 9: Most Significant 3 bits of Virtual Channel (VC) Source Mapping register, MAP_SRC_9, for use in VC extended mode. See MAP_SRC_9 register associated with this Video Pipe. Incoming Video streams whose VC and Data Type match this setting are mapped to the VC and Data Type programmed in MAP_DST_9_H. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source part of the 9th mapping pair.	0bXXX: MS 3 bits of VC mapping for MAP_SRC_9

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BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_9_H	4:2	Video Pipe Extended VC Destination Mapping register 9: Most Significant 3 bits of Virtual Channel (VC) Destination mapping register, MAP_DST_9, for use in VC extended mode. See MAP_DST_9 register associated with this Video Pipe. This setting provides the corresponding destination map associated with the MAP_SRC_9_H register. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination part of the 9th mapping pair.	0bXXX: MS 3 bits of VC destination mapping for MAP_DST_9

MIPI_TX_EXT10 (0x80A, 0x81A, 0x82A, 0x83A, 0x84A, 0x85A, 0x86A, 0x87A)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_10_H[2:0]			MAP_DST_10_H[2:0]			–	–
Reset	0x0			0x0			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_10_H	7:5	Video Pipe Extended VC Source Mapping register 10: Most Significant 3 bits of Virtual Channel (VC) Source Mapping register, MAP_SRC_10, for use in VC extended mode. See MAP_SRC_10 register associated with this Video Pipe. Incoming Video streams whose VC and Data Type match this setting are mapped to the VC and Data Type programmed in MAP_DST_10_H. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source part of the 10th mapping pair.	0bXXX: MS 3 bits of VC mapping for MAP_SRC_10

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BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_10_H	4:2	Video Pipe Extended VC Destination Mapping register 10: Most Significant 3 bits of Virtual Channel (VC) Destination mapping register, MAP_DST_10, for use in VC extended mode. See MAP_DST_10 register associated with this Video Pipe. This setting provides the corresponding destination map associated with the MAP_SRC_10_H register. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination part of the 10th mapping pair.	0bXXX: MS 3 bits of VC destination mapping for MAP_DST_10

MIPI_TX_EXT11 (0x80B, 0x81B, 0x82B, 0x83B, 0x84B, 0x85B, 0x86B, 0x87B)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_11_H[2:0]			MAP_DST_11_H[2:0]			–	–
Reset	0x0			0x0			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_11_H	7:5	Video Pipe Extended VC Source Mapping register 11: Most Significant 3 bits of Virtual Channel (VC) Source Mapping register, MAP_SRC_11, for use in VC extended mode. See MAP_SRC_11 register associated with this Video Pipe. Incoming Video streams whose VC and Data Type match this setting are mapped to the VC and Data Type programmed in MAP_DST_11_H. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source part of the 11th mapping pair.	0bXXX: MS 3 bits of VC mapping for MAP_SRC_11

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BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_11_H	4:2	Video Pipe Extended VC Destination Mapping register 11: Most Significant 3 bits of Virtual Channel (VC) Destination mapping register, MAP_DST_11, for use in VC extended mode. See MAP_DST_11 register associated with this Video Pipe. This setting provides the corresponding destination map associated with the MAP_SRC_11_H register. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination part of the 11th mapping pair.	0bXXX: MS 3 bits of VC destination mapping for MAP_DST_11

MIPI_TX_EXT12 (0x80C, 0x81C, 0x82C, 0x83C, 0x84C, 0x85C, 0x86C, 0x87C)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_12_H[2:0]			MAP_DST_12_H[2:0]			–	–
Reset	0x0			0x0			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_12_H	7:5	Video Pipe Extended VC Source Mapping register 12: Most Significant 3 bits of Virtual Channel (VC) Source Mapping register, MAP_SRC_12, for use in VC extended mode. See MAP_SRC_12 register associated with this Video Pipe. Incoming Video streams whose VC and Data Type match this setting are mapped to the VC and Data Type programmed in MAP_DST_12_H. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source part of the 12th mapping pair.	0bXXX: MS 3 bits of VC mapping for MAP_SRC_12

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BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_12_H	4:2	Video Pipe Extended VC Destination Mapping register 12: Most Significant 3 bits of Virtual Channel (VC) Destination mapping register, MAP_DST_12, for use in VC extended mode. See MAP_DST_12 register associated with this Video Pipe. This setting provides the corresponding destination map associated with the MAP_SRC_12_H register. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination part of the 12th mapping pair.	0bXXX: MS 3 bits of VC destination mapping for MAP_DST_12

MIPI_TX_EXT13 (0x80D, 0x81D, 0x82D, 0x83D, 0x84D, 0x85D, 0x86D, 0x87D)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_13_H[2:0]			MAP_DST_13_H[2:0]			–	–
Reset	0x0			0x0			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_13_H	7:5	Video Pipe Extended VC Source Mapping register 13: Most Significant 3 bits of Virtual Channel (VC) Source Mapping register, MAP_SRC_13, for use in VC extended mode. See MAP_SRC_13 register associated with this Video Pipe. Incoming Video streams whose VC and Data Type match this setting are mapped to the VC and Data Type programmed in MAP_DST_13_H. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source part of the 13th mapping pair.	0bXXX: MS 3 bits of VC mapping for MAP_SRC_13

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BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_13_H	4:2	Video Pipe Extended VC Destination Mapping register 13: Most Significant 3 bits of Virtual Channel (VC) Destination mapping register, MAP_DST_13, for use in VC extended mode. See MAP_DST_13 register associated with this Video Pipe. This setting provides the corresponding destination map associated with the MAP_SRC_13_H register. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination part of the 13th mapping pair.	0bXXX: MS 3 bits of VC destination mapping for MAP_DST_13

MIPI_TX_EXT14 (0x80E, 0x81E, 0x82E, 0x83E, 0x84E, 0x85E, 0x86E, 0x87E)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_14_H[2:0]			MAP_DST_14_H[2:0]			–	–
Reset	0x0			0x0			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_14_H	7:5	Video Pipe Extended VC Source Mapping register 14: Most Significant 3 bits of Virtual Channel (VC) Source Mapping register, MAP_SRC_14, for use in VC extended mode. See MAP_SRC_14 register associated with this Video Pipe. Incoming Video streams whose VC and Data Type match this setting are mapped to the VC and Data Type programmed in MAP_DST_14_H. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source part of the 14th mapping pair.	0bXXX: MS 3 bits of VC mapping for MAP_SRC_14

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BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_14_H	4:2	Video Pipe Extended VC Destination Mapping register 14: Most Significant 3 bits of Virtual Channel (VC) Destination mapping register, MAP_DST_14, for use in VC extended mode. See MAP_DST_14 register associated with this Video Pipe. This setting provides the corresponding destination map associated with the MAP_SRC_14_H register. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination part of the 14th mapping pair.	0bXXX: MS 3 bits of VC destination mapping for MAP_DST_14

MIPI_TX_EXT15 (0x80F, 0x81F, 0x82F, 0x83F, 0x84F, 0x85F, 0x86F, 0x87F)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_15_H[2:0]			MAP_DST_15_H[2:0]			–	–
Reset	0x0			0x0			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_15_H	7:5	Video Pipe Extended VC Source Mapping register 15: Most Significant 3 bits of Virtual Channel (VC) Source Mapping register, MAP_SRC_15, for use in VC extended mode. See MAP_SRC_15 register associated with this Video Pipe. Incoming Video streams whose VC and Data Type match this setting are mapped to the VC and Data Type programmed in MAP_DST_15_H. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source part of the 15th mapping pair.	0bXXX: MS 3 bits of VC mapping for MAP_SRC_15

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BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_15_H	4:2	Video Pipe Extended VC Destination Mapping register 15: Most Significant 3 bits of Virtual Channel (VC) Destination mapping register, MAP_DST_15, for use in VC extended mode. See MAP_DST_15 register associated with this Video Pipe. This setting provides the corresponding destination map associated with the MAP_SRC_15_H register. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination part of the 15th mapping pair.	0bXXX: MS 3 bits of VC destination mapping for MAP_DST_15

MIPI_PHY0 (0x8A0)

BIT	7	6	5	4	3	2	1	0
Field	force_csi_out_en	force_clk3_en	force_clk0_en	phy_1x4b_22	phy_1x4a_22	phy_2x4	RSVD	phy_4x2
Reset	0b0	0b0	0b0	0b0	0b0	0b1	0x0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
force_csi_out_en	7	Set to force all MIPI clocks running.	0b0: Normal mode 0b1: Force all MIPI clocks running
force_clk3_en	6	Set to force PHY3 MIPI clock running.	0b0: DPHY3 not enabled as clock 0b1: DPHY3 enabled as clock
force_clk0_en	5	Set to force PHY0 MIPI clock running.	0b0: DPHY0 not enabled as clock 0b1: DPHY0 not enabled as clock
phy_1x4b_22	4	MIPI PHY 1x4b + 2x2 mode: MIPI output configured as one 4-lane port and two 2-lane ports. PHY2 and PHY3 combined as 4-lane. PHY0 and PHY1 are 2-lane ports.	0b0: 1x4b_22 not selected 0b1: 1x4b_22 selected
phy_1x4a_22	3	MIPI PHY 1x4a + 2x2 mode: MIPI output configured as one 4-lane port and two 2-lane ports. PHY0 and PHY1 combined as 4-lane. PHY2 and PHY3 are 2-lane ports.	0b0: 1x4a_22 not selected 0b1: 1x4a_22 selected
phy_2x4	2	MIPI PHY 2x4 mode: MIPI output configured as two ports with four data lanes each. PHY0 and PHY1 combined, and PHY2 and PHY3 combined.	0b0: 2x4 not selected 0b1: 2x4 selected
phy_4x2	0	MIPI PHY 4x2 mode: MIPI output configured as four 2-lane MIPI ports.	0b0: 4x2 configuration not selected 0b1: 4x2 configuration selected

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MIPI_PHY1 (0x8A1)

BIT	7	6	5	4	3	2	1	0
Field	t_hs_przero[1:0]		t_hs_prep[1:0]		t_clk_trail[1:0]		t_clk_przero[1:0]	
Reset	0x0		0x0		0x0		0x0	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
t_hs_przero	7:6	Typical DPHY data lane HS_prep + HS_zero timing	0b00: 146ns + 24UI 0b01: 160ns + 24UI 0b10: 173ns + 24UI 0b11: 200ns + 24UI
t_hs_prep	5:4	Typical DPHY data lane HS_prepare timing	0b00: 46.7ns + 4UI 0b01: 53.4ns + 4UI 0b10: 60.0ns + 4UI 0b11: 66.7ns + 4UI
t_clk_trail	3:2	Typical DPHY clock HS_trail timing	0b00: 160ns 0b01: 167ns 0b10: 173ns 0b11: 180ns
t_clk_przero	1:0	Typical DPHY clock lane HS_prepare + HS_zero timing	0b00: 306ns 0b01: 600ns 0b10: 900ns 0b11: 1200ns

MIPI_PHY2 (0x8A2)

BIT	7	6	5	4	3	2	1	0
Field	phy_Stdby_n[3:0]				t_lpx[1:0]		t_hs_trail[1:0]	
Reset	0xF				0x1		0x0	
Access Type	Write, Read				Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
phy_Stdby_n	7:4	MIPI PHY Enable bit [7]: Enable MIPI PHY3 bit [6]: Enable MIPI PHY2 bit [5]: Enable MIPI PHY1 bit [4]: Enable MIPI PHY0	0bXXX0: Put MIPI PHY0 in standby mode 0bXXX1: Enable MIPI PHY0 0bXX0X: Put MIPI PHY1 in standby mode 0bXX1X: Enable MIPI PHY1 0bX0XX: Put MIPI PHY2 in standby mode 0bX1XX: Enable MIPI PHY2 0b0XXX: Put MIPI PHY3 in standby mode 0b1XXX: Enable MIPI PHY3
t_lpx	3:2	Typical DPHY Tlpx timing	0b00: 53.4ns 0b01: 106.7ns 0b10: 160ns 0b11: 213.4ns
t_hs_trail	1:0	Typical DPHY data lane HS_trail timing	0b00: 66.7ns + 8UI 0b01: 80ns + 8UI 0b10: 93.4ns + 8UI 0b11: 106.7ns + 8UI

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MIPI_PHY3 (0x8A3)

BIT	7	6	5	4	3	2	1	0
Field	phy1_lane_map[3:0]				phy0_lane_map[3:0]			
Reset	0x4				0xE			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
phy1_lane_map	7:4	MIPI PHY1 lane mapping register: bits [5:4]: Set PHY1 D0 Output mapping bits [7:6]: Set PHY1 D1 Output mapping The settings for these bit fields are dependent upon the settings for the MIPI configuration (see register fields at Address 0x8A0) For MIPI configurations 4x2 and (1x4b+2x2), the following mappings apply: 2'b00 = Map PHY Output to data lane D0 2'b01 = Map PHY Output to data lane D1 2'b10 = Map PHY Output to data lane D2 2'b11 = Map PHY Output to data lane D3 Note: CSI-2 Controller 1 is mapped to PHY1 for MIPI configurations 4x2 and (1x4b+2x2). For MIPI configurations 2x4 and (1x4a+2x2), the following mappings apply: 2'b00 = Map PHY Output to data lane D0 2'b01 = Map PHY Output to data lane D1 2'b10 = Map PHY Output to data lane D2 2'b11 = Map PHY Output to data lane D3 Note: CSI-2 Controller 1 is mapped to both PHY0 and PHY1 for MIPI configurations 2x4 and (1x4a+2x2). CSI-2 Controller 0 is unused.	0bXX00: Map D0 to data lane D0 0bXX01: Map D0 to data lane D1 0bXX10: Map D0 to data lane D2 0bXX11: Map D0 to data lane D3 0b00XX: Map D1 to data lane D0 0b01XX: Map D1 to data lane D1 0b10XX: Map D1 to data lane D2 0b11XX: Map D1 to data lane D3

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BITFIELD	BITS	DESCRIPTION	DECODE
phy0_lane_map	3:0	MIPI PHY0 lane mapping register: bits [1:0]: Set PHY0 D0 Output mapping bits [3:2]: Set PHY0 D1 Output mapping The settings for these bit fields are dependent upon the settings for the MIPI configuration (see register fields at Address 0x8A0). For MIPI configurations 4x2 and (1x4b+2x2), the following mappings apply: 2'b00 = Map PHY Output to data lane D0 2'b01 = Map PHY Output to data lane D1 2'b10 = RSVD, do not use 2'b11 = RSVD, do not use Note: CSI-2 Controller 0 is mapped to PHY0 for MIPI configurations 4x2 and (1x4b+2x2). For MIPI configurations 2x4 and (1x4a+2x2), the following mappings apply: 2'b00 = Map PHY Output to data lane D0 2'b01 = Map PHY Output to data lane D1 2'b10 = Map PHY Output to data lane D2 2'b11 = Map PHY Output to data lane D3 Note: CSI-2 Controller 1 is mapped to both PHY0 and PHY1 for MIPI configurations 2x4 and (1x4a+2x2). CSI-2 Controller 0 is unused.	0bXX00: Map D0 to data lane D0 0bXX01: Map D0 to data lane D1 0bXX10: Map D0 to data lane D2 0bXX11: Map D0 to data lane D3 0b00XX: Map D1 to data lane D0 0b01XX: Map D1 to data lane D1 0b10XX: Map D1 to data lane D2 0b11XX: Map D1 to data lane D3

MIPI_PHY4 (0x8A4)

BIT	7	6	5	4	3	2	1	0
Field	phy3_lane_map[3:0]				phy2_lane_map[3:0]			
Reset	0xE				0x4			
Access Type	Write, Read				Write, Read			

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BITFIELD	BITS	DESCRIPTION	DECODE
phy3_lane_map	7:4	MIPI PHY3 lane mapping register: bits [5:4]: Set PHY3 D0 Output mapping bits [7:6]: Set PHY3 D1 Output mapping The settings for these bit fields are dependent upon the settings for the MIPI configuration (see register fields at Address 0x8A0). For MIPI configurations 4x2 and (1x4a+2x2), the following mappings apply: 2'b00 = Map PHY Output to data lane D0 2'b01 = Map PHY Output to data lane D1 2'b10 = RSVD, do not use 2'b11 = RSVD, do not use Note: CSI-2 Controller 3 is mapped to PHY3 for MIPI configurations 4x2 and (1x4a+2x2). For MIPI configurations 2x4 and (1x4b+2x2), the following mappings apply: 2'b00 = Map PHY Output to data lane D0 2'b01 = Map PHY Output to data lane D1 2'b10 = Map PHY Output to data lane D2 2'b11 = Map PHY Output to data lane D3 Note: CSI-2 Controller 2 is mapped to both PHY2 and PHY3 for MIPI configurations 2x4 and (1x4b+2x2). CSI-2 Controller 3 is unused.	0bXX00: Map D0 to data lane D0 0bXX01: Map D0 to data lane D1 0bXX10: Map D0 to data lane D2 0bXX11: Map D0 to data lane D3 0b00XX: Map D1 to data lane D0 0b01XX: Map D1 to data lane D1 0b10XX: Map D1 to data lane D2 0b11XX: Map D1 to data lane D3
phy2_lane_map	3:0	MIPI PHY2 lane mapping register: bits [1:0]: Set PHY2 D0 Output mapping bits [3:2]: Set PHY2 D1 Output mapping The settings for these bit fields are dependent upon the settings for the MIPI configuration (see register fields at Address 0x8A0) For MIPI configurations 4x2 and (1x4a+2x2), the following mappings apply: 2'b00 = Map PHY Output to data lane D0 2'b01 = Map PHY Output to data lane D1 2'b10 = Map PHY Output to data lane D2 2'b11 = Map PHY Output to data lane D3 Note: CSI-2 Controller 2 is mapped to PHY2 for MIPI configurations 4x2 and (1x4a+2x2). For MIPI configurations 2x4 and (1x4b+2x2), the following mappings apply: 2'b00 = Map PHY Output to data lane D0 2'b01 = Map PHY Output to data lane D1 2'b10 = Map PHY Output to data lane D2 2'b11 = Map PHY Output to data lane D3 Note: CSI-2 Controller 2 is mapped to both PHY2 and PHY3 for MIPI configurations 2x4 and (1x4b+2x2). CSI-2 Controller 3 is unused.	0bXX00: Map D0 to data lane D0 0bXX01: Map D0 to data lane D1 0bXX10: Map D0 to data lane D2 0bXX11: Map D0 to data lane D3 0b00XX: Map D1 to data lane D0 0b01XX: Map D1 to data lane D1 0b10XX: Map D1 to data lane D2 0b11XX: Map D1 to data lane D3

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MIPI_PHY5 (0x8A5)

BIT	7	6	5	4	3	2	1	0
Field	t_clk_prep[1:0]		phy1_pol_map[2:0]			phy0_pol_map[2:0]		
Reset	0x0		0x0			0x0		
Access Type	Write, Read		Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
t_clk_prep	7:6	Typical DPHY clock lane HS_prepare timing	0b00: 40ns 0b01: 46.7ns 0b10: 53.4ns 0b11: 60ns
phy1_pol_map	5:3	MIPI PHY1 lane polarity register: bit [5]: Set polarity on PHY1 CLK lane bit [4]: Set polarity on PHY1 D1 lane bit [3]: Set polarity on PHY1 D0 lane 1'b0 = normal polarity, 1'b1 = inversed polarity	0bXX0: D0 normal polarity, P is positive, N is negative 0bXX1: D0 inverse polarity, P is negative, N is positive 0bX0X: D1 normal polarity, P is positive, N is negative 0bX1X: D1 inverse polarity, P is negative, N is positive 0b0XX: CK normal polarity, P is positive, N is negative 0b1XX: CK inverse polarity, P is negative, N is positive
phy0_pol_map	2:0	MIPI PHY0 lane polarity register: bit [2]: Set polarity on PHY0 CLK lane bit [1]: Set polarity on PHY0 D1 lane bit [0]: Set polarity on PHY0 D0 lane 1'b0 = normal polarity, 1'b1 = inversed polarity	0bXX0: D0 normal polarity, P is positive, N is negative 0bXX1: D0 inverse polarity, P is negative, N is positive 0bX0X: D1 normal polarity, P is positive, N is negative 0bX1X: D1 inverse polarity, P is negative, N is positive 0b0XX: CK normal polarity, P is positive, N is negative 0b1XX: CK inverse polarity, P is negative, N is positive

MIPI_PHY6 (0x8A6)

BIT	7	6	5	4	3	2	1	0
Field	–	–	phy3_pol_map[2:0]			phy2_pol_map[2:0]		
Reset	–	–	0x0			0x0		
Access Type	–	–	Write, Read			Write, Read		

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BITFIELD	BITS	DESCRIPTION	DECODE
phy3_pol_map	5:3	MIPI PHY3 lane polarity register: bit [5]: Set polarity on PHY3 CLK lane bit [4]: Set polarity on PHY3 D1 lane bit [3]: Set polarity on PHY3 D0 lane 1'b0 = normal polarity, 1'b1 = inversed polarity	0bXX0: D0 normal polarity, P is positive, N is negative 0bXX1: D0 inverse polarity, P is negative, N is positive 0bX0X: D1 normal polarity, P is positive, N is negative 0bX1X: D1 inverse polarity, P is negative, N is positive 0b0XX: CK normal polarity, P is positive, N is negative 0b1XX: CK inverse polarity, P is negative, N is positive
phy2_pol_map	2:0	MIPI PHY2 lane polarity register: bit [2]: Set polarity on PHY2 CLK lane bit [1]: Set polarity on PHY2 D1 lane bit [0]: Set polarity on PHY2 D0 lane 1'b0 = normal polarity, 1'b1 = inversed polarity	0bXX0: D0 normal polarity, P is positive, N is negative 0bXX1: D0 inverse polarity, P is negative, N is positive 0bX0X: D1 normal polarity, P is positive, N is negative 0bX1X: D1 inverse polarity, P is negative, N is positive 0b0XX: CK normal polarity, P is positive, N is negative 0b1XX: CK inverse polarity, P is negative, N is positive

MIPI_PHY8 (0x8A8)

BIT	7	6	5	4	3	2	1	0
Field	t_lpxesc[2:0]			RSVD	RSVD	RSVD	RSVD	RSVD
Reset	0x0			0b0	0b0	0b0		0b0
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
t_lpxesc	7:5	Typical DPHY Tlpx timing in escape mode	0b000: 66.67ns 0b001: 80ns 0b010: 100ns 0b011: 133ns 0b100: 200ns 0b101: 400ns 0b110: 1000ns 0b111: 2000ns

MIPI_PHY9 (0x8A9)

BIT	7	6	5	4	3	2	1	0
Field	phy_cp0[4:0]					–	RSVD	RSVD
Reset	0x00					–	0b0	0b0
Access Type	Write, Read					–		

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BITFIELD	BITS	DESCRIPTION	DECODE
phy_cp0	7:3	PHY copy 0, replicates data from source PHY to destination PHY	[4:3]: PHY copy 0 source [6:5]: PHY copy 0 destination [7]: PHY copy 0 enable

MIPI_PHY10 (0x8AA)

BIT	7	6	5	4	3	2	1	0
Field	phy_cp1[4:0]					–	RSVD	RSVD
Reset	0x00					–	0b1	0b0
Access Type	Write, Read					–		

BITFIELD	BITS	DESCRIPTION	DECODE
phy_cp1	7:3	PHY copy 1, replicates data from source PHY to destination PHY	[4:3]: PHY copy 1 source [6:5]: PHY copy 1 destination [7]: PHY copy 1 enable

MIPI_PHY11 (0x8AB)

BIT	7	6	5	4	3	2	1	0
Field	phy_cp_err[3:0]				–	–	RSVD	–
Reset	0x00				–	–	0b0	–
Access Type	Read Only				–	–		–

BITFIELD	BITS	DESCRIPTION	DECODE
phy_cp_err	7:4		0bXXX1: PHY copy 0 FIFO overflow 0bXX1X: PHY copy 0 FIFO underflow 0bX1XX: PHY copy 1 FIFO overflow 0b1XXX: PHY copy 1 FIFO underflow

MIPI_PHY13 (0x8AD)

BIT	7	6	5	4	3	2	1	0
Field	–	–	t_t3_prebegin[5:0]					
Reset	–	–	0x00					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
t_t3_prebegin	5:0	CPHY pre-begin phase of the preamble (t3_prebegin + 1) x 7UI	0b000000: 7UI 0b000001: 14UI . . . 0b111110: 441UI 0B111111: 448UI

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MIPI_PHY14 (0x8AE)

BIT	7	6	5	4	3	2	1	0
Field	–	t_t3_post[4:0]					t_t3_prep[1:0]	
Reset	–	0x00					0x1	
Access Type	–	Write, Read					Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
t_t3_post	6:2	CPHY post length after HS data = (t3_post + 1) x 7UI	0bXXXXX: CPHY post length
t_t3_prep	1:0	CPHY Ths_prepare timing	0b00: 40ns 0b01: 55ns 0b10: 66.7ns 0b11: 86.7ns

MIPI_PRBS_0 (0x8C0)

BIT	7	6	5	4	3	2	1	0
Field	MIPI_PRBS_EN_P1_LN1[1:0]		MIPI_PRBS_EN_P1_LN0[1:0]		MIPI_PRBS_EN_P0_LN1[1:0]		MIPI_PRBS_EN_P0_LN0[1:0]	
Reset	0x0		0x0		0x0		0x0	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MIPI_PRBS_EN_P1_LN1	7:6	PRBS enable for PHY1 lane 1 eye diagram. Set CPHY enable for CPHY symbols.	0b00: Disabled 0b01: PRBS 9 enabled 0b10: PRBS 11 enabled 0b11: PRBS 18 enabled
MIPI_PRBS_EN_P1_LN0	5:4	PRBS enable for PHY1 lane 0 eye diagram. Set CPHY enable for CPHY symbols.	0b00: Disabled 0b01: PRBS 9 enabled 0b10: PRBS 11 enabled 0b11: PRBS 18 enabled
MIPI_PRBS_EN_P0_LN1	3:2	PRBS enable for PHY0 lane 1 eye diagram. Set CPHY enable for CPHY symbols.	0b00: Disabled 0b01: PRBS 9 enabled 0b10: PRBS 11 enabled 0b11: PRBS 18 enabled
MIPI_PRBS_EN_P0_LN0	1:0	PRBS enable for PHY0 lane 0 eye diagram. Set CPHY enable for CPHY symbols.	0b00: Disabled 0b01: PRBS 9 enabled 0b10: PRBS 11 enabled 0b11: PRBS 18 enabled

MIPI_PRBS_1 (0x8C1)

BIT	7	6	5	4	3	2	1	0
Field	MIPI_PRBS_EN_P3_LN1[1:0]		MIPI_PRBS_EN_P3_LN0[1:0]		MIPI_PRBS_EN_P2_LN1[1:0]		MIPI_PRBS_EN_P2_LN0[1:0]	
Reset	0x0		0x0		0x0		0x0	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

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BITFIELD	BITS	DESCRIPTION	DECODE
MIPI_PRBS_EN_P3_LN1	7:6	PRBS enable for PHY3 lane 1 eye diagram. Set CPHY enable for CPHY symbols.	0b00: Disabled 0b01: PRBS 9 enabled 0b10: PRBS 11 enabled 0b11: PRBS 18 enabled
MIPI_PRBS_EN_P3_LN0	5:4	PRBS enable for PHY3 lane 0 eye diagram. Set CPHY enable for CPHY symbols.	0b00: Disabled 0b01: PRBS 9 enabled 0b10: PRBS 11 enabled 0b11: PRBS 18 enabled
MIPI_PRBS_EN_P2_LN1	3:2	PRBS enable for PHY2 lane 1 eye diagram. Set CPHY enable for CPHY symbols.	0b00: Disabled 0b01: PRBS 9 enabled 0b10: PRBS 11 enabled 0b11: PRBS 18 enabled
MIPI_PRBS_EN_P2_LN0	1:0	PRBS enable for PHY2 lane 0 eye diagram. Set CPHY enable for CPHY symbols.	0b00: Disabled 0b01: PRBS 9 enabled 0b10: PRBS 11 enabled 0b11: PRBS 18 enabled

MIPI_PRBS_3 (0x8C3)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	–	–	MIPI_CUSTOM_SEED_2[1:0]	
Reset	0b1	0b1	0b1	0b1	–	–	0x2	
Access Type					–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MIPI_CUSTOM_SEED_2	1:0	Custom seed [17:16] for MIPI PRBS eye diagrams. Reset value for PRBS if enabled by MIPI custom seed enable register. Default reset is from CPHY spec.	Bits [17:16]: Reset value for PRBS if enabled by MIPI custom seed enable register

MIPI_PRBS_4 (0x8C4)

BIT	7	6	5	4	3	2	1	0
Field	MIPI_CUSTOM_SEED_1[7:0]							
Reset	0x78							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MIPI_CUSTOM_SEED_1	7:0	Custom seed [15:8] for MIPI PRBS eye diagrams. Reset value for PRBS if enabled by MIPI custom seed enable register. Default reset is from CPHY spec.	Bits [15:8]: Reset value for PRBS if enabled by MIPI custom seed enable register

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MIPI_PRBS_5 (0x8C5)

BIT	7	6	5	4	3	2	1	0
Field	MIPI_CUSTOM_SEED_0[7:0]							
Reset	0x9a							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MIPI_CUSTOM_SEED_0	7:0	Custom seed [7:0] for MIPI PRBS eye diagrams. Reset value for PRBS if enabled by MIPI custom seed enable register. Default reset is from CPHY spec.	Bits [7:0]: Reset value for PRBS if enabled by MIPI custom seed enable register

MIPI_PHY_15 (0x8C6)

BIT	7	6	5	4	3	2	1	0
Field	Force_Video_Mask[3:0]				Auto_Mask_En[3:0]			
Reset	0x0				0xF			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
Force_Video_Mask	7:4	Forces video output to be masked (send all 0's) in 4WxH or Wx4H synchronous aggregation modes. Masking impacts video streams from video pipes 0-3.	0bXXX1: Force video from Video Pipe 0 to be masked. 0bXX1X: Force video from Video Pipe 1 to be masked. 0bX1XX: Force video from Video Pipe 2 to be masked. 0b1XXX: Force video from Video Pipe 3 to be masked.
Auto_Mask_En	3:0	Auto Video Mask Enable Automatically insert 0's into synchronized aggregated video outputs if a Video Pipe 0-3 video lock is lost. This allows the other video streams to continue being transmitted on the MIPI interface.	0bXXX1: Auto video mask enabled for Video Pipe 0 0bXX1X: Auto video mask enabled for Video Pipe 1 0bX1XX: Auto video mask enabled for Video Pipe 2 0b1XXX: Auto video mask enabled for Video Pipe 3

MIPI_PHY_16 (0x8C7)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	–	–	–	Video_Mask_Restart_En[3:0]			
Reset	0b0	–	–	–	0xF			
Access Type		–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
Video_Mask_Restart_En	3:0	Automatically restarts video streams that were previously masked off due to loss of video lock	0bXXX1: Restart video from Video Pipe 0 0bXX1X: Restart video from Video Pipe 1 0bX1XX: Restart video from Video Pipe 2 0b1XXX: Restart video from Video Pipe 3

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MIPI_PHY_18 (0x8C9)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	RST_MIPITX_LOC[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
RST_MIPITX_LOC	3:0	Active high reset to MIPI controllers. New for Rev C. Disabled by asserting DP_RST_MIPI. Bit 0: Controller 0 reset Bit 1: Controller 1 reset Bit 2: Controller 2 reset Bit 3: Controller 3 reset	0bxxx0: Controller 0 reset not asserted 0bxxx1: Controller 0 reset asserted 0bxx0x: Controller 1 reset not asserted 0bxx1x: Controller 1 reset asserted 0bx0xx: Controller 2 reset not asserted 0bx1xx: Controller 2 reset asserted 0b0xxx: Controller 3 reset not asserted 0b1xxx: Controller 3 reset asserted

MIPI_PHY_19 (0x8D0)

BIT	7	6	5	4	3	2	1	0
Field	csi2_tx1_pkt_cnt[3:0]				csi2_tx0_pkt_cnt[3:0]			
Reset	0x00				0x00			
Access Type	Read Only				Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
csi2_tx1_pkt_cnt	7:4	Packet count of CSI2 Controller 1	0bXXX1: PHY copy 0 FIFO overflow 0bXX1X: PHY copy 0 FIFO underflow 0bX1XX: PHY copy 1 FIFO overflow 0b1XXX: PHY copy 1 FIFO underflow
csi2_tx0_pkt_cnt	3:0	Packet count of CSI2 Controller 0	0bXXX1: PHY copy 0 FIFO overflow 0bXX1X: PHY copy 0 FIFO underflow 0bX1XX: PHY copy 1 FIFO overflow 0b1XXX: PHY copy 1 FIFO underflow

MIPI_PHY_20 (0x8D1)

BIT	7	6	5	4	3	2	1	0
Field	csi2_tx3_pkt_cnt[3:0]				csi2_tx2_pkt_cnt[3:0]			
Reset	0x00				0x00			
Access Type	Read Only				Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
csi2_tx3_pkt_cnt	7:4	Packet count of CSI2 Controller 3	0bXXX1: PHY copy 0 FIFO overflow 0bXX1X: PHY copy 0 FIFO underflow 0bX1XX: PHY copy 1 FIFO overflow 0b1XXX: PHY copy 1 FIFO underflow
csi2_tx2_pkt_cnt	3:0	Packet count of CSI2 Controller 2	0bXXX1: PHY copy 0 FIFO overflow 0bXX1X: PHY copy 0 FIFO underflow 0bX1XX: PHY copy 1 FIFO overflow 0b1XXX: PHY copy 1 FIFO underflow

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MIPI_PHY_21 (0x8D2)

BIT	7	6	5	4	3	2	1	0
Field	phy1_pkt_cnt[3:0]				phy0_pkt_cnt[3:0]			
Reset	0x00				0x00			
Access Type	Read Only				Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
phy1_pkt_cnt	7:4	Packet count of MIPI PHY1	0bXXX1: PHY copy 0 FIFO overflow 0bXX1X: PHY copy 0 FIFO underflow 0bX1XX: PHY copy 1 FIFO overflow 0b1XXX: PHY copy 1 FIFO underflow
phy0_pkt_cnt	3:0	Packet count of MIPI PHY0	0bXXX1: PHY copy 0 FIFO overflow 0bXX1X: PHY copy 0 FIFO underflow 0bX1XX: PHY copy 1 FIFO overflow 0b1XXX: PHY copy 1 FIFO underflow

MIPI_PHY_22 (0x8D3)

BIT	7	6	5	4	3	2	1	0
Field	phy3_pkt_cnt[3:0]				phy2_pkt_cnt[3:0]			
Reset	0x00				0x00			
Access Type	Read Only				Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
phy3_pkt_cnt	7:4	Packet count of MIPI PHY3	0bXXX1: PHY copy 0 FIFO overflow 0bXX1X: PHY copy 0 FIFO underflow 0bX1XX: PHY copy 1 FIFO overflow 0b1XXX: PHY copy 1 FIFO underflow
phy2_pkt_cnt	3:0	Packet count of MIPI PHY2	0bXXX1: PHY copy 0 FIFO overflow 0bXX1X: PHY copy 0 FIFO underflow 0bX1XX: PHY copy 1 FIFO overflow 0b1XXX: PHY copy 1 FIFO underflow

MIPI_TX1 (0x901, 0x941, 0x981, 0x9C1)

BIT	7	6	5	4	3	2	1	0
Field	MODE[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MODE	7:0	MIPI Tx mode: b0 = 1: Enables MIPI VS short packet counter, cyclic 1~16.	0bXXXXXXX0: Disable MIPI VS short packet counter 0bXXXXXXX1: Enable MIPI VS short packet counter

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MIPI_TX2 (0x902, 0x942, 0x982, 0x9C2)

BIT	7	6	5	4	3	2	1	0
Field	STATUS[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
STATUS	7:0	MIPI Tx Status Register	0bXXXXXXX0: SYNC mode disabled 0bXXXXXXX1: SYNC mode enabled 0bXXXXXX0X: Video channels not in-sync 0bXXXXXX1X: Video channels in-sync 0xXXXXX0XX: No loss of video sync 0xXXXXX1XX: Video sync lost after last read of this register or reset.

MIPI_TX3 (0x903, 0x943, 0x983, 0x9C3)

BIT	7	6	5	4	3	2	1	0
Field	DESKEW_INIT[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DESKEW_INIT	7:0	DPHY Deskew Initial Calibration Control The register is split into six decode segments: bit [7]: Selects auto-initial deskew calibration on or off bit [6]: Reserved bit [5]: Any bit change initiates an initial calibration if bit 4 = 1 bit [4]: Selects manual initial on or off bit [3]: Reserved bits [2:0]: Selects initial deskew width	0bXXXXX000: Initial deskew width = 1 x 32k UI 0bXXXXX001: Initial deskew width = 2 x 32k UI 0bXXXXX010: Initial deskew width = 3 x 32k UI 0bXXXXX011: Initial deskew width = 4 x 32k UI 0bXXXXX100: Initial deskew width = 5 x 32k UI 0bXXXXX101: Initial deskew width = 6 x 32k UI 0bXXXXX110: Initial deskew width = 7 x 32k UI 0bXXXXX111: Initial deskew width = 8 x 32k UI 0bXXXX0XXX: Reserved 0bXXXX1XXX: Reserved 0bXXX0XXXX: Manual initial off 0bXXX1XXXX: Manual initial on 0bXX0XXXXX: If bit 4 = 1, triggers one time immediate initial skew calibration 0bXX1XXXXX: If bit 4 = 1, triggers one time immediate initial skew calibration 0bX0XXXXXX: Reserved 0bX1XXXXXX: Reserved 0b0XXXXXXX: Auto initial deskew off 0b1XXXXXXX: Auto initial deskew on

MIPI_TX4 (0x904, 0x944, 0x984, 0x9C4)

BIT	7	6	5	4	3	2	1	0
Field	DESKEW_PER[7:0]							
Reset	0x00							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
DESKEW_PER	7:0	DPHY Periodic Deskew Calibration Control The register is split into four decode segments: bit [7]: Selects periodic deskew calibration on or off bit [6]: Selects generation on rising or falling edge of VS bits [5:3]: Selects periodic interval bits [2:0]: Selects periodic deskew width	0bXXXXX000: Periodic deskew width = 1k UI 0bXXXXX001: Periodic deskew width = 2k UI 0bXXXXX010: Periodic deskew width = 3k UI 0bXXXXX011: Periodic deskew width = 4k UI 0bXXXXX100: Periodic deskew width = 5k UI 0bXXXXX101: Periodic deskew width = 6k UI 0bXXXXX110: Periodic deskew width = 7k UI 0bXXXXX111: Periodic deskew width = 8k UI 0bXX000XXX: Periodic deskew calibration generated every frame 0bXX001XXX: Periodic deskew calibration generated every 2 frames 0bXX010XXX: Periodic deskew calibration generated every 4 frames 0bXX011XXX: Periodic deskew calibration generated every 8 frames 0bXX100XXX: Periodic deskew calibration generated every 16 frames 0bXX101XXX: Periodic deskew calibration generated every 32 frames 0bXX110XXX: Periodic deskew calibration generated every 64 frames 0bXX111XXX: Periodici deskew calibration generated every 128 frames 0bX0XXXXXX: Periodic deskew calibration generated at rising edge of VS 0bX1XXXXXX: Periodic deskew calibration generated at falling edge of VS 0b0XXXXXXX: Periodic deskew calibration off 0b1XXXXXXX: Periodic deskew calibration on

MIPI_TX5 (0x905, 0x945, 0x985, 0x9C5)

BIT	7	6	5	4	3	2	1	0
Field	CSI2_T_PRE[7:0]							
Reset	0x71							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CSI2_T_PRE	7:0	Number of clock cycles to wait before enabling HS data	0xXX: Number of MIPI byte clocks

MIPI_TX6 (0x906, 0x946, 0x986, 0x9C6)

BIT	7	6	5	4	3	2	1	0
Field	CSI2_T_POST[7:0]							
Reset	0x19							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CSI2_T_POST	7:0	Number of byte clocks to hold clock active after data	0xXX: Number of MIPI byte clocks

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MIPI_TX7 (0x907, 0x947, 0x987, 0x9C7)

BIT	7	6	5	4	3	2	1	0
Field	CSI2_TX_GAP[7:0]							
Reset	0x1C							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CSI2_TX_GAP	7:0	Sets the number of clocks to wait after the HS CLK has entered LP before enabling it again for the next transmission	0xXX: Number of MIPI byte clocks

MIPI_TX8 (0x908, 0x948, 0x988, 0x9C8)

BIT	7	6	5	4	3	2	1	0
Field	CSI2_TWAKEUP_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CSI2_TWAKEUP_L	7:0	Sets DPHY timing parameter T_{wakeup}. Set the number of clock cycles to keep clock and data in Mark-1 state after exiting ULPS.	0xXX: Number of MIPI byte clocks

MIPI_TX9 (0x909, 0x949, 0x989, 0x9C9)

BIT	7	6	5	4	3	2	1	0
Field	CSI2_TWAKEUP_M[7:0]							
Reset	0x01							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CSI2_TWAKEUP_M	7:0	Sets DPHY timing parameter T_{wakeup}. Set the number of clock cycles to keep clock and data in Mark-1 state after exiting ULPS.	0xXX: Number of MIPI byte clocks

MIPI_TX10 (0x90A, 0x94A, 0x98A, 0x9CA)

BIT	7	6	5	4	3	2	1	0
Field	CSI2_LANE_CNT[1:0]		CSI2_CPHY_EN	csi2_vcx_en	–	CSI2_TWAKEUP_H[2:0]		
Reset	0x3		0b0	0x0	–	0x0		
Access Type	Write, Read		Write, Read	Write, Read	–	Write, Read		

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BITFIELD	BITS	DESCRIPTION	DECODE
CSI2_LANE_CNT	7:6	MIPI Lane Count	0b00: One data lane 0b01: Two data lanes 0b10: Three data lanes (**Reserved** for registers 0x90A and 0x9CA) 0b11: Four data lanes (**Reserved** for registers 0x90A and 0x9CA)
CSI2_CPHY_EN	5	CPHY Enable	0b0: DPHY mode 0b1: CPHY mode
csi2_vcx_en	4	Enables virtual channel extension	0b0: Select 2-bit VC 0b1: Select 5-bit VC (CPHY) or 4-bit VC (DPHY)
CSI2_TWAKEUP_H	2:0	High bits of DPHY timing parameter T_{wakeup}. Sets the number of clock cycles to keep clock and data in Mark-1 state after exiting ULPS.	0bXXX: Number of MIPI byte clocks

MIPI_TX11 (0x90B, 0x94B, 0x98B, 0x9CB)

BIT	7	6	5	4	3	2	1	0
Field	MAP_EN_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_EN_L	7:0	Mapping enable low byte [7:0]. Each bit enables 1 of 8 mapping and distribution entries (defined in MAP_SRC_x, MAP_DST_x, and MAP_DPHY_DST_x) for the current video stream. Non-matched virtual channel (VC) and data types (DT) pass to the corresponding CSI2 controller.	0b00000000: No mapping enabled 0bXXXXXXX1: Map SRC_0 to DES_0 0bXXXXXX1X: Map SRC_1 to DES_1 0bXXXXX1XX: Map SRC_2 to DES_2 0bXXXX1XXX: Map SRC_3 to DES_3 0bXXX1XXXX: Map SRC_4 to DES_4 0bXX1XXXXX: Map SRC_5 to DES_5 0bX1XXXXXX: Map SRC_6 to DES_6 0b1XXXXXXX: Map SRC_7 to DES_7

MIPI_TX12 (0x90C, 0x94C, 0x98C, 0x9CC)

BIT	7	6	5	4	3	2	1	0
Field	MAP_EN_H[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_EN_H	7:0	Mapping enable high byte [15:8]. Each bit enables 1 of 8 mapping and distribution entries (defined in MAP_SRC_x, MAP_DST_x, and MAP_DPHY_DST_x) for the current video stream. Non-matched virtual channel (VC) and data types (DT) pass to the corresponding CSI2 controller.	0b0000000: No mapping enabled 0bXXXXXXX1: Map SRC_8 to DES_8 0bXXXXXX1X: Map SRC_9 to DES_9 0bXXXXX1XX: Map SRC_10 to DES_10 0bXXXX1XXX: Map SRC_11 to DES_11 0bXXX1XXXX: Map SRC_12 to DES_12 0bXX1XXXXX: Map SRC_13 to DES_13 0bX1XXXXXX: Map SRC_14 to DES_14 0b1XXXXXXX: Map SRC_15 to DES_15

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MIPI_TX13 (0x90D, 0x94D, 0x98D, 0x9CD)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_0	7:0	Video Pipe Source Mapping Register 0 - Virtual Channel / Data Type The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_SRC_0_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the 0th mapping pair. See register MAP_DST_0 to program the destination setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX14 (0x90E, 0x94E, 0x98E, 0x9CE)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_0	7:0	Video Pipe Destination Mapping Register 0 - Virtual Channel / Data Type The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_DST_0_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the 0th mapping pair. See register MAP_SRC_0 to program the source setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX15 (0x90F, 0x94F, 0x98F, 0x9CF)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_1	7:0	Video Pipe Source Mapping Register 1 - Virtual Channel / Data Type The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_SRC_1_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the 1st mapping pair. See register MAP_DST_1 to program the destination setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

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MIPI_TX16 (0x910, 0x950, 0x990, 0x9D0)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_1	7:0	Video Pipe Destination Mapping Register 1 - Virtual Channel / Data Type The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_DST_1_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the 1st mapping pair. See register MAP_SRC_1 to program the source setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX17 (0x911, 0x951, 0x991, 0x9D1)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_2	7:0	Video Pipe Source Mapping Register 2 - Virtual Channel / Data Type The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_SRC_2_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the 2nd mapping pair. See register MAP_DST_2 to program the destination setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX18 (0x912, 0x952, 0x992, 0x9D2)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_2	7:0	Video Pipe Destination Mapping Register 2 - Virtual Channel / Data Type The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_DST_2_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the 2nd mapping pair. See register MAP_SRC_2 to program the source setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

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MIPI_TX19 (0x913, 0x953, 0x993, 0x9D3)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_3[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_3	7:0	Video Pipe Source Mapping Register 3 - Virtual Channel / Data Type The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_SRC_3_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the 3rd mapping pair. See register MAP_DST_3 to program the destination setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX20 (0x914, 0x954, 0x994, 0x9D4)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_3[7:0]							
Reset	0x00							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_3	7:0	Video Pipe Destination Mapping Register 3 - Virtual Channel / Data Type The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_DST_3_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the 3rd mapping pair. See register MAP_SRC_3 to program the source setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX21 (0x915, 0x955, 0x995, 0x9D5)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_4[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_4	7:0	Video Pipe Source Mapping Register 4 - Virtual Channel / Data Type The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_SRC_4_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the 4th mapping pair. See register MAP_DST_4 to program the destination setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

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MIPI_TX22 (0x916, 0x956, 0x996, 0x9D6)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_4[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_4	7:0	Video Pipe Destination Mapping Register 4 - Virtual Channel / Data Type The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_DST_4_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the 4th mapping pair. See register MAP_SRC_4 to program the source setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX23 (0x917, 0x957, 0x997, 0x9D7)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_5[7:0]							
Reset	0x00							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_5	7:0	Video Pipe Source Mapping Register 5 - Virtual Channel / Data Type The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_SRC_5_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the 5th mapping pair. See register MAP_DST_5 to program the destination setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX24 (0x918, 0x958, 0x998, 0x9D8)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_5[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_5	7:0	Video Pipe Destination Mapping Register 5 - Virtual Channel / Data Type The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_DST_5_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the 5th mapping pair. See register MAP_SRC_5 to program the source setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

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MIPI_TX25 (0x919, 0x959, 0x999, 0x9D9)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_6[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_6	7:0	Video Pipe Source Mapping Register 6 - Virtual Channel / Data Type The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_SRC_6_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the 6th mapping pair. See register MAP_DST_6 to program the destination setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX26 (0x91A, 0x95A, 0x99A, 0x9DA)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_6[7:0]							
Reset	0x00							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_6	7:0	Video Pipe Destination Mapping Register 6 - Virtual Channel / Data Type The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_DST_6_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the 6th mapping pair. See register MAP_SRC_6 to program the source setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX27 (0x91B, 0x95B, 0x99B, 0x9DB)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_7[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_7	7:0	Video Pipe Source Mapping Register 7 - Virtual Channel / Data Type The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_SRC_7_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the 7th mapping pair. See register MAP_DST_7 to program the destination setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

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MIPI_TX28 (0x91C, 0x95C, 0x99C, 0x9DC)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_7[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_7	7:0	Video Pipe Destination Mapping Register 7 - Virtual Channel / Data Type The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_DST_7_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the 7th mapping pair. See register MAP_SRC_7 to program the source setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX29 (0x91D, 0x95D, 0x99D, 0x9DD)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_8[7:0]							
Reset	0x00							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_8	7:0	Video Pipe Source Mapping Register 8 - Virtual Channel / Data Type The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_SRC_8_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the 8th mapping pair. See register MAP_DST_8 to program the destination setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX30 (0x91E, 0x95E, 0x99E, 0x9DE)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_8[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_8	7:0	Video Pipe Destination Mapping Register 8 - Virtual Channel / Data Type The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_DST_8_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the 8th mapping pair. See register MAP_SRC_8 to program the source setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

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MIPI_TX31 (0x91F, 0x95F, 0x99F, 0x9DF)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_9[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_9	7:0	Video Pipe Source Mapping Register 9 - Virtual Channel / Data Type The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_SRC_9_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the 9th mapping pair. See register MAP_DST_9 to program the destination setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX32 (0x920, 0x960, 0x9A0, 0x9E0)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_9[7:0]							
Reset	0x00							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_9	7:0	Video Pipe Destination Mapping Register 9 - Virtual Channel / Data Type The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_DST_9_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the 9th mapping pair. See register MAP_SRC_9 to program the source setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX33 (0x921, 0x961, 0x9A1, 0x9E1)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_10[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_10	7:0	Video Pipe Source Mapping Register 10 - Virtual Channel / Data Type The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_SRC_10_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the 10th mapping pair. See register MAP_DST_10 to program the destination setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

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MIPI_TX34 (0x922, 0x962, 0x9A2, 0x9E2)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_10[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_10	7:0	Video Pipe Destination Mapping Register 10 - Virtual Channel / Data Type The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_DST_10_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the 10th mapping pair. See register MAP_SRC_10 to program the source setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX35 (0x923, 0x963, 0x9A3, 0x9E3)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_11[7:0]							
Reset	0x00							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_11	7:0	Video Pipe Source Mapping Register 11 - Virtual Channel / Data Type The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_SRC_11_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the 11th mapping pair. See register MAP_DST_11 to program the destination setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX36 (0x924, 0x964, 0x9A4, 0x9E4)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_11[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_11	7:0	Video Pipe Destination Mapping Register 11 - Virtual Channel / Data Type The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_DST_11_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the 11th mapping pair. See register MAP_SRC_11 to program the source setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

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MIPI_TX37 (0x925, 0x965, 0x9A5, 0x9E5)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_12[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_12	7:0	Video Pipe Source Mapping Register 12 - Virtual Channel / Data Type The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_SRC_12_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the 12th mapping pair. See register MAP_DST_12 to program the destination setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX38 (0x926, 0x966, 0x9A6, 0x9E6)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_12[7:0]							
Reset	0x00							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_12	7:0	Video Pipe Destination Mapping Register 12 - Virtual Channel / Data Type The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_DST_12_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the 12th mapping pair. See register MAP_SRC_12 to program the source setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX39 (0x927, 0x967, 0x9A7, 0x9E7)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_13[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_13	7:0	Video Pipe Source Mapping Register 13 - Virtual Channel / Data Type The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_SRC_13_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the 13th mapping pair. See register MAP_DST_13 to program the destination setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

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MIPI_TX40 (0x928, 0x968, 0x9A8, 0x9E8)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_13[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_13	7:0	Video Pipe Destination Mapping Register 13 - Virtual Channel / Data Type The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_DST_13_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the 13th mapping pair. See register MAP_SRC_13 to program the source setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX41 (0x929, 0x969, 0x9A9, 0x9E9)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_14[7:0]							
Reset	0x00							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_14	7:0	Video Pipe Source Mapping Register 14 - Virtual Channel / Data Type The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_SRC_14_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the 14th mapping pair. See register MAP_DST_14 to program the destination setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX42 (0x92A, 0x96A, 0x9AA, 0x9EA)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_14[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_14	7:0	Video Pipe Destination Mapping Register 14 - Virtual Channel / Data Type The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_DST_14_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the 14th mapping pair. See register MAP_SRC_1, to program the source setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

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MIPI_TX43 (0x92B, 0x96B, 0x9AB, 0x9EB)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_15[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_15	7:0	Video Pipe Source Mapping Register 15 - Virtual Channel / Data Type The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_SRC_15_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the 15th mapping pair. See register MAP_DST_15 to program the destination setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX44 (0x92C, 0x96C, 0x9AC, 0x9EC)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_15[7:0]							
Reset	0x00							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_15	7:0	Video Pipe Destination Mapping Register 15 - Virtual Channel / Data Type The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_DST_15_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the 15th mapping pair. See register MAP_SRC_15 to program the source setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX45 (0x92D, 0x96D, 0x9AD, 0x9ED)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DPHY_DEST_3[1:0]		MAP_DPHY_DEST_2[1:0]		MAP_DPHY_DEST_1[1:0]		MAP_DPHY_DEST_0[1:0]	
Reset	0x0		0x0		0x0		0x0	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_3	7:6	DPHY and CPHY Mapping destination controller register. CSI2 PHY destination for MAP_SRC_3 and MAP_DST_3 mapping registers.	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_2	5:4	DPHY and CPHY Mapping destination controller register. CSI2 PHY destination for MAP_SRC_2 and MAP_DST_2 mapping registers.	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_1	3:2	DPHY and CPHY Mapping destination controller register. CSI2 PHY destination for MAP_SRC_1 and MAP_DST_1 mapping registers	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_0	1:0	DPHY and CPHY Mapping destination controller register. CSI2 PHY destination for MAP_SRC_0 and MAP_DST_0 mapping registers.	0b00: Map to controller 0 0b01: Map to controller 1 0b10: Map to controller 2 0b11: Map to controller 3

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MIPI_TX46 (0x92E, 0x96E, 0x9AE, 0x9EE)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DPHY_DEST_7[1:0]		MAP_DPHY_DEST_6[1:0]		MAP_DPHY_DEST_5[1:0]		MAP_DPHY_DEST_4[1:0]	
Reset	0x0		0x0		0x0		0x0	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_7	7:6	DPHY and CPHY Mapping destination controller register. CSI2 PHY destination for MAP_SRC_7 and MAP_DST_7 mapping registers.	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_6	5:4	DPHY and CPHY Mapping destination controller register. CSI2 PHY destination for MAP_SRC_6 and MAP_DST_6 mapping registers.	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_5	3:2	DPHY and CPHY Mapping destination controller register. CSI2 PHY destination for MAP_SRC_5 and MAP_DST_5 mapping registers.	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_4	1:0	DPHY and CPHY Mapping destination controller register. CSI2 PHY destination for MAP_SRC_4 and MAP_DST_4 mapping registers.	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3

MIPI_TX47 (0x92F, 0x96F, 0x9AF, 0x9EF)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DPHY_DEST_11[1:0]		MAP_DPHY_DEST_10[1:0]		MAP_DPHY_DEST_9[1:0]		MAP_DPHY_DEST_8[1:0]	
Reset	0x0		0x0		0x0		0x0	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_11	7:6	DPHY and CPHY Mapping destination controller register. CSI2 PHY destination for MAP_SRC_11 and MAP_DST_11 mapping registers.	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_10	5:4	DPHY and CPHY Mapping destination controller register. CSI2 PHY destination for MAP_SRC_10 and MAP_DST_10 mapping registers.	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_9	3:2	DPHY and CPHY Mapping destination controller register. CSI2 PHY destination for MAP_SRC_9 and MAP_DST_9 mapping registers.	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3

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BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_8	1:0	DPHY and CPHY Mapping destination controller register. CSI2 PHY destination for MAP_SRC_8 and MAP_DST_8 mapping registers.	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3

MIPI_TX48 (0x930, 0x970, 0x9B0, 0x9F0)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DPHY_DEST_15[1:0]		MAP_DPHY_DEST_14[1:0]		MAP_DPHY_DEST_13[1:0]		MAP_DPHY_DEST_12[1:0]	
Reset	0x0		0x0		0x0		0x0	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_15	7:6	DPHY and CPHY Mapping destination controller register. CSI2 PHY destination for MAP_SRC_15 and MAP_DST_15 mapping registers.	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_14	5:4	DPHY and CPHY Mapping destination controller register. CSI2 PHY destination for MAP_SRC_14 and MAP_DST_14 mapping registers.	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_13	3:2	DPHY and CPHY Mapping destination controller register. CSI2 PHY destination for MAP_SRC_13 and MAP_DST_13 mapping registers.	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_12	1:0	DPHY and CPHY Mapping destination controller register. CSI2 PHY destination for MAP_SRC_12 and MAP_DST_12 mapping registers	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3

MIPI_TX49 (0x931, 0x971, 0x9B1, 0x9F1)

BIT	7	6	5	4	3	2	1	0
Field	MAP_CON[7:0]							
Reset	0x00							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
MAP_CON	7:0	MIPI controller SYNC concatenation register. The register is split into four decode segments: bit [7]: 1'b1 = 4WxH, 1'b0 = Wx4H bit [6]: Reserved bits [5:4]: Select the first line to concatenate. All others follow in order bits [3:0]. 2'b00 = Select Pipe 0 to be the main 2'b01 = Select Pipe 1 to be the main 2'b10 = Select Pipe 2 to be the main 2'b11 = Select Pipe 3 to be the main bit [3]: 1'b0 = disable, 1'b1 = concatenate Video Pipe 3 bit [2]: 1'b0 = disable, 1'b1 = concatenate Video Pipe 2 bit [1]: 1'b0 = disable, 1'b1 = concatenate Video Pipe 1 bit [0]: 1'b0 = disable, 1'b1 = concatenate Video Pipe 0	0bXXXXXXX1: Concatenate Video Pipeline 0 0bXXXXXX1X: Concatenate Video Pipeline 1 0bXXXXX1XX: Concatenate Video Pipeline 2 0bXXXX1XXX: Concatenate Video Pipeline 3 0bXX00XXXX: Select Video Pipeline 0 as main 0bXX01XXXX: Select Video Pipeline 1 as main 0bXX10XXXX: Select Video Pipeline 2 as main 0bXX11XXXX: Select Video Pipeline 3 as main 0b0XXXXXXX: Enable Wx4H mode 0b1XXXXXXX: Enable 4WxH mode

MIPI_TX50 (0x932, 0x972, 0x9B2, 0x9F2)

BIT	7	6	5	4	3	2	1	0
Field	SKEW_PER_SEL[7:0]							
Reset	0x00							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
SKEW_PER_SEL	7:0	Periodic deskew select register. The register is split into three decode segments: bit [7]: Select periodic deskew calibration for one or all virtual channels bits [6:5]: Reserved bits [4:0]: Virtual channel to generate periodic deskew calibration when only one channel is selected by bit 7	0b0xxxxxxx: Generate periodic calibration deskew calibration on all virtual channels 0b1xx00000: Periodic deskew calibration generated by virtual Channel 0 0b1xx00001: Periodic deskew calibration generated by virtual Channel 1 0b1xx00010: Periodic deskew calibration generated by virtual Channel 2 0b1xx00011: Periodic deskew calibration generated by virtual Channel 3 0b1xx00100: Periodic deskew calibration generated by virtual Channel 4 0b1xx00101: Periodic deskew calibration generated by virtual Channel 5 0b1xx00110: Periodic deskew calibration generated by virtual Channel 6 0b1xx00111: Periodic deskew calibration generated by virtual Channel 7 0b1xx01000: Periodic deskew calibration generated by virtual Channel 8 0b1xx01001: Periodic deskew calibration generated by virtual Channel 9 0b1xx01010: Periodic deskew calibration generated by virtual Channel 10 0b1xx01011: Periodic deskew calibration generated by virtual Channel 11 0b1xx01100: Periodic deskew calibration generated by virtual Channel 12 0b1xx01101: Periodic deskew calibration generated by virtual Channel 13 0b1xx01110: Periodic deskew calibration generated by virtual Channel 14 0b1xx01111: Periodic deskew calibration generated by virtual Channel 15

MIPI_TX51 (0x933, 0x973, 0x9B3, 0x9F3)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	ALT2_MEM_MAP8	MODE_DT	ALT_MEM_MAP10	ALT_MEM_MAP8	ALT_MEM_MAP12
Reset	–	–	–	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ALT2_MEM_MAP8	4	Alternative memory read mapping enable for 8-bit DT when sharing the same video pipe with RAW16	0b0: Alternative memory read mapping not enabled for 8-bit DT 0b1: Alternative memory read mapping enabled for 8-bit DT
MODE_DT	3	Select 24-bit mode for user-defined data types	0b0: 24-bit mode for user-defined data types not enabled 0b1: 24-bit mode for user-defined data types enabled

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BITFIELD	BITS	DESCRIPTION	DECODE
ALT_MEM_MAP10	2	Alternative memory read mapping enable for 10-bit DT	0b0: Alternative memory read mapping not enabled for 10-bit DT 0b1: Alternative memory read mapping enabled for 10-bit DT
ALT_MEM_MAP8	1	Alternative memory read mapping enable for 8-bit DT	0b0: Alternative memory read mapping not enabled for 8-bit DT 0b1: Alternative memory read mapping enabled for 8-bit DT
ALT_MEM_MAP12	0	Alternative memory read mapping enable for 12-bit DT	0b0: Alternative memory read mapping not enabled for 12-bit DT 0b1: Alternative memory read mapping enabled for 12-bit DT

MIPI_TX52 (0x934, 0x974, 0x9B4, 0x9F4)

BIT	7	6	5	4	3	2	1	0
Field	video_masked_latched[3:0]				video_masked[3:0]			
Reset	0x0				0x0			
Access Type	Read Only				Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
video_masked_latched	7:4	Indicates video pipes 0-3 were masked off at one point while in 4WxH or Wx4H synchronous aggregation mode.	0bXXX1: Video pipe 0 previously masked off 0bXX1X: Video pipe 1 previously masked off 0bX1XX: Video pipe 2 previously masked off 0b1XXX: Video pipe 3 previously masked off
video_masked	3:0	Video pipe currently masked off while in 4WxH or Wx4H synchronous aggregation mode.	0bXXX1: Video pipe 0 previously masked off 0bXX1X: Video pipe 1 previously masked off 0bX1XX: Video pipe 2 previously masked off 0b1XXX: Video pipe 3 previously masked off

MIPI_TX11 (0xA0B, 0xA4B, 0xA8B, 0xACB)

BIT	7	6	5	4	3	2	1	0
Field	MAP_EN_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_EN_L	7:0	Mapping enable low byte [7:0]. MAP_EN[15:0]: each bit enable 1 of maximum 16 mapping and distribution entries for current video stream. Non-matched VC/DT pass to corresponding CSI2 controller.	0b00000000: No mapping enabled 0bXXXXXXX1: Map SRC_0 to DES_0 0bXXXXXX1X: Map SRC_1 to DES_1 0bXXXXX1XX: Map SRC_2 to DES_2 0bXXXX1XXX: Map SRC_3 to DES_3 0bXXX1XXXX: Map SRC_4 to DES_4 0bXX1XXXXX: Map SRC_5 to DES_5 0bX1XXXXXX: Map SRC_6 to DES_6 0b1XXXXXXX: Map SRC_7 to DES_7

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MIPI_TX12 (0xA0C, 0xA4C, 0xA8C, 0xACC)

BIT	7	6	5	4	3	2	1	0
Field	MAP_EN_H[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_EN_H	7:0	Mapping enable high byte [15:8]. MAP_EN[15:0]: each bit enable 1 of maximum 16 mapping and distribution entries for current video stream. Non-matched VC/ DT pass to corresponding CSI2 controller.	0b0000000: No mapping enabled 0bXXXXXXX1: Map SRC_8 to DES_8 0bXXXXXX1X: Map SRC_9 to DES_9 0bXXXXX1XX: Map SRC_10 to DES_10 0bXXXX1XXX: Map SRC_11 to DES_11 0bXXX1XXXX: Map SRC_12 to DES_12 0bXX1XXXXX: Map SRC_13 to DES_13 0bX1XXXXXX: Map SRC_14 to DES_14 0b1XXXXXXX: Map SRC_15 to DES_15

MIPI_TX13 (0xA0D, 0xA4D, 0xA8D, 0xACD)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_0	7:0	Mapping Regulator Source - Virtual Channel / Data Type	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX14 (0xA0E, 0xA4E, 0xA8E, 0xACE)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_0	7:0	Mapping Regulator Target - Virtual Channel / Data Type	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX15 (0xA0F, 0xA4F, 0xA8F, 0xACF)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_1	7:0	Mapping Regulator Source - Virtual Channel / Data Type	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX16 (0xA10, 0xA50, 0xA90, 0xAD0)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_1	7:0	Mapping Regulator Source - Virtual Channel / Data Type	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX17 (0xA11, 0xA51, 0xA91, 0xAD1)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_2	7:0	Mapping Regulator Source - Virtual Channel / Data Type	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX18 (0xA12, 0xA52, 0xA92, 0xAD2)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_2	7:0	Mapping Regulator Source - Virtual Channel / Data Type	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX19 (0xA13, 0xA53, 0xA93, 0xAD3)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_3[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_3	7:0	Mapping Regulator Source - Virtual Channel / Data Type	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

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MIPI_TX20 (0xA14, 0xA54, 0xA94, 0xAD4)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_3[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_3	7:0	Mapping Regulator Source - Virtual Channel / Data Type	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX21 (0xA15, 0xA55, 0xA95, 0xAD5)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_4[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_4	7:0	Mapping Regulator Source - Virtual Channel / Data Type	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX22 (0xA16, 0xA56, 0xA96, 0xAD6)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_4[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_4	7:0	Mapping Regulator Source - Virtual Channel / Data Type	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX23 (0xA17, 0xA57, 0xA97, 0xAD7)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_5[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_5	7:0	Mapping Regulator Source - Virtual Channel / Data Type	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

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MIPI_TX24 (0xA18, 0xA58, 0xA98, 0xAD8)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_5[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_5	7:0	Mapping Regulator Source - Virtual Channel / Data Type	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX25 (0xA19, 0xA59, 0xA99, 0xAD9)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_6[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_6	7:0	Mapping Regulator Source - Virtual Channel / Data Type	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX26 (0xA1A, 0xA5A, 0xA9A, 0xADA)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_6[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_6	7:0	Mapping Regulator Source - Virtual Channel / Data Type	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX27 (0xA1B, 0xA5B, 0xA9B, 0xADB)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_7[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_7	7:0	Mapping Regulator Source - Virtual Channel / Data Type	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

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MIPI_TX28 (0xA1C, 0xA5C, 0xA9C, 0xADC)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_7[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_7	7:0	Mapping Regulator Source - Virtual Channel / Data Type	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX29 (0xA1D, 0xA5D, 0xA9D, 0xADD)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_8[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_8	7:0	Mapping Regulator Source - Virtual Channel / Data Type	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX30 (0xA1E, 0xA5E, 0xA9E, 0xADE)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_8[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_8	7:0	Mapping Regulator Source - Virtual Channel / Data Type	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX31 (0xA1F, 0xA5F, 0xA9F, 0xADF)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_9[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_9	7:0	Mapping Regulator Source - Virtual Channel / Data Type	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

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MIPI_TX32 (0xA20, 0xA60, 0xAA0, 0xAE0)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_9[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_9	7:0	Mapping Regulator Source - Virtual Channel / Data Type	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX33 (0xA21, 0xA61, 0xAA1, 0xAE1)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_10[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_10	7:0	Mapping Regulator Source - Virtual Channel / Data Type	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX34 (0xA22, 0xA62, 0xAA2, 0xAE2)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_10[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_10	7:0	Mapping Regulator Source - Virtual Channel / Data Type	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX35 (0xA23, 0xA63, 0xAA3, 0xAE3)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_11[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_11	7:0	Mapping Regulator Source - Virtual Channel / Data Type	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

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MIPI_TX36 (0xA24, 0xA64, 0xAA4, 0xAE4)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_11[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_11	7:0	Mapping Regulator Source - Virtual Channel / Data Type	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX37 (0xA25, 0xA65, 0xAA5, 0xAE5)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_12[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_12	7:0	Mapping Regulator Source - Virtual Channel / Data Type	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX38 (0xA26, 0xA66, 0xAA6, 0xAE6)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_12[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_12	7:0	Mapping Regulator Source - Virtual Channel / Data Type	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX39 (0xA27, 0xA67, 0xAA7, 0xAE7)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_13[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_13	7:0	Mapping Regulator Source - Virtual Channel / Data Type	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

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MIPI_TX40 (0xA28, 0xA68, 0xAA8, 0xAE8)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_13[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_13	7:0	Mapping Regulator Source - Virtual Channel / Data Type	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX41 (0xA29, 0xA69, 0xAA9, 0xAE9)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_14[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_14	7:0	Mapping Regulator Source - Virtual Channel / Data Type	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX42 (0xA2A, 0xA6A, 0xAAA, 0xAEA)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_14[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_14	7:0	Mapping Regulator Source - Virtual Channel / Data Type	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX43 (0xA2B, 0xA6B, 0xAAB, 0xAEB)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_15[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_15	7:0	Mapping Regulator Source - Virtual Channel / Data Type	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

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MIPI_TX44 (0xA2C, 0xA6C, 0xAAC, 0xAEC)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_15[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_15	7:0	Mapping Regulator Source - Virtual Channel / Data Type	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX45 (0xA2D, 0xA6D, 0xAAD, 0xAED)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DPHY_DEST_3[1:0]		MAP_DPHY_DEST_2[1:0]		MAP_DPHY_DEST_1[1:0]		MAP_DPHY_DEST_0[1:0]	
Reset	0x0		0x0		0x0		0x0	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_3	7:6	Destination of CSI2 controller 0, 1, 2, and 3 for 16 mapping registers	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_2	5:4	Destination of CSI2 controller 0, 1, 2, and 3 for 16 mapping registers	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_1	3:2	Destination of CSI2 controller 0, 1, 2, and 3 for 16 mapping registers	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_0	1:0	Destination of CSI2 controller 0, 1, 2, and 3 for 16 mapping registers	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3

MIPI_TX46 (0xA2E, 0xA6E, 0xAAE, 0xAEE)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DPHY_DEST_7[1:0]		MAP_DPHY_DEST_6[1:0]		MAP_DPHY_DEST_5[1:0]		MAP_DPHY_DEST_4[1:0]	
Reset	0x0		0x0		0x0		0x0	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_7	7:6	Destination of CSI2 controller 0, 1, 2, and 3 for 16 mapping registers	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3

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BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_6	5:4	Destination of CSI2 controller 0, 1, 2, and 3 for 16 mapping registers	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_5	3:2	Destination of CSI2 controller 0, 1, 2, and 3 for 16 mapping registers	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_4	1:0	Destination of CSI2 controller 0, 1, 2, and 3 for 16 mapping registers	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3

MIPI_TX47 (0xA2F, 0xA6F, 0xAAF, 0xAEF)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DPHY_DEST_11[1:0]		MAP_DPHY_DEST_10[1:0]		MAP_DPHY_DEST_9[1:0]		MAP_DPHY_DEST_8[1:0]	
Reset	0x0		0x0		0x0		0x0	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_11	7:6	Destination of CSI2 controller 0, 1, 2, and 3 for 16 mapping registers	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_10	5:4	Destination of CSI2 controller 0, 1, 2, and 3 for 16 mapping registers	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_9	3:2	Destination of CSI2 controller 0, 1, 2, and 3 for 16 mapping registers	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_8	1:0	Destination of CSI2 controller 0, 1, 2, and 3 for 16 mapping registers	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3

MIPI_TX48 (0xA30, 0xA70, 0xAB0, 0xAF0)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DPHY_DEST_15[1:0]		MAP_DPHY_DEST_14[1:0]		MAP_DPHY_DEST_13[1:0]		MAP_DPHY_DEST_12[1:0]	
Reset	0x0		0x0		0x0		0x0	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

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BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_15	7:6	Destination of CSI2 controller 0, 1, 2, and 3 for 16 mapping registers	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_14	5:4	Destination of CSI2 controller 0, 1, 2, and 3 for 16 mapping registers	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_13	3:2	Destination of CSI2 controller 0, 1, 2, and 3 for 16 mapping registers	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_12	1:0	Destination of CSI2 controller 0, 1, 2, and 3 for 16 mapping registers	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3

MIPI_TX49 (0xA31, 0xA71, 0xAB1, 0xAF1)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	MODE_DT	ALT_MEM_MAP10	ALT_MEM_MAP8	ALT_MEM_MAP12
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MODE_DT	3	Selects 24-bit mode for user-defined data types	0b0: 24-bit mode for user-defined data types not enabled 0b1: 24-bit mode for user-defined data types enabled
ALT_MEM_MAP10	2	Alternative memory read mapping enable for 10-bit DT	0b0: Alternative memory read mapping not enabled for 10-bit DT 0b1: Alternative memory read mapping enabled for 10-bit DT
ALT_MEM_MAP8	1	Alternative memory read mapping enable for 8-bit DT	0b0: Alternative memory read mapping not enabled for 8-bit DT 0b1: Alternative memory read mapping enabled for 8-bit DT
ALT_MEM_MAP12	0	Alternative memory read mapping enable for 12-bit DT	0b0: Alternative memory read mapping not enabled for 12-bit DT 0b1: Alternative memory read mapping enabled for 12-bit DT

GMSL1_2 (0xB02, 0xC02, 0xD02, 0xE02)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	RSVD[1:0]	
Reset	–	–	–	–	–	–	0x3	
Access Type	–	–	–	–	–	–		

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GMSL1_4 (0xB04, 0xC04, 0xD04, 0xE04)

BIT	7	6	5	4	3	2	1	0
Field	–	–	PRBSEN	CC_PORT_SEL[1:0]		–	RSVD	FWDCCEN
Reset	–	–	0x0	0x0		–	0x1	0x1
Access Type	–	–	Write, Read	Write, Read		–		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
PRBSEN	5	PRBS test enable (in HIBW mode, PRBS_TYPE—0xB0F must be set to zero)	0b0: Set device normal operation 0b1: Enable PRBS test
CC_PORT_SEL	4:3	Selects which I^{2}C/UART port is connected to this link	0b00: Port 0 (RX0_SDA0, TX0_SCL0) 0b01: Port 1 (RX1_SDA1, TX1_SCL1) 0B10: Port 2 (RX2_SDA2, TX2_SCL2)
FWDCCEN	0	Enables forward control channel to deserializer	0b0: Disable forward control channel transmitter 0b1: Enable forward control channel transmitter

GMSL1_5 (0xB05, 0xC05, 0xD05, 0xE05)

BIT	7	6	5	4	3	2	1	0
Field	I2CMETHOD	NO_REM_MST	HVTR_MODE	EN_EQ	EQTUNE[3:0]			
Reset	0x0	0x0	0x1	0x1	0x9			
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
I2CMETHOD	7	I^{2}C method, skips register address when converting UART-to-I^{2}C	0b0: Send the register address during UART-to-I^{2}C conversion 0b1: Do not send the register address during UART-to- I^{2}C conversion
NO_REM_MST	6	Set to 1 to indicate there is no I^{2}C main on the remote side. This (local) chip should ignore any I^{2}C packet initiation (start condition) from the remote side.	0b0: Main 0b1: No main
HVTR_MODE	5	HV tracking allows continuous HSYNC format	0b0: Use partial periodic HV tracking 0b1: Use partial and full periodic HV tracking
EN_EQ	4	Enables equalizer for manual and adaptive modes	0b0: Disable equalization 0b1: Enable equalization

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BITFIELD	BITS	DESCRIPTION	DECODE
EQTUNE	3:0	Equalizer boost level at 750 MHz (effective when adaptive EQ is turned off)	0b0000: 1.6dB manual EQ setting 0b0001: 2.1dB manual EQ setting 0b0010: 2.8dB manual EQ setting 0b0011: 3.5dB manual EQ setting 0b0100: 4.3dB manual EQ setting 0b0101: 5.2dB manual EQ setting 0b0110: 6.3dB manual EQ setting 0b0111: 7.3dB manual EQ setting 0b1000: 8.5dB manual EQ setting 0b1001: 9.7dB manual EQ setting 0b1010: 11dB manual EQ setting 0b1011: 12.2dB manual EQ setting 0b1100: Reserved 0b1101: Reserved 0b1110: Reserved 0b1111: Reserved

GMSL1_6 (0xB06, 0xC06, 0xD06, 0xE06)

BIT	7	6	5	4	3	2	1	0
Field	HIGHIMM	MAX_RT_EN	I2C_RT_EN	GPI_COMP_EN	GPI_RT_EN	HV_SRC[2:0]		
Reset	0x0	0x1	0x1	0x0	0x1	0x7		
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
HIGHIMM	7	Reverse channel high immunity mode (initial value set by the CFG1 pin state at power-up)	0b0: Reverse channel high immunity mode disabled 0b1: Reverse channel high immunity mode enabled
MAX_RT_EN	6	Maximum retransmission limit enable	0b0: Disable maximum retransmission limit 0b1: Enable maximum retransmission limit
I2C_RT_EN	5	I^2C retransmission enable	0b0: Disable I^2C retransmission 0b1: Enable I^2C retransmission enable
GPI_COMP_EN	4	Reverse channel high immunity mode (initial value set by the CFG1 pin state at power-up)	0b0: Disable GPI skew compensation 0b1: Enable GPI skew compensation
GPI_RT_EN	3	GPI retransmission enable	0b0: Disable GPI retransmission 0b1: Enable GPI retransmission

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BITFIELD	BITS	DESCRIPTION	DECODE
HV_SRC	2:0	HS_VS bit selection	0b000: Use D18/D19 for HS/VS (use this setting when the serializer is a 3.12Gbps device or if HIBW mode is used; otherwise, this setting is for use with the MAX9273 when DBL = 0 or HVEN = 1) 0b001: Use D14/D15 for HS/VS (for use with the MAX9271/ MAX96705 when DBL = 0 or HVEN = 1) 0b010: Use D12/D13 for HS/VS (for use with the MAX96707 when DBL = 0 or HVEN = 1) 0b011: Use D0/D1 for HS/VS (for use with the MAX9271/ MAX9273/MAX96705/MAX96707 when DBL = 1 and HVEN = 0) 0b100: Reserved 0b101: Reserved 0b110: Automatically determine the source of HSYNC/VSYNC (for use with the MAX96707) 0b111: Automatically determine the source of HSYNC/VSYNC (for use with the MAX96705)

GMSL1_7 (0xB07, 0xC07, 0xD07, 0xE07)

BIT	7	6	5	4	3	2	1	0
Field	DBL	DRS	BWS	–	HIBW	HVEN	–	PXL_CRC
Reset	0x0	0x0	0x0	–	0x0	0x0	–	0x0
Access Type	Write, Read	Write, Read	Write, Read	–	Write, Read	Write, Read	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DBL	7	Double-output mode	0b0: Use single-rate output 0b1: Use double-rate output (2x word rate at 1/2x width)
DRS	6	Data rate select	0b0: Use normal data rate output 0b1: Use 1/2 rate data output (for use with low data rates)
BWS	5	Bus width select	0b0: Set bus width for 22-/24-bit bus, 24-/27-bit mode (depending on HIBW setting) 0b1: Set bus width for 30-bit bus (32-bit mode)
HIBW	3	High-bandwidth mode	0b0: Disable high-bandwidth mode 0b1: Enable high-bandwidth mode (when BWS = 0)
HVEN	2	HS/VS encoding enable	0b0: Disable HS/VS encoding 0b1: Enable HS/VS encoding
PXL_CRC	0	Pixel error detection type (this is controllable by pin when LCCEN = 0)	0b0: Use 1-bit parity (compatible with all devices) 0b1: Use 6-bit CRC

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GMSL1_8 (0xB08, 0xC08, 0xD08, 0xE08)

BIT	7	6	5	4	3	2	1	0
Field	GPI_SEL[1:0]		GPI_EN	EN_FSYNC_TX	–	PKTCC_EN	CC_CRC_LENGTH[1:0]	
Reset	0x0		0x1	0x0	–	0x0	0x1	
Access Type	Write, Read		Write, Read	Write, Read	–	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
GPI_SEL	7:6	Selects GPI pin to transmit to serializer	0b00: GPI_0 0b01: GPI_1 0b10: GPI_2 0b11: GPI_3
GPI_EN	5	Enables GPI-to-GPO signal transmission to serializer	0b0: Disable GPI-to-GPO transmission 0b1: Enable GPI-to-GPO transmission
EN_FSYNC_TX	4	Enables frame sync signal transmission	0b0: Disable frame sync signal transmission 0b1: Enable frame sync signal transmission
PKTCC_EN	2	Packet-based control-channel mode enable	0b0: Disable packet-based control-channel mode 0b1: Enable packet-based control-channel mode
CC_CRC_LENGTH	1:0	Control channel CRC length	0b00: 1-bit CRC 0b01: 5-bit CRC 0b10: 8-bit CRC 0b11: Reserved

GMSL1_D (0xB0D, 0xC0D, 0xD0D, 0xE0D)

BIT	7	6	5	4	3	2	1	0
Field	I2C_LOC_ACK	RSVD	–	–	–	HS_TRACK_FSYNC	RSVD	RSVD
Reset	0x0	0x0	–	–	–	0x0	0x0	0x0
Access Type	Write, Read		–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
I2C_LOC_ACK	7	Enables I^2C-to-I^2C subordinate local acknowledge when forward channel is not available	0b0: Disable local acknowledge when forward channel is not available 0b1: Enable local acknowledge when forward channel is not available
HS_TRACK_FSYNC	2	0 = Allow infinite length vertical blanking 1 = Lose HLOCKED with VLOCKED	0x0: Allow infinite length vertical blanking 0x1: Lose HLOCKED with VLOCKED

GMSL1_E (0xB0E, 0xC0E, 0xD0E, 0xE0E)

BIT	7	6	5	4	3	2	1	0
Field	DET_THR[7:0]							
Reset	0x00							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
DET_THR	7:0	Threshold for detected errors	0xXX: Number of errors for detected error threshold

GMSL1_F (0xB0F, 0xC0F, 0xD0F, 0xE0F)

BIT	7	6	5	4	3	2	1	0
Field	–	EN_DE_FILT	EN_HS_FILT	EN_VS_FILT	DE_EN	–	–	PRBS_TYPE
Reset	–	0x0	0x0	0x0	0x1	–	–	0x1
Access Type	–	Write, Read	Write, Read	Write, Read	Write, Read	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
EN_DE_FILT	6	Enables glitch filtering on DE	0b0: Disable DE glitch filtering 0b1: Enable DE glitch filtering
EN_HS_FILT	5	Enables glitch filtering on HS	0b0: Disable HS glitch filtering 0b1: Enable HS glitch filtering
EN_VS_FILT	4	Enables glitch filtering on VS	0b0: Disable VS glitch filtering 0b1: Enable VS glitch filtering
DE_EN	3	Enables processing separate HS and DE signals	0b0: Disable processing HS and DE signals 0b1: Enable processing HS and DE signals
PRBS_TYPE	0	PRBS type select (in HIBW mode, set PRBS_TYPE = 0)	0b0: GMSL1 Legacy style PRBS test 0b1: Non-GMSL1 Legacy style PRBS test

GMSL1_10 (0xB10, 0xC10, 0xD10, 0xE10)

BIT	7	6	5	4	3	2	1	0
Field	RCEG_TYPE[1:0]		RCEG_BOUND	RCEG_ERR_NUM[3:0]				RCEG_EN
Reset	0x0		0x0	0x1				0x0
Access Type	Write, Read		Write, Read	Write, Read				Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RCEG_TYPE	7:6	Reverse channel generated error type	0b00: Random 0b01: Short burst 0b10: Long burst 0b11: Long burst
RCEG_BOUND	5	Reverse channel generated error boundary (effective when RCEG_TYPE = 0x)	0b0: Errors are unbounded to symbols 0b1: Errors are bounded to symbols
RCEG_ERR_NUM	4:1	Number of RCEG errors generated with each request (effective when RCEG_TYPE = 0x)	0xX: Number of errors generated per request
RCEG_EN	0	Enable reverse channel error generator	0b0: Disable reverse channel error generator 0b1: Enable reverse channel error generator enabled

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GMSL1_11 (0xB11, 0xC11, 0xD11, 0xE11)

BIT	7	6	5	4	3	2	1	0
Field	RCEG_ERR_RATE[3:0]				RCEG_LO_BST_PRB[1:0]		RCEG_LO_BST_LEN[1:0]	
Reset	0xF				0x0		0x0	
Access Type	Write, Read				Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
RCEG_ERR_RATE	7:4	Error generation rate in terms of bit time = $2^{-(RCEG_ERR_RATE + 3)}$. Effective when RCEG_TYPE = 0X.	0x0: Rate is 2^{-3} 0x1: Rate is 2^{-4} 0x2: Rate is 2^{-5} . . . 0xF: Rate is 2^{-18}
RCEG_LO_BST_PRB	3:2	Long burst error probability. Effective when RCEG_TYPE = 10.	0b00: 1/1024 0b01: 1/128 0b10: 1/32 0b11: 1/8
RCEG_LO_BST_LEN	1:0	Long burst error length in terms of bit time. Effective when RCEG_TYPE = 10.	0b00: Continuous 0b01: 128 (~150µs) 0b10: 8192 (~9.83ms) 0b11: 1048576 (~1.26s)

GMSL1_12 (0xB12, 0xC12, 0xD12, 0xE12)

BIT	7	6	5	4	3	2	1	0
Field	UNDERBST_DET_EN	CC_CRC_ERR_EN	LINE_CRC_LOC[1:0]		LINE_CRC_EN_GMSL1	–	MAX_RT_ERR_EN	RCEG_ERR_PER_EN
Reset	0x0	0x1	0x1		0x0	–	0x1	0x0
Access Type	Write, Read	Write, Read	Write, Read		Write, Read	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
UNDERBST_DET_EN	7	Allows underboost detection driving ERRORB pin	0b0: Disable underboost detection driving ERRORB pin 0b1: Enable underboost detection driving ERROR pin
CC_CRC_ERR_EN	6	Enables reporting of (CC_CRC_ERR_CNT > 0) on the ERRORB pin	0b0: Disable reporting of errors on ERRB 0b1: Enable reporting of errors on ERRB
LINE_CRC_LOC	5:4	Video line CRC insertion location	0b00: [1..4] 0b01: [5..8] 0b10: [9..12] 0b11: [13..16]
LINE_CRC_EN_GMSL1	3	Video line CRC enable	0b0: Disable video line CRC 0b1: Enable video line CRC
MAX_RT_ERR_EN	1	Enables reflection of maximum retransmission error on the ERRORB pin	0b0: Disable maximum retransmission error on the ERROR pin 0b1: Enable maximum retransmission error on the ERROR pin
RCEG_ERR_PER_EN	0	Periodic error generation enable. Effective when RCEG_TYPE (0xB10) = 0x.	0b0: Disable periodic error generator 0b1: Enable periodic error generator

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GMSL1_13 (0xB13, 0xC13, 0xD13, 0xE13)

BIT	7	6	5	4	3	2	1	0
Field	EOM_EN_G1	EOM_PER_MODE_G1	EOM_MAN_TRG_REQ_G1	EOM_MIN_THR_G1[4:0]				
Reset	0x1	0x1	0x0	0x00				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_EN_G1	7	Eye-opening monitor enable	0b0: Disable EOM 0b1: Enable EOM
EOM_PER_MODE_G1	6	Eye-opening monitor periodic mode select	0b0: Set EOM to use nonperiodic mode 0b1: Set EOM to use periodic mode
EOM_MAN_TRG_REQ_G1	5	Eye-opening monitor (EOM) manual trigger request. Valid on the rising edge of this bit when not in periodic mode.	0b0: Do not trigger EOM 0b1: Manually trigger the EOM
EOM_MIN_THR_G1	4:0	Eye-opening minimum threshold (in terms of percent) for flagging ERRORB pin	0b00000: Disabled 0b00001: 3.125% 0b00010: 6.25% . . . 0b11111: 100%

GMSL1_14 (0xB14, 0xC14, 0xD14, 0xE14)

BIT	7	6	5	4	3	2	1	0
Field	AEQ_EN	AEQ_PER_MODE	AEQ_MAN_TRG_REQ	EOM_PER_THR[4:0]				
Reset	0x1	0x0	0x0	0x00				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
AEQ_EN	7	Adaptive equalization enable	0b0: Disable AEQ 0b1: Enable AEQ
AEQ_PER_MODE	6	Adaptive equalizer periodic mode select	0b0: Set AEQ to use nonperiodic mode 0b1: Set AEQ to use periodic mode
AEQ_MAN_TRG_REQ	5	Adaptive equalizer manual fine-tune request enable. Valid on the rising edge of this bit when not in periodic mode.	0b0: Do not trigger AEQ fine tuning 0b1: Manually trigger the AEQ fine tuning
EOM_PER_THR	4:0	Eye-opening threshold to trigger a fine-tune operation	0b00000: Eye-opening threshold is disabled 0b10000: 50% eye-opening triggers fine-tune operation All other values: Reserved

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GMSL1_15 (0xB15, 0xC15, 0xD15, 0xE15)

BIT	7	6	5	4	3	2	1	0
Field	DET_ERR[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
DET_ERR	7:0	Detected error counter	0xXX: Number of detected errors

GMSL1_16 (0xB16, 0xC16, 0xD16, 0xE16)

BIT	7	6	5	4	3	2	1	0
Field	PRBS_ERR[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
PRBS_ERR	7:0	PRBS error counter	0xXX: Number of detected PRBS errors

GMSL1_17 (0xB17, 0xC17, 0xD17, 0xE17)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	MAX_RT_ERR_I2C	PRBS_OK	GPI_IN	MAX_RT_ERR_GPI	–	–	–
Reset	0x0	0x0	0x0	0x0	0x0	–	–	–
Access Type		Read Only	Read Only	Read Only	Read Only	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR_I2C	6	Maximum retransmission error flag. Cleared when read.	0b0: No control-channel retransmission error 0b1: Control-channel retransmission maximum limit reached
PRBS_OK	5	MAX9271/73 compatible PRBS test for link is completed normally. Check PRBS_ERR register for the PRBS success. For other SERDES read PRBS_ERR registers.	0b0: No MAX9271/MAX9273 compatible PRBS test completed 0b1: MAX9271/MAX9273 compatible PRBS test completed normally
GPI_IN	4	GPI pin level	0b0: GPI is input low 0b1: GPI is input high
MAX_RT_ERR_GPI	3	Maximum retransmission error flag. Cleared when read.	0b0: No control-channel retransmission error 0b1: Control-channel retransmission maximum limit reached

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GMSL1_18 (0xB18, 0xC18, 0xD18, 0xE18)

BIT	7	6	5	4	3	2	1	0
Field	CC_RETR_CNT[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
CC_RETR_CNT	7:0	I^2C packet retransmit count	0xXX: Number of I^2C packets retransmitted

GMSL1_19 (0xB19, 0xC19, 0xD19, 0xE19)

BIT	7	6	5	4	3	2	1	0
Field	CC_CRC_ERRCNT[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
CC_CRC_ERRCNT	7:0	Packet-based control-channel CRC error counter	0xXX: Number of control-channel CRC errors

GMSL1_1A (0xB1A, 0xC1A, 0xD1A, 0xE1A)

BIT	7	6	5	4	3	2	1	0
Field	RCEG_ERR_CNT[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
RCEG_ERR_CNT	7:0	Control-channel number of generated errors	0xXX: Number of control-channel generated errors

GMSL1_1B (0xB1B, 0xC1B, 0xD1B, 0xE1B)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	LINE_CRC_ERR	–	–
Reset	–	–	–	–	–	0x0	–	–
Access Type	–	–	–	–	–	Read Only	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
LINE_CRC_ERR	2	CRC error bit. Latched on error, cleared to 0 when read.	0b0: Video line CRC ok 0b1: Video line CRC mismatch detected

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GMSL1_1C (0xB1C, 0xC1C, 0xD1C, 0xE1C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	EOM_EYE_WIDTH[5:0]					
Reset	–	–	0x00					
Access Type	–	–	Read Only					

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_EYE_WIDTH	5:0	Measured eye opening. Opening width = EOM_EYE_WIDTH/63 x 100%	0b000000: Width is 0% 0b000001: Width is 1/63 x 100% 0b000010: Width is 2/63 x 100% . . . 0b11111: Width is 63/63 x 100%

GMSL1_1D (0xB1D, 0xC1D, 0xD1D, 0xE1D)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	UNDERBOOST_DET	AEQ_BST[3:0]			
Reset	–	–	–	0x0	0x0			
Access Type	–	–	–	Read Only	Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
UNDERBOOST_DET	4	Underboost detected	0b0: Normal operation 0b1: Underboost (at maximum AEQ gain) detected
AEQ_BST	3:0	Adaptive equalizer boost value. Selected adaptive equalizer value; settings correspond to gain at 750MHz	0b0000: 1.6dB manual EQ setting 0b0001: 2.1dB manual EQ setting 0b0010: 2.8dB manual EQ setting 0b0011: 3.5dB manual EQ setting 0b0100: 4.3dB manual EQ setting 0b0101: 5.2dB manual EQ setting 0b0110: 6.3dB manual EQ setting 0b0111: 7.3dB manual EQ setting 0b1000: 8.5dB manual EQ setting 0b1001: 9.7dB manual EQ setting 0b1010: 11dB manual EQ setting 0b1011: 12.2dB manual EQ setting 0b1100: Reserved 0b1101: Reserved 0b1110: Reserved 0b1111: Reserved

GMSL1_20 (0xB20, 0xC20, 0xD20, 0xE20)

BIT	7	6	5	4	3	2	1	0
Field	CRC_VALUE_0[7:0]							
Reset	0x00							
Access Type	Read Only							

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BITFIELD	BITS	DESCRIPTION	DECODE
CRC_VALUE_0	7:0	Bits [7:0] of CRC output for the latest line	0xXX: CRC[7:0] of latest line

GMSL1_21 (0xB21, 0xC21, 0xD21, 0xE21)

BIT	7	6	5	4	3	2	1	0
Field	CRC_VALUE_1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
CRC_VALUE_1	7:0	Bits [15:8] of CRC output for the latest line	0xXX: CRC[15:8] of latest line

GMSL1_22 (0xB22, 0xC22, 0xD22, 0xE22)

BIT	7	6	5	4	3	2	1	0
Field	CRC_VALUE_2[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
CRC_VALUE_2	7:0	Bits [23:16] of CRC output for the latest line	0xXX: CRC[23:16] of latest line

GMSL1_23 (0xB23, 0xC23, 0xD23, 0xE23)

BIT	7	6	5	4	3	2	1	0
Field	CRC_VALUE_3[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
CRC_VALUE_3	7:0	Bits [31:24] of CRC output for the latest line	0xXX: CRC[31:24] of latest line

GMSL1_96 (0xB96, 0xC96, 0xD96, 0xE96)

BIT	7	6	5	4	3	2	1	0
Field	CONV_GMSL1_DATATYPE[4:0]					RSVD	CONV_GMSL1_EN	RSVD
Reset	0x00					0x0	0x0	0x1
Access Type	Write, Read						Write, Read	

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BITFIELD	BITS	DESCRIPTION	DECODE
CONV_GMSL1_DATATYPE	7:3	Converts from GMSL1 color format mapping to GMSL2 CSI transmitter color format	0x0: RGB888 OLDI 0x1: RGB565 0x2: RGB666 0x3: YUV422 8-bit mux mode (use yuv_8_10_mux_mode) 0x4: YUV422 10-bit mux mode (use yuv_8_10_mux_mode) 0x5: RAW8 single 0x6: RAW10 single 0x7: RAW12 single 0x8: RAW14 0x9: User-defined generic 24-bit 0xA: User-defined YUV422 12-bit 0xB: User-defined generic 8-bit 0xC: Reserved 0xD: Reserved 0xE: Reserved 0xF: Reserved 0x10: RGB888 VESA® 0x11: Reserved 0x12: Reserved 0x13: YUV422 8-bit normal mode 0x14: YUV422 10-bit normal mode 0x15: RAW8 double (use alt_mem_map8) 0x16: RAW10 double (use alt_mem_map10) 0x17: RAW12 double (use alt_mem_map12) 0x18: Reserved 0x19: Reserved 0x1A: Reserved 0x1B: Reserved 0x1C: Reserved 0x1D: Reserved 0x1E: Reserved 0x1F: Reserved
CONV_GMSL1_EN	1	Enable conversion from GMSL1 color format mapping to GMSL2 CSI transmitter	

GMSL1_A7 (0xBA7, 0xCA7, 0xDA7, 0xEA7)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	SHIFT_VID_HVD	RSVD	–	RSVD[3:0]			
Reset	0x0	0x0	0x0	–	0x5			
Access Type		Write, Read		–				

BITFIELD	BITS	DESCRIPTION
SHIFT_VID_HVD	6	Shift video bits to make sure that the HS,VS does not appear on pixel data

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GMSL1_CB (0xBCB, 0xCCB, 0xDCB, 0xECB)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	LOCKED_G1
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type								Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
LOCKED_G1	0	Link Locked	0b0: Link not locked 0b1: Link locked

GMSL1_D1 (0xBD1, 0xCD1, 0xDD1, 0xED1)

BIT	7	6	5	4	3	2	1	0
Field	CNTL_OUT_ORD[2:0]			CNTL_OUT_EN[4:0]				
Reset	0x0			0x00000				
Access Type	Write, Read			Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CNTL_OUT_ORD	7:5	Internal CNTL_OUT order to pins CNTL4 to CNTL0	0x0: 4,3,2,1,0 0x1: 3,2,1,0,4 0x2: 2,1,0,4,3 0x3: 1,0,4,3,2 0x4: 0,1,2,3,4 0x5: 1,2,3,4,0 0x6: 2,3,4,0,1 0x7: 3,4,0,1,2
CNTL_OUT_EN	4:0	CNTL output enable for CNTL 0, 1, 2, 3, 4	

TX1 (0x1001)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	–	–	ERRG_EN	–	–	RSVD	RSVD
Reset	0b0	–	–	0b0	–	–	0b0	0b0
Access Type		–	–	Write, Read	–	–		

BITFIELD	BITS	DESCRIPTION	DECODE
ERRG_EN	4	Error generator enable	0b0: Disable error generator for Link A 0b1: Enable error generator for Link A

TX2 (0x1002)

BIT	7	6	5	4	3	2	1	0
Field	ERRG_CNT[1:0]		ERRG_RATE[1:0]		ERRG_BURST[2:0]			ERRG_PER
Reset	0x0		0x2		0x0			0b0
Access Type	Write, Read		Write, Read		Write, Read			Write, Read

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BITFIELD	BITS	DESCRIPTION	DECODE
ERRG_CNT	7:6	Number of errors to be generated	0b00: Continuous 0b01: 16 0b10: 128 0b11: 1024
ERRG_RATE	5:4	Error generator average bit error rate	0b00: 1/5120 bits 0b01: 1/81920 bits 0b10: 1/1310720 bits 0b11: 1/20971520 bits
ERRG_BURST	3:1	Error generator burst error length	0b000: 1 0b001: 2 0b010: 3 0b011: 4 0b100: 8 0b101: 12 0b110: 16 0b111: 20
ERRG_PER	0	Error generator error distribution selection	0b0: Pseudorandom 0b1: Periodic

TX3 (0x1003)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		–	–	–	TIMEOUT[2:0]		
Reset	0x1		–	–	–	0x4		
Access Type			–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TIMEOUT	2:0	Link ARQ Timeout Duration Multiplier Multiplies a timeout base constant to set the ARQ timeout. Timeout Base = 8µs	0b000: 0.5 x Timeout Base 0b001: 1.0 x Timeout Base 0b010: 1.5 x Timeout Base 0b011: 2.0 x Timeout Base 0b100: 2.5 x Timeout Base 0b101: 3.0 x Timeout Base 0b110: 3.5 x Timeout Base 0b111: 4.0 x Timeout Base

RX0 (0x1004)

BIT	7	6	5	4	3	2	1	0
Field	PKT_CNT_LBW[1:0]		–	RSVD	PKT_CNT_SEL[3:0]			
Reset	0x0		–	0b0	0x0			
Access Type	Write, Read		–		Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
PKT_CNT_LBW	7:6	Select the sub-type of low-bandwidth packets to count at PKT_CNT register	0b00: Count data packets 0b01: Count acknowledge packets 0b10: Count data and acknowledge packets 0b11: Reserved

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BITFIELD	BITS	DESCRIPTION	DECODE
PKT_CNT_SEL	3:0	Select the type of received packets to count at PKT_CNT(0x40 – 0x43)	0b0000: None 0b0001: Video 0b0010: Reserved 0b0011: INFOFR 0b0100: SPI 0b0101: I^2C 0b0110: UART 0b0111: GPIO 0b1000: Reserved 0b1001: Reserved 0b1010: Reserved 0b1011: Reserved 0b1100: Reserved 0b1101: Reserved 0b1110: All non-idle packets 0b1111: Unknown/Error

GPIOA (0x1008)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	GPIO_FWD_CDLY[5:0]					
Reset	0b0	0x1	0x01					
Access Type			Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_FWD_CDLY	5:0	Compensation delay multiplier for the forward direction. This must be the same value as GPIO_FWD_CDLY of the chip on the other side of the link. Total delay is the (value + 1) multiplied by 1.7µs. Default delay is 3.4µs.	0bXXXXXX: Forward compensation delay multiplier value

GPIOB (0x1009)

BIT	7	6	5	4	3	2	1	0
Field	GPIO_TX_WNDW[1:0]		GPIO_REV_CDLY[5:0]					
Reset	0x2		0x08					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_TX_WNDW	7:6	Wait time after a GPIO transition to create a packet. This allows grouping transitions of different GPIO inputs in a single packet and increases GPIO bandwidth usage efficiency.	0b00: Disabled 0b01: 200ns 0b10: 500ns 0b11: 1000ns

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BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_REV_CDLY	5:0	Compensation delay multiplier for the reverse direction. This must be the same value as GPIO_REV_CDLY of the chip on the other side of the link. Total delay is the (value + 1) multiplied by 1.7µs. Default delay is 15.3µs. Note: In delay compensation mode, a fixed delay is guaranteed once the link is locked. However, each link reset could change the delay between two values that are 1.7us apart.	0bXXXXXX: Reverse compensation delay multiplier value

TX1 (0x1011, 0x1021, 0x1031)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	–	–	ERRG_EN	–	–	RSVD	RSVD
Reset	0b0	–	–	0b0	–	–	0b0	0b0
Access Type		–	–	Write, Read	–	–		

BITFIELD	BITS	DESCRIPTION	DECODE
ERRG_EN	4	Error generator enable	0b0: Disable error generator 0b1: Enable error generator

TX2 (0x1012, 0x1022, 0x1032)

BIT	7	6	5	4	3	2	1	0
Field	ERRG_CNT[1:0]		ERRG_RATE[1:0]		ERRG_BURST[2:0]			ERRG_PER
Reset	0x0		0x2		0x0			0b0
Access Type	Write, Read		Write, Read		Write, Read			Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ERRG_CNT	7:6	Number of errors to be generated	0b00: Continuous 0b01: 16 errors 0b10: 128 errors 0b11: 1024 errors
ERRG_RATE	5:4	Error generator average bit error rate	0b00: 1/5120 bits 0b01: 1/81920 bits 0b10: 1/1310720 bits 0b11: 1/20971520 bits
ERRG_BURST	3:1	Error generator burst error length	0b000: 1 0b001: 2 0b010: 3 0b011: 4 0b100: 8 0b101: 12 0b110: 16 0b111: 20
ERRG_PER	0	Error generator error distribution selection	0b0: Pseudorandom 0b1: Periodic

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TX3 (0x1013, 0x1023, 0x1033)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		–	–	–	TIMEOUT[2:0]		
Reset	0x1		–	–	–	0x4		
Access Type			–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TIMEOUT	2:0	Link ARQ Timeout Duration Multiplier Multiplies a timeout base constant to set the ARQ timeout. Timeout Base = 8µs	0b000: 0.5 x Timeout Base 0b001: 1.0 x Timeout Base 0b010: 1.5 x Timeout Base 0b011: 2.0 x Timeout Base 0b100: 2.5 x Timeout Base 0b101: 3.0 x Timeout Base 0b110: 3.5 x Timeout Base 0b111: 4.0 x Timeout Base

RX0 (0x1014, 0x1024, 0x1034)

BIT	7	6	5	4	3	2	1	0
Field	PKT_CNT_LBW[1:0]		–	RSVD	PKT_CNT_SEL[3:0]			
Reset	0x0		–	0b0	0x0			
Access Type	Write, Read		–		Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
PKT_CNT_LBW	7:6	Selects the sub-type of low-bandwidth packets to count at PKT_CNT_x bitfield (0x40—0x43).	0b00: Count data packets 0b01: Count acknowledge packets 0b10: Count data and acknowledge packets 0b11: Reserved
PKT_CNT_SEL	3:0	Selects the type of received packets to count at PKT_CNT_x bitfield (0x40—0x43)	0x0: None 0x1: Video 0x2: Reserved 0x3: INFOFR 0x4: SPI 0x5: I^2C 0x6: UART 0x7: GPIO 0x8: Reserved 0x9: Reserved 0xA: Reserved 0xB: Reserved 0xC: Reserved 0xD: Reserved 0xE: All non-idle packets 0xF: Unknown/Error

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GPIOA (0x1018, 0x1028, 0x1038)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	GPIO_FWD_CDLY[5:0]					
Reset	0b0	0x1	0x01					
Access Type			Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_FWD_CDLY	5:0	Compensation delay multiplier for the forward direction. This must be the same value as GPIO_FWD_CDLY of the chip on the other side of the link. Total delay is the (value + 1) multiplied by 1.7µs. Default delay is 3.4µs. Note: In delay compensation mode, a fixed delay is guaranteed once the link is locked. However, each link reset could change the delay between two values that are 1.7us apart.	0bXXXXXX: Forward compensation delay multiplier value

GPIOB (0x1019, 0x1029, 0x1039)

BIT	7	6	5	4	3	2	1	0
Field	GPIO_TX_WNDW[1:0]		GPIO_REV_CDLY[5:0]					
Reset	0x2		0x08					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_TX_WNDW	7:6	Wait time after a GPIO transition to create a packet. This allows grouping transitions of different GPIO inputs in a single packet and increases GPIO bandwidth usage efficiency.	0b00: Disabled 0b01: 200 ns 0b10: 500 ns 0b11: 1000 ns
GPIO_REV_CDLY	5:0	Compensation delay multiplier for the reverse direction. This must be same value as GPIO_REV_CDLY of the chip on the other side of the link. Total delay is the (value + 1) multiplied by 1.7µs. Default delay is 15.3µs.	0bXXXXXX: Reverse compensation delay multiplier value

PATGEN_0 (0x1050, 0x1080)

BIT	7	6	5	4	3	2	1	0
Field	GEN_VS	GEN_HS	GEN_DE	VS_INV	HS_INV	DE_INV	VTG_MODE[1:0]	
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x3	
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	

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BITFIELD	BITS	DESCRIPTION	DECODE
GEN_VS	7	Enable to generate VS output according to the timing definition	0b0: Do not generate VS 0b1: Generate VS
GEN_HS	6	Enable to generate HS output according to the timing definition	0b0: Do not generate HS 0b1: Generate HS
GEN_DE	5	Enable to generate DE output according to the timing definition	0b0: Do not generate DE 0b1: Generate DE
VS_INV	4	Inverts VSYNC output of video timing generator	0b0: Do not invert VS 0b1: Invert VS
HS_INV	3	Inverts HSYNC output of video timing generator	0b0: Do not invert HS 0b1: Invert HS
DE_INV	2	Inverts DE output of video timing generator	0b0: Do not invert DE 0b1: Invert DE
VTG_MODE	1:0	Video interface timing generation mode. 00 or 11 = VS tracking mode. VS input's period (VS_HIGH + VS_LOW) is tracked. After VS tracking is locked, any VS input edge (glitches) not in the expected PCLK cycle is ignored. VS tracking is locked with three consecutive matches and unlocked by three consecutive mismatches. When unlocked or power-up, the next VS input edge is assumed to be the right VS edge. 01 = VS one-trigger mode One VS input edge will trigger the generation of ONE frame of VSO/HSO/DEO. If next VS input edge comes earlier or later than expected by VS period, the newly generated frame will be correct. The current VSO/HSO/DEO will be cut or extended at the time point of rising edge of the newly generated VSO/HSO/DEO. 10 = Auto-repeat mode (default) VS input edge will trigger the generation of continuous frames of VSO/HSO/DEO even if no more VS input edges. If next VS input edge comes earlier or later than expected by VS period, the newly generated frame will be correct. The current VSO/HSO/DEO will be cut or extended at the time point of rising edge of the newly generated VSO/HSO/DEO.	0b00: VS tracking mode 0b01: VS on trigger mode 0b10: Auto-repeat mode 0b11: Free-running mode

PATGEN_1 (0x1051, 0x1081)

BIT	7	6	5	4	3	2	1	0
Field	GRAD_MODE	–	PATGEN_MODE[1:0]		–	–	–	VS_TRIG
Reset	0x0	–	0x0		–	–	–	0x0
Access Type	Write, Read	–	Write, Read		–	–	–	Write, Read

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BITFIELD	BITS	DESCRIPTION	DECODE
GRAD_MODE	7	Gradient pattern generator mode	0b0: Gradient mode increasing. Each gradient color starts from a value of 0x00 and increases to 0xFF 0b1: Gradient mode decreasing. Each gradient color starts from a value of 0xFF and decreases to 0x00
PATGEN_MODE	5:4	Pattern generator mode	0b00: Pattern generator disabled - use video from the serializer input (default) 0b01: Generate checkerboard pattern 0b10: Generate gradient pattern 0b11: Reserved
VS_TRIG	0	Select VS trigger edge	0b0: Falling edge 0b1: Rising edge

VS_DLY_2 (0x1052, 0x1082)

BIT	7	6	5	4	3	2	1	0
Field	VS_DLY_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_DLY_2	7:0	VS delay in terms of PCLK cycles. The output VS is delayed by VS_DELAY cycles from the input VS. (bits [23:16])	0xXX: Most significant byte of VS delay

VS_DLY_1 (0x1053, 0x1083)

BIT	7	6	5	4	3	2	1	0
Field	VS_DLY_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_DLY_1	7:0	VS delay in terms of PCLK cycles. The output VS is delayed by VS_DELAY cycles from the input VS. (bits [15:8])	0xXX: Middle significant byte of VS delay

VS_DLY_0 (0x1054, 0x1084)

BIT	7	6	5	4	3	2	1	0
Field	VS_DLY_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_DLY_0	7:0	VS delay in terms of PCLK cycles. The output VS is delayed by VS_DELAY cycles from the input VS. (bits [7:0])	0xXX: Least significant byte of VS delay

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VS_HIGH_2 (0x1055, 0x1085)

BIT	7	6	5	4	3	2	1	0
Field	VS_HIGH_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_HIGH_2	7:0	VS high period in terms of PCLK cycles (bits [23:16])	0xXX: Most significant byte of VS high period

VS_HIGH_1 (0x1056, 0x1086)

BIT	7	6	5	4	3	2	1	0
Field	VS_HIGH_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_HIGH_1	7:0	VS high period in terms of PCLK cycles (bits [15:8])	0xXX: Middle significant byte of VS high period

VS_HIGH_0 (0x1057, 0x1087)

BIT	7	6	5	4	3	2	1	0
Field	VS_HIGH_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_HIGH_0	7:0	VS high period in terms of PCLK cycles (bits [7:0])	0xXX: Least significant byte of VS high period

VS_LOW_2 (0x1058, 0x1088)

BIT	7	6	5	4	3	2	1	0
Field	VS_LOW_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_LOW_2	7:0	VS low period in terms of PCLK cycles (bits [23:16])	0xXX: Most significant byte of VS low period

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VS_LOW_1 (0x1059, 0x1089)

BIT	7	6	5	4	3	2	1	0
Field	VS_LOW_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_LOW_1	7:0	VS low period in terms of PCLK cycles (bits [15:8])	0xXX: Middle significant byte of VS low period

VS_LOW_0 (0x105A, 0x108A)

BIT	7	6	5	4	3	2	1	0
Field	VS_LOW_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_LOW_0	7:0	VS low period in terms of PCLK cycles (bits [7:0])	0xXX: Least significant byte of VS low period

V2H_2 (0x105B, 0x108B)

BIT	7	6	5	4	3	2	1	0
Field	V2H_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V2H_2	7:0	VS edge to the rising edge of the first HS in terms of PCLK cycles (bits [23:16])	0xXX: Most significant byte of VS edge to first HS rising edge

V2H_1 (0x105C, 0x108C)

BIT	7	6	5	4	3	2	1	0
Field	V2H_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V2H_1	7:0	VS edge to the rising edge of the first HS in terms of PCLK cycles (bits [15:8])	0xXX: Middle significant byte of VS edge to first HS rising edge

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V2H_0 (0x105D, 0x108D)

BIT	7	6	5	4	3	2	1	0
Field	V2H_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V2H_0	7:0	VS edge to the rising edge of the first HS in terms of PCLK cycles (bits [7:0])	0xXX: Least significant byte of VS edge to first HS rising edge

HS_HIGH_1 (0x105E, 0x108E)

BIT	7	6	5	4	3	2	1	0
Field	HS_HIGH_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HS_HIGH_1	7:0	HS high period in terms of PCLK cycles (bits [15:8])	0xXX: Most significant byte of HS high period

HS_HIGH_0 (0x105F, 0x108F)

BIT	7	6	5	4	3	2	1	0
Field	HS_HIGH_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HS_HIGH_0	7:0	HS high period in terms of PCLK cycles (bits [7:0])	0xXX: Least significant byte of HS high period

HS_LOW_1 (0x1060, 0x1090)

BIT	7	6	5	4	3	2	1	0
Field	HS_LOW_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HS_LOW_1	7:0	HS low period in terms of PCLK cycles (bits [15:8])	0xXX: Most significant byte of HS low period

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HS_LOW_0 (0x1061, 0x1091)

BIT	7	6	5	4	3	2	1	0
Field	HS_LOW_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HS_LOW_0	7:0	HS low period in terms of PCLK cycles (bits [7:0])	0xXX: Least significant byte of HS low period

HS_CNT_1 (0x1062, 0x1092)

BIT	7	6	5	4	3	2	1	0
Field	HS_CNT_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HS_CNT_1	7:0	HS pulses per frame (bits [15:8])	0xXX: Most significant byte of HS pulses per frame

HS_CNT_0 (0x1063, 0x1093)

BIT	7	6	5	4	3	2	1	0
Field	HS_CNT_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HS_CNT_0	7:0	HS pulses per frame (bits [7:0])	0xXX: Least significant byte of HS pulses per frame

V2D_2 (0x1064, 0x1094)

BIT	7	6	5	4	3	2	1	0
Field	V2D_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V2D_2	7:0	VS edge to the rising edge of the first DE in terms of PCLK cycles (bits [23:16])	0xXX: Most significant byte of VS edge to first DE

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V2D_1 (0x1065, 0x1095)

BIT	7	6	5	4	3	2	1	0
Field	V2D_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V2D_1	7:0	VS edge to the rising edge of the first DE in terms of PCLK cycles (bits [15:8])	0xXX: Middle significant byte of VS edge to first DE

V2D_0 (0x1066, 0x1096)

BIT	7	6	5	4	3	2	1	0
Field	V2D_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V2D_0	7:0	VS edge to the rising edge of the first DE in terms of PCLK cycles (bits [23:16])	0xXX: Least significant byte of VS edge to first DE

DE_HIGH_1 (0x1067, 0x1097)

BIT	7	6	5	4	3	2	1	0
Field	DE_HIGH_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DE_HIGH_1	7:0	DE high period in terms of PCLK cycles (bits [15:8])	0xXX: Most significant byte of DE high period

DE_HIGH_0 (0x1068, 0x1098)

BIT	7	6	5	4	3	2	1	0
Field	DE_HIGH_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DE_HIGH_0	7:0	DE high period in terms of PCLK cycles (bits [7:0])	0xXX: Least significant byte of DE high period

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DE_LOW_1 (0x1069, 0x1099)

BIT	7	6	5	4	3	2	1	0
Field	DE_LOW_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DE_LOW_1	7:0	DE low period in terms of PCLK cycles (bits [15:8])	0xXX: Most significant byte of DE low period

DE_LOW_0 (0x106A, 0x109A)

BIT	7	6	5	4	3	2	1	0
Field	DE_LOW_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DE_LOW_0	7:0	DE low period in terms of PCLK cycles (bits [7:0])	0xXX: Least significant byte of DE low period

DE_CNT_1 (0x106B, 0x109B)

BIT	7	6	5	4	3	2	1	0
Field	DE_CNT_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DE_CNT_1	7:0	Active lines per frame (bits [15:8])	0xXX: Most significant byte of DE pulses per frame

DE_CNT_0 (0x106C, 0x109C)

BIT	7	6	5	4	3	2	1	0
Field	DE_CNT_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DE_CNT_0	7:0	Active lines per frame (bits [7:0])	0xXX: Least significant byte of DE pulses per frame

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GRAD_INCR (0x106D, 0x109D)

BIT	7	6	5	4	3	2	1	0
Field	GRAD_INCR[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
GRAD_INCR	7:0	Gradient mode increment amount (increment amount is the register value divided by 4)	0xXX: Gradient increment base

CHKR_COLOR_A_L (0x106E, 0x109E)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_COLOR_A_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_COLOR_A_L	7:0	Checkerboard mode color A low byte	0xXX: Least significant byte of checkerboard mode color A

CHKR_COLOR_A_M (0x106F, 0x109F)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_COLOR_A_M[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_COLOR_A_M	7:0	Checkerboard mode color A middle byte	0xXX: Middle significant byte of checkerboard mode color A

CHKR_COLOR_A_H (0x1070, 0x10A0)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_COLOR_A_H[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_COLOR_A_H	7:0	Checkerboard mode color A high byte	0xXX: Most significant byte of checkerboard mode color A

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CHKR_COLOR_B_L (0x1071, 0x10A1)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_COLOR_B_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_COLOR_B_L	7:0	Checkerboard mode color B low byte	0xXX: Least significant byte of checkerboard mode color B

CHKR_COLOR_B_M (0x1072, 0x10A2)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_COLOR_B_M[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_COLOR_B_M	7:0	Checkerboard mode color B middle byte	0xXX: Middle significant byte of checkerboard mode color B

CHKR_COLOR_B_H (0x1073, 0x10A3)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_COLOR_B_H[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_COLOR_B_H	7:0	Checkerboard mode color B high byte	0xXX: Most significant byte of checkerboard mode color B

CHKR_RPT_A (0x1074, 0x10A4)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_RPT_A[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_RPT_A	7:0	Checkerboard mode color A repeat count	0xXX: Repeat count of checkerboard mode color A

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CHKR_RPT_B (0x1075, 0x10A5)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_RPT_B[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_RPT_B	7:0	Checkerboard mode color B repeat count	0xXX: Repeat count of checkerboard mode color B

CHKR_ALT (0x1076, 0x10A6)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_ALT[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_ALT	7:0	Checkerboard mode alternate line count	0xXX: Checkerboard mode alternate line count

CNT_AX (0x11D0)

BIT	7	6	5	4	3	2	1	0
Field	VID_PXL_CRC_ERR_AX[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
VID_PXL_CRC_ERR_AX	7:0	Total number of video pixel CRC errors detected at video stream AX. Reset after reading or with the rising edge of LOCK.	0xXX: Total number of video pixel CRC errors detected at video stream AX

CNT_AY (0x11D1)

BIT	7	6	5	4	3	2	1	0
Field	VID_PXL_CRC_ERR_AY[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
VID_PXL_CRC_ERR_AY	7:0	Total number of video pixel CRC errors detected at video stream AY. Reset after reading or with the rising edge of LOCK.	0xXX: Total number of video pixel CRC errors detected at video stream AY

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CNT_AZ (0x11D2)

BIT	7	6	5	4	3	2	1	0
Field	VID_PXL_CRC_ERR_AZ[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
VID_PXL_CRC_ERR_AZ	7:0	Total number of video pixel CRC errors detected at video stream AZ. Reset after reading or with the rising edge of LOCK.	0xXX: Total number of video pixel CRC errors detected at video stream AZ

CNT_AU (0x11E0)

BIT	7	6	5	4	3	2	1	0
Field	VID_PXL_CRC_ERR_AU[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
VID_PXL_CRC_ERR_AU	7:0	Total number of video pixel CRC errors detected at video stream AU. Reset after reading or with the rising edge of LOCK.	0xXX: Total number of video pixel CRC errors detected at video stream AU

CNT_BX (0x11E1)

BIT	7	6	5	4	3	2	1	0
Field	VID_PXL_CRC_ERR_BX[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
VID_PXL_CRC_ERR_BX	7:0	Total number of video pixel CRC errors detected at video stream BX. Reset after reading or with the rising edge of LOCK.	0xXX: Total number of video pixel CRC errors detected at video stream BX

CNT_BY (0x11E2)

BIT	7	6	5	4	3	2	1	0
Field	VID_PXL_CRC_ERR_BY[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
VID_PXL_CRC_ERR_BY	7:0	Total number of video pixel CRC errors detected at video stream BY. Reset after reading or with the rising edge of LOCK.	0xXX: Total number of video pixel CRC errors detected at video stream BY

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CNT_BZ (0x11E3)

BIT	7	6	5	4	3	2	1	0
Field	VID_PXL_CRC_ERR_BZ[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
VID_PXL_CRC_ERR_BZ	7:0	Total number of video pixel CRC errors detected at video stream BZ. Reset after reading or with the rising edge of LOCK.	0xXX: Total number of video pixel CRC errors detected at video stream BZ

CNT_BU (0x11E4)

BIT	7	6	5	4	3	2	1	0
Field	VID_PXL_CRC_ERR_BU[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
VID_PXL_CRC_ERR_BU	7:0	Total number of video pixel CRC errors detected at video stream BU. Reset after reading or with the rising edge of LOCK.	0xXX: Total number of video pixel CRC errors detected at video stream BU

CNT_CX (0x11E5)

BIT	7	6	5	4	3	2	1	0
Field	VID_PXL_CRC_ERR_CX[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
VID_PXL_CRC_ERR_CX	7:0	Total number of video pixel CRC errors detected at video stream CX. Reset after reading or with the rising edge of LOCK.	0xXX: Total number of video pixel CRC errors detected at video stream CX

CNT_CY (0x11E6)

BIT	7	6	5	4	3	2	1	0
Field	VID_PXL_CRC_ERR_CY[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
VID_PXL_CRC_ERR_CY	7:0	Total number of video pixel CRC errors detected at video stream CY. Reset after reading or with the rising edge of LOCK.	0xXX: Total number of video pixel CRC errors detected at video stream CY

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CNT_CZ (0x11E7)

BIT	7	6	5	4	3	2	1	0
Field	VID_PXL_CRC_ERR_CZ[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
VID_PXL_CRC_ERR_CZ	7:0	Total number of video pixel CRC errors detected at video stream CZ. Reset after reading or with the rising edge of LOCK.	0xXX: Total number of video pixel CRC errors detected at video stream CZ

CNT_CU (0x11E8)

BIT	7	6	5	4	3	2	1	0
Field	VID_PXL_CRC_ERR_CU[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
VID_PXL_CRC_ERR_CU	7:0	Total number of video pixel CRC errors detected at video stream CU. Reset after reading or with the rising edge of LOCK.	0xXX: Total number of video pixel CRC errors detected at video stream CU

CNT_DX (0x11E9)

BIT	7	6	5	4	3	2	1	0
Field	VID_PXL_CRC_ERR_DX[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
VID_PXL_CRC_ERR_DX	7:0	Total number of video pixel CRC errors detected at video stream DX. Reset after reading or with the rising edge of LOCK.	0xXX: Total number of video pixel CRC errors detected at video stream DX

CNT_DY (0x11EA)

BIT	7	6	5	4	3	2	1	0
Field	VID_PXL_CRC_ERR_DY[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
VID_PXL_CRC_ERR_DY	7:0	Total number of video pixel CRC errors detected at video stream DY. Reset after reading or with the rising edge of LOCK.	0xXX: Total number of video pixel CRC errors detected at video stream DY

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CNT_DZ (0x11EB)

BIT	7	6	5	4	3	2	1	0
Field	VID_PXL_CRC_ERR_DZ[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
VID_PXL_CRC_ERR_DZ	7:0	Total number of video pixel CRC errors detected at video stream DZ. Reset after reading or with the rising edge of LOCK.	0xXX: Total number of video pixel CRC errors detected at video stream DZ

CNT_DU (0x11EC)

BIT	7	6	5	4	3	2	1	0
Field	VID_PXL_CRC_ERR_DU[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
VID_PXL_CRC_ERR_DU	7:0	Total number of video pixel CRC errors detected at video stream DU. Reset after reading or with the rising edge of LOCK.	0xXX: Total number of video pixel CRC errors detected at video stream DU

DE_DET (0x11F0)

BIT	7	6	5	4	3	2	1	0
Field	DE_DET_7	DE_DET_6	DE_DET_5	DE_DET_4	DE_DET_3	DE_DET_2	DE_DET_1	DE_DET_0
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
DE_DET_7	7	DE activity is detected in Video Pipe 7	0b0: DE is not detected 0b1: DE is detected
DE_DET_6	6	DE activity is detected in Video Pipe 6	0b0: DE is not detected 0b1: DE is detected
DE_DET_5	5	DE activity is detected in Video Pipe 5	0b0: DE is not detected 0b1: DE is detected
DE_DET_4	4	DE activity is detected in Video Pipe 4	0b0: DE is not detected 0b1: DE is detected
DE_DET_3	3	DE activity is detected in Video Pipe 3	0b0: DE is not detected 0b1: DE is detected
DE_DET_2	2	DE activity is detected in Video Pipe 2	0b0: DE is not detected 0b1: DE is detected
DE_DET_1	1	DE activity is detected in Video Pipe 1	0b0: DE is not detected 0b1: DE is detected
DE_DET_0	0	DE activity is detected in Video Pipe 0	0b0: DE is not detected 0b1: DE is detected

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HS_DET (0x11F1)

BIT	7	6	5	4	3	2	1	0
Field	HS_DET_7	HS_DET_6	HS_DET_5	HS_DET_4	HS_DET_3	HS_DET_2	HS_DET_1	HS_DET_0
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
HS_DET_7	7	HS activity is detected in Video Pipe 7	0b0: HS is not detected 0b1: HS is detected
HS_DET_6	6	HS activity is detected in Video Pipe 6	0b0: HS is not detected 0b1: HS is detected
HS_DET_5	5	HS activity is detected in Video Pipe 5	0b0: HS is not detected 0b1: HS is detected
HS_DET_4	4	HS activity is detected in Video Pipe 4	0b0: HS is not detected 0b1: HS is detected
HS_DET_3	3	HS activity is detected in Video Pipe 3	0b0: HS is not detected 0b1: HS is detected
HS_DET_2	2	HS activity is detected in Video Pipe 2	0b0: HS is not detected 0b1: HS is detected
HS_DET_1	1	HS activity is detected in Video Pipe 1	0b0: HS is not detected 0b1: HS is detected
HS_DET_0	0	HS activity is detected in Video Pipe 0	0b0: HS is not detected 0b1: HS is detected

VS_DET (0x11F2)

BIT	7	6	5	4	3	2	1	0
Field	VS_DET_7	VS_DET_6	VS_DET_5	VS_DET_4	VS_DET_3	VS_DET_2	VS_DET_1	VS_DET_0
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
VS_DET_7	7	VS activity is detected in Video Pipe 7	0b0: VS is not detected 0b1: VS is detected
VS_DET_6	6	VS activity is detected in Video Pipe 6	0b0: VS is not detected 0b1: VS is detected
VS_DET_5	5	VS activity is detected in Video Pipe 5	0b0: VS is not detected 0b1: VS is detected
VS_DET_4	4	VS activity is detected in Video Pipe 4	0b0: VS is not detected 0b1: VS is detected
VS_DET_3	3	VS activity is detected in Video Pipe 3	0b0: VS is not detected 0b1: VS is detected
VS_DET_2	2	VS activity is detected in Video Pipe 2	0b0: VS is not detected 0b1: VS is detected
VS_DET_1	1	VS activity is detected in Video Pipe 1	0b0: VS is not detected 0b1: VS is detected
VS_DET_0	0	VS activity is detected in Video Pipe 0	0b0: VS is not detected 0b1: VS is detected

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HS_POL (0x11F3)

BIT	7	6	5	4	3	2	1	0
Field	HS_POL_7	HS_POL_6	HS_POL_5	HS_POL_4	HS_POL_3	HS_POL_2	HS_POL_1	HS_POL_0
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
HS_POL_7	7	Detected HS polarity in Video Pipe 7	0b0: Active low 0b1: Active high
HS_POL_6	6	Detected HS polarity in Video Pipe 6	0b0: Active low 0b1: Active high
HS_POL_5	5	Detected HS polarity in Video Pipe 5	0b0: Active low 0b1: Active high
HS_POL_4	4	Detected HS polarity in Video Pipe 4	0b0: Active low 0b1: Active high
HS_POL_3	3	Detected HS polarity in Video Pipe 3	0b0: Active low 0b1: Active high
HS_POL_2	2	Detected HS polarity in Video Pipe 2	0b0: Active low 0b1: Active high
HS_POL_1	1	Detected HS polarity in Video Pipe 1	0b0: Active low 0b1: Active high
HS_POL_0	0	Detected HS polarity in Video Pipe 0	0b0: Active low 0b1: Active high

VS_POL (0x11F4)

BIT	7	6	5	4	3	2	1	0
Field	VS_POL_7	VS_POL_6	VS_POL_5	VS_POL_4	VS_POL_3	VS_POL_2	VS_POL_1	VS_POL_0
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
VS_POL_7	7	Detected VS polarity in Video Pipe 7	0b0: Active low 0b1: Active high
VS_POL_6	6	Detected VS polarity in Video Pipe 6	0b0: Active low 0b1: Active high
VS_POL_5	5	Detected VS polarity in Video Pipe 6	0b0: Active low 0b1: Active high
VS_POL_4	4	Detected VS polarity in Video Pipe 4	0b0: Active low 0b1: Active high
VS_POL_3	3	Detected VS polarity in Video Pipe 3	0b0: Active low 0b1: Active high
VS_POL_2	2	Detected VS polarity in Video Pipe 2	0b0: Active low 0b1: Active high
VS_POL_1	1	Detected VS polarity in Video Pipe 1	0b0: Active low 0b1: Active high
VS_POL_0	0	Detected VS polarity in Video Pipe 0	0b0: Active low 0b1: Active high

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WM_0 (0x1200)

BIT	7	6	5	4	3	2	1	0
Field	WM_LEN	WM_MODE[2:0]			WM_DET[1:0]		–	WM_EN
Reset	0x0	0x0			0x0		–	0x0
Access Type	Write, Read	Write, Read			Write, Read		–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
WM_LEN	7	Watermark Length	0b0: Watermark length is 32 bits 0b1: Watermark length is 64 bits
WM_MODE	6:4	Select watermark generation mode	0b000: Default generator mode - cycle through all four watermarks in video stream 0b001: Error generator mode - cycle through only two watermarks to replicate a frozen frame 0b010 to 0b111: Reserved
WM_DET	3:2	Watermark Detection/Generation	0b00: Insert watermark in video stream 0b01: Detect watermark and remove from outgoing video stream 0b10: Reserved 0b11: Reserved
WM_EN	0	Enable/Disable of watermarking generation/ detection block	0b0: Watermarking block disabled 0b1: Watermarking block enabled

WM_1 (0x1201)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		WM_KO[1:0]		RSVD[3:0]			
Reset	0x1		0x1		0x9			
Access Type			Write, Read					

BITFIELD	BITS	DESCRIPTION
WM_KO	5:4	Watermark Gain

WM_2 (0x1202)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD[2:0]			HsyncPol	VsyncPol	WM_NPFILT[1:0]	
Reset	–	0x5			0b0	0b0	0x0	
Access Type	–				Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
HsyncPol	3	HS Polarity	0b0: Non-inverting 0b1: Invert
VsyncPol	2	VS Polarity	0b0: Non-inverting 0b1: Invert
WM_NPFILT	1:0	Phase accumulator terminal count	0bXX: Phase accumulator terminal count

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WM_3 (0x1203)

BIT	7	6	5	4	3	2	1	0
Field	–	WM_TH[6:0]						
Reset	–	0x14						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
WM_TH	6:0	Matched-filter threshold	0bXXXXXXX: Matched-filter threshold

WM_4 (0x1204)

BIT	7	6	5	4	3	2	1	0
Field	–	–	RSVD[1:0]		RSVD	–	WM_MASKMODE[1:0]	
Reset	–	–	0x01		0x0	–	0x0	
Access Type	–	–				–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
WM_MASKMODE	1:0	Sets watermark mask for the device	0b00: Mask if WM is detected 0b01: Mask if WM is detected, blank if error is detected 0b10: Reserved b011: Reserved

WM_5 (0x1205)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	RSVD	WM_DETOUT	WM_ERROR
Reset	–	–	–	–	–	0x0	0x0	0x0
Access Type	–	–	–	–	–		Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
WM_DETOUT	1	Live frame based detection output	0b0: Watermark not detected 0b1: Watermark detected
WM_ERROR	0	Live active high watermark error	0b0: No watermark error 0b1: Watermark error active, bit automatically clears when error clears.

WM_6 (0x1206)

BIT	7	6	5	4	3	2	1	0
Field	WM_TIMER[7:0]							
Reset	0x00							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
WM_TIMER	7:0	Time in 2ms steps the frozen frame condition must be observed before an error is generated. 0 = No filter	0xXX: Number of milliseconds

WM_WREN_0 (0x121E)

BIT	7	6	5	4	3	2	1	0
Field	WM_WREN_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
WM_WREN_L	7:0	Write 0xBA to WM_WREN_L and 0xDC to WM_WREN_H registers to enable writing to watermark registers. Otherwise, watermark registers are read only.	0xBA: Enable writing to watermark registers others: Disable - Read Only

WM_WREN_1 (0x121F)

BIT	7	6	5	4	3	2	1	0
Field	WM_WREN_H[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
WM_WREN_H	7:0	Write 0xBA to WM_WREN_L and 0xDC to WM_WREN_H registers to enable writing to watermark registers. Otherwise, watermark registers are read-only.	0xBA: Enable writing to watermark registers others: Disable - Read Only

WM_0 (0x1220)

BIT	7	6	5	4	3	2	1	0
Field	WM1_LEN	WM1_MODE[2:0]			WM1_DET[1:0]		–	WM1_EN
Reset	0x0	0x0			0x0		–	0x0
Access Type	Write, Read	Write, Read			Write, Read		–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
WM1_LEN	7	Watermark Length	0b0: Watermark length is 32 bits 0b1: Watermark length is 64 bits
WM1_MODE	6:4	Select watermark generation mode	0b000: Default generator mode - cycle through all four watermarks in video stream 0b001: Error generator mode - cycle through only two watermarks to replicate a frozen frame 0b010 to 0b111: Reserved

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BITFIELD	BITS	DESCRIPTION	DECODE
WM1_DET	3:2	Watermark Detection/Generation	0b00: Insert watermark in video stream 0b01: Detect watermark and remove from outgoing video stream 0b10: Reserved 0b11: Reserved
WM1_EN	0	Enable/Disable of watermarking generation/ detection block	0b0: Watermarking block disabled 0b1: Watermarking block enabled

WM_1 (0x1221)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		WM1_KO[1:0]		RSVD[3:0]			
Reset	0x1		0x1		0x9			
Access Type			Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
WM1_KO	5:4	Watermark Gain	0b00: 1 bit 0b01: 2 bits 0b10: 3 bits 0b11: 4 bits

WM_2 (0x1222)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD[2:0]			HsyncPol1	VsyncPol1	RSVD[1:0]	
Reset	–	0x5			0b0	0b0	0x0	
Access Type	–				Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
HsyncPol1	3	HS Polarity	0b0: Non-inverting 0b1: Invert
VsyncPol1	2	VS Polarity	0b0: Non-inverting 0b1: Invert

WM_4 (0x1224)

BIT	7	6	5	4	3	2	1	0
Field	–	–	WM1_YUV_IN[1:0]		WM1_COLORADJ	–	WM1_MASKMODE[1:0]	
Reset	–	–	0x01		0x0	–	0x0	
Access Type	–	–	Write, Read		Write, Read	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
WM1_YUV_IN	5:4	Input color format	0b00: RGB 8-bit color data 0b01: YUV444 8-bits each 0b10: Reserved 0b11: Reserved

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BITFIELD	BITS	DESCRIPTION	DECODE
WM1_COLORADJ	3	Color adjust	0b0: Masked off LSbs of U. Use if temporal dithering is enabled. 0b1: Set U [Ko:0] = 1/2 WM gain. Use this mode if temporal dithering is disabled
WM1_MASKMODE	1:0	Sets watermark mask for the device	0b00: Mask if WM is detected 0b01: Mask if WM is detected, blank if error is detected 0b10: Reserved b011: Reserved

WM_5 (0x1225)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	RSVD	WM1_DETOUT	WM1_ERROR
Reset	–	–	–	–	–	0x0	0x0	0x0
Access Type	–	–	–	–	–		Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
WM1_DETOUT	1	Live frame based detection output	0b0: Watermark not detected 0b1: Watermark detected
WM1_ERROR	0	Live active high watermark error	0b0: No watermark error 0b1: Watermark error active, bit automatically clears when error clears.

WM_6 (0x1226)

BIT	7	6	5	4	3	2	1	0
Field	WM1_TIMER[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
WM1_TIMER	7:0	Time in 2ms steps the frozen frame condition must be observed before an error is generated. 0 = No filter	0xXX: Number of milliseconds

WM_WREN_0 (0x123E)

BIT	7	6	5	4	3	2	1	0
Field	WM1_WREN_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
WM1_WREN_L	7:0	Write 0xBA to WM_WREN_L and 0xDC to WM_WREN_H registers to enable writing to watermark registers. Otherwise, watermark registers are read-only.	0xBA: Enable writing to watermark registers Others: Disable - Read Only

WM_WREN_1 (0x123F)

BIT	7	6	5	4	3	2	1	0
Field	WM1_WREN_H[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
WM1_WREN_H	7:0	Write 0xBA to WM_WREN_L and 0xDC to WM_WREN_H registers to enable writing to watermark registers. Otherwise, watermark registers are read-only.	0xBA: Enable writing to watermark registers Others: Disable - Read Only

MEM_ECC0 (0x1250)

BIT	7	6	5	4	3	2	1	0
Field	MEM_ECC_ERR2_THR[2:0]			MEM_ECC_ERR1_THR[2:0]			RESET_MEM_ECC_ERR2_CNT	RESET_MEM_ECC_ERR1_CNT
Reset	0x0			0x0			0b0	0b0
Access Type	Write, Read			Write, Read			Write Clears All, Read	Write Clears All, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MEM_ECC_ERR2_THR	7:5	Decoding and error reporting threshold. MEM_ECC_ERR2 is asserted when MEM_ECC_ERR2_CNT ≥ MEM_ECC_ERR2_THR.	0b000: 1 0b001: 2 0b010: 4 0b011: 8 0b100: 16 0b101: 32 0b110: 64 0b111: 128
MEM_ECC_ERR1_THR	4:2	Decoding and error reporting threshold. MEM_ECC_ERR1 is asserted when MEM_ECC_ERR1_CNT ≥ MEM_ECC_ERR1_THR.	0b000: 1 0b001: 2 0b010: 4 0b011: 8 0b100: 16 0b101: 32 0b110: 64 0b111: 128
RESET_MEM_ECC_ERR2_CNT	1	Reset memory ECC 2-bit error count to 0	0b0: Do not reset ECC 2-bit error count 0b1: Reset ECC 2-bit error count
RESET_MEM_ECC_ERR1_CNT	0	Reset memory ECC 1-bit error count to 0	0b0: Do not reset ECC 1-bit error count 0b1: Reset ECC 1-bit error count

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MEM_ECC1 (0x1251)

BIT	7	6	5	4	3	2	1	0
Field	MEM_ECC_ERR1_CNT[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
MEM_ECC_ERR1_CNT	7:0	Number of 1-bit correctable memory ECC errors seen	0xXX: Number of 1-bit memory ECC errors

MEM_ECC2 (0x1252)

BIT	7	6	5	4	3	2	1	0
Field	MEM_ECC_ERR2_CNT[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
MEM_ECC_ERR2_CNT	7:0	Number of 2-bit uncorrectable memory ECC errors seen	0xXX: Number of 2-bit memory ECC errors

MEM_ECC_ERR_DEBUG (0x1253)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	MEM_INJ_E2A	MEM_INJ_E1A
Reset	–	–	–	–	–	–	0b0	0b0
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MEM_INJ_E2A	1	Injects 2 error bits for every 39-bit write into all 64 ECC memories in backtop	0b0: Do not inject error bits 0b1: Inject error bits
MEM_INJ_E1A	0	Injects 1 error bit for every 39-bit write into all 64 ECC memories in backtop	0b0: Do not inject error bits 0b1: Inject error bits

MEM_ECC_ERR_FLAG (0x1254)

BIT	7	6	5	4	3	2	1	0
Field	BACKTOP8_ECC_ERR_FLAG	BACKTOP7_ECC_ERR_FLAG	BACKTOP6_ECC_ERR_FLAG	BACKTOP5_ECC_ERR_FLAG	BACKTOP4_ECC_ERR_FLAG	BACKTOP3_ECC_ERR_FLAG	BACKTOP2_ECC_ERR_FLAG	BACKTOP1_ECC_ERR_FLAG
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

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BITFIELD	BITS	DESCRIPTION	DECODE
BACKTOP8_ECC_ERR_FLAG	7	Flag reads out 1-bit or 2-bit error in BACKTOP8, selected by ECC_ERR_FLAG_SEL. ECC_ERR_FLAG_SEL = 0 selects 2-bit error ECC_ERR_FLAG_SEL = 1 selects 1-bit error	0b0: No error detected 0b1: Error detected
BACKTOP7_ECC_ERR_FLAG	6	Flag reads out 1-bit or 2-bit error in BACKTOP7, selected by ECC_ERR_FLAG_SEL. ECC_ERR_FLAG_SEL = 0 selects 2-bit error ECC_ERR_FLAG_SEL = 1 selects 1-bit error	0b0: No error detected 0b1: Error detected
BACKTOP6_ECC_ERR_FLAG	5	Flag reads out 1-bit or 2-bit error in BACKTOP6, selected by ECC_ERR_FLAG_SEL. ECC_ERR_FLAG_SEL = 0 selects 2-bit error ECC_ERR_FLAG_SEL = 1 selects 1-bit error	0b0: No error detected 0b1: Error detected
BACKTOP5_ECC_ERR_FLAG	4	Flag reads out 1-bit or 2-bit error in BACKTOP5, selected by ECC_ERR_FLAG_SEL. ECC_ERR_FLAG_SEL = 0 selects 2-bit error ECC_ERR_FLAG_SEL = 1 selects 1-bit error	0b0: No error detected 0b1: Error detected
BACKTOP4_ECC_ERR_FLAG	3	Flag reads out 1-bit or 2-bit error in BACKTOP4, selected by ECC_ERR_FLAG_SEL. ECC_ERR_FLAG_SEL = 0 selects 2-bit error ECC_ERR_FLAG_SEL = 1 selects 1-bit error	0b0: No error detected 0b1: Error detected
BACKTOP3_ECC_ERR_FLAG	2	Flag reads out 1-bit or 2-bit error in BACKTOP3, selected by ECC_ERR_FLAG_SEL. ECC_ERR_FLAG_SEL = 0 selects 2-bit error ECC_ERR_FLAG_SEL = 1 selects 1-bit error	0b0: No error detected 0b1: Error detected
BACKTOP2_ECC_ERR_FLAG	1	Flag reads out 1-bit or 2-bit error in BACKTOP2, selected by ECC_ERR_FLAG_SEL. ECC_ERR_FLAG_SEL = 0 selects 2-bit error ECC_ERR_FLAG_SEL = 1 selects 1-bit error	0b0: No error detected 0b1: Error detected
BACKTOP1_ECC_ERR_FLAG	0	Flag reads out 1-bit or 2-bit error in BACKTOP1, selected by ECC_ERR_FLAG_SEL. ECC_ERR_FLAG_SEL = 0 selects 2-bit error ECC_ERR_FLAG_SEL = 1 selects 1-bit error	0b0: No error detected 0b1: Error detected

SPARE_DIGITAL (0x12A1)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RESET_MEM_FLUSH	BACKTOP_ECC_ERR_SEL
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type							Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RESET_MEM_FLUSH	1	Write to 1 then 0 to reset memory flushed register in all BACKTOPs	0b0: Do not reset backtop memory flags 0b1: Reset backtop memory flags

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BITFIELD	BITS	DESCRIPTION	DECODE
BACKTOP_ECC_ERR_SEL	0	Selection bit for 1-bit or 2-bit ECC error flag read-out from BACKTOPx_ECC_ERR_FLAG register. Defaults to 2-bit error.	0b0: 2-bit errors reported 0b1: 1-bit errors reported

RLMS3 (0x1403, 0x1503, 0x1603, 0x1703)

BIT	7	6	5	4	3	2	1	0
Field	AdaptEn	RSVD	RSVD	RSVD	RSVD	–	RSVD[1:0]	
Reset	0x0	0x0	0x0	0x0	0x1	–	0x2	
Access Type	Write, Read					–		

BITFIELD	BITS	DESCRIPTION	DECODE
AdaptEn	7	Adapt process enable	0b0: Timing adjust disabled 0b1: Timing adjust enabled

RLMS4 (0x1404, 0x1504, 0x1604, 0x1704)

BIT	7	6	5	4	3	2	1	0
Field	EOM_CHK_AMOUNT[3:0]				EOM_CHK_THR[1:0]		EOM_PER_MODE	EOM_EN
Reset	0x4				0x2		0x1	0x1
Access Type	Write, Read				Write, Read		Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_CHK_AMOUNT	7:4	Number of samples collected in a measurement window (unit: millions)	0xX: N factor
EOM_CHK_THR	3:2	Eye-opening monitor number of error bits to allow in a measurement window	0b00: Allow no errors 0b01: Allow one error 0b10: Allow two errors 0b11: Allow three errors
EOM_PER_MODE	1	Eye-opening monitor periodic mode enable	0b0: Eye-opening monitor periodic mode disabled 0b1: Eye-opening monitor periodic mode enabled
EOM_EN	0	Eye-opening monitor enable	0b0: Eye-opening monitor disabled 0b1: Eye-opening monitor enabled

RLMS5 (0x1405, 0x1505, 0x1605, 0x1705)

BIT	7	6	5	4	3	2	1	0
Field	EOM_MAN_TRG_REQ	EOM_MIN_THR[6:0]						
Reset	0x0	0x10						
Access Type	Write Only	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_MAN_TRG_REQ	7	Eye-opening monitor manual trigger. For use when periodic mode is disabled.	0b0: No action 0b1: EOM manual trigger request
EOM_MIN_THR	6:0	Eye-opening measurement result lower than this flag's warning interrupt	0bXXXXXXX: EOM minimum threshold factor

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RLMS6 (0x1406, 0x1506, 0x1606, 0x1706)

BIT	7	6	5	4	3	2	1	0
Field	EOM_PV_MODE	EOM_RST_THR[6:0]						
Reset	0x1	0x00						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_PV_MODE	7	Eye-opening is measured vertically or horizontally	0b0: Vertical opening mode 0b1: Horizontal opening mode
EOM_RST_THR	6:0	Eye-opening measurement lower than this value resets the link. Disabled when set to 0.	0bXXXXXXX: EOM refresh threshold factor

RLMS7 (0x1407, 0x1507, 0x1607, 0x1707)

BIT	7	6	5	4	3	2	1	0
Field	EOM_DONE	EOM[6:0]						
Reset	0x0	0x00						
Access Type	Read Only	Read Only						

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_DONE	7	Eye-opening monitor measurement done	0b0: EOM not complete 0b1: EOM complete
EOM	6:0	Eye-opening measurement result	0bXXXXXXX: EOM measurement result

RLMS34 (0x1434, 0x1534, 0x1634, 0x1734)

BIT	7	6	5	4	3	2	1	0
Field	EyeMonPerCntL[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
EyeMonPerCntL	7:0	Eye-monitor period count (RxClk20) LSb	0xXX: Eye-monitor period count (least significant byte)

RLMS35 (0x1435, 0x1535, 0x1635, 0x1735)

BIT	7	6	5	4	3	2	1	0
Field	EyeMonPerCntH[7:0]							
Reset	0x00							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
EyeMonPerCntH	7:0	Eye-monitor period count (RxClk20) MSb	0xXX: Eye-monitor period count (most significant byte)

RLMS37 (0x1437, 0x1537, 0x1637, 0x1737)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	RSVD	EyeMonDone	EyeMonCntClr	EyeMonStart	EyeMonPh	EyeMonDPol
Reset	–	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	–			Read Only	Write Only	Write Only	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
EyeMonDone	4	Eye-monitor period complete (read-only, reset on start)	0b0: Eye-monitor data collection not complete 0b1: Eye-monitor data collection complete
EyeMonCntClr	3	Eye-monitor error/valid count clear (one-shot) Read-back is EyeMonClrPL from long-pulse generation	0b0: NA 0b1: Clear eye-monitor data collection counters
EyeMonStart	2	Eye-monitor start (one-shot) Read-back is EyeMonStClrPL from long-pulse generation for both start and clear	0b0: NA 0b1: Start eye-monitor data collection
EyeMonPh	1	Eye-monitor phase	0b0: Eye-monitor search early phase 0b1: Eye-monitor search late phase
EyeMonDPol	0	Eye-monitor data polarity	0b0: Eye-monitor search for 1's 0b1: Eye-monitor search for 0's

RLMS38 (0x1438, 0x1538, 0x1638, 0x1738)

BIT	7	6	5	4	3	2	1	0
Field	EyeMonErrCntL[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
EyeMonErrCntL	7:0	Eye-monitor error count (read-only)	0xXX: Eye-monitor error count (least significant byte)

RLMS39 (0x1439, 0x1539, 0x1639, 0x1739)

BIT	7	6	5	4	3	2	1	0
Field	EyeMonErrCntH[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
EyeMonErrCntH	7:0	Eye-monitor error count (read-only)	0xXX: Eye-monitor error count (most significant byte)

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RLMS3A (0x143A, 0x153A, 0x163A, 0x173A)

BIT	7	6	5	4	3	2	1	0
Field	EyeMonValCntL[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
EyeMonValCntL	7:0	Eye-monitor valid (hit) count (read-only)	0xXX: Eye-monitor valid count (least significant byte)

RLMS3B (0x143B, 0x153B, 0x163B, 0x173B)

BIT	7	6	5	4	3	2	1	0
Field	EyeMonValCntH[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
EyeMonValCntH	7:0	Eye-monitor valid (hit) count (read-only)	0xXX: Eye-monitor valid count (most significant byte)

RLMS3D (0x143D, 0x153D, 0x163D, 0x173D)

BIT	7	6	5	4	3	2	1	0
Field	ErrChPh[6:0]							ErrChPhTogEn
Reset	0x00							0x1
Access Type	Read Only							Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPh	7:1	Error channel phase (read-only)	0bXXXXXXX: 5.6 degrees per step
ErrChPhTogEn	0	Error channel phase toggle enable	0b0: Use primary phase only 0b1: Auto toggle phase between primary and secondary

RLMS3E (0x143E, 0x153E, 0x163E, 0x173E)

BIT	7	6	5	4	3	2	1	0
Field	ErrChPhSecTA	ErrChPhSec[6:0]						
Reset	0x1	0x33						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPhSecTA	7	Error channel phase secondary timing adjust	0b0: Timing adjust disabled 0b1: Timing adjust enabled

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BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPhSec	6:0	A 7-bit phase command used for eye monitoring and used during adaptation by the error channel. Value: 7'h3A	0bxxxxxxx: Error channel phase secondary (odd)

RLMS3F (0x143F, 0x153F, 0x163F, 0x173F)

BIT	7	6	5	4	3	2	1	0
Field	ErrChPhPriTA	ErrChPhPri[6:0]						
Reset	0x0	0x72						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPhPriTA	7	Error channel phase primary timing adjust	0b0: Timing adjust disabled 0b1: Timing adjust enabled
ErrChPhPri	6:0	A 7-bit phase command used for eye monitoring and used during adaptation by the error channel. Value 7'h79	0bxxxxxxx: Error channel phase primary (even)

RLMS45 (0x1445, 0x1545, 0x1645, 0x1745)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	–	–	–	RSVD[2:0]		
Reset	0x0	0x0	–	–	–	0x1		
Access Type	Write, Read	Write, Read	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	Reserved	Must write value of 0.
RSVD	6	Reserved	Must write value of 0.
RSVD	2:0	Reserved	Must write value of 0.

RLMS49 (0x1449, 0x1549, 0x1649, 0x1749)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	RSVD	RSVD	RSVD	ErrChPwrUp	–	RSVD
Reset	–	0x1	0x1	0x1	0b0	0x0	–	0x1
Access Type	–					Write, Read	–	

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPwrUp	2	Error channel power-up	0b0: Normal error channel operation 0b1: Force error channel power on

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RLMS58 (0x1458, 0x1558, 0x1658, 0x1758)

BIT	7	6	5	4	3	2	1	0
Field	–	ErrChVTh1[6:0]						
Reset	–	0x28						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChVTh1	6:0	Error channel target amplitude for ones. Bits 7, 5:0	0b0: Error channel power disabled 0b1: Error channel power enabled

RLMS59 (0x1459, 0x1559, 0x1659, 0x1759)

BIT	7	6	5	4	3	2	1	0
Field	–	ErrChVTh0[6:0]						
Reset	–	0x68						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChVTh0	6:0	Error channel target amplitude for zeros Bits 7, 5:0	0bxxxxxxx: Format: {sign, Magnitude[5:0]} where sign: 1 = negative, 0 = positive Magnitude: binary amplitude 4.7mV per count

RLMS64 (0x1464, 0x1564, 0x1664, 0x1764)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	RSVD	TxSSCMode[1:0]	
Reset	–	–	–	–	–	0x0	0x0	
Access Type	–	–	–	–	–		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCMode	1:0	Tx spread spectrum mode	0b00: Spread spectrum disabled 0b01: Reserved 0b10: Reserved 0b11: Spread spectrum enabled (center spread)

RLMS70 (0x1470, 0x1570, 0x1670, 0x1770)

BIT	7	6	5	4	3	2	1	0
Field	–	TxSSCFrqCtrl[6:0]						
Reset	–	0x01						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCFrqCtrl	6:0	Tx spread spectrum frequency control	0bXXXXXXX: Tx spread spectrum center frequency control

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RLMS71 (0x1471, 0x1571, 0x1671, 0x1771)

BIT	7	6	5	4	3	2	1	0
Field	–	TxSSCCenSprSt[5:0]						TxSSCEn
Reset	–	0x01						0x0
Access Type	–	Write, Read						Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCCenSprSt	6:1	Tx spread spectrum center spread startup control	0bXXXXXX: Tx spread spectrum center spread startup control
TxSSCEn	0	Tx spread spectrum enable	0b0: Tx spread spectrum disabled 0b1: Tx spread spectrum enabled

RLMS72 (0x1472, 0x1572, 0x1672, 0x1772)

BIT	7	6	5	4	3	2	1	0
Field	TxSSCPreSclL[7:0]							
Reset	0xCF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCPreSclL	7:0	Tx spread spectrum frequency pre-scaler	0xXX: Tx spread spectrum frequency pre-scaler low byte

RLMS73 (0x1473, 0x1573, 0x1673, 0x1773)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TxSSCPreSclH[2:0]		
Reset	–	–	–	–	–	0x0		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCPreSclH	2:0	Tx spread spectrum frequency pre-scaler	0bXXX: Tx spread spectrum frequency pre-scaler high bits

RLMS74 (0x1474, 0x1574, 0x1674, 0x1774)

BIT	7	6	5	4	3	2	1	0
Field	TxSSCPhL[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCPhL	7:0	Tx spread spectrum interpolator phase	0xXX: Tx spread spectrum frequency interpolator phase low byte

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RLMS75 (0x1475, 0x1575, 0x1675, 0x1775)

BIT	7	6	5	4	3	2	1	0
Field	–	TxSSCPhH[6:0]						
Reset	–	0x0						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCPhH	6:0	Tx spread spectrum interpolator phase	0bXXXXXXX: Tx spread spectrum frequency interpolator phase high bits

RLMS76 (0x1476, 0x1576, 0x1676, 0x1776)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	TxSSCPhQuad[1:0]	
Reset	–	–	–	–	–	–	0x0	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCPhQuad	1:0	Tx spread spectrum interpolator phase quadrant	0xbXX: Tx spread spectrum interpolator phase quadrant

RLMS95 (0x1495, 0x1595, 0x1695, 0x1795)

BIT	7	6	5	4	3	2	1	0
Field	TxAmplManEn	RSVD	TxAmplMan[5:0]					
Reset	0x0	0x1	0x29					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
TxAmplManEn	7	Tx amplitude manual override	0b0: Do not manually override Tx amplitude 0b1: Manually override Tx amplitude
TxAmplMan	5:0	Tx amplitude	0bXXXXXX: Binary amplitude 10mV per count

RLMS98 (0x1498, 0x1598, 0x1698, 0x1798)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD[2:0]			Rxhpf_cnt[2:0]		
Reset	0x0	0x1	0x0			0x0		
Access Type						Write, Read		

BITFIELD	BITS	DESCRIPTION
Rxhpf_cnt	2:0	Rxhpf_cnt value during RLMS (MSB = Enable)

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RLMSA4 (0x14A4, 0x15A4, 0x16A4, 0x17A4)

BIT	7	6	5	4	3	2	1	0
Field	AEQ_PER_MULT[1:0]		AEQ_PER[5:0]					
Reset	0x2		0x3D					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
AEQ_PER_MULT	7:6	Adaptive EQ period multiplier	0b00: 1ms 0b01: 4ms 0b10: 16ms 0b11: 64ms
AEQ_PER	5:0	Adaptive EQ Period Periodic adaptation is disabled when value is zero. Adaptive EQ period is (AEQ_PER value times AEQ_PER_MULT)	0bXXXXXX: Only zeros have a special meaning

RLMSAC (0x14AC, 0x15AC, 0x16AC, 0x17AC)

BIT	7	6	5	4	3	2	1	0
Field	ErrChPhSecTAFR3G	ErrChPhSecFR3G[6:0]						
Reset	0x1	0x4D						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPhSecTAFR3G	7	Error channel phase secondary timing adjust	0b0: Timing adjust disabled 0b1: Timing adjust enabled
ErrChPhSecFR3G	6:0	A 7-bit phase command used for eye monitoring and used during adaptation by the error channel. (Fast Receive, Secondary Phase, 3Gbps)	0bXXXXXXX: 7'h4D

RLMSAD (0x14AD, 0x15AD, 0x16AD, 0x17AD)

BIT	7	6	5	4	3	2	1	0
Field	ErrChPhPriTAFR3G	ErrChPhPriFR3G[6:0]						
Reset	0x0	0x0D						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPhPriTAFR3G	7	Error channel phase primary timing adjust	0b0: Timing adjust disabled 0b1: Timing adjust enabled

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BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPhPriFR3G	6:0	A 7-bit phase command used for eye monitoring and used during adaptation by the error channel. (Fast Receive, Primary Phase, 3Gbps)	0bXXXXXXX: 7'h0D

RLMSB6 (0x14B6, 0x15B6, 0x16B6, 0x17B6)

BIT	7	6	5	4	3	2	1	0
Field	ErrChPhSecTASRG1875	ErrChPhSecSRG1875[6:0]						
Reset	0x1	0x3B						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPhSecTASRG1875	7	Error channel phase secondary timing adjust	0b0: Timing adjust disabled 0b1: Timing adjust enabled
ErrChPhSecSRG1875	6:0	A 7-bit phase command used for eye monitoring and used during adaptation by the error channel. (Slow Receive, Secondary Phase, 187.5Mbps)	0bXXXXXXX: 7'h3B

RLMSB7 (0x14B7, 0x15B7, 0x16B7, 0x17B7)

BIT	7	6	5	4	3	2	1	0
Field	ErrChPhPriTASRG1875	ErrChPhPriSRG1875[6:0]						
Reset	0x0	0x7A						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPhPriTASRG1875	7	Error channel phase primary timing adjust	0b0: Timing adjust disabled 0b1: Timing adjust enabled
ErrChPhPriSRG1875	6:0	A 7-bit phase command used for eye monitoring and used during adaptation by the error channel. (Slow Receive, Primary Phase, 187.5Mbps)	0bXXXXXXX: 7'h7A

RLMSC4 (0x14C4, 0x15C4, 0x16C4, 0x17C4)

BIT	7	6	5	4	3	2	1	0
Field	RevTrfManEn	RevTrfMan[2:0]			–	RevFast	–	–
Reset	0b0	0x4			–	0b0	–	–
Access Type	Write, Read	Write, Read			–	Write, Read	–	–

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BITFIELD	BITS	DESCRIPTION	DECODE
RevTrfManEn	7	Enable manual override of reverse channel rise/fall time setting	0x0: Disable manual override 0x1: Enable manual override
RevTrfMan	6:4	GMSL1 manual rise/fall time setting	0b000: Slowest rise/fall time ... 0b111: Fastest rise/fall time
RevFast	2	GMSL1 reverse channel fast mode	0b0: Reverse channel fast mode disabled 0b1: Reverse channel fast mode enabled

RLMSC5 (0x14C5, 0x15C5, 0x16C5, 0x17C5)

BIT	7	6	5	4	3	2	1	0
Field	RevLenManEn	RevFLenMan[6:0]						
Reset	0b0	0x40						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
RevLenManEn	7	Enable manual override of reverse channel pulse length	0b0: Disable manual override 0b1: Enable manual override
RevFLenMan	6:0	GMSL1 reverse channel first pulse length (x 6.666 ns)	0bXXXXXXX: GMSL1 reverse channel first pulse length (x 6.666 ns)

RLMSD1 (0x14D1, 0x15D1, 0x16D1, 0x17D1)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[2:0]			RSVD[2:0]			RSVD	RSVD
Reset	0x4			0x2			0x0	0x0
Access Type	Write, Read			Write, Read			Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7:5	Reserved	Must write value of 0.
RSVD	4:2	Reserved	Must write value of 0.
RSVD	1	Reserved	Must write value of 1.
RSVD	0	Reserved	Must write value of 1.

DPLL_0 (0x1C00)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	config_soft_rst_n
Reset	0x1	0x1	0x1	0x1	0x0	0x1	0x0	0x1
Access Type								Write, Read

BITFIELD	BITS	DESCRIPTION
config_soft_rst_n	0	Setting this to 1 resets the PLL functional registers; config_regs are not reset.

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DPLL_0 (0x1D00)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	config_soft_rst_n
Reset	0x1	0x1	0x1	0x1	0x0	0x1	0x0	0x1
Access Type								Write, Read

BITFIELD	BITS	DESCRIPTION
config_soft_rst_n	0	Setting this to 1 resets the PLL functional registers; config_regs are not reset.

DPLL_0 (0x1E00)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	config_soft_rst_n
Reset	0x1	0x1	0x1	0x1	0x0	0x1	0x0	0x1
Access Type								Write, Read

BITFIELD	BITS	DESCRIPTION
config_soft_rst_n	0	Setting this to 1 resets the PLL functional registers; config_regs are not reset.

DPLL_0 (0x1F00)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	config_soft_rst_n
Reset	0x1	0x1	0x1	0x1	0x0	0x1	0x0	0x1
Access Type								Write, Read

BITFIELD	BITS	DESCRIPTION
config_soft_rst_n	0	Setting this to 1 resets the PLL functional registers; config_regs are not reset.

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/19	Initial Release	—

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REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
1	7/20	This document is published directly from contour. Some formatting and page numbers may be changed relative to revision 0 as a result. 1. add line-fault detection feature: Benefits and Features Simplified Block Diagram Electrical Characteristics Pin Description Detailed Block Diagram External Components Table GMSL1 Feature Availability Table MFP Pin Function Map Detailed Description Text Register Map (registers 0x27, 0x28; registers 0xE0 to 0xE6) 2. change "Single Ended Output Impedance Mismatch" specifications for D-PHY and C-PHY HS transmitters from TYP to MAX in Electrical Characteristics Table 3. simplify power supply current conditions in Electrical Characteristics Table 4. change C-PHY data rate from 5200M to 5700M in power supply current conditions in Electrical Characteristics Table 5. update GMSL2 lock time specification in Electrical Characteristics Table, add MAX specification 6. change parameter name of C-PHY and D-PHY tREOT specification to "30% to 85% Rise Time" in Electrical Characteristics Table 7. change C-PHY and D-PHY differenetial mode and common mode reflection coefficient specifications from MAX to TYP in Electrical Characteristics Table 8. update SPI Master and SPI Slave timing specifications and diagrams for improved clarity Electrical Characteristics Functional Diagrams 9. add external SIO_N termination resistors to External Components Table 10. update figures 30, 31, 33, and 34 in Detailed Description to clarify video routing constraints 11. remove statement in Detailed Description text that mentions that HVD monitor bits are only available in GMSL2 mode. This function is now available in GMSL1 mode 12. remove MIPI spread spectrum feature Detailed Description Register Map 13. remove UART permanent bypass mode Applications Information Register Map 14. add power supply monitoring features (register 0x12; registers 0x46 - 0x4A) 15. remove GPIO_TX_CASC bits (register map) 16. clarification of WM_0 register fields (register map) 17. fixed bug in phy3_lane_map 18. add register 0x03 19. Add register 0x49 20. Add LIM_HEART in registers 0x106/0x118/0x12A/0x13C/0x14E/0x166/0x178/0x18A 21. Reduce SPI Master maximum clock frequency to 25MHz 22. Remove power up default from GPIO4 description (GPIO4 is not a default function) 23. Remove power up default from GPIO14 description (GPIO14 is not a default function) 24. Add register 0x06C2, bit 4 25. Add bits [1:0] in registers 0x14D1, 0x15D1, 0x16D1, 0x17D1 26. Updated Applications Information Section for improved organizational clarity 27. Edited PATGEN_MODE and GRAD_MODE decode in registers 0x1051 and 0x1081 28. Noted MFP pin power-down state in Power-up and Link Start-up Section 29. remove all instances of registers RLMSAE, RLMSAF, RLMSB0, RLMSB1, RLMSB2, RLMSB3, RLMSB4, RLMSB5 (4 instances of each) 30. remove TX_PRIO feature from all GPIO pin functions in register table 31. Mandatory configuration of registers 0x14D1, 0x15D1, 0x16D1, 0x17D1, and 0x6C2 specified on first page of register table	see sections associated with each change

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		32. update VDD18 power supply current TYP and MAX specifications in EC Table 33. Clearly specify "4 video pipes enabled" in GMSL2 power supply current conditions 34. Updated GMSL2 Lock Time Figure. 35. Update TLOCK parameter name in EC table to TLOCK1 (GMSL1) and TLOCK2 (GMSL2) for improved clarity	
2	10/20	Updated cabling options information on first page General Description and in Detailed Description section. Opened registers 0x6C2, 0x1445, 0x1545, 0x1645, and 0x1745. Added note to the programming notes section in the register table stating :“Set bits [2:0] = 3’b000 in registers 0x1445, 0x1545, 0x1645, 0x1745”. fixed typo in units of PWDNB Hold Time specification.	1, 15, 16, 69, 86, 124, 158, 159, 160, 162, 408, 527
3	7/21	Added B variant to allow RoR; updated General Description, Benefits and Features, Absolute Maximum Ratings, Electrical Characteristics table, Note 2, Pin Description, Functional Block Diagram, Introduction, Product Overview, GMLS2 Overview, Video Pipes, Aggregation, and Replication, Watermarking, Video Line CRC, Video Timing Monitor, Control Channel and Side Channels, I^2C/UART, SPI, General Purpose Inputs and Outputs (GPIO), GMSL2 Physical Layer, Cabling Options, Video PRBS Generator/Checker, added RoR (Reference over Reverse), updated GMSL1 Backwards Compatibility, Table 6, CSI Video Output Ports, Video Pattern Generator, Video PRBS Generator/Checker, CSI Output Raw PRBS Generator, CFG Latch at Power-up Pins, Multifunction Pin Configuration, Speed Programming for SPI, Link Lock, Error and Fault Condition Monitoring, Line-Fault, Power Supplies, Standby and Sleep Mode, Thermal Management, Control-Channel Programming, Main I^2C Host-to-GMSL2 Device Communication, Ordering Information, Programming Notes, Register Details, REG13 (0xD), ARQ0 (0x585), ARQ0 (0x5A5), ARQ1 (0x5B5), ARQ0 (0x5D5), REG13 (0xD), GMSL1_96 (0xB96, 0xC96, 0xC96, 0xD96, 0xE96), GMSL1_A7 (AxBA7, 0xCA7, 0DA7, 0xEA7), and added MIPI Notice of Disclaimer	1–550
4	11/23	Front Page: Added recommended cable length table. Package Information: Added "in still air" after "four-layer board." EC Table: 1. Added "+" to positive temps for clarity. 2. Added lock time note. 3. Increased typ i2c wake time. 4. Moved ESD table to align with other datasheets. ESD moved to its own section. External components: Matched formating with the MAX96722. Detailed Description: 1. Added references to other documents. 2. Removed explicit mention of 1MHz operation. 3. Removed priority programming from description. 4. Added limitations to video timing. 5. Added reccomendation not to use RESET_ALL with sleep. 6. Added link lock note. 7. Changed spread range from +/-2500ppm to 2500ppm pk-pk. Register table: 1. Added error channel power up writes. 2. Added and fixed CNTL OUT_ORD and CNTL_OUT_EN WM_YUV_IN errchpwrup TX Ampl Man and enable Rxhpf_cnt RevtRFMAN. Applications information: Added Software programming model section. Global: Words matter initiative.	1-504

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