

- 1.9

- a

The CPU first sets up the DMA registers, containing a pointer to the source of a transfer, a pointer to the destination, and a counter of the size to be transferred. Then the DMA controller proceeds to place addresses on the bus to perform transfers, while the CPU is available to accomplish other work.

- b

When the transfer is finished, the DMA controller interrupts the CPU.

- c

If the CPU has the access to the memory when DMA controller is transferring data, a coherency issue may occur if both CPU and DMA controller update the same memory location.

- 2.7

Message-passing and shared-memory model.

The shared-memory model is faster, but memory protection and synchronization problems may occur.

The Message-passing model is easier to implement, but it is slower because of the time usage of connection setup.

- 3.1

- Short-term : Selects from jobs in memory those jobs that are ready to execute and allocates the CPU to them.
- Medium-term : Used especially with time-sharing systems as an intermediate scheduling level. A swapping scheme is implemented to remove partially run programs from memory and reinstate them later to continue where they left off.
- Long-term: Determines which jobs are brought into memory for processing.