1. Project 2 Description

ALU Design.

2. Objective

Design a scaled-down version of a microprocessor module to achieve an in-depth understanding of design trade-offs associated with CMOS digital circuits.

3. Basic Operation

The block diagram of the ALU is shown in Fig. 1. A, B, C, and SEL are inputs. Y is the output. Each bit of the output vector Y drives a 50fF load. A and B are operands. Assume both A and B to be unsigned inputs. SEL selects the type of function to be performed. C is an additional control input that is used only with certain functions. The operation of the ALU is given in Table I:

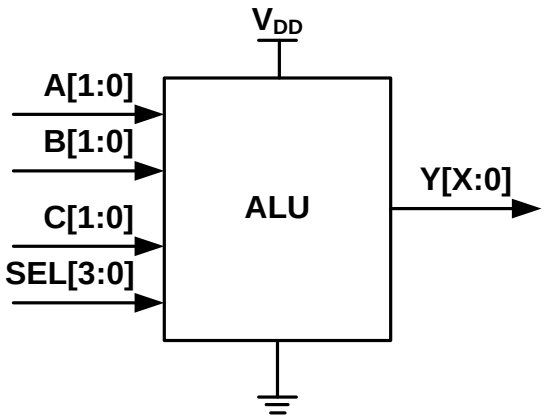

Figure 1. ALU

Table I: Operation of the ALU

SEL	C	Y (Function)
000	Don't care	Add A to B
001	Don't care	Subtract B from A
010	Don't care	Multiply A with B
011	Don't care	Divide B by A
100	00: No shift 01: 1-bit shift 10: 2-bit shift 11: 3-bit shift	Logical shift left of A
101	Don't care	Bitwise NOR operation of A1 and B1 concatenated with bitwise NOR operation of A0 and B0
110	Don't care	Bitwise NAND operation of A1 and B1 concatenated with bitwise NAND operation of A0 and B0
111	Don't care	Z[X:0] – Tri-stated outputs

4. Detailed Specification

a) You may select any one CMOS logic family for the implementation.
b) Your design must use only one Vdd source, which is 1.8V.
c) All inputs and outputs should swing between 0V and 1.8V.
d) All inputs should have a 10%-90% rise/fall time of ~100ps.
e) A[1:0] = 01 means MSB is 0 and LSB is 1.

5. Implementation

You are expected to complete the ALU circuit design, schematic-level simulation, layout, and post-layout simulation. Next, you will need to measure key performance metrics including delay, area, active power, and standby power consumption using appropriate functions from the Cadence built-in calculator tool.

Suggested approach:
Think about the design and complete the schematic first. Then perform a schematic-level (behavioral) simulation to ensure your design meets the specification. Next, very briefly optimize your design for speed, power and area. Then, design an optimized layout in terms of silicon area, parasitic resistance, and capacitance. Reduce the capacitance and resistance of critical nodes by careful transistor/wire sizing and routing. Finally, route the power and ground tracks. Perform post-layout simulations to gather data for the Figure of Merit, FoM (explained below).

6. Figure of Merit

Your design will be evaluated using the following Figure of Merit (FoM). All values must be taken from post-layout simulation data.

FoM = (1/Layout area) * (1/Switching power) * (1/Leakage power) * (1/Delay)

The higher the FoM metric, the better your design will be and the higher your project grade will be. The group with the highest FoM will be given the highest points. For the FoM calculation, all simulations must be performed in the Typical corner (Typical NMOS Typical PMOS), at T = 80 Deg C, and VDD = 1.8V.

Layout area : The total area that your implementation occupies. To calculate the area of the layout, open the top cell (click on *Design* → *Properties*) to display the coordinates of the outermost boundary box of your layout (Fig. 2). These coordinates can then be used to calculate the area of the layout.

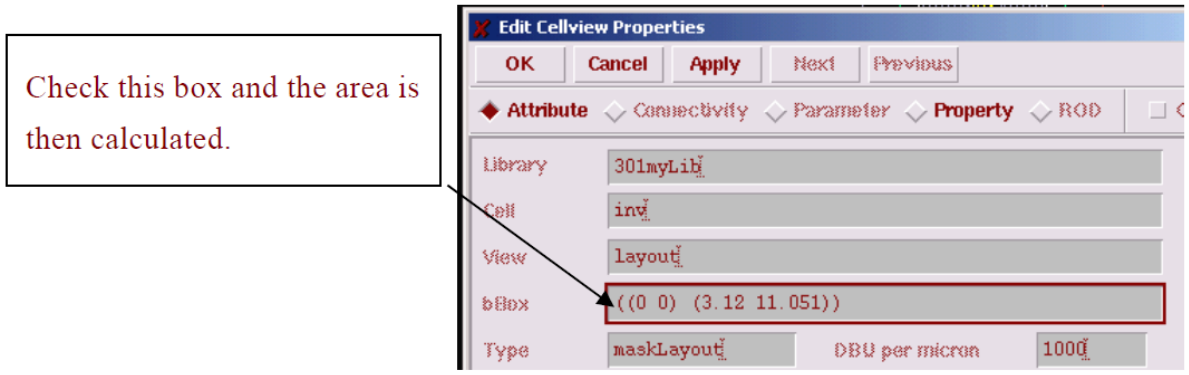

Figure 2. Calcultion of layout area

Switching power : This is the dynamic switching power of the ALU when performing a multiplication operation. Initially, both A and B are 00. The output Y is also 0. Then A changes to 11 and B changes to 01. You need to measure the switching power consumed for this multiplication. C is fixed at 1 and SEL is fixed at 010.

Leakage power : The total standby power consumed by the ALU after the above-mentioned multiplication operation has been completed.

Delay : Set A and B to 00. Then toggle A to 11 and B to 01. Set SEL to 010 and C to 1. Calculate the delay between the inputs toggling (at 50% transition) to when the last bit of the output Y becomes stable (at 50% transition).

7. Grading

This project is worth 20% of the total course grade. 5% is allocated to the Q&A session during the presentation. 10% is allocated to the post-layout functionality of the ALU and other requirements mentioned in Section 9 below. 5% is allocated to the FoM achieved by your design (compared to all other groups in class).

8. Group Work

You will be working in groups of 2, according to the groups you have already formed. The work of the project should be done jointly. You are responsible for time management, workload and task distribution. You are required to sign a declaration indicating the relative amount of work (in %) each member of the group has contributed.

9. Project Report & Demonstration

Describe your work in a report which will highlight the performance of your circuit. Explain your choice of the CMOS logic family selected and the transistor sizing methodology used. Include a detailed schematic and layout of your circuit. Highlight the size of key transistors. Describe how your layout was optimized and show the result of your LVS check. Clearly show the floor-planning used to minimize silicon area. Your floorplan needs to clearly show the distribution of all the signals and power/ground tracks. Also comment on the number of metal layers used in your layout. Finally, be prepared to demonstrate the operation of your circuit and answer questions during the demonstration session.

Report Format:

A sample report has been given to you already. Please use that format to complete your report. Both projects will have an individual (i.e. separate) report.
Include group information: Names and Student IDs
Maximum number of pages: 20
Font type: Times New Roman
Font size: 12
Page margins: At least 0.7" on all sides

You are not allowed to copy figures from other sources in your report. You need to draw (with Cadence, Visio, or some other tool) all the figures that you will present in the report. Make sure the figures are clearly readable. The report also needs to have the following information:

(a) The operation of the adder (A = 11 and B = 01) in the Slow corner, (Slow NMOS Slow PMOS), at T = 125 Deg C, and VDD = 1.71V.
(b) The operation of the subtractor (A = 10 and B = 01) in the Fast corner, (Fast NMOS Fast PMOS), at T = –40 Deg C, and VDD = 1.89V.
(c) The operation of the divider (A = 10 and B = 10) in the Typical corner, (Typical NMOS Typical PMOS), at T = 80 Deg C, and VDD = 1.8V.
(d) Logical shift of A: (A = 01 and B = Don't care) in the Typical corner, (Typical NMOS Typical PMOS), at T = 80 Deg C, and VDD = 1.8V when C = 00, 01, 10, and 11.
(e) Bitwise NOR when A = 01 and B = 00 in the Typical corner, (Typical NMOS Typical PMOS), at T = 80 Deg C, and VDD = 1.8V. C = Don't care.
(f) Bitwise NAND when A = 11 and B = 10 in the Typical corner, (Typical NMOS Typical PMOS), at T = 80 Deg C, and VDD = 1.8V. C = Don't care.
(g) When SEL = 111, C = 0, A = 11 and B = 00. Perform post-layout simulation in the Typical corner to show that all output bits are tri-stated. Find the most convenient way to demonstrate/prove tri-stated outputs.

The due date for the report is Nov 28. The demonstrations will be scheduled from 9:00am to 6:00pm on Nov 29-30. The exact schedule for each project group will be announced later. All group members are required to be present during the project demonstration.

10. Cheating & Copying

Cheating in any form (whether from other groups, former groups, or online forums) will be severely penalized. The students who are identified to copy (any form of plagiarism) will get a direct 'F' grade in this course. Additional sanctions and penalties will also be imposed by the department and the school.

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