Implementation task 12

Group 23

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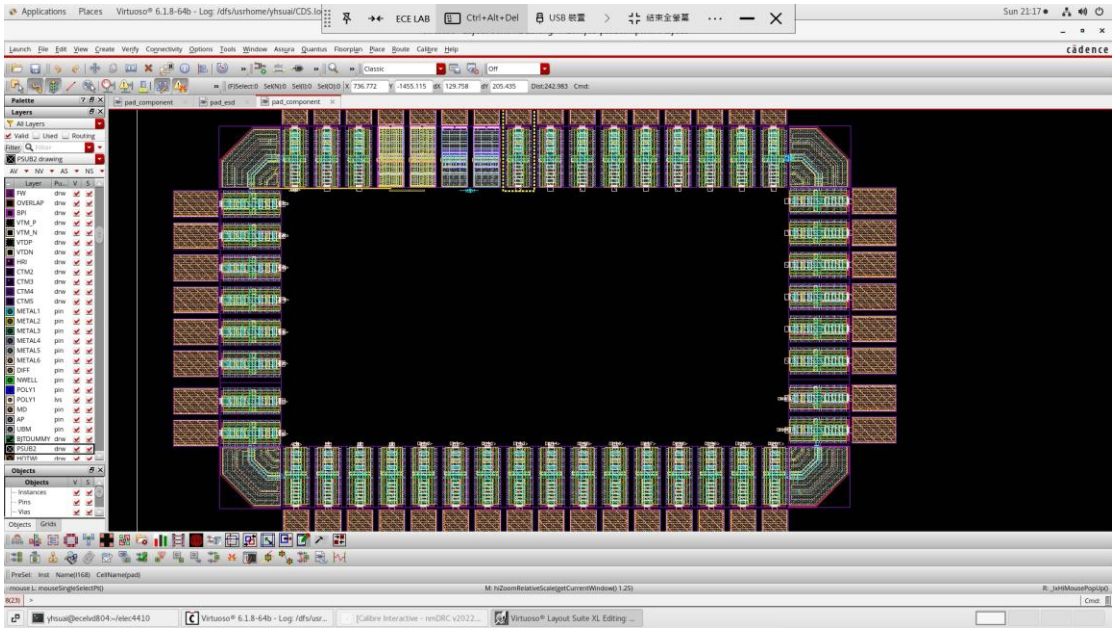
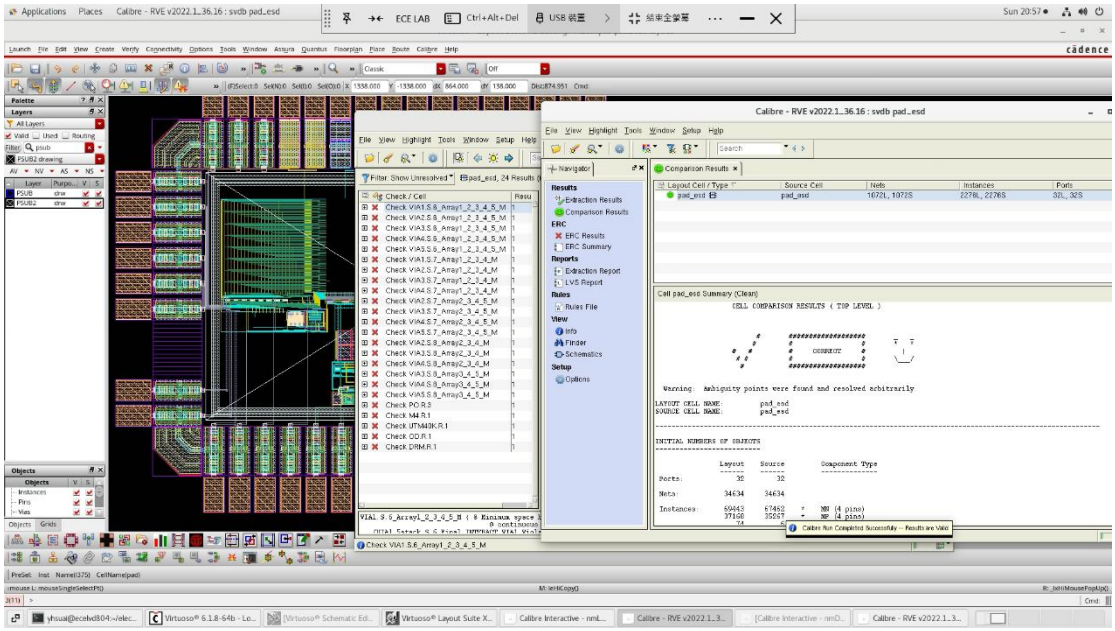
Group member responsible for this task: Hsu, Yung-hsiang

A



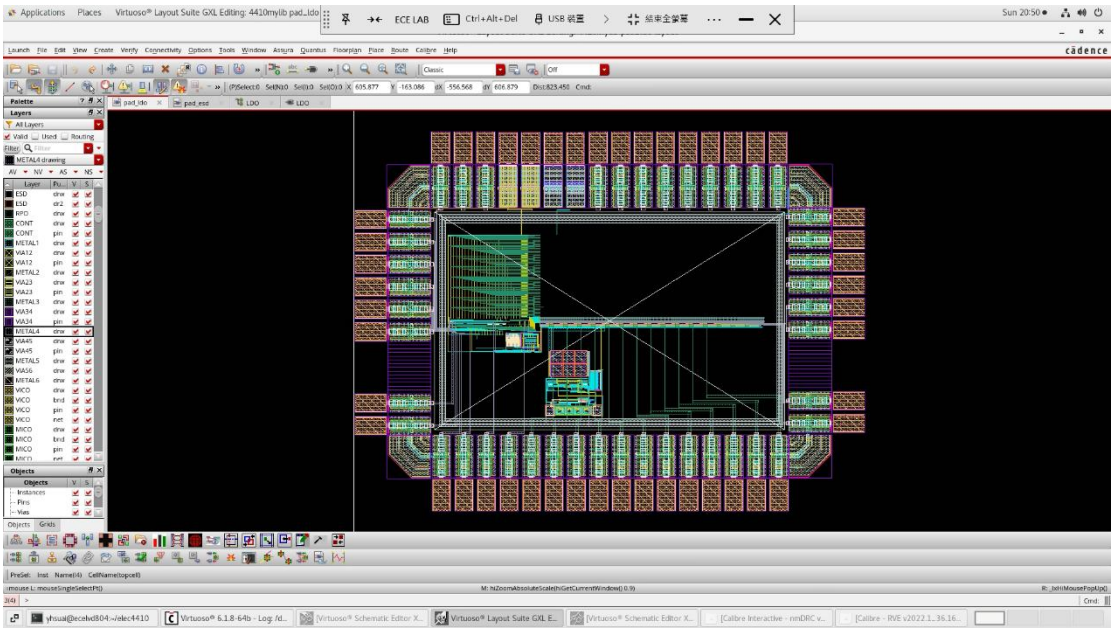
Layout of pad and esd

B



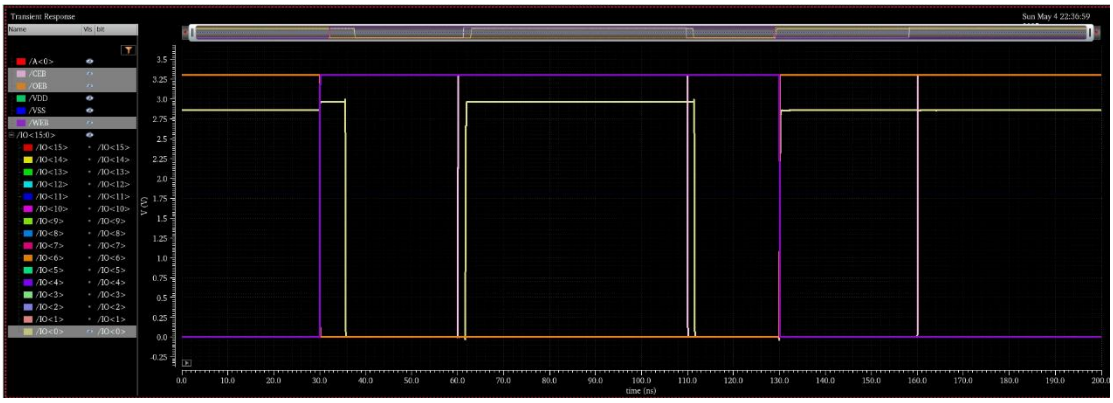
DRC and LVS of entire sram

C



Entire layout of the final chip with grid the height have been extended compare to above one as the space is not enough

D



The i/o pad is initial to be 3.3V, I have use a transmission gate to make sure the initial data won’t go in pad during read so the IO<0> didn’t go to 3.3, the delay is about 32ns