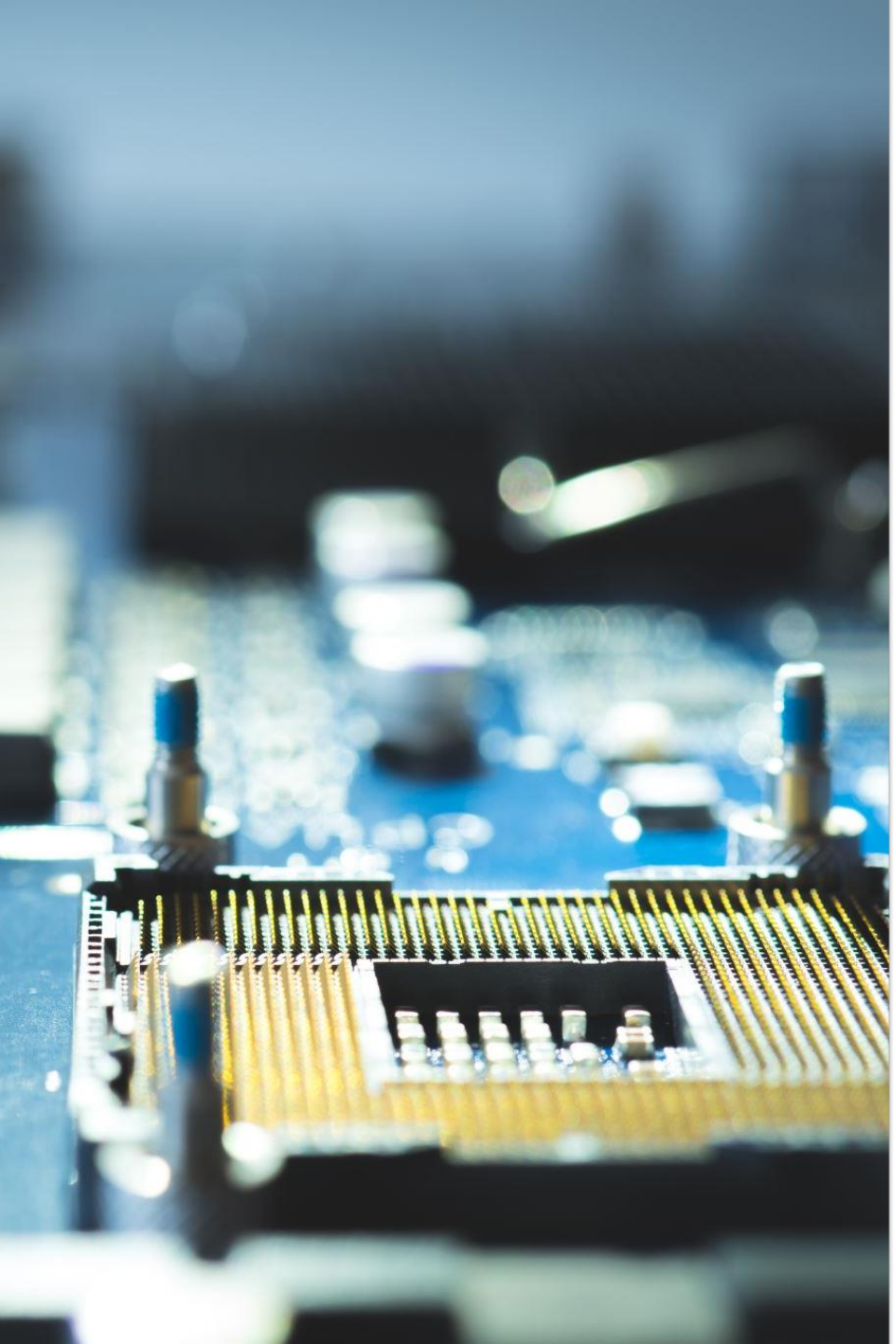
LOW-POWER SRAM CHIP DESIGN

HSU, Yung-Hsiang

YU, Kuang Jung

NG, Cheuk Hei



INTRODUCTION

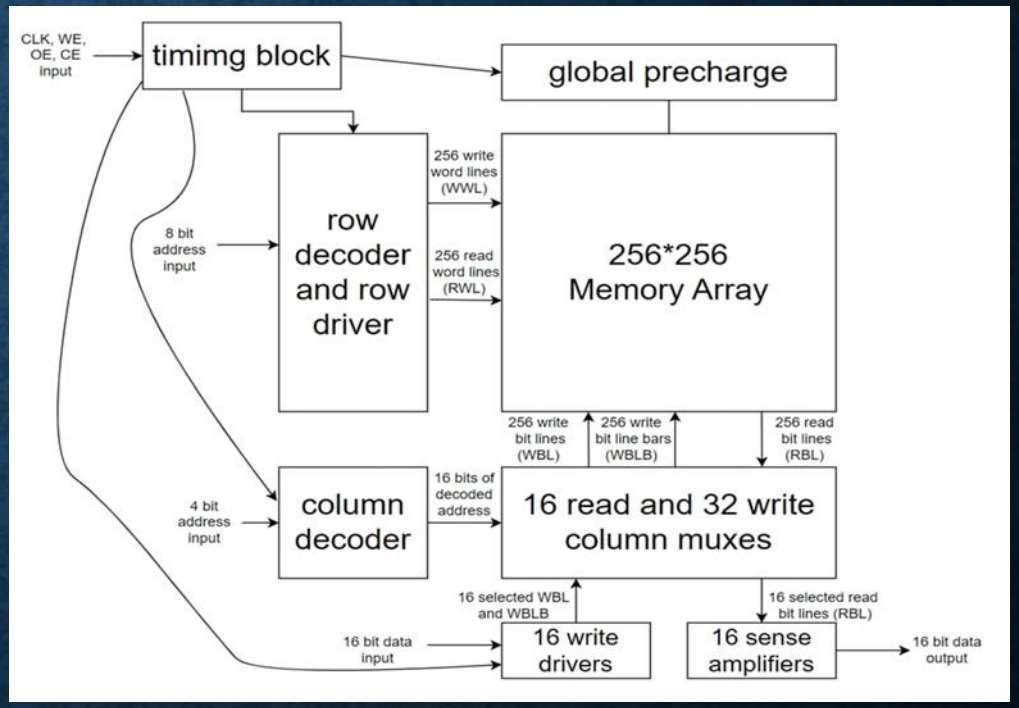
- SRAM (Static Random Access Memory)
- Volatile read-write memory
- Faster but larger area compared to DRAM(Dynamic Random Access Memory)
- High in the memory hierarchy (i.e. internal registers of the CPU and Level-1/2/3 cache)

OBJECTIVE

- Implement essential components of an SRAM
- Reading paper and understand ideas that express novelty on top of existing designs
- Design an SRAM that strikes a balance between area, cost, performance and power consumption
- Complete the layout and simulation of the SRAM

METHODOLOGY

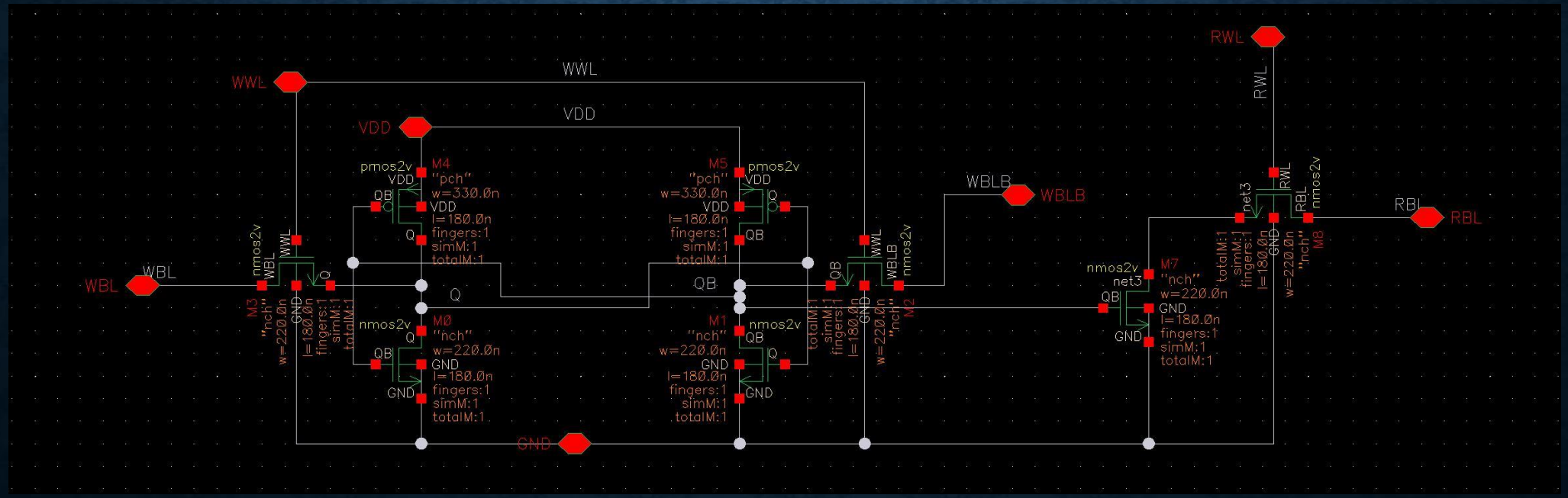
- Bit cell
- Array design(precharge, write driver, row driver, column mux, sense amplifier)
- Decoder
- Timing circuit
- Top level verification



Block diagram of our SRAM design

BIT CELL

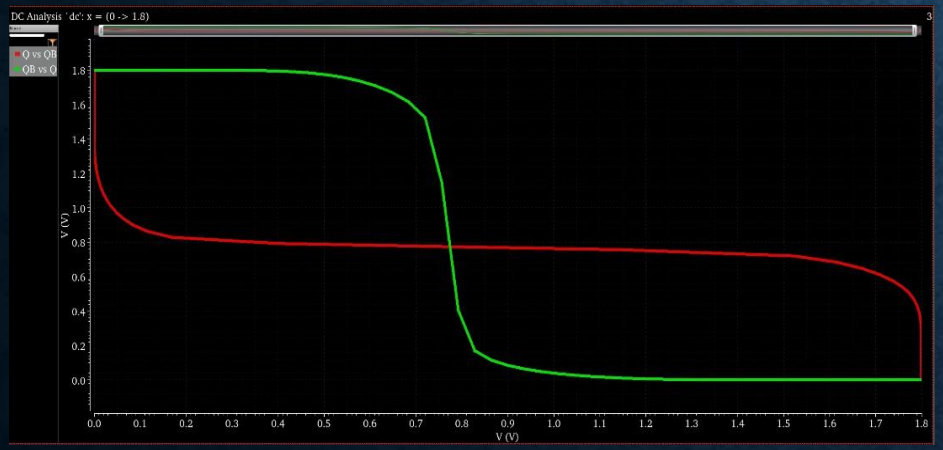
- Conventional 8-T SRAM bitcell
- Pull-up ratio = 1.5, cell ratio = 1
- Smallest width for access and read transistors



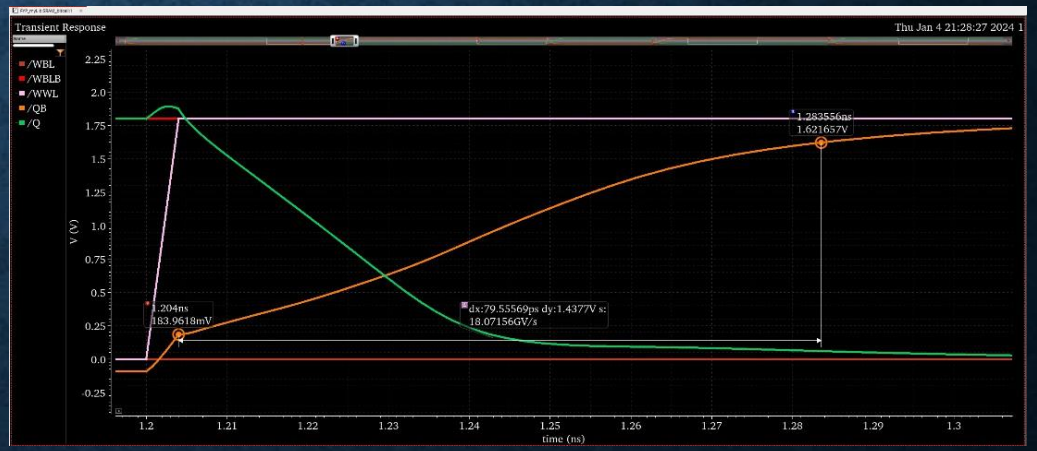
Schematic of bitcell circuit

BIT CELL - SIMULATION

- HSNM(hold static noise margin) : about 0.64V
- Dynamic Write Margin: about 80ps



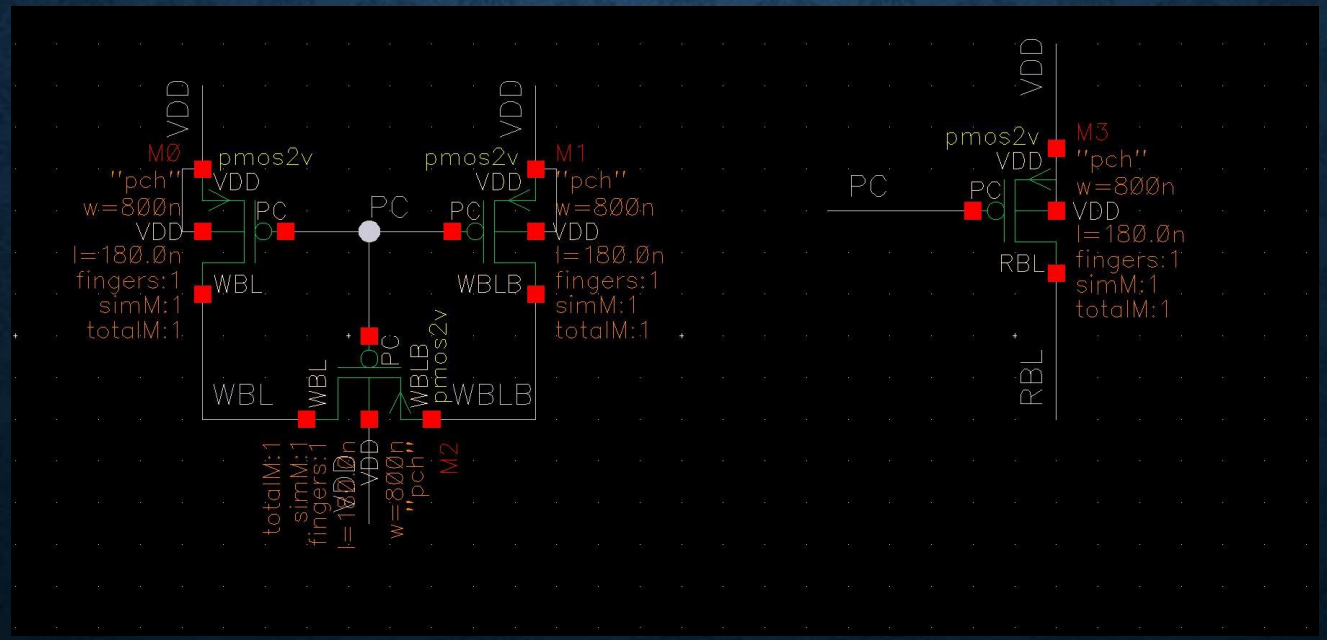
DC simulation - HSNM



transient analysis - dynamic write margin

MEMORY ARRAY – PRECHARGE CIRCUIT

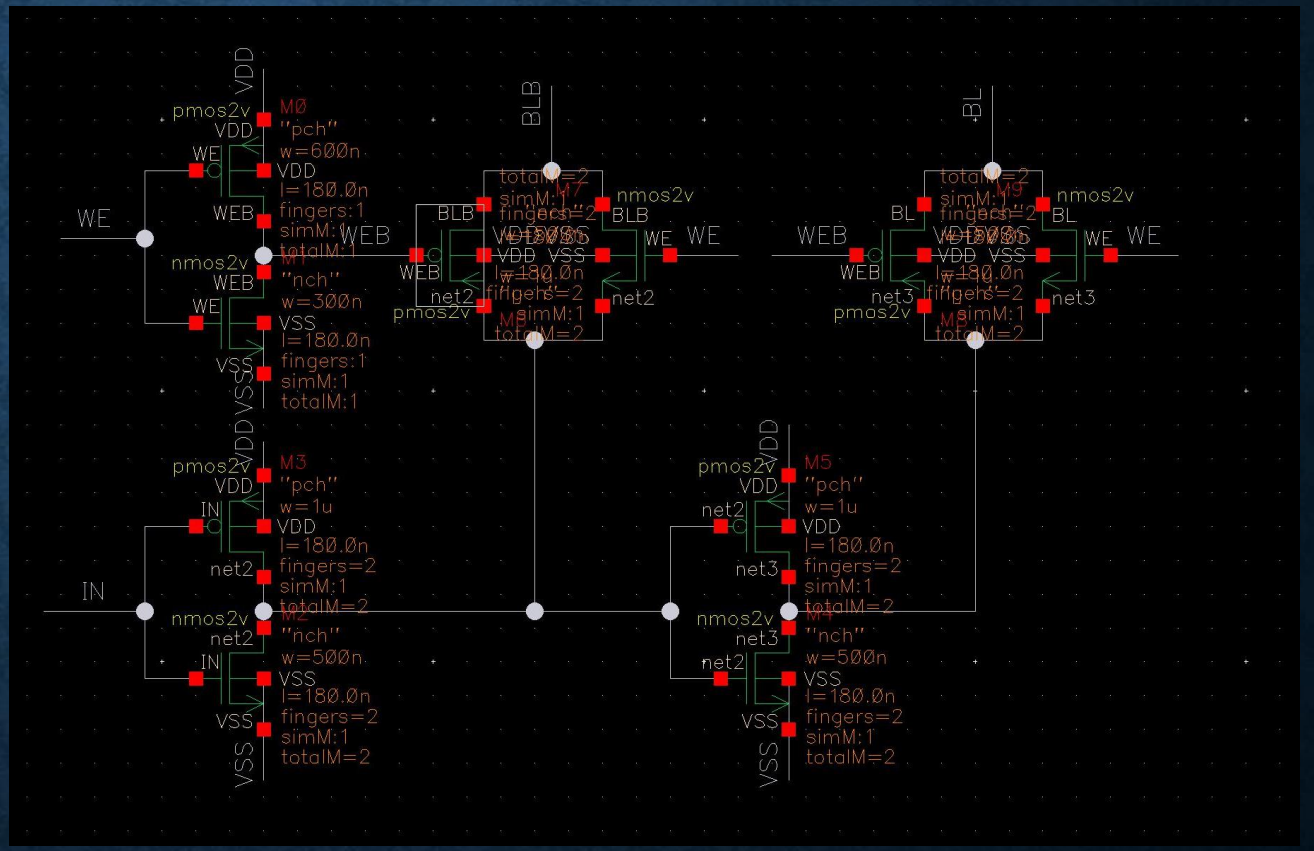
- Read and write bitlines precharged together
- Transistors upsized for faster precharge
- PMOS between WBL/WBLB to account for variation



Schematic of precharge circuit

MEMORY ARRAY – WRITE DRIVER

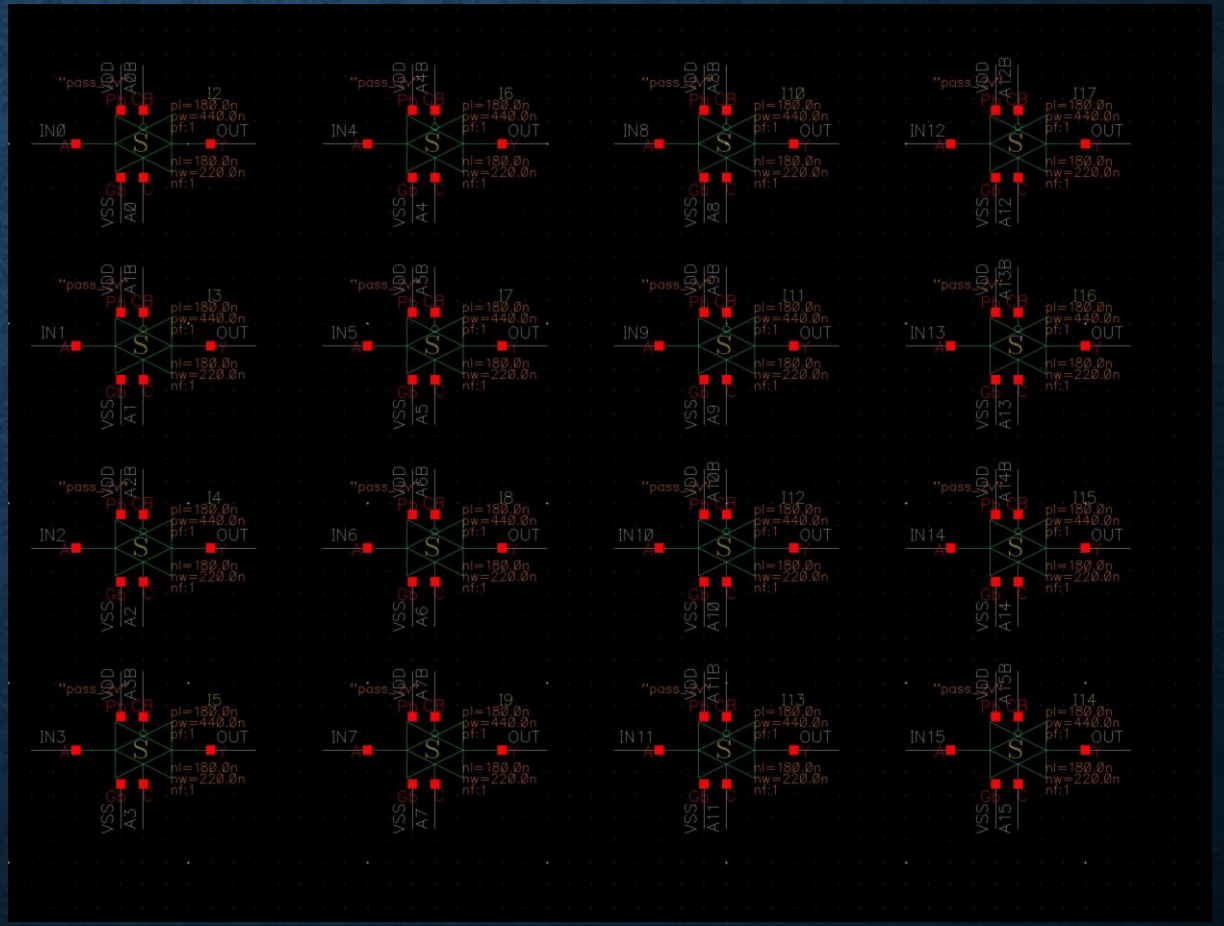
- Two transmission gates to drive WBL/WBLB
- Transmission gates upsized for better performance



Schematic of write driver

MEMORY ARRAY – COLUMN MUX

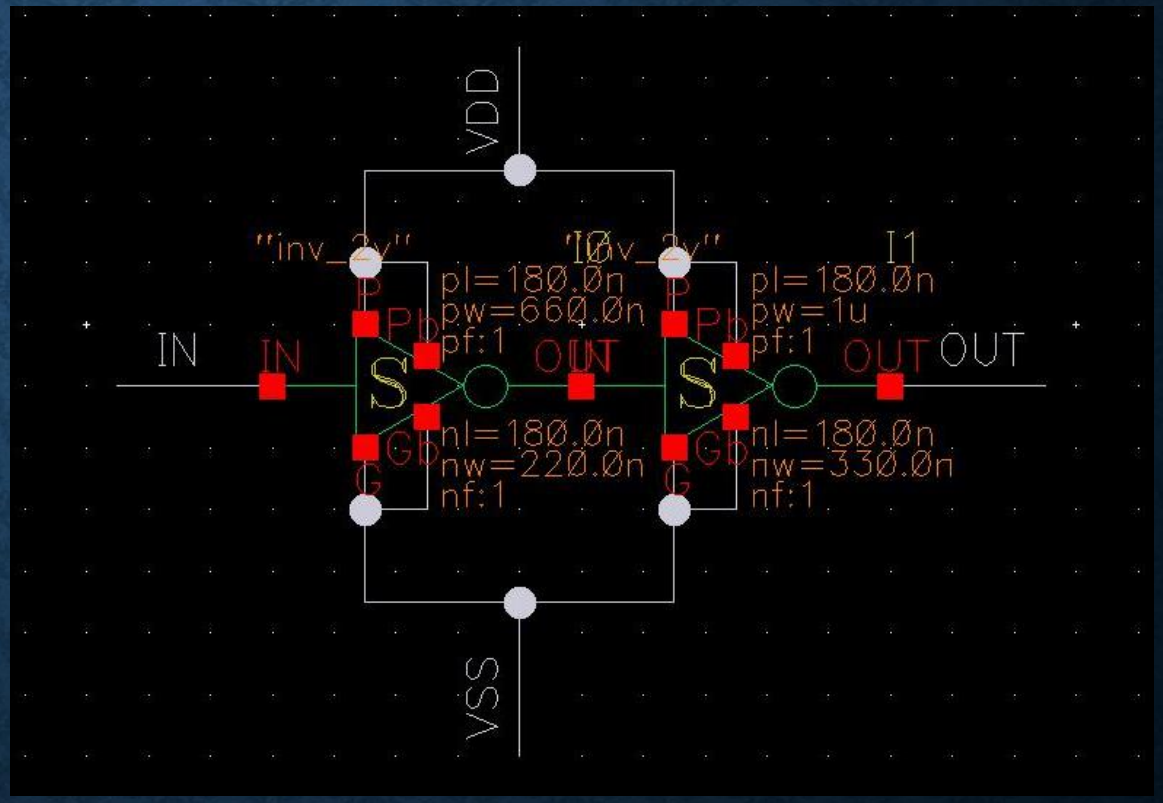
- 16 read muxes and 32 write muxes
- Transmission gates, upsize transistors for write column mux



Schematic of read column mux

MEMORY ARRAY – SENSE AMPLIFIER

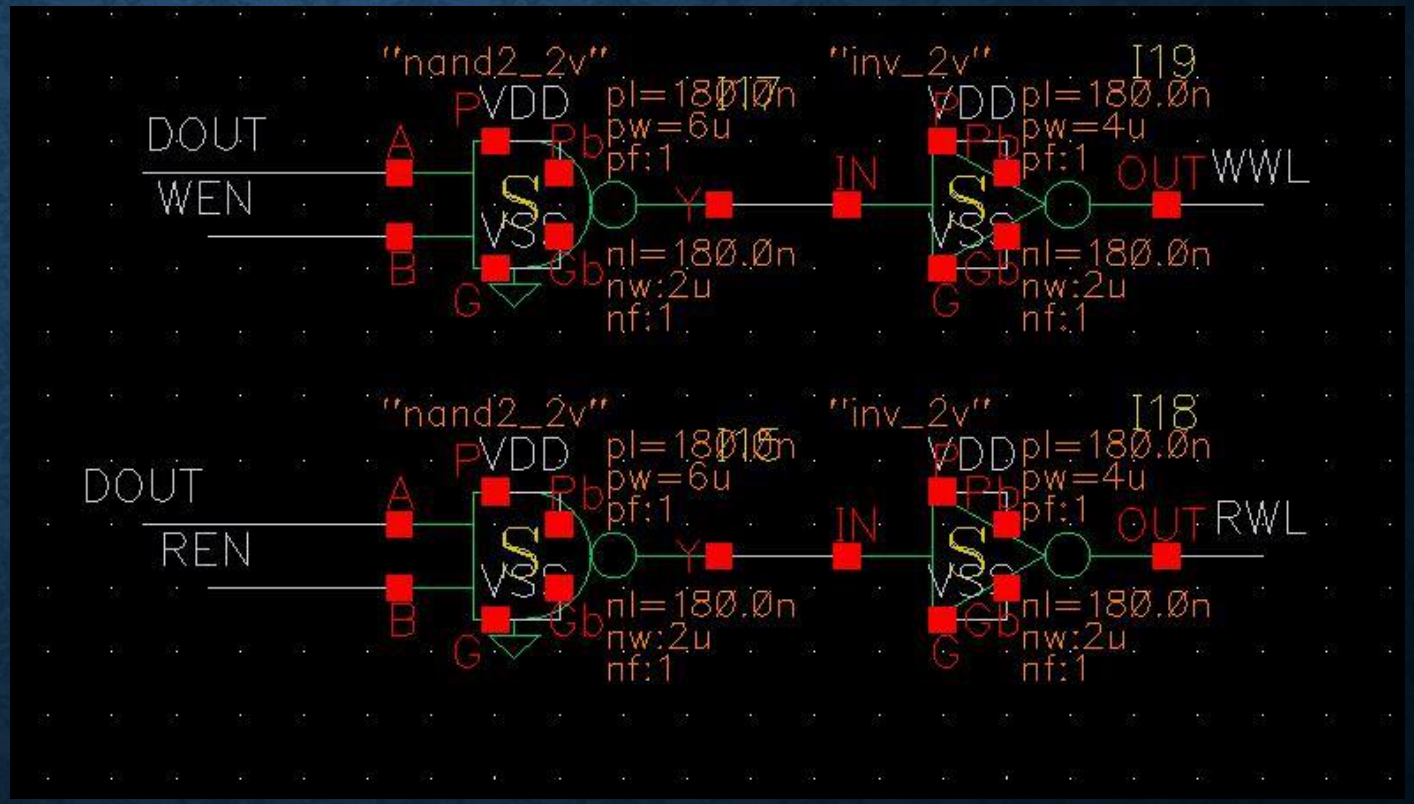
- 8T -> single ended
- Two inverters in series
- High skewed



Schematic of sense amplifier

MEMORY ARRAY – ROW DRIVER

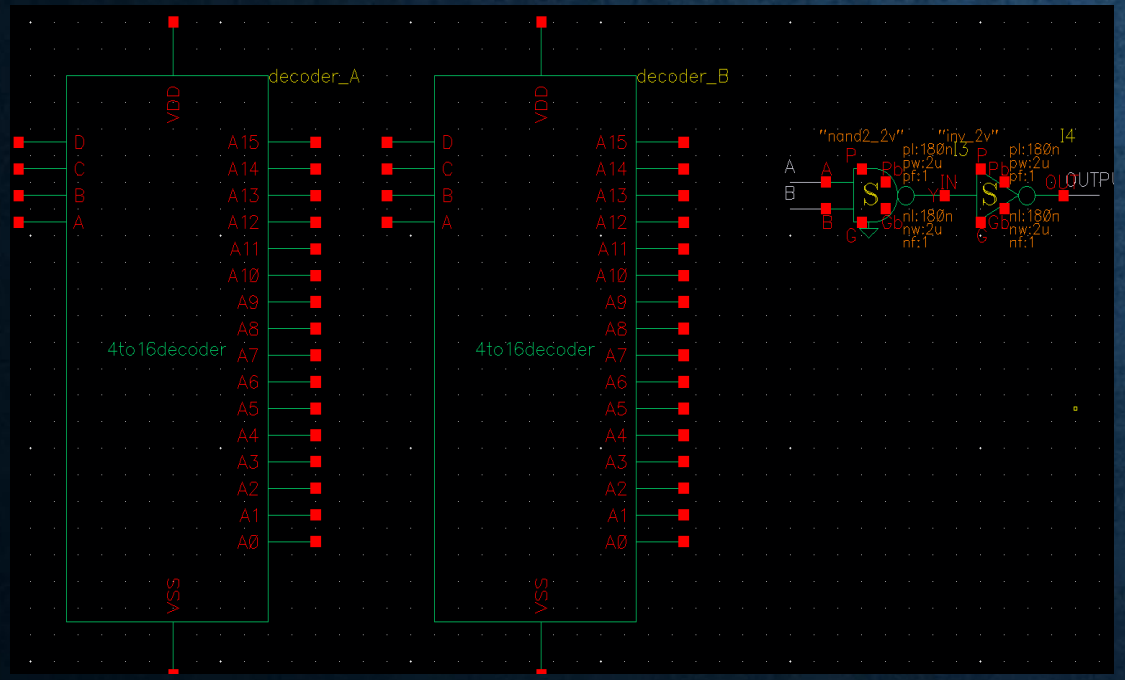
- Interface between row decoder and WWL or RWL
- Control and timing signals determine which to select
- Sizing according to logical effort



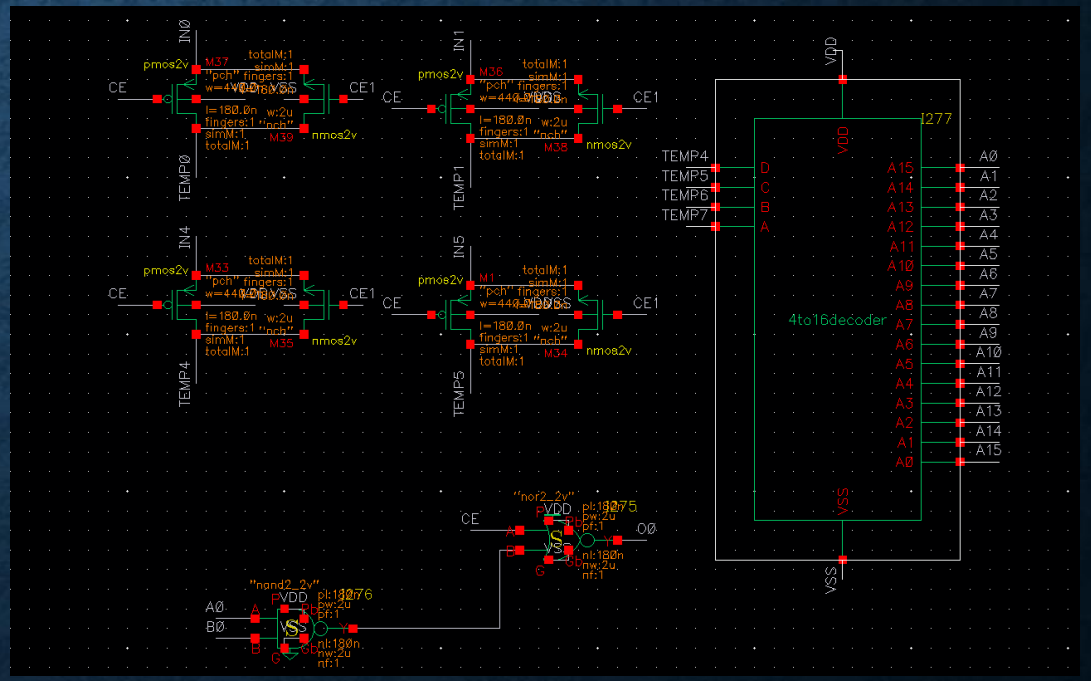
Schematic of row driver

DECODER

- Predecoding technique applied to decrease the logical effect
- Implemented transmission gates to connect chip enable signal and decoder



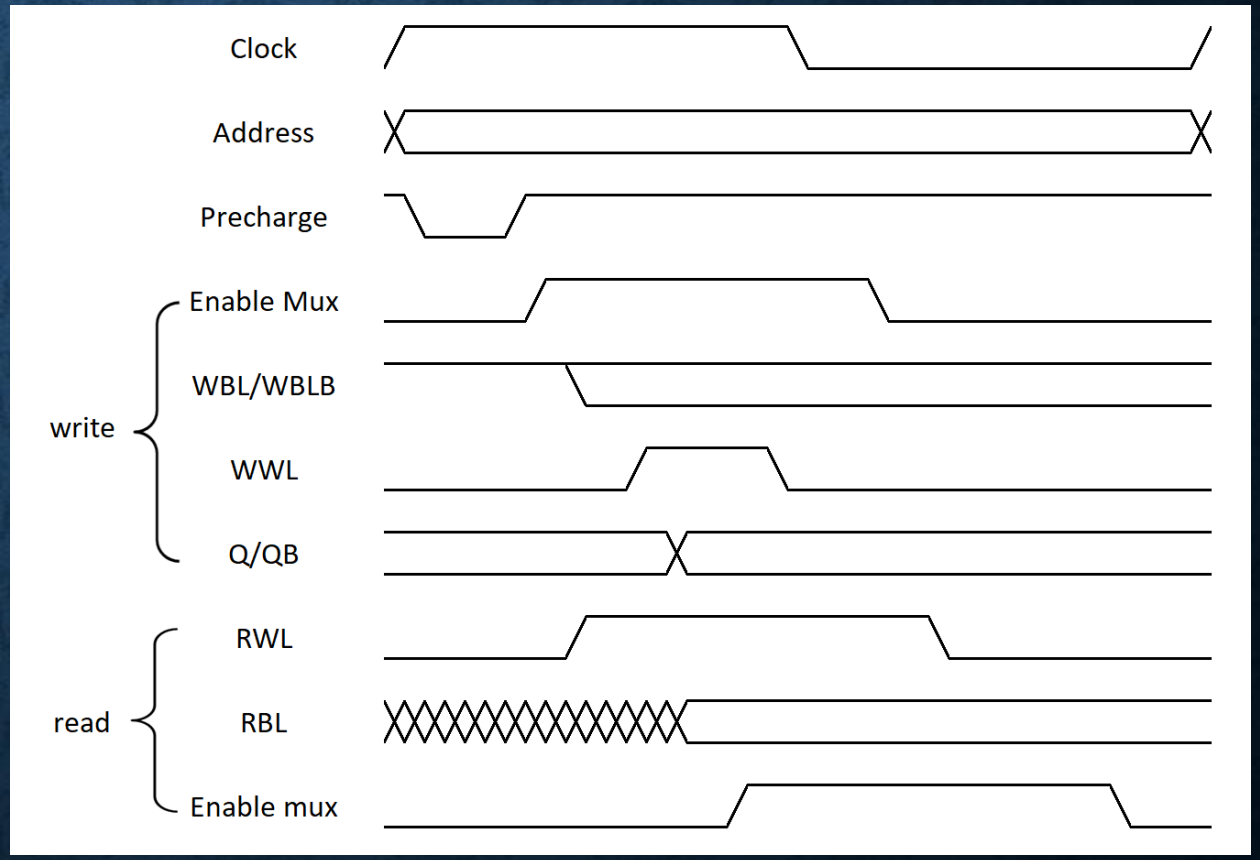
Schematic diagram of two stage decoder



Schematic diagram of chip enable signal and transmission gate

TIMING

- Timing diagram
- Timing circuit(inverter chain)
- Pulse register

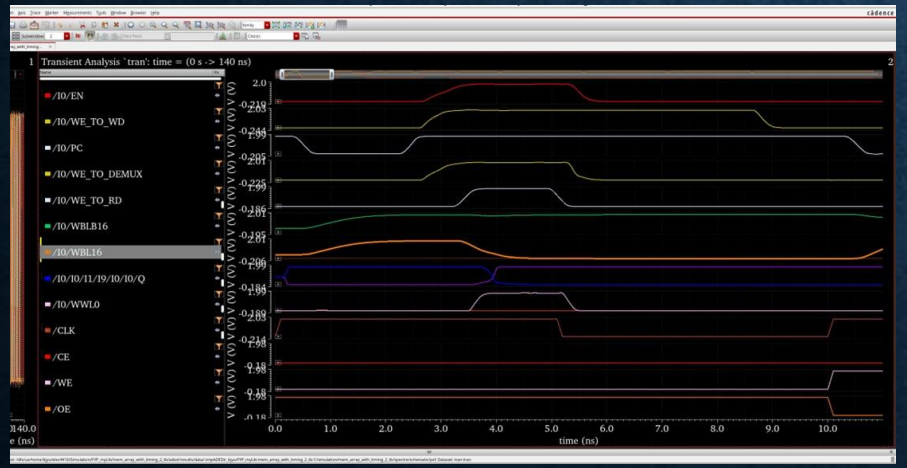


Timing diagram of read and write operation

VERIFICATION

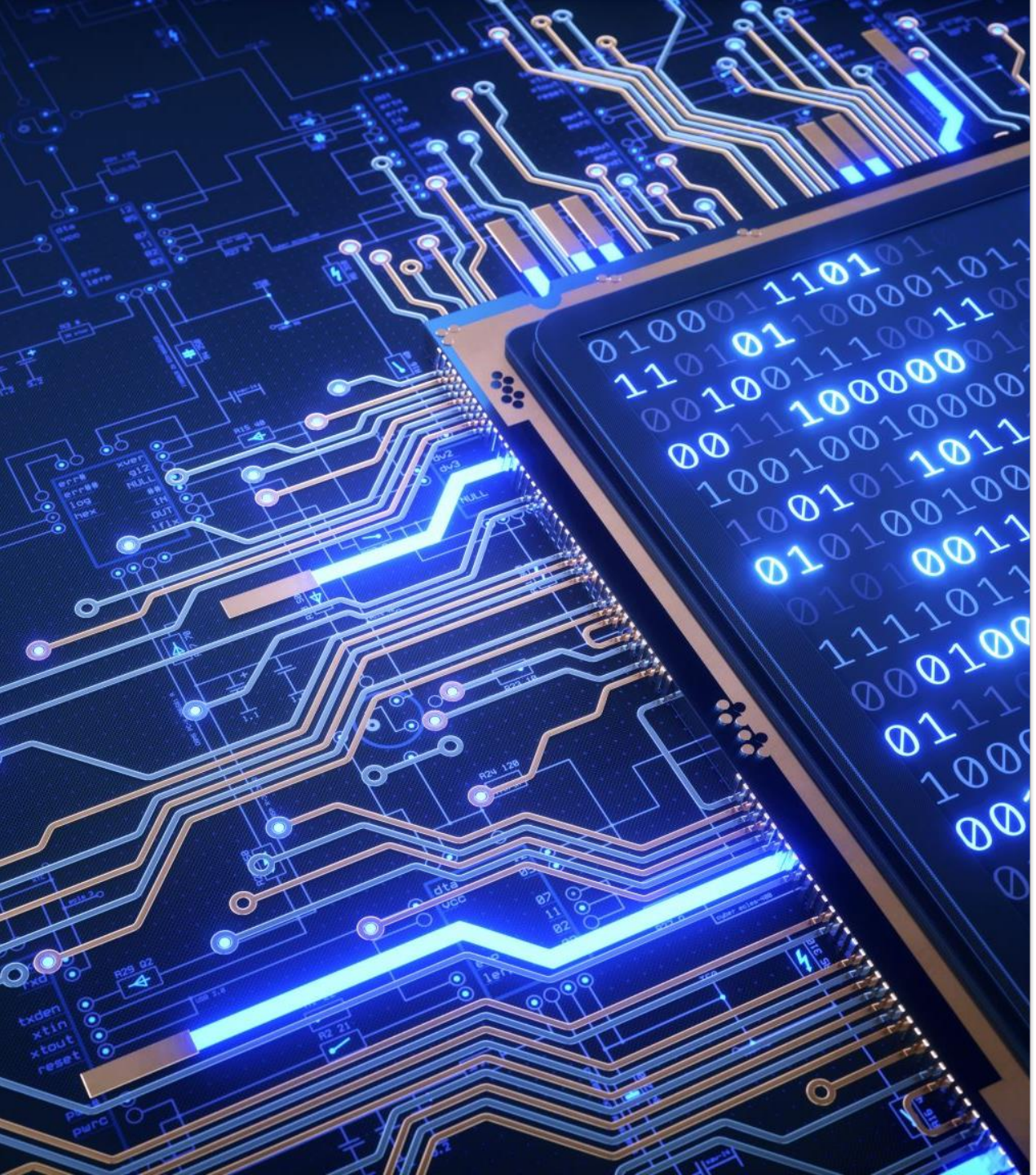
- Read follow by write simulation
- Random read and write simulation
- Worst-case and best-case clock cycle analysis

Table for Minimum Clock Cycle		
Ss, 125degrees, 1.71V	Tt, 27 degrees, 1.8V	Ff, -40 degrees, 1.89V
10ns	7ns	5.2ns



Write operation

Read operation



CHALLENGE

- Bit cell design
- Adding chip enable signal into row decoder
- Time management

RESULT

- In this project, a 256x256 8T SRAM has been designed, and the schematic as well as the simulation of the entire system have been completed successfully. The margin and operation of the design are functioning well. Furthermore, the layout for each component has been finished, and post-layout simulation and tests have been conducted to measure the worst-case and best-case delay. It is important to note that the simulation was performed without integrating the layout together.

THANK YOU FOR LISTENING