

SECTION 1 - INTRODUCTION

1.1 Background and Engineering Problem

Static random access memory (SRAM) is a very commonly used data storage for modern microprocessors, and is often utilized as cache memory for the CPU to have faster read or write access to or for other components' memory storage. Dynamic random access memory (DRAM) is also another kind of RAM and is often compared with SRAM. An SRAM cell may consist of four to ten transistors, and the bit is latched in between whereas a DRAM cell usually consists of a transistor and a capacitor. Although DRAMs are cheaper than SRAMs in general, SRAM is still more popular as it has several advantages such as less power consumption, the ability to operate at a higher speed, and can be fabricated with the same process with other elements as mentioned by [1]. Moreover, low-power chips are vital to ensure stability of miniature devices and technology scaling and to solve the problems that arise from the increasing demand of computation power for different applications.

There are two main reasons why low-power SRAMs are crucial nowadays. One of them is due to the lifetime of the batteries. As many devices have a small size but may require huge computation power, their batteries cannot be large, and low power consumption may be a key requirement of the product. On top of that, heat consumption is another reason why the development of low-power SRAMs is necessary. When more power is consumed, more heat is generated. This may lead to several problems such as run time failures or other reliability problems [2]. Although different packaging and cooling techniques can be applied, this may also increase the overall cost [2]. In summary, low-power SRAM is the trend as it's key to better performance, better reliability, lower power consumption, technology scaling, and cutting down the overall costs of the IC [2].

1.2 Objectives

The goal of this project is to design a low-power SRAM chip. This chip should be designed with eight-transistor bitcells using TSMC's 180nm technology. Moreover, power gating should be added to the logic to minimize power consumption.

1.2.1 Objective Statements

1. To implement essential components of an SRAM including but not limited to the bit array, decoder, sense amplifier, column multiplexer, timing circuits, precharge logic and the write drivers.
2. To realize ideas that express novelty on top of existing designs.
3. To design an SRAM that strikes a balance between area, cost, performance and power consumption.
4. To complete the layout and simulation of the SRAM.

1.3 Literature Review of Existing Solutions

A lot of studies are focused on more advanced processing nodes such as 65nm or 45 nm which is much smaller compared to the 180 nm technology. However, we may still reference them as they may also be suitable for our project.

6-transistor(6T) bit cell design

The 6T bit cell design is one of the most popular due to its robustness, low-power and low-voltage operation. The schematic is shown as below.

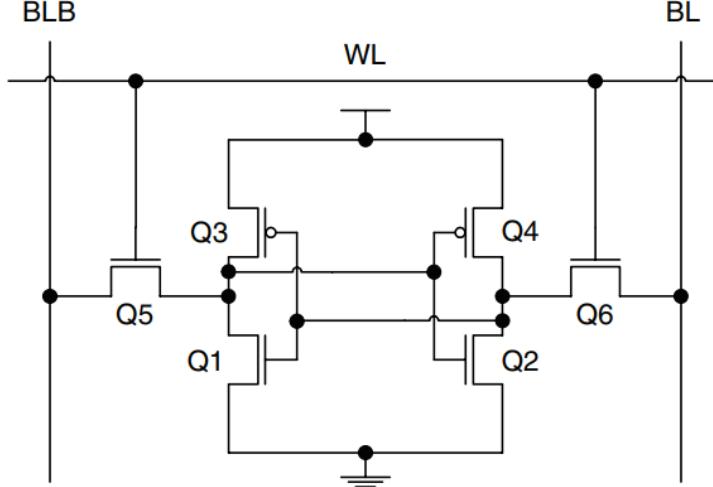


Figure 1. Six-transistor (6T) CMOS SRAM cell [3]

In the circuit diagram, WL stands for word line and is used for controlling Q5 and Q6 for read and write operations. When a read or write operation occurs, WL will be pulled high so that Q5 and Q6 can be turned on. The true (BL) and complementary bit (BLB) lines are for reading the data or writing new data into the bit cell. In a read operation, both BL and BLB are precharged. After WL is asserted, the differential voltage between BL and BLB will be sensed by the sense amplifier. Upon a read operation, one of the bit lines is driven from precharged value to ground. The data will be stored when WL is asserted [3].

Transistor sizing is critical in ensuring a reasonable read current as well as a non-destructive read. In addition, it should also ensure a successful write. There are conflicting requirements for read and write operations of the bit cell and the challenge increases with technology scaling [3].

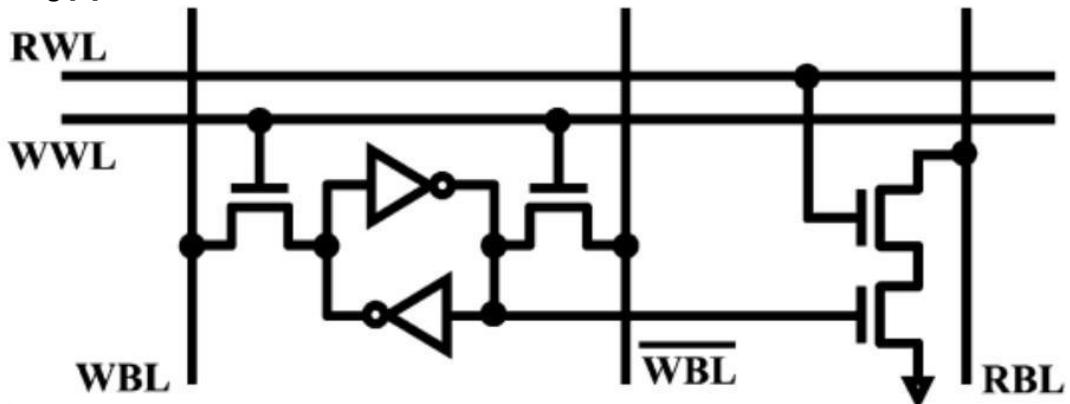


Figure 2. 8-transistor(8T) bit cell design [4]

One of the main differences between an 8T bit cell design is that the write bit lines and the read bit lines are separated. Compared to the 6T bit cell, the sizing requirements of the transistors do not face conflicting requirements. As mentioned by [4], as the read operation of 8T SRAMs do not affect the content of the cell, it provides a significantly improved static noise margin and will subsequently improve cell yield. Furthermore, as 8T has better robustness of read ability compared to 6T bit cells, it is more capable of the scaling trend of transistor sizes. In this case,

8T bit cells may be smaller than 6T bit cells even if they require more transistors.

In terms of power dissipation, different studies revealed different results. Some studies suggest that 8T SRAMs consume more power than 6T SRAMs [5, 6], while some point that it is on the contrary [7].

For this project, we will implement the 8T design due to its stability and its capability for more advanced processing nodes.

In terms of low-power SRAM design techniques, many methods found are related to multi-threshold SRAM cell and implementing power gating for the bitcell. For the control logic, there are different methods as well including power gating, half swing pulse mode technique, and hybrid type decoder technique.

Multi Threshold SRAM Cell

Many studies focused on cutting down on power consumption on the bit cell, and one of the methods is to adjust different threshold voltages for different transistors. This adjustment is typically achieved by modifying the base voltage of the transistors. In the context of the SRAM bit cell, certain transistors may necessitate a higher threshold voltage to mitigate leakage currents, while others may require a lower threshold voltage to enhance performance [8].

According to the design proposed in [9], after implementing multi-threshold techniques, the noise margins increased and the static power consumption decreased. However, it is worth noting that this design also leads to an increase in dynamic power dissipation, thereby limiting the effectiveness of the low-power feature. One advantage of this technique is that it does not impose any additional area overhead or require extra circuitry compared to alternative approaches [8]. Nevertheless, limited research has been conducted on the implementation of multi-threshold transistors specifically in 8-T SRAMs.

Power Gating

Power gating is a technique to reduce power consumption when the transistor is in the off state. Multi-threshold CMOS (MTCMOS) can be used to alter the threshold voltage (V_{th}) of different transistors. For low V_{th} transistors, although the switching speed is fast, the off current can be large, which may be capable of reducing delays, but not capable of reducing leakage currents. Hence, access transistors with high V_{th} are implemented on non-critical paths to reduce leakage current. The transistor then acts as a gate, so it's called power gating [10]. Power gating can be applied to many parts of the SRAM. For instance, gating can be applied to the bitcell or the sense amplifier as proposed in [11].

Half Swing Pulse Mode Technique

Another approach to cut back on power consumption is to reduce the swing of the signal that drives the decoder to half. According to [12], although reducing the voltage swing may lead to reduced gate overdrive and the need of level-conversion at the receiving gates, if there is a positive voltage swing (between V_{dd} to $V_{dd}/2$) and a negative voltage swing (between $V_{dd}/2$ and 0) combined with the logic style in the figure below, the receiving gates see a full gate overdrive and the negative of low swing inputs can be negligible.

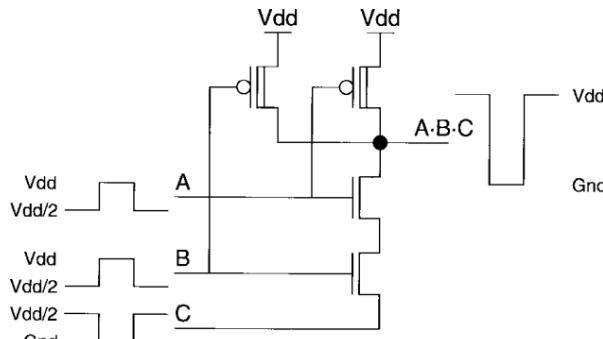


Figure 3. Half-swing pulse-mode AND gate [12] Hybrid Type Decoder Technique

One study proposed a method mainly focusing on fixing the decoder logic to reduce the number of transistors used, which is an effective way of cutting down on power consumption [13]. The proposed design consists of the buffer control circuit, pre-decoders, and the NAND-NOR stages-based gates. From the testing result, the proposed design consumes considerably less power compared to traditional static NAND or traditional static NAND-NOR decoder design [13].

SECTION 2—METHODOLOGY

2.1 Overview

2.1.1 Product/ System Description

In this project, a low-power 8T SRAM is built. It is a static random-access memory with an 8-transistor based cell structure. It is commonly used for on-chip cache memory in microprocessors and other integrated circuits. The 8T cell has better stability, higher SNM, and lower power consumption, but the increased area consumption, since there are more transistors, might limit the memory or increase the cost.

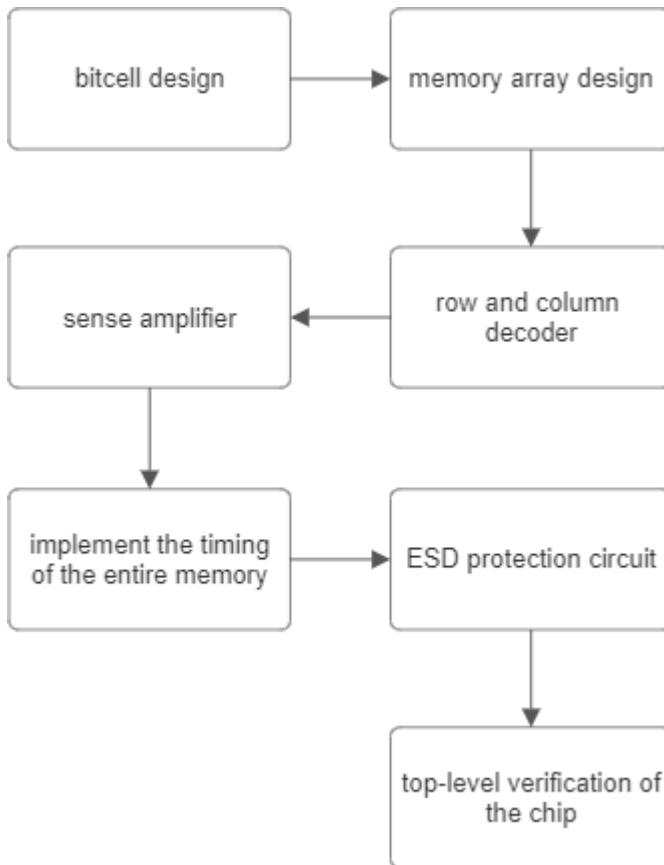


Figure 4. 8T SRAM workflow

In our project, we followed the conventional design and added some of our own ideas on top of that. For the bitcell, we have searched for papers related to stacking methods, but after discussion with the professor, we have decided to implement the conventional design as the stacking method may consume more power in many cases. Also, most transistors in the bitcell are implemented with the smallest size to reduce area except for the PMOS to maintain a better HSNM. Our pull-up ratio is 1.5 and cell ratio is 1.

For the precharge, write drivers, and column muxes, we have adopted conventional designs with well-crafted sizing of transistors to provide enough driving power to maintain an acceptable performance without consuming too much power and area. The sense amplifier consists of two high-skewed inverters connected in series.

The 8 to 256 row decoder consists of two main parts. The first part contains two 4 to 16 predecoders, and the second part consists of 256 2-input AND gates. This has several benefits on the performance such as eliminating the use of large fan-in AND gates, better pitch-fitting, reducing power consumption as well as better performance. The column decoder is simply a 4 to 16 decoder. Both decoders have an enable input and the output will all be zeros when the decoders are not enabled (ex: when the decoder is in hold mode).

The timing block is designed to implement self-timing of the SRAM. The input signals are the clock, output enable, write enable and chip enable signals. The

timing blocks are well-designed to trigger different operations in a sequence and with certain delays. This is done mainly by utilizing inverter chains, pulse registers as well as our designed logic to ensure a timing closure of the SRAM.

To make the layout smaller, we have tried to arrange the bitcell in pairs for better space utilization. As a result, the layout of the 256 times 256 memory array (excluding the peripheral circuits) consumes only 1.343 mm². Layout of other blocks are done in a way to fit the size of the memory array for better routing purposes.

2.1.2 System Block Diagram

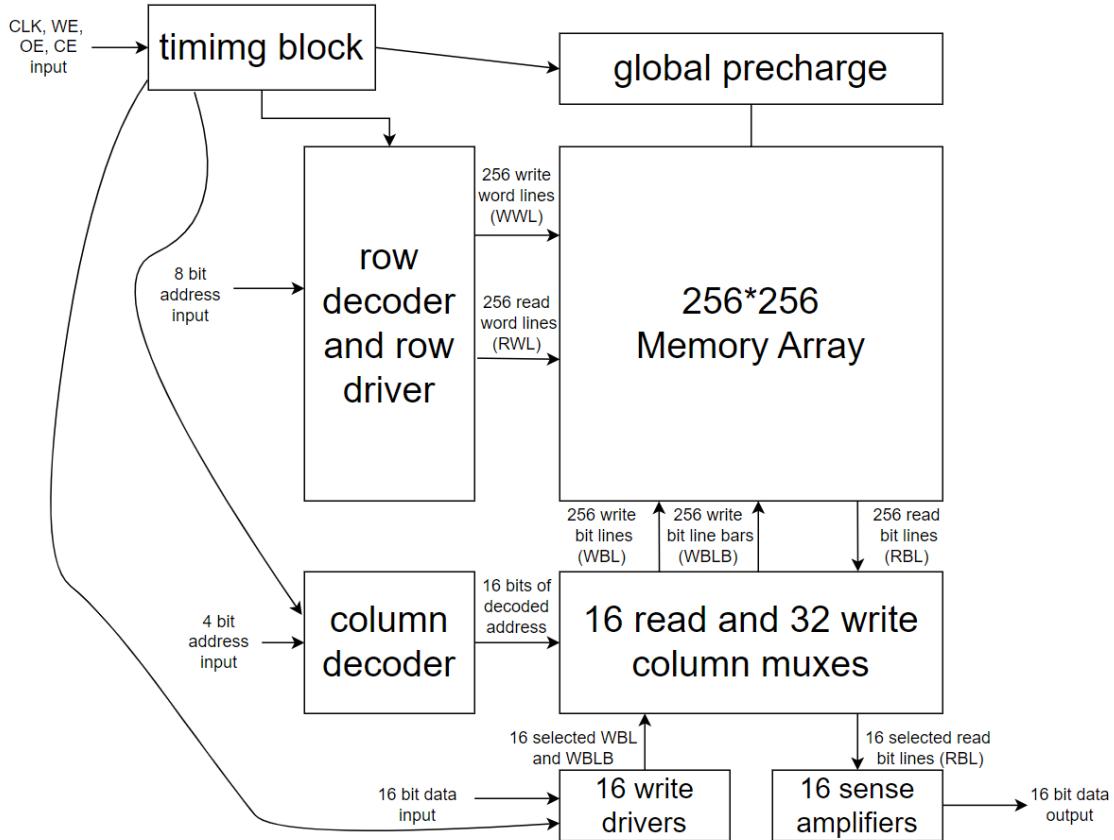


Figure 5. SRAM array and the associated peripheral circuits

Figure 5 shows the overview design of our project. The structure of the 8T SRAM can be logically divided into several parts: bit arrays, decoder, sense amplifier, and input. To further elaborate on the design idea, the bit array can be further categorized into bit cells, bit lines, and write lines. We utilize bit lines and write lines to facilitate read and write operations, while the bit cells store the actual data. The decoder plays a crucial role in the system as it helps us identify the memory address we want to access. By decoding the address inputs, the decoder selects the appropriate memory location for read or write operations. The sense amplifier is responsible for amplifying voltage changes. It assists us in observing even slight voltage differences. Overall, this design allows for efficient data storage and retrieval in the 8T SRAM structure, with distinct components serving specific functions to ensure reliable operation.

2.1.3 component list

Item	Specifications/Model
Development Software	Cadence, Synopsys Matlab, Verilog-A
Operating System	Windows 10

2.1.4 ECE Knowledge

ELEC 2400 - Electronic Circuits

This course introduced fundamental electronic circuits, and how we analyze the voltage and current through each part. Basic components like diodes, op-amp, MOS transistors as well as related circuits are introduced. In our project, we need to utilize these fundamental knowledge to design our circuit and see if we can reduce our circuit's power consumption.

ELEC 3310 - Digital Fundamentals and System Design

In this course we have learned about the mechanisms of decoders and multiplexers, how they are built and how they work. The course also introduces how we can combine basic logic components to enhance performance. On top of that, we have learned how to write rtl code in VHDL, for example 4 bit Adder Subtractor with 7-Segment LED display, 4-bit binary up counter, which is very similar to verilog.

ELEC 3400 - Introduction to Integrated Circuits and Systems

This course presents an overview, applications, fundamentals and design flow of the state-of-the-art integrated circuits (IC) and systems. Course contents include diodes, bipolar transistors and MOS transistors and modes of operations. We have a basic concept on how to design a chip, what we should be aware of, and where we can make it better.

ELEC 4410 - CMOS VLSI Design

This course introduces the process, logic characterization, performance estimation and design rules for CMOS circuits. On top of that, we will learn VLSI design and some verification tools. This course is mainly about how we design a chip, which is quite related to our project.

ELEC 4420 - Analogue Integrated Circuits Design and Analysis

This course talks about multiple-stage operational amplifiers, frequency response,

feedback analysis, stability and compensation, Slew rate, advanced amplifier design techniques, analog VLSI building blocks. As the SRAM consists of analog components, we believe this course can equip us with some knowledge that we may encounter during the design process.

2.2 Objective Statement Execution

In this subsection, detailed procedures will be introduced in view of meeting set objectives on target and on time. Note that the objective statements in 1.2 will be discussed together with the full optimization of the 8T SRAM

- 1. To implement essential components of an SRAM including but not limited to the bit array, decoder, sense amplifier, column multiplexer, timing circuits, pre-charge logic and the write drivers.**

Bitcell:

The schematic of the conventional 8T SRAM is shown below, and this is the design we implemented in our SRAM. The pull-up ratio is $(W/L)_5 / (W/L)_2$ or $(W/L)_4 / (W/L)_3$ and is 1.5. The cell ratio is $(W/L)_1 / (W/L)_2$ or $(W/L)_0 / (W/L)_3$ and is 1. All the labels are according to the figure below. Also, we have done DC simulations of hold static noise margin and dynamic noise margin, and the simulation results can be found in Appendix G

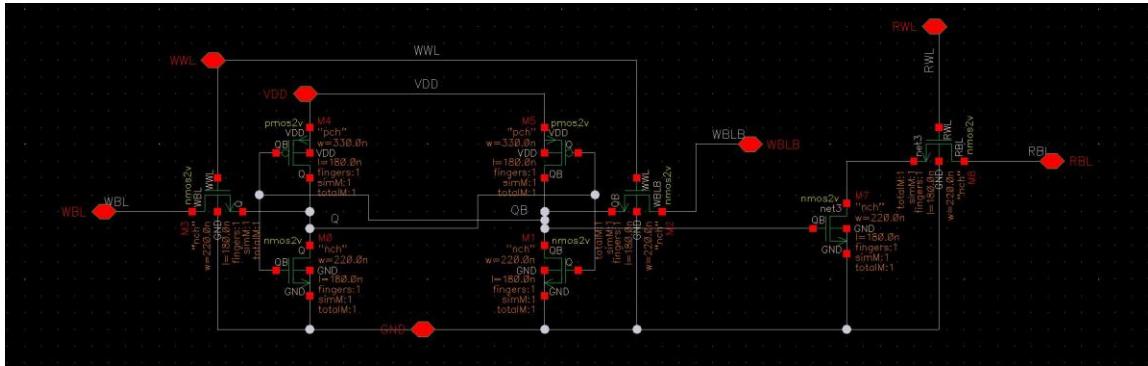


Figure 6. The schematic of our bitcell design.

Precharge:

The precharge design we proposed is from the conventional designs of 8T SRAMs. This is due to the separation of read and write bit lines, and its robustness. In our design, the read (RBL) and write bit lines (WBL, WBLB) are precharged at the same time. The pmos between WBL and WBLB is used for equalizing them to compensate for process variations.

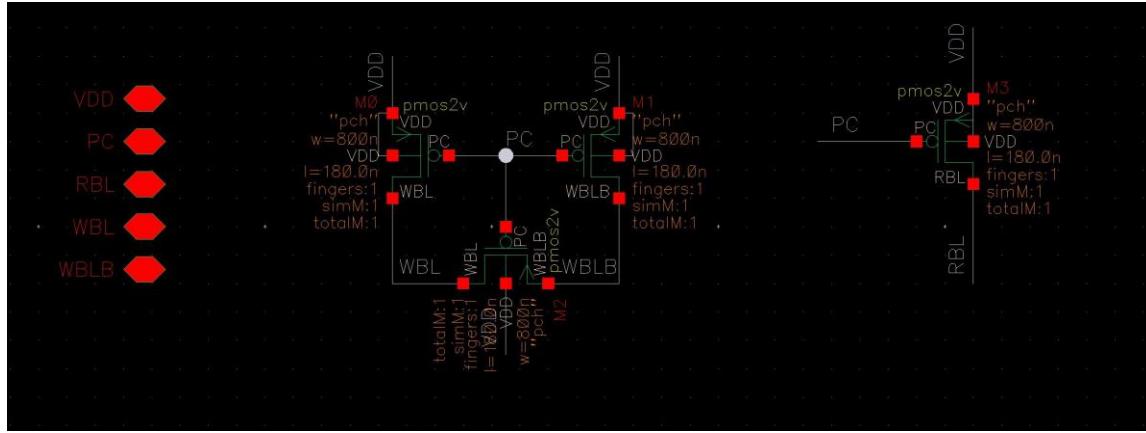


Figure 7. The schematic of our precharge design.

Write Driver:

The write driver consists of two transmission gates and three inverters to write to the bit cell in the SRAM. The schematic is shown below. The size of the transistors is larger for a better driving strength.

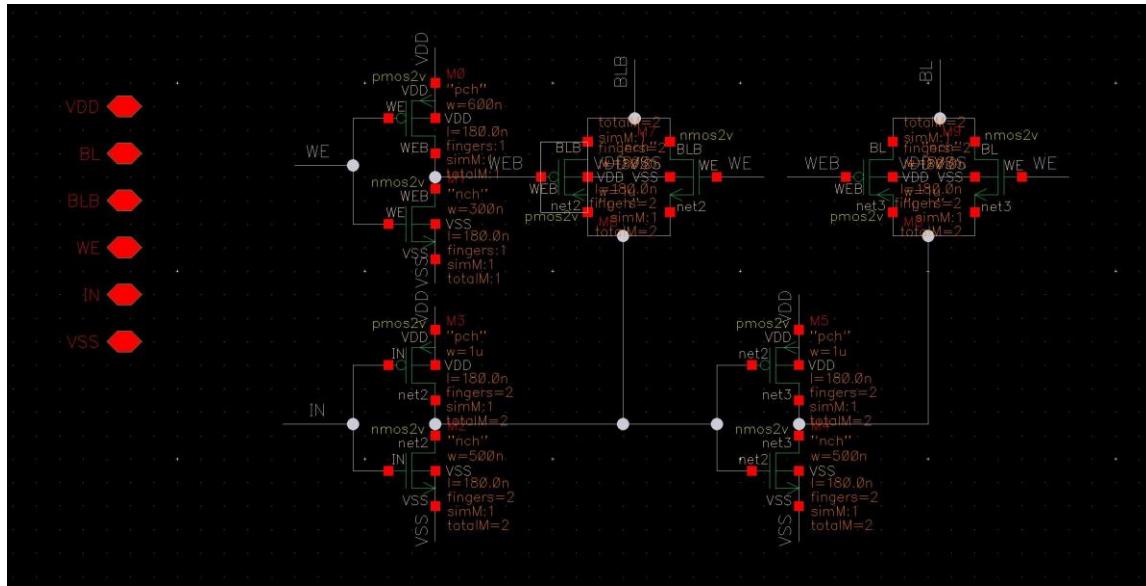


Figure 8. Schematic of write driver.

Row Decoder

For the decoder, since we are going to create a 256x256 SRAM array, the decoder design involves creating two 4-to-16 predecoders that will be combined using a NAND gate to form both the row and column decoders. Inverters may be used to ensure equivalence of rise and fall time and delay in the worst case [14]. Similarly, the column decoder is responsible for selecting the bit line. It is similar to the row decoder but typically utilizes multiplexers connected to the bit line for read or write circuitry. The decoder design of the SRAM has been completed at the schematic level, and simulations have been conducted to verify the correct decoding of all inputs.

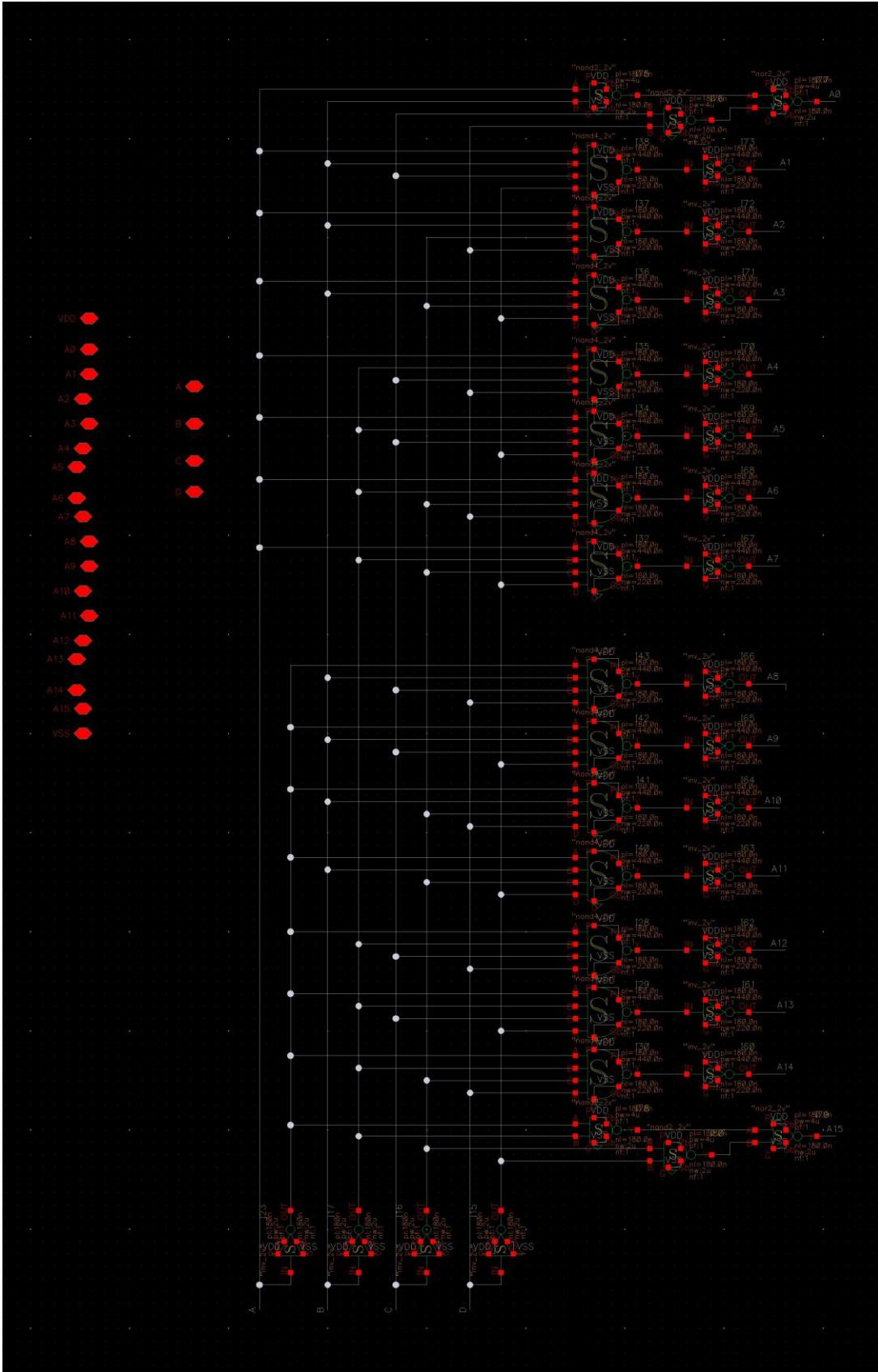


Figure 9. Schematic of Row Predecoder: The NAND gates are at the right of the picture and the top most and bottom most NAND gates are implemented differently to provide a different write strength. The 4 inverters at the bottom are used for generating the negate input signals.

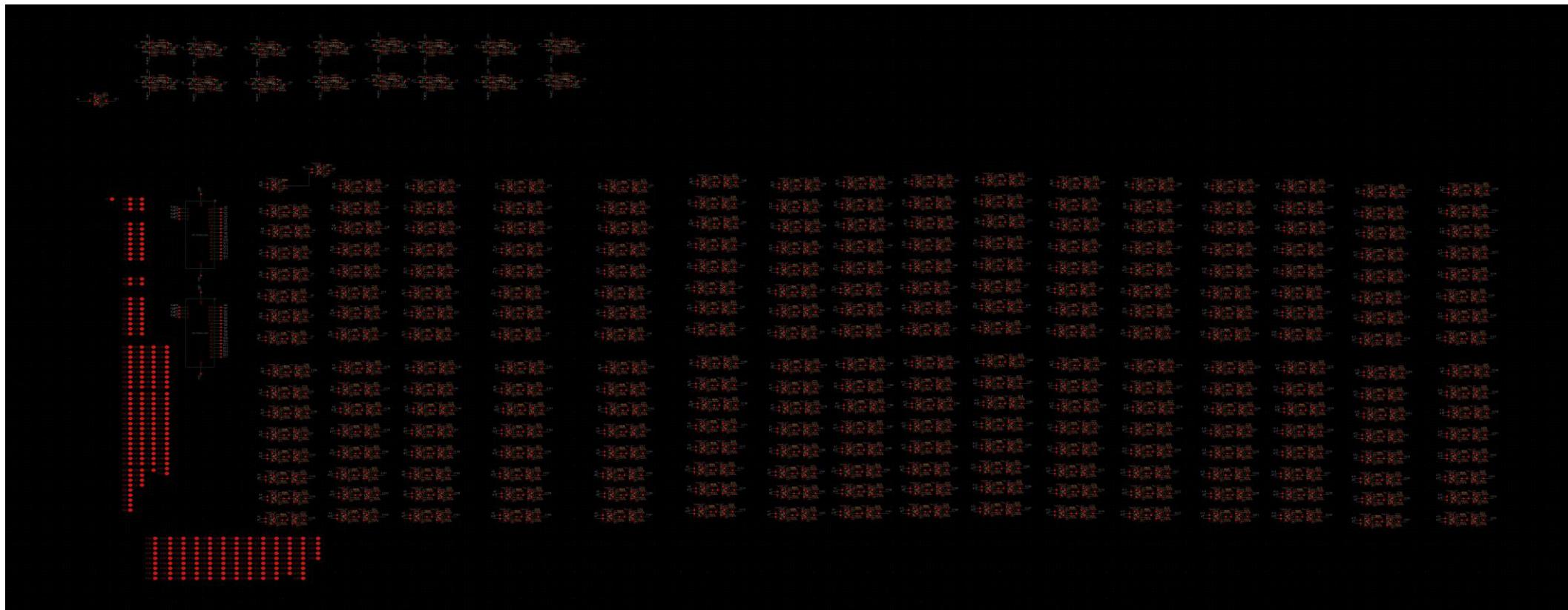


Figure 10: Schematic of the whole row decoder: The middle left part of the picture are the two predecoders and the schematic is shown in figure 9. The top part of the picture are transmission gates for enable signal of the decoder. This is to reduce power and avoid any word lines being asserted when the SRAM is in idle state. The rest of the picture are two input AND gates and is the final stage of the 8 to 256 decoder. The inputs are from all combinations of the outputs from two predecoders.

Row Driver

The row driver serves as an interface between the row decoder and the word lines. The row driver provides enough driving strength so as to minimize the time required to charge the word lines. Whether to assert the write word line or read word line depends on the two input ports – WEN and REN. The SRAM will perform a read or write when REN or WEN is high respectively. When none of them are high, the SRAM is in idle state.

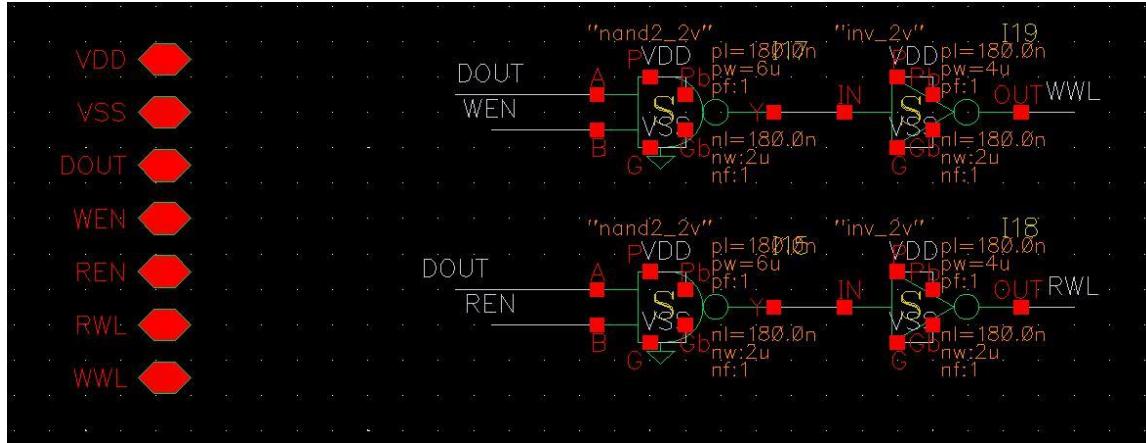


Figure 11. Schematic of Row Driver

Column Mux

The column mux is vital for the SRAM to select which word to read or write in the memory array. In our design, each word consists of 16 bits and each row consists of 16 words. Therefore, 16 muxes for read and 32 muxes for write are required in our design. The mux for write contains larger transistors to increase the speed of writing to the array. The select signals of the muxes are generated from the column decoder of the SRAM.

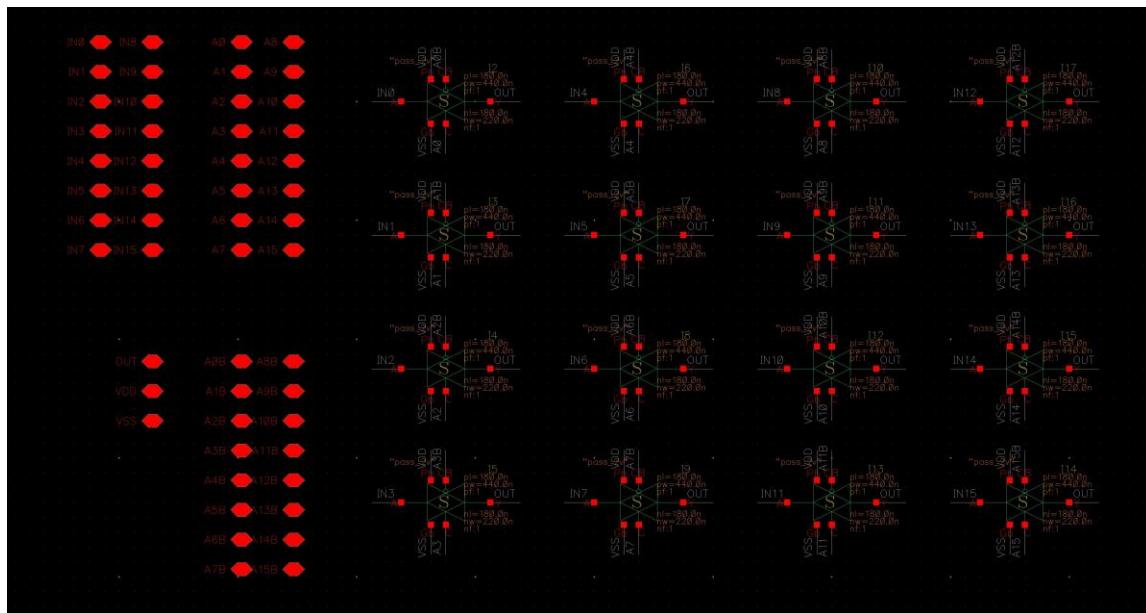


Figure 12. Schematic of Read Column Mux

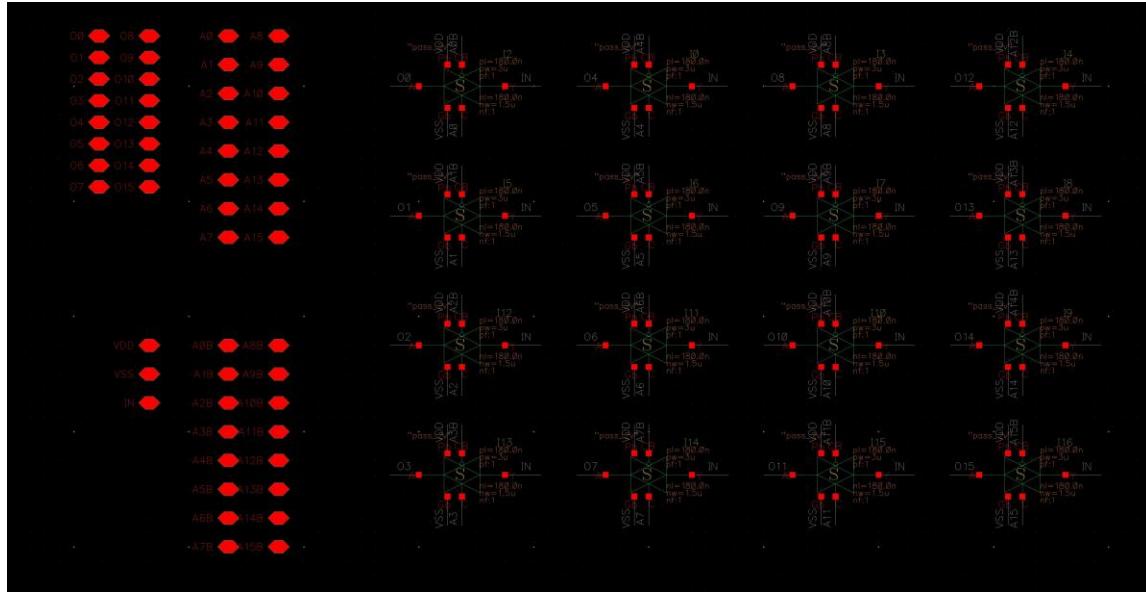


Figure 13. Schematic of Write Column Mux

Sense Amplifier

In a read process, the bitcell will discharge RBL if a 0 is stored in the bitcell. However, this process may be time-consuming due to the size of the transistor. Hence, the sense amplifier accelerates the reading process. Our sense amplifier consists of two high-skewed inverters connected in series with a much larger transistor size compared to that in the bitcell.

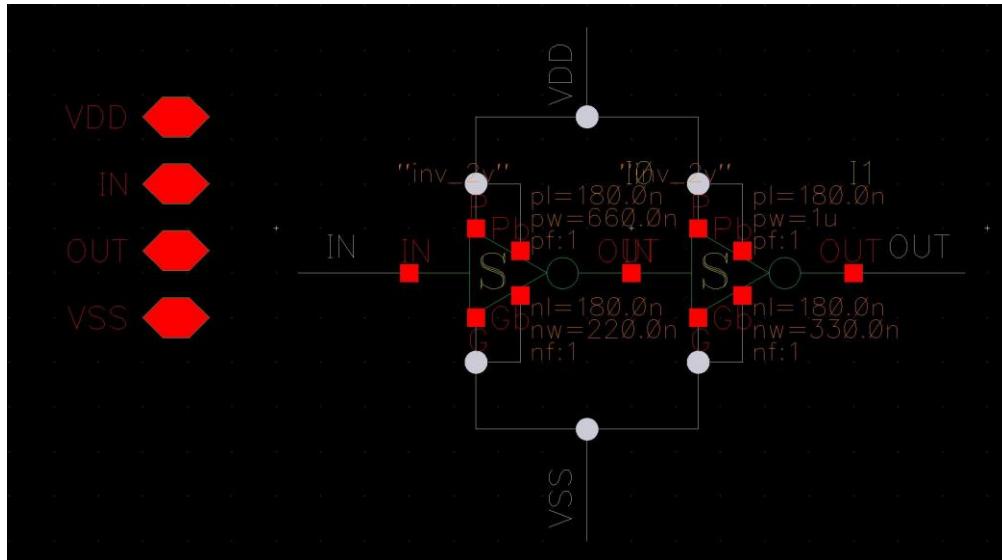


Figure 14. Schematic of Sense Amplifier

Timing Circuits

The timing block is used for controlling the sequence of events in the SRAM. During the writing process, the SRAM starts to precharge right after the rising edge of the clock. After the precharge operation, the write drivers will be activated, followed by the write column mux and then the write word line will be asserted after a certain delay. After a successful write, the write word line, write column mux and the write drivers will be deactivated one

after another. For the read process after the precharge process, the read column mux will be enabled, then followed by the read word line. Next, the read word line will be turned off followed by the read column mux. There is no sense amplifier enable signal as our sense amplifier only consists of inverters.

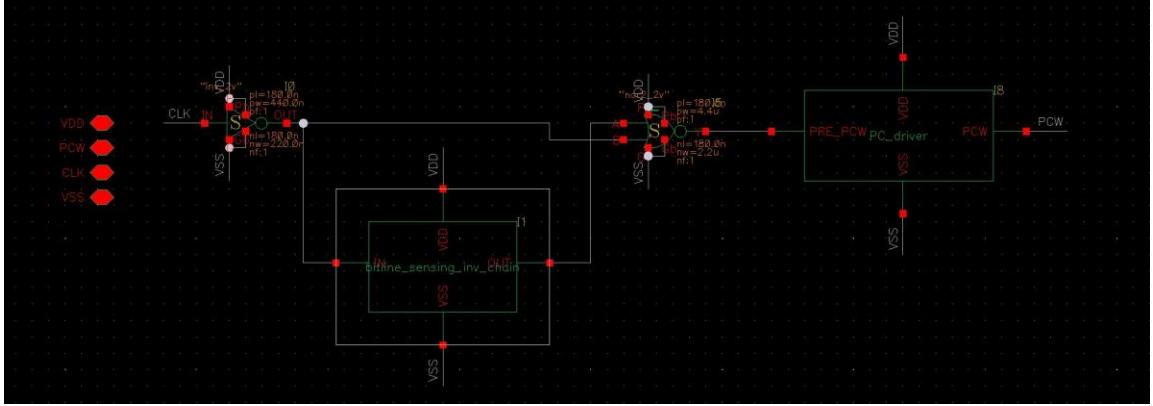


Figure 15. Schematic of Timing Block from Clock to Precharge: The inv_chain below is a chain of inverters and governs the duration of precharge process. The PC_driver consists of an inverter to drive the large capacitive load for global precharge.

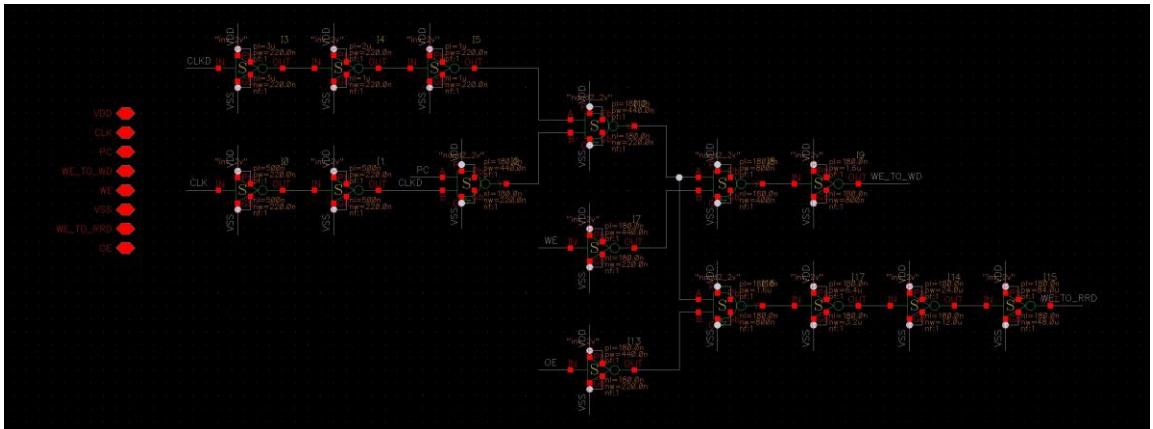


Figure 16. Schematic of Timing Block From Completion of Precharge to Write Enable or Read Drivers For Read: This block decides whether it should proceed to a write process or a read process. Also, some delay elements are added in between.

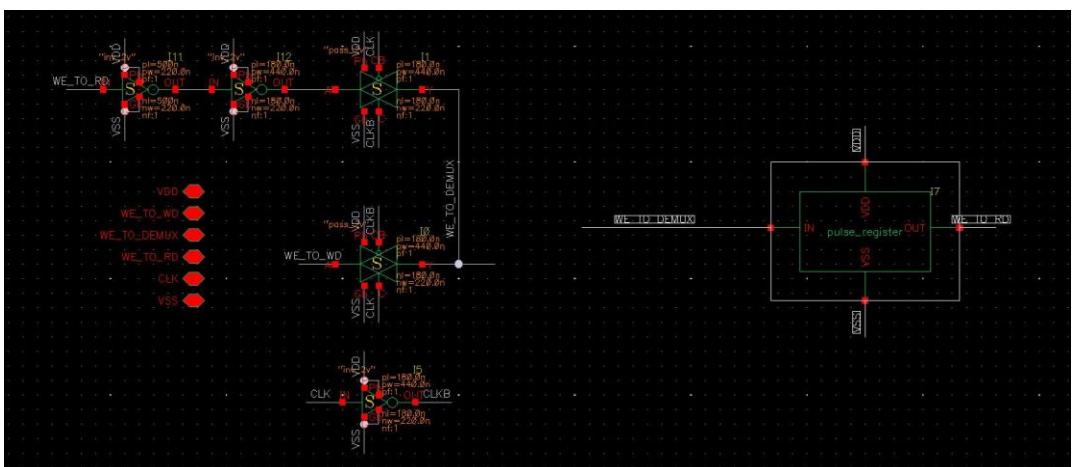


Figure 17. Schematic of Timing Block From Activation of Write Driver to Write Column Mux and Then to the Row Driver: The pulse register gives a pulse that is long enough to assert the word line and write the corresponding data to the memory.

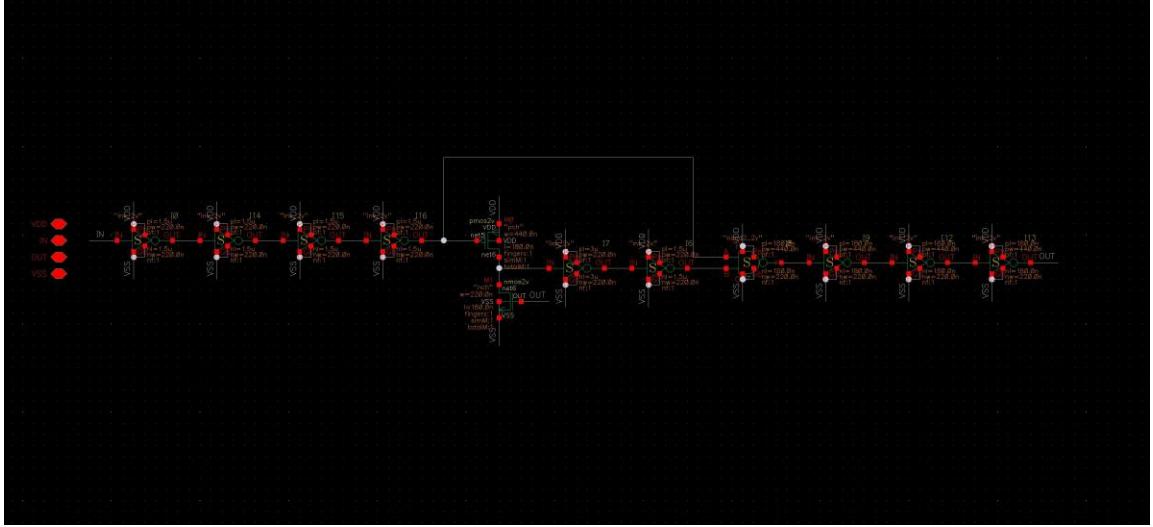


Figure 18. Schematic of Timing block from Activation of Read Row Driver to Read Column Mux: This part will activate the read column mux when needed and deactivate it after some time.

2. To realize ideas that express novelty on top of existing designs.

We have come up with some ideas during our design process. In the decoder design, usually all the output of the decoder must go through an AND gate with all the other signals. This may increase a lot of area and power consumption as shown below.

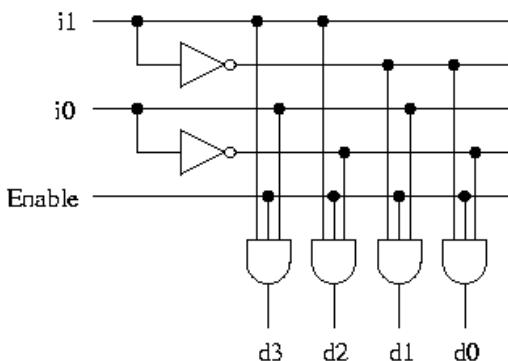


Figure 19. Schematic of Decoder With Enable Signal [15]

If we implemented this in our 8 to 256 row decoder, the area will increase sharply and may even cause problems in the layout stage. To solve this problem, the enable signal controls 8 transmission gates with address inputs as the transmission gate input. If the decoder is not enabled, another transmission gate that connects to VSS will be on. The output of the decoder for all 0 address input will be go through some logic with the enable signal to tackle the corner case.

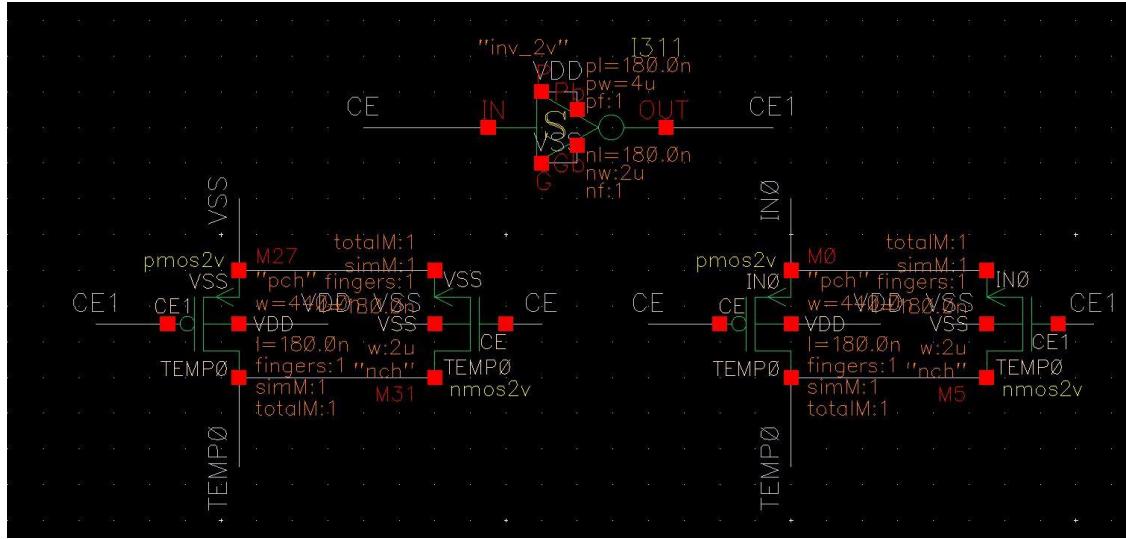


Figure 20. Schematic of Solution to Enable Signal: In the schematic CE is the chip enable signal and will enable the decoder when it is low. In this case the transmission gate at the right will be on and IN0 will go to one of the inputs of the predecoder. If CE is high, VSS will be connected to the input of the decoder. All inputs (IN0 to IN7 in our design) are connected like this to TEMPO0 to TEMP07 respectively.

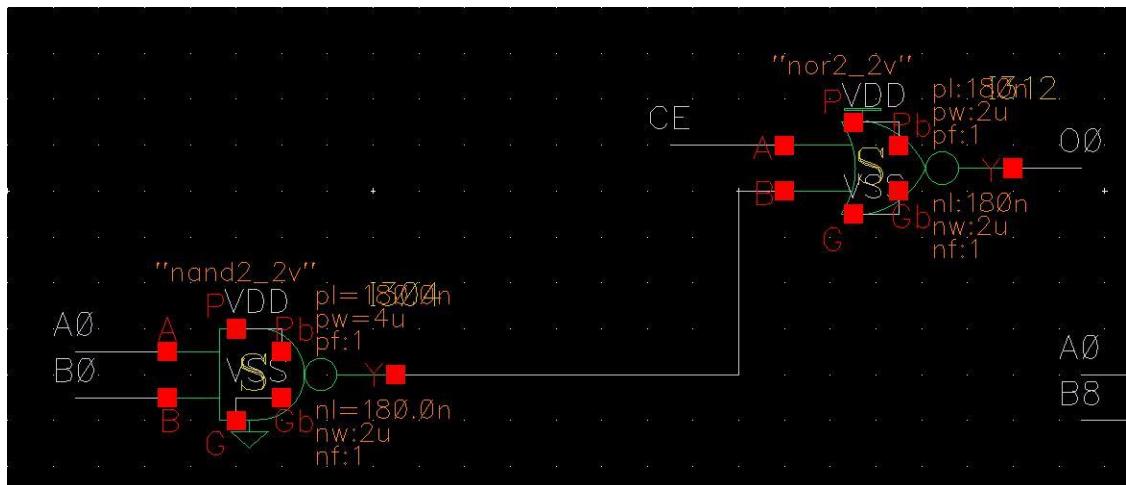


Figure 21. Schematic of Solution to Corner Case for Enable Signal: When the output of the predecoder are all 0s, there are two possibilities. One is that CE is high, the other is that CE is low but all inputs (IN0 to IN7) are low. The circuit shown in the picture is to differentiate these two cases. When both CE and all inputs are low, Output 0(denoted as O0 in the schematic) will be high. If CE is high, then O0 is guaranteed to be low.

Another special design from our project is the layout of the bitcell. As mentioned before, our layout of the bitcell is formed in pairs, and this can enhance space utilization which is shown in the picture below.

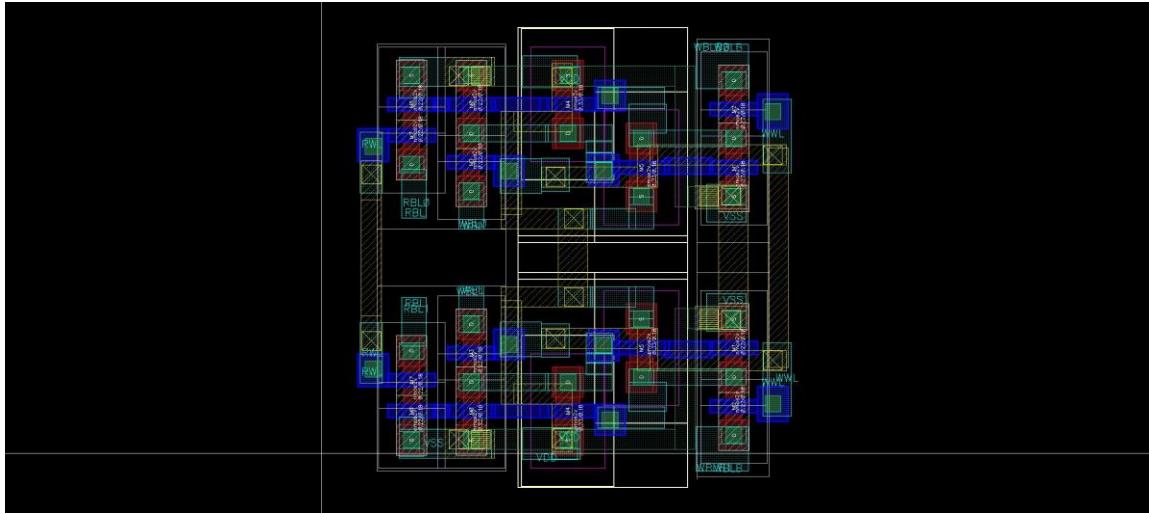


Figure 22. layout of two bitcells

Another part of the design that demonstrated more originality is the timing block of the SRAM. As shown in the first objective statement execution, all the timing blocks are tailored made for our SRAM design.

However, we must admit that most of our SRAM design adopted conventional designs due to their robustness. We have read other papers about different designs as well, but we did not adopt these designs because of their drawbacks.

3. To design an SRAM that strikes a balance between area, cost, performance and power consumption.

During the design process, we have used different methods to improve area consumption, performance or power consumption. For example, in the bit cell design, most transistors use the smallest sizing. However, the two PMOS are sized larger to increase hold static noise margin. If we continue to increase Q3 and Q4, the write stability will decrease drastically, so this is why we set the pull-up ratio to be 1.5.

In the decoder design, it has been observed that incorporating a pre-decoder can improve decoding speed. This is particularly beneficial when dealing with large memory storage, where the presence of numerous bit cells in the array can lead to longer decoding times. Decoding all inputs directly in a single AND gate can result in a high fan-in and significant logical effects, which can adversely impact performance. By introducing a pre-decoder, the decoding process is divided into two stages. This approach helps to reduce power consumption by minimizing the number of active output lines and also improves access time, leading to a faster operation.

4. To complete the layout and simulation of the SRAM.

We have completed the whole schematic of the SRAM from the bitcell to timing implementation and tested the functionality of it at the schematic level. As for the layout, we have completed most of the essential components but couldn't finish the whole layout due to time limit. The pre-post-layout simulations as well as the post-layout simulations of certain blocks can be found in appendix G.

2.3 Main Objective Evaluation and Discussion

Our main objective of the project is to design a low-power SRAM chip and complete the layout as well as top-level verification. Also, we had to implement power gating to reduce power consumption.

In terms of our progress, we have completed the schematic and our SRAM works at the schematic level. However, we didn't implement power gating cells to further reduce power consumption. As for the layout, we completed most of the parts but failed to finish the whole SRAM in time and perform post-layout simulations.

Next, the quality of our work is also an important part of evaluation. During the design process, we have tried our best to apply what we have learned and what we have read to our design. However, SRAM circuits are much more complicated than the results we have learned from textbooks and there are too many factors that has to be considered when tuning our design. We have adopted some good design methods, such as calculating the capacitance and applying some formulas for transistor sizing rather than pure trial and error, but more should be done to accomplish a well-crafted design.

In terms of the novelty of our design, we have made some changes in the decoder, layout as well as the timing block implementation. However, most of the designs we followed are conventional designs. If we had to do better, we should do more literature reviews for us to generate more ideas and spend more time discussing them with our supervisor. In a nutshell, we believe that more can be done and especially to come up with low-power solutions or some special features.

When compared to the literature review, our design didn't really have a better performance compared to their design. We believe that one of the reasons may be due to some mistakes we made during the design process.

Overall, our project partly achieves the objectives we set at the beginning. We have finished the SRAM schematic level and completed most of the layout. We also had some of our own ideas in our SRAM design and also tried to build an SRAM with lower power consumption, less area consumption and better performance. However, we could have achieved more by working more on power gating or other low power designs.

SECTION 3 - CONCLUSION

The aim of our project is to design a low-power SRAM chip with power gating. We partly completed the project, and there is room of improvement for us.

During the design phase, we used Cadence for everything, but it would be better if we could make use of other tools as well such as Synopsys and Verilog-A as they can speed up the design process. Also, as mentioned earlier, we should do more research and spend time to organize the knowledge we obtained. The testing phase should also be automated. The only way we test our design is to look at the waveform and input the waveform by ourselves. If this can be done automatically, we could have our circuit tested much thoroughly and may spot some corner cases before it's too late.

Some of the features that are missing on our chip are low-power designs and ESD protection circuits. It turns out that we should manage our time better so as to achieve more in this project. To improve this, we should set a better goal and work together more efficiently at the early stage of the project. For example, if we can distribute the workload effectively at the beginning, maybe someone can already get some insight into ESD protection while another teammate is working on decoder design.

Moreover, we should try to improve the layout of the project. Although we did fine for the layout of the bitcells and memory array, there is always some space wasted after layout. This may result in large area consumption as well as parasitic capacitances. Another skill we can learn is to apply place and route with other software, which may save us lots of time on the project.

References

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APPENDICES

Appendix A: Final Schedule

Objective Statements	Task	Member in charge	Wk 1	Wk 2	Wk 3	Wk 4	Wk 5	Wk 6	Wk 7	Wk 8	Wk 9	Wk10	Wk 11	Wk12	Wk 13	Wk 14	Wk 15	Wk 16	Wk 17
Research and Planning		All																	
	SRAM Bit Cell Design	ALL																	
	Design Memory Array	YU Kuang Jung																	
	Design the Decoder	HSU Yung-hsiang																	
	Design Sense Amplifier	Ng Cheuk Hei																	

Objective Statements	Task	Member in charge	Wk 18	Wk 19	Wk 20	Wk 21	Wk 22	Wk 23	Wk 24	Wk 25	Wk 26	Wk 27	Wk 28	Wk 29	Wk 30	Wk 31	Wk 32	Wk 33	Wk 34
Research and Planning		All																	
	Design Memory Array	YU Kuang Jung																	
	Design the Decoder	HSU Yung-hsiang																	
	Design Sense Amplifier	Ng Cheuk Hei																	
	Implement the timing	YU Kuang Jung																	
	ESD protection circuits	HSU Yung-hsiang																	
	verification of the chip	ALL																	

Appendix B: Budget

Expected budget

Items	Cost
MATLAB	\$0
Synopsys	\$0
Verilog-A	\$0
Cadence	\$0
TSMC's 180nm technology	\$0
TOTAL	\$0

Since the above software is provided free by HKUST.

Appendices

Appendix C – Meeting Minutes

1st Meeting

Date: 7/09/2022

Time: 11:30am

Location: HKUST, Room 2423

Attendees: Yung-Hsiang HSU, Kuang Jung YU, Cheuk Hei NG, Professor Sarfraz Khawar

Absent : None

Minutes taken by: Cheuk Hei NG

- Main objective is confirmed.
 - Some of the technical requirements are set.
 - Methodology of the project is discussed.
- Action Items for Next Meeting

Action Item to be completed	By when	By whom
Draft of Proposal Report <ul style="list-style-type: none">- Introduction- Methodology- Project Plan	11th September	Yung Hsiang HSU, Kuang Jung YU, Cheuk Hei NG

Next Meeting: 12th September / 15:00 / HKUST Library (LG4)

2nd Meeting

Date: 12/09/2022

Time: 3pm

Location: HKUST, Library (LG4)

Attendees: Yung-Hsiang HSU, Kuang Jung YU, Cheuk Hei NG

Absent : None

Minutes taken by: Cheuk Hei NG

Table 1. Action Items from Previous Meeting

Action Item to be completed	By when	By whom	Status
Draft of Proposal Report - Introduction - Methodology - Project Plan	12 th September.	Yung-Hsiang HSU, Kuang Jung YU, Cheuk Hei NG	Completed

Table 2. Action Items for Next Meeting

Action Item to be completed	By when	By whom
Finalize the Proposal Report	13th September	Yung-Hsiang HSU, Kuang Jung YU, Cheuk Hei NG

Next Meeting: To be scheduled with professor

3rd Meeting

Date: 15/02/2024

Time: 2pm

Location: Room 2423

Attendees: Yung-Hsiang HSU, Kuang Jung YU, Professor Sarfraz Khawar

Absent : Cheuk Hei NG

Minutes taken by: Kuang Jung YU

Table 1. Action Items from Previous Meeting

Action Item to be completed	By when	By whom	Status

Precharge circuit, Write driver, Decoder	15/02/2024	Yung-Hsiang HSU, Kuang Jung YU	Patially Completed
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Table 2. Action Items for Next Meeting

Action Item to be completed	By when	By whom
Ensure that our memory array can perform a successful read and write operation	01/03/2024	Yung-Hsiang HSU, Kuang Jung Yu

Next Meeting: To be scheduled with professor

4th Meeting

Date: 15/02/2024

Time: 2pm

Location: Room 2423

Attendees: Yung-Hsiang HSU, Kuang Jung YU, Professor Sarfraz Khawar

Absent : Cheuk Hei NG

Minutes taken by: Kuang Jung YU

Table 1. Action Items from Previous Meeting

Action Item to be completed	By when	By whom	Status
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Read and write operation	04/03/2024	Yung-Hsiang HSU, Kuang Jung YU	Completed
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Table 2. Action Items for Next Meeting

Action Item to be completed	By when	By whom
Come up with ideas about SRAM timing	11/03/2024	Yung-Hsiang HSU, Kuang Jung Yu

Next Meeting: To be scheduled with professor

Appendix D — Group Members' Contributions

Kuang Jung YU: During my summer vacation, I dedicated time to reading various background materials for our project, including the course materials of ELEC4410. Later on, I delved into books and journals to gather more information specifically about SRAM bit cells. Then I participated in designing and testing of the bit cell. Subsequently, I focused on studying materials related to the precharge and write driver aspects. In the case of the precharge circuit, I decided to deviate from the conventional three-transistor configuration for global precharge in 6T SRAMs. Instead, I opted for utilizing only an equalizer to address the two bit lines during the write process. This modification aimed to reduce power consumption and area requirements. In terms of documentation, I specifically worked on developing the introductory section of the proposal report. Additionally, for the progress report, I took responsibility for executing part of the objective statement. Moreover, I dedicated time to conducting a literature review on existing solutions for low-power designs, which could potentially be beneficial for our future design endeavors. As an example, one of the papers I read explored the concept of reducing voltage swing by a factor of two, while simultaneously incorporating another swing reduction by two that is connected to VSS. This approach aimed to conserve power while maintaining an acceptable level of performance. After that I worked extensively on the timing implementation of the SRAM. I designed mainly on the write timing. This includes how to trigger the precharge, how to enable the write drivers, column mux as well as asserting the word line. After that, I spent some time on the layout of the sram. I am in charge of the read and write column mux, the sense amplifier and the write driver as well as the precharge layout. However, I didn't manage to finish all of the layout.

Yung-Hsiang HSU: During my summer vacation, I dedicated time to reading various background materials for our project, including the course materials of ELEC4410. Later on, I delved into books and journals to gather more information specifically about SRAM bit cells. Since we are focus on reducing power consumption of the sram, we are trying to see if there is any technique that we might be able to implement in the bit cell design. I have found that stacking two transistor can increase the performance of the bit cell, so I plan to place a transistor under the nmos of the inverter of the bit cell, but this will increase the leakage current, and also since we designing 8t sram we are removing one of the transistor for the read operation, and this will decrease the stability too, so after discussion, we give up this design. After that, I have found a paper mentioning that we can put a pmos in the middle of two inverters. When we are doing read or write operation, the pmos of that bit cell will be on while other bit cell will be off. This will cut off the feedback loop between two inverters and improve the performance. But after discussing with the professor, this design might be good when we are only looking at the bit cell, but when we are doing the rest of the parts, there might be some problems. Therefore, we decided to use conventional design. Also, I have helped Kuang Jung YU to finish the simulation of the bit cell. After that, I am working on the decoder part. Since we need to store at least one kb of memory in our sram, I plan to do a 8 to 256 decoder for both row decoder and column decoder. This the memory is large, we can't just done everything in one and gate, that will cause huge logical effect, and reduce the performance of it. So after doing some research, I make it into two stages, I decode 8 input signal with two 4 to 16 decoder then use and gate to get the final address. With this we can lower the power consumption and also the access time. For the proposal report, I took responsibility for methodology part. I also do literature review on existing ways to lower the power consumption or increase the performance. For example, I have read that one paper mention that the power consumption isn't the same when doing read and write operation, so the paper suggest that we can increase the probability of writing data in '0' or '1', thus lower the power consumption. After the decoder I have search for sense amplifier, since it is a simple skewed inverter, I only search for the better ratio of it. After that, I have improved the design of the row driver. After that we are doing timing diagram I have design the timing circuit and test for the delay time of the read operation. While doing timing I also redesign the row decoder to deal with the chip enable signal. After that, I also have search for the ESD protection circuit and finish the schematic and simulation of it, which is later cancel. For the layout part, I have finish the single bit cell design and combine it into a 256x256 array, also I have finish the layout of row driver and make it suit the size of the bit cell. After that I have finish the layout of the 4 to 16 decoder and also the row decoder which combine of two stages.

Cheuk Hei NG: Doing the project planning part for the proposal report. Doing research on sense amplifier.

Appendix E – Deviation(s) from the proposal and supporting reason(s)

For the bit cell we will not use techniques like stacking and so on to reduce the power consumption because after discussing with the professor, there is something that we didn't consider about and might have a worse output than the conventional one.

Appendix F – Monthly Report

Monthly Report for ECE FYP/FYT

Project Code:	SK02d-23	Supervisor(s) :	Khawar SARFRAZ
Project Title:	Low-Power SRAM Chip Design		
Group Member(s):	1) YU, Kuang Jung	2) HSU, Yung-hsiang	3) NG, Cheuk Hei
Reporting Period:	Report #1 Report #2 Report #3	<input checked="" type="checkbox"/> Oct (Fall) <input type="checkbox"/> Nov (Fall) <input type="checkbox"/> Feb (Spring)	(please attach Reports #1-2 to the Progress Report to be submitted in Jan) (please attach Reports #3 to the Final Report to be submitted in Apr)
Progress Report:	<ul style="list-style-type: none"> • List the work completed in this reporting period. • Identify the major difficulties encountered. • Comment on the overall progress. <p>During this phase, we dedicated our efforts to comprehending the fundamental workings of the 8T SRAM bit cell. Following that, we focused on conducting simulations of various aspects related to the bit cell, including hold static noise margin, write static noise margin, and dynamic write margin. Moreover, we have tested different sizing of the transistors to improve the noise margins of the bit cell.</p> <p>Throughout this process, we encountered several challenges. Understanding the operational mechanisms of the 8T SRAM and grasping the concept of noise margins posed initial difficulties. Additionally, we faced some problems when using Cadence to do simulations as all of use are quite new to the software. However, we believe these problems will occur less often as we are getting more familiar with it.</p> <p>Admittedly, the overall progress has not met our expectations thus far. Nonetheless, we remain optimistic that we are heading in the right direction. After this report, we plan to set small goals for every week to keep up with the schedule.</p>		
Future Plan:	<ul style="list-style-type: none"> • Write down the working plan for the next reporting period. <p>Before the next progress report, we plan to finalize and finish the bit cell design and simulations including Monte Carlo simulations to take different process corners into account. Afterwards, we will work on the design of the bit array, this includes the pre-charge transistors, the body contact, column MUX, and write drivers.</p>		
Group Representative's Signature:			

Monthly Report for ECE FYP/FYT

Project Code:	SK02d-23	Supervisor(s) :	Khawar SARFRAZ
Project Title:	Low-Power SRAM Chip Design		
Group Member(s):	1) YU, Kuang Jung 2) HSU, Yung-hsiang 3) NG, Cheuk Hei		
Reporting Period:	Report #1 <input type="checkbox"/> Oct (Fall) Report #2 <input checked="" type="checkbox"/> Nov (Fall) Report #3 <input type="checkbox"/> Feb (Spring) (please attach Reports #1-2 to the Progress Report to be submitted in Jan) (please attach Reports #3 to the Final Report to be submitted in Apr)		
Progress Report:	<ul style="list-style-type: none"> • List the work completed in this reporting period. • Identify the major difficulties encountered. • Comment on the overall progress. <p>During this phase, we dedicated our efforts to reading some materials about different components of the SRAM such as the write driver, precharge circuits, sense amplifiers and the decoder structure. Also, we have done more testing on the bit cell such as the dynamic write margin and testing under different process corners and temperatures.</p> <p>Admittedly, the overall progress has not met our expectations thus far. Nonetheless, we remain optimistic that we are heading in the right direction. After this report, we plan to set small goals for every week to keep up with the schedule.</p>		
Future Plan:	<ul style="list-style-type: none"> • Write down the working plan for the next reporting period. <p>Before the next progress report, we will try to work out the schematic of write drivers, precharge circuits, sense amplifier and the row and column decoders. We will first work on the schematics and will do the layout later.</p>		
Group Representative's Signature:			

Monthly Report for ECE FYP/FYT

Project Code:	SK02d-23	Supervisor(s)	Khawar SARFRAZ
Project Title:	Low-Power SRAM Chip Design		
Group Member(s):	1) YU, Kuang Jung 2) HSU, Yung-hsiang		
Reporting Period:	Report #1 <input type="checkbox"/> Oct (Fall) Report #2 <input type="checkbox"/> Nov (Fall) Report #3 <input checked="" type="checkbox"/> Feb (Spring) (please attach Reports #1-2 to the Progress Report to be submitted in Jan) (please attach Reports #3 to the Final Report to be submitted in Apr)		
Progress Report:	<ul style="list-style-type: none"> • List the work completed in this reporting period. • Identify the major difficulties encountered. • Comment on the overall progress. <p>During this phase, we are working on the schematic of different components of the SRAM such as the write driver, precharge circuits, sense amplifiers and the decoder structure. Also, we have done the simulation of each part individually, and we are now reading material of timing to combine different part together. Also we are doing research on the esd protection circuit and I/O pad.</p> <p>Admittedly, the overall progress has not met our expectations thus far. Nonetheless, we remain optimistic that we are heading in the right direction. After this report, we plan to set small goals for every week to keep up with the schedule.</p>		
Future Plan:	<ul style="list-style-type: none"> • Write down the working plan for the next reporting period. <p>Before final report, we will try to work out the schematic of whole sram, do the timing diagram and make sure it works properly. After finish schematic, we will work on the layout of the sram.</p>		
Group Representative's Signature:			

Appendix G Figures

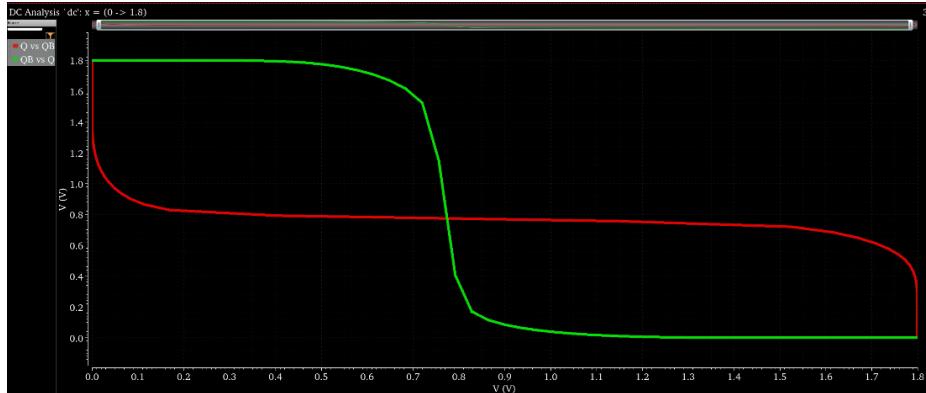


Figure 23. DC simulation of hold static noise margin of SRAM bit cell

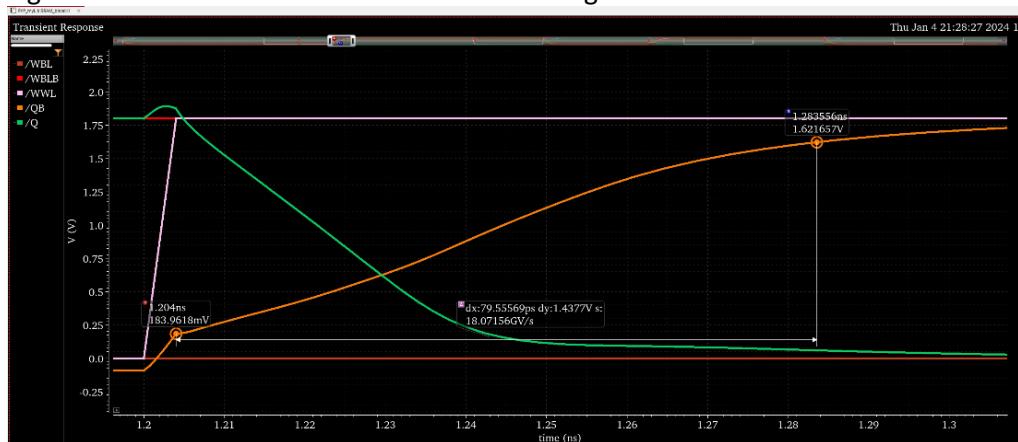


Figure 24. transient analysis of dynamic write margin of SRAM bit cell, the dynamic write margin is 80ps

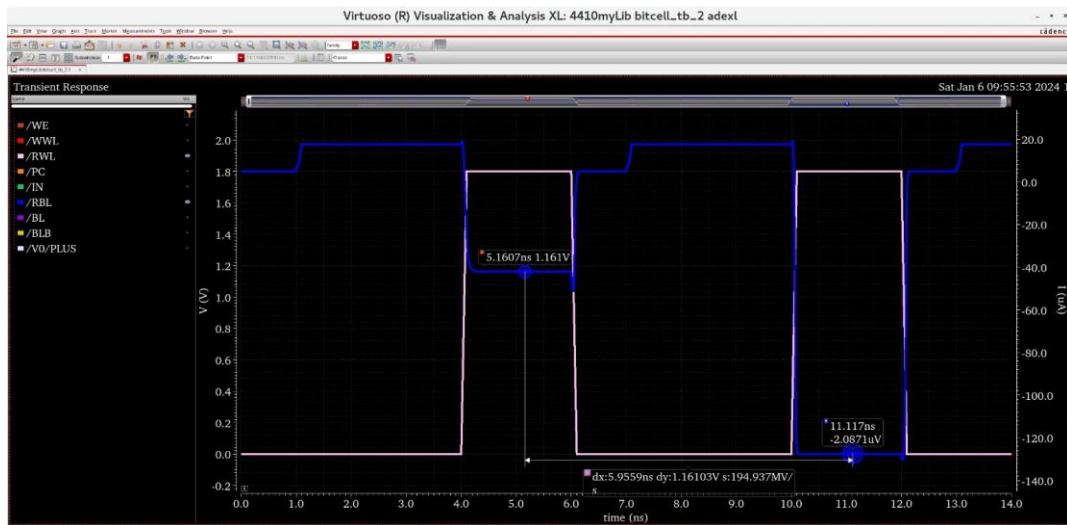


Figure 25. successful read and write operation combined with write driver and precharge

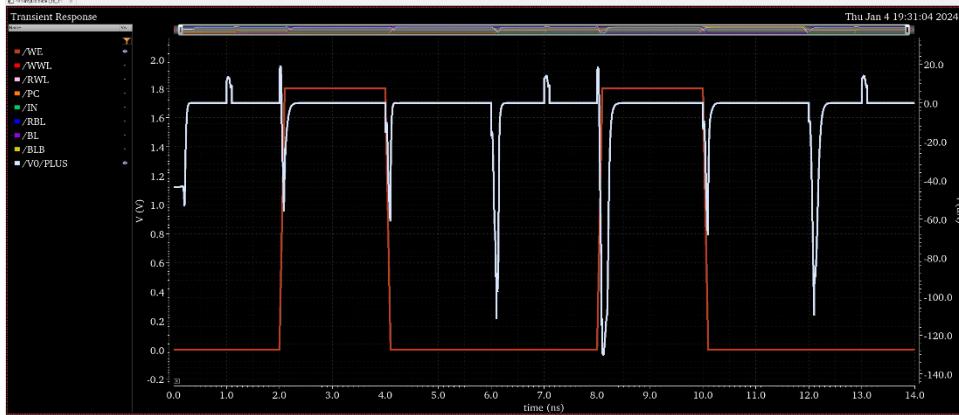


Figure 26. dynamic power consumption of SRAM bit cell, the largest power consumption during the write process is about 0.101mW

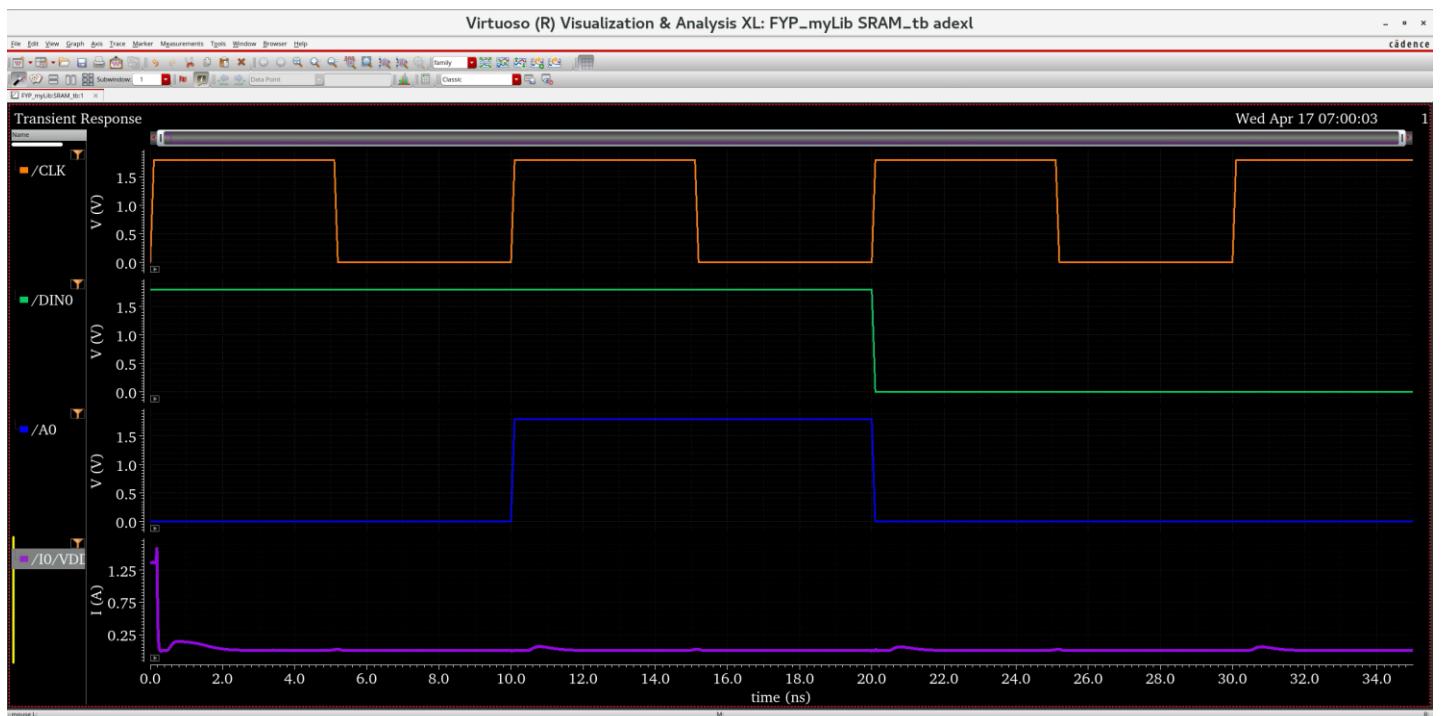


Figure 27. This is the simulation for the worst case power consumption during transient simulation. The worst case occurs when all input switches from 0 to 1 (or 1 to 0) and when we also have to write to 16 bits that are already written by the negated value before. First we wrote all 1s when the address is all 0s. Next I switch the address to all 1s. The final step is to switch the address back to all zeros and write all zeros to the cells. The power consumption will be measured at this step. After calculation, the power consumption is 5.534mW.

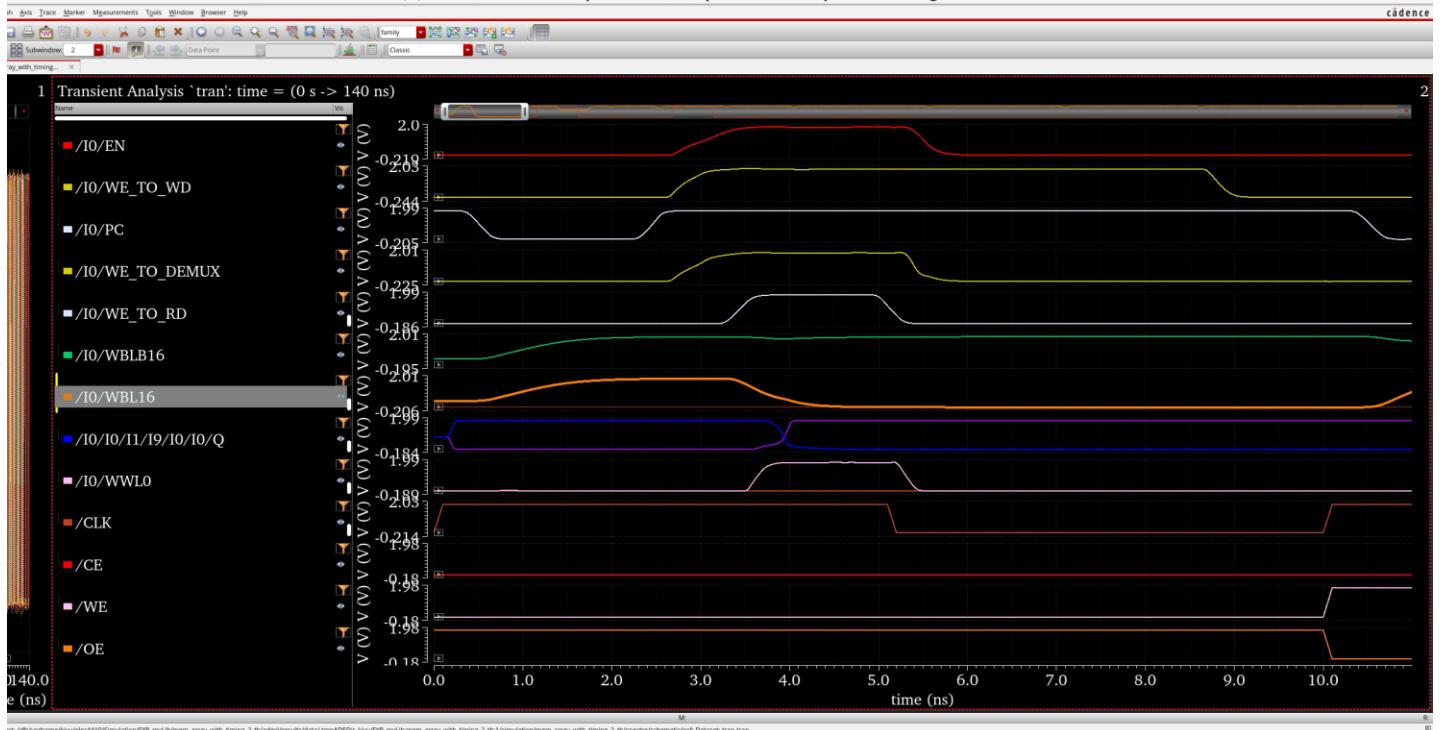


Figure 28. This is the write timing waveform of the SRAM. We can see that WBL and WBLB are precharged (6th and 7th plot) after PC is low (3rd plot). Then write driver is enabled(2nd plot) and the write column mux is also enabled(4th plot). After a little bit of delay, the row driver is enabled(5th plot) and it triggers WWL(9th plot) which causes the data to flip in the bitcell(8th plot, the blue curve is Q and purple is Qbar).

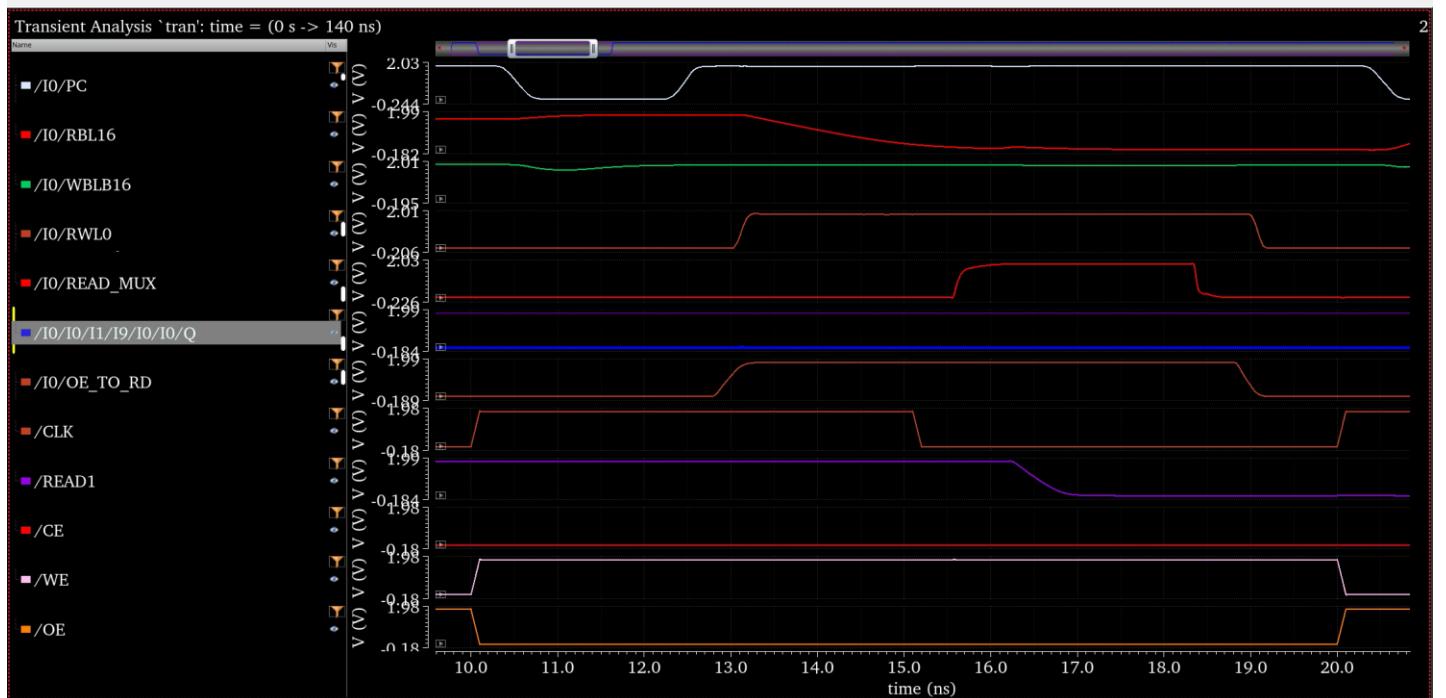


Figure 29. This is the read timing of the diagram. We can see that after the precharge process(1st plot), the output enable to row driver(7th plot) is high, then RWL is triggered (4th plot) which causes RBL(2nd plot) to be discharged as a 0 is stored in Q(6th plot, Q is blue and Qbar is purple). After the read column mux is on(5th plot), output(9th plot) is discharge to 0 in a very short period of time.

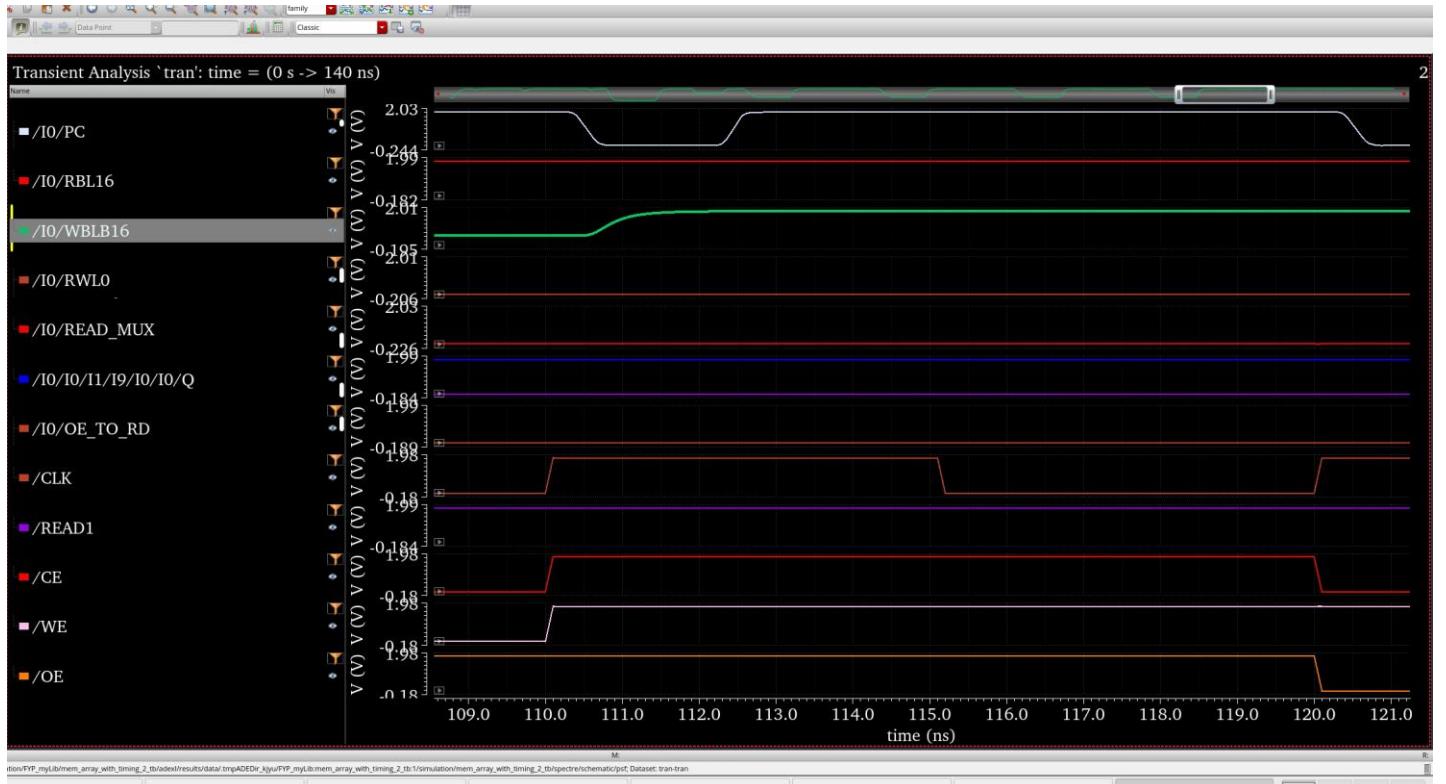


Figure 30. Idle mode waveform: When chip enable is high, the SRAM is in idle mode. Only the precharge process will continue to maintain the data in it.

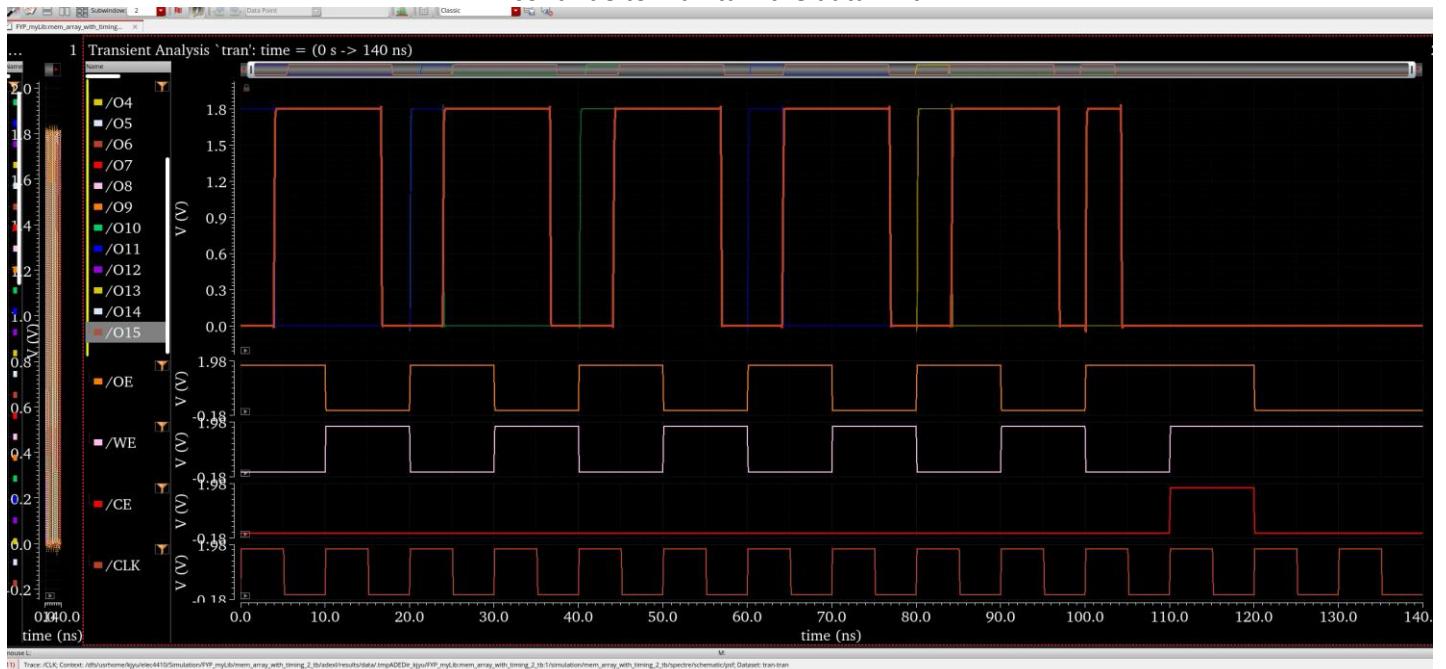


Figure 31. This is the pre-layout simulation of SRAM. The SRAM runs at a clock period of 10ns. Each write process followed by a read. The output waveform shown above is the XOR product of the output port with the input value. Read operation is carried out at 10 to 20ns, 30 to 40ns, 50 to 60ns, 70 to 80ns and 90 to 100ns which write operation is carried out at 0 to 10ns, 20 to 30ns, 40 to 50ns, 60 to 70ns, 80 to 90ns. The data input will change every 20ns. We can see that, at the end of each read operation, the output port has the same value as the input value (so the XOR product is 0). Also, during 110ns to 120ns the SRAM is in hold mode. After that, data is read at 120ns to 130ns and the XOR output is still 0. This means our SRAM is functioning well. The simulation is done at 27C, tt corner and 1.8V.

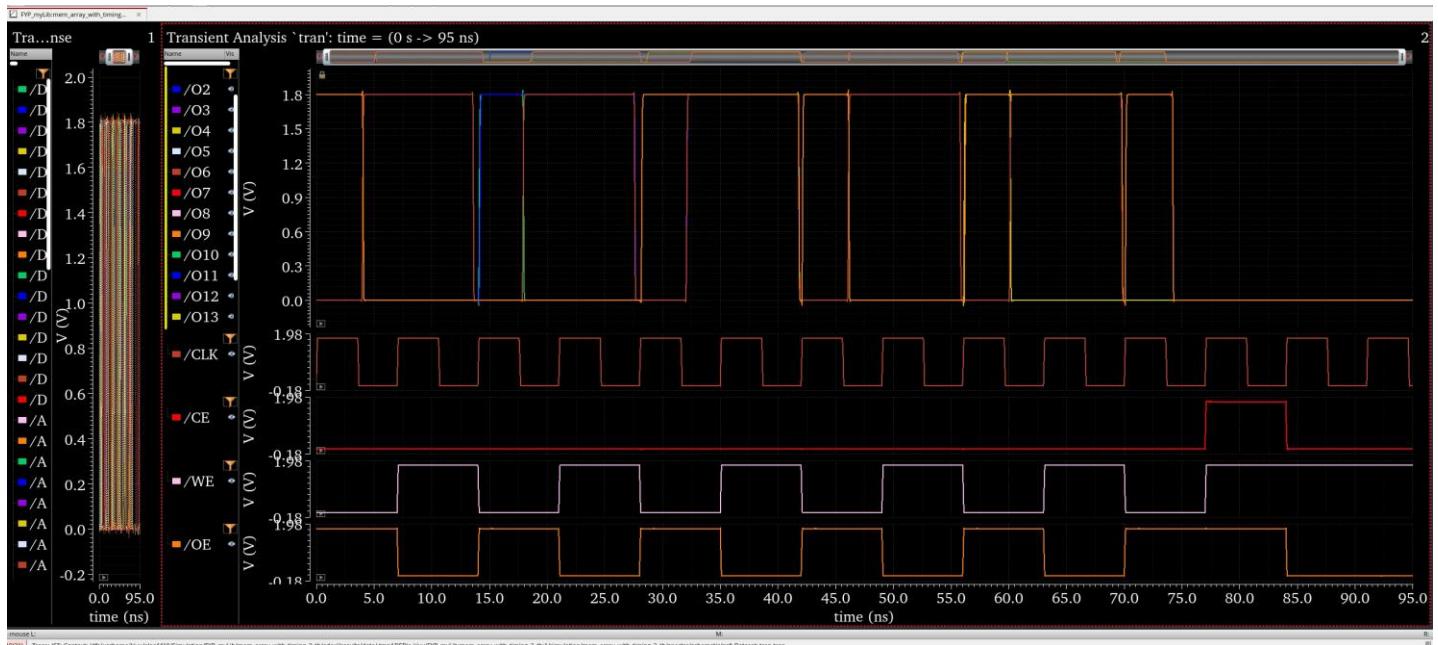


Figure 32. Simulation at clock period of 7ns, the data settles down before the end of every read cycle. If I decrease the clock period even further, the read and write operation cannot be guaranteed. This is done under 27degrees, tt corner and 1.8V.

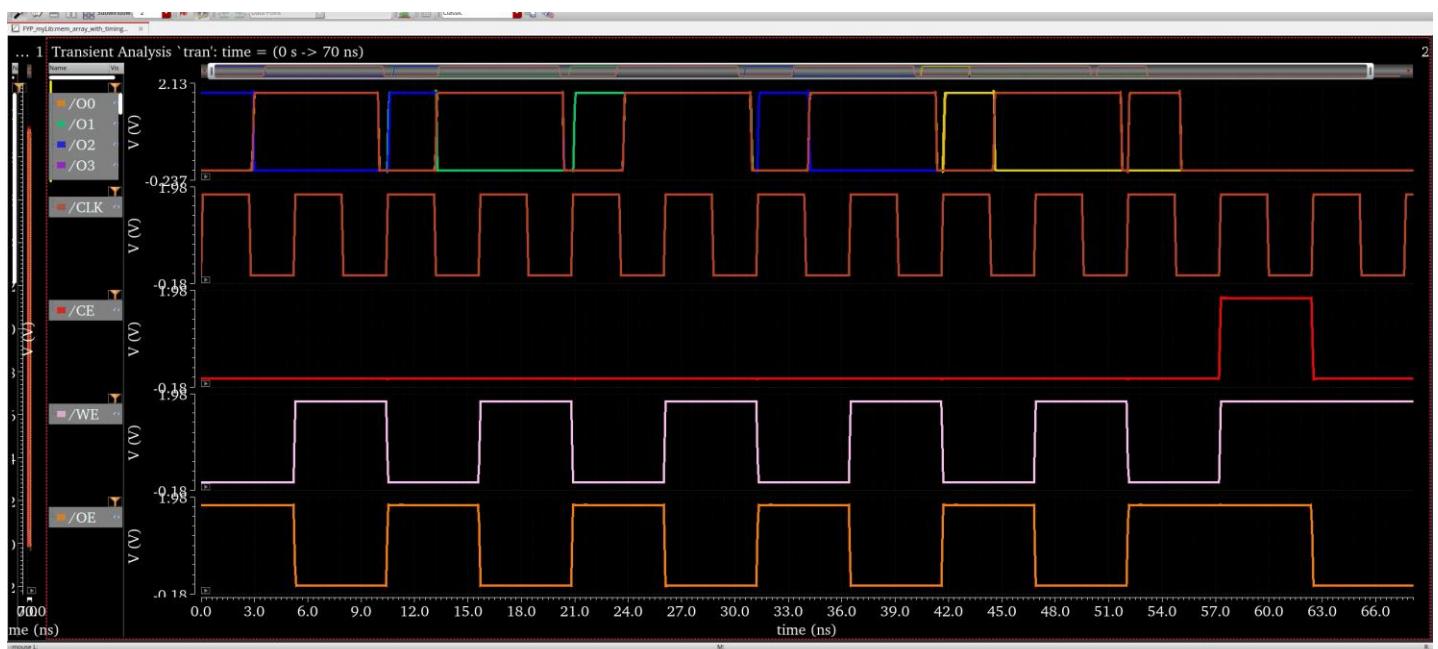


Figure 33. This is the simulation of the SRAM with ff corner at -40 degrees, clock period = 5.2ns, 1.89V

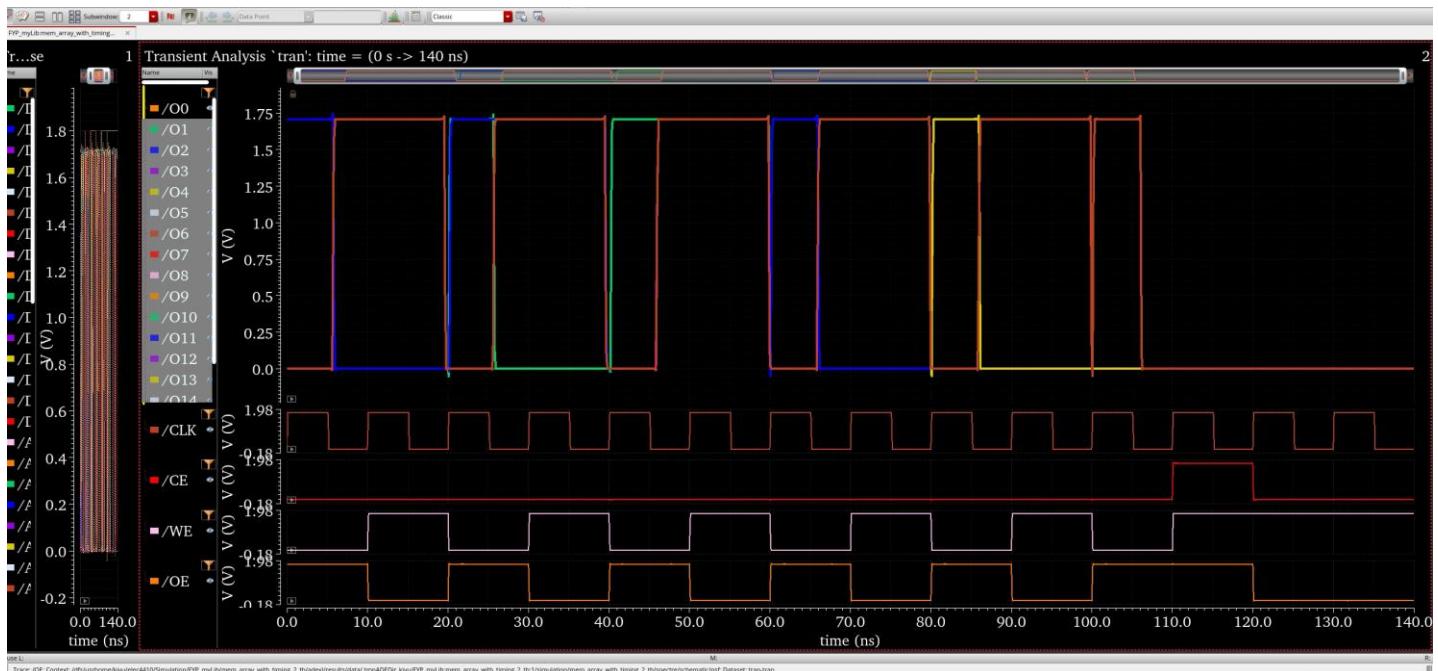
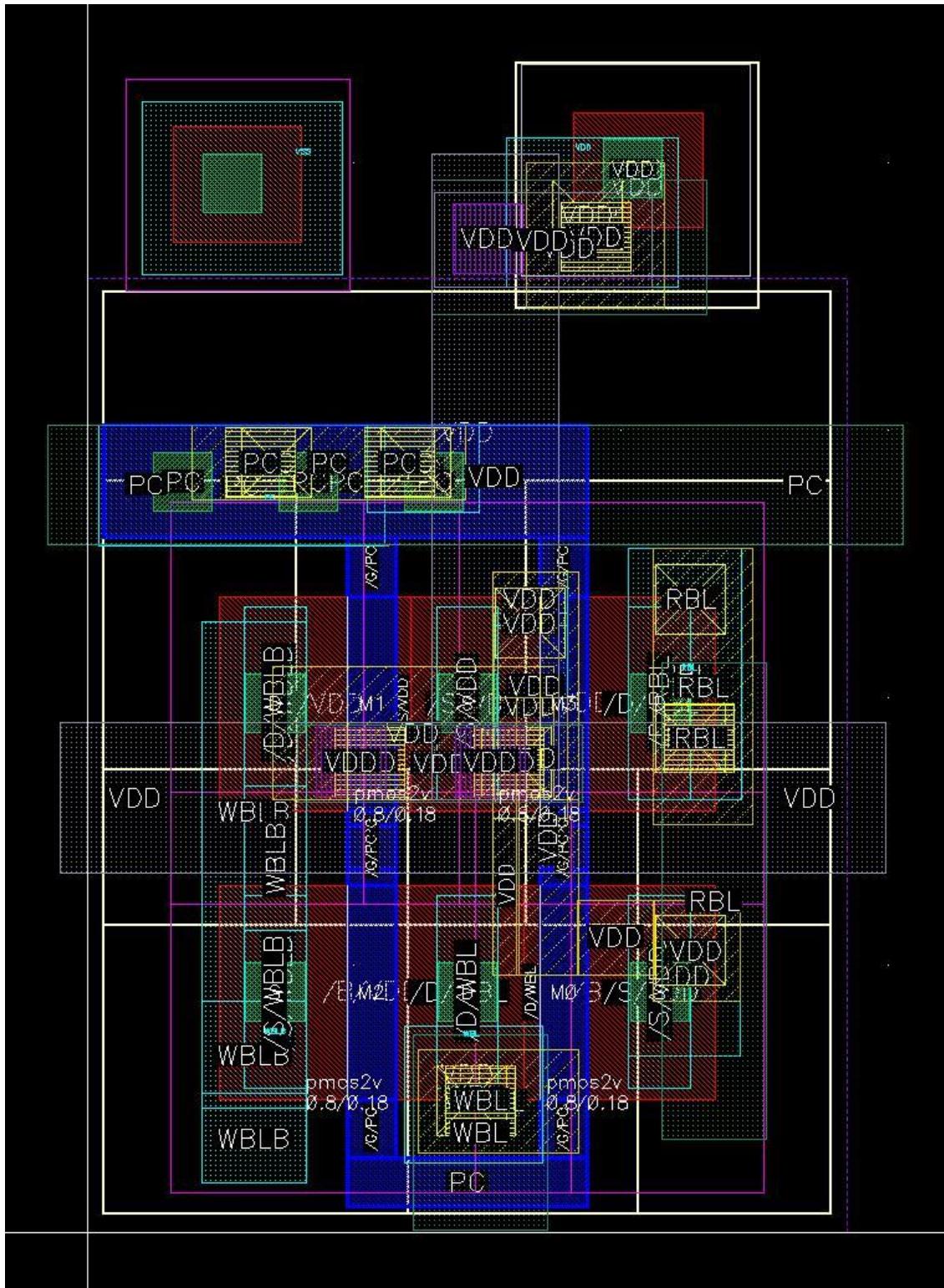


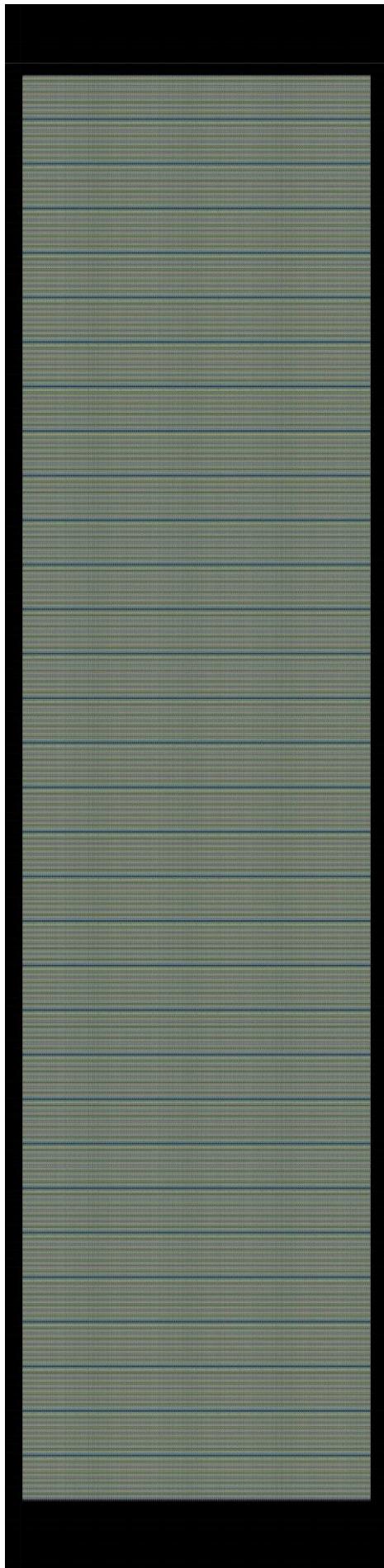
Figure 34. This is the waveform of the SRAM at ss corner at 125 degrees with 10ns clock period, powered up at 1.71V

Table for Minimum Clock Cycle

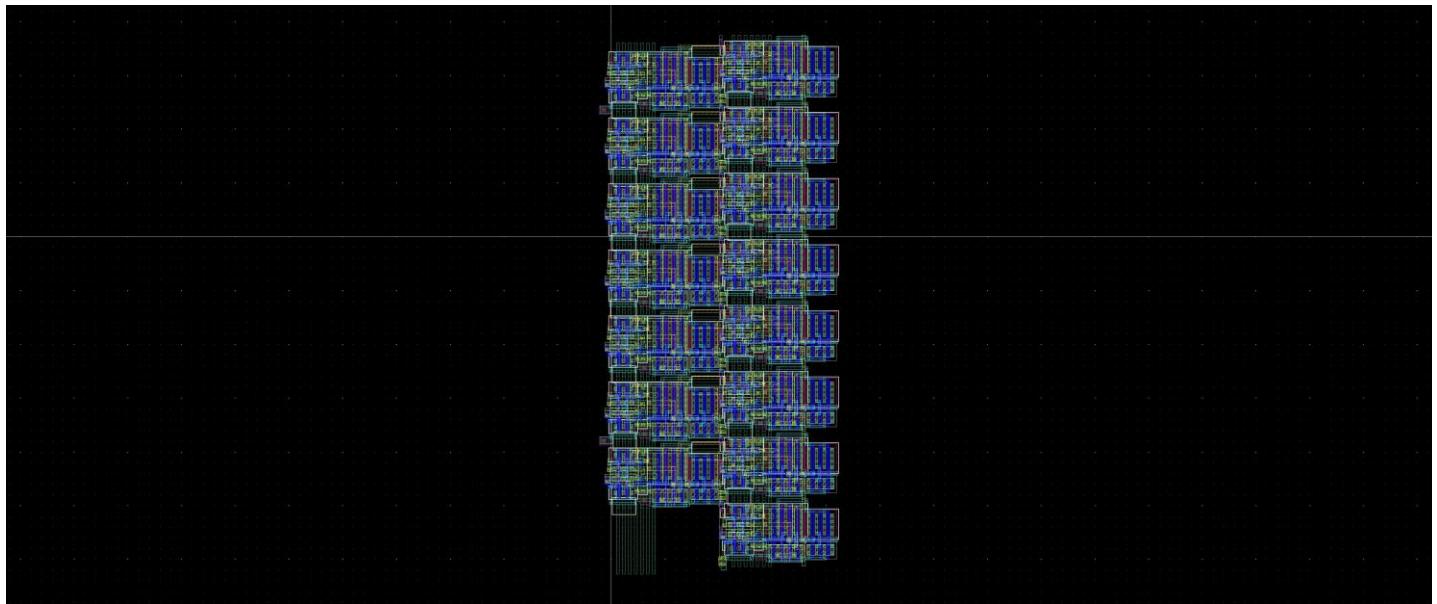
Ss, 125degrees, 1.71V	Tt, 27 degrees, 1.8V	Ff, -40 degrees, 1.89V
10ns	7ns	5.2ns



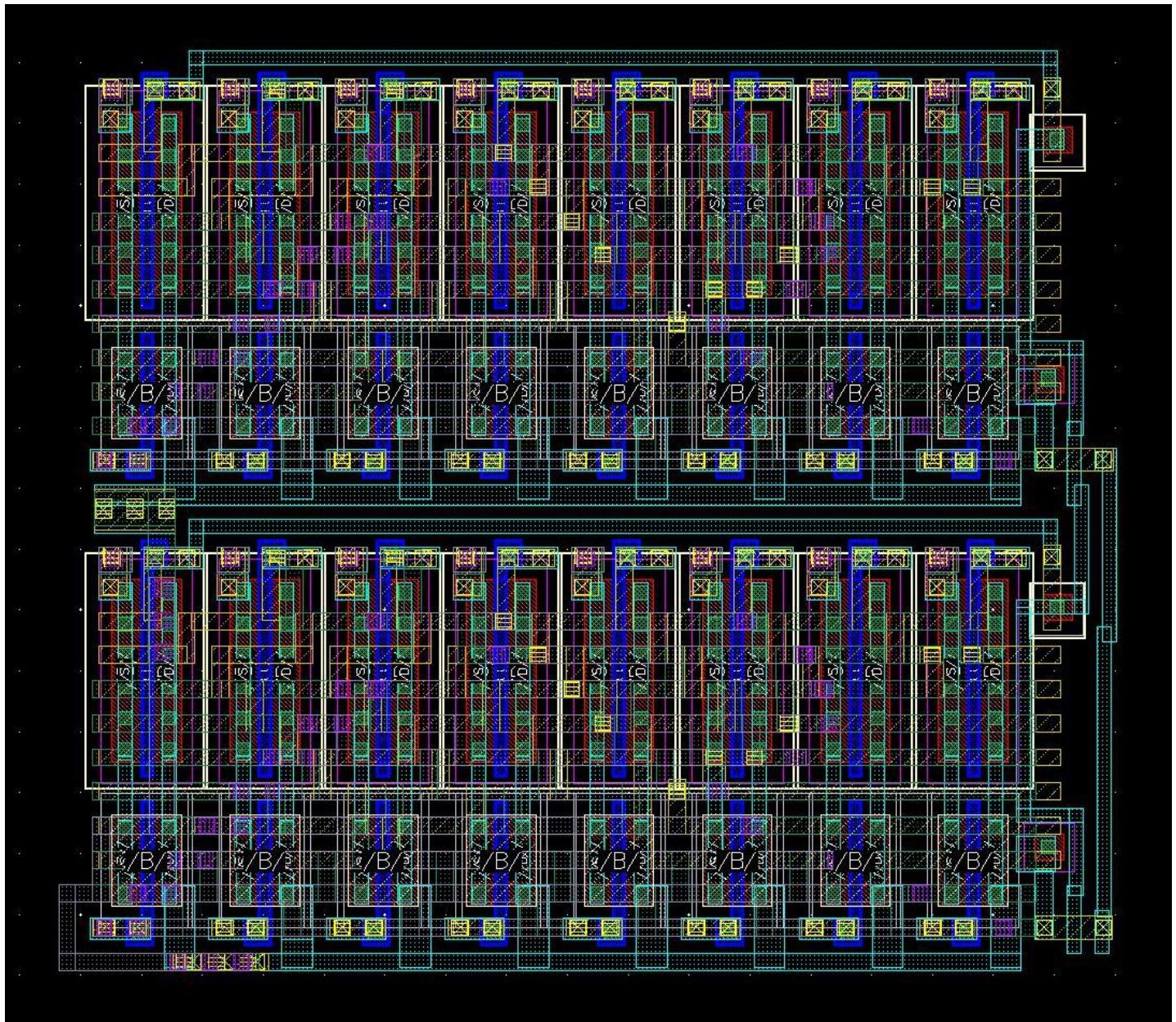
Precharge



256*256 memory array



Column decoder



Column mux