File 2\*256 memory array 90% delay

WEN (write enable of write driver) to BL (connected to demux)

(assume same as WEN to BLB)

Tphl: 1.013ns

Tplh: --

Clock to node PCW

Tplh: 1.012ns

Tphl: 850.82ps

PCW(precharge write) to BL

Tplh: 1.357ns (needs modification now)

Tphl: ---

BL to WBL1 (assume same as BL to WBL2, BLB to WBLB1, BLB to WBLB2)

Tplh: 0.82ns

Tphl: 166ps

PCR (precharge read) to RBL

Tplh: 2.54ns

Tphl: ---

REN(read enable) to RBL

Tplh: ---

TPhl: 2.338ns

Decoder

Tplh: 0.324ns

Row Driver

DOUT(asserted address) to WWL (word line in memory array)

Tplh: 0.496ns

Tphl: 0.440ns

DOUT(asserted address) to RWL (word line in memory array)

Tplh: 0.339ns

Tphl: 0.342ns

SA input to output

Tplh: 64.6ps

Tphl: 72.6ps

Comparing different precharge

Precharge 6

Tplh: 5.474ns

Tphl: 0.573ns

Energy consumption: 106.9\*10^-15J

Precharge 4

Tplh: 5.482ns

Tphl: 0.4617ns

Energy consumption: 106.5\*10^-15J