Advanced Analog Integrated-Circuit Design and Analysis

Midterm Project Report

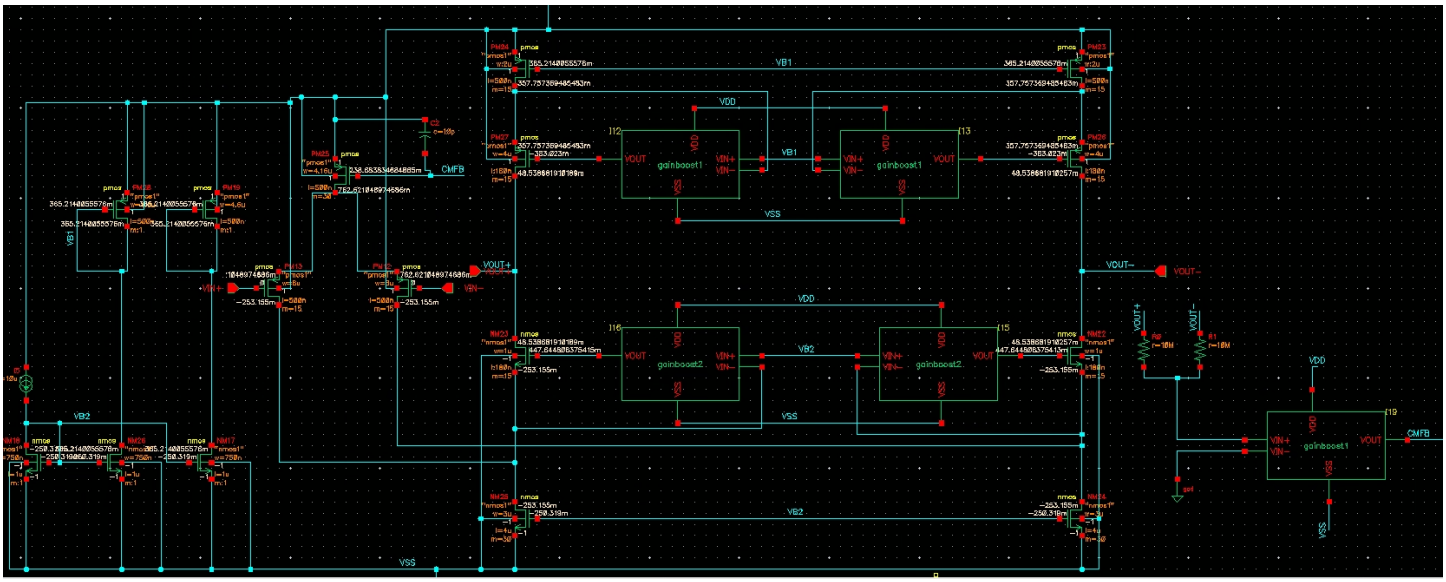
Course: EESM5120

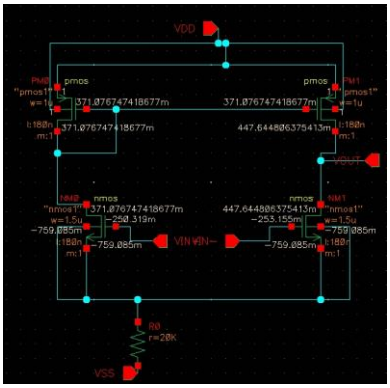
Semester: Spring

Group Members: Lo Evan Hong Tik, Hsu Yung Hsiang, Chio Yat Hei

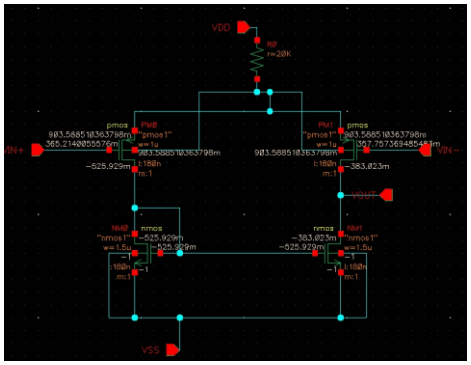
Date: 11/4

Amplifier topology





NMOS input pair auxiliary amplifer



PMOS input pair auxiliary amplifer

Summary Table – Specification vs. Performance

Fill in the table below with calculated and simulated performance values for each parameter.

Parameter	Specification	Calculation	Simulation	Meets Spec? (Y/N)	Comments
Supply Voltage	+/- 1.0 V	+/-1V	+/-1V	Y	/
Power Consumption	<= 2.0 mW	1.292mW	1.657mW	Y	Id will also be influence by vds and lamda
Low-Frequency Gain A_0	>= 80 dB	80dB	83.23dB	Y	Also influence by Id
Unity-Gain Frequency f_0	>= 300 MHz	368MHz	440.313MHz	Y	Id affectgm of the ouput so affect UGF
Slew Rate SR	>= 80 V/µs	130	Rising=121.5677 V/us Falling=125.6246 V/us	Y	
Phase Margin PM	>= 60°	78.25	70.72°	Y	parasitic capacitance and gain boosting amplifier produce poles
CMRR	>= 80 dB	infinite	362.279dB	Y	Pmos will have finite output resistance
PSRR (DC)	>= 80 dB	infinite	316.514dB	Y	Same as CMRR
PSRR (1 MHz)	>= 60 dB	infinite	316.482dB	Y	Same as CMRR
DC Output	0V +/- 50 mV	0V	$vo+$= 48.5387 mV $vo-$= 48.5387 mV	Y	
Differential Output Swing	>= +/- 1.2 V	+/-1.2V	+/- 1.20387V	Y	
Total Harmonic Distortion	< -30 dBc	/	-33db	Y	/
Input Offset Voltage	<= 100 mV	0V	9m	Y	
Equivalent Input Noise	<= 1 mVrms (1 MHz BW)	1.92uVrms	532.2u Vrms	Y	

1. Introduction

This project focuses on the design and analysis of a high-performance fully differential folded cascode operational amplifier featuring a PMOS input pair and gain-boosting amplifiers. The folded cascode topology is chosen for its high gain, wide output swing, and robust frequency response, making it ideal for precision analog applications such as data converters, sensor front-ends, and analog signal conditioning blocks.

The motivation behind this design is to explore advanced analog design strategies that balance gain, bandwidth, and power efficiency in modern CMOS processes. The use of gain boosting enhances the intrinsic gain of the amplifier by increasing the output impedance without increasing bias current, allowing us to meet tight performance targets within stringent power constraints.

The specific design goals for this op-amp are as follows:

- Topology: Fully differential folded cascode amplifier with PMOS input pair and NMOS folded cascode branch
- Gain-boosting: Two auxiliary amplifiers used to enhance output resistance of the cascode transistors
- Technology: gdpk180

2. Background and Theory

The design of a high-performance analog amplifier requires a solid understanding of both **device-level behavior** and **system-level analog design principles**. This section summarizes the key theoretical concepts that guided the design of the folded cascode amplifier with a PMOS input pair and gain-boosting.

MOSFET Operation and Transconductance Efficiency

The MOSFET operates in three regions: cutoff, triode, and saturation. For analog amplifiers, operation in the **saturation region** is essential to achieve high intrinsic gain and predictable current behavior. The key small-signal parameter is the **transconductance** gmg_mgm, which quantifies the current drive capability:

$$gm = \frac{2ID}{Vov} = \frac{2I_D}{V_{GS} - V_{TH}}$$

To design for both performance and power efficiency, we used the **gm/ID design methodology**, which directly relates the **transconductance efficiency** to the **inversion level** of the device. This approach helps balance **linearity**, **gain**, and **bandwidth** while optimizing current usage.

Folded Cascode Topology

The **folded cascode** is a two-stage amplifier configuration that uses a cascode current path to isolate the input stage from the output. It provides:

- **High gain** via high output impedance
- **Wide output swing** compared to a telescopic op-amp
- **Better input-output headroom management**

In our design, a **PMOS input pair** is used to maximize input common-mode range, and a **folded NMOS branch** is used to steer current into the output stage. The output impedance is significantly enhanced by **cascode devices**, which stack multiple transistors to multiply resistance:

$$Rout \approx (roN1 \parallel roN2) \parallel (roP1 \parallel roP2) R_{out} \approx (r_{oN1} \parallel r_{oN2}) \parallel (r_{oP1} \parallel r_{oP2}) Rout \approx (roN1 \parallel roN2) \parallel (roP1 \parallel roP2)$$

Gain-Boosting Technique

To further improve DC gain without increasing channel length or current, **gain-boosting amplifiers** are used to drive the gates of the cascode devices. By sensing small variations at the cascode nodes and feeding back a correcting signal, gain boosters effectively increase the output resistance of the amplifier:

$$ro, boosted \approx ro(1 + Aboost)$$

This allows us to achieve **gains above 80 dB** with only moderate power consumption.

Common-Mode Feedback (CMFB)

In a **fully differential amplifier**, the common-mode output voltage can drift due to mismatches or variation. To stabilize it, a **common-mode feedback (CMFB)** circuit is implemented. It senses the average of the two outputs:

$$VCM = \frac{V_{out+} + V_{out-}}{2}$$

The CMFB amplifier compares this to a reference (e.g., 0 V) and adjusts the tail current or biasing of the output stage to maintain common-mode stability.

Bandwidth, UGF, and Stability

The **unity-gain frequency (UGF)** is primarily determined by:

$$f_{UGF} = \frac{g_m}{2\pi C_L}$$

3. Design Approach

Detail your design methodology. Explain your topology choice (e.g., folded cascode), design flow (gm/ID strategy, sizing), and simulation strategy. Include design trade-offs and decisions.

The topology chosen was folded cascode with gain boosting/regulated cascode. This topology was chosen with the intention of achieving high gain and bandwidth, with enough headroom. The sizing was determined by the following equation:

$$\frac{W}{L} = \frac{2Id}{uCox(Vov)^2}$$

The result calculated initially: (We assumed Vov = 0.2 as Vov <= 0.2 to maintain a +/-1.2V output swing)

		L	1.80E-07
NMOS W/L	1.448016		
		Wn	2.61E-07
PMOS W/L	9.191176		

Wp 1.65E-06

i. Unity Gain Frequency, Low-Frequency Gain, Phase Margin

$$f_0 = \frac{gm}{2\pi C_{out}} \geq 300Mhz$$

2.314m/2piCOUT=368Mhz

ii. Gain: $Av \approx gm1 \cdot [(ro1 \parallel ro5) \cdot gm3 \cdot ro3 \cdot (1 + Aboost)] \parallel (gm7 \cdot ro7 \cdot ro9 \cdot (1 + Aboost))$

which can be transformed to $A_v \approx \frac{2}{\lambda^2 V_{ov} I_D} \cdot (1 + A_{\text{boost}})$

For A_v >= 60dB with A_{boost} >= 20dB,

For Vds ~ 400-600mV, lambda is around 0.1, with Vov = 200mV, the Av can be around 80-90dB as

$A_{boost} = Av \approx gm \cdot (ro,p \parallel ro,n) = \frac{2}{\lambda \ V_{ov}}$, with lambda being proportional to channel length.

iii. Slew Rate:

SR=2Id/Cout

Consider the above equation

Id minimum= 40uA to fulfil SR larger than 80u

Take into other considerations. We take Id=65

SR~130

iv. Phase Margin: $f_p > 2f_u$ Identify the dominant pole $p1 \approx \frac{1}{2\pi RoutCL}$, and second pole $p1 \approx \frac{1}{2\pi RcasCcas}$

PM = 180 - $tan^{-1}\left(\frac{p2}{\omega UGF}\right) - tan^{-1}\left(\frac{p1}{\omega UGF}\right)$ = 180 - ~90 - 11.25=78.25

v. Output Swing: As mentioned above, Vov = 0.2V and output swing = (1-0.2-0.2)x2 = +/-1.2V

vi. DC output: For DC output = 0V, we must make sure the total two PMOS pairs Vds is 1V, which can ensure DC output to be 0V. ie (Each Vds = 500mV or the load is 300mV with the folded one being 700mV). In our case, we will ensure that the Vdsat for both pmos to be <= 200mV. Thus, we also make use of common mode feedback to ensure the DC output can be guaranteed to be in the range of 0V as it sense 0V at the amplifier to feedback to 0V.

vii CMRR PSRR : no mismatch so both = infinite

Viii input noise voltage

Veq^2=2(4KT)(2/3)(1/gm1)1Mhz=1.92uVrms

x.power consumption
10u bias circuit current, 2u pmos gain boosting, 6u nmos gain boosting, 300u folded cascode circuit total consumption

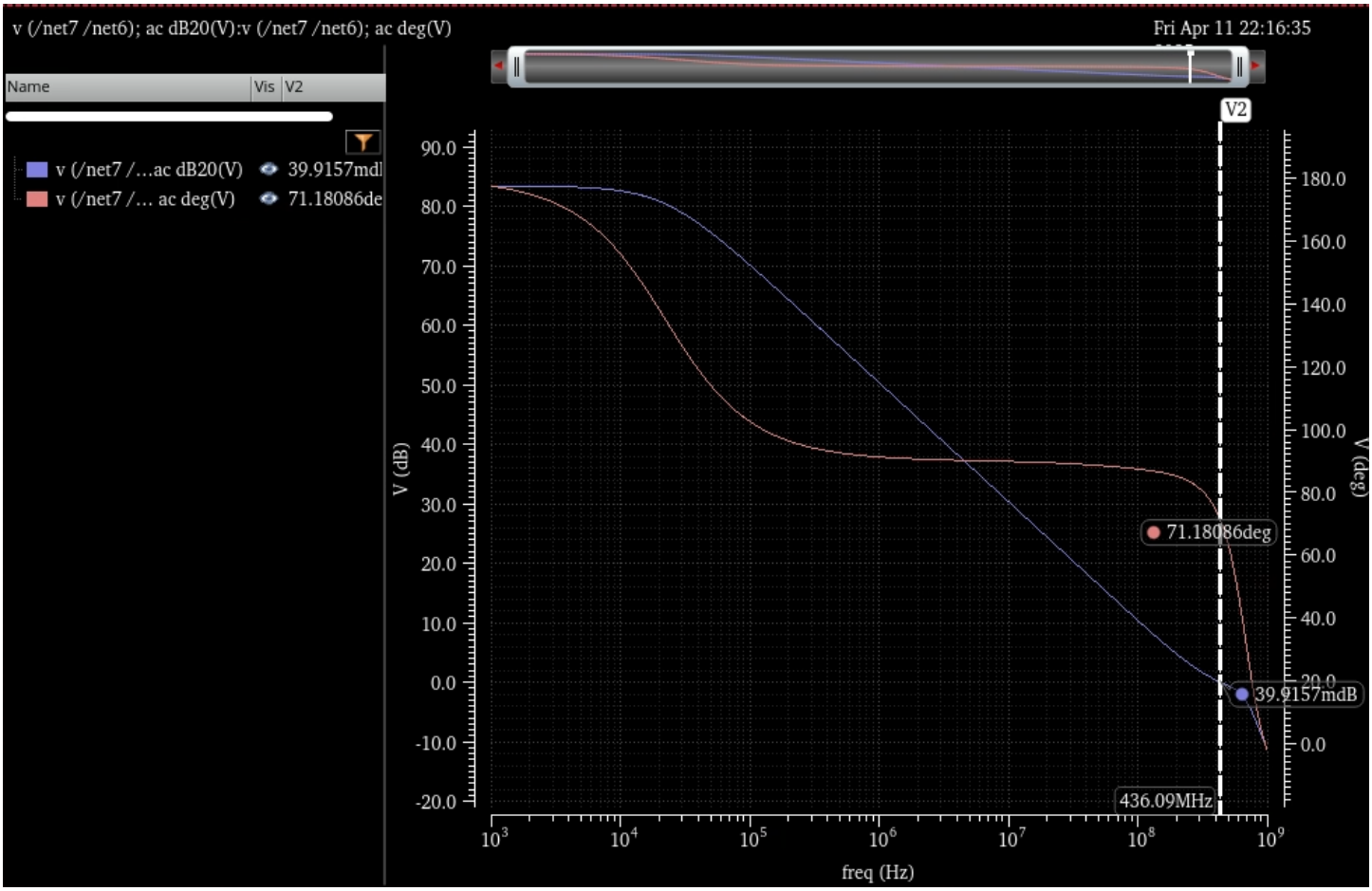
(10u*3+2u*2+6u*2+300u*2)*2=1.292m

Without any mismatch, there should be very small input offset voltage or close to 0V.

4. Simulation Results

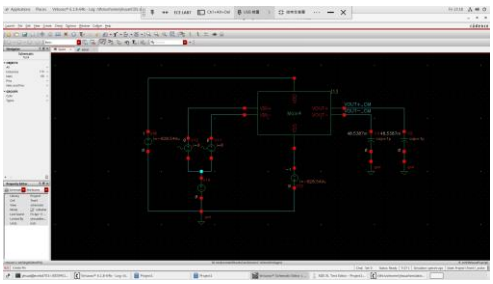
Provide key simulation results: gain, UGF, phase margin, power consumption, transient response, etc. Include annotated plots where applicable. Discuss how results match design targets and theory.

i. Unity Gain Frequency, Low-Frequency Gain, Phase Margin



A0=83.23dB, f0=436.313Mhz, PM=71.718°

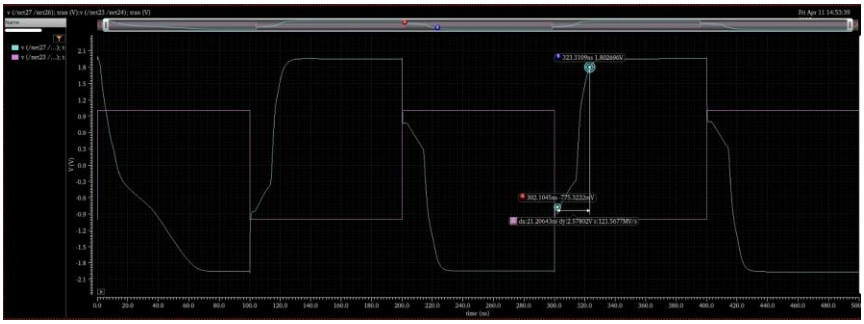
ii. Power Consumption & DC Output

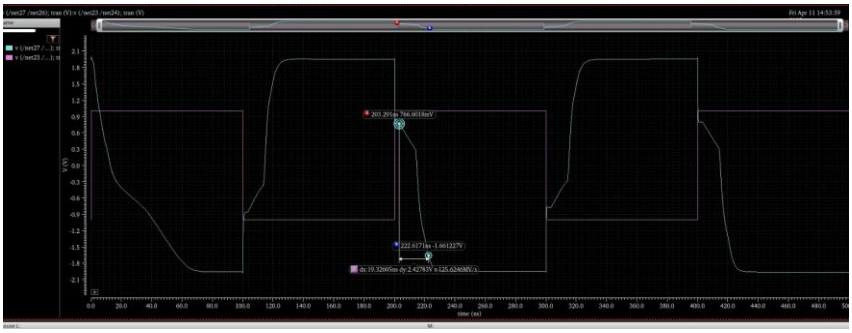


$Power\ Consumption = 828.54uA \times 2 = 1.657mW$

DC Output: $vo+ = 48.5387\ mV$, $vo- = 48.5387\ mV$

iii. Slew Rate SR

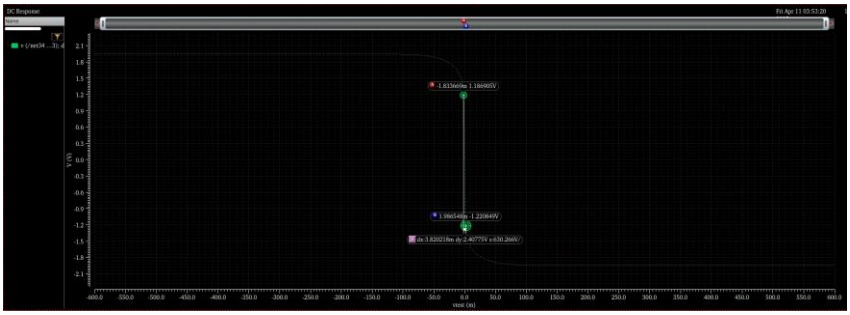




SR Rising = 121.5677 V/us

SR Falling = 125.6246 V/us

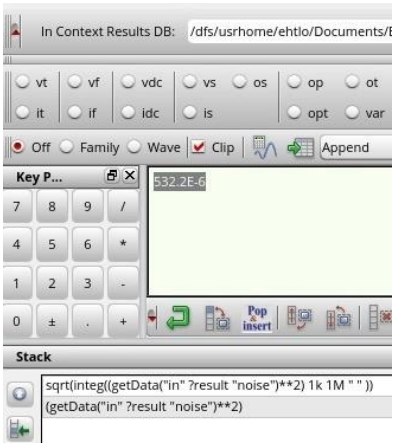
iv. Differential Output Swing



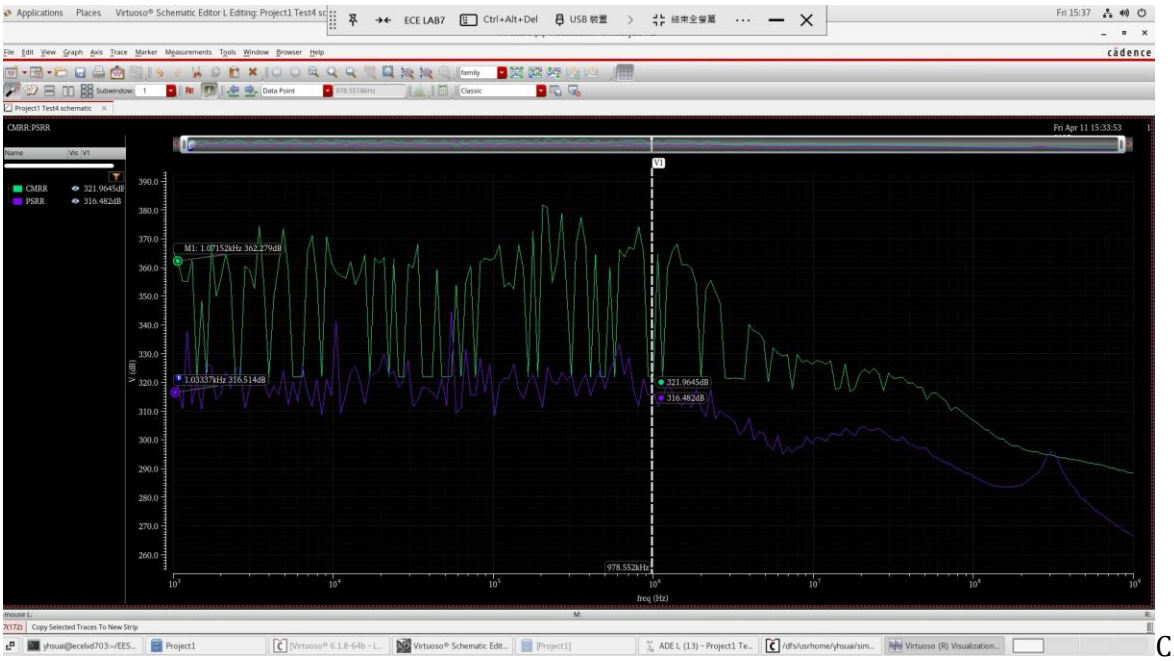
Differential Output Swing = +/- 1.20387V

v. Equivalent Input Noise

Input Noise = 532.2u *V*rms



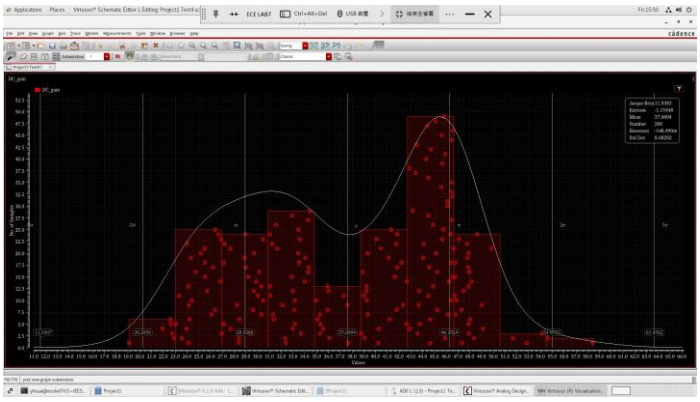
vi. CMRR & PSRR



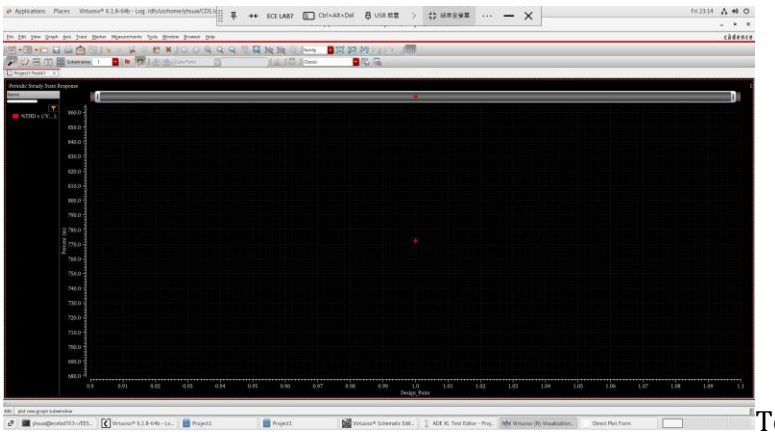
CMRR = 362.279dB

PSRR at dc = 316.514dB, 316.482dB at 1Mhz

vii. Monte Carol Simulation Result

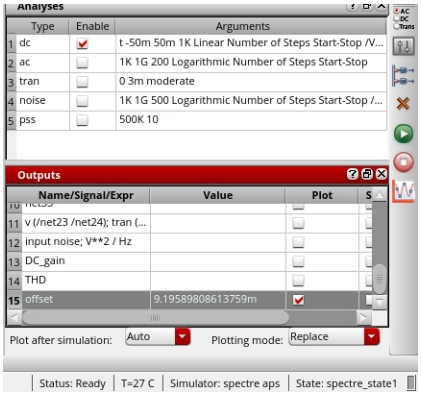


viii. Total Harmonic Distortion



Total Harmonic Distortion =772.344m% = -42.2db

ix. Input Offset Voltage: Input Offset Voltage = 9.19mV



5. Discussion and Analysis

The results were satisfactory, as the topology chosen has a possibility of being made much better, including the gain, bandwidth, phase margin, total harmonic distortion and output swing. The biasing of the circuit was done poorly which caused the opamp to fail for a large amount of the project time. This proves the importance of biasing points as well as hand calculations.

Initially, the amplifier was subject to **improper biasing**, which led to multiple degradation effects:

- **Common-mode drift**: The output common-mode voltage was not held at the intended 0 V reference, due to an unstable or under-compensated **common-mode feedback (CMFB)** loop. This caused unequal voltage drops across the differential branches, pushing some devices out of saturation.
- **Tail current instability**: In some cases, the **PMOS current source** controlled by CMFB was either too aggressive or not properly settled, leading to over- or under-driving of the input pair, which in turn affected both **gain** and **linearity**.
- **Gain boosters out of range**: The **gain-boosting amplifiers** that control the cascode gate voltages are also bias-sensitive. When bias voltages were not properly tuned, the boosters operated near their rail limits, causing their outputs to clip or saturate, which degraded their effectiveness in increasing the output resistance.

Gain Degradation

The **DC gain** target for this design was ≥ 80 dB. However, early simulations showed gain values closer to **40–50 dB**, primarily due to the following reasons:

- **Low r_0** from cascode devices due to insufficient channel length or improper inversion region (e.g., strong inversion with low gm/ID).
- **Gain-boosting failure**: When the gain boosters operated outside their linear region (due to poor bias), they failed to enhance the output impedance of the cascode nodes. As a result, the effective output resistance dropped significantly, reducing overall voltage gain.
- **Saturation loss**: In some simulations, certain transistors entered the **linear region** due to poor node voltage control (especially in the folded branches), effectively reducing the active output path gain.
- **Mismatch between input and folded currents**: When the current in the input pair was not properly mirrored into the folded path, the gain dropped due to unbalanced transconductance and voltage swings.

As letting the common mode feedback amplifier to bias the PMOS current source, this acts as a last resort due to the lack of time and effort, it poses an instability in the circuit which can lead to poor start up behaviour or uncontrolled bias condition if you don't design it carefully.

The main difference between the simulation and the hand calculations are mainly due to the short channel effect as well as the parasitic capacitance that messes up the pole positions, which in turn made the phase margin hard to achieve. The gain boosting amplifier is also a big problem to phase margin and a big effect on the bandwidth, as it also creates a lot more poles that are unidentifiable at first glance. The gain is also lower than expected as the r_0 of the mosfets varies with the channel length modulations which made it hard to identify a precise gain.

6. Conclusion

This project designed and analyzed a high-performance fully differential folded cascode operational amplifier with a PMOS input pair and gain-boosting amplifiers, meeting most specified performance targets in the gdpk180 CMOS process. The amplifier achieved the required specifications, demonstrating robust performance suitable for precision analog applications such as data converters and sensor interfaces.

We have learned to include the critical importance of precise biasing to maintain transistor operation in the saturation region, the sensitivity of gain-boosting amplifiers to bias conditions, and the need for robust common-mode feedback (CMFB) design to stabilize output voltages. The project underscored the trade-offs between gain, linearity, and power efficiency. Additionally, re-evaluating the phase margin measurement and refining the CMFB loop could enhance overall stability and performance.

In summary, this project provided advanced analog design introduction, achieving a high-performance amplifier. folded cascode topologies and gain-boosting techniques.

7. Individual Contributions

Specify what each group member contributed to the project (design, simulation, documentation, etc.).

Lo Evan Hong Tik: most design, simulation and part1,2,3,5 report

Hsu Yung Hsiang: some design, sizing, simulation, and part4,6 report

Chio Yat Hei: sizing, simulation, part3 report

Appendix

Include detailed derivations, extended simulation data, or any relevant supporting material.

I. Transistor Sizing

MOSFET numbers	W(um)	L(um)
PM18	4.6	0.5
PM19	4.6	0.5
NM18	0.75	1
NM26	0.75	1
NM17	0.75	1
PM25	4.16	0.5
PM13	6	0.5
PM2	6	0.5
PM24	2	0.5
PM23	2	0.5
PM26	4	0.18
PM27	4	0.18
NM23	1	0.18
NM22	1	0.18
NM24	3	4

NM25	3	4
PM0(GAINBOOST_P)	1	0.18
PM1(GAINBOOST_P)	1	0.18
NM0(GAINBOOST_P)	1.5	0.18
NM1(GAINBOOST_P)	1.5	0.18
PM0(GAINBOOST_N)	1	0.18
PM1(GAINBOOST_N)	1	0.18
NM0(GAINBOOST_N)	1.5	0.18
NM1(GAINBOOST_N)	1.5	0.18

References

Razavi, B. (2001). *Design of analog CMOS integrated circuits* (International ed.). McGraw-Hill.