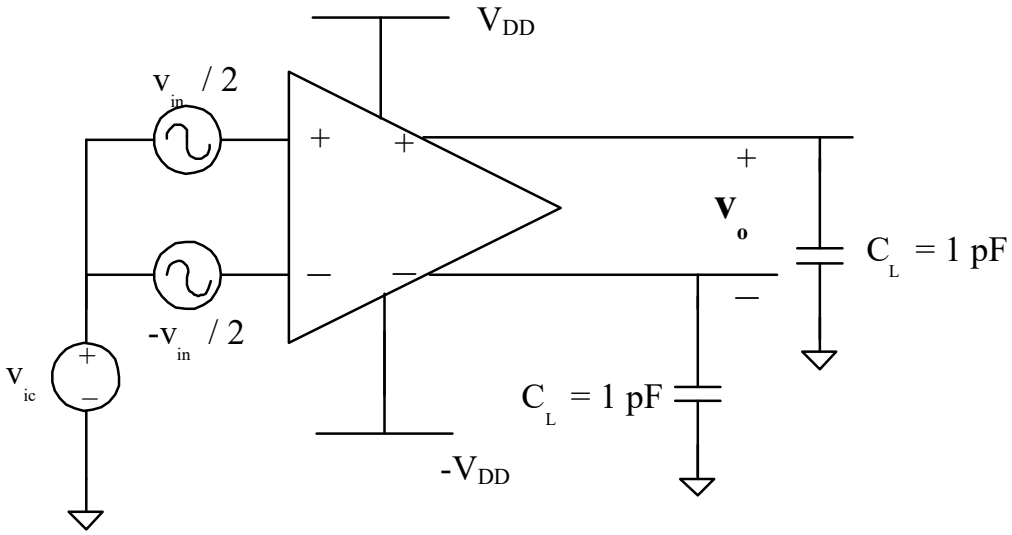
EESM 5120 8 February 2025
Spring 2025 Howard Luong

Advanced Analog Integrated-Circuit Design and Analysis

Midterm Project – Amplifier Design

(Due before 11:59PM on April 11th)

In this project, you are to design a low-power low-supply fully-differential CMOS amplifier as shown below and to verify the performance using simulations. The main objective is to meet ALL the specifications listed in Table 1 with minimum power consumption.



To give you an opportunity and more motivation to work on an amplifier project that is more related to your own work/research and thus more interesting to you, you are welcome to propose changes in some of the specifications, in particular in terms of speed, power, and supply voltage. However, you would need to submit your proposal with explanation and justification to me before March 11 for approval first.

You are to work in groups of two or three, and only one report is required from each team. You can use any CMOS process and any technology node with available models or PDKs. You are free to choose any circuit approach, configuration, and technology for your design. However, you should be able to justify your choice.

For each of the required specifications, you are required to

a. Come up with an appropriate test circuit

b. Run HSPICE simulations

c. Include in the report the schematic diagram of the test circuit and its simulation results.

d. Comment and justify any discrepancy from the hand calculation.

Table 1: Specifications of the amplifier

Parameters	Specifications
Supply Voltage	+/- 1.0 V
Power Consumption	<= 2.0 mW
Low-frequency Gain A_0	>= 80 dB
Unity-Gain Frequency f_0	>= 300 MHz
Slew Rate SR	>= 80 V/μs
Phase Margin PM	>= 60°
CMRR	>= 80 dB
PSRR	>= 80 dB at dc
	>= 60 dB at 1 MHz
DC Output	0V +/- 50 mV
Differential Output Swing	>= +/- 1.2 V
Total Harmonic Distortion (v_{id} = 75% FS)	≤ -30 dBc
Input Offset Voltage	<= 100 mV
Equivalent Input Noise	<= 1 mV_{rms} (integrated over 1MHz BW)
(Single-Ended) Load Capacitor C_L	1 pF

For device mismatches, you can use the Monte Carlo models from available PDKs, or you can simply assume that the worst-case mismatches for passive devices and active devices are 0.5% and 5%, respectively. You can assume that the worst-case mismatch in threshold voltage is 50 mV.

You are free to use as many bias current and voltage sources as necessary. However, all these bias sources need to be generated from a single external current source or voltage source, and the power consumption of these bias sources would need to be included in the total power consumption.

It is important to meet all the specifications. However, clever and creative designs will be valued much higher. As such, you should not hesitate to try out *novel* designs or topologies.

In designing the amplifier, you are highly recommended to apply the methodology illustrated in the following flow chart. More specifically, you are encouraged to:

a. First determine which specifications are the most difficult to achieve
b. Accordingly, select a suitable amplifier topology
c. Do enough hand calculation and preliminary HSPICE simulation to make sure that those difficult specifications are met
d. Estimate and include all parasitic capacitance
e. Resimulate the circuit with all parasitic and fine-tune the device sizes if needed
f. Verify the circuit performance and if necessary repeat the whole procedure until all the specifications are met.

For your information and motivation, in the final project, you will be asked to design an active filter, for which you will need to reuse the amplifier you are designing as a key building block.

Hints on Simulation:

1. Slew Rate: For differential amplifiers, you cannot use the same unity-gain feedback configuration for single-ended versions to determine the slew rate. Instead, you would need to simulate it in an open loop, ie. applying a small step at the input and measuring the slew rate at the output before it becomes saturated. Please make sure to reset or to do separate simulation for positive-slewing and negative slewing input signals.

2. Offset: Similarly, you cannot use the unity-gain feedbackconfiguration for offset, but you would need to plot dc transfer curve and to determine the offset by definition, which is the input voltage required for the output voltage to be zero. Without the random process variation, the offset is systematic and typically is very small, and you would need to zoom in the plots for high resolution and high accuracy.

Reminder:

Plagiarism, as serious academic misconduct, will not be accepted, and violators will be subject to disciplinary actions according to the university policy, including an F grade for the course or even possible expel from the university