EESM 5120 Project Report: Analog Filter Design

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Contents

1 Introduction

This report presents the design, simulation, and analysis of an analog filter circuit . We involve a systematic design of passive and active filter stages, calculated results and verified with Cadence simulation.

The simulation results demonstrate that the filter achieves a cutoff frequency of 245MHz, with a passband ripple of 0.5 dB, meeting the target specifications. Detailed comparisons between calculated, simulated, and specified parameters are provided in the beginning of the report.

Specifications

Parameters	UWB Specifications	Calculated	Simulated
Characteristic	Low-pass	Low-pass	Low-pass
Passband Gain	0–10 dB	10	7
Passband Ripple	<=1 dB	0.5 dB	0.762 dB

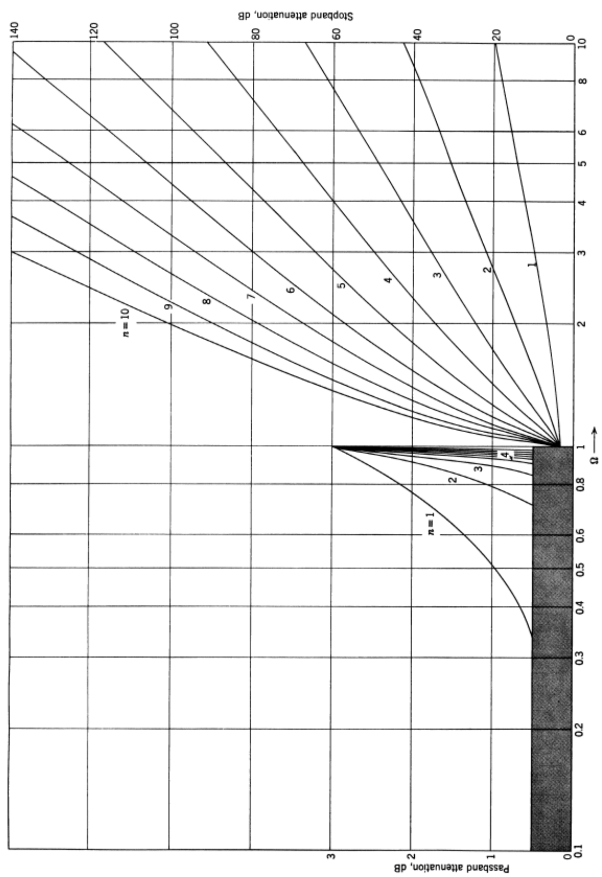
Clock Frequency fs	<= 200 MHz	Must less than 200MHz	10.4323MHz
Lower -3 dB Frequency	5KHz < flo < 2 MHz	150kHz	161.075kHZ
Upper -3 dB Frequency fup	253 MHz < fup < 264 MHz	250MHz	254.084MHz
Lower Corner Channel Attenuation	>15 dBc @ dc	>15dBc	95dBc
Adjacent Channel Attenuation	> 12 dBc @ 500 MHz	>30dBc	25.02223dBc
Alternating Channel Attenuation	> 30 dBc @ 792 MHz	>50dBc	42.18612dBc
Source Resistor	1KΩ	1KΩ	1KΩ
Load Resistor	200Ω	200Ω	200Ω

2 Circuit Performance

2.1 Passive and Active Filter Design

The filter design began with a passive Chebyshev filter for basic frequency response, followed by active stages to enhance gain and selectivity. The passive filter was designed with a cutoff frequency of 245M Hz, using a 4^{th} order LC filter as decided from the attenuation curve. We then replaced the passive components with active ones using Gm-C topology.

Component values were chosen based on the Chebyshev type I 0.5 dB ripple 4^{th} order table, and calculations ensured compliance with the target specifications. The N = 4 is decided from the attenuation curve. From the attenuation curve[1], we can see that n = 4 can provide some margins.



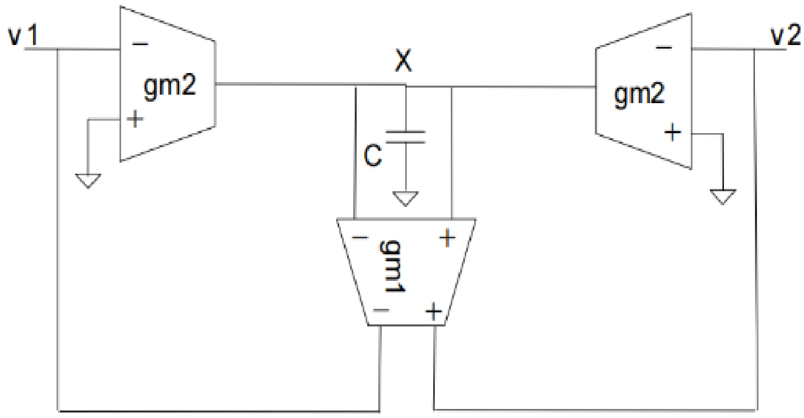
Curve 7. Attenuation characteristics for Chebyshev filter with 0.5 dB ripple.

The design process is as follows, from the table (refer to reference) as Rs/RL = 5.0. After frequency and impedance scaling, we get C1 = 466.5fF, L2 = 967.8nH, C3 = 1.004pF, L4 = 960.3nH. The equations are shown on the left:

$$C' = \frac{C}{R\omega} \qquad L' = \frac{RL}{\omega}$$

This provides us with a low pass Chebyshev type I filter with 0.5 ripple with a cutoff frequency at 245MHz, with my lower 3 dB frequency using a high-pass filter with a 150kHz, which uses a ac-coupled capacitor with a value of around 2nF.

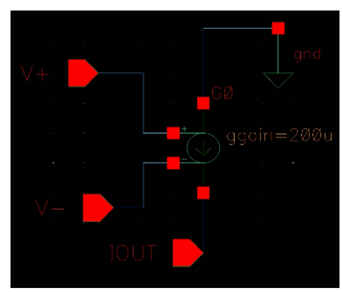
For the passive to active transformation, We only need to transform L2 and L4 using gm cells of 200uS.



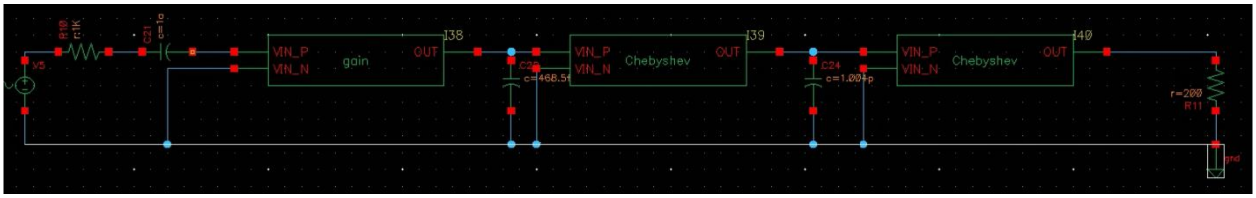
The equation is as follows:

$$C = gm^2 L$$

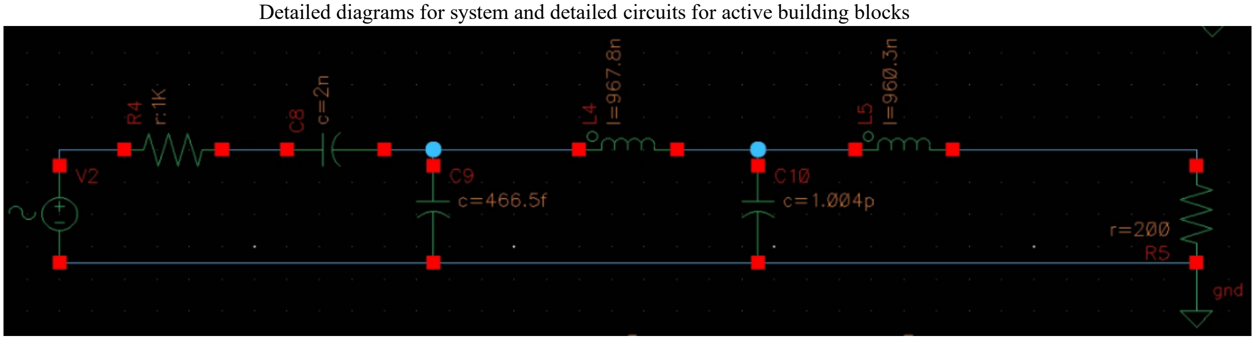
With the given topology on the left, we are able to transform series inductors into gm-c topology. Through the given equation, we are able to find the C values for both inductors, denoted by C2 and C4 as 38.7fF and 38.412fF respectively. Afterwards, as we decided to calculate the gain stage as 10, we used gm cells 1mS and 100uS as our gain stage gm cells, with the active resistor being $gm = \frac{1}{Rs}$. We are able to find Gm for active resistor being 1mS. We used ideal VCCS source to act as our gm cells as shown here.



2.2 Detailed diagrams

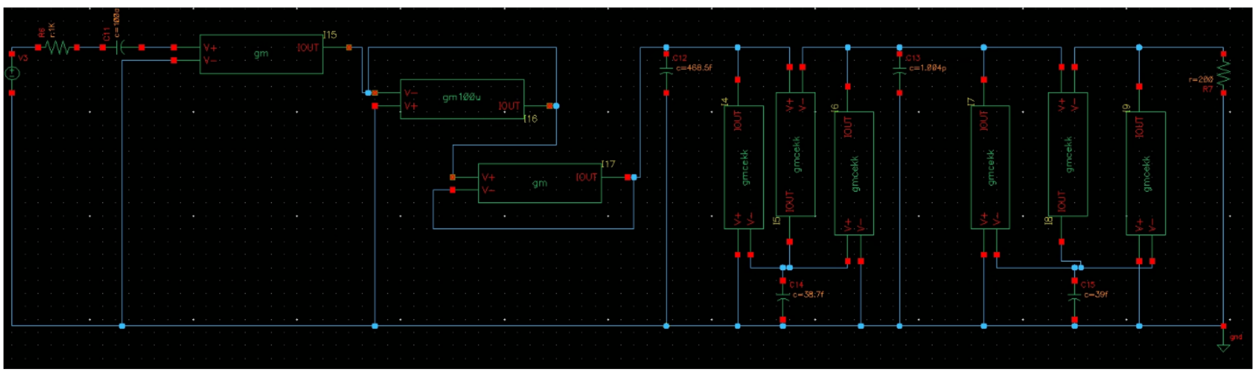


Detailed diagrams for system and detailed circuits for active building blocks

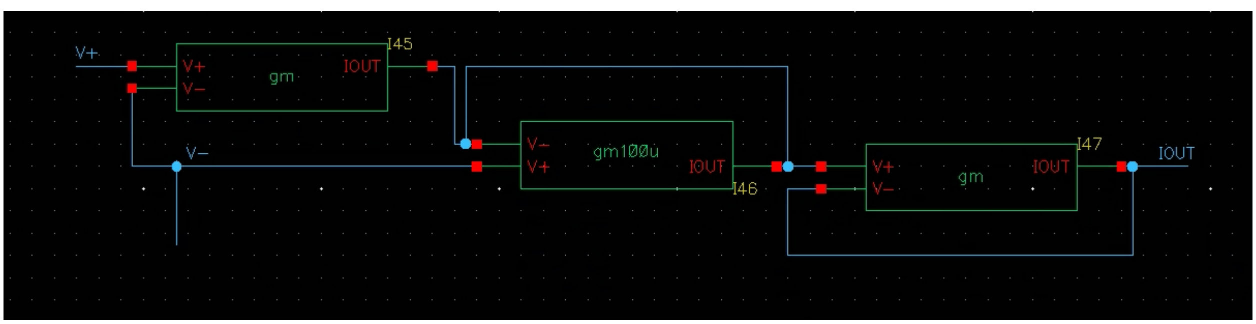


Passive filter schematic

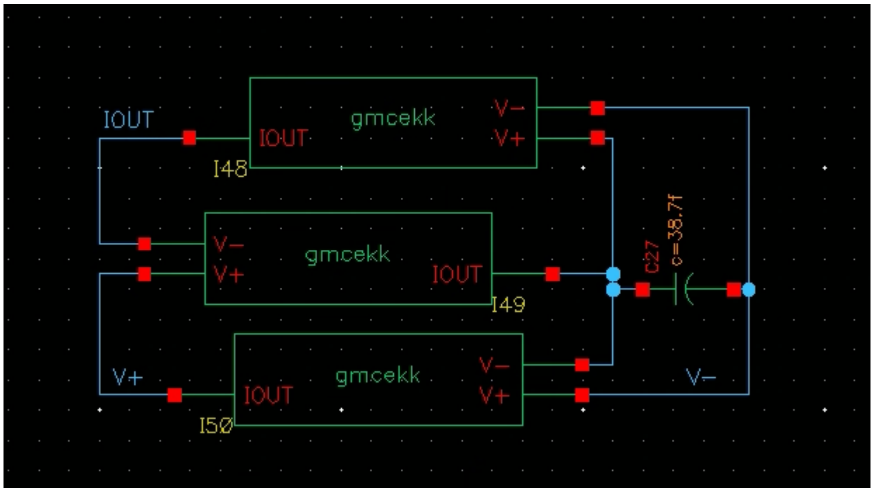
Overall Circuit Diagrams illustrates the overall system



Active filter schematic



Gain



Chebyshev

Simulations were conducted using Cadence. Key results include:

- Frequency response:
    - Lower -3 dB cutoff frequency is at 161kHz.
    - Higher -3 dB cut-off frequency is at 254.084MHz
    - Ripple is found at 0.762 difference between the highest and lowest points
    - Clock Frequency fs is around 10.4323MHz which is far lower than 200MHz
    - Lower corner channel attenuation is less than -90 dB which is ideal
    - Adjacent Channel attenuation is -25dB which is very ideal
    - Alternating Channel attenuation is -42.18dB
- Gain: 10dB

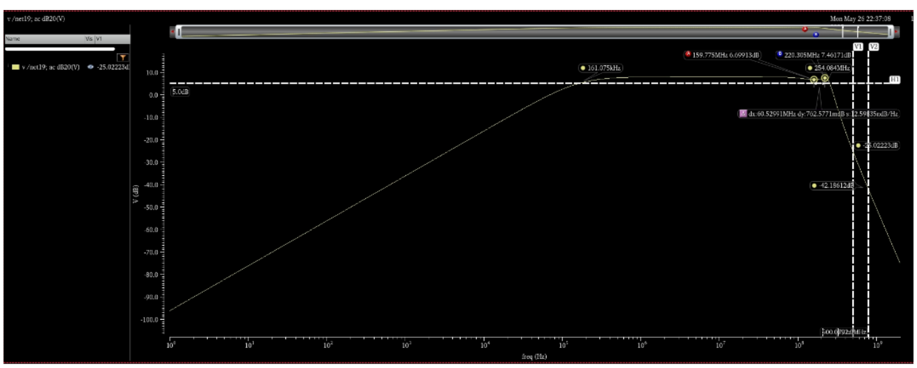


Figure 2: Frequency Response from Cadence Simulation

2.3 Discussion and Comparison

The target specifications required a cutoff frequency of 250M Hz and a passband ripple 0.5 dB. Calculated values predicted 245MHz as the hard cutoff, to provide it some margin for >250 -3 dB cutoff frequency, while simulations yielded 254MHz which is close to our estimates. Table 1 summarizes the comparison.

Table 1: Comparison of Specifications, Calculated, and Simulated Results

Parameter	Specification	Calculated	Simulated
Cutoff Frequency (Hz)	253 MHz -264 MHz	245MHz	254MHz
Passband Ripple (dB)	0.5dB	0.5dB	0.7dB
Gain (dB)	0-10	10	8

Discrepancies are further analyzed in Section 3.1.

3 Discussion

3.1 Effects of Non-Idealities

Including parasitic effects and gain stage non-idealities.

For our HPF capacitor, it usually has equivalent series resistance which will slightly damping the response.

It will also have parasitic capacitance, a parallel capacitance with Rs which will form a low pass effect. The effective resistance will drop due to interactions with gain stage.

Our low pass filter may contain inductor parasitics and capacitor parasitics which will cause a lower Q-factor which broadens the passband and reduces attenuation.

The biggest problem is the non linearity from the gm cells which will create harmonic distortions as the nonlinear terms generate harmonics of the input signals which are unwanted signals. The harmonic power may exceed our required 12dBc or 30dBc at higher frequencies due to these harmonics. Gain compression will also occur as nonlinearity will reduce the effective gm at higher input amplitudes due to saturation. Thus, as Vin increase, the gain will decrease from our simulated 8dB gain, which will greatly decrease the SNR and affects the dBc measurements. Our filter cutoffs will also be impacted, as it will alter the position of poles. Producing intermodulation distortion which will made a few frequency products being within the passband and pass unattenuated, which will be interferences. Higher-order products (e.g., 600 MHz) are attenuated by the LPF but still contribute to out-of-band emissions

To mitigate these, increasing LPF orders, improving linearity by using degeneration resistors were considered.

3.2 Problems Encountered and Solutions

Key challenges includes calculation from the lookup tables , which made the whole calculation process with frequency scaling and impedance scaling become extremely tedious. The textbook and lectures did not exactly cover the correct way to use these normalized values and thus required students to use other materials to obtain more information. This was resolved by resources from another course, calculators and online videos that gave thorough step by step process on designing a Chebyshev type I filter properly. Another issue was the HPF not working. At last, we found that the ac-coupled capacitor value needed to be extremely small to make it work, therefore we made it as small as possible, hence 1aF.This unfortunately cannot be explained through calculations as my calculations on the capacitor value was around 1-2nF, but it was far from correct.

4 Conclusion

4.1 Summary

In this project, we have learn how to design an active filter with specification. With the given frequency require, we need to balance filter characteristics with different trade off. Through iterative analysis, we deepened our understanding of analog filter design. Also with the difference between simulation and hand calculation . By analyzing the frequency response waveform and the calculation, we can find some difference between them, especially upper cut off frequency, shows us how to do careful tuning and validation at all frequency ranges. On top of that, using an ideal gm cell makes the simulation results more consistent with the hand calculation results, whereas considering non-idealities introduces many problems. In summary, this project provided a learning opportunity on analog filter design, from selecting and implementing a filter type and balancing design trade-offs. These insights will be invaluable for future analog filter designs, ensuring better alignment with specifications and improved robustness against practical challenges.

4.2 Possible Improvements

Future improvements could include transistor level design using actual op-amps to do the gm cells. Additionally, more advanced filter types for example elliptic filters could enhance performance. We can also design and simulate non-ideal case of filter design in the future which may include more tuning on frequency parameters and other components.

5 References

4	1.9841	0.9202	2.5864	1.3036	1.8258		
	2.0000	0.8452	2.7198	1.2383	1.9849		
	2.5000	0.5162	3.7659	0.8693	3.1205		
	3.3333	0.3440	5.1196	0.6208	4.4790		
	5.0000	0.2100	7.7076	0.3996	6.9874		
	10.0000	0.0975	15.3520	0.1940	14.2616		
	INF.	1.4361	1.8888	1.6211	0.9129		

Table for normalized values (Chebyshev type I 0.5 dB ripple) N = 4

[1] A. I. Zverev, Handbook of Filter Synthesis, Wiley, New York, NY, USA, 1967.

B Individual Contributions

- Lo Evan Hong Tik: design ,calculation, simulation and report
- Chio yat hei : design ,calculation, simulation and report
- Hsu Yung Hsiang: design ,calculation, simulation and report