FPGA_Zynq 瑕疵檢測應用

Kria KV260 Vision AI Starter Kit

大綱

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硬體說明

K26 SOM 概述
基於 Zynq® UltraScale+™ MPSoC 架構

77 x 60 x 11mm

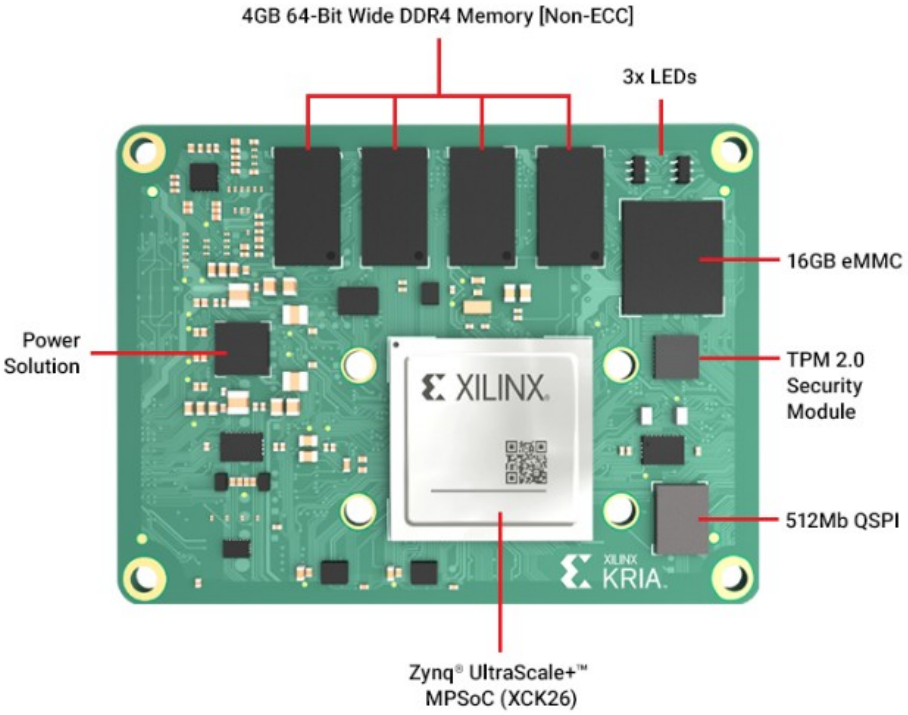
運算能力

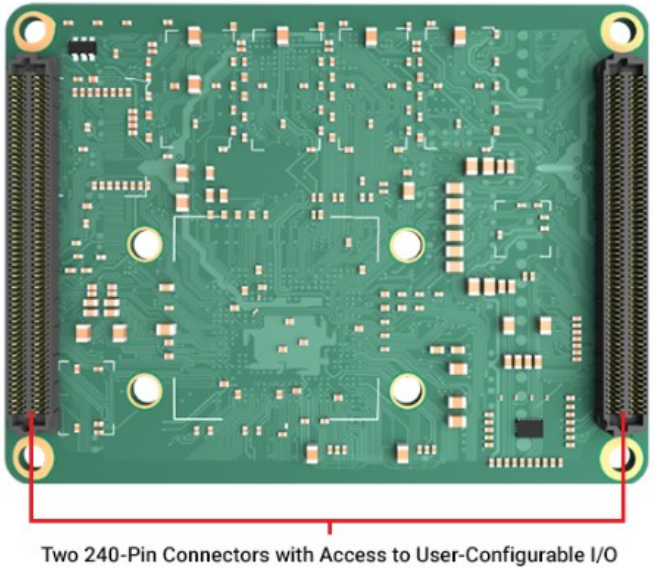
Arm®	256K	1.4 TOPS	4K60p
四核心子系統	系統邏輯單元	AI 處理效能	H.264/265 視訊轉碼器

介面

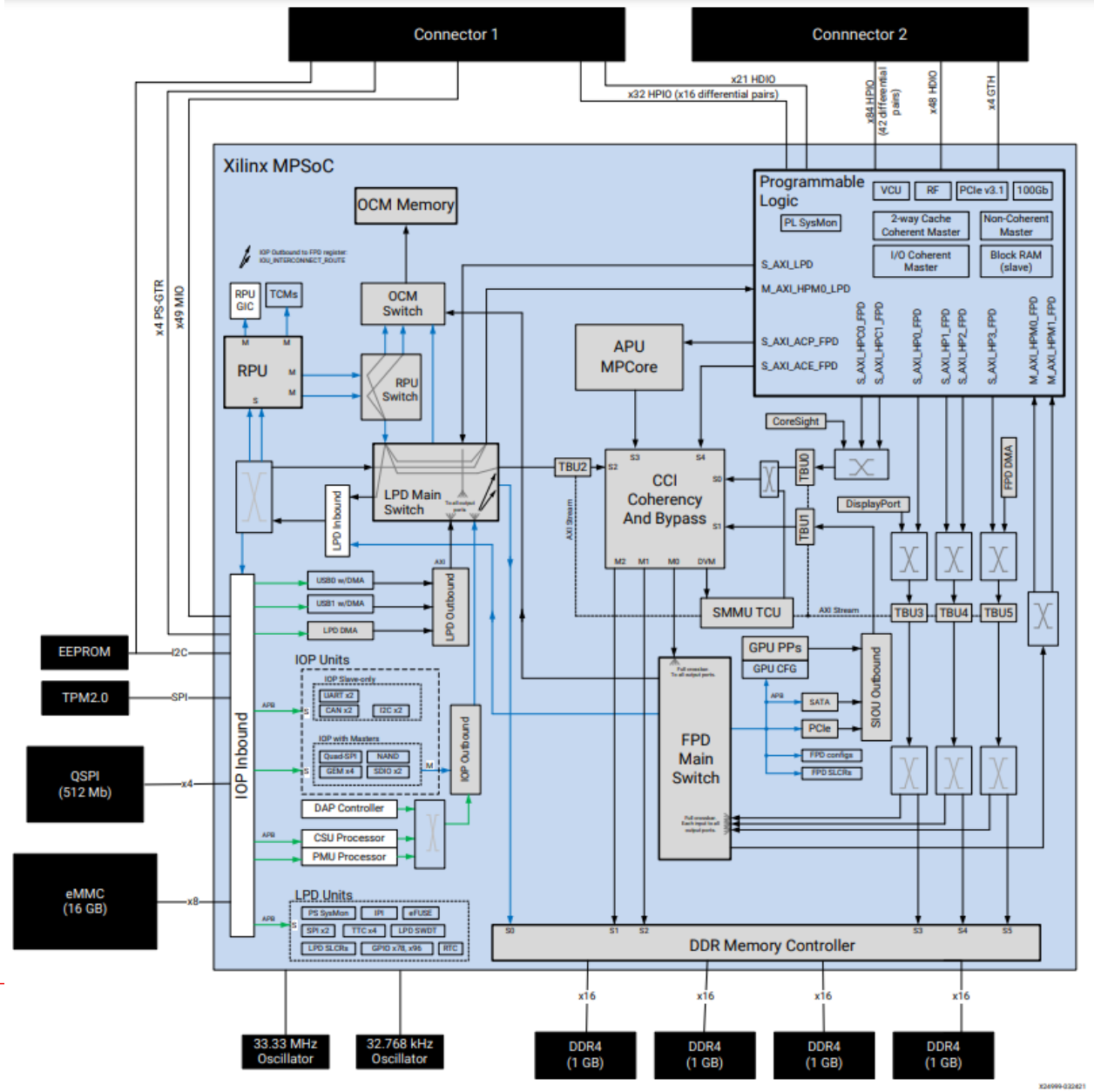
245 個 I/O	15 台攝影機	40G 乙太網路	4x USB	4GB
雙 240 針腳連接器	混合 MIPI、sub-LVDS、SLVS-EC	透過 4x 10G 提供 1Gb 到 40Gb	混合USB 2.0 和 3.0	64 位元 DDR4 記憶體

硬體說明(續)

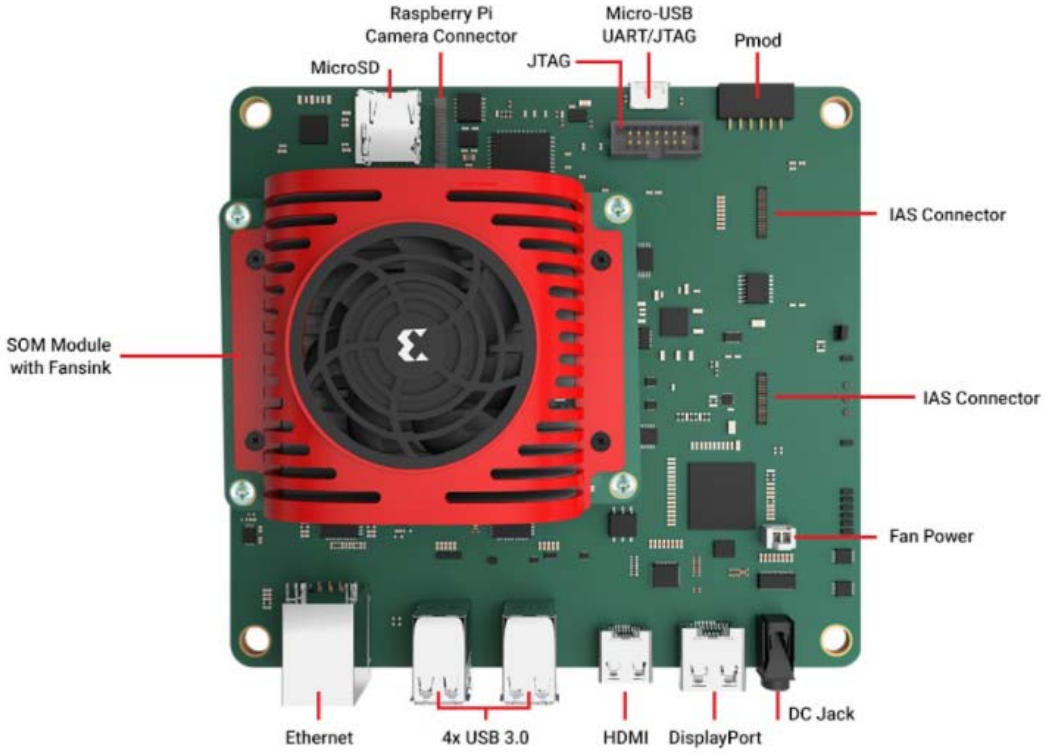

4GB 64-Bit Wide DDR4 Memory [Non-ECC]
3x LEDs
16GB eMMC
Power Solution
TPM 2.0 Security Module
512Mb QSPI
XILINX
KRIA
Zynq® UltraScale+™ MPSoC (XCK26)

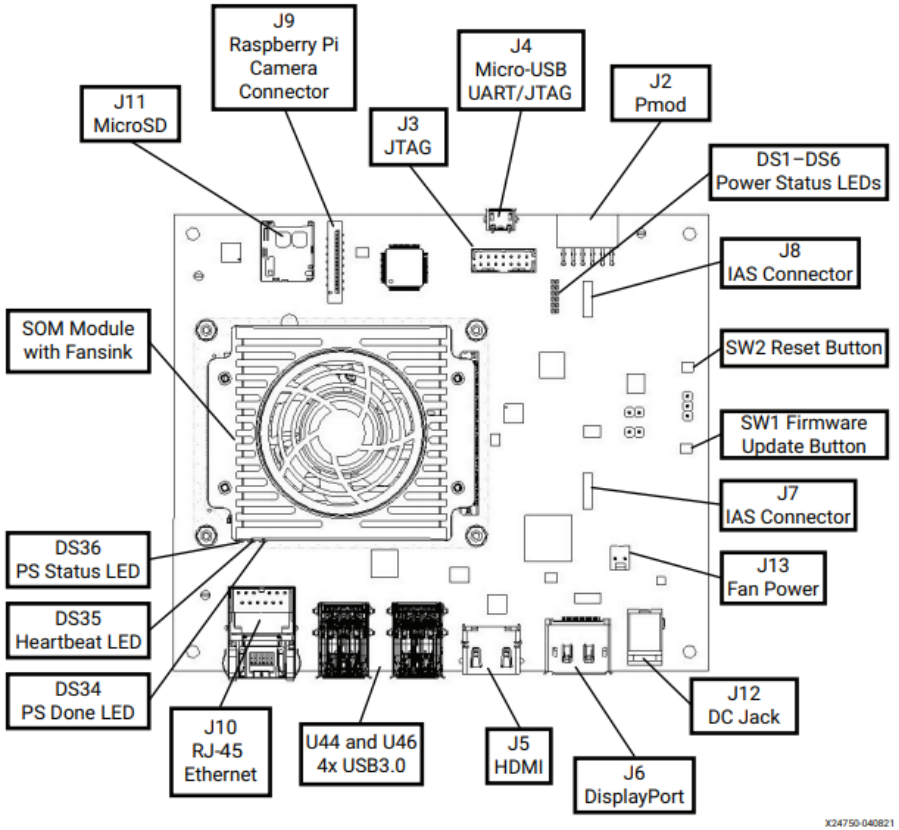

Two 240-Pin Connectors with Access to User-Configurable I/O

硬體說明(續)

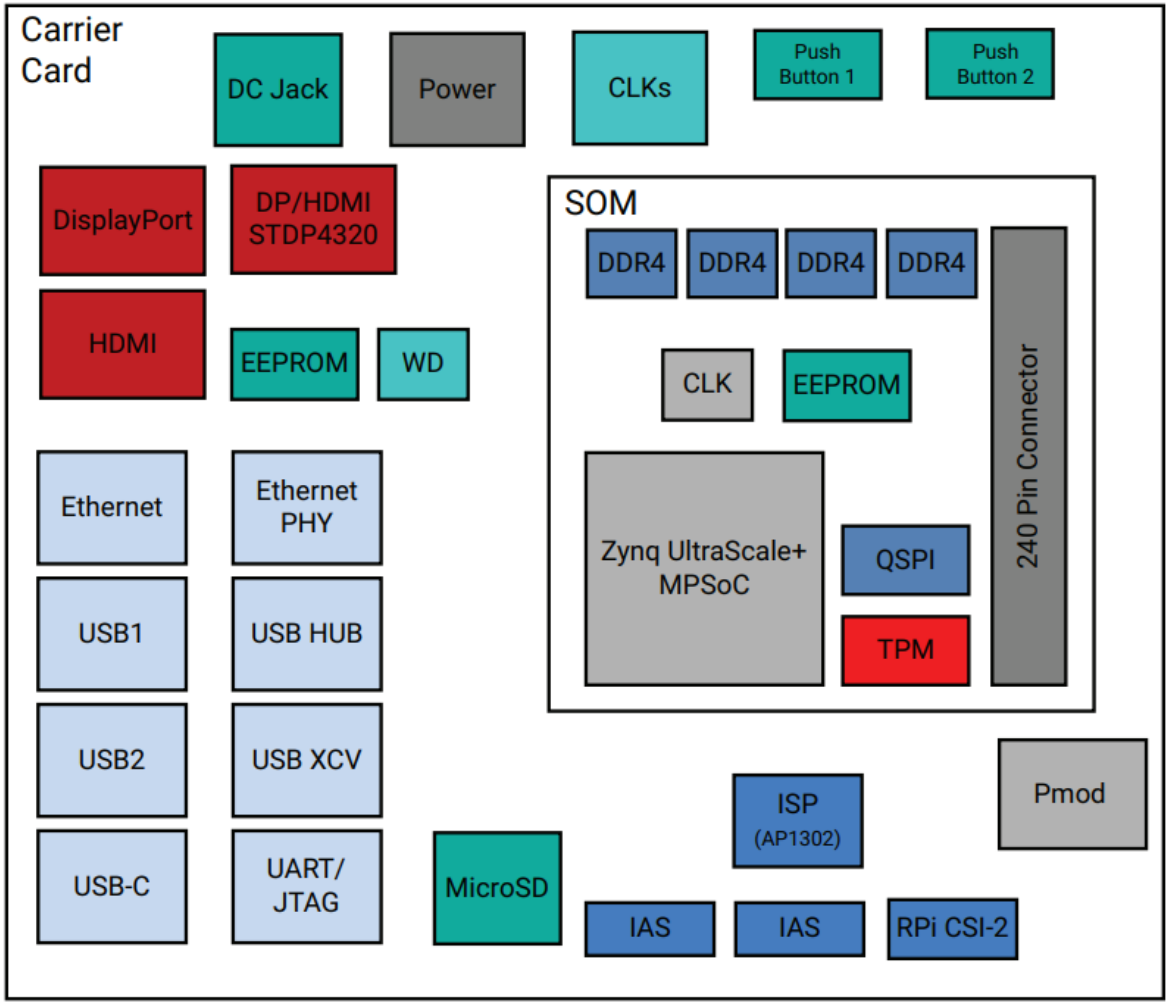

Connector 1
Connnector 2
x21 HDIO
x32 HPIO (x16 differential pairs)
x84 HPIO (42 differential pairs)
x48 HDIO
x4 GTH
Xilinx MPSoC
OCM Memory
Programmable Logic
VCU
RF
PCIe v3.1
100Gb
PL SysMon
2-way Cache Coherent Master
Non-Coherent Master
I/O Coherent Master
Block RAM (slave)
S_AXI_LPD
M_AXI_HPM0_LPD
S_AXI_ACP_FPD
S_AXI_ACE_FPD
RPU GIC
TCMs
OCM Switch
RPU
RPU Switch
APU MPCore
CoreSight
LPD Main Switch
LPD Inbound
TBU2
CCI Coherency And Bypass
TBU0
TBU1
DisplayPort
FPD DMA
SMMU TCU
TBU3
TBU4
TBU5
GPU PPs
GPU CFG
SIOU Outbound
FPD Main Switch
SATA
PCIe
FPD configs
FPD SLCRs
USB0 w/DMA
USB1 w/DMA
LPD DMA
LPD Outbound
IOP Units
IOP Inbound
IOP Outbound
DAP Controller
CSU Processor
PMU Processor
LPD Units
DDR Memory Controller
x4 PS-GTR
x49 MIO
EEPROM
I2C
TPM2.0
SPI
QSPI (512 Mb)
x4
eMMC (16 GB)
x8
33.33 MHz Oscillator
32.768 kHz Oscillator
x16
DDR4 (1 GB)
DDR4 (1 GB)
DDR4 (1 GB)
DDR4 (1 GB)

硬體說明(續)


Raspberry Pi
Camera Connector
Micro-USB
UART/JTAG
Pmod
MicroSD
JTAG
IAS Connector
SOM Module
with Fansink
IAS Connector
Fan Power
Ethernet
4x USB 3.0
HDMI
DisplayPort
DC Jack


J9
Raspberry Pi
Camera
Connector
J4
Micro-USB
UART/JTAG
J2
Pmod
J11
MicroSD
J3
JTAG
DS1–DS6
Power Status LEDs
J8
IAS Connector
SOM Module
with Fansink
SW2 Reset Button
SW1 Firmware
Update Button
J7
IAS Connector
DS36
PS Status LED
J13
Fan Power
DS35
Heartbeat LED
DS34
PS Done LED
J12
DC Jack
J10
RJ-45
Ethernet
U44 and U46
4x USB3.0
J5
HDMI
J6
DisplayPort
X24750-040821

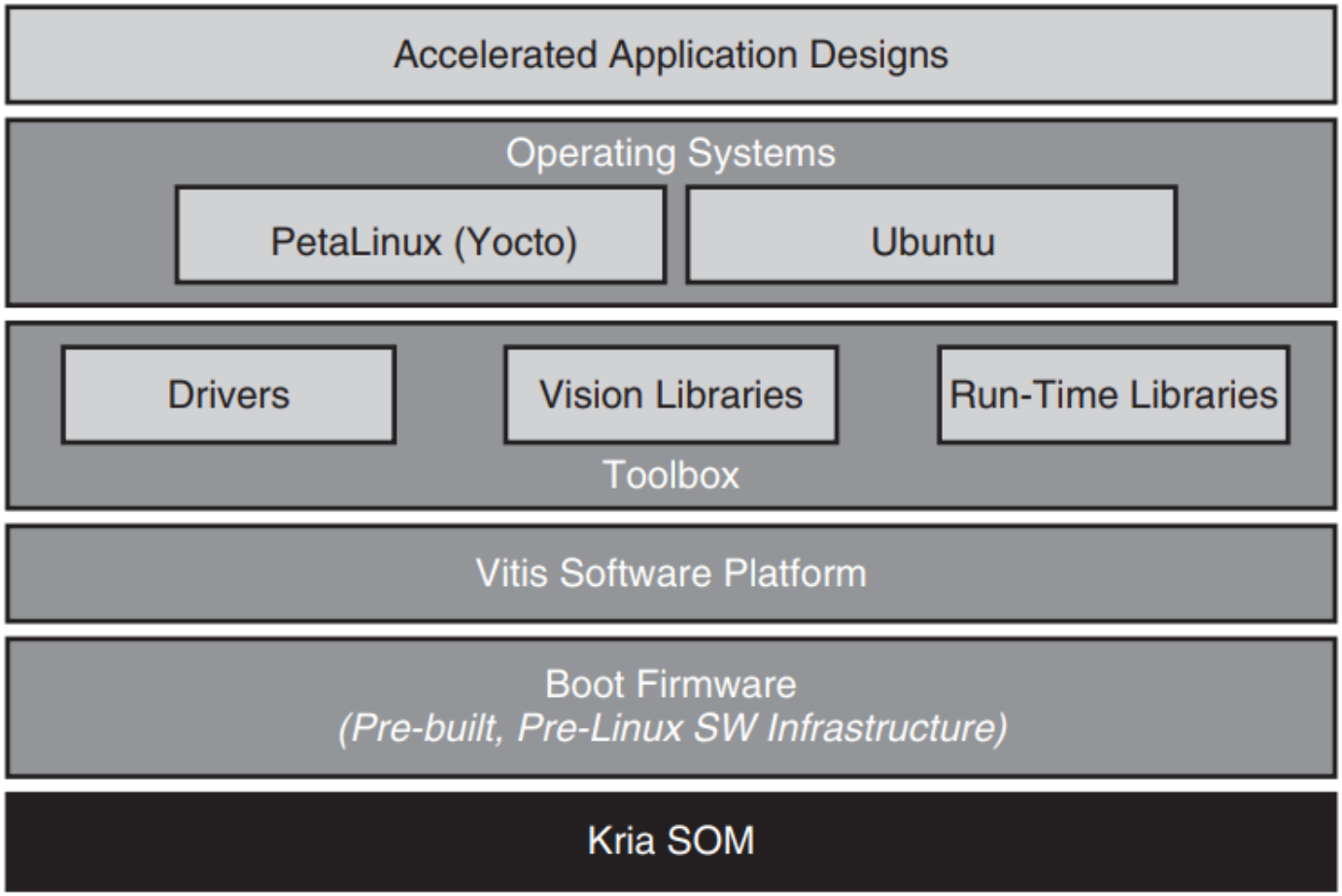
硬體說明(續)



X24612-040621

- 元件：Kria K26 SOM、載卡、散熱解決方案
- FPGA晶片：Kria K26 SOM採用Zynq UltraScale+ MPSoC
- 中央處理器：應用處理器64位元4核心Arm Cortex-A53、即時處理器32位元雙核心Arm Cortex-R5F、繪圖處理器Arm Mali-400MP2、Infineon 2.0
- 可程式化邏輯：系統邏輯單元256,000個，DSP切片為1,248個
- 記憶體：4 GB DDR
- 儲存空間：16GB eMMC
- 網路介面：GbE埠
- 顯示介面：HDMI 1.4、DisplayPort 1.2a
- 連接介面： 4個USB 3.0
- 耗電：7.5瓦，最大為15瓦

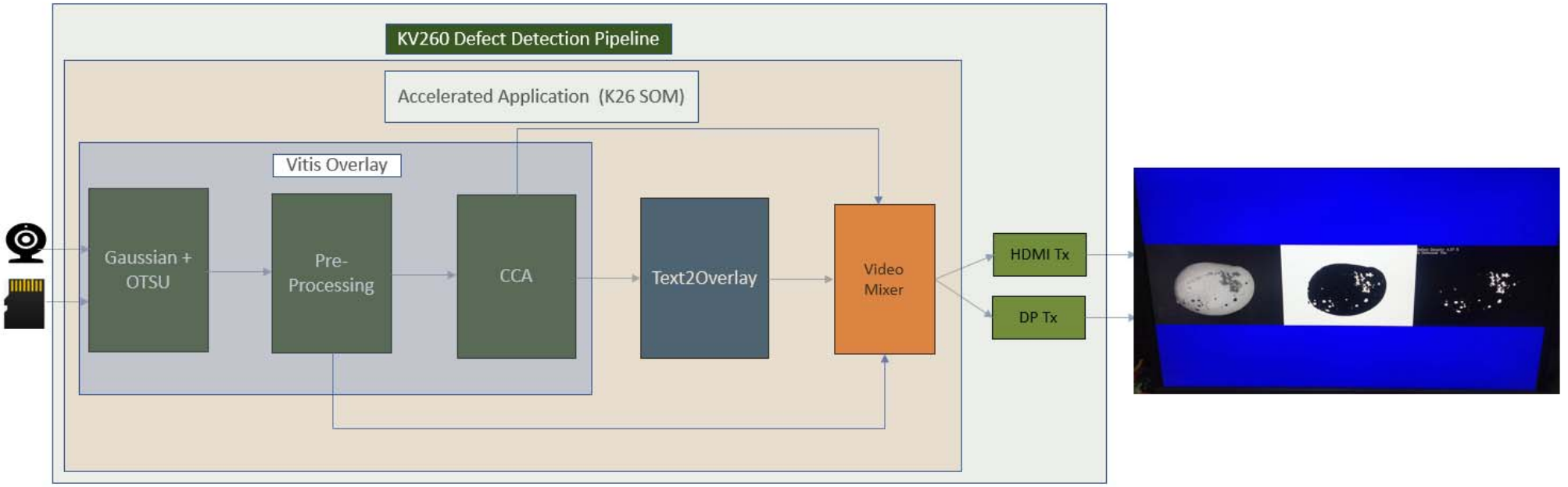
系統架構說明


Accelerated Application Designs
Operating Systems
PetaLinux (Yocto)
Ubuntu
Drivers
Vision Libraries
Run-Time Libraries
Toolbox
Vitis Software Platform
Boot Firmware
(Pre-built, Pre-Linux SW Infrastructure)
Kria SOM
WP528_2_041521

應用案例說明

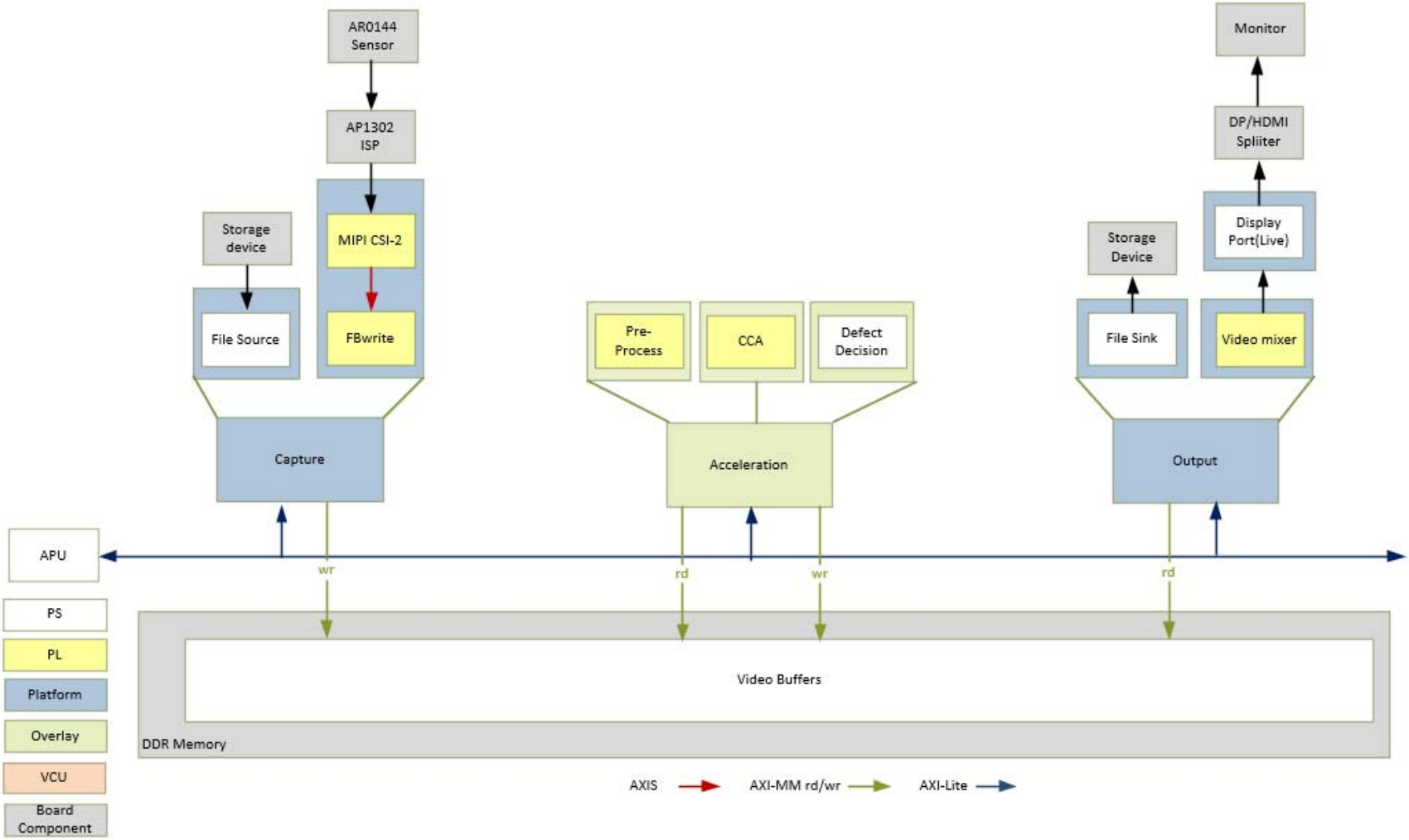
Defect Detect

The Defect Detection accelerated application is a machine vision application that automates detection of defects in mangoes and sorting in high-speed factory pipelines by using computer vision library functions.

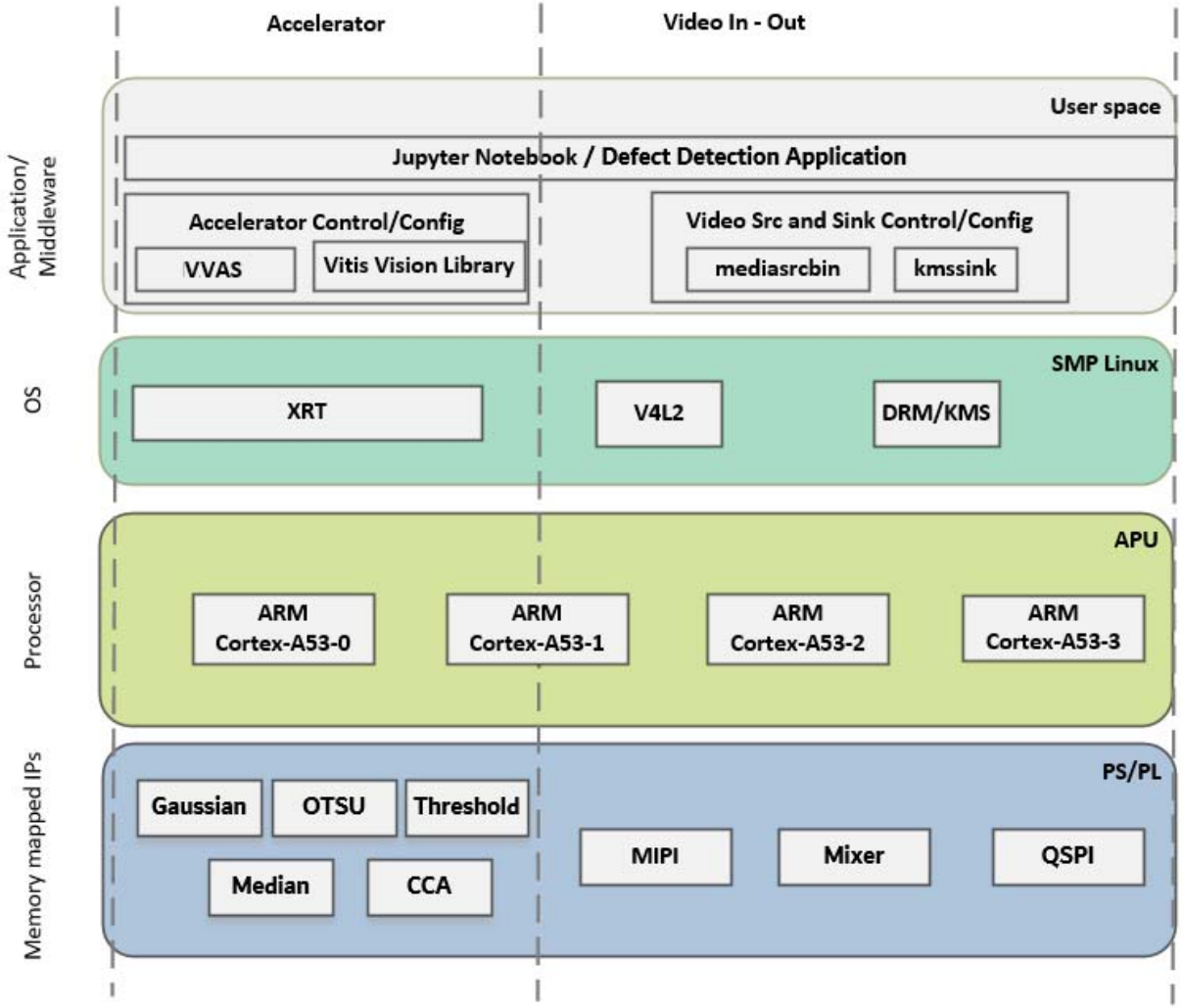


應用案例說明(續)

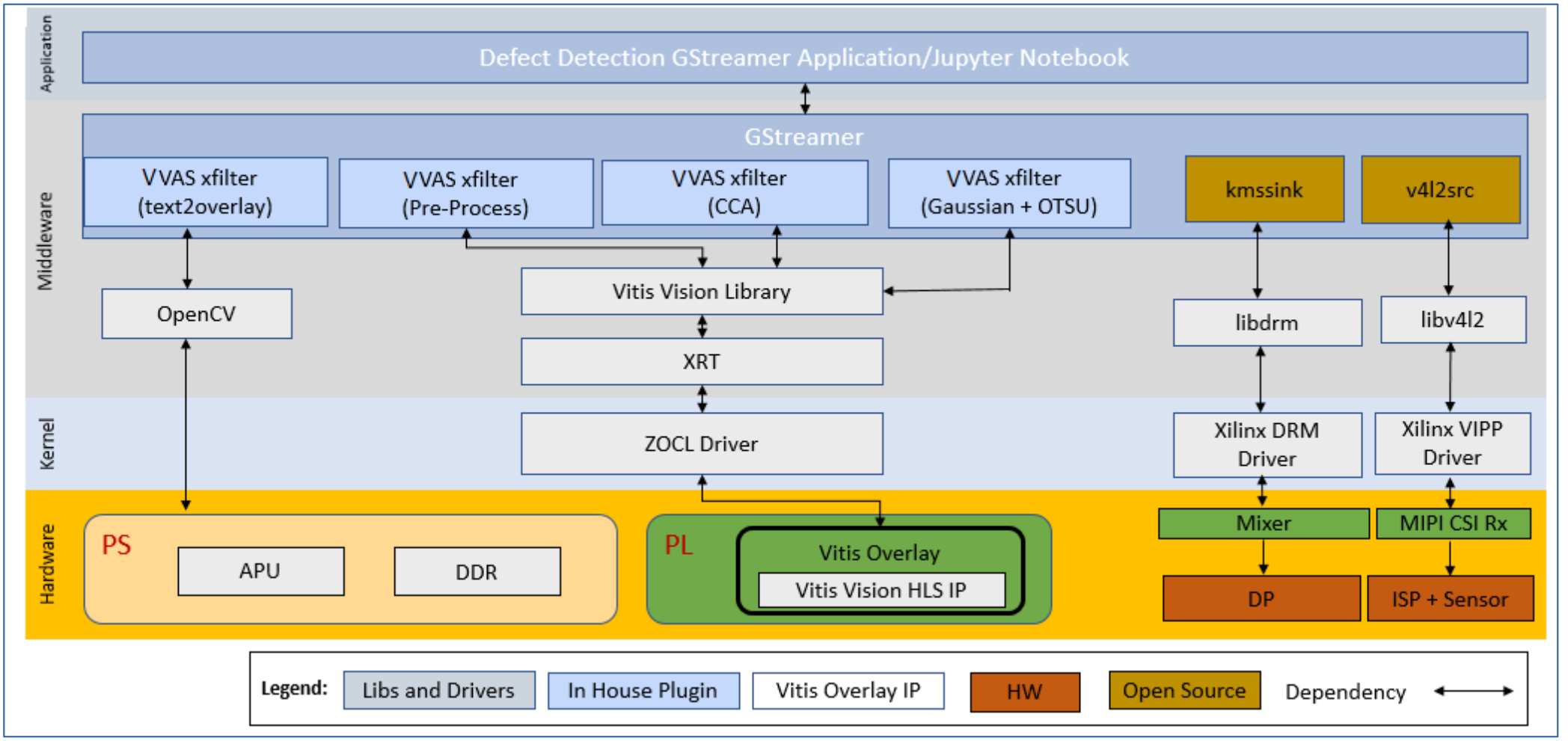
檢測流程


AR0144 Sensor
AP1302 ISP
MIPI CSI-2
FBwrite
Storage device
File Source
Capture
Pre-Process
CCA
Defect Decision
Acceleration
Monitor
DP/HDMI Spliiter
Display Port(Live)
Storage Device
File Sink
Video mixer
Output
APU
wr
rd
wr
rd
PS
PL
Platform
Overlay
VCU
Board Component
Video Buffers
DDR Memory
AXIS
AXI-MM rd/wr
AXI-Lite

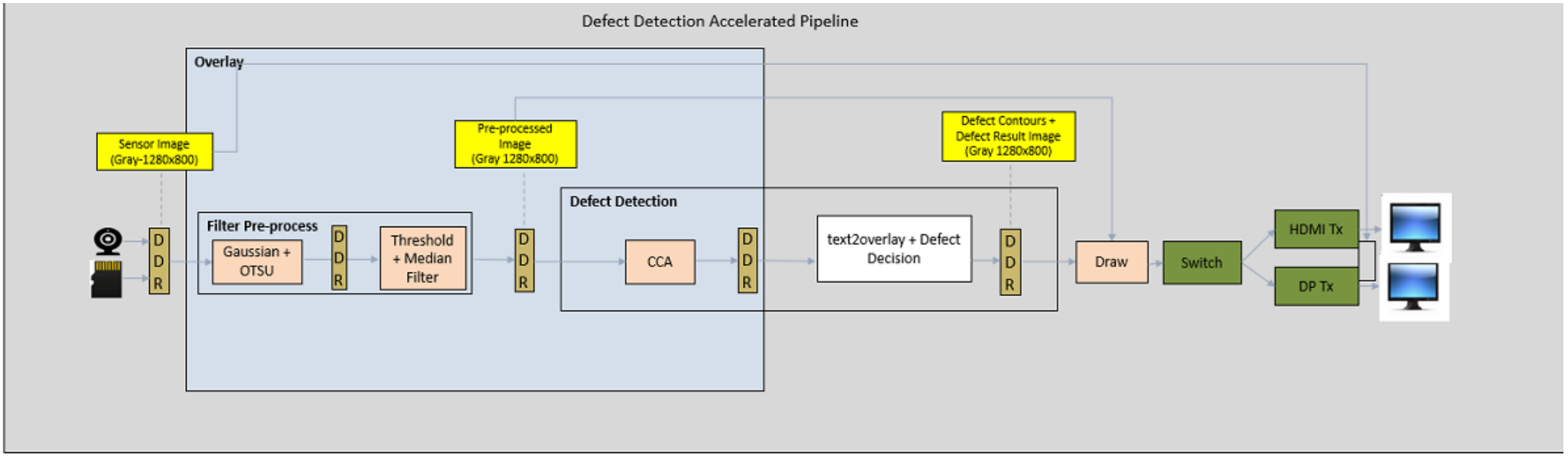
系統架構


Accelerator
Video In - Out
Application/ Middleware
User space
Jupyter Notebook / Defect Detection Application
Accelerator Control/Config
VVAS
Vitis Vision Library
Video Src and Sink Control/Config
mediasrcbin
kmssink
OS
SMP Linux
XRT
V4L2
DRM/KMS
Processor
APU
ARM Cortex-A53-0
ARM Cortex-A53-1
ARM Cortex-A53-2
ARM Cortex-A53-3
Memory mapped IPs
PS/PL
Gaussian
OTSU
Threshold
Median
CCA
MIPI
Mixer
QSPI

平台軟體架構


Application
Defect Detection GStreamer Application/Jupyter Notebook
Middleware
GStreamer
VVAS xfilter (text2overlay)
VVAS xfilter (Pre-Process)
VVAS xfilter (CCA)
VVAS xfilter (Gaussian + OTSU)
kmssink
v4l2src
OpenCV
Vitis Vision Library
XRT
libdrm
libv4l2
Kernel
ZOCL Driver
Xilinx DRM Driver
Xilinx VIPP Driver
Hardware
PS
APU
DDR
PL
Vitis Overlay
Vitis Vision HLS IP
Mixer
MIPI CSI Rx
DP
ISP + Sensor
Legend:
Libs and Drivers
In House Plugin
Vitis Overlay IP
HW
Open Source
Dependency

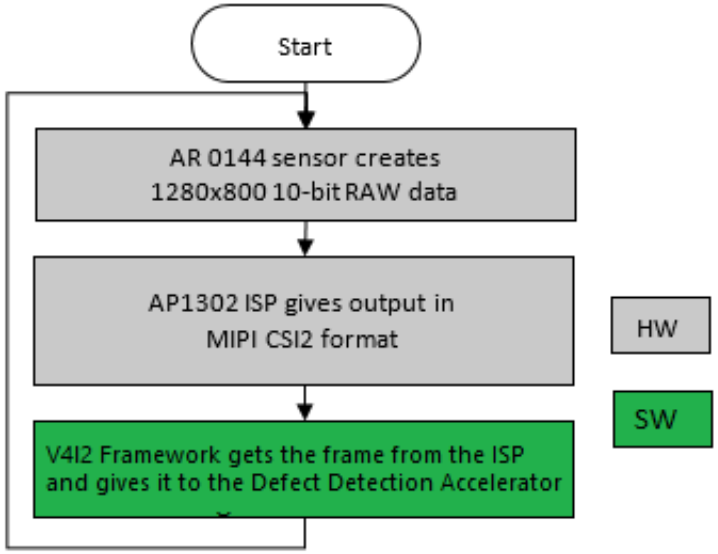
加速器之軟體架構

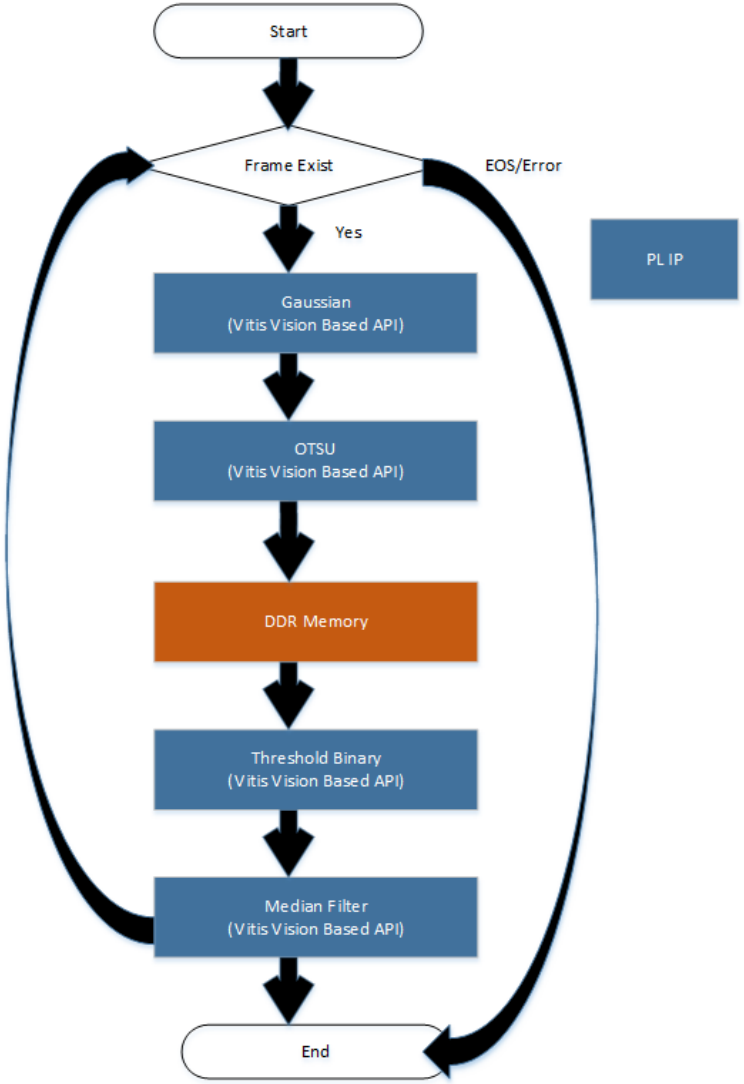


▼ The following table lists the Component types used in the application.

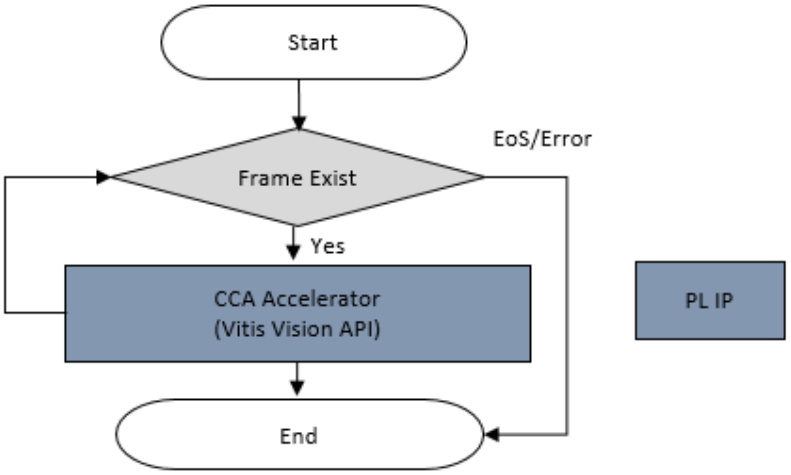
Pipeline	Component	Component Type
Pre-Process	Gaussian + OTSU Accelerator	PL
	Threshold + Median Filter	PL
Defect Decision	CCA	PL
	Text2Overlay + Defect Decision	SW

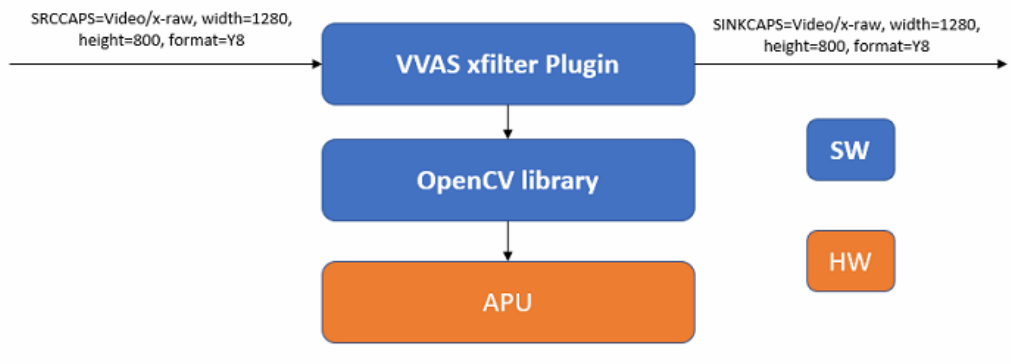
加速器之軟體架構(續)

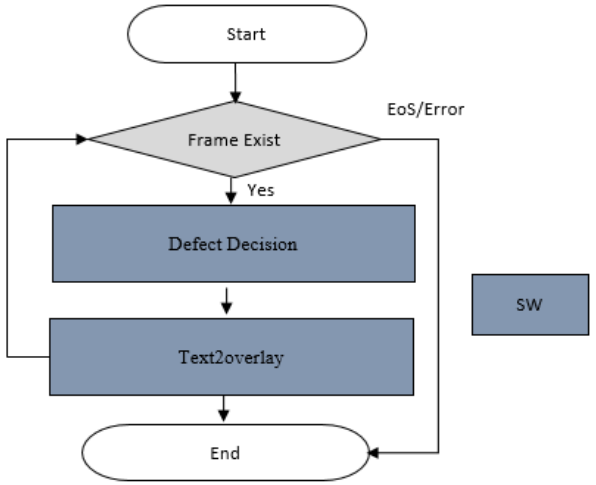

Start
AR 0144 sensor creates
1280x800 10-bit RAW data
AP1302 ISP gives output in
MIPI CSI2 format
V4I2 Framework gets the frame from the ISP
and gives it to the Defect Detection Accelerator
HW
SW


Start
Frame Exist
EOS/Error
Yes
PL IP
Gaussian
(Vitis Vision Based API)
OTSU
(Vitis Vision Based API)
DDR Memory
Threshold Binary
(Vitis Vision Based API)
Median Filter
(Vitis Vision Based API)
End

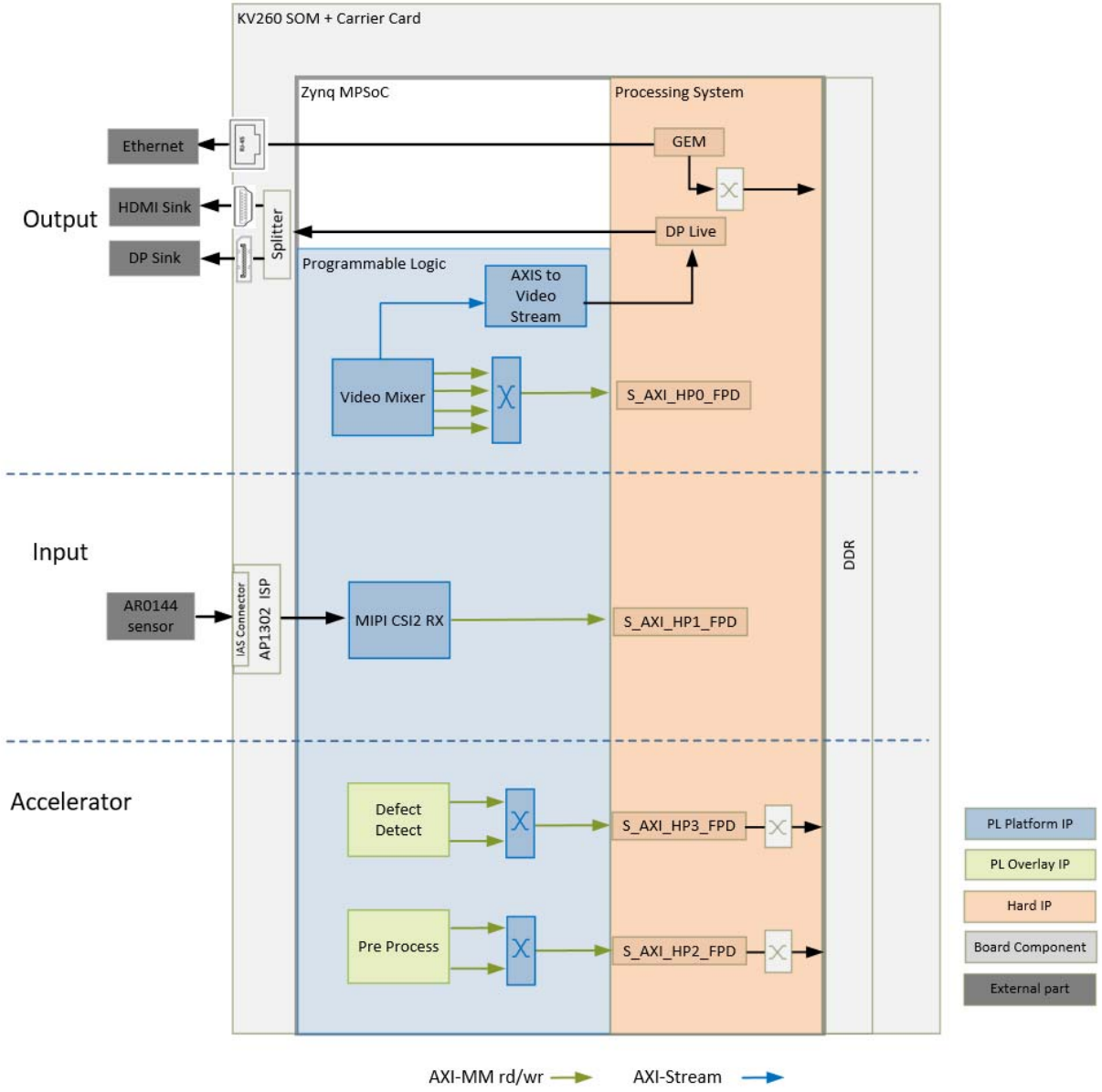
加速器之軟體架構(續)


Start
Frame Exist
EoS/Error
Yes
CCA Accelerator
(Vitis Vision API)
End
PL IP

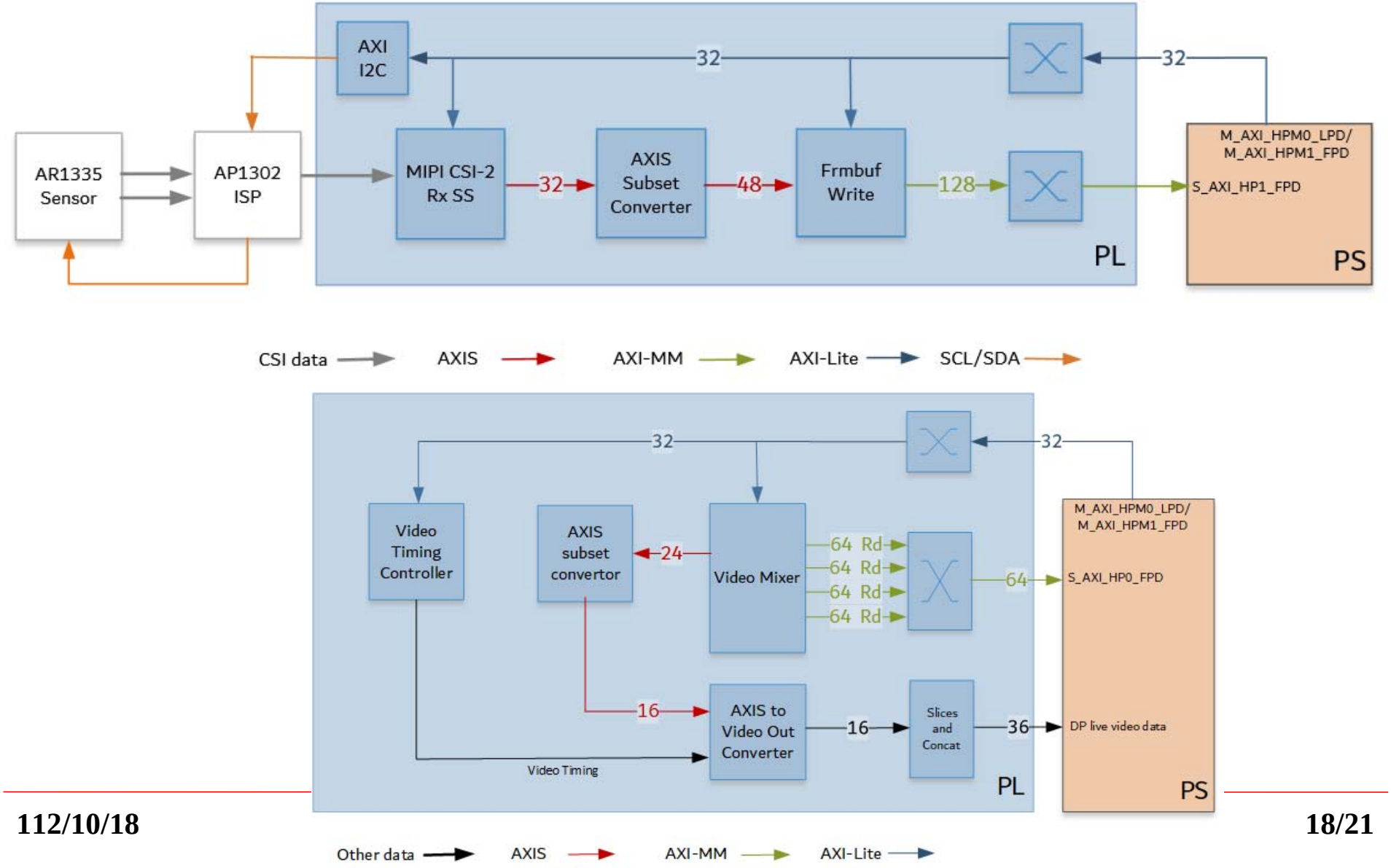

SRCCAPS=Video/x-raw, width=1280, height=800, format=Y8
VVAS xfilter Plugin
SINKCAPS=Video/x-raw, width=1280, height=800, format=Y8
OpenCV library
APU
SW
HW


Start
Frame Exist
EoS/Error
Yes
Defect Decision
Text2overlay
End
SW

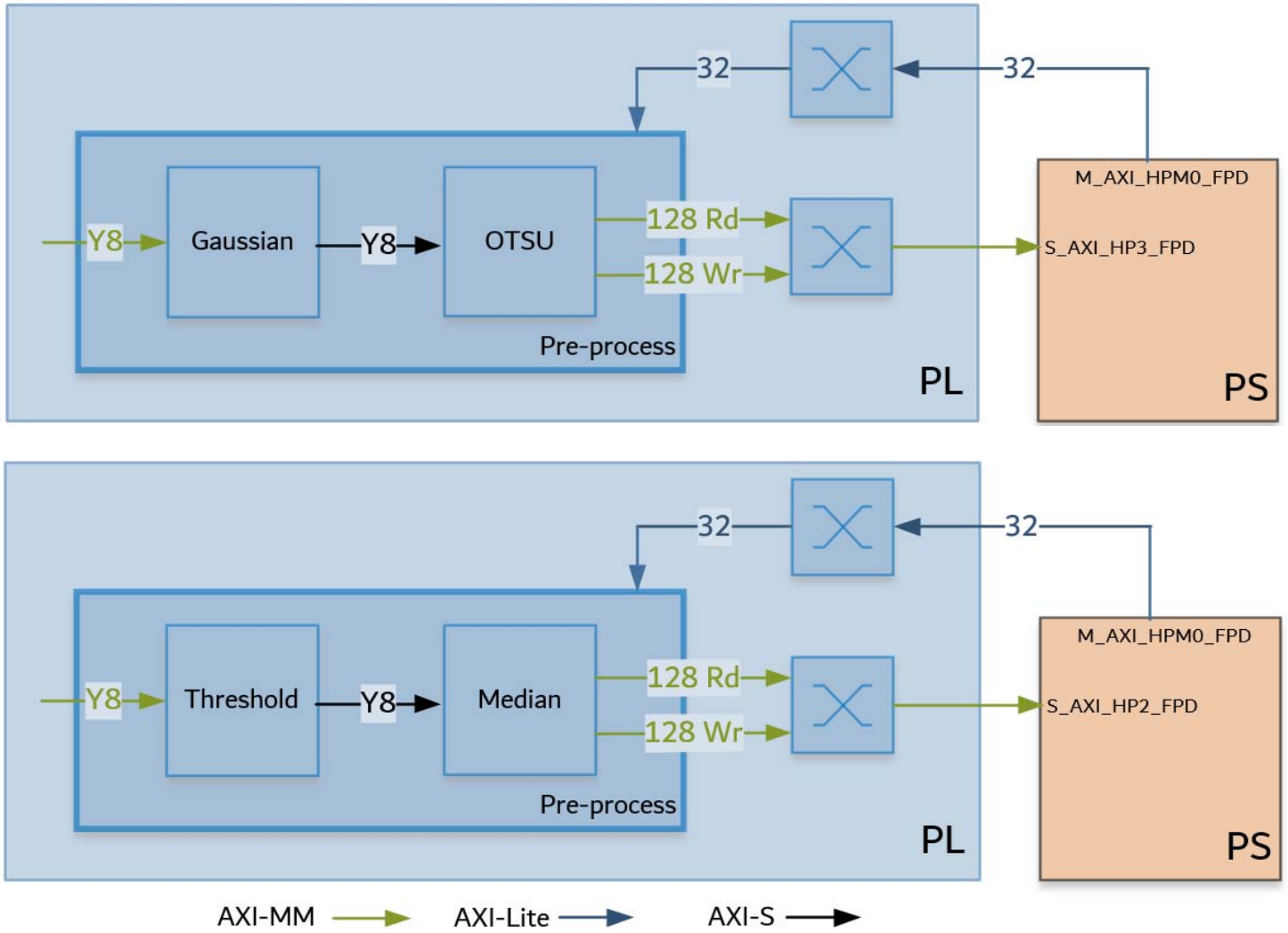
平台硬體架構


KV260 SOM + Carrier Card
Zynq MPSoC
Processing System
Ethernet
GEM
Output
HDMI Sink
Splitter
DP Live
DP Sink
Programmable Logic
AXIS to Video Stream
Video Mixer
S_AXI_HP0_FPD
Input
AR0144 sensor
IAS Connector
AP1302 ISP
MIPI CSI2 RX
S_AXI_HP1_FPD
DDR
Accelerator
Defect Detect
S_AXI_HP3_FPD
Pre Process
S_AXI_HP2_FPD
PL Platform IP
PL Overlay IP
Hard IP
Board Component
External part
AXI-MM rd/wr
AXI-Stream

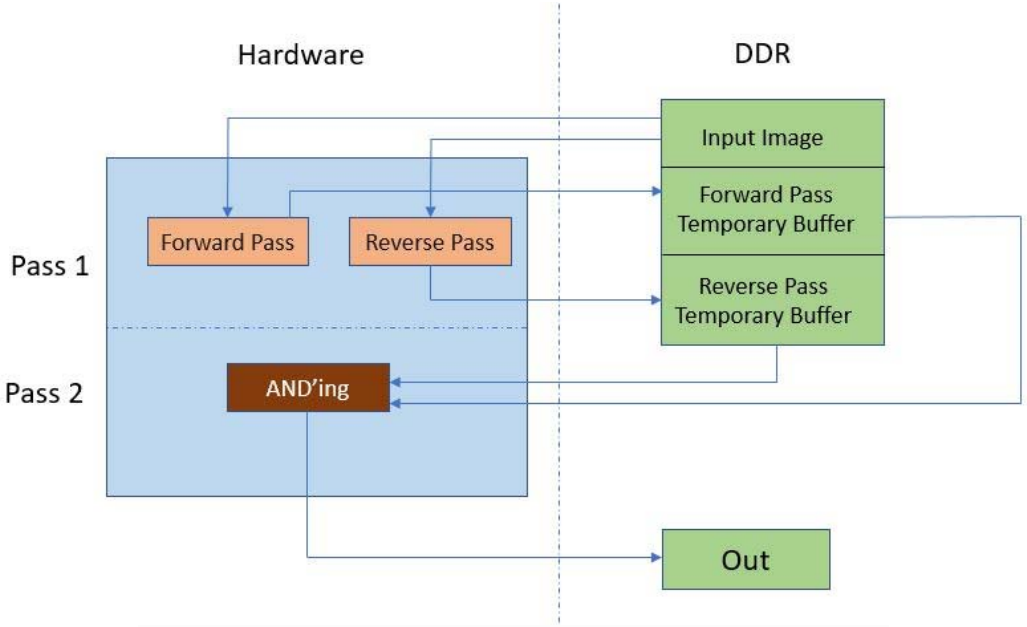
平台硬體架構(續)


AXI I2C
32
32
AR1335 Sensor
AP1302 ISP
MIPI CSI-2 Rx SS
32
AXIS Subset Converter
48
Frmbuf Write
128
M_AXI_HPM0_LPD/ M_AXI_HPM1_FPD
S_AXI_HP1_FPD
PL
PS
CSI data
AXIS
AXI-MM
AXI-Lite
SCL/SDA
32
32
Video Timing Controller
AXIS subset convertor
24
Video Mixer
64 Rd
64 Rd
64 Rd
64 Rd
64
M_AXI_HPM0_LPD/ M_AXI_HPM1_FPD
S_AXI_HP0_FPD
16
AXIS to Video Out Converter
16
Slices and Concat
36
DP live video data
Video Timing
PL
PS
Other data
AXIS
AXI-MM
AXI-Lite

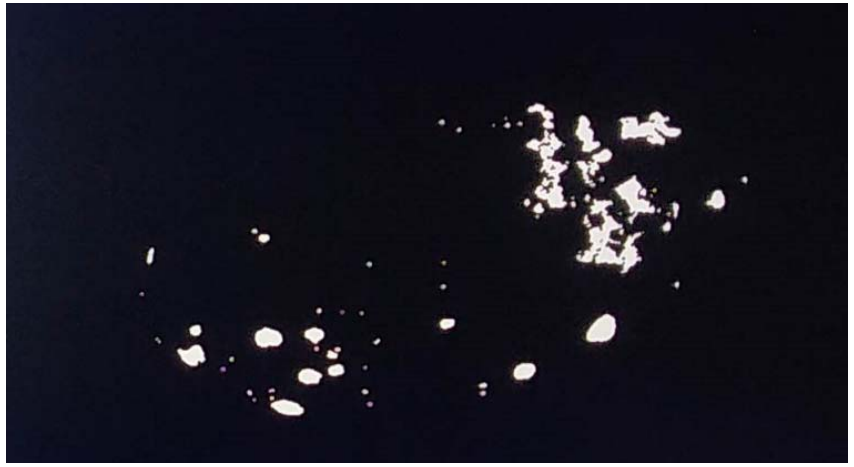
加速器之硬體架構


32
32
Y8
Gaussian
Y8
OTSU
128 Rd
128 Wr
Pre-process
PL
M_AXI_HPM0_FPD
S_AXI_HP3_FPD
PS
32
32
Y8
Threshold
Y8
Median
128 Rd
128 Wr
Pre-process
PL
M_AXI_HPM0_FPD
S_AXI_HP2_FPD
PS
AXI-MM
AXI-Lite
AXI-S

加速器之硬體架構(續)



K26	CLB LUTs	BRAM	DSP	URAM
Available	117120	144	1248	64
Platform	22646	18	30	1
Gaussian_OTSU	13633	6	71	0
Pre-processing	5244	3.5	9	0
CCA	13756	5	10	0
Other*	6062	39	0	0
Total	61341	71.5	120	1
Total %	52.37%	49.65%	9.05%	1.56%



程式碼範例

Deliveries	Type	Definition
libvvas_otsu.so	Kernel Library	Vitis Vision library for the Gaussian + OTSU detector. Preserves edges while smoothening and calculates the optimum threshold between foreground and background pixels.
libvvas_preprocess.so	Kernel Library	Vitis Vision library to filter and remove the salt and pepper noise for defect detection.
libvvas_cca.so	Kernel Library	Vitis Vision library to determine the defective pixels in the image.
libvvas_text2overlay.so	Kernel Library	*OpenCV* software library to calculate the defect density, determine the quality of the mango, and embed text as result into output images.
defect-detect	Application Executable	Executable to invoke the whole application with options to choose a source, width, height, framerate, configuration file path, and other parameters.

Vitis_Libraries / vision / L1 / examples / ccacustom / xf_cca_custom_config.h

Code | Blame | 40 lines (35 loc) · 1.28 KB

```
17  #ifndef __XF_VITIS_CCA_CUSTOM_CONFIG_H__
18  #define __XF_VITIS_CCA_CUSTOM_CONFIG_H__
19
20  #include "ap_int.h"
21  #include "common/xf_common.hpp"
22  #include "common/xf_utility.hpp"
23  #include "hls_stream.h"
24  #include "imgproc/xf_cca_custom.hpp"
25
26  /* config width and height */
27  constexpr int WIDTH = 3840;
28  constexpr int HEIGHT = 2160;
29
30  void cca_custom_accel(uint8_t* in_ptr1,
31                        uint8_t* in_ptr2,
32                        uint8_t* tmp_out_ptr1,
33                        uint8_t* tmp_out_ptr2,
34                        uint8_t* out_ptr,
35                        int* obj_pix,
36                        int* def_pix,
37                        int height,
38                        int width);
39
40  #endif // __XF_VITIS_CCA_CUSTOM_CONFIG_H__
```