**Mega Prelab**

A hard copy of this Mega Prelab is required to be turned in. Answers should not be handwritten. The timing diagram may be NEATLY drawn by hand with the assistance of a straightedge on engineering paper.

| **Name** | **Pin #** | **Type** | **PxDIR** | **PxREN** | **PxOUT** |
| --- | --- | --- | --- | --- | --- |
| GND | 20 | Power | - | - | - |
| RST | 8 | Output | 1 | 0 | 1 |
| P1.4 | 6 | Output | 1 | 0 | 1 |
| MOSI | 15 | Output | 1 | 0 | 1 |
| SCLK | 7 | Output | 1 | 0 | 1 |
| VCC | 1 | power | - | - | - |
| S1 | 9 | input | 0 | 1 | 1 |
| S2 | 10 | input | 0 | 1 | 1 |
| S3 | 11 | input | 0 | 1 | 1 |
| S4 | 12 | input | 0 | 1 | 1 |

| **Mystery Label** | **Register** |
| --- | --- |
| A | P1DIR |
| B | P1OUT |
| C | P2DIR |
| D | P2OUT |

| **ID** | **Bit** | **Function as set in the code** |
| --- | --- | --- |
| UCCKPH | 7 | Clock phase select |
| UCMSB | 5 | Controls direction of Tx/Rx shift registers |
| UCMST | 3 | Master mode select |
| UCSYNCH | 0 | Synchronous mode enabled |
| UCSSEL\_2 | 7-6 | Select smclk as source clk in master mode |
| UCSWRST | 0 | software reset enabled |

| **Symbolic Constant** | **Hex** | **Function** |
| --- | --- | --- |
| #STE2007\_RESET | E2 | Internal reset |
| #STE2007\_DISPLAYALLPOINTSOFF | A4 | LCD display normal display |
| #STE2007\_POWERCONTROL | 28 | Sets on chip power supply function |
| #STE2007\_POWERCTRL\_ALL\_ON | 2F | Booster voltage regulator voltage follower all on |
| #STE2007\_DISPLAYNORMAL | A6 | Normal: DDRAM data “H”=LCD on voltage |
| #STE2007\_DISPLAYON | AF | display turned on |

DOCUMENTATION: The following cadets worked together and discussed Lab 3 Mega Prelab on Sunday, 28 September 2014 starting at 1830 in the 321 classroom.

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