COSC 301: Operating Systems - Homework 4

Due Wednesday, October 17, 2012

1. Consider a logical address space of 32 pages with 1,024 words per page, mapped onto a physical memory of 16 frames.

   a. How many bits are required in the logical address?

   b. How many bits are requried in the physical address?

2. Consider a computer system with a 32-bit logical address and a 4-KB page size. The system supports up to 512 MB of physical memory. How many entries are there in each of the following?

   a. A conventional single-level page table

   b. An inverted page table

3. Consider a paging system with the page table stored in memory.

   a. If a memory reference takes 200 nanoseconds, how long does a paged memory reference take?

   b. If we add TLBs, and 75 percent of all page-table references are found in the TLBs, what is the effective memory reference time? (Assume that finding a page-table entry in the TLBs takes zero time if the entry is there.)

4. A simplified view of process states is "ready", "running", and "blocked", where a process is either ready and waiting to be scheduled, running on the processor, or blocked waiting for I/O. Assuming a process is in the running state, answer the following questions, including a brief explanation:

   a. Will the process change state if it incurs a page fault? If so, what is the new state?

   b. Will the process change state if it generates a TLB miss that is resolved in the page table? If so, to what new state?

   c. Will the process change state if an address reference is resolved in the page table? If so, what is the new state?

5. What is the copy-on-write feature, and under what circumstances is it beneficial to use this feature? What hardware support is required to implement this feature? (See the VAX/VMS chapter, section 22.5.)

6. Assume that we have demand-paged memory. The page table is held in registers. It takes 8 milliseconds to service a page fault if an empty frame is available or if the replaced page was not modified and 20 milliseconds if the replaced page was modified. Memory-access time is 100 nanoseconds.

   Assume that the page to be replaced is modified 70% of the time. What is the maximum acceptable page-fault rate for an effective access time of no more than 200 nanoseconds?

7. Consider a demand-paged system with a paging disk that has an average access and transfer time of 20 milliseconds. Addresses are translated through a page table in main memory, with an access time of 1 microsecond per memory access. Thus, each memory reference through the page table takes two accesses. To improve this time, we have added an associative memory (i.e., a TLB) that reduces access time to one memory reference if the page table entry is in the associative memory.

   Assume that 80% of the accesses are in the associative memory, i.e., TLB hits, and that of those remaining, 10 percent (or 2 percent of the total) cause page faults. What is the effective memory access time?