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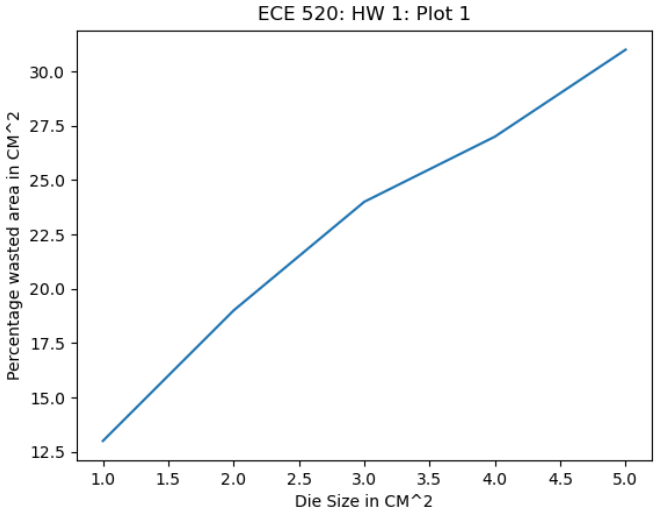
ECE 520 HW 1

1. In order to estimate the fabrication cost, we need to determine the number of dies in a wafer. Prove the equations in slide 61 of Lecture 1. Then, use the equations in the slide to determine the percentage of wasted silicon (due to the edge of the wafer), as a function of die size. Plot the % wasted area as a function of die size for die sizes from 1 Cm to 5 Cm in an 8-inch wafer.

The formula from slide 61 can be broken up into portions, each of which should provide an integer number of chips.

$$\frac{\pi \times (\text{wafer diameter}/2)^2}{\text{die area}} - \frac{\pi \times \text{wafer diameter}}{\sqrt{2 \times \text{die area}}}$$

The floor value of the left side of the equation returns a value of the total number of dies that could be assembled out of the total area in the wafer if it were possible to take the edge bits and cut them into dies.



The floor value of the right side of the equation returns a ratio of the wafer diameter to the corner to corner distance in each die that could possibly fit inside the circumference of the wafer. This dimensionless number describes how much bigger the wafer is than the space taken up by the whole dies. Any die that has an uninterrupted corner (nearest to wafer center) to corner (nearest edge of wafer) is contained within the wafer.

The right side of this equation effectively subtracts the difference in area between the wafer diameter and the circle defined by the number of whole chip radii that can fit on the wafer. This allows us to reduce the total count by the wasted area between the wafer edge and the whole dies that are intact.

Quick and dirty python code to plot the requested data. Assume 2.54 CM per inch.

```
#!/usr/bin/python3

import math
import matplotlib.pyplot as plot

data = []
wafer_diameter_cm = (8 * 2.54)

for diesize in range(1,6):
    wasted_dies = math.floor(
            (math.pi * wafer_diameter_cm) / math.sqrt(2 * (diesize)))
    total_dies = math.floor(
            (math.pi * (wafer_diameter_cm / 2) ** 2) / (diesize))
    percentage_wasted_area = math.floor(
            (wasted_dies / total_dies) * 100)
    print ("diesize(",diesize,") - wasted(",wasted_dies,") - total_dies(",
            total_dies,") - percentage_wasted(",percentage_wasted_area,")")
    data.insert(diesize, percentage_wasted_area)

plot.plot(range(1,6), data)
plot.title('ECE 520: HW 1: Plot 1')
plot.ylabel('Percentage wasted area in CM^2')
plot.xlabel('Die Size in CM^2')

plot.show()
```

Reference Used: https://ieeexplore.ieee.org/document/17237

2. In this problem, we would like to derive the equation for drain current in saturation region considering channel-length modulation. Assume that the change in channel length is proportional to VDS (i.e., ∆L/L=λVDS). Show how equation (3.29) in your textbook becomes (3.30) when you include channel length modulation.

Beginning with equation 3.29 from the text:

$$I_D = \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_T)^2 \qquad (3.29)$$

We allow our “L” to really become the effective length that we are trying to find and substitute in our physical length implemented minus some manufacturing dependent calculation as no material is a perfect conductor. This “delta L” needs to be factored into the equation and will result in the following change to 3.29.

$$I_{ds} = (\frac{k}{2})(\frac{W}{L - \Delta L})(V_{GS} - V_t)^2$$

Assuming that the ratio of manufacturing length parameter and the physical length is less than 1, some arithmetic will allow the middle term to be transformed to a sum of 1 + this ratio. Now one can factor the Width and the Length parameters arithmetically to simplify the middle term.

$$I_{ds} = (\frac{k}{2L})(\frac{W}{1 - \frac{\Delta L}{L}})(V_{GS} - V_t)^2$$

$$I_{ds} = (\frac{kW}{2L})(1 + \frac{\Delta L}{L})(V_{GS} - V_t)^2$$

We are given that the ratio in the middle term is equivalent to λVDS. We can now rearrange and substitute in this value to get something that resembles 3.30

$$I_{ds} = (\frac{kW}{2L})(1 + \lambda V_{ds})(V_{GS} - V_t)^2$$

$$I_{ds} = (\frac{kW}{2L})(V_{GS} - V_t)^2(1 + \lambda V_{ds})$$

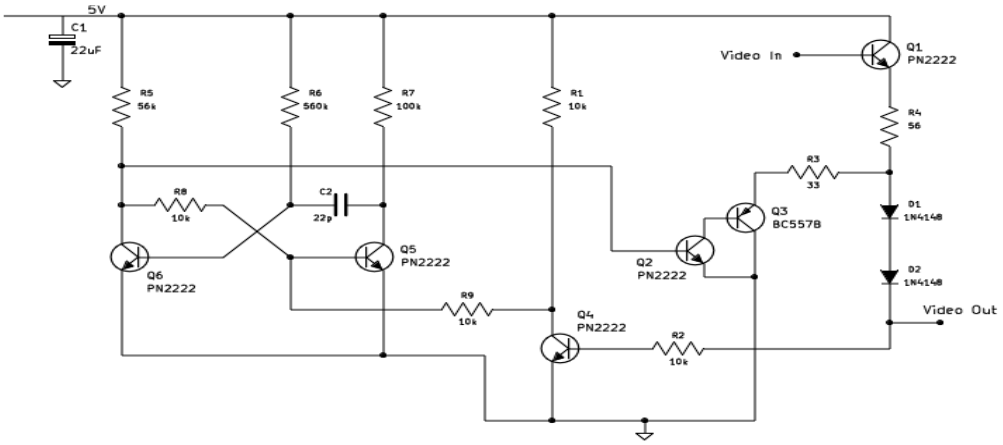
This can now be cleaned up by substituting our original eq in 3.29 to provide us the final form of 3.30.

$$I_{ds} = I_D(1 + \lambda V_{ds})$$

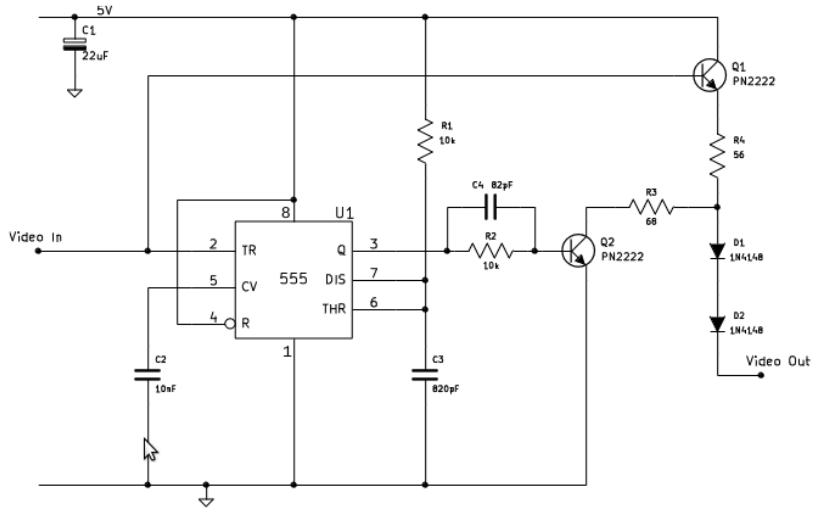
Reference Used: https://buzztech.in/channel-length-modulation-in-mosfet-vlsi-design/

3. Based on the list of previous VLSI projects for ECE520/424 that we discussed in Lecture 1, please suggest at least one new project that you will be interested in designing and working on during this semester. Please explain how you design your suggested project. Feel free to use online resources, for example https://www.upwithtech.com/post/best-vlsi-projects-for-final-year.

I'm a novice retro computing repair and hobby programmer from the 1980s. I've come into possession of several old Z80 based, Timex/Sinclair ZX-81 machines. Terrible keyboards and completely useless with modern screens. If we have the time, it might be fun to take the discrete logic design below and try to translate this into a working IC. The 2-3 transistors are simple enough that, while I can simply hack one together on my workbench from parts, it would be really interesting to compare that to a single piece of integrated logic.



An evenmore fancy version could be built with a 555 timer.



SRC: http://zx.zigg.net/misc-projects/ZX81_Video_Conditioning.pdf
FAQ: https://www.youtube.com/watch?v=1irH3KuGyl0