ECE520 – VLSI Design

Lecture 1: Introduction to VLSI Technology

Payman Zarkesh-Ha

Office: ECE Bldg. 230B
Office hours: Wednesday 2:00-3:00PM or by appointment
E-mail: pzarkesh@unm.edu

Course Objectives

- We will focus mainly on ***CMOS integrated circuits***
- There will be a design project assigned including:
  - Schematic design using S-Edit
  - Spice simulations and design verification
  - Layout design using L-Edit (including LVS and DRC)
  - Circuit extract and spice simulation (again)
- Project will be done by groups of 3-4 students
- Project grade will be based on:
  - Quality of report
  - Performance (speed/delay)
  - Power dissipation
  - Layout area
- There will be a 10% extra credit for any design that beats certain criteria for layout area, performance, or power consumption

Textbook and References

- **Main textbook:**
  - **"Digital Integrated Circuits" by J. M. Rabaey et al. (2nd edition)**
- **Other reference books:**
  - **"Physical Design of CMOS Integrated Circuits Using L-Edit" by J. Uyemura**
  - **"Design of High-Performance Microprocessor Circuits", by A. Chandrakasan**
- **Lecture Notes: combination of slides and discussions**
  - **Slides will be posted on the class webpage**
  - **Class webpage: *www.unm.edu/~pzarkesh/ECE520***
- **Reference papers posted on the class webpage**

Grading Policy

- Your grade in the course will be comprised of:
  - Homework (25%)
  - Project (25%)
  - Midterm Exam (25%)
  - Final Exam (25%)
- Final letter grade will be based on curve and class performance
- No makeup exam

Homework Policy

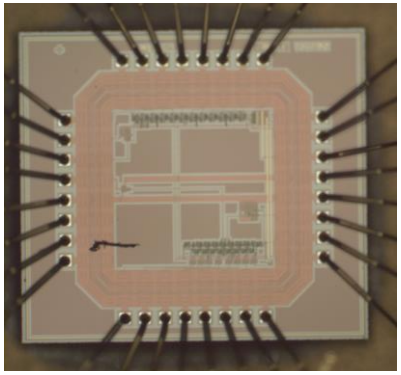
- Homework will be on weekly basis and is setup for the project
  - Learn CAD tools and basic circuits
  - Require lab work
- Solutions will be posted on the class website as soon as I can
- Late homework and projects have 20% per day credit penalty

Class Project & Tools

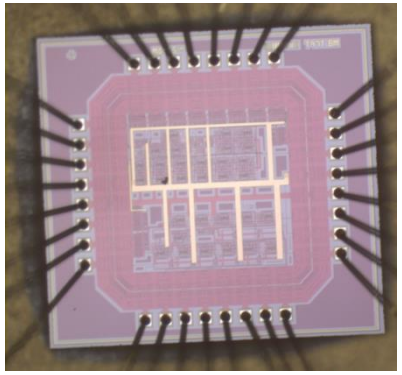
- Use of CAD tools will be required for most assignments. Get yourself familiarized with the tools from today!
- This is a project-oriented course. Be prepared for extensive lab work!
- We will be using L-Edit for our VLSI project
  - all Tanner tools including L-Edit, S-Edit, T-SPICE, LVS, and W-Edit are installed on all machines in ECE 211 Lab
  - The tools can also be installed on your own computer for the project use
  - for more information about these tools, please visit class website
- We will be using 0.5 um ON Semiconductor for our process
  - Selected projects will be submitted for manufacturing by MOSIS, if it becomes available on time
  - for more information about this process please visit https://themosisservice.com/university-support

Projects Manufactured by MOSIS in 2009

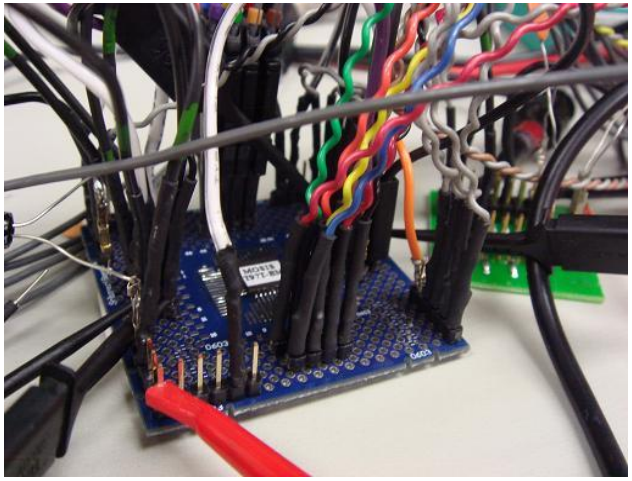
Test Chip 1	Test Chip 2
Thomas Leboeuf John (Colby) Hoffman	Kevin Fox Srinivasan Sridhar Shawn Levesque

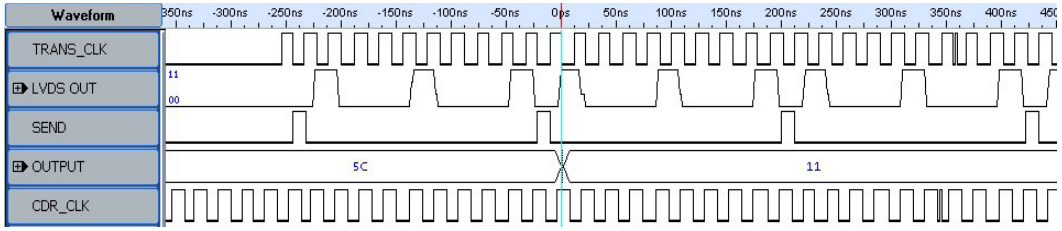


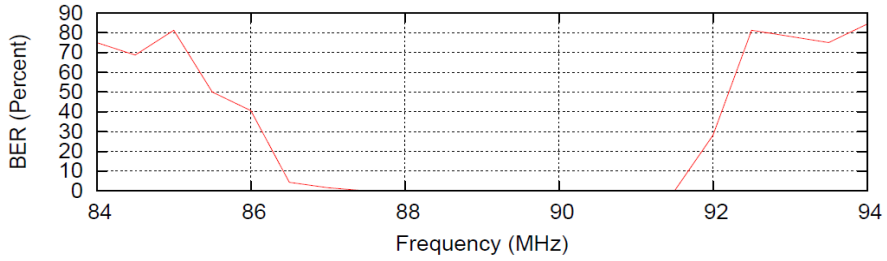
Test Chip 1



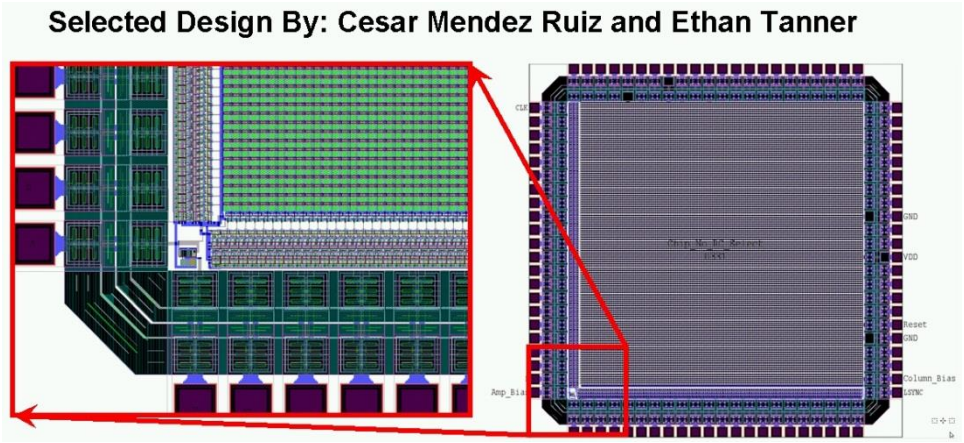
Test Chip 2

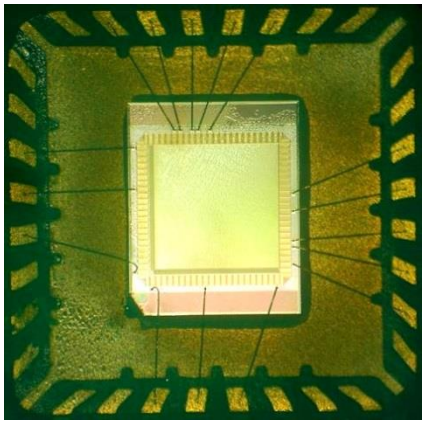




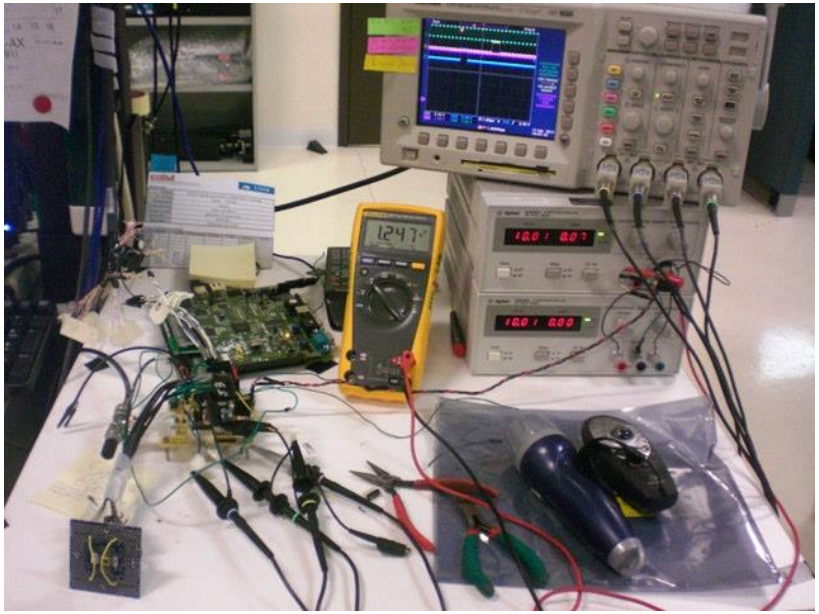


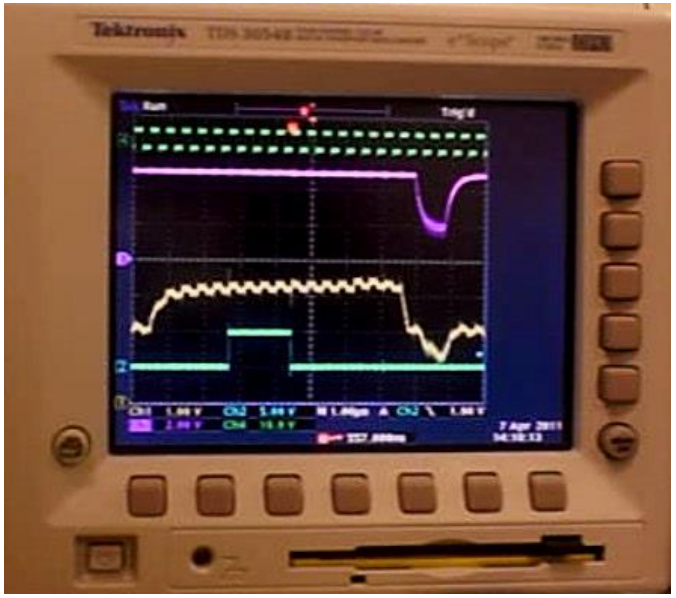
Projects Manufactured by MOSIS in 2010





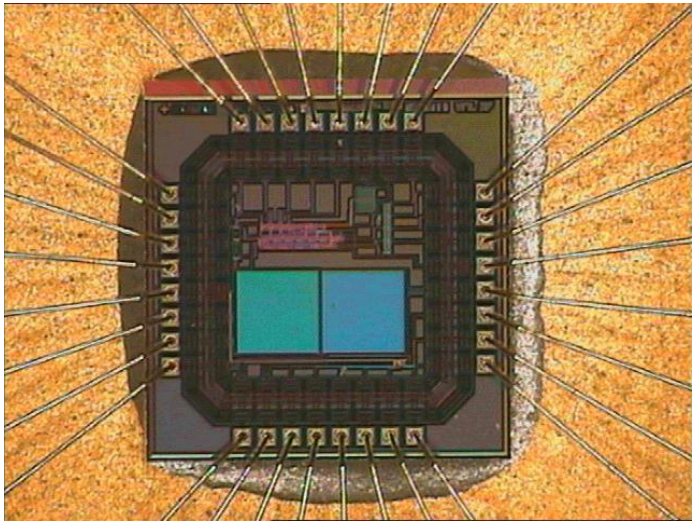
Die Photograph of the Test Chip



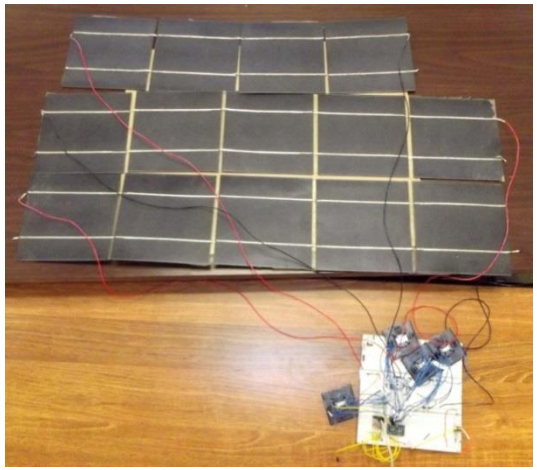


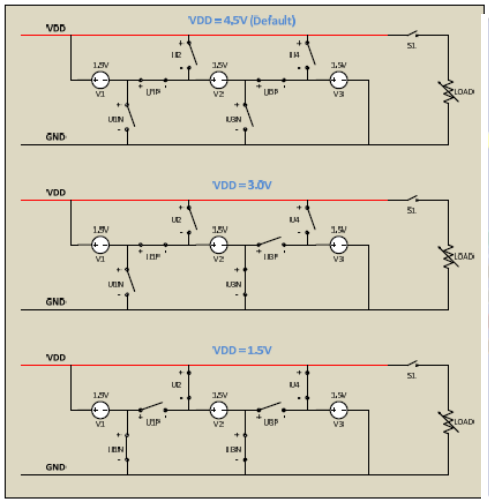
Projects Manufactured by MOSIS in 2011

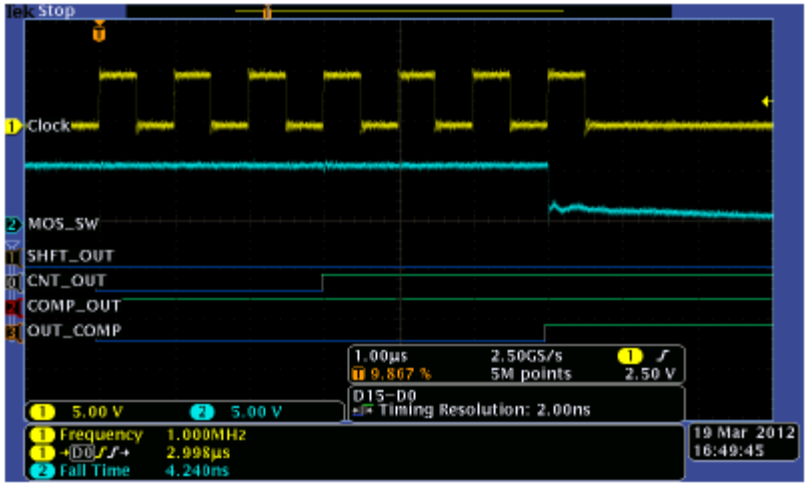
Design 1	Design 2
Mike Echert Roger Flateau	William Cavanaugh Jing Ju Kanamu Pupuhi



Die Photograph of the Test Chip 2

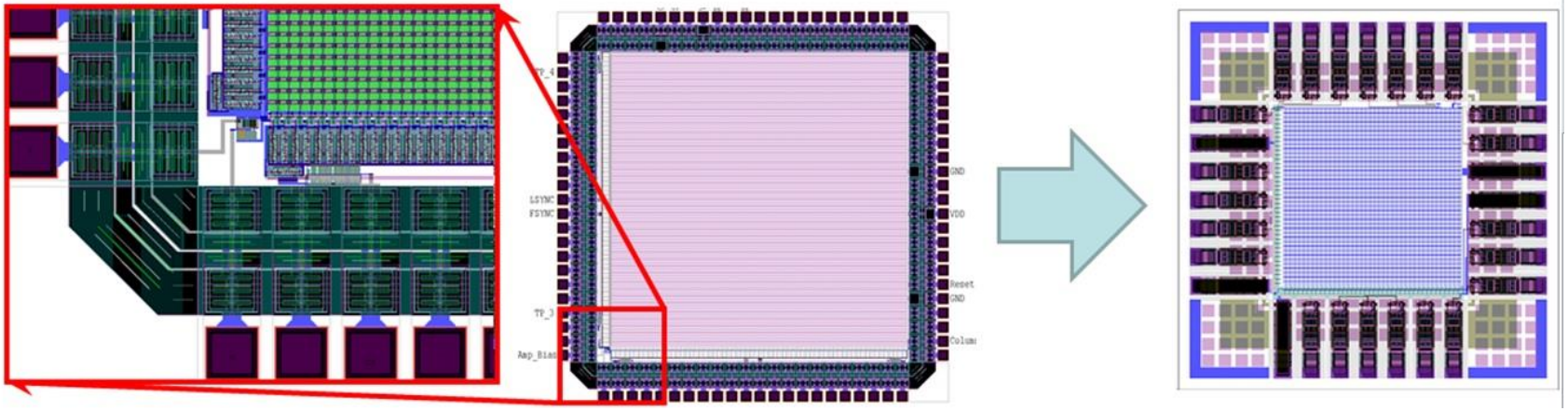


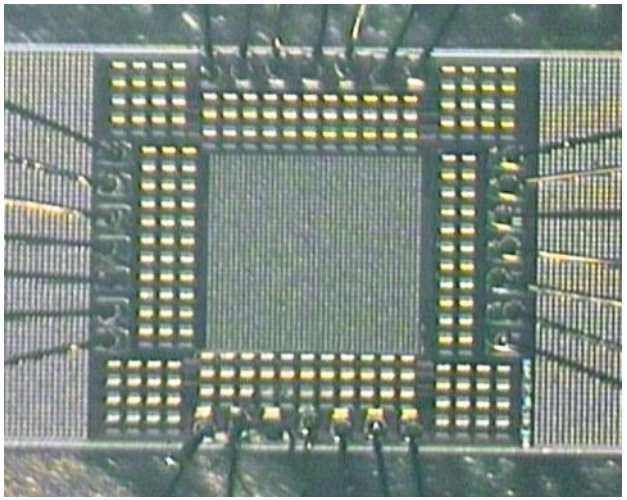


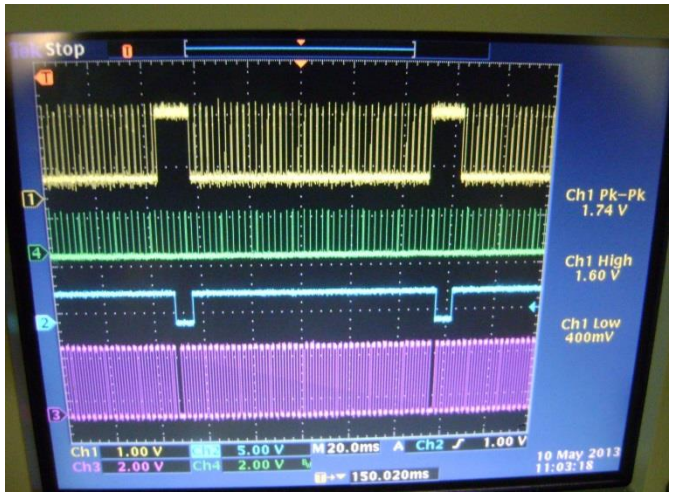


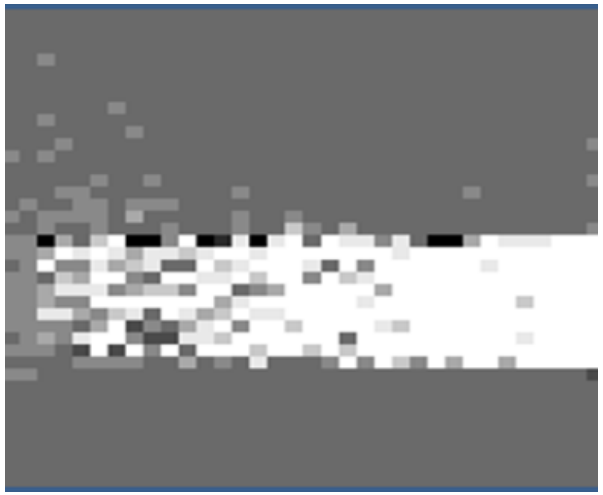
Projects Manufactured by MOSIS in 2012

Selected Design By: Javad Ghasemi









Class Schedule

Warning: Lecture schedule subject to change!!

Date	Day	Topic	Reading/Coverage
January 16	Tue	Introduction to VLSI Technology	1.1-1.3
January 18	Thr	Basic MOS Physics	3.2 - 3.3
January 23	Tue	PSPICE Demo 1	-
January 25	Thr	More MOS Physics	-
January 30	Tue	Device Scaling Issues	3.4-3.5
February 1	Thr	Basic CMOS Inverter	5.1.4
February 6	Tue	Basic CMOS Inverter - cont.	5.1-5.4
February 8	Thr	Dynamic Behavior of CMOS Inverter	5.4-5.6
February 13	Tue	CMOS Manufacturing Process	2.1-2.3, 2.4 (review), 2.5
February 15	Thr	Interconnect Manufacturing & Modeling	4.1-4.5
February 20	Tue	Design Rules	2.3, insert A
February 22	Thr	Layout Techniques & L-Edit Demo	handouts
February 27	Tue	Combinational Static Logic	6.1-6.2
February 29	Thr	Gate Sizing (Inveter Chain)	5.4
March 5	Tue	Gate Sizing (Inveter Chain) - cont.	5.4
March 7	Tue	Midterm Exam	-
March 12	Tue	Spring Break	-
March 14	Thr	Spring Break	-
March 19	Tue	Logical Effort	6.1 - 6.2
March 21	Thr	Logical Effort - cont.	6.1 - 6.2
March 26	Tue	Pseudo Logic and Pass-Transistor Logic	6.2
March 28	Thr	Project Review	-
April 2	Tue	Dynamic Logic	6.3
April 4	Thr	Advanced topics: Power Reduction	Handout
April 9	Tue	Sequential Logic	7.1-7.2
April 11	Thr	Sequential Logic - cont.	7.1-7.2
April 16	Tue	Timing Issues	10.1-10.2
April 18	Thr	Clock Distribution - PLL	10.3
April 23	Tue	Power Distribution & I/O Circuits	9.1-9.4
April 25	Thr	Memories	12.1-12.2
April 30	Tue	Nonvolatile Memories	12.2
May 2	Thr	SRAM Memories & Review for Final	Project Due
May 7	Tue	Final Exam (12:30-2:30PM)	-

Reading Assignment

- **Today we will review Chapter 1 and some more**
  - **Introduction and history**
- **Our next class will be on Chapter 3 (MOS Physics)**
  - **Skim through Diodes but focus on Section 3.2.3 (diode transient behavior)**
  - **Study Section 3.3 (MOS transistor) *thoroughly***
- **We will get back to Chapter 2 (Manufacturing Process) later**

VLSI Design Flow

- **The goal of VLSI designers is to design a circuit block that meets the following objectives:**
  - **Maximize speed or performance**
  - **Minimize power consumption**
  - **Minimize area**
  - **Maximized robustness**
- **Methods that they use are:**
  - **Circuit design, transistor sizing**
  - **Use of new architectures, clock gating, etc**
  - **Choice of circuit style, efficient layout design**
  - **Interconnect design and optimization**

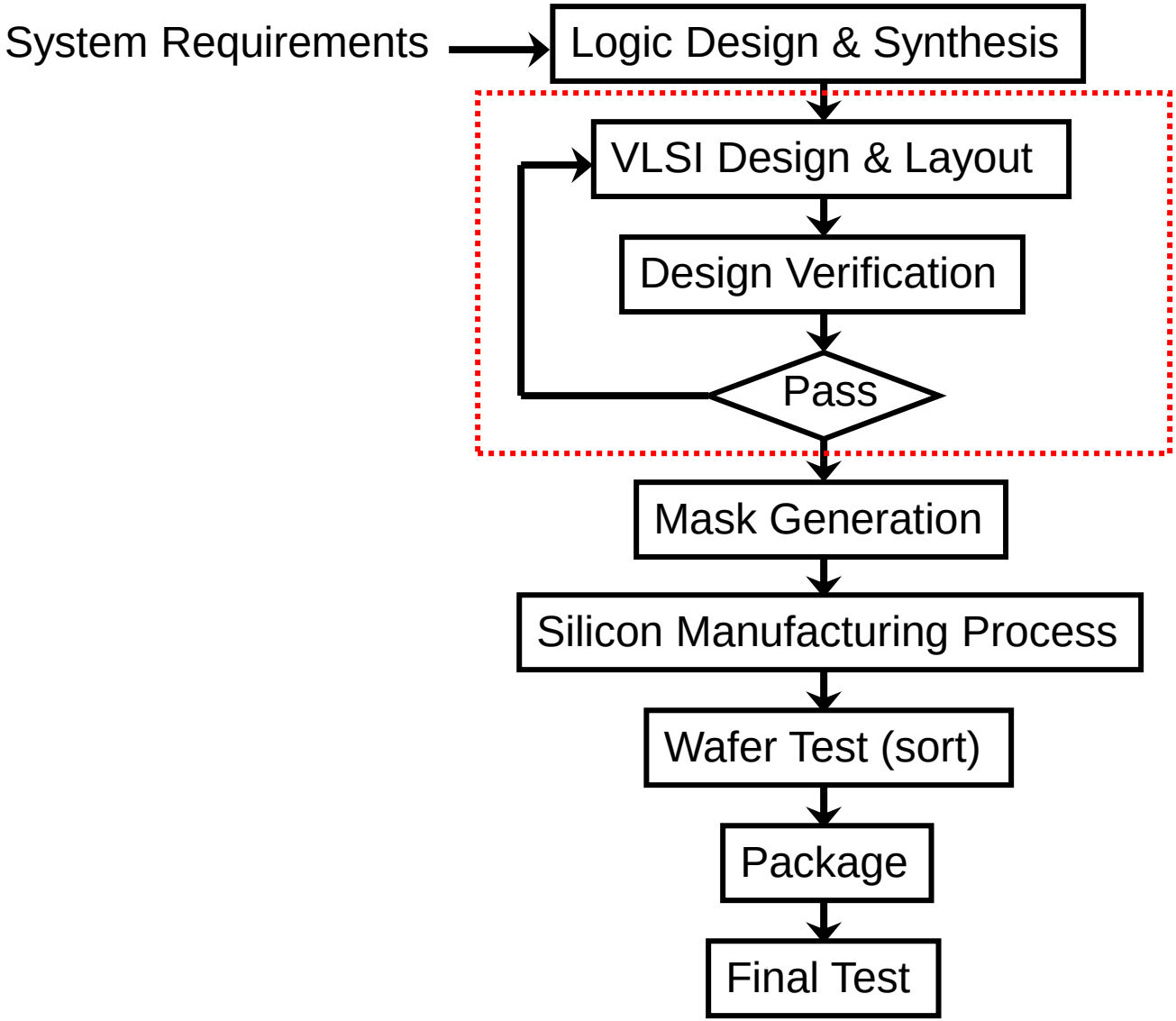
VLSI Design Approaches

- **Gate Arrays (Old technology, but still attractive)**
  - Pre-fabricated chips containing transistors and local wiring
  - Upper-level wires added to implement design
  - Rapid design, but very sub-optimal, slow, and usually high-power consumption
- **Standard Cells (Used for ASIC design)**
  - Cells in a library with fixed sizes
  - Cells pre-characterized for delay and power
  - Design is fast and layout is done automatically
  - Better performance, in the range of several 100's MHz
- **Custom Design (Used for Microprocessor design)**
  - Optimal circuit design and sizes
  - Extensive design verification required
  - Slowest, but densest layout design
  - Best performance, in the range of 1-5 GHz

VLSI Design Tools

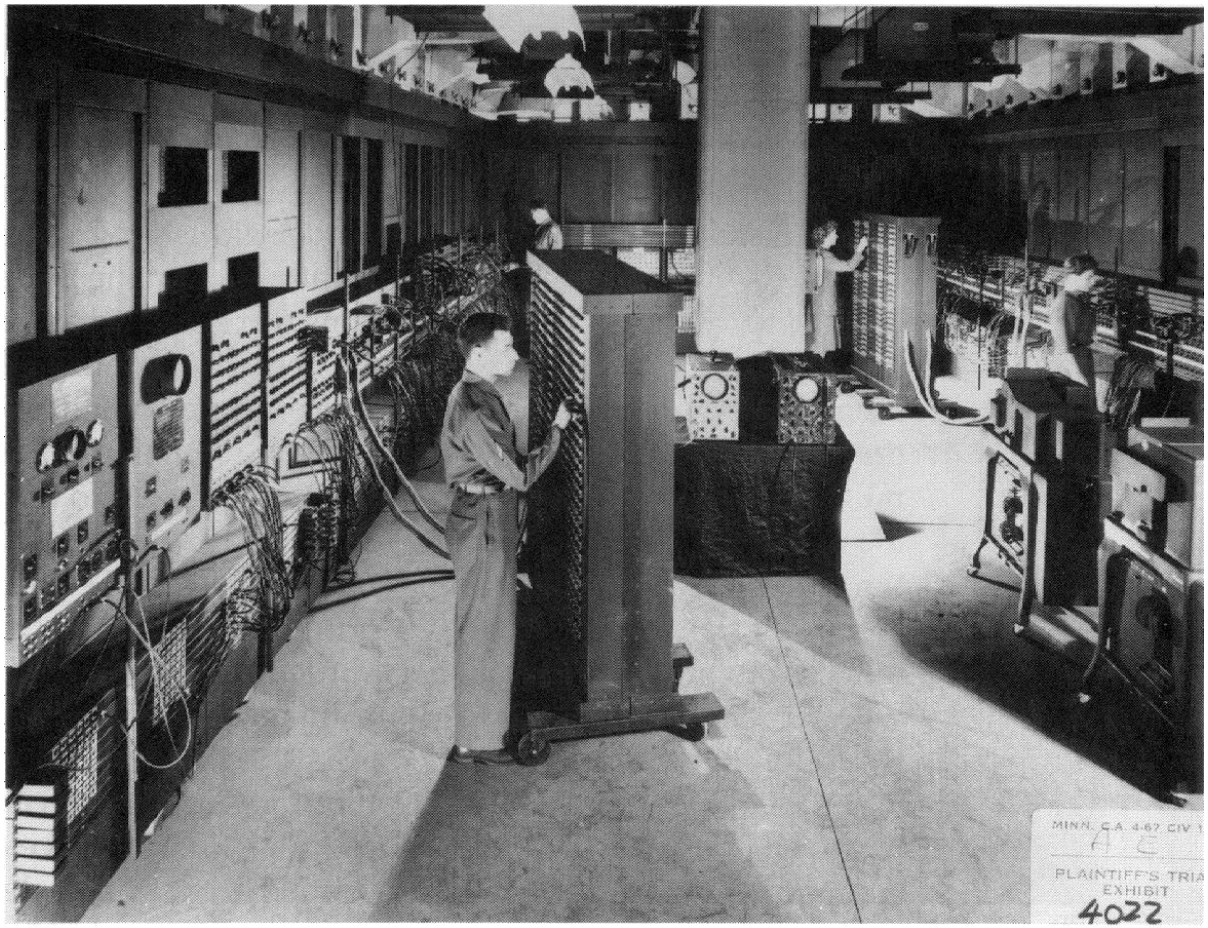
- **Synthesis**
  - Logic, micro-architecture, automatic physical generation
- **Static Analysis**
  - Design rule checking (DRC)
  - Circuit extraction
  - Timing analysis
  - Test generation (ATPG)
- **Dynamic Analysis**
  - Architectural simulation
  - Logic simulation
  - Circuit simulation (SPICE)
  - Test verification

High Level VLSI Design Steps



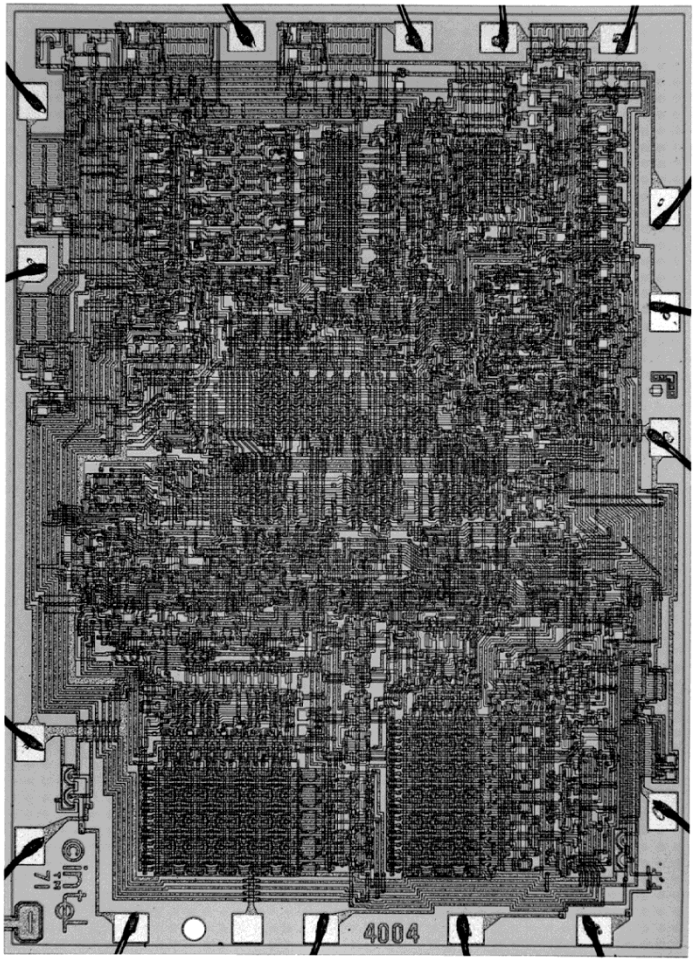
Introduction

Beginning of the Computer: ENIAC, the first electronic computer (1946)



- 333 integer multiplication/second
- A six-week run was equivalent to 100 person-years of manual computation
- Program resides in the wired connections

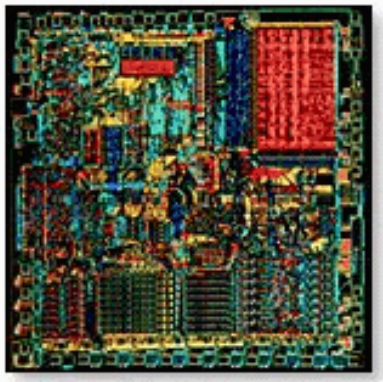
Intel 4004 Microprocessor



- 1971
- 10 um NMOS-only
- 2300 transistors
- 1 MHz

Intel Technology Advancement

Processor Comparison



Intel® i8088

Year: 1981
29,000 transistors

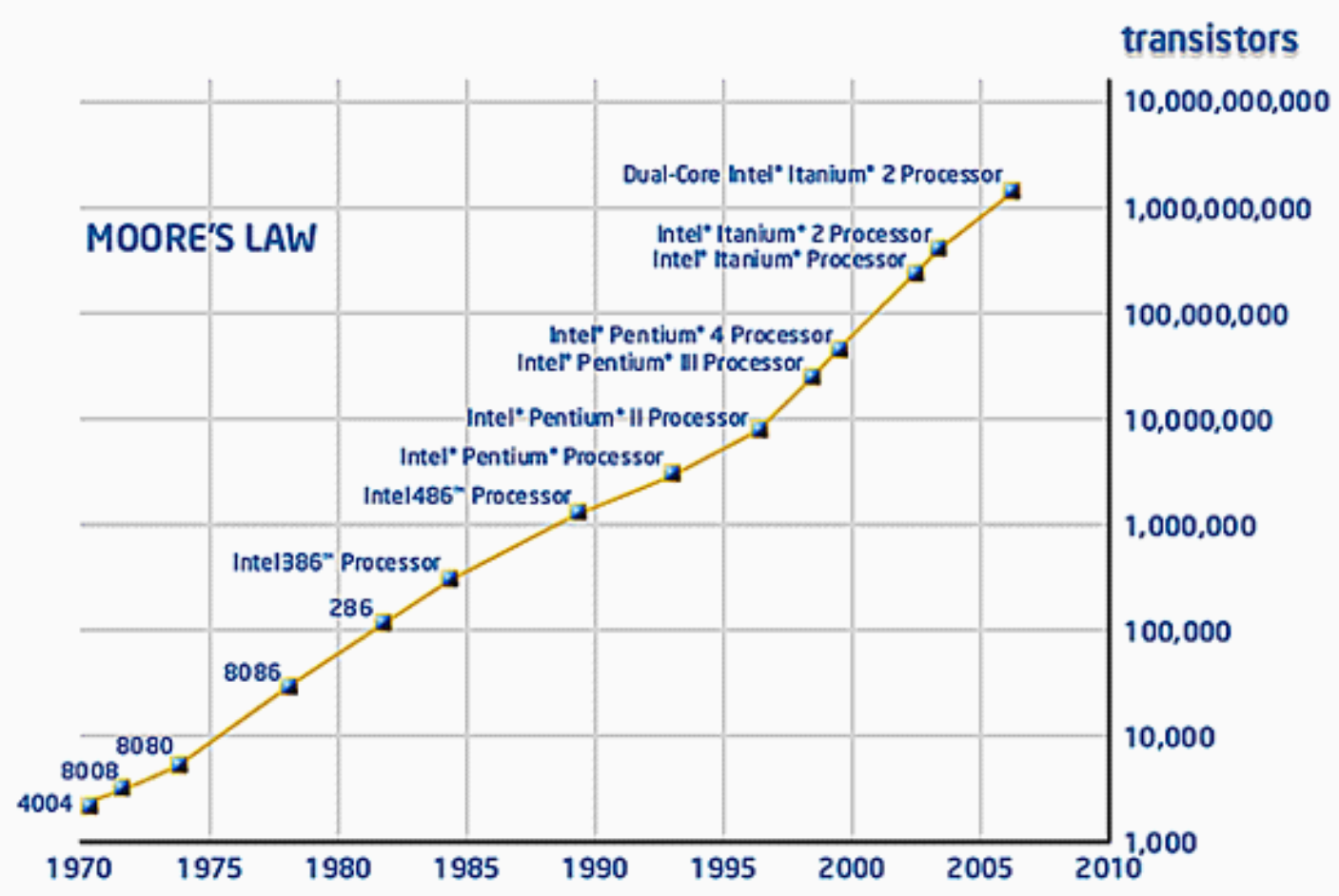
Intel® Pentium® 4 Processor with HT Technology

Year: 2004
125,000,000 transistors

Moore's Law

- In 1965, Gordon Moore (founder of Intel) had a very interesting observation. He noticed that the number of transistors on a chip doubled every 18 to 24 months.
- He made a prediction that semiconductor technology would double its effectiveness every 18 months.

Moore's Law for Intel Microprocessors



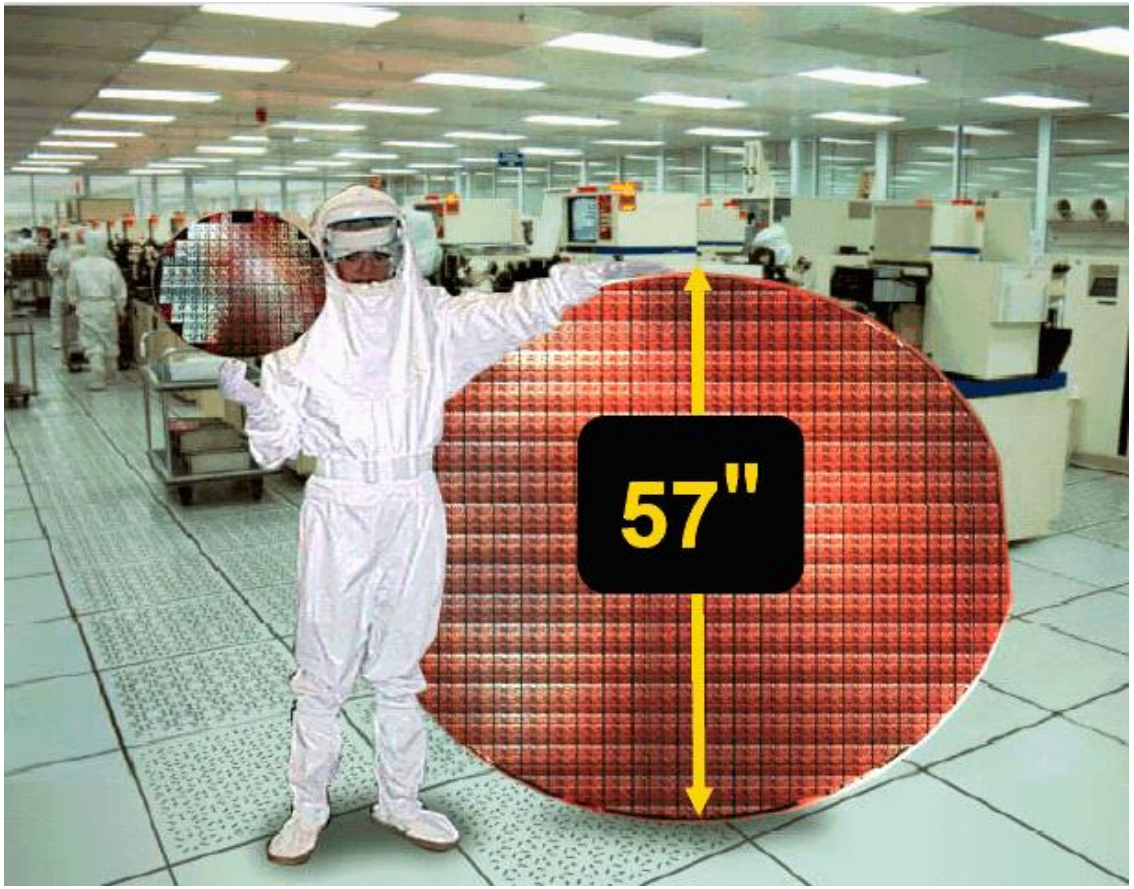
Source: www.intel.com

Moore's Law in Travel Industry

1978
Approximate Cost: **$900**
Approximate Travel Time: **7 hours**

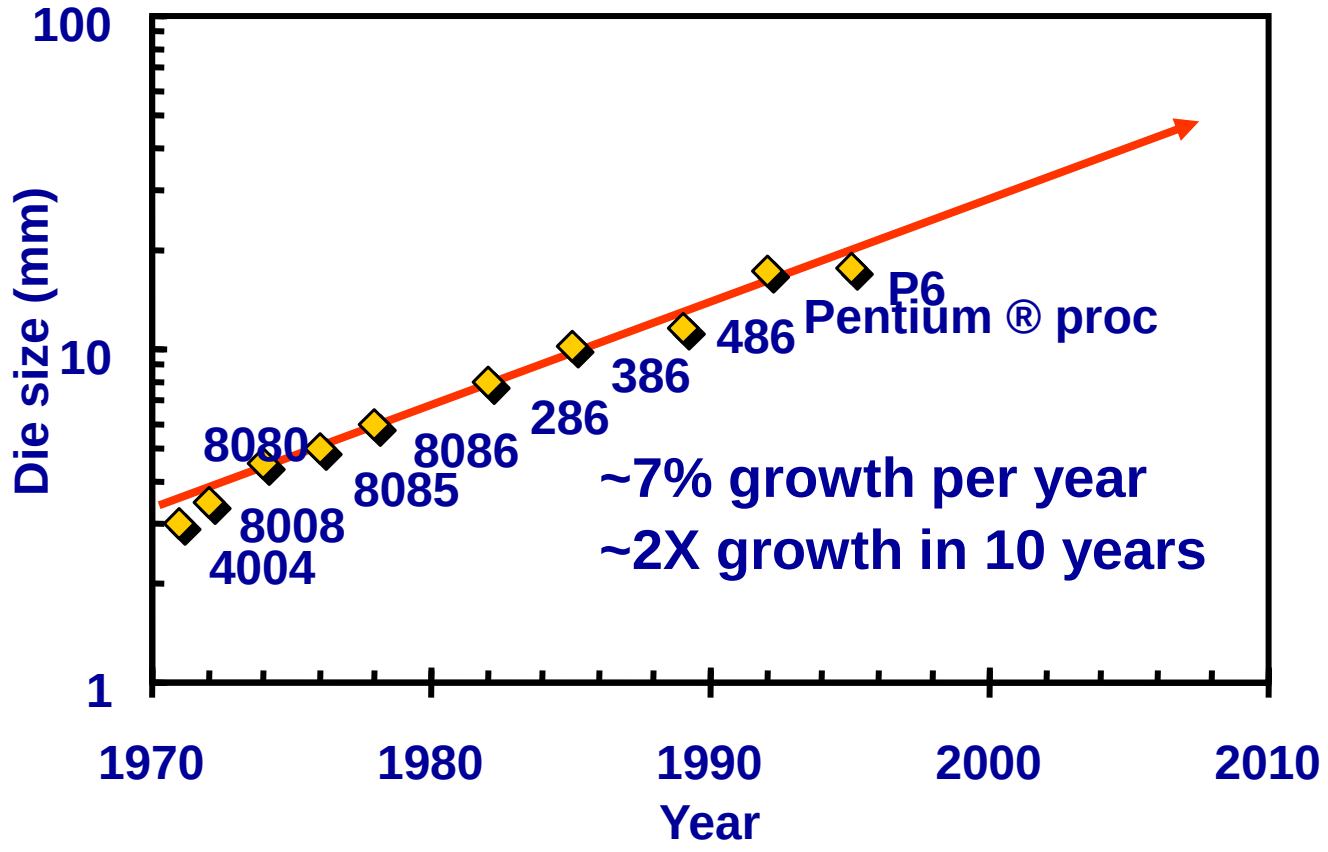
2003
Approximate Cost: **1¢**
Approximate Travel Time: **¼ second**

Projected Wafer in 2000, circa 1975



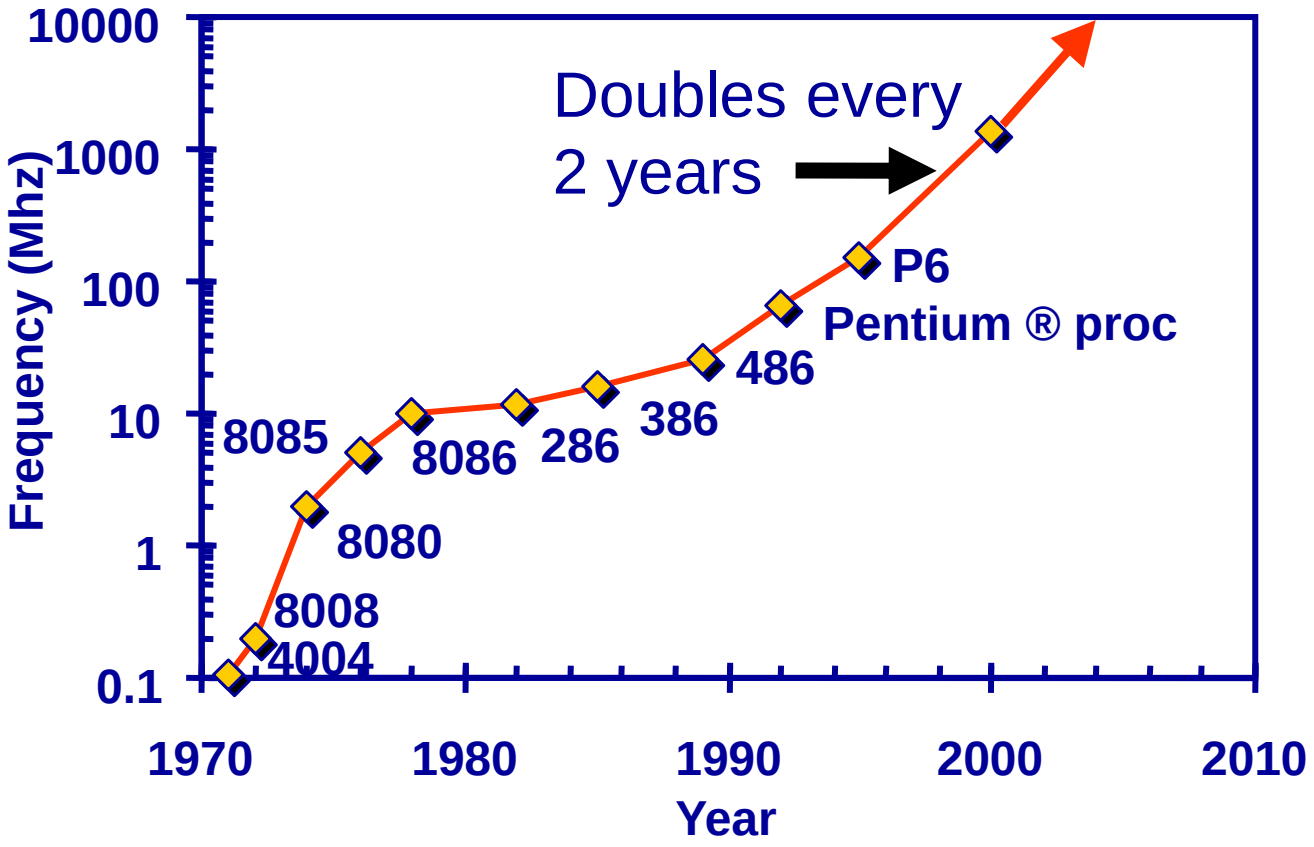
Moore was not always accurate

Die Size Growth



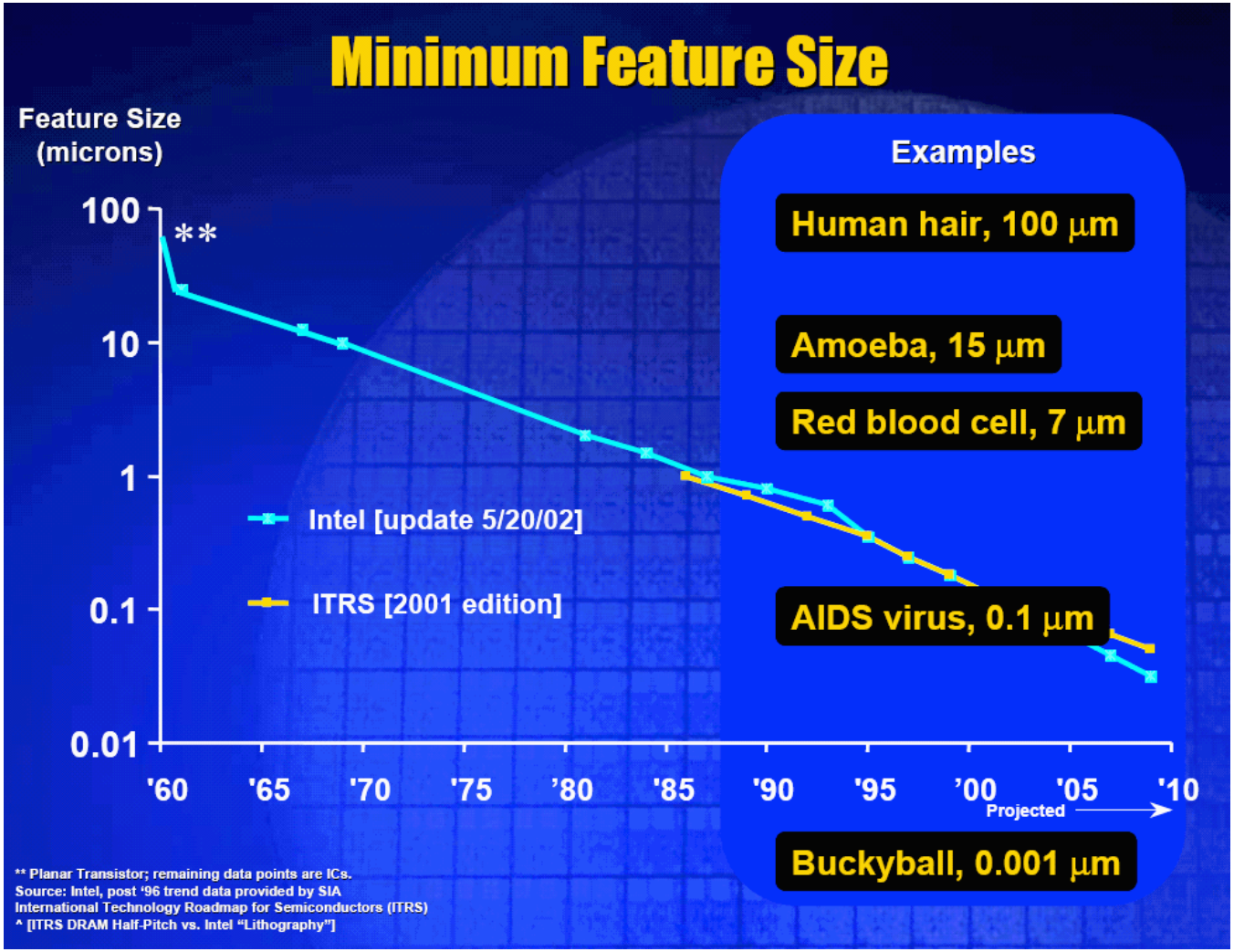
Die size has grown by 14% to satisfy Moor's law, BUT the growth is almost stopped because of manufacturing and cost issues

Clock Frequency



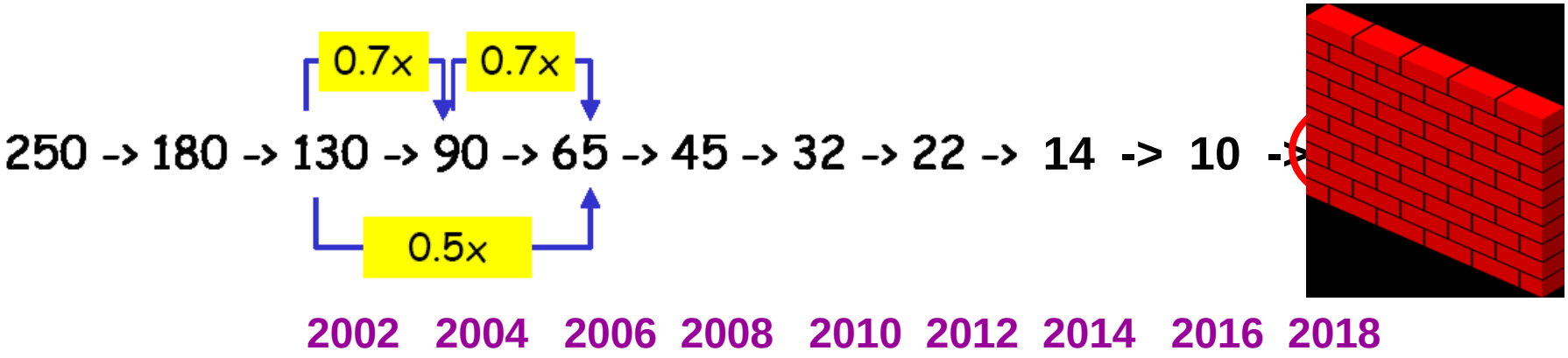
Lead microprocessors frequency doubles every 2 year, BUT the growth is slower because of power dissipation issue

CMOS Scaling Scenario

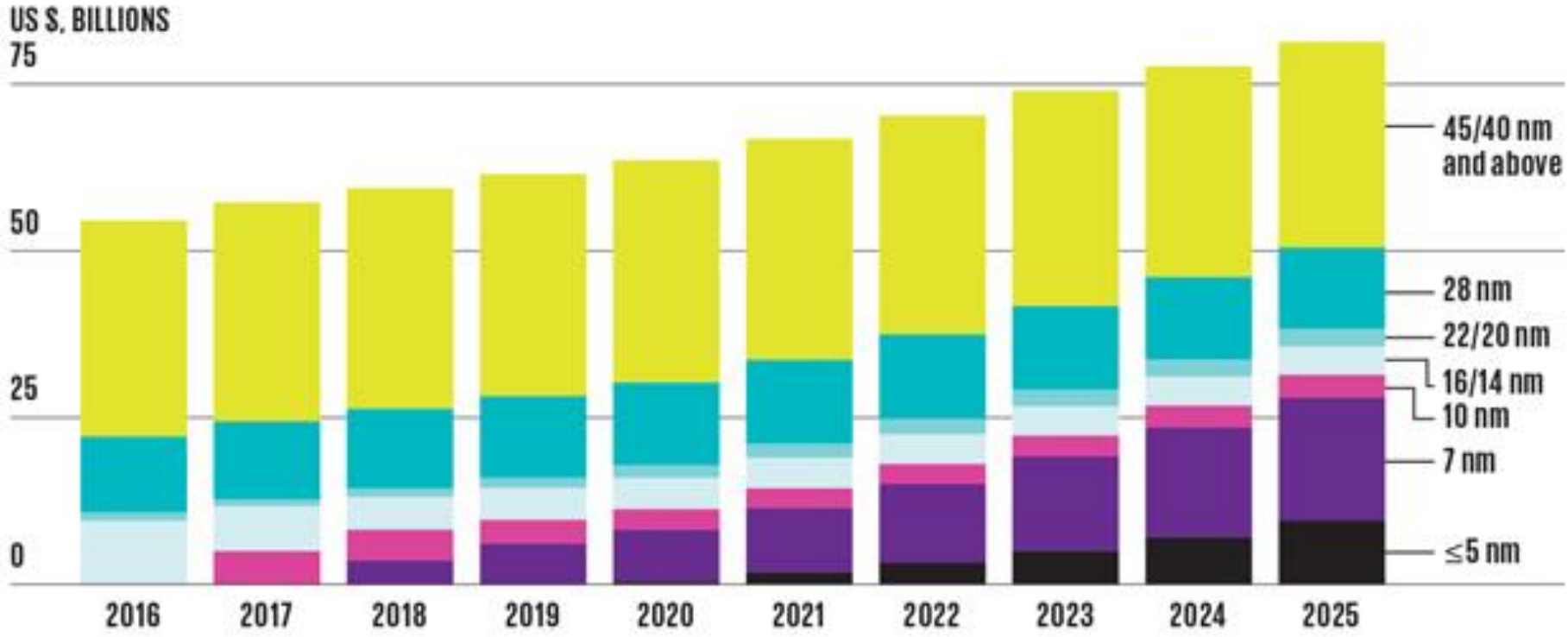


CMOS Scaling Calculation

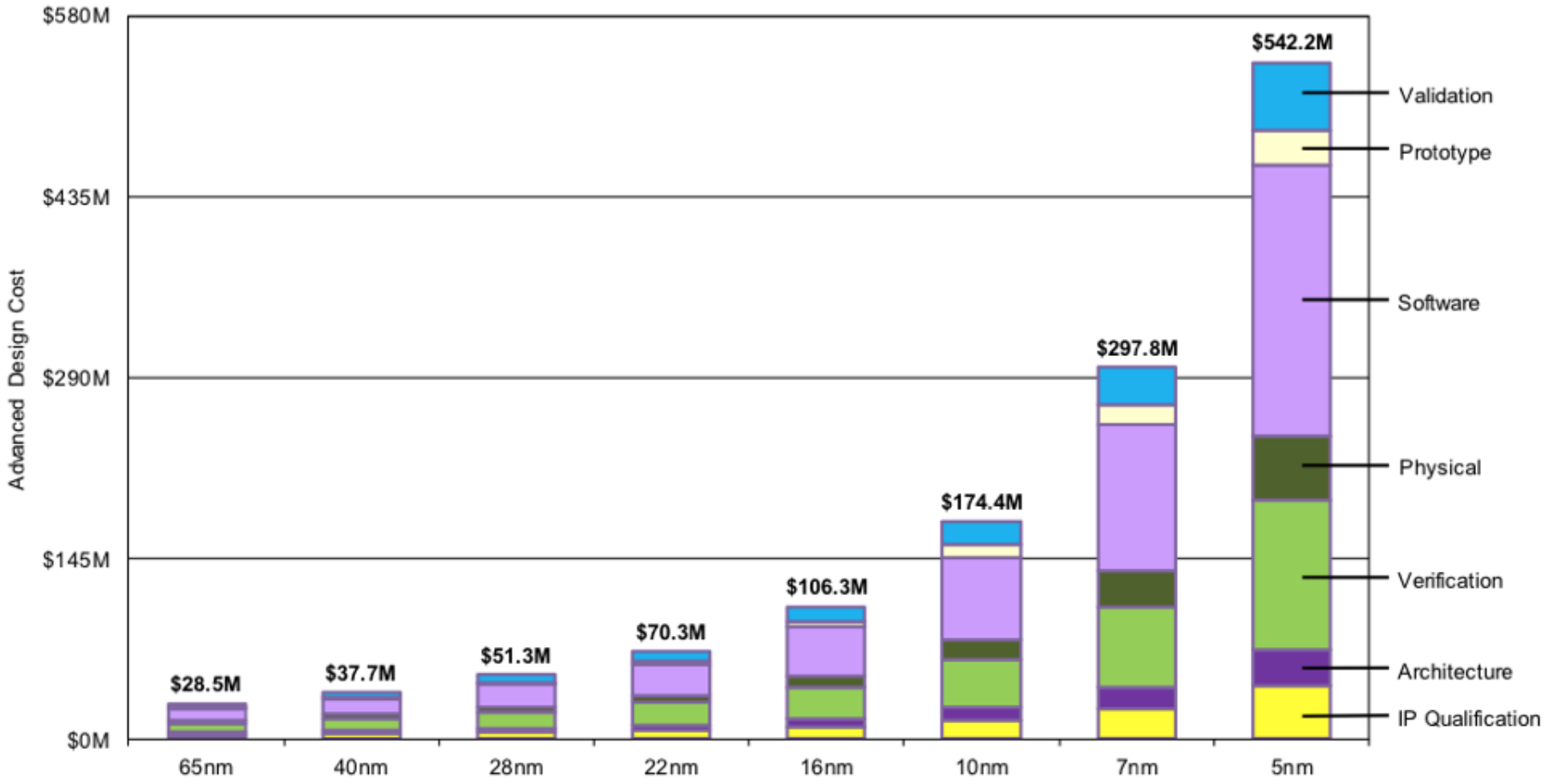
Scaling Calculator



The Prediction of Foundry Market

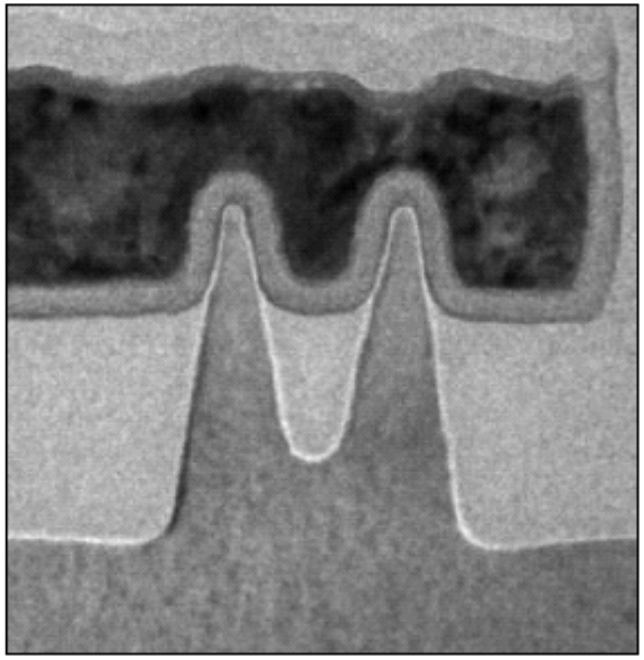


Cost of Design versus Technology Node

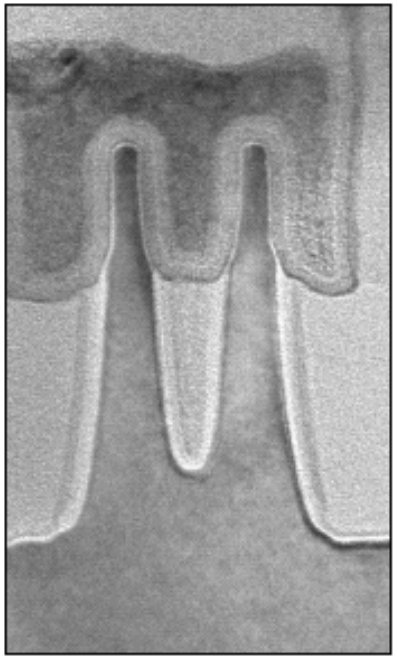


Intel's 22nm and 14nm Fin-FET Technology

Transistor Fin Improvement

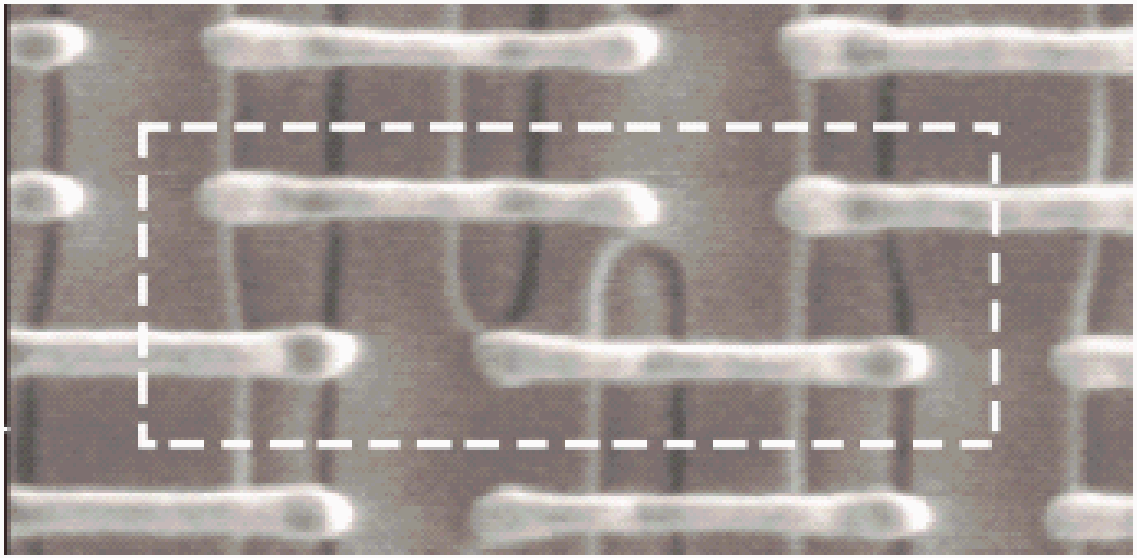


22 nm 1st Generation
Tri-gate Transistor



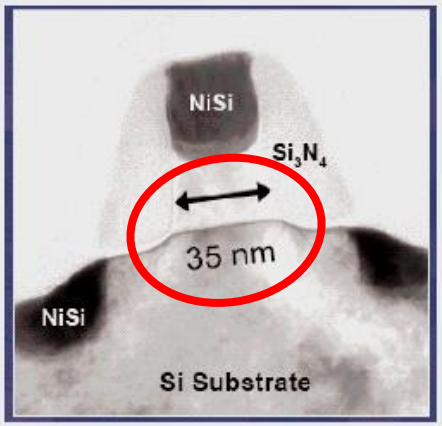
14 nm 2nd Generation
Tri-gate Transistor

65nm SRAM Memory Cell



10 million of these transistors could fit in a square millimeter – about the size of the tip of a ballpoint pen

MOS in 65nm of Core Due Processor



Intel strained silicon (top) and a 65-nm wafer of Intel® Core™ Duo processors (bottom).

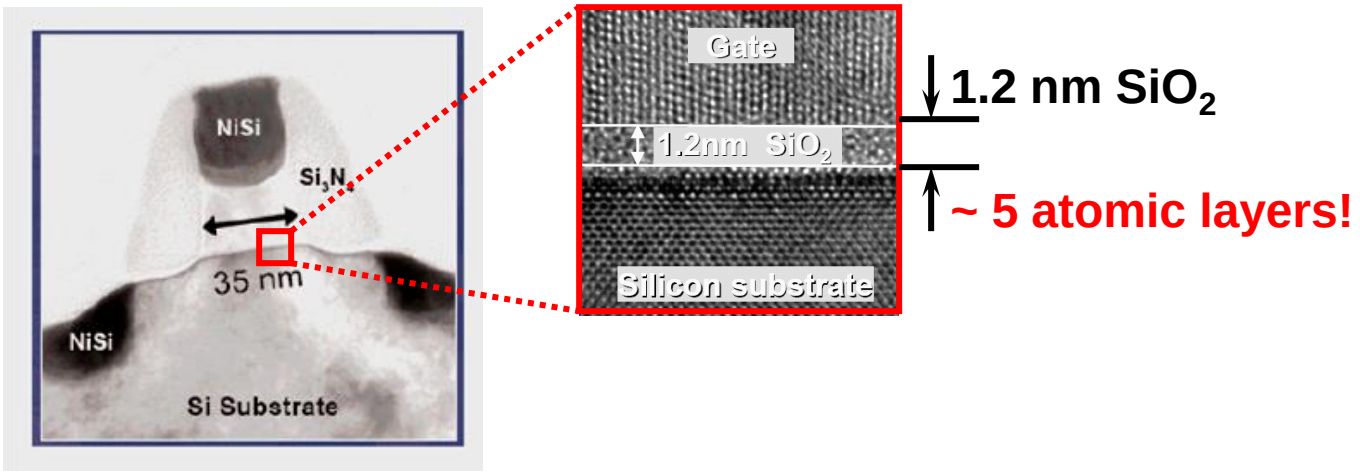
Distance between Si atoms = 5.43 ºA

No. of atoms in channel = 35 nm / 0.543 nm

= 64 Atoms!

Problem: Uncertainty in transistor behavior and difficult to control variation!

Gate Insulator Thickness



Problem: Electrons can easily jump over the 5 atomic layers!

This is known as leakage current

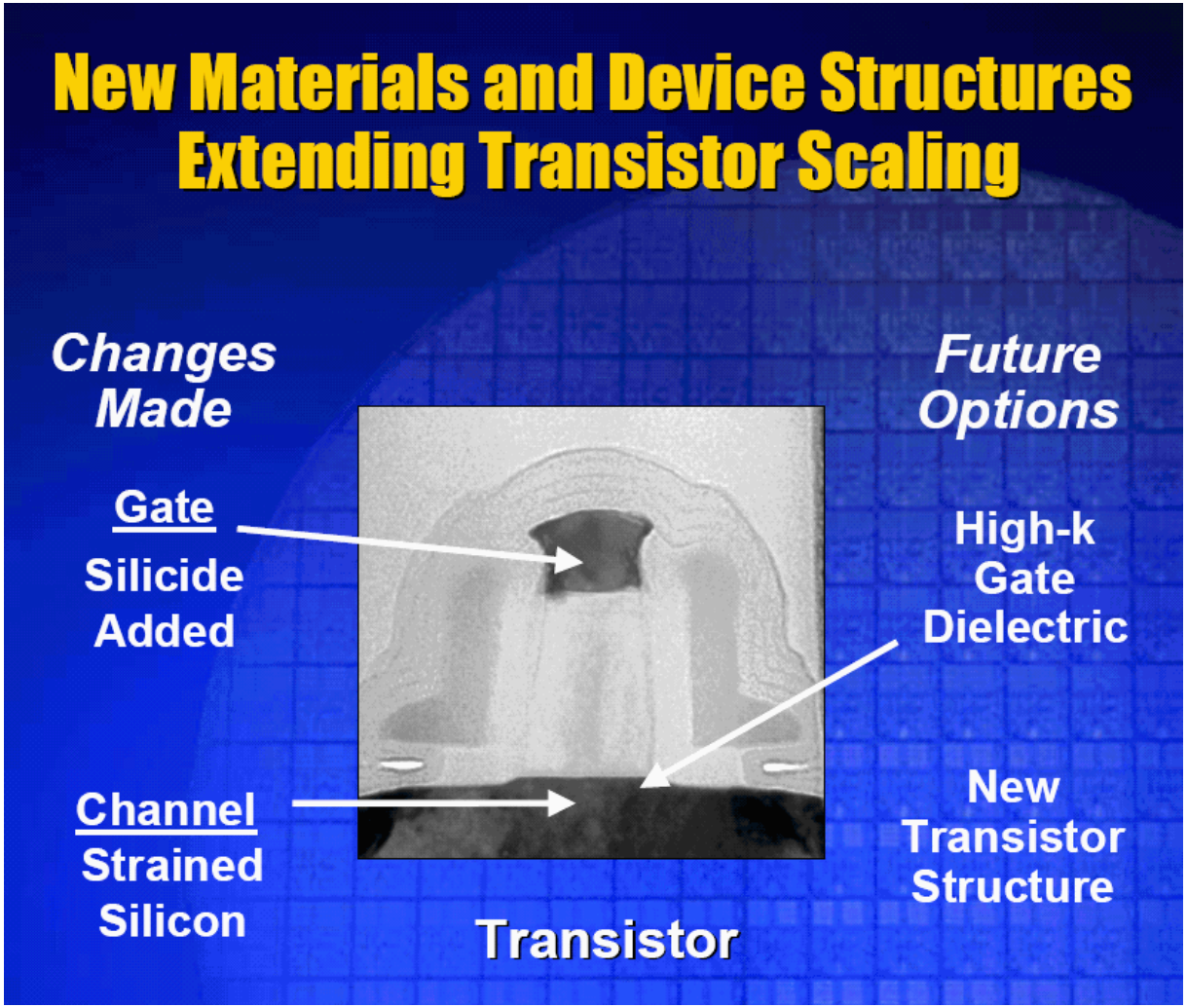
Benefit of Smaller Transistors

1) **More transistors in the same foot-print**
2) **More functionality**
3) **Reduced cost per function**
4) **Faster devices and higher performance**
5) **Lower switching energy per transistor**

Transistor Scaling Challenges

1) **Feature sizes down to few atomic layers**
2) **Increase uncertainty of transistor behavior**
3) **Increase leakage power consumption**
4) **Difficult to maintain performance enhancement**
5) **Thermal limit issue**

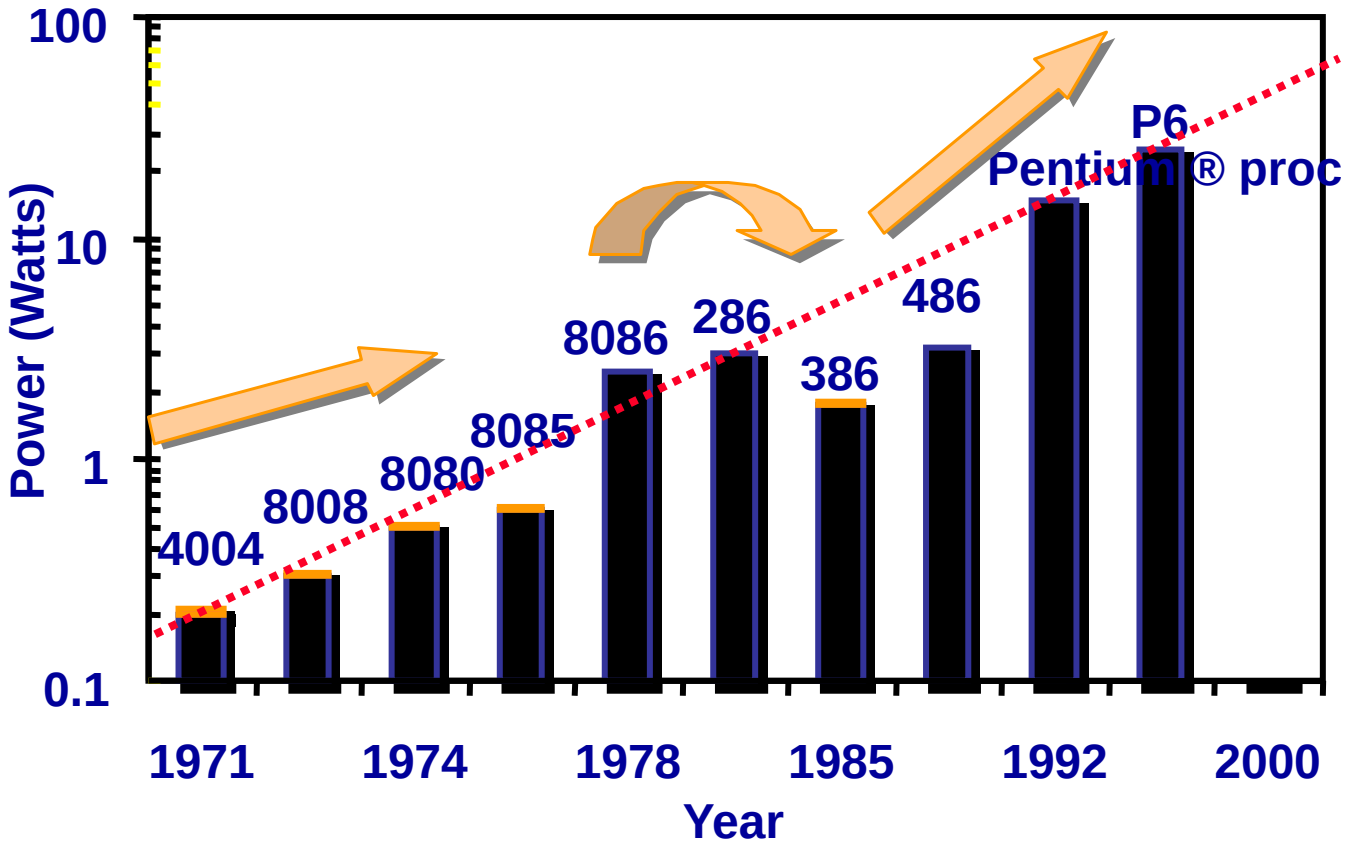
New Method to Deal with Scaling



Far-future Alternative Logic Devices

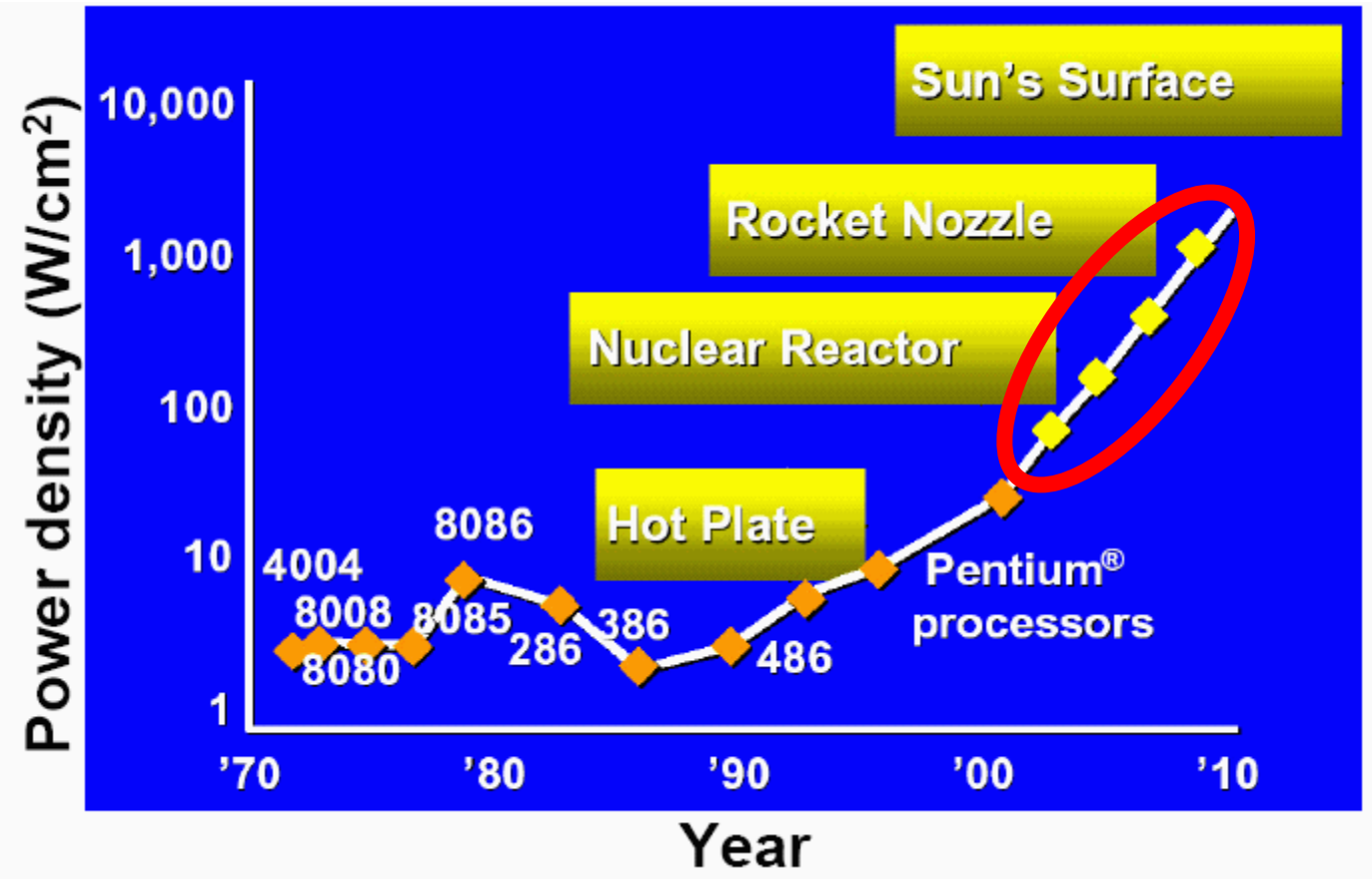
1) **Spintronics (spin-based electronics)**
2) **Quantum Computing**
3) **DNA Computing**
4) **Optical Computing**

Power Dissipation



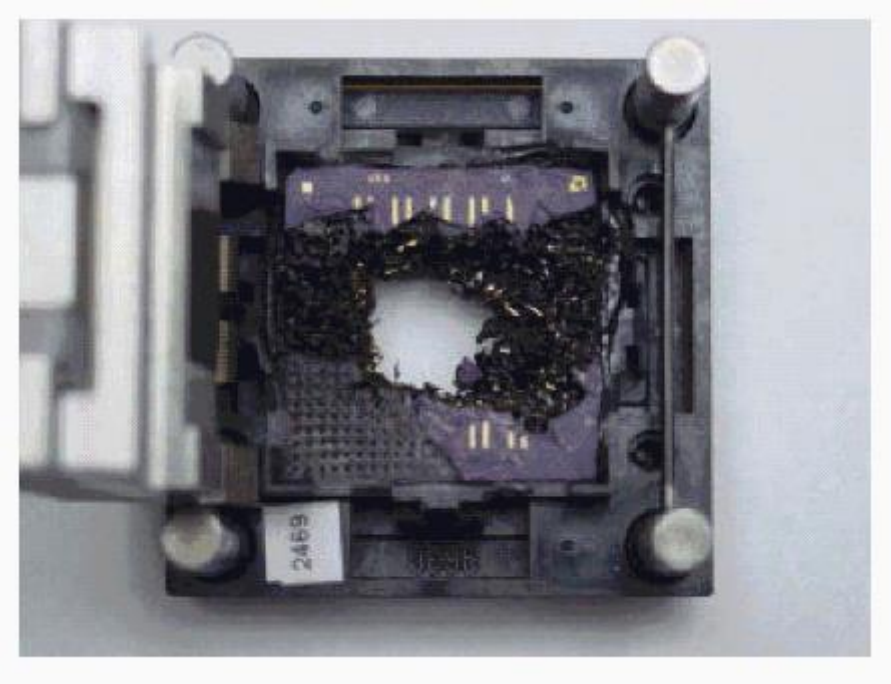
Lead microprocessors power dissipation continue to increase, <u>BUT</u> it is getting too hard (and expensive) to keep up

Power Density Problem

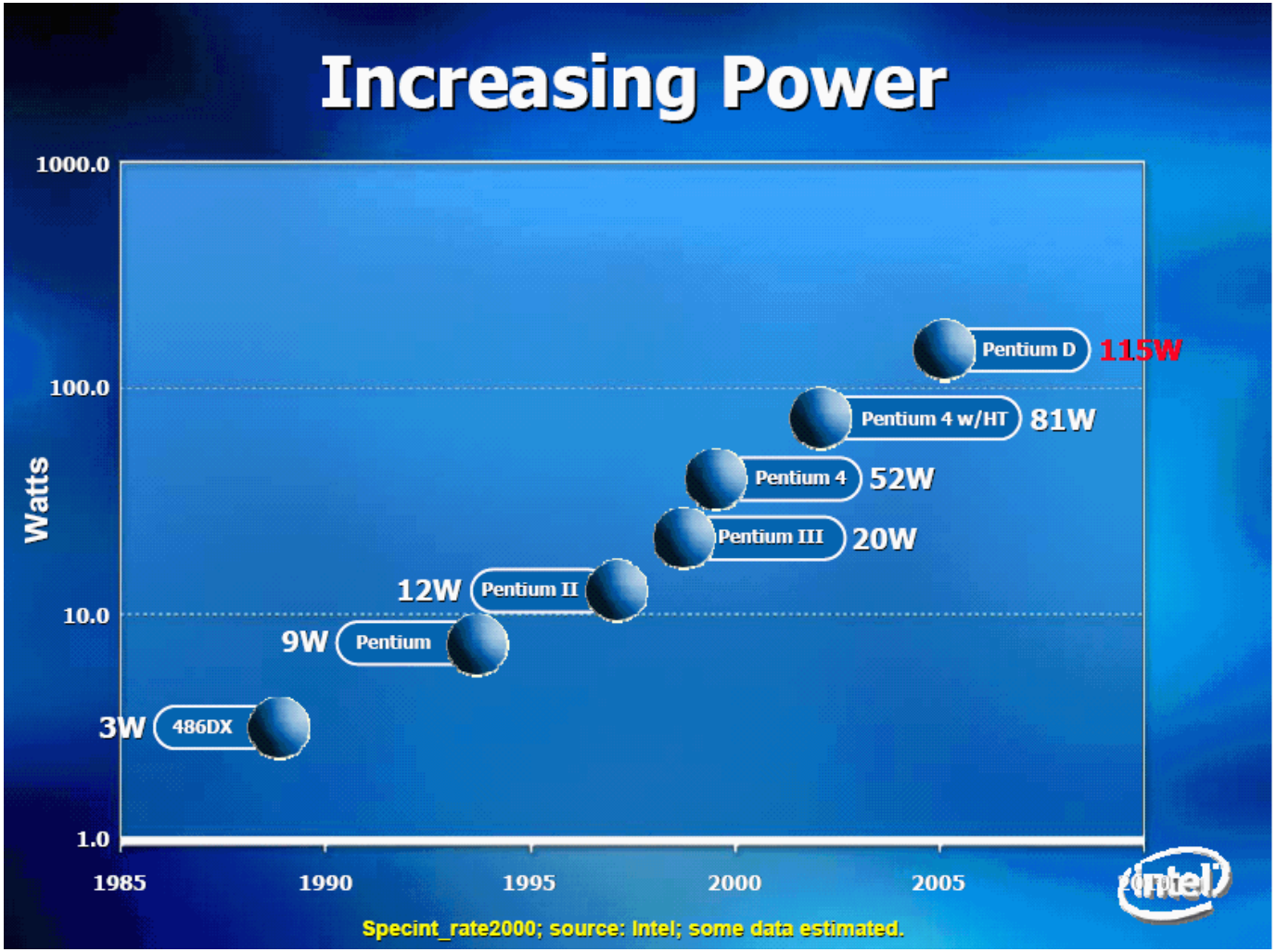


Power density too high to keep junction at low temperature.
Power reaching limits of air cooling.

Heat Management Consideration



Power Consumption Scenario



Some Calculations!

Power = 115 Watts

Supply Voltage = 1.2 V

Supply Current = 115 W / 1.2 V = 96 Amps!

Problem: Current density becomes a serious problem!

This is known as electromigration

Note: Fuses used for household appliances = 15 to 40 Amps

Another Calculations!

Power = 115 Watts

Chip Area = 2.2 Cm^2

Heat Flux = 115 W / 2.2 Cm^2 = 50 W/Cm^2 !

Problem: Heat flux is another serious issue!

Notes:

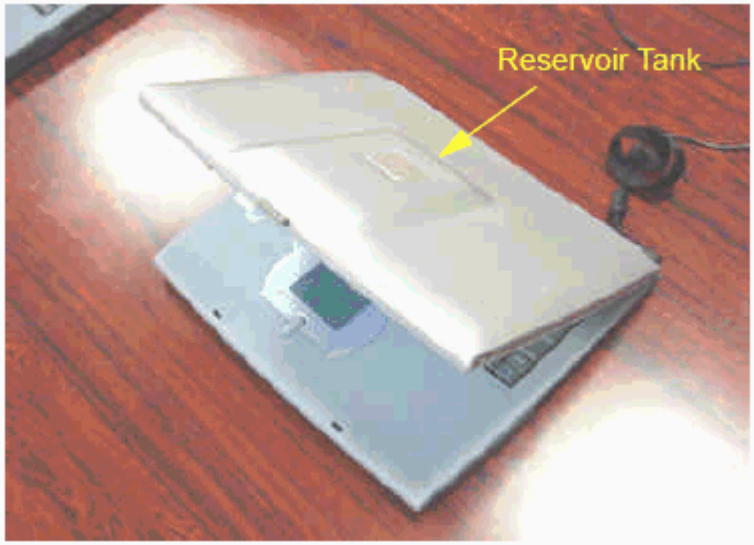
Heat flux in iron = 0.2 W/Cm^2

Heat flux in frying pan = 10 W/Cm^2

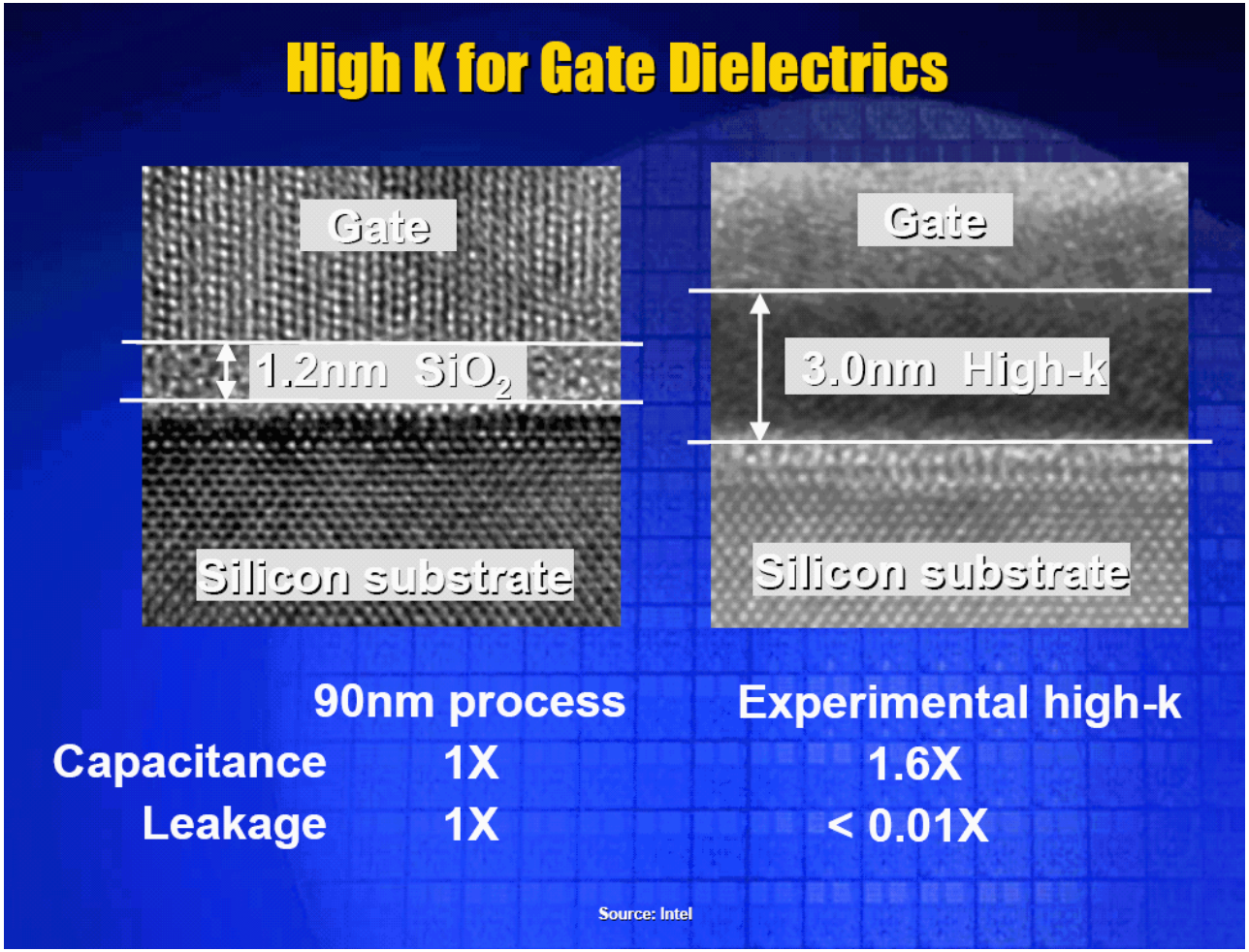
Method of Heat Management

1) **Proper heat removal system (expensive)**
2) **Improve manufacturing for low power MOS**
3) **Architectural solutions (multi-cores)**

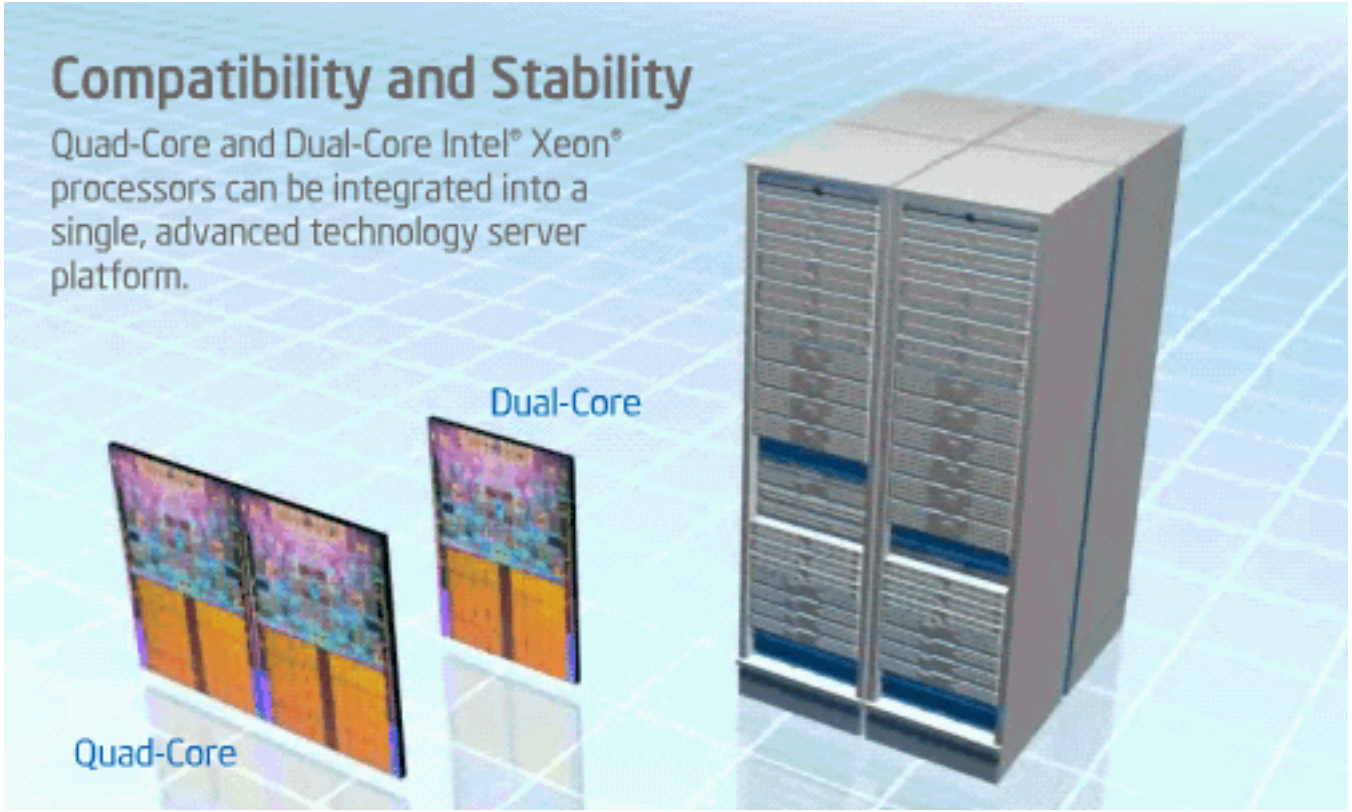
Hitachi Water Cooling Laptop



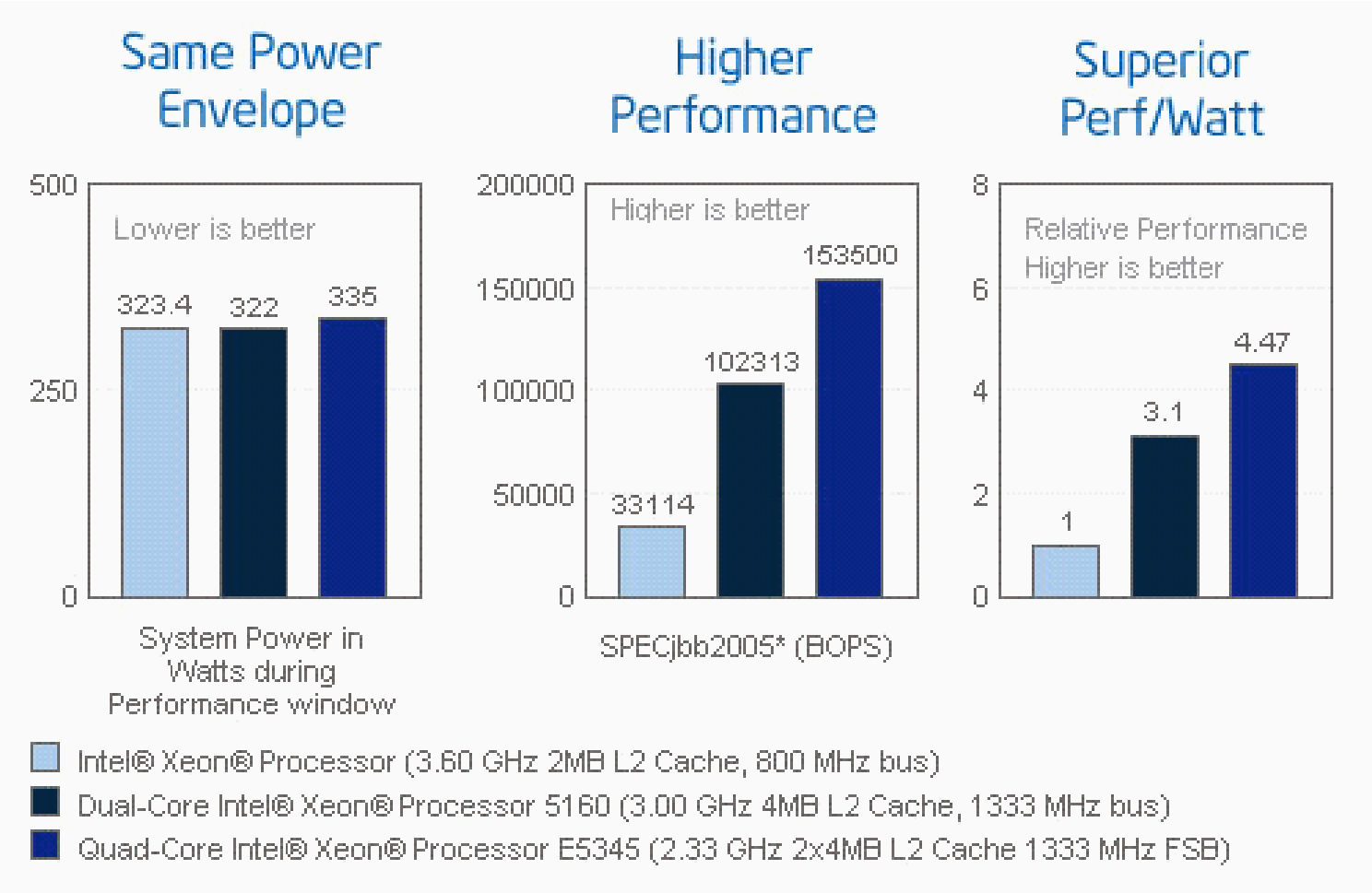
Manufacturing Solution



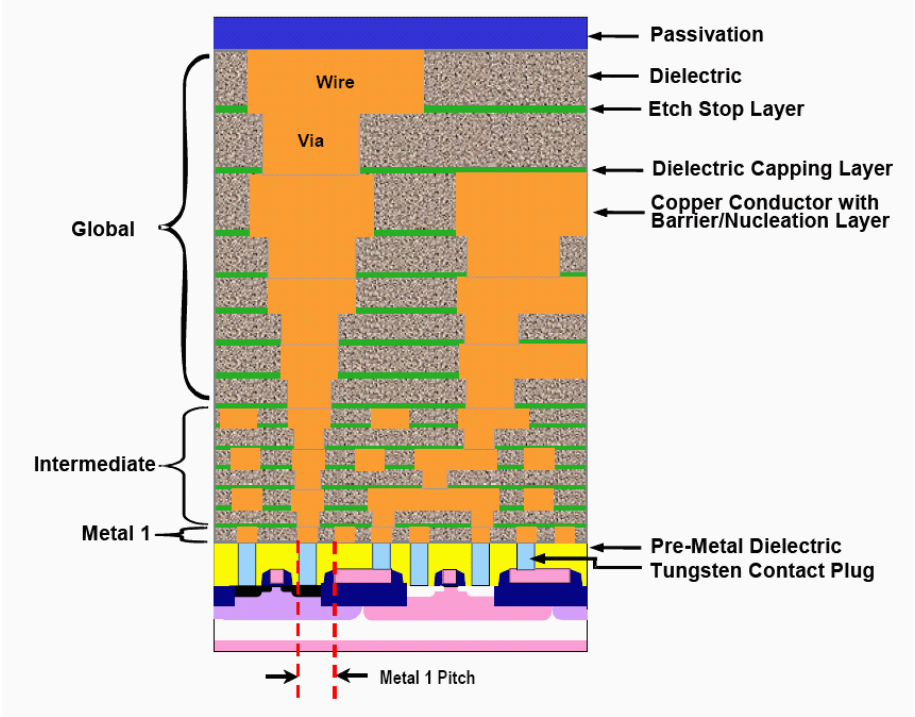
Architectural Solution



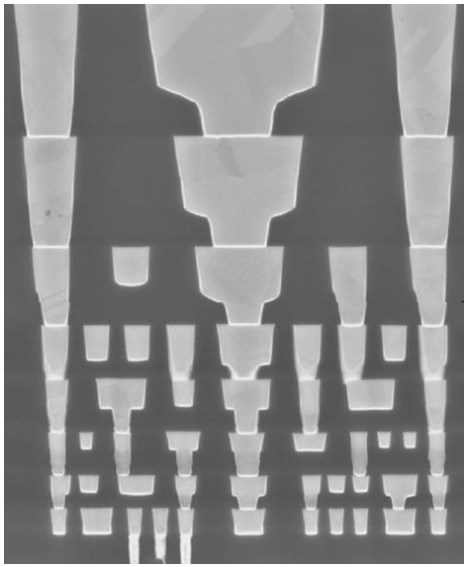
Architectural Solution



Interconnect Architecture



Metal stack over Silicon

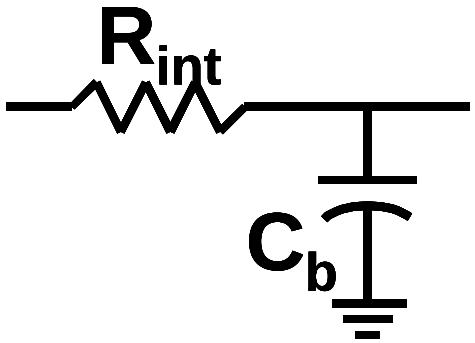


Real wiring cross section photograph

Interconnect Scaling Scenario

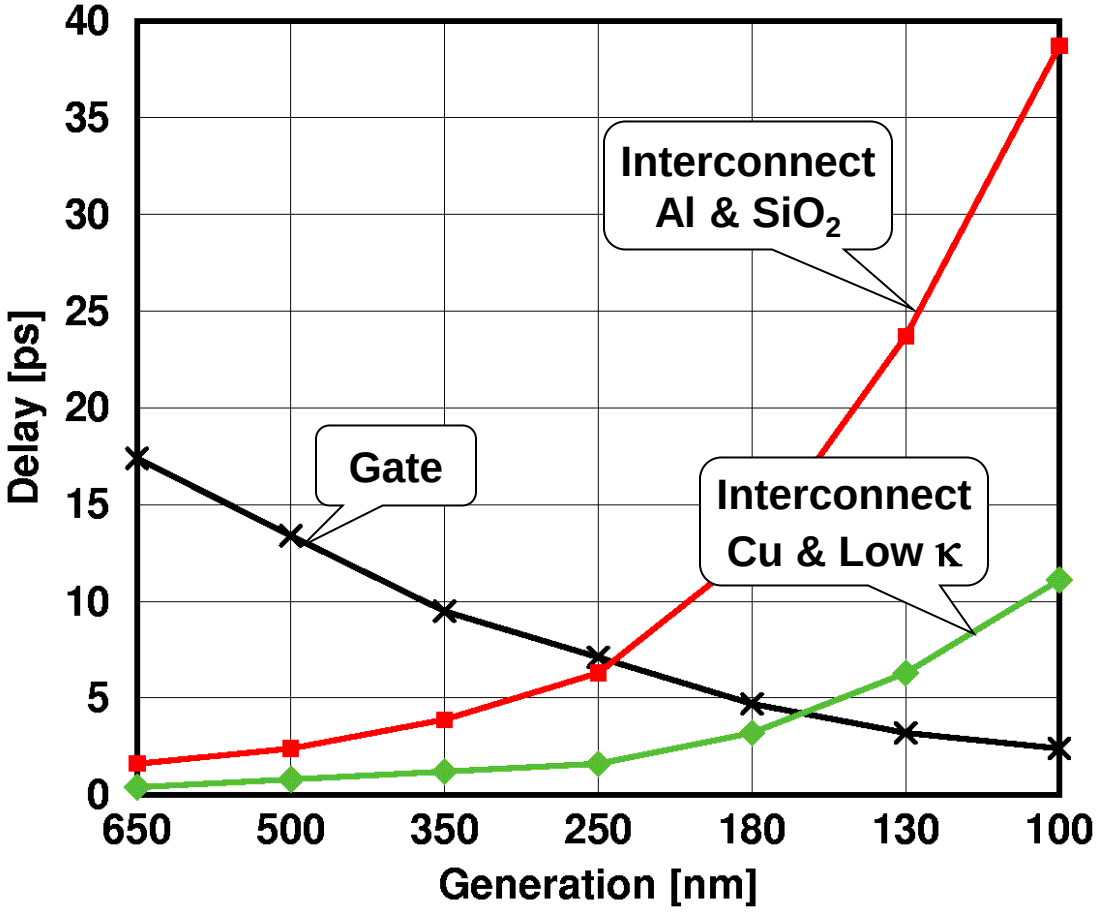
Technology	45 nm (2008)	35 nm (2010)	22 nm (2012)
Wire width	45 nm	32 nm	22 nm
Wire Thickness	80 nm	60 nm	40 nm
Total Number of Wires	150 Million	300 Million	600 Million
Total wire length	1.4 mile	2 mile	2.8 mile

Delay versus Interconnect Scaling



$$\text{Delay} \propto R_{int}\, C_b$$

Interconnect versus Gate Delay



[Bohr, IEDM '95]

Al	*3.0* μΩ cm
Cu	*1.7* μΩ cm
SiO_2	κ = *4.0*
Low κ	κ = *2.0*
Al & Cu	*0.8* μ *Thick*
Al & CU Line	*43* μ *Long*

Interconnect Challenges

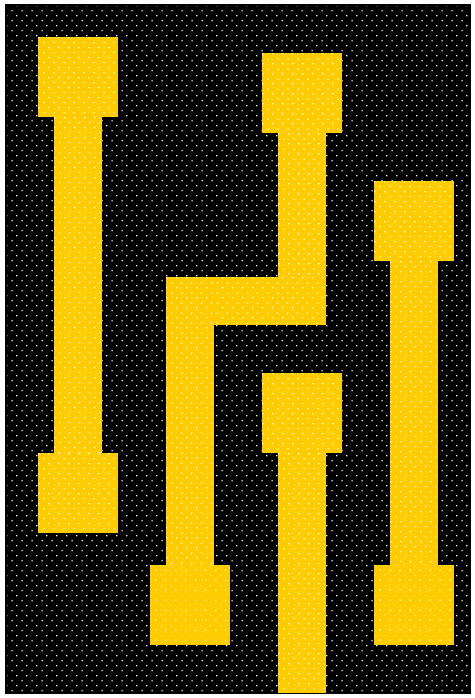
1) **Slows down with scaling**
2) **Consume more power**
3) **Generate more heat**
4) **Electromigration**

Far-future Alternative Interconnects

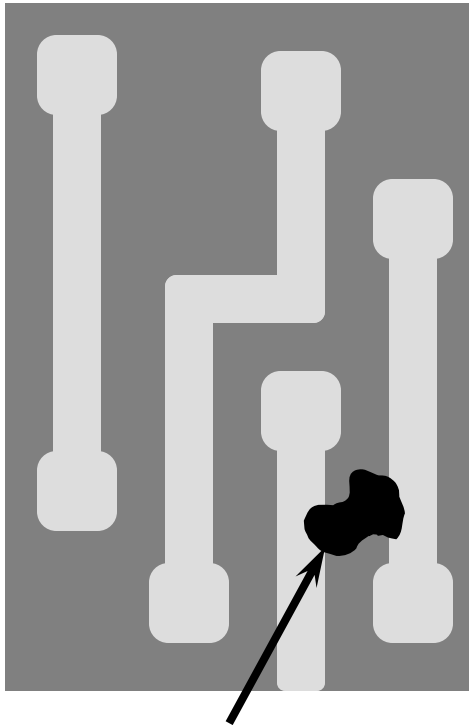
1) **Carbon nanotubes**
2) **Optical Interconnect**
3) **Molecular wires**
4) **Spintronics interconnect system**

Process Defects and Yield Loss

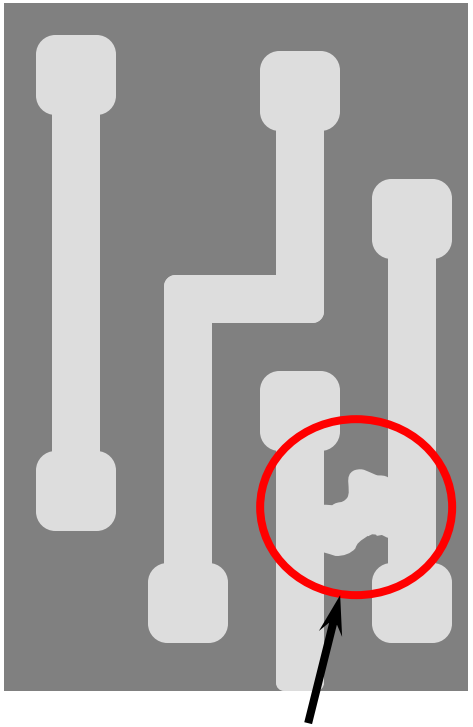
Process Defect Causing Fault (Short)



Original layout



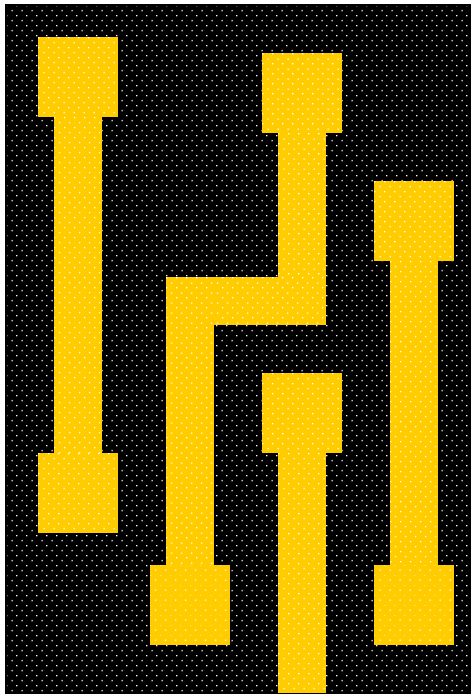
A particle or
a process defect



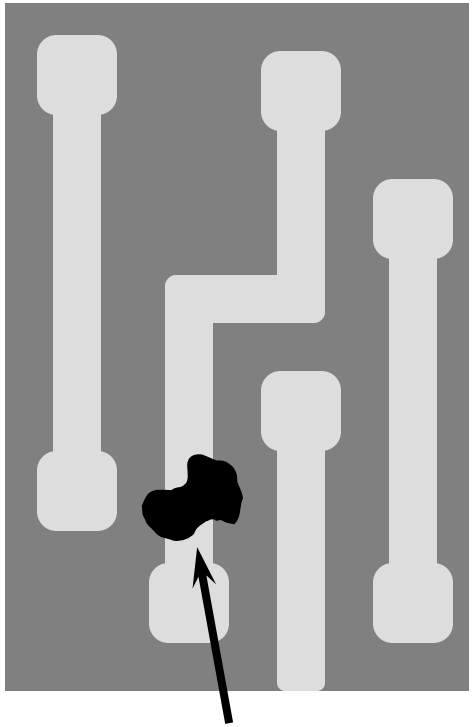
Short defect

Process Defects and Yield Loss

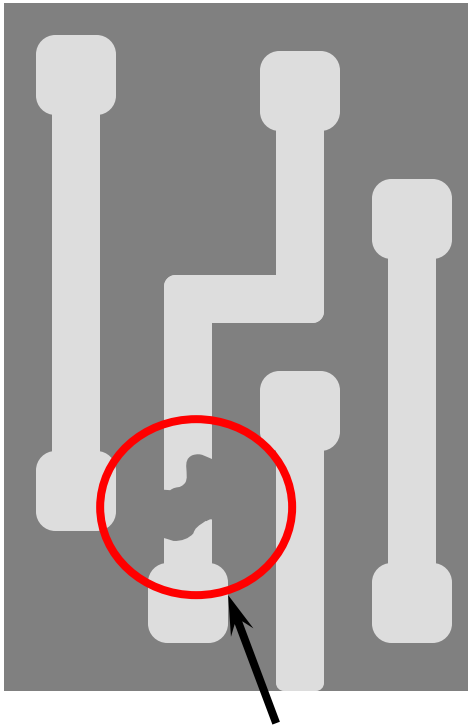
Process Defect Causing Fault (Opens)



Original layout

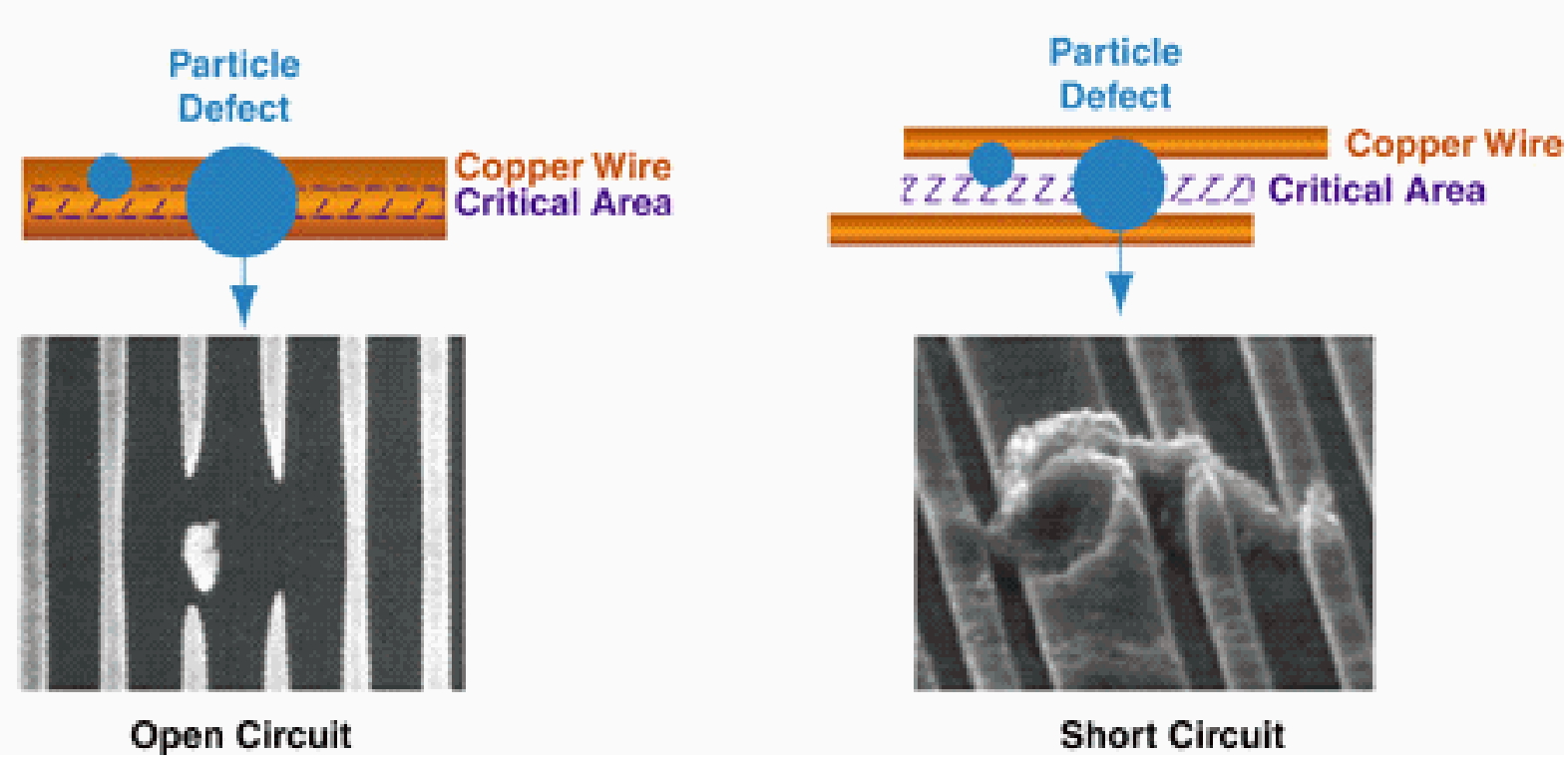


A particle or
a process defect



open defect

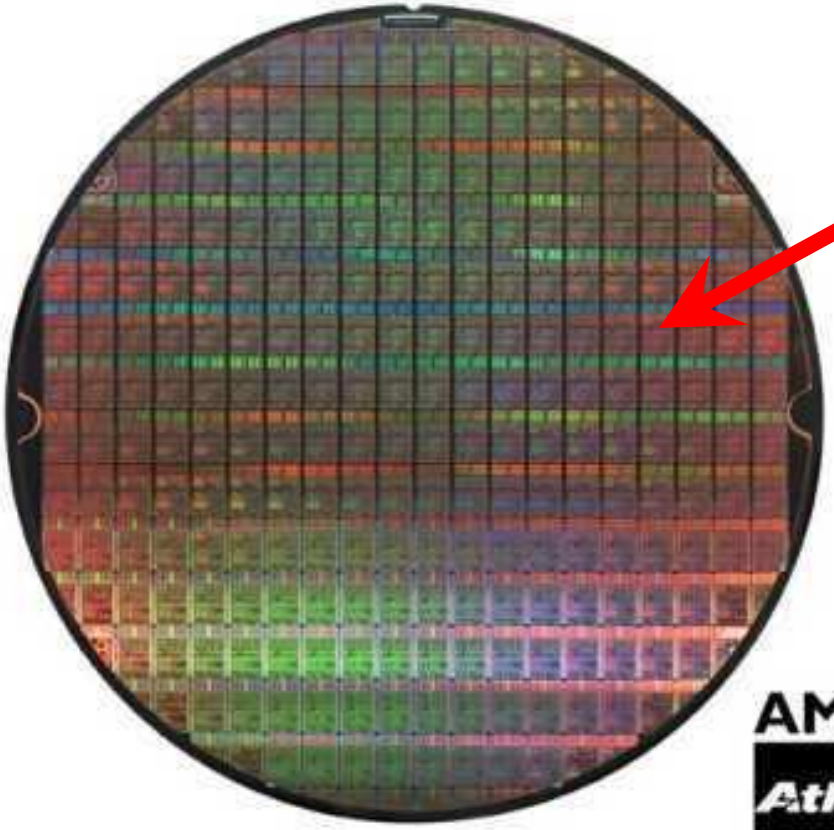
Process Defect Photograph



Manufacturing Issues

1) **Smaller feature size requires ultra-clean manufacturing facility (expensive)**
2) **Because of the increase in complexity, defects could drastically reduces the manufacturing yield (% of working chips)**
3) **There are much more issues related to "Design for Manufacturability" (DFM)**

Die Cost



Single die

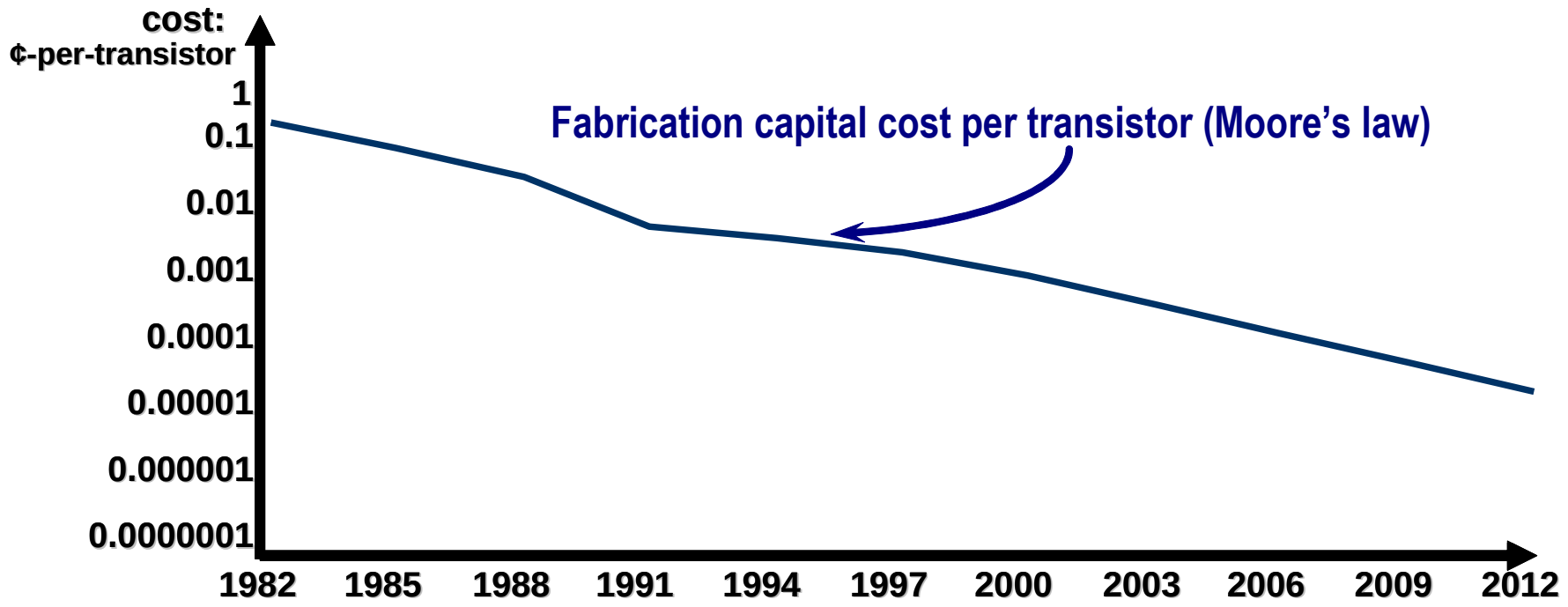
Wafer

AMD Athlon

Going up to 12" (30cm)

From http://www.amd.com

Cost per Transistor



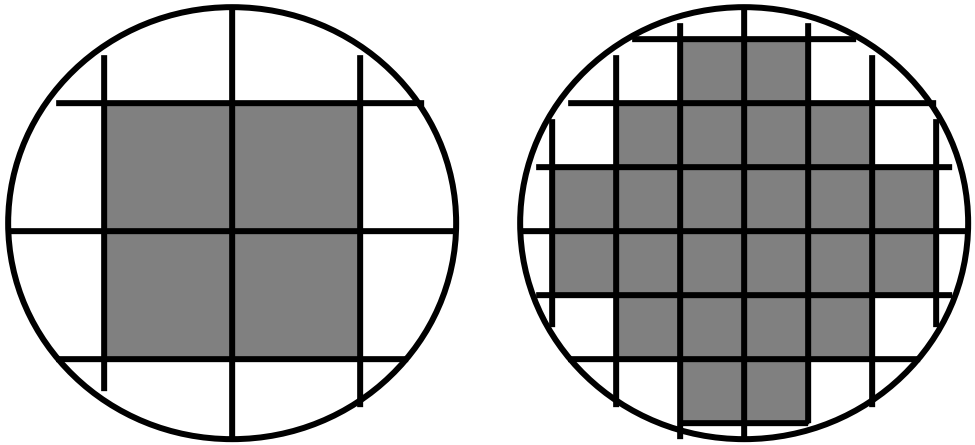
Cost per transistor is reducing exponentially following Moor's law.

Yield

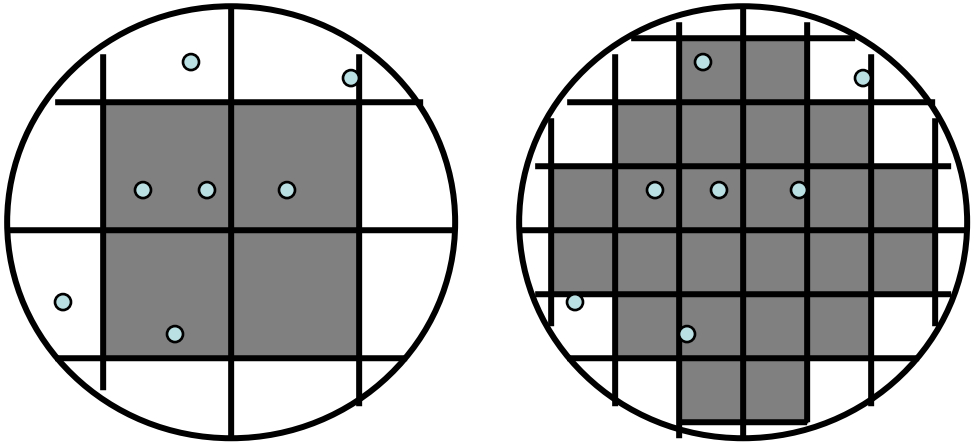
$$Y = \frac{\text{No. of good chips per wafer}}{\text{Total number of chips per wafer}} \times 100\%$$

$$\text{Die cost} = \frac{\text{Wafer cost}}{\text{Dies per wafer} \times \text{Die yield}}$$

$$\text{Dies per wafer} = \frac{\pi \times (\text{wafer diameter}/2)^2}{\text{die area}} - \frac{\pi \times \text{wafer diameter}}{\sqrt{2 \times \text{die area}}}$$



Defects and Die Cost



$$\text{die yield} = \left(1 + \frac{\text{defects per unit area} \times \text{die area}}{\alpha}\right)^{-\alpha}$$

α is approximately 3

$$\text{die cost} = f(\text{die area})^4$$

Some Examples (1994)

Chip	Metal layers	Line width	Wafer cost	Def./ cm^2	Area mm^2	Dies/ wafer	Yield	Die cost
386DX	2	0.90	$900	1.0	43	360	71%	$4
486 DX2	3	0.80	$1200	1.0	81	181	54%	$12
Power PC 601	4	0.80	$1700	1.3	121	115	28%	$53
HP PA 7100	3	0.80	$1300	1.0	196	66	27%	$73
DEC Alpha	3	0.70	$1500	1.2	234	53	19%	$149
Super Sparc	3	0.70	$1700	1.6	256	48	13%	$272
Pentium	3	0.80	$1500	1.5	296	40	9%	$417

Summary

Digital IC Business is Unique

- Things Get Better Every Few Years
- Companies Have to Stay on Moore's Law Curve to Survive

Benefits of Transistor Scaling

- Higher Frequencies of Operation
- Massive Functional Units, Increasing On-Die Memory
- Cost/Functionality Going Down

Downside of Transistor Scaling

- Power (Dynamic and Static)
- Design and Manufacturing Cost
- ….