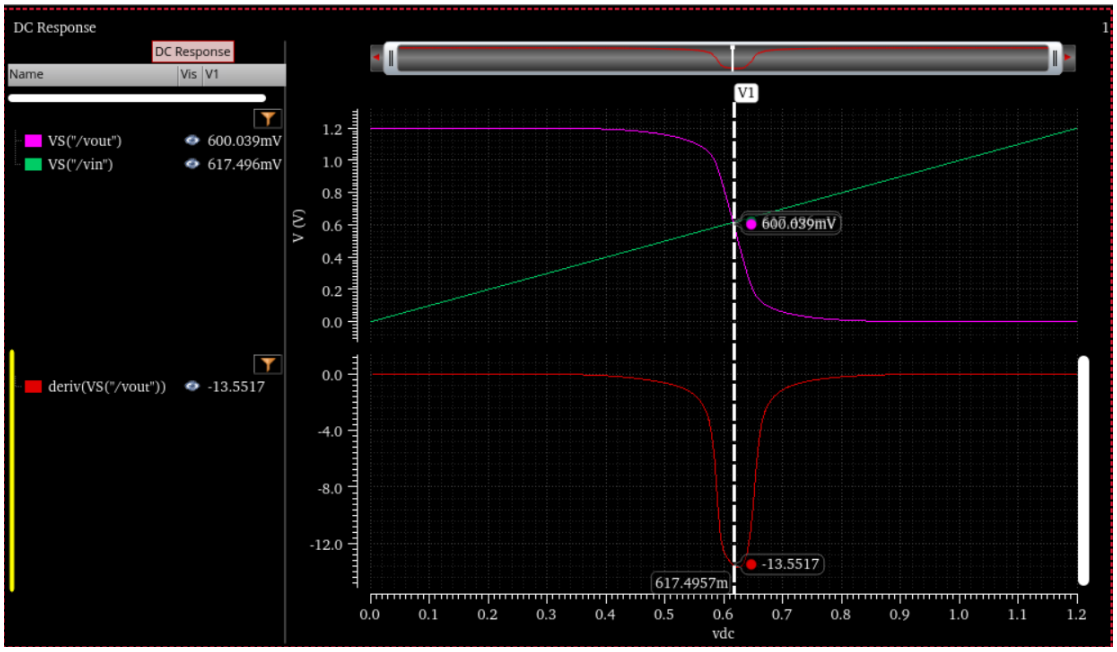
EECS 413 LAB1

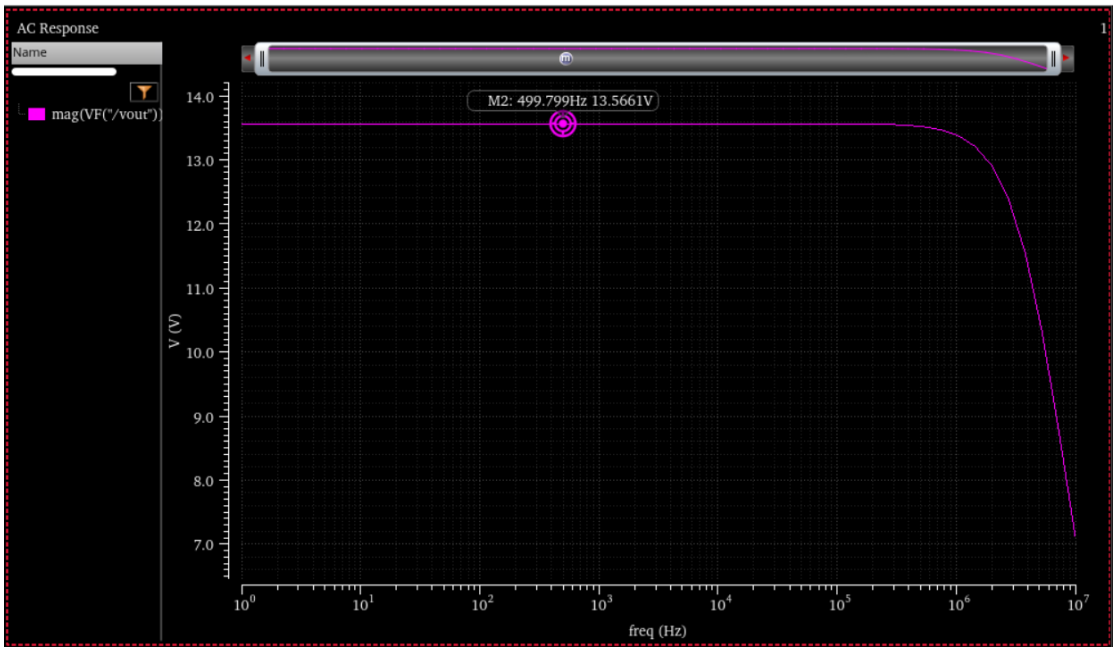
Hsiang-Yang Fan

1.

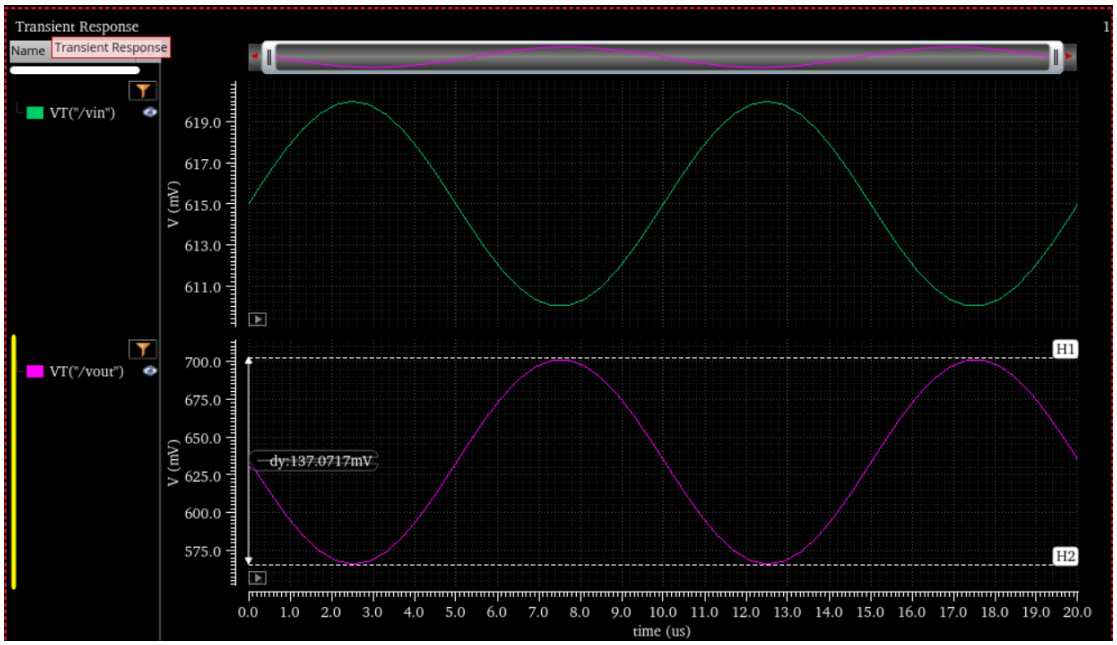
- Figure 2&3



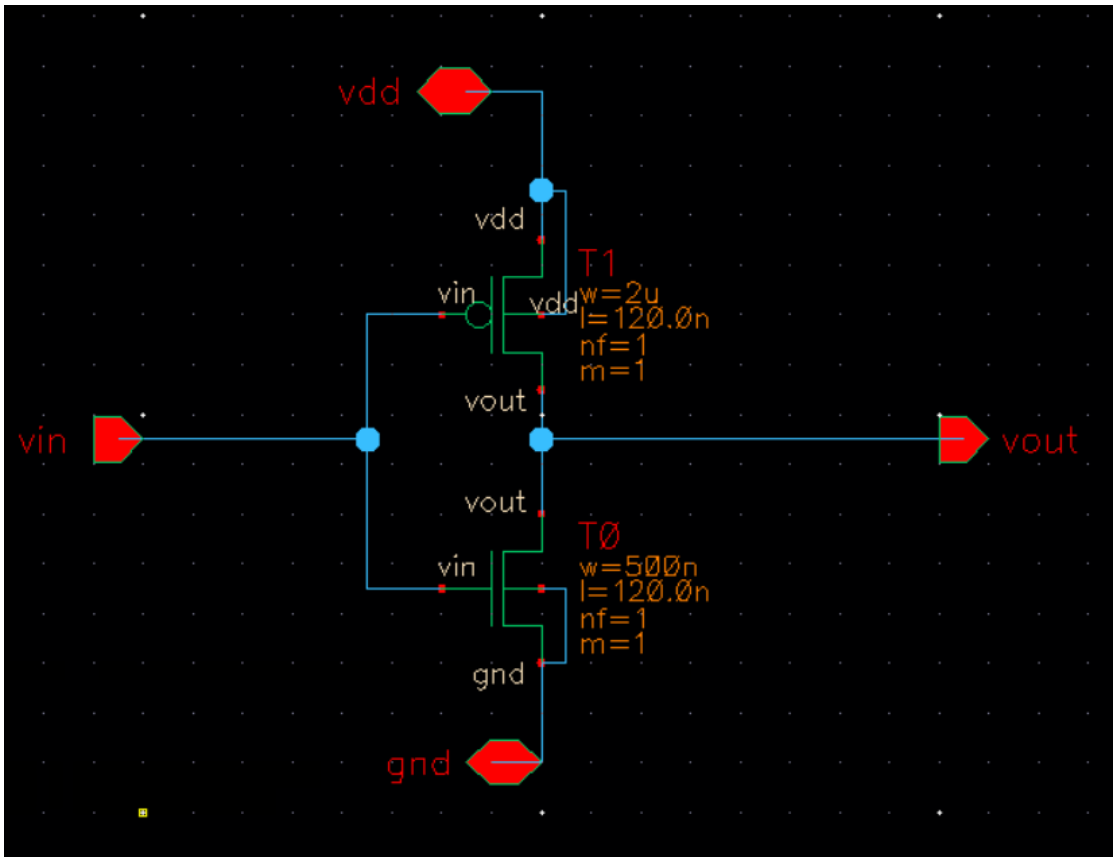
- Figure 4



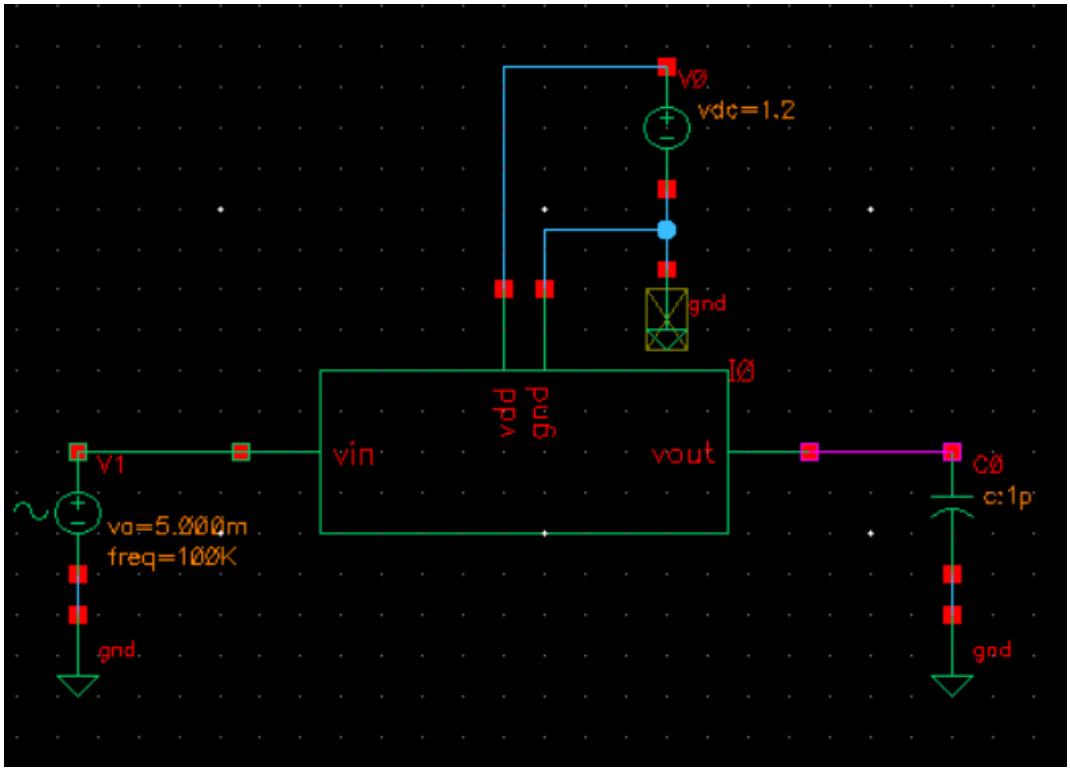
- Figure 5



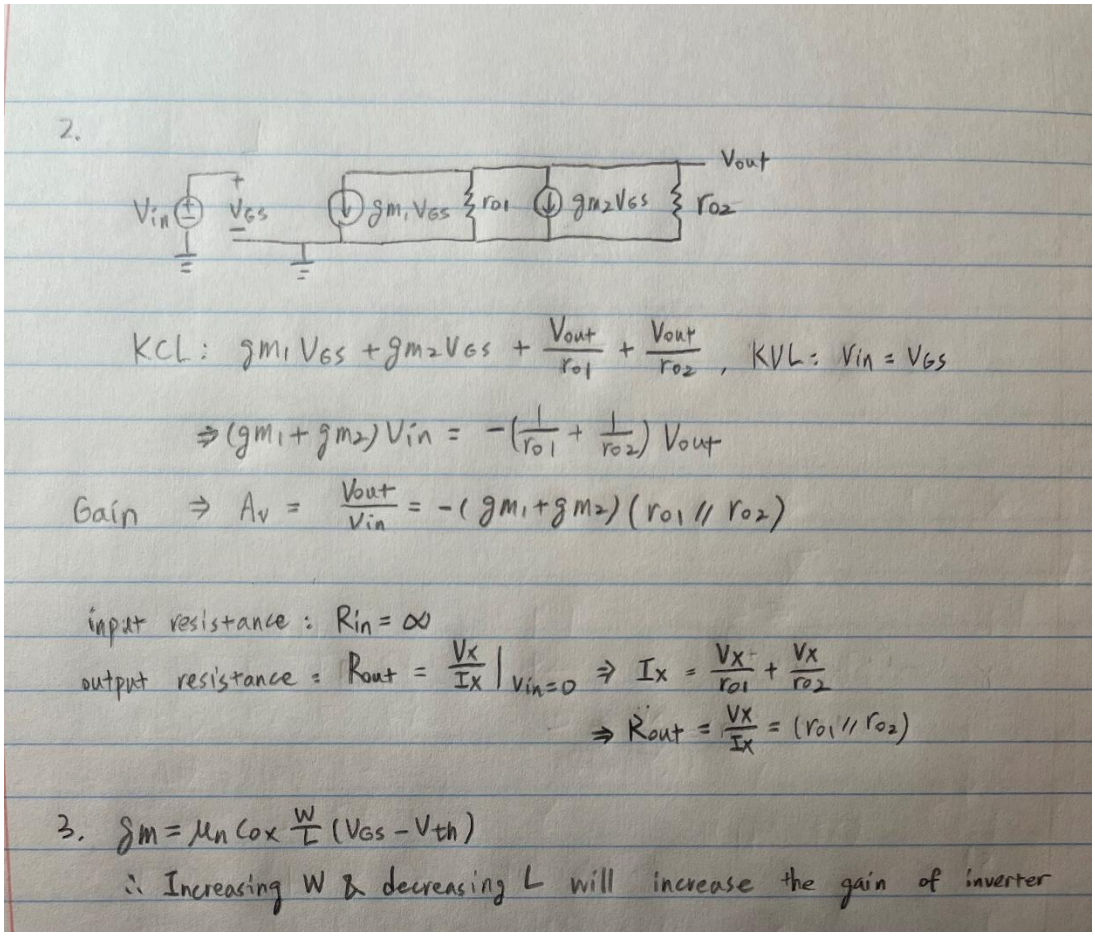
- Figure 6



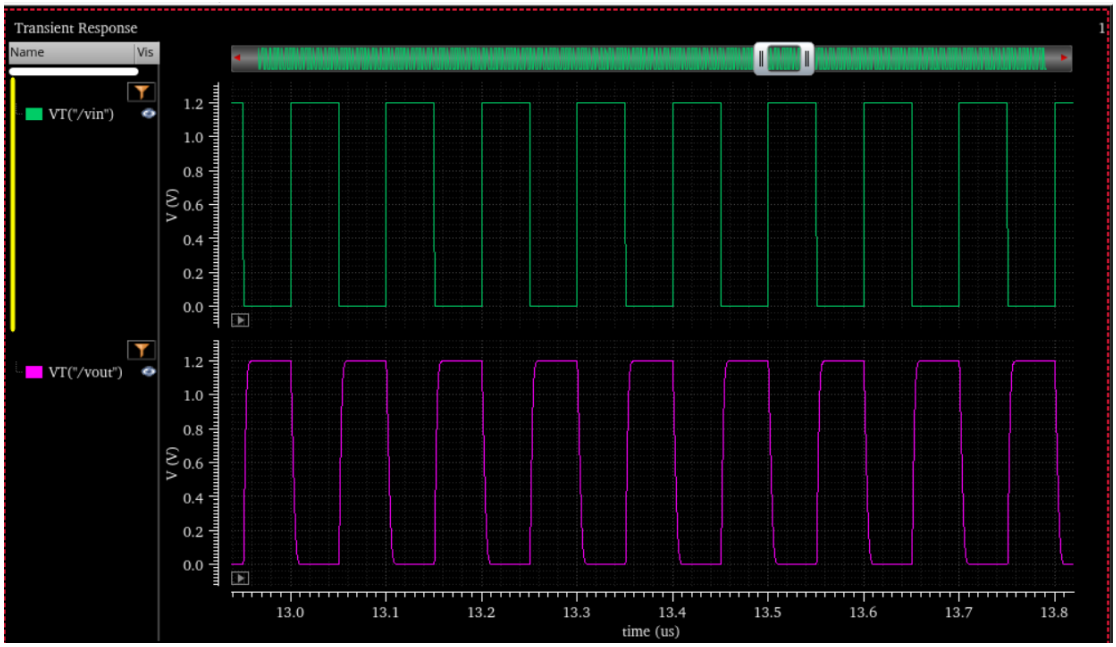
- Figure 8


V0
vdc=1.2
gnd
I0
vdd
ppa
vin
vout
V1
va=5.000m
freq=100K
gnd.
C0
c:1p
gnd

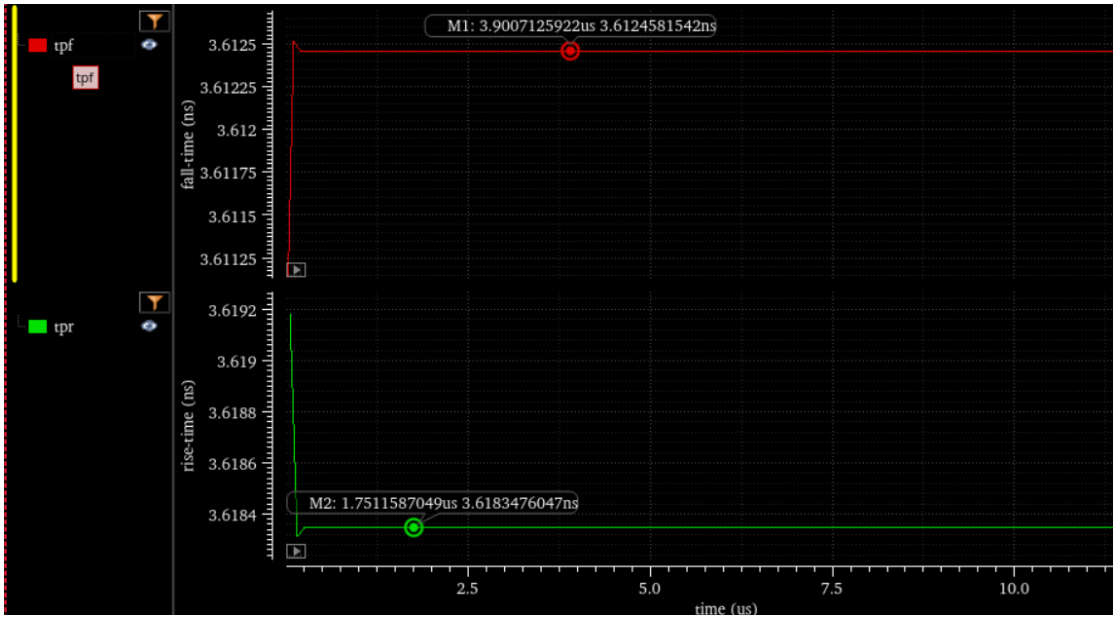
2.


2.
Vout
Vin
VGS
gm1VGS
ro1
gm2VGS
ro2
KCL: gm1VGS + gm2VGS + Vout/ro1 + Vout/ro2, KVL: Vin = VGS
⇒ (gm1 + gm2) Vin = −(1/ro1 + 1/ro2) Vout
Gain ⇒ Av = Vout/Vin = −(gm1 + gm2)(ro1 // ro2)
input resistance : Rin = ∞
output resistance : Rout = Vx/Ix |Vin=0 ⇒ Ix = Vx/ro1 + Vx/ro2
⇒ Rout = Vx/Ix = (ro1 // ro2)
3. gm = μn Cox W/L (VGS − Vth)
∴ Increasing W & decreasing L will increase the gain of inverter

4. Input & Output pulse waveforms

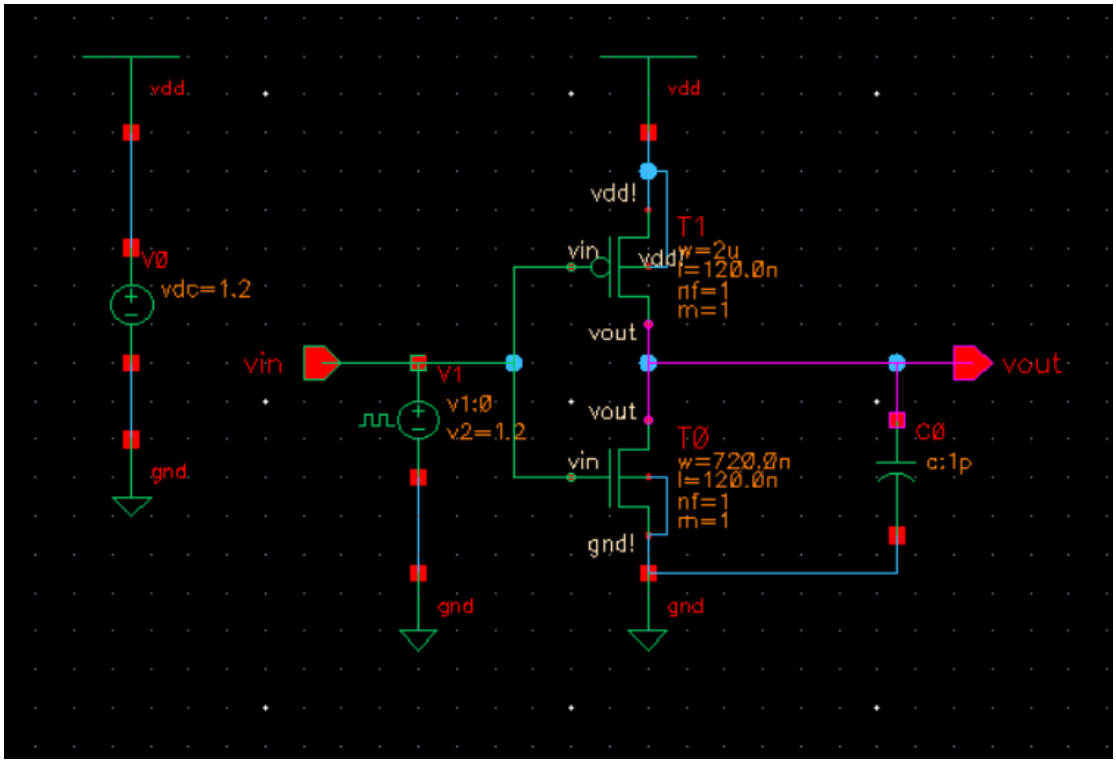


5. Rise time, Fall time and Circuit



	time (s)	riseTime(...me") (s)
1	51.16E-9	3.619E-9
2	151.2E-9	3.618E-9
3	251.2E-9	3.618E-9
4	351.2E-9	3.618E-9
5	451.2E-9	3.618E-9
6	551.2E-9	3.618E-9
7	651.2E-9	3.618E-9
8	751.2E-9	3.618E-9
9	851.2E-9	3.618E-9
10	951.2E-9	3.618E-9
11	1.051E-6	3.618E-9
12	1.151E-6	3.618E-9
13	1.251E-6	3.618E-9
14	1.351E-6	3.618E-9
15	1.451E-6	3.618E-9
16	1.551E-6	3.618E-9
17	1.651E-6	3.618E-9
18	1.751E-6	3.618E-9
19	1.851E-6	3.618E-9
20	1.951E-6	3.618E-9
21	2.051E-6	3.618E-9
22	2.151E-6	3.618E-9

	time (s)	fallTime(...ime") (s)
1	700.7E-12	3.611E-9
2	100.7E-9	3.613E-9
3	200.7E-9	3.612E-9
4	300.7E-9	3.612E-9
5	400.7E-9	3.612E-9
6	500.7E-9	3.612E-9
7	600.7E-9	3.612E-9
8	700.7E-9	3.612E-9
9	800.7E-9	3.612E-9
10	900.7E-9	3.612E-9
11	1.001E-6	3.612E-9
12	1.101E-6	3.612E-9
13	1.201E-6	3.612E-9
14	1.301E-6	3.612E-9
15	1.401E-6	3.612E-9
16	1.501E-6	3.612E-9
17	1.601E-6	3.612E-9
18	1.701E-6	3.612E-9
19	1.801E-6	3.612E-9
20	1.901E-6	3.612E-9
21	2.001E-6	3.612E-9
22	2.101E-6	3.612E-9



6.

(1) At the beginning, the fall time is larger than the rise time. The width of NMOS needs to be longer in order to decrease the fall time value. Finally, the PMOS W/L is unchanged 2u/120nm, and NMOS W/L is changed to 720nm/120nm.

(2) Due to the capacitor, PMOS charges the capacitor from 0 to 1, hence PMOS determines the rise time. NMOS lets the capacitor to drain from 1 to 0, NMOS determines the fall time.