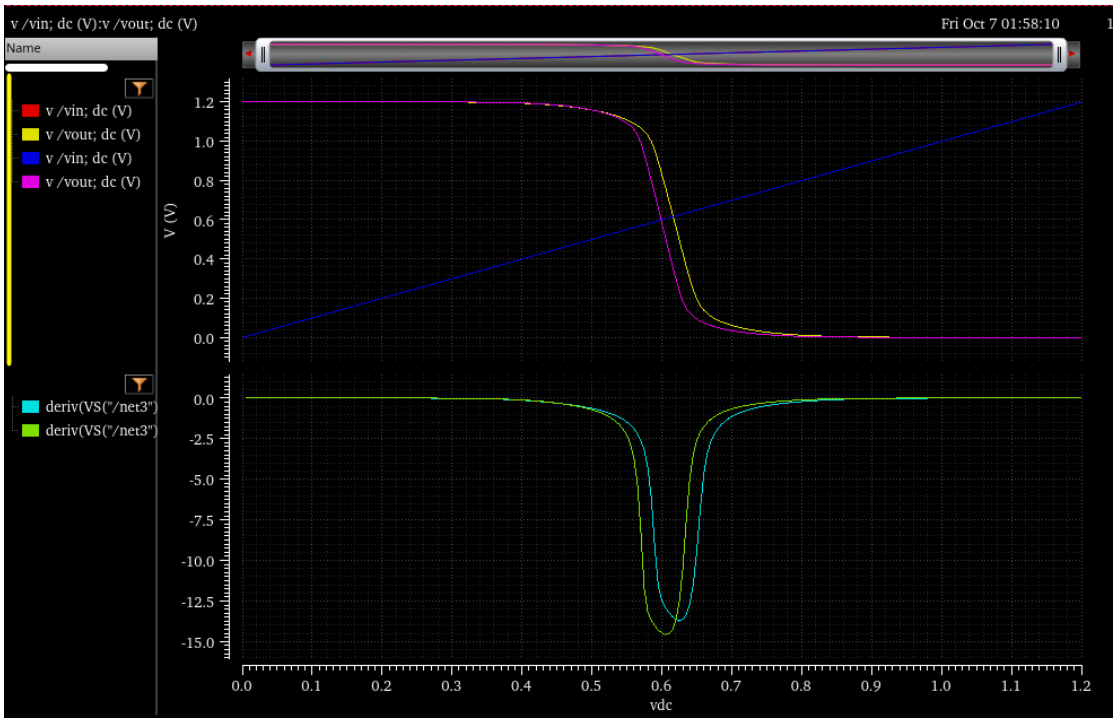
EECS 413 LAB2

Hsiang-Yang Fan

1.

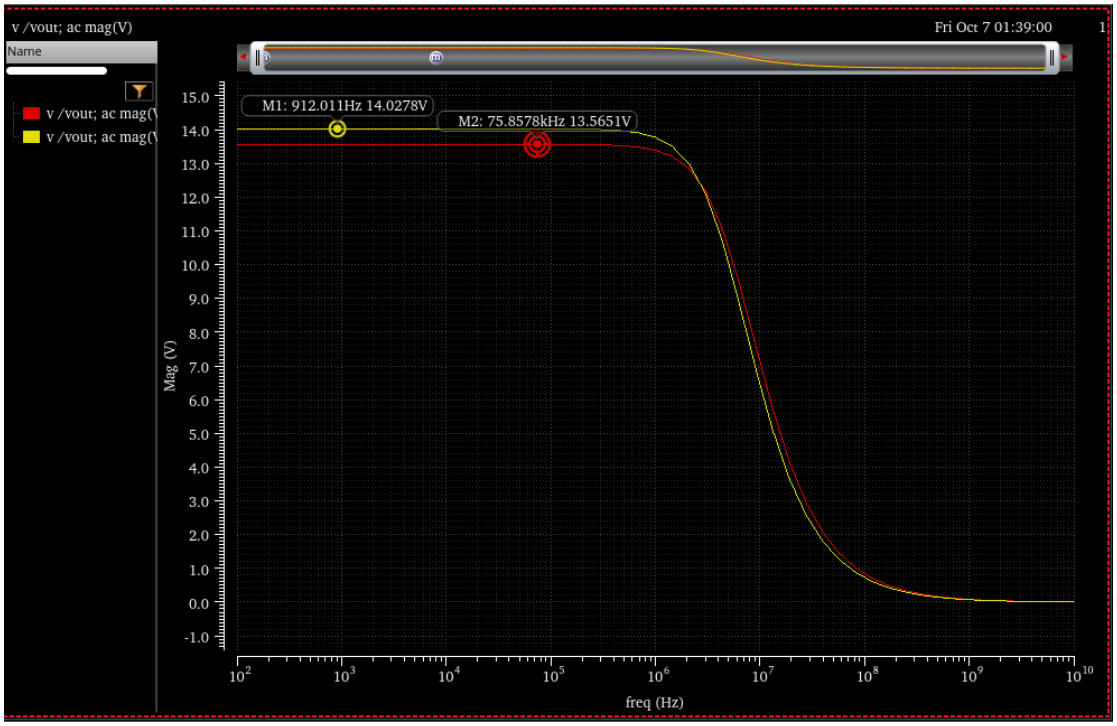
- Figure 3 (DC transfer characteristics):

The yellow line is Vin of schematic results, and the pink line is Vin of PEX results.



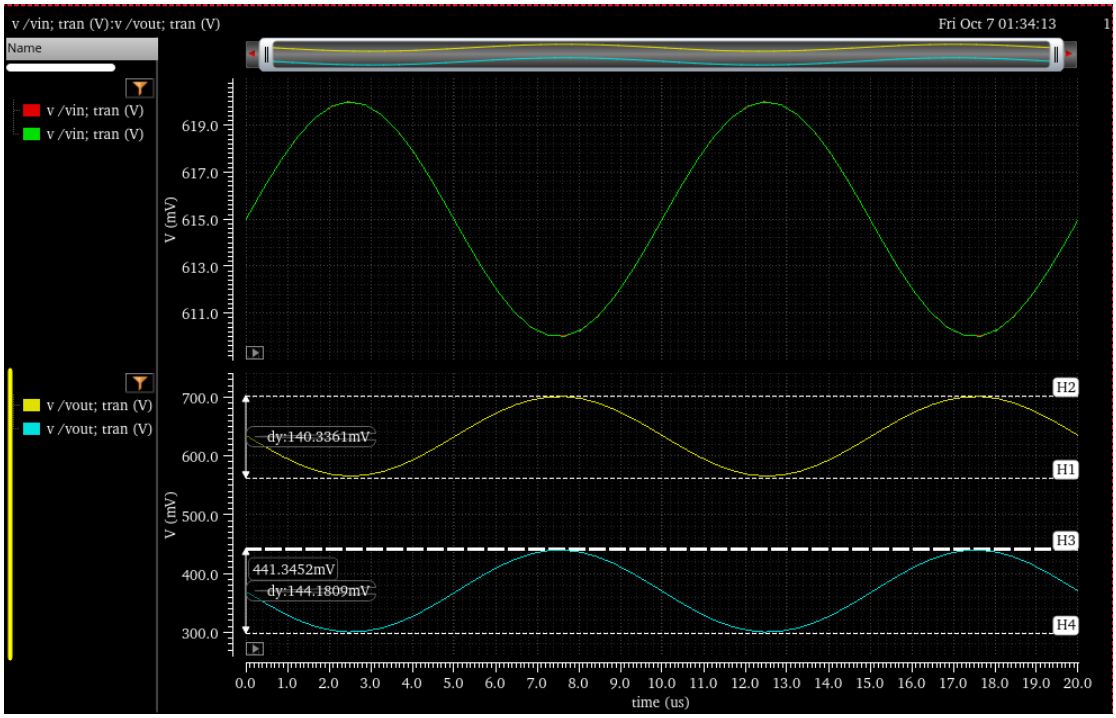
- Figure 4 (AC transfer characteristics):

The red line is Vout of schematic results, and the yellow line is Vout of PEX results.

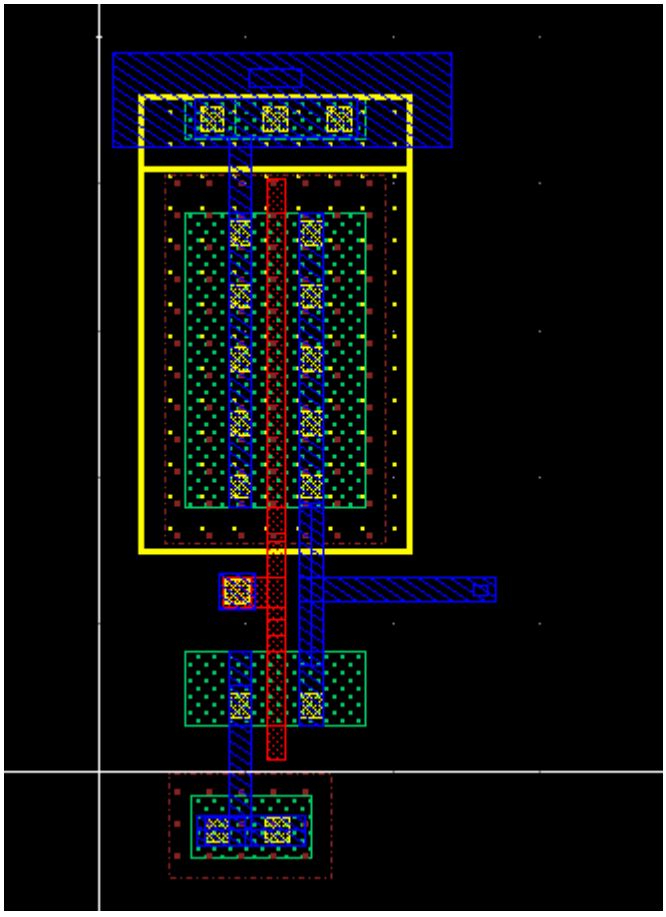


- Figure 5 (Transient characteristics):

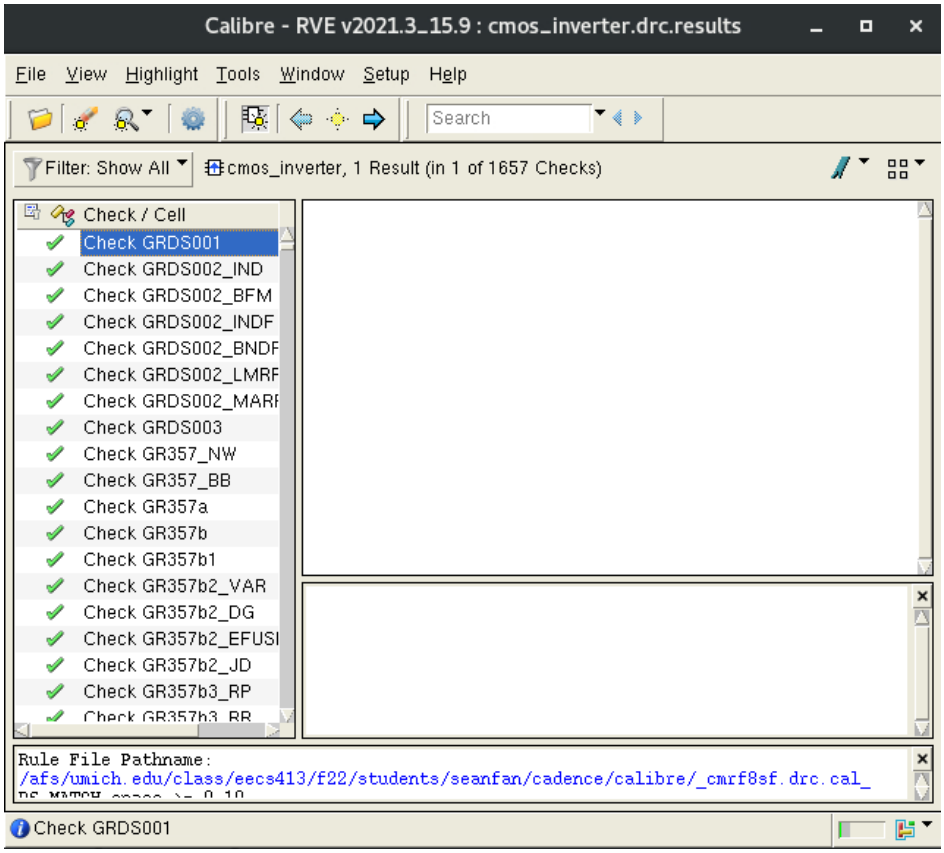
The yellow line is Vout of schematic results, and the blue line is Vout of PEX results.



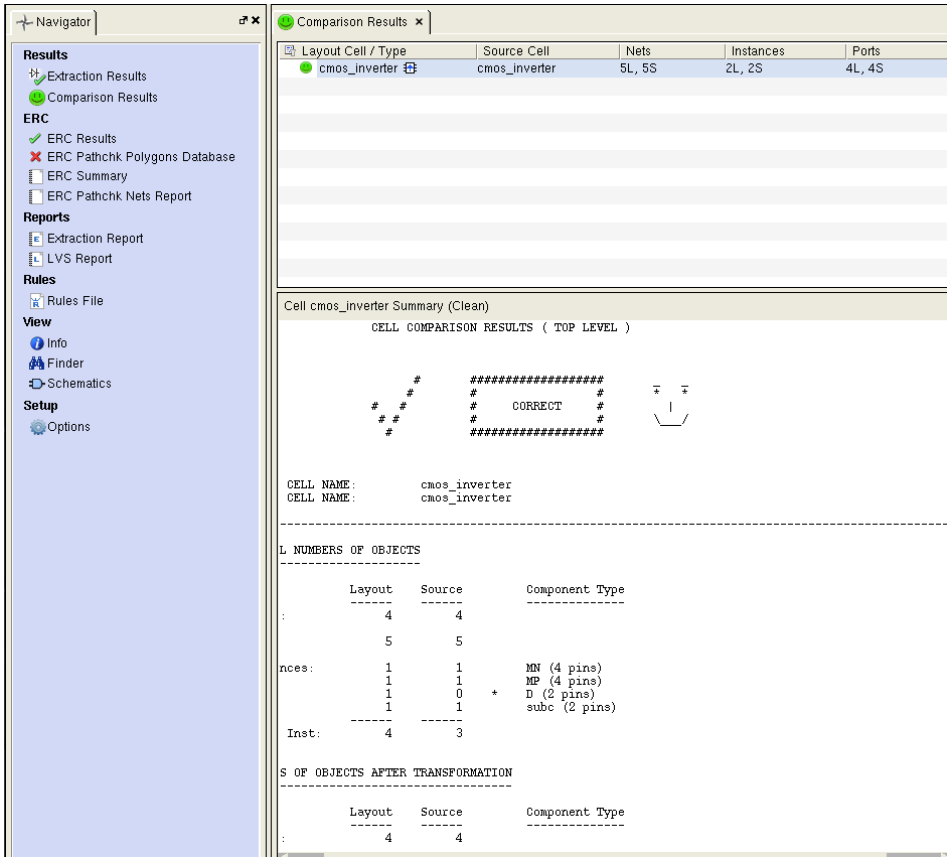
- Layout figure



- DRC result window



- LVS result window



2.

The widths of the geometries defined on a mask must exceed a minimum value imposed by both lithography and the processing capabilities of the technology. In general, the thicker a layer, the greater its minimum allowable width, indicating that as technologies scale, the thickness must be decreased proportionally.

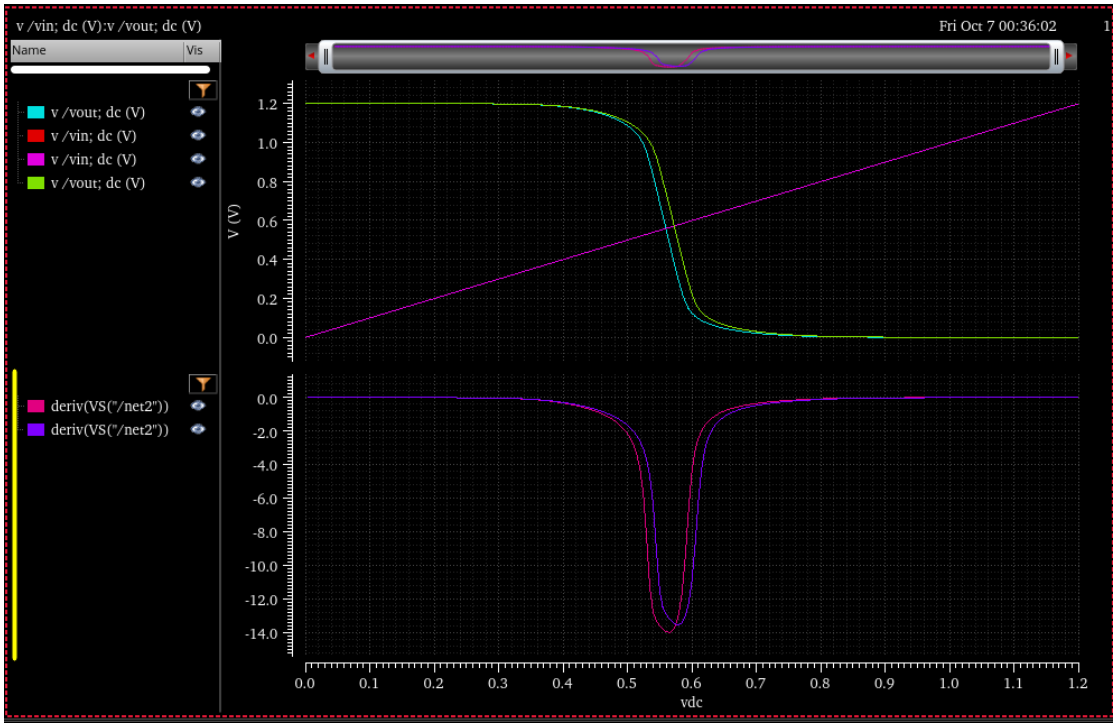
3.

Make the metal wider can lower the parasitic inductance and parasitic resistance. If draw the metal in VDD and GND wider can reduce the resistive loss.

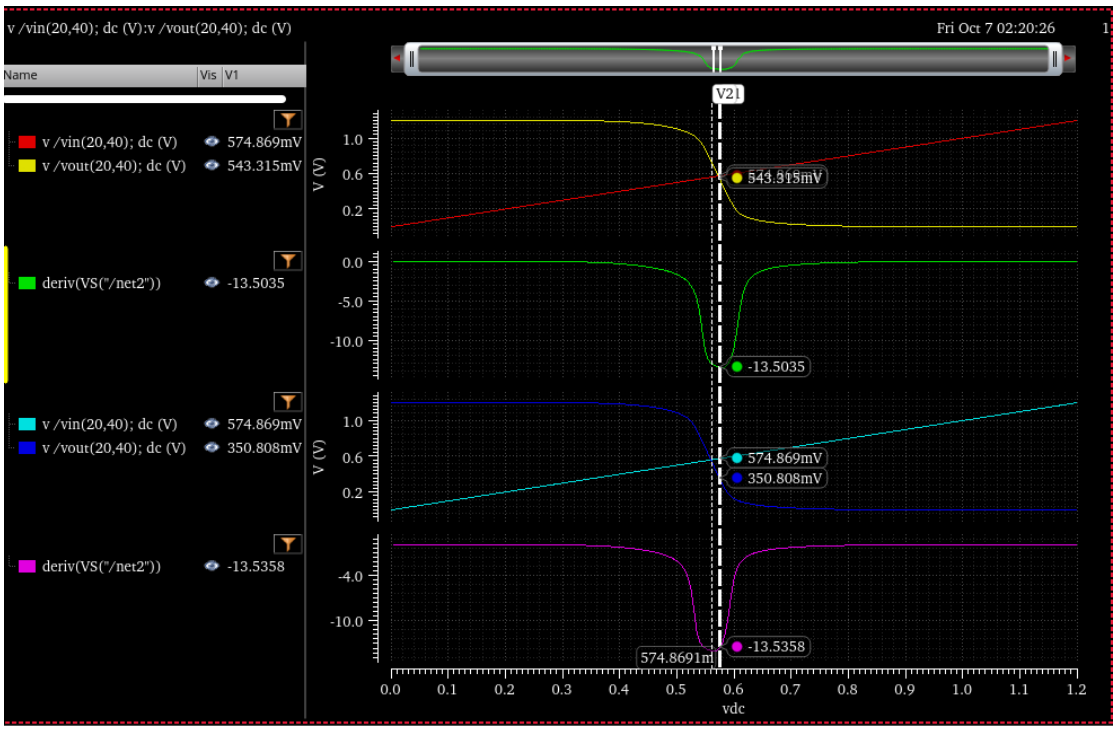
4.

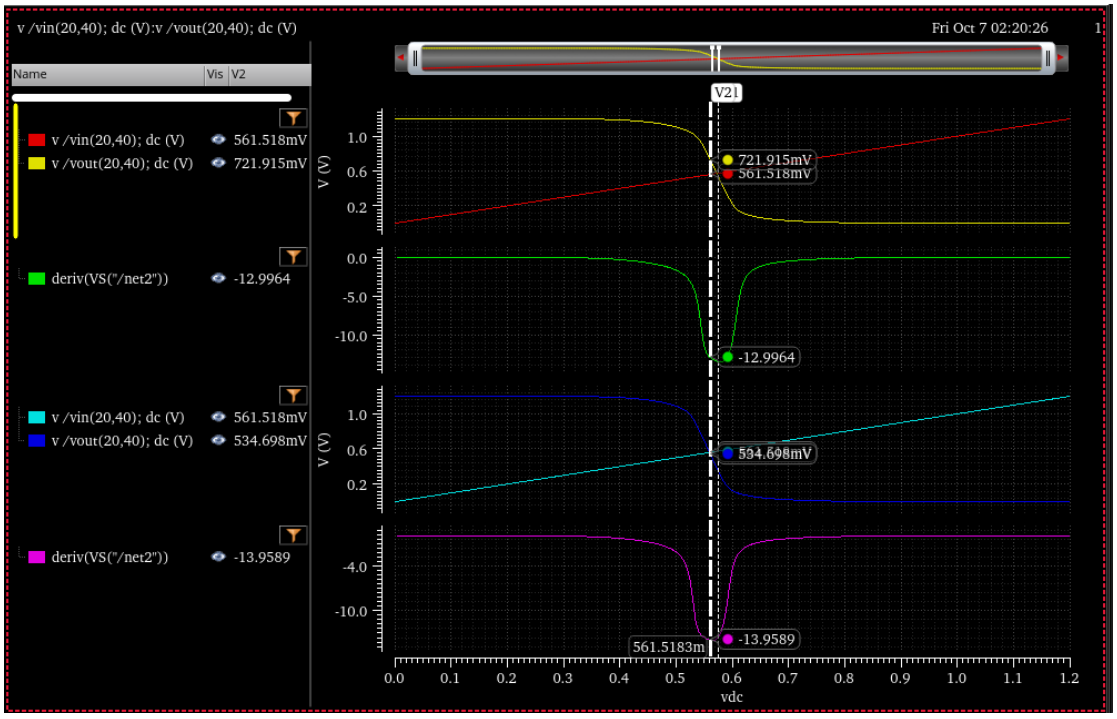
a. DC transfer characteristics of NMOS = 20um, PMOS = 40um

The green line is Vin of schematic results. The blue line is Vin of PEX results.



b. The yellow line is Vin and the green line is the gain = -13.5 of schematic results.
The blue line is Vin and the pink line is the gain = -13.96 of PEX results.

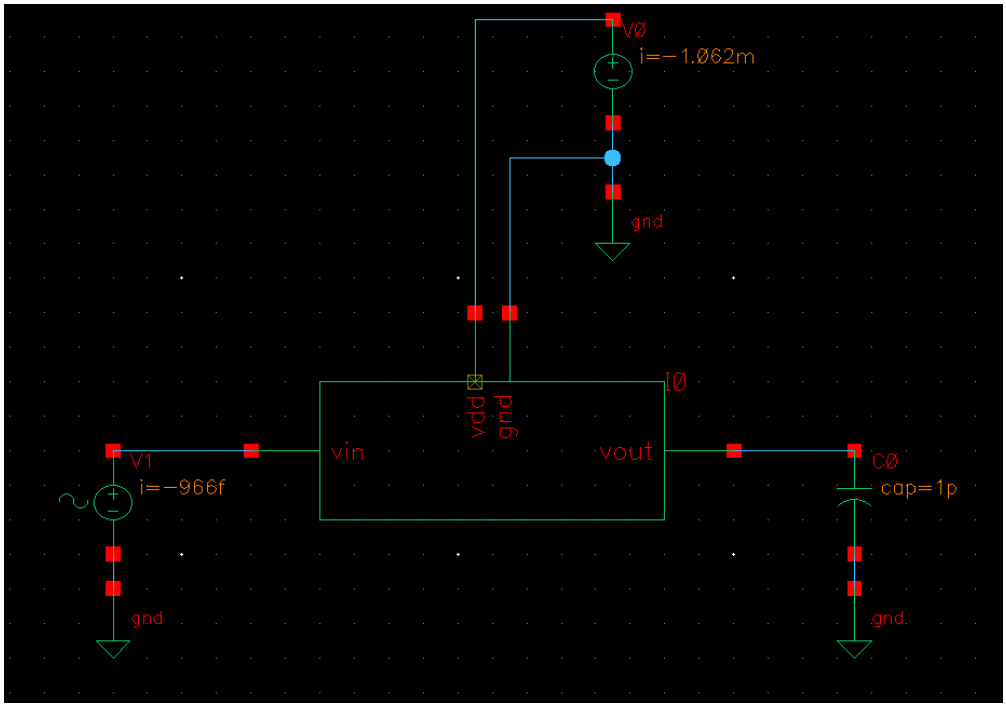




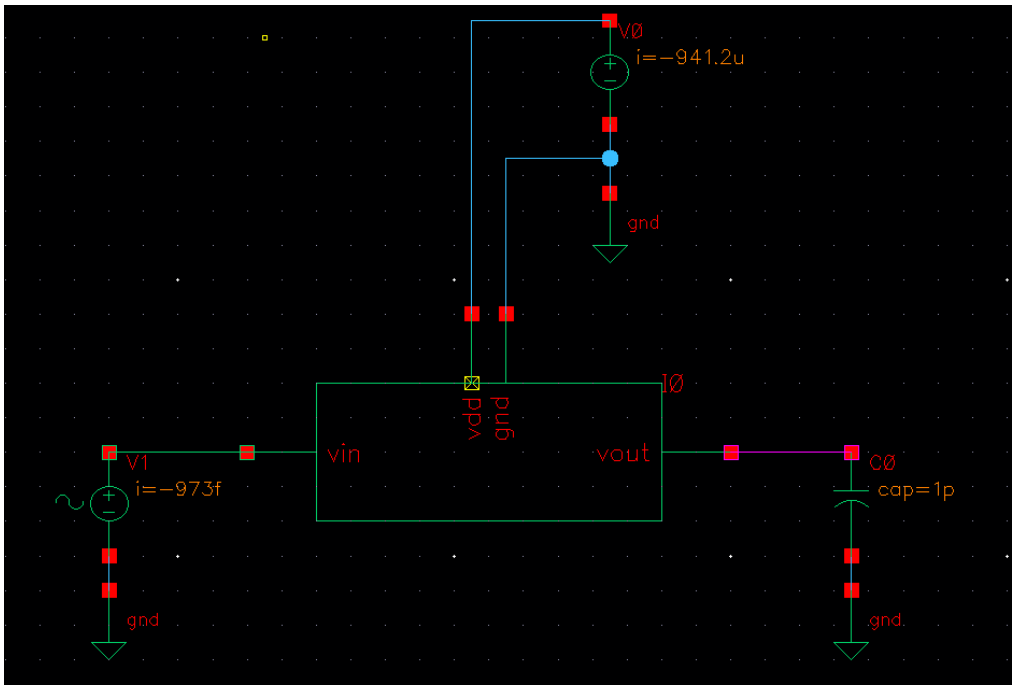
5.

In the PEX result, the resistance of drain and source will combine with parasitic resistance. Hence, the resistance in the PEX result will be larger than schematic result. If I need to keep VDD = 1.2V, the dc current near the VDD pin will have to decrease. So, the dc current in schematic result will be larger than PEX result.

- DC current of schematic results

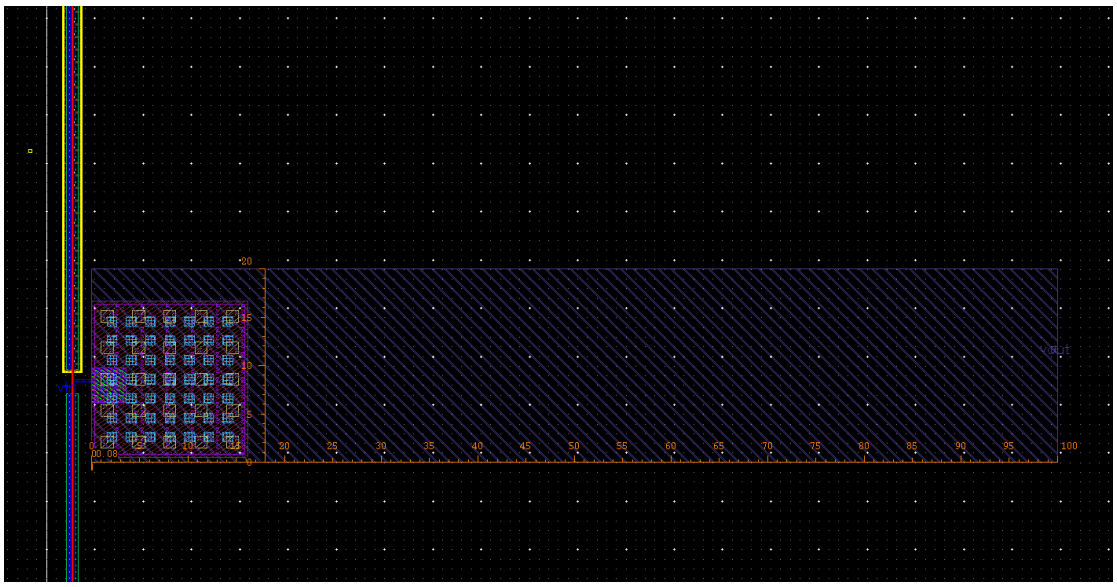


- DC current of PEX results

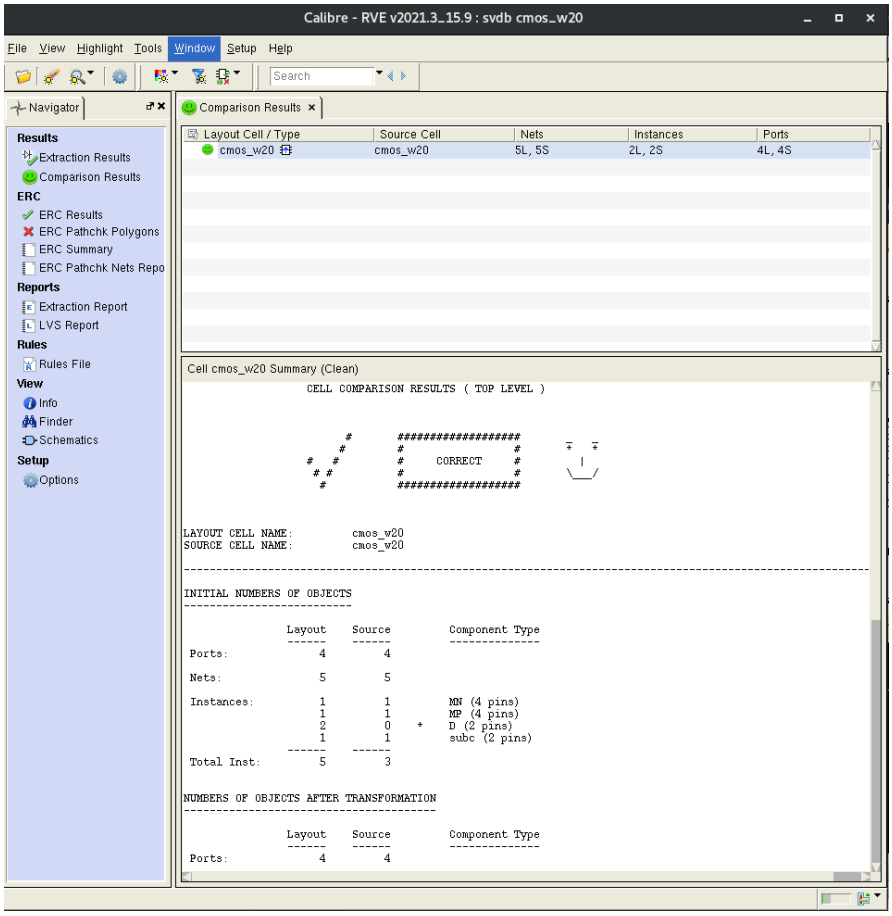


6.

- Layout figure

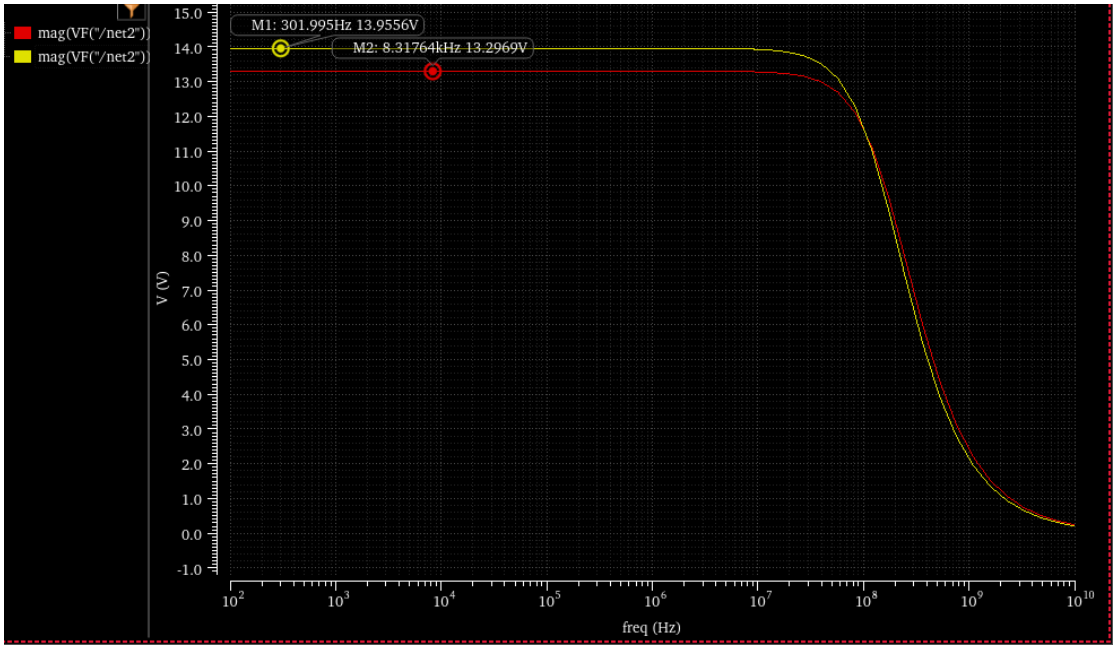


- Clean LVS result



- AC transfer characteristics:

The red line is Vout in schematic results, and the yellow line is Vout in PEX results.



- 3dB bandwidth of schematic

	Expression	Value
1	bandwidth(mag(...	184.6E6

- 3dB bandwidth of PEX

	Expression	Value
1	bandwidth(VF("/...	155.6E6

The parasitic resistance and capacitor of PEX result will be larger than schematic result, and the equation of 3dB cutoff frequency=1/(2*π*R*C). So, the bandwidth of PEX result will truly be larger than schematic result.