

# Lab 1: Cadence Tutorial on Schematic Entry and Circuit Simulation of a CMOS Inverter

## Introduction

This tutorial describes the steps involved in the design and simulation of a CMOS inverter using the Cadence Virtuoso Schematic editor and Spectre Circuit Simulator. IBM's 0.13 $\mu$ m mixed-mode CMOS process technology kit is used. Models and design data for this kit are proprietary and you must first sign a non-disclosure agreement before you will be able to get access to the kit files.

**Commands you enter at a shell prompt will be in bold.** LMB, MMB and RMB refer to left, middle and right mouse buttons. The LMB is used for selecting and positioning objects and making selections in dialog boxes in Cadence applications. The MMB brings up pop-up menus depending on the context.

The basic steps you will go through are:

- 1) Setup a working directory for you to use Cadence all semester.
- 2) Create a library where your design files will reside.
- 3) Enter a schematic using the Virtuoso Schematic Editor.
- 4) Simulate your circuit with the Virtuoso Spectre Circuit Simulator.

## Setup

Before invoking the Cadence tools, you must set up the environment under which these tools will be used throughout the semester. You only need to do this once. First, you need to setup your working directory. We will use a symbolic link to your class directory. To create the link, do the following (notice that there is a space between your username and "eecs413"):

```
cd ~  
ln -s /afs/umich.edu/class/eecs413/f21/students/<username> eeecs413
```

From your home directory you will now be able to access your class work space by typing:

```
cd eeecs413
```

Create a new folder to keep all your Cadence files in:

```
mkdir cadence
```

The configuration files are available in /afs/umich.edu/class/eecs413/f21/Public. Copy all of the files in this directory by typing (note there is a space after the \* in both lines. Ignore any omitting directory warnings.

```
cd ~/eecs413/cadence
cp /afs/umich.edu/class/eecs413/f21/Public/* .
cp /afs/umich.edu/class/eecs413/f21/Public/* .
```

## Creating a Library

**Whether creating a library, entering a schematic or running Spectre, you should always launch virtuoso from your eeecs413 “cadence” folder.** This needs to be done every time you open cadence from a new terminal window.

```
cd ~/eecs413/cadence
module load /afs/umich.edu/class/coe/modules/eecs413/f21
virtuoso &
```

The "&" runs the application in the background such that you can use the shell for further interactive commands if you wish.

The Command Interpreter Window (CIW) is the first window that appears. To make sure that you've copied the correct files and started “virtuoso” in the correct folder, look for the “IBM\_PDK” menu in the CIW. Then from the popup menu, choose

IBM\_PDK > Library > Create

A window pops up and you can type in the name for your library. Name your library *tutorial* for this example. Under Technology File click the ‘Attach to an existing techfile’ radio button and click ok. In the next dialog window select cmrf8sf and click ok. Click ok again in the next dialog window and your library is created!

Open the library manager from the CIW by selecting

Tools > Library Manager

The Library Manager window pops up and you will see three columns: Library, Cell, and View. A library is a container for cells. Libraries typically contain multiple cells and cells often have multiple views. A cell is the basic design component. For example, in this tutorial you will create an inverter cell with two views: schematic and symbol. Libraries containing user-defined cells are called design libraries whereas libraries containing technology-specific components (e.g. transistors for the IBM 0.13µm technology) are called reference libraries.

Next, click LMB on tutorial and you can see the name appears in the Library field. You can create a new cell by choosing


File > New > Cell View

In the dialog box, type *inverter* for the Cell Name, Type to *schematic* and Application to *Schematics-L*, then click OK. Say “yes” or “always” to any license-related pop-ups. This will automatically set the view to schematic. A new window will open called Virtuoso Schematic Editor. Later in the semester, you can create a new library for each of your homework assignments or projects.

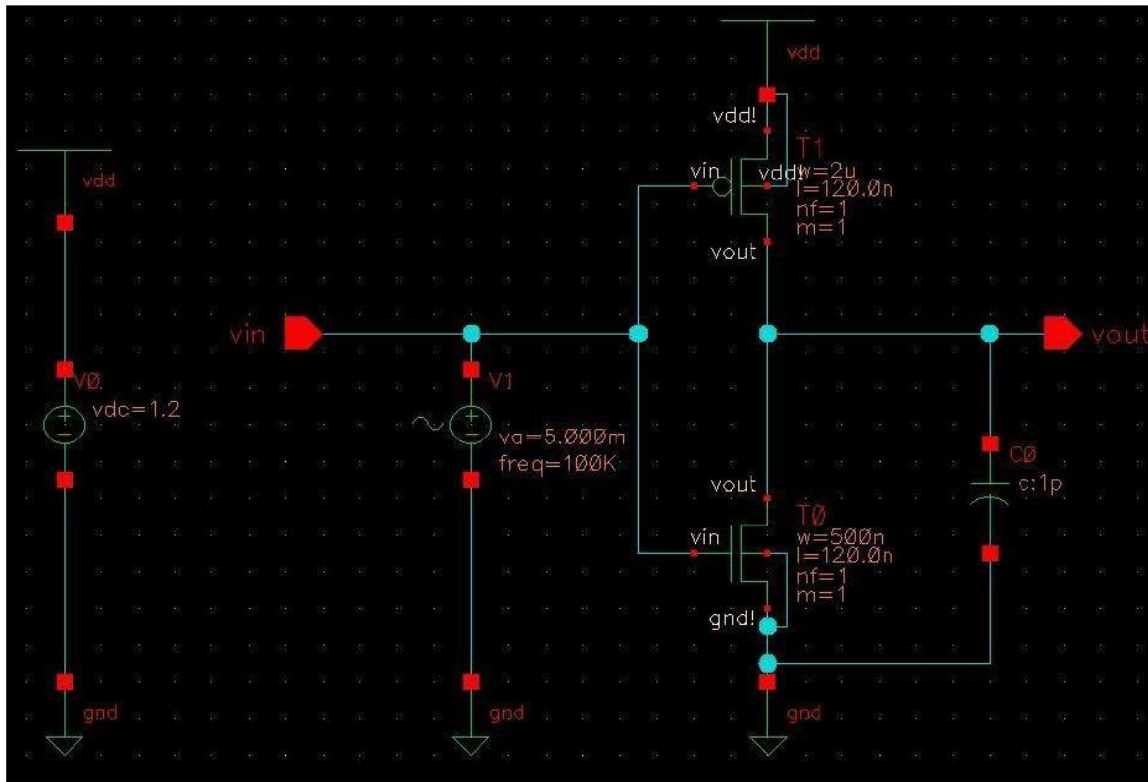
## **Schematic Entry**

First, expand the schematic window to its maximum size by clicking on the square box in the upper right corner. The pull-down menus at the top of this window and the icon bar on the left provide two ways to complete various editing tasks. For example, you can add an instance by choosing

Create > Instance

or by clicking on the icon bar entry that looks like an IC, “”. Bindkeys are shortcuts for common editing tasks. Notice the letter “i” next to the Add > Instance menu entry. This indicates that you can activate the add instance task by typing the “i” key while the cursor is in the main edit window (the window with the black background). After activating the add instance task in one of these ways, click Browse in the ensuing dialog box. Choose *cmrf8sf* for the library, *nfet* for the cell in this library and the *symbol* view. Move your cursor over the main edit window and you will see a ghost image of the nmos transistor. Click with the LMB to place the instance. Type the ESC key to end the add instance task. Repeat these steps, adding a *pfet* symbol to the schematic.

The transistors and other technology-specific components used in your designs will always be selected from the *cmrf8sf* library. Generic symbols like vdd, gnd and voltage sources will be selected from the *analogLib* library. Add the remaining symbols to the inverter schematic. Add a *vdc*, *vsin*, two *vdd*, three *gnd* symbols and a *cap* symbol with its default value from *analogLib*. Complete the schematic as shown in Figure 1. You don’t have to be concerned about the relative placements of the instances.



**Figure 1. Inverter schematic**

You can select an instance by clicking on it with the LMB. You can then move it with

Edit > Move

or simply by dragging the instance while holding down the LMB. Instance pins are connected together by wires. The connections can either be explicit, in which the wire extends to each pin, or by name, in which pins connect to two graphically separate wires bearing the same name. To make an explicit connection, first type the bindkey "w" or click the LMB on the Wire (narrow) icon in the icon bar. Click the LMB at the desired starting point in the schematic window and move the mouse to the destination and double click the LMB at the end point (single click if the endpoint is another wire or pin). You can draw as many different wires as you need until the task is cancelled by pressing the Esc key. If you wish to connect by name, give the same wire name to two separate wires. To name a wire, choose

Add > Wire Name

Fill in the wire name in the dialog box then move the cursor over the wire to be named. Note that the schematic in Figure 1 uses only explicit connections. Don't forget to connect the bulk of the *nfet* to *gnd* and the bulk of the *pfet* to *vdd*. Next, add input and output pins to the schematic. Type the bindkey "p" or click the LMB on the pin icon in the icon bar. In the dialog box, give a pin name and specify the direction of the pin. Then move your cursor on the schematic window to place the pin. The pins in Figure 1 are *vin* and *vout*.

The next step is to edit the properties of various components. First select the instance, then type the bindkey "q" or click the LMB on the Property icon in the icon bar. In the lower part of the

dialog box that appears, you will see the CDF parameter fields. Different parameters mean different things to downstream tools and you typically will only be interested in a few of the parameters. Edit the parameter fields of interest and click Apply. You can use variables as well as constants for parameters. For example, for the vsin voltage source at the input, type “vdc” for the DC voltage parameter. Later in analog simulation, you will sweep this variable. Also, for vsin set **AC magnitude = 1**, this normalizes the vout/vin small signal transfer function so that only vout is needed when plotting the frequency response. Finally, set **Amplitude = 0.005** (10mV peak to peak), **Frequency = 100K**. Click on Apply and OK. Now, set the DC voltage parameter for the source between vdd and gnd to 1.2. Change the width of the pfet transistor to 2u. Leave the length at 0.12u (120n). Change the width of the nfet transistor to 500n and leave the length at 120n. Your schematic should now look similar to Figure 1. The final step in the schematic capture is to *Check and Save*. Click the LMB on the Check and Save icon in the icon bar. Look in the CIW for errors or warnings.

## **Circuit Simulation**

You will use the Spectre circuit simulator via the Cadence Analog Environment. Enter the Analog Environment as follows:

Launch > ADE L

You can also invoke this from the CIW by choosing:

Tools > ADE L > Simulation

If you open the simulator from CIW, you have to load the design. You can do this by choosing:

Setup > Design

In the dialog box, choose the library and cell you want to simulate. Before running any simulations, the simulator needs to know about the process and the device models. Choose:

Setup > Model Libraries

Click on Browse and select the following file:


**/afs/umich.edu/class/eecs413/f21/IBM\_PDK/cmrf8sf/V1.8.0.3DM/Spectre/models/allModels.scs**  
**/afs/umich.edu/class/eecs413/f21/IBM\_PDK/cmrf8sf/ V1.8.0.3DM /Spectre/models/design.scs**



In the same window, make sure to set the section tab as **tt** for allModels.scs

Click on Apply and then click OK to close the dialogue window. Next, load and edit the design

variable vdc. Choose:

Variables > Copy From Cellview

You will see the design variable appear in the window. Click the LMB on the Edit Variables icon  in the icon bar. Click on vdc, set the value to 0 and click OK. Note that you can overwrite this value later when you run the simulation. But you must always set the variables to some default values before you run the simulation. The next step is to select the analysis type. Click the LMB on

the Choose Analysis icon  in the icon bar. In the dialog box, choose dc analysis. DC analysis simulates a circuit's steady-state (i.e. time-independent) behavior. Select Design Variable in the field of Sweep Variable. Click on the Select Design Variable and choose vdc. In the field of Sweep range, type 0 for start and 1.2 for stop. For Sweep Type, click and select Linear then select Step Size and enter 0.005 (i.e. 5mV) in the field of Step Size. Click OK. To run the simulation, click the LMB on the Netlist and Run icon  in the icon bar. A general information window will pop up along with a simulation log. To show the waveform, choose:

Results > Direct Plot > DC

In the schematic window, click on the vin and vout wires or pins. Press ESC to finish selection. Figure 2 shows the resulting DC transfer characteristic curve.

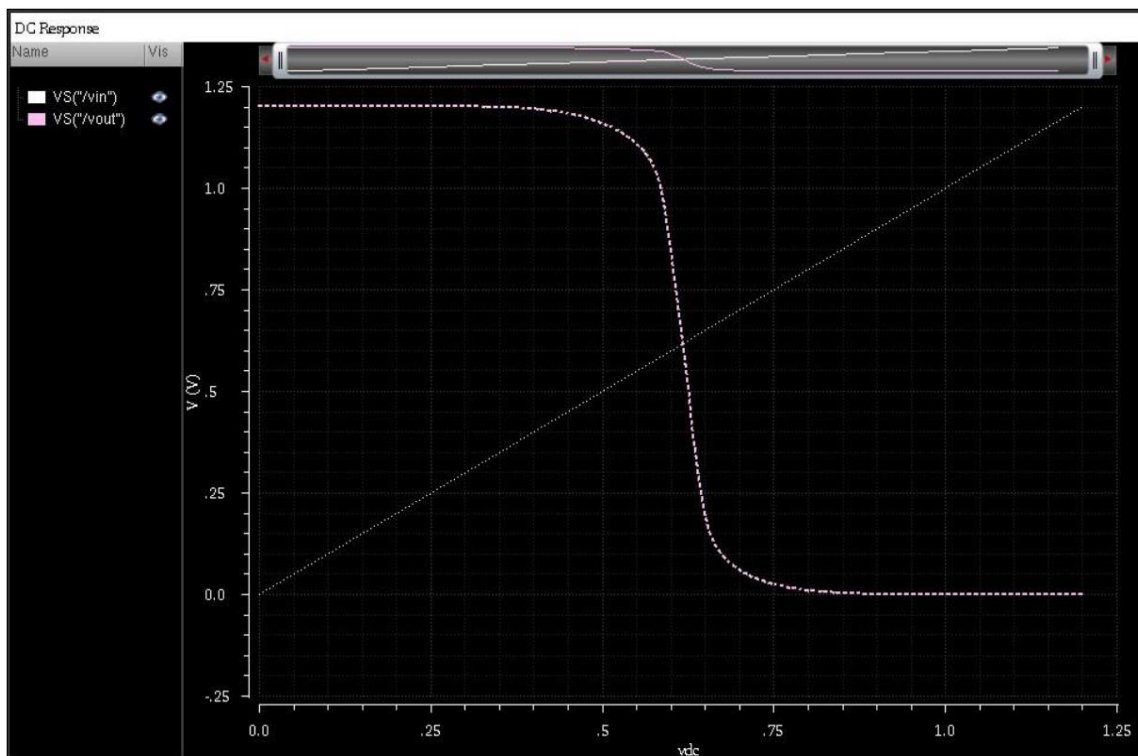



Figure 2. Inverter DC transfer characteristics


Alternatively, you can plot using the calculator. From the waveform window click:

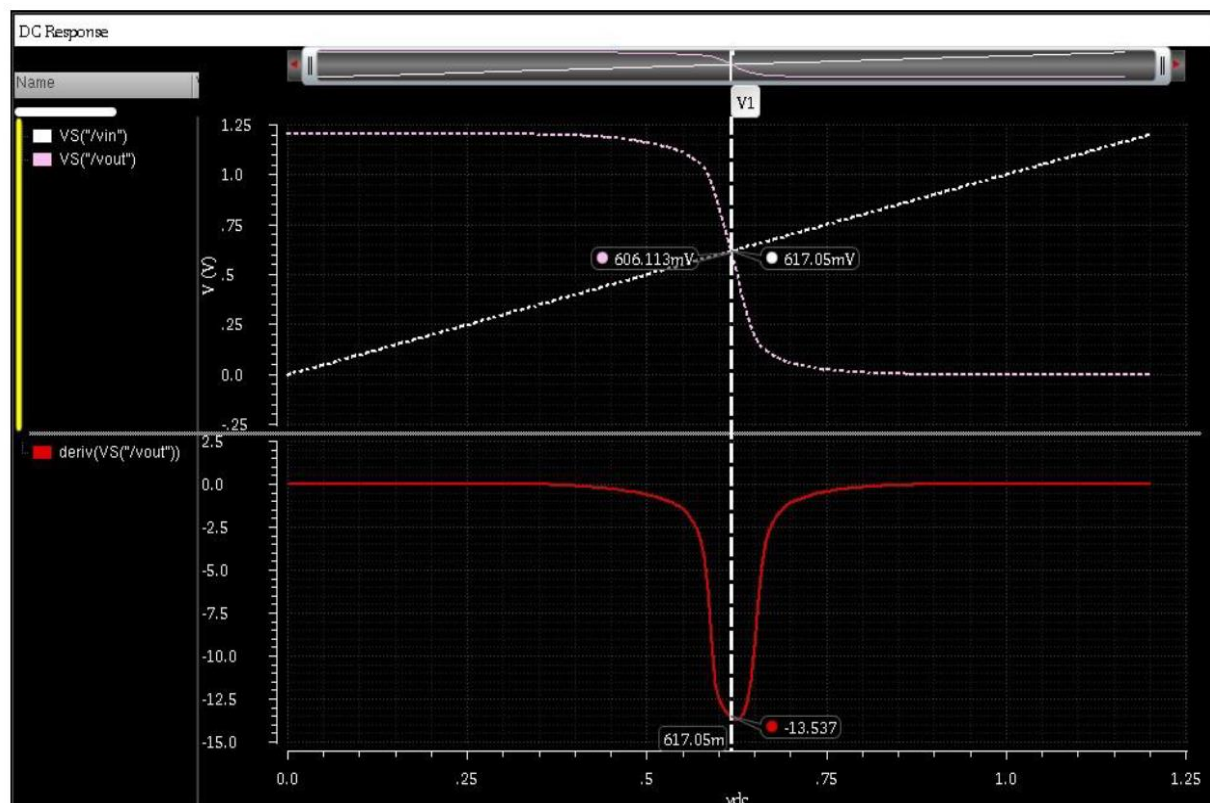
Tools > Calculator

The calculator can also be brought up by clicking the calculator icon from the tools menu of the waveform window or from the tools menu of Analog Environment. From the calculator window, click the “vs” button and in the schematic window click on the vout pin. In general, use “vs”(“is”) for voltage(current) data from a DC sweep analysis, “vdc”(“idc”) for voltage(current) data from a DC analysis, “vf”(“if”) for voltage(current) data from an AC analysis and “vt”(“it”) for voltage(current) data from a transient analysis. Now return to the calculator window and click

“deriv” in the Function Panel. Now click the “” button on the calculator. To separate the curves, from the waveform window click:

Graph > Split Current Strip

Or click on the Strip Chart Mode icon “” in the waveform window. You can also overlay curves by clicking and dragging them onto one another. Click and drag the “VS(“/vout”)” curve onto the VS(“/vin”) curve and you should have a plot similar to the one in Figure 3.



**Figure 3. Inverter DC transfer characteristics**

Use a vertical trace to find the value for vdc that corresponds to the maximum magnitude of the slope. From the waveform window you can either

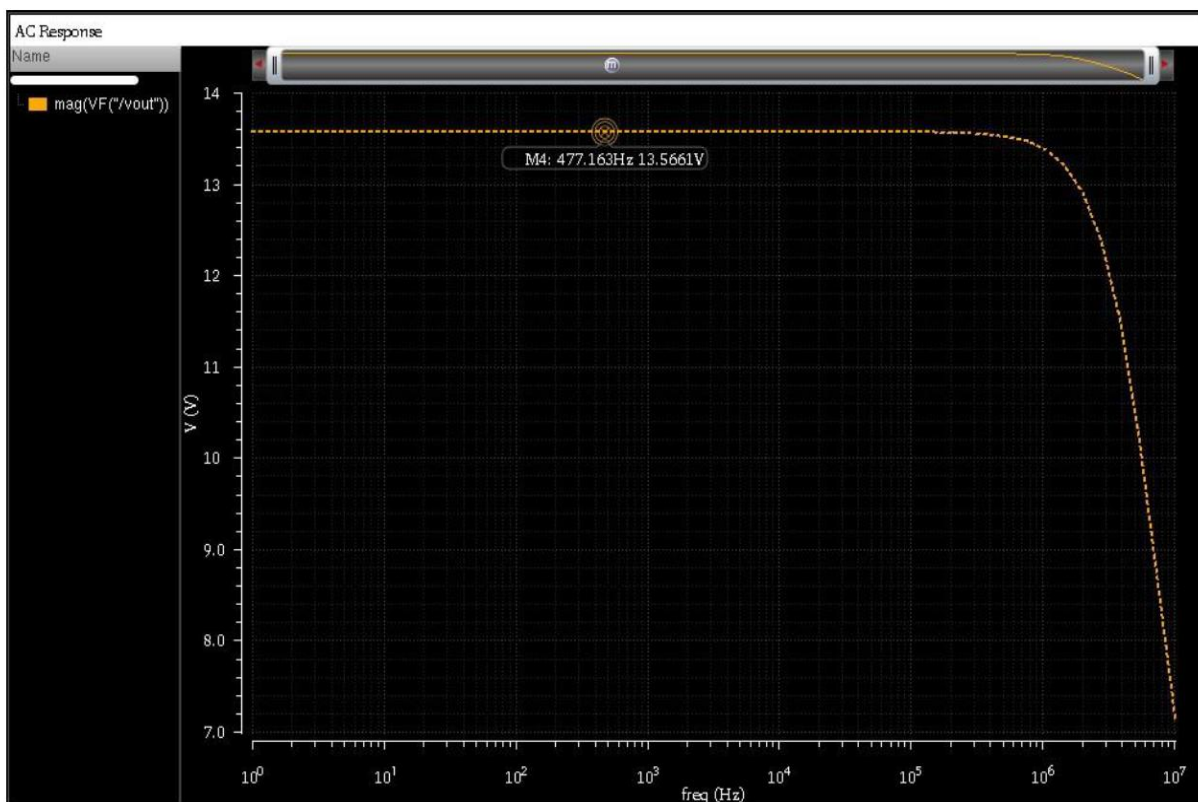


Shortcut “v” > adjust manually

You should get a value of 615 mV for vdc corresponding to a magnitude of about 13.7 for the slope of the curve. This is the maximum gain of the circuit. Next, run the AC analysis. AC analysis simulates a circuit’s small-signal frequency dependent behavior. Choose ac analysis in the Choosing Analyses dialog box, and for Sweep Range select the Start-Stop option. Enter 1 in the start field and 10M in the Stop field. Click OK. In the Analog Environment window, set the value for vdc to 615 m and then click the Netlist and Run icon in the icon bar. Plot the output with:

Results > Direct Plot > AC Magnitude

In your schematic window click vout and then press ESC. Your curve should look like Figure 4. Using a Crosshair marker, a low frequency magnitude of about 13.68 should be observed. Note that this is the low-frequency gain of the circuit and agrees with our previous DC analysis.




**Figure 4. Inverter AC transfer characteristic**

Next, run the transient analysis. Transient analysis simulates a circuit’s behavior over time and is the closest simulation to real operation. Choose “tran” analysis in the Choosing Analyses dialog box and set the stop time as 20u. Run the simulation by clicking the LMB on the Netlist and Run icon. You can plot the output with:

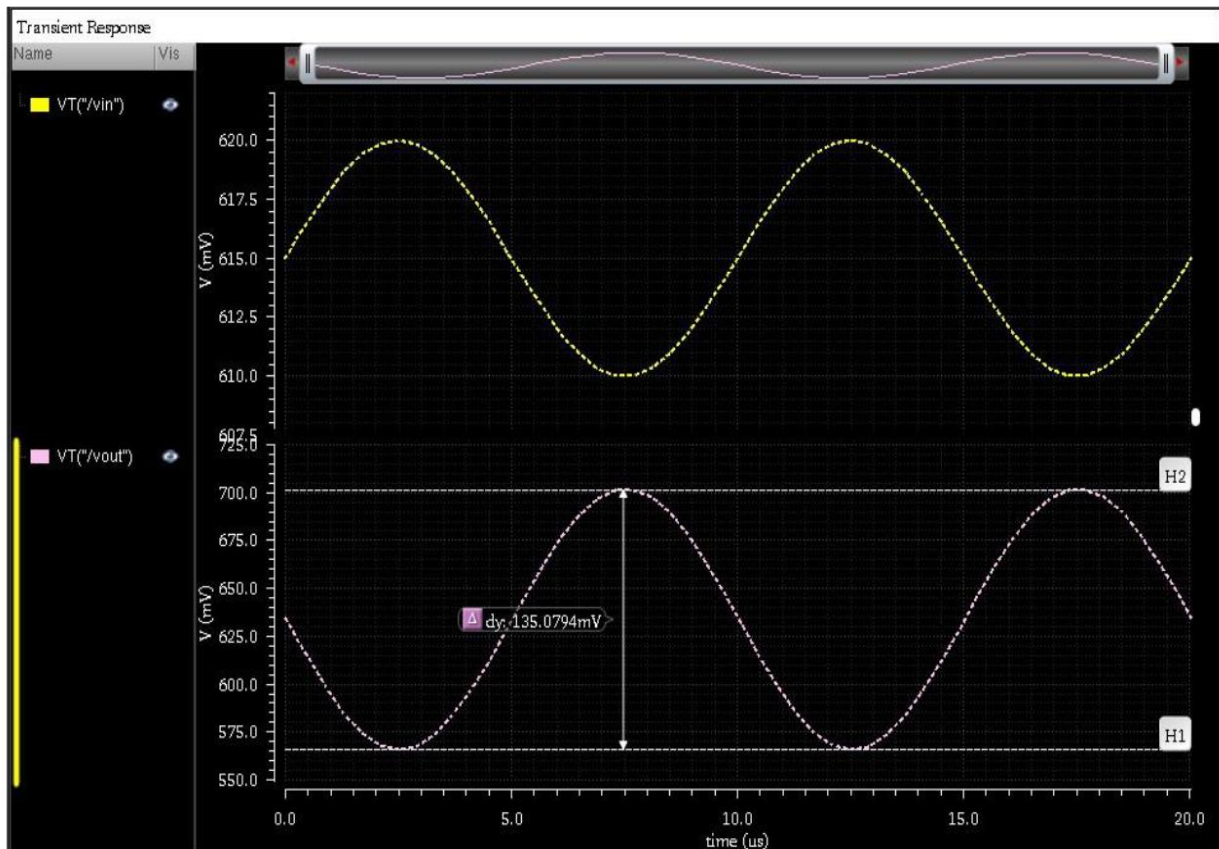


Results > Direct Plot > Transient Signal

In your schematic window, first click vin, then vout and then press ESC. Click on the Strip Chart Mode Icon “” and your curves should look like Figure 5. Use the horizontal delta markers (make sure you selected VT (“/vout”) by observing yellow vertical bar at the left side chosen figure):

Shortcut “h” > shortcut “d” > adjust manually

Then, you can adjust the trace to measure the peak-to-peak output voltage. To help you determine the ratio of the peak-to-peak output voltage and the peak-to-peak input voltage. A value of about 13.7 should be observed for the gain. Note that this value agrees with those observed in the previous two simulations.



**Figure 5. Transient analysis of inverter**

Operating point characteristics for devices and elements can be viewed as well. In the Analog Environment window click:

Results > Print > Transient Operating Points

In the schematic window select the NMOS device and then select the PMOS device. A window displaying their respective device parameters and operating points will appear. Locate the

“region” parameter and observe the number to the right of it. This number indicates the region of operation in which the device is operating. In general a “0” means the device is operating in cutoff, a “1” indicates triode, a “2” indicates saturation and a “3” indicates the subthreshold region. From this window use the “gm” and “gds” values of both devices to calculate the following:

$$(g_{m,NMOS} + g_{m,PMOS}) \left( \frac{1}{g_{ds,NMOS} + g_{ds,PMOS}} \right) = \frac{243.3 + 300.7}{19.32 + 20.46} = 13.675$$

The previous expression is the small signal gain of the circuit and a value around 13.7 should be calculated. Note that it is in agreement with all previous simulations. You can save the state of a simulation so that you don’t have to repeat these steps every time you want to simulate this or a similar circuit. To save the state, choose:

Session > Save State

Click on OK. This will save the state to the default name state1. You will load this state in a later simulation session.

## Plots

You can print waveforms by choosing:

File > Print

To save schematic image choose:

File > Export Image

Select the Export Region, your preferences via Size and Appearance section, and write a name via Output section in the ensuing dialog box.

## Design Hierarchy

Using hierarchy effectively is important when creating large designs. Hierarchy helps to make the design task more manageable by adding levels of abstraction and reducing the overall complexity of a design. Low-level “leaf cells” composed of primitive transistor instances and wires can be represented by a black box or symbol. This symbol can then be instantiated in other schematics to represent circuits of greater complexity. The remainder of this tutorial demonstrates how to generate a symbol, instantiate it and simulate the new circuit. The resulting design isn’t truly hierarchical, but it demonstrates the techniques involved with creating and simulating hierarchical circuit representations.

## Symbol Generation

The schematic you've entered to this point has voltage sources on vdd and the input that should not be present in a leaf cell. Therefore, create a new schematic cell view called `cmos_inverter` in your design library. Copy the inverter schematic into it (select all by click/drag with LMB, then click on the Copy icon), then remove the voltage sources and add new pins as shown in Figure 6. The vdd and gnd pins are created as "inputOut" direction pins.

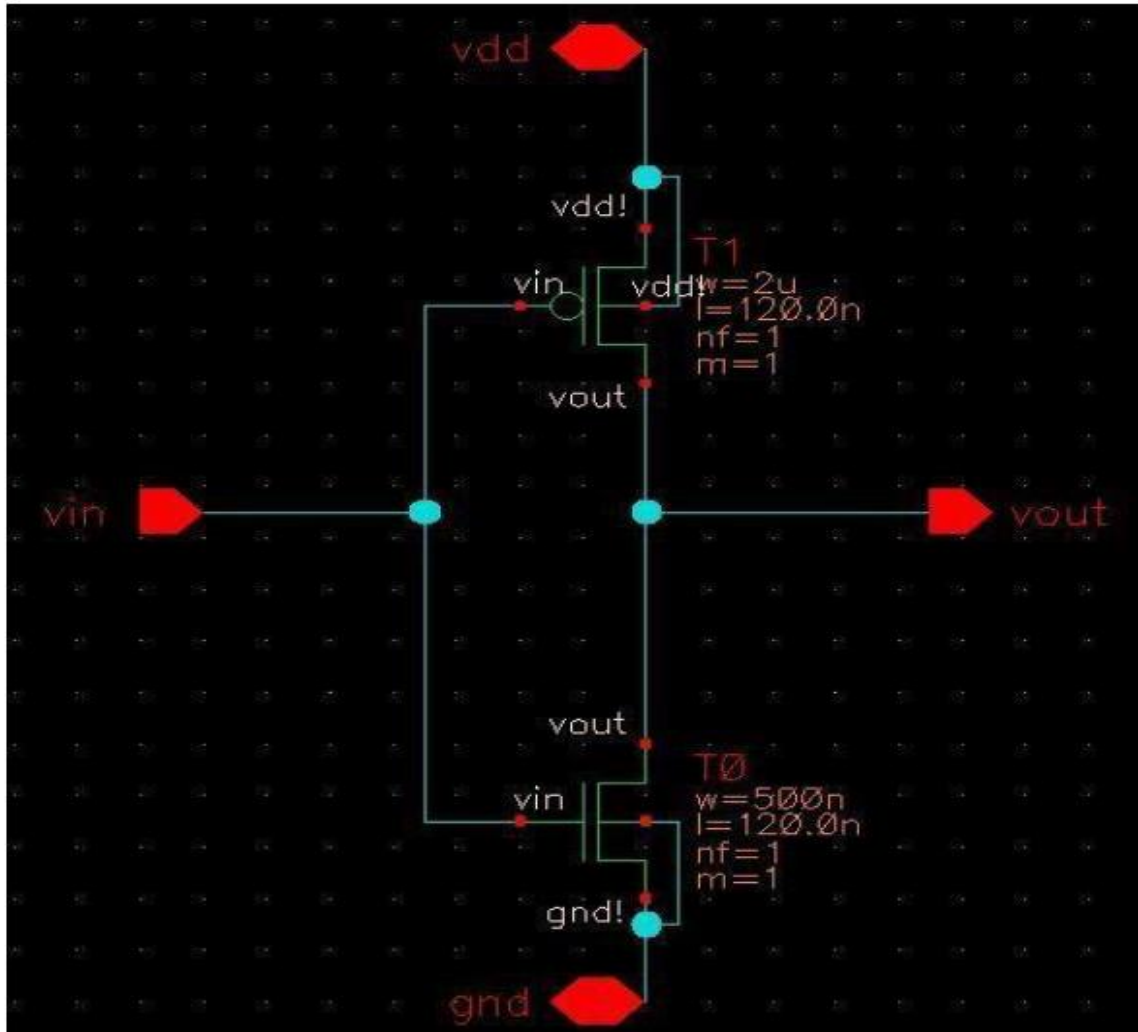


Figure 6. CMOS inverter schematic

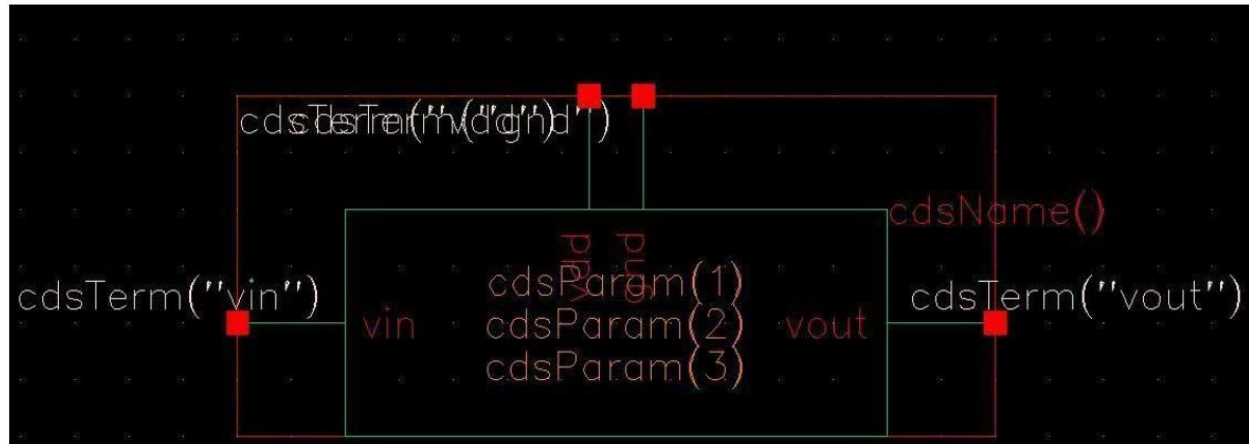
Save the schematic and choose:

Create > Cellview > From Cellview

In the dialog box, make sure that the field of "To View Name" is symbol and then click OK. Accept the defaults for the Symbol Generation Options dialog. You can redraw the symbol if you want by using the icon bar. Check/Save with:

File > Check and Save

The symbol can be used as a subcircuit in larger designs. The symbol is shown in Figure 7.



**Figure 7. CMOS inverter symbol**

### Simulation Using a User Defined Symbol

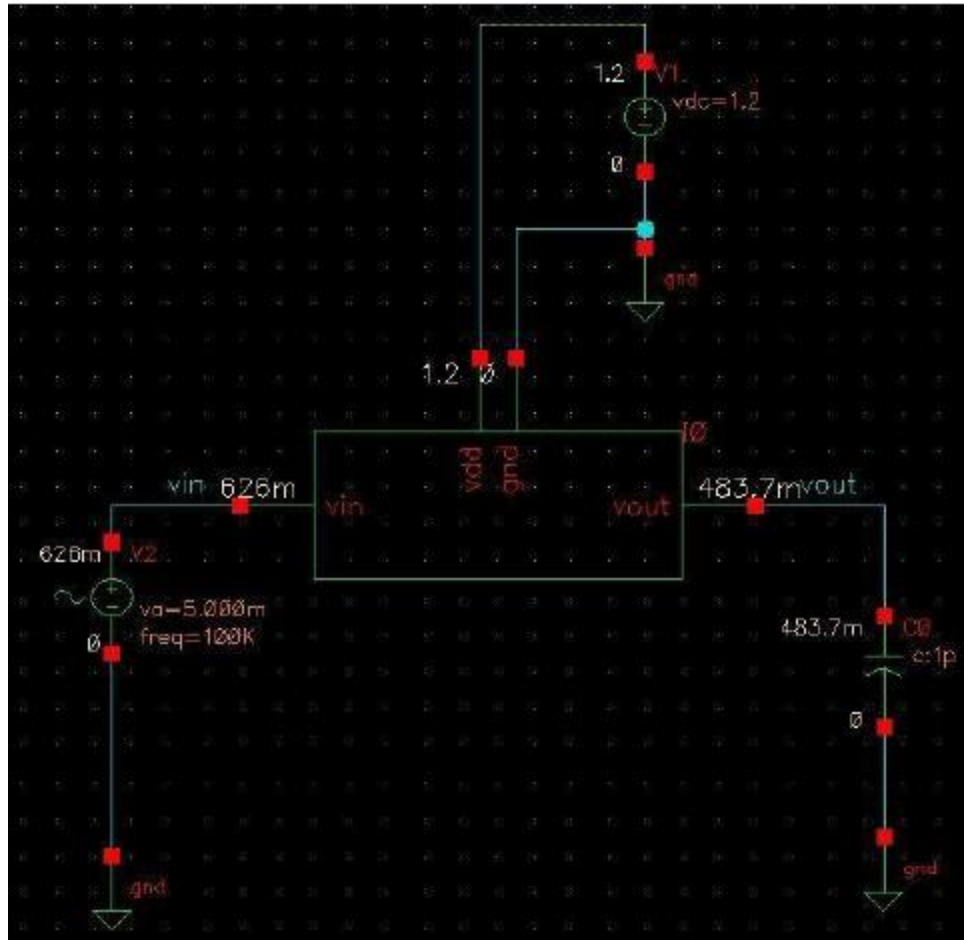
Create a new cell, named test\_inverter, and instantiate the inverter symbol by choosing:

Create > Instance

Click on Browse, choose the tutorial library, the cmos\_inverter cell, and the symbol view. Place this on the schematic. Add vdc, vsin and gnd symbols from the analogLib library. Add a capacitor from the analogLib library to the output of the inverter. To add the capacitor, choose:

Create > Instance

Click on Browse, choose the analogLib library, and add an instance of the cap symbol to the schematic. Rearrange and connect the symbols so the schematic looks like Figure 8. Click on the vdc source and then click on the Properties icon. Enter 1.2 for the DC voltage. Set the properties of the vsin source to AC magnitude = 1, Amplitude = 0.005, Frequency = 100K and set the DC voltage to the vdc variable. Enter the properties of the cap (click on capacitor and press “q”) and change the capacitance to 1pF.



**Figure 8. Schematic using user defined inverter**

To simulate the new circuit, choose:

Launch > ADE L

You can load the previously saved state, so it is not necessary to re-enter all of the device model files and simulation commands. Choose:

Session > Load State

Make sure the Library is set to tutorial, the Cell is set to inverter. There should be a saved state called state1 available. Click OK. Now click on the Netlist and Run icon. You can view the output of the simulation by following the procedures used earlier in this tutorial.