University of Michigan

EECS413

Final Project Proposal

Group 7

Team Members

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Project Information

Project Idea: 8-bit SAR ADC

Project Motivation: We are interested in building a ADC circuit because ADC is one of the most important components in analog circuit design, and Successive Approximation ADC is one of the classcial models of ADC. It is a reasonable goal for a ADC beginner.

Design Goal: Build a SAR ADC circuit whose diagram is Fig.1. The S&H block uses the technique of CMOS S&H, as Fig.2. The comparator block uses the instance in the library. The register is a normal clk rising edge register and control logic is made by logic gates. The DAC uses the technique of R-2R ladder DAC, as Fig.3.

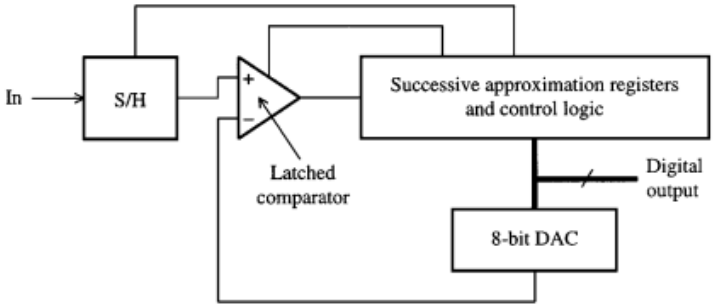

Fig.1: system block diagram[1]

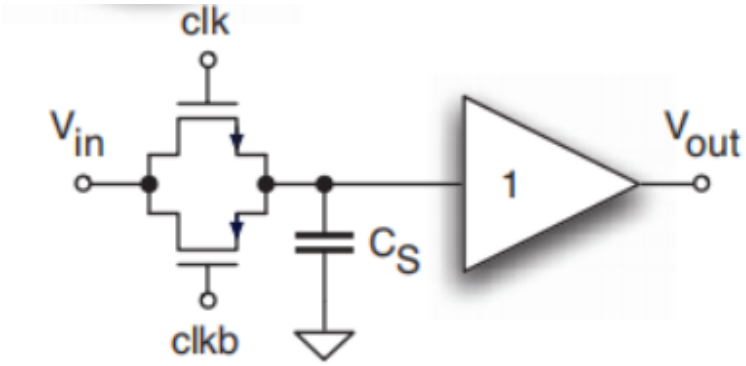

Fig.2: CMOS S&H block[2]

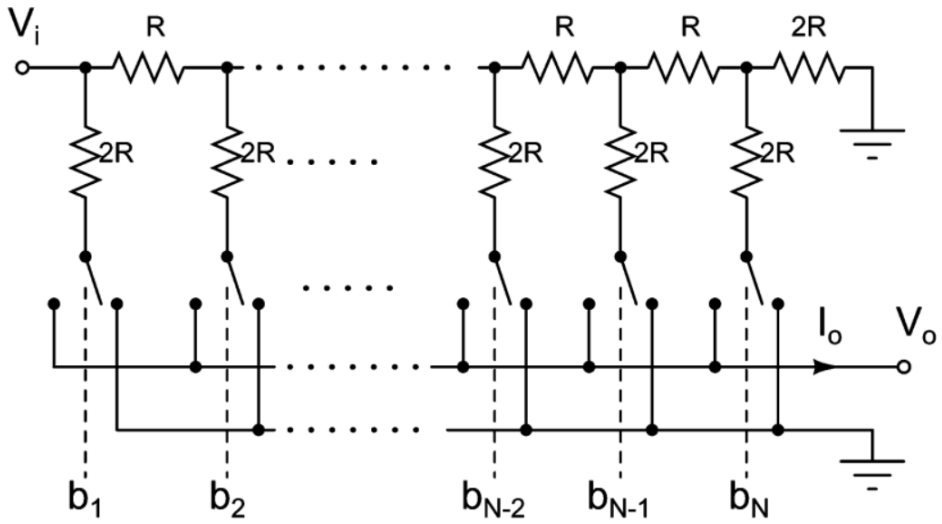

Fig.3: R-2R ladder DAC[3]

Design Specifications: Based on the datasheet of ADC1175 from Texas Instruments[4], important and reasonable specifications should include supply voltage, input voltage range, bandwidth, input capacitance and resistance. The following table is our expected specifications.

	Value	unit
Supply Voltage	5	V
Input Voltage Range	0.7-3.7	V
Bandwidth	>1	MHz
Input Capactance	<20	pF
Input Resistance	>1	MΩ

Reference

[1] S. Mortezapour and E. K. F. Lee, A 1-V, 8-bit successive approximation ADC in standard CMOS process, in IEEE Journal of Solid-State Circuits, vol. 35, no. 4, pp. 642-646, April 2000, doi: 10.1109/4.839925.

[2] Franco Maloberti, CMOS Sample and Hold, Data Converters, Springer Publishing Company, Incorporated, 2010, pp.213-217.

[3] D. Marche and Y. Savaria, Modeling R-2R Segmented-Ladder DACs, in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 57, no. 1, pp. 31-43, Jan. 2010, doi: 10.1109/TCSI.2009.2019396.

[4] Texas Instruments, "ADC1175 8-Bit, 20MHz, 60mW A/D Converter," ADC1175 datasheet, Apr. 2013.