University of Michigan

EECS413

Final Report
8-bit SAR ADC

Group 7

Name : Yiwei Zeng, Duanxie Shen, Hsiang-Yang Fan

Date : 6 December 2022

Achieved Performance

	Expected Performance	Actual Performance
Supply Voltage(V)	5	5
Input Voltage Range(V)	0.7-3.7	0-3
Clock Frequency(MHz)	>2	2
Input Capactance(pF)	<20	0.02
Input Resistance(MΩ)	>1	>>1

Schematic

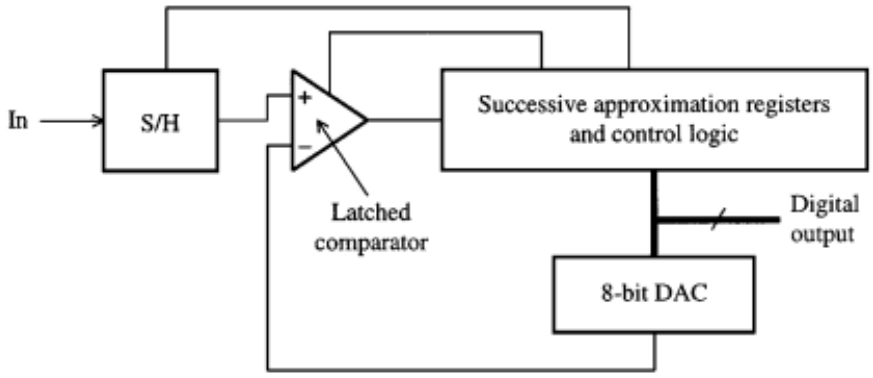

Fig.1: block diagram[1]

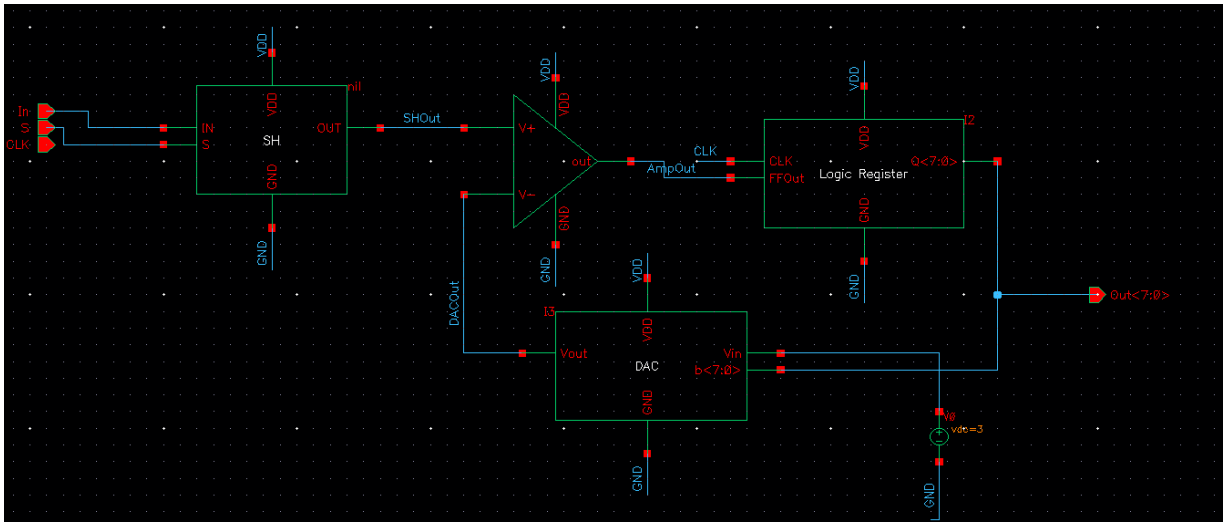

Fig.2: schematic

Abstract

Analog-to-digital converter(ADC) plays an important role in many circuits nowadays. It transfers analog signals from real world to digital signals which can be used easily in digital circuits. In this project, a successive approximation ADC with high clock frequency is realized based on inverting op-amp configurations with biasing currents added to the op-amp negative input terminal so that the op-amp input common-mode voltages can be biased near ground to minimize the supply voltage. It is shown that in the worst case, the circuit is sufficient to convert analog signals in 2MHz clock frequency.

1. Introduction

In many mixed-signal systems, analog-to-digital converters (AD's) are required for interfacing analog signals to digital circuits. The requirement is usually to integrate these ADC's with digital signal processors in a low-cost CMOS technology. To make a fast convertion, different techniques have been used to realize ADCs including counter type ADC, tracking type ADC and flash ADC. This project uses an technique called successive approximation to design a 1-V 8-bit successive approximation ADC[2]. The ADC was designed for high speed applications such as sensitive sensors. The block diagram of the ADC is shown in Fig. 1. The major analog building blocks are discussed in the following sections.

2. Division of labor

Theoretial circuit construction: Yiwei Zeng
Circuit building:
1. Sampling and Hold Circuit: Duanxie Shen
2. Op Amp: Yiwei Zeng
3. Control Logic and Registers: Hsiang-Yang Fan
4. DAC: Duanxie Shen
5. ADC: Yiwei Zeng
Report Writing: Yiwei Zeng, Duanxie Shen, Hsiang-Yang Fan

3. Design and Simulation Analysis

A. Sampling and Hold Circuit

The Sampling and Hold function is realized under the control of two phases, one for sampling the input signal and the other for retaining the signal and making it

available at the output during the hold phase. This circuit is realized by CMOS switch technique[2], which uses CMOS complementary transistors as the switch for the sampling and hold. Fig.3 shows the schematic.

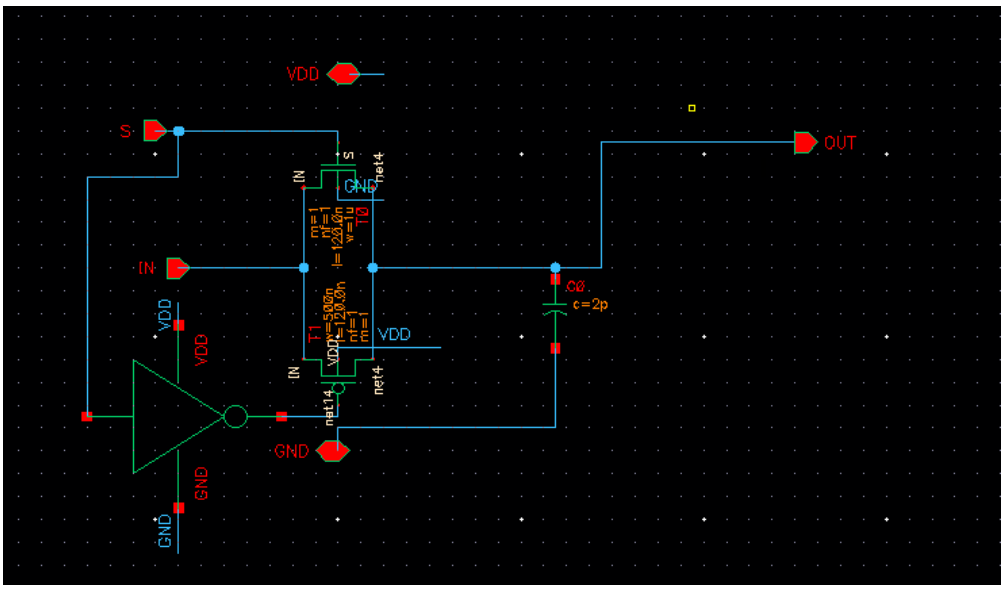

Fig.3: Sampling and Hold Circuit schematic

When control signal S is high, the transmission gate is open and sampling the analog signal, and when S changes to low, the gate shuts so that the capacitor holds the analog signal.

This technique is a easy technique to implement and it has drawbacks. One abvious backward is that when transmission gate is close, there are still leakage current, which means the voltage stores in capacitor will drop with time going. Proper capacitor addition at the node can hold the voltage for longer time.

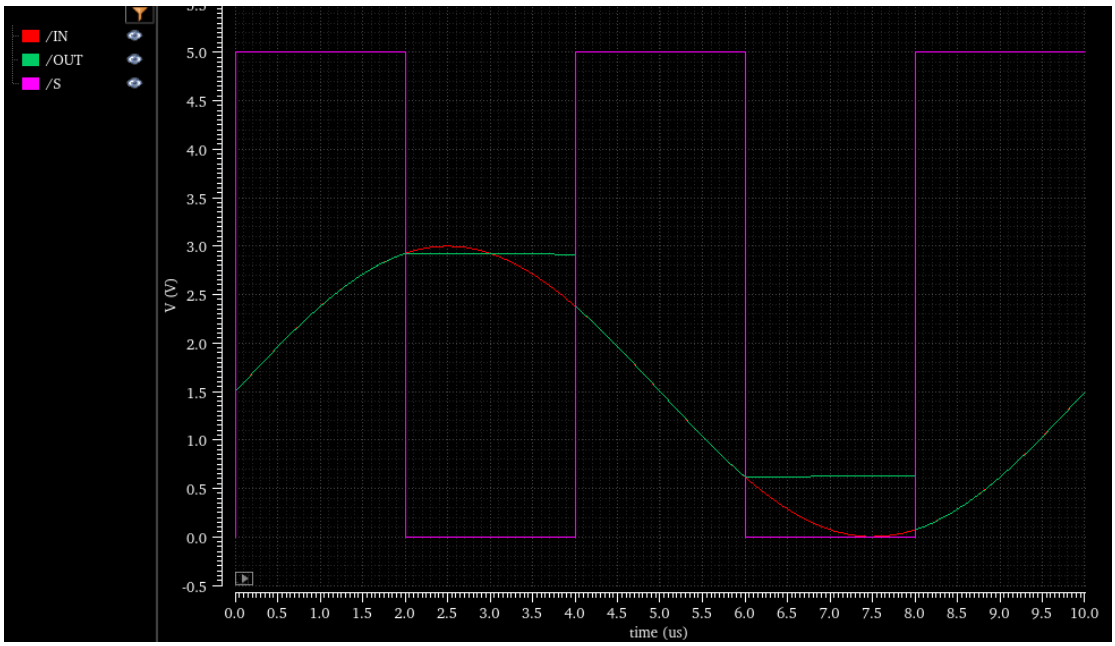

Fig.4: Sampling and Hold Circuit simulation

The simulation result(Fig.4) shows that the voltage holds well in assigned sampling frequency(8 times of clock frequency, because a 8 bit SAR ADC needs 8 clock cycles to convert signal).

B. Op Amp

The Op Amp is a cascode differential amplifier, and have a dual rail voltage output. It has a large low-frequency gain so that when the difference between two voltage inputs is slightly large than 0, the output of the amplifier will be high because of the large gain, which can be used to compare two input voltage. Fig.5 shows the schematic.

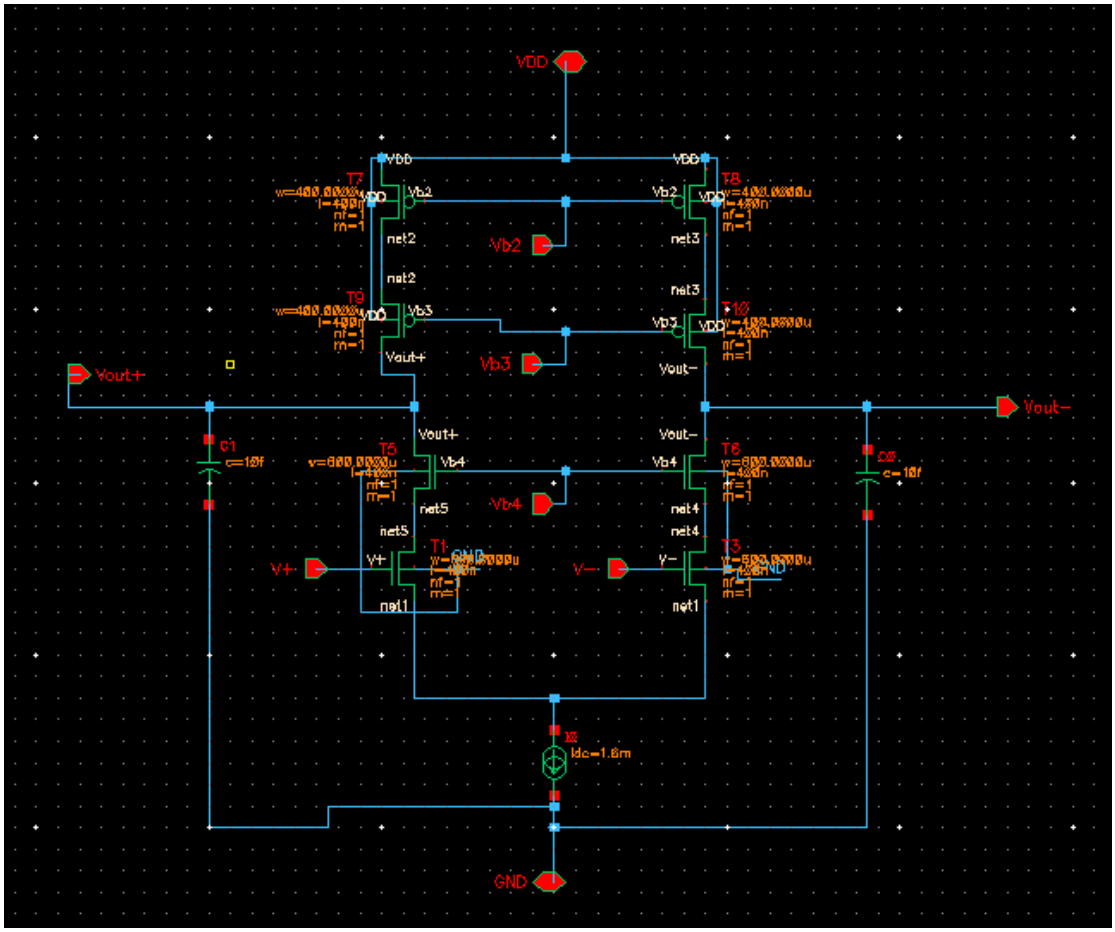

Fig.5: Op Amp schematic

The disadvantage of cascode Op Amp is limited output swing, which should be minused by 4 overdrive voltage. Another drawback is the difficulty in shorting their inputs and outputs, to implement a unity-gain buffer, because the input range to make every transistors saturation is very narrow. That can be solved by using a folded cascode Op Amp in necessary situation.

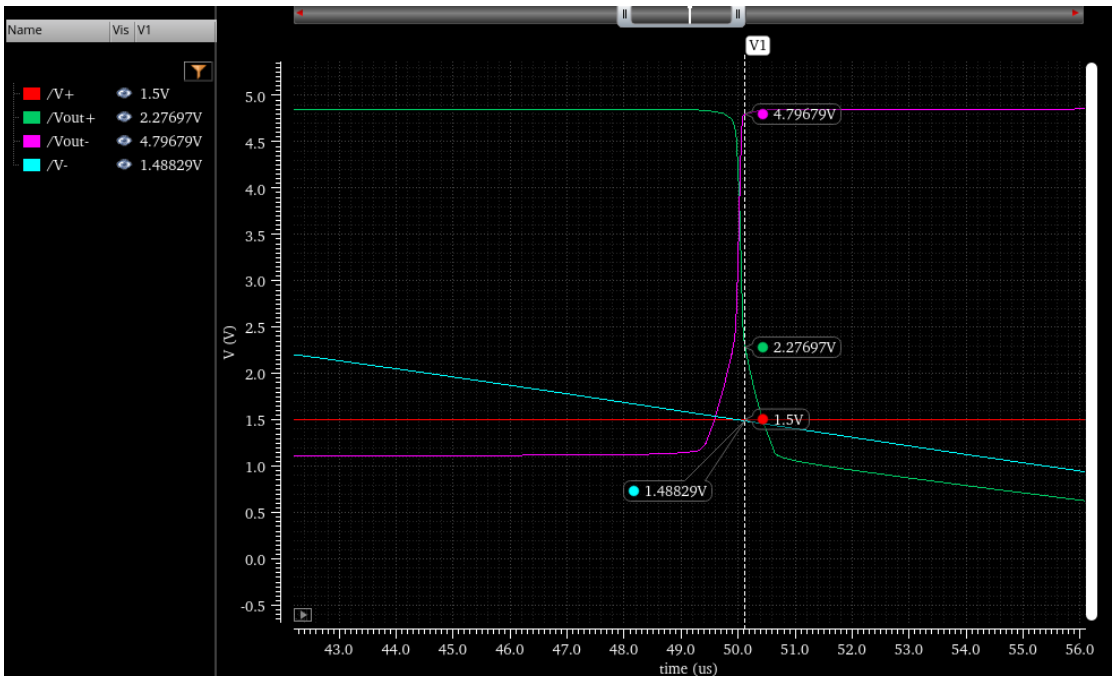

Fig.6: Op Amp low-frequency gain

From Fig.6, the low-frequency gain of Op Amp is about 250, and voltage swing isn't large enough. The result shows that some enhance network is necessary to make the output closer to digital signal, in this circuit several inverters is used to enhance the circuit, Fig.7 is the result.

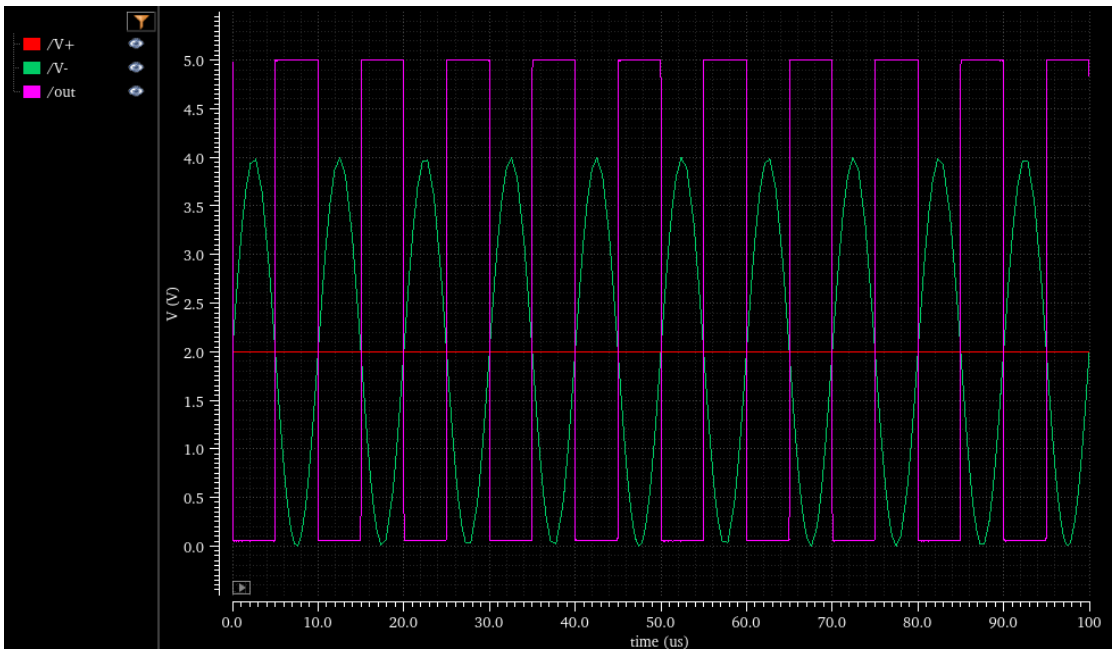

Fig.7: Op Amp output

C. Control Logic and Registers

The control logic is built to generate a output prediction and check whether the prediction is successful. Every bit of the digital output has 3 stage. The first stage is initializing and set to 0. In the second stage, the most significant bit that hasn't

be changed is set to 1. Then the register will send the output to DAC and the new signal from Op Amp will come in. The third stage, the logic circuit transfer the Op Amp output into the bit register, which shows whether the prediction is successful. There is a 3-bit counter to help find which bit needs to be changed in present clock cycle. Fig.8 is the schematic.

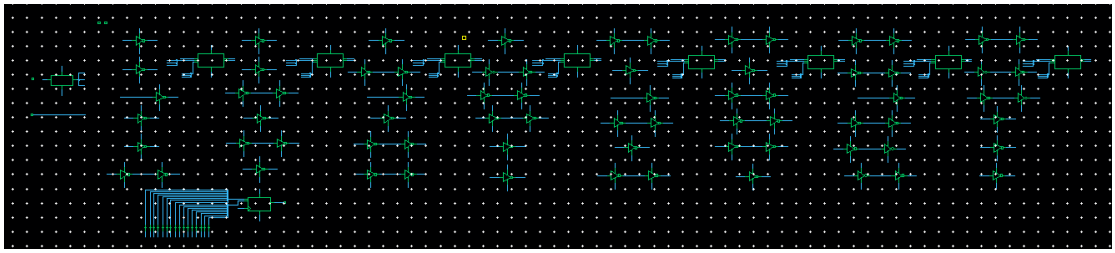

Fig.8: Control Logic and Registers schematic

There is a functional disadvantage for this logic circuit. At the beginning, everything in the circuit is initialized so DAC output is 0, which means the Op Amp output is 1 before the first rising edge of the clock. Considering the 8h bit is in the third stage in the 8th clock cycle, it is also in the third stage in the 0th clock cycle, which means the output 1 of Op Amp before the first rising edge of the clock will be stored. That will possibly cause 1 bit error in the 8 bit ouput, which cause a relative mean error for 0.2%. A solution to this problem is adding a register after the input, which can hold 0 before the first rising edge of the clock. This will cause another problem that the third stage of every bit comes at the clock cycle after the next clock cycle of the second stage. To ensure correct prediction feedback, the clock cycle which is necessary to measure a signal from 8 clock cycles to 16 clock cycles, which is doubled.

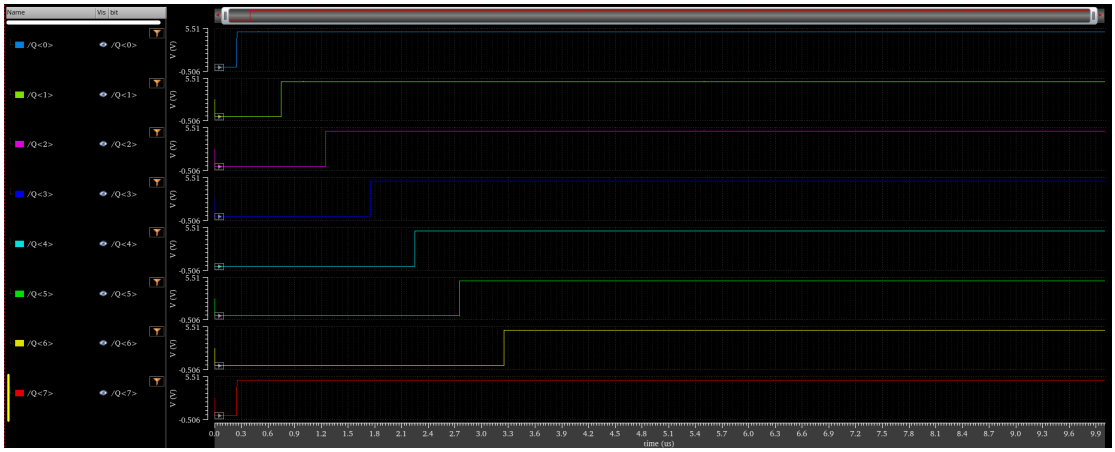

Fig.9: Control Logic and Registers output

The output of Fig.9 shows the functional disadvantage, for all 1 input, Q(7) rises at the very beginning, which should rise at the 8th clock cycle.

D. DAC

DAC is used to convert digital signal into analog signal. It is realized by a sequence of voltage divider and the output merges output of these dividers. This DAC uses the logic of R-2R Ladder, which is in Fig.10[3]. Using thevenin theory, we can find that each input bit b_n contributes voltage of $b_{n-1}/2$ to output voltage, which can control output signal by bit within assigned precision. The schematic is Fig.11.

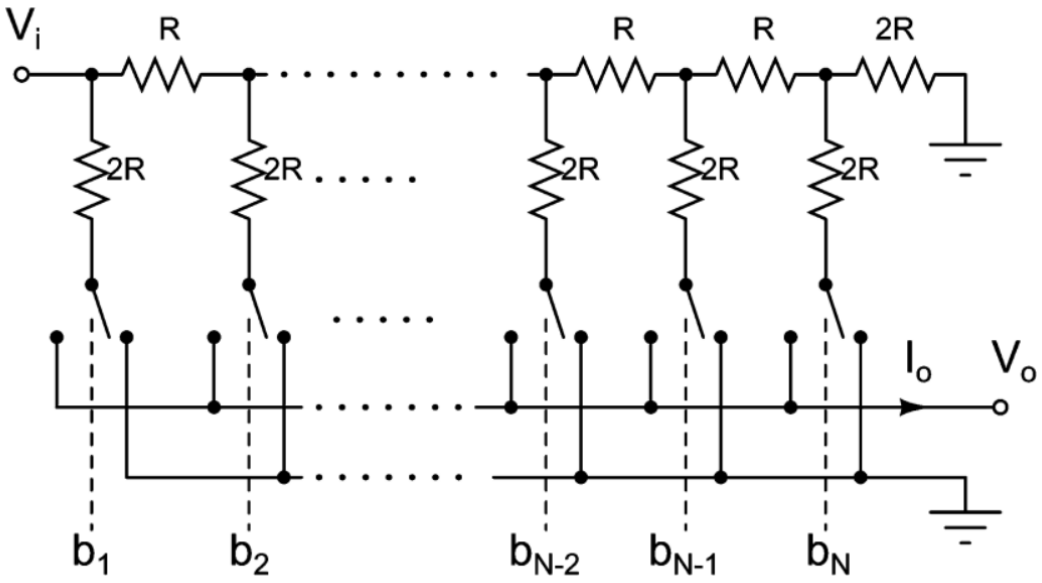

Fig.10: R-2R Ladder

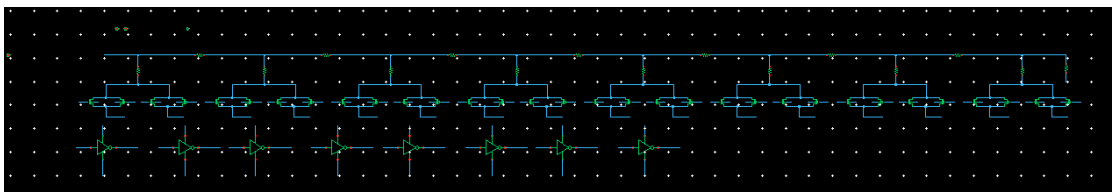

Fig.11: R-2R Ladder DAC schematic

Parasitic impedence of transistors which is used as switch is a important problem. The R-2R ladder logic divides voltage by precise resistor ratio, which means unexpected impedence will cause error. That effect can be decreased by increasing the magnitude of R, but in real situation it is hard to produce large resistors precisely. The output from Fig.12 shows that with input increasing by 1 every step, V_{out} increase about 5.85mV on average, which is 5.86 mV in theory. By checking the largest output and smallest output both in error durable range, the DAC circuit works well.

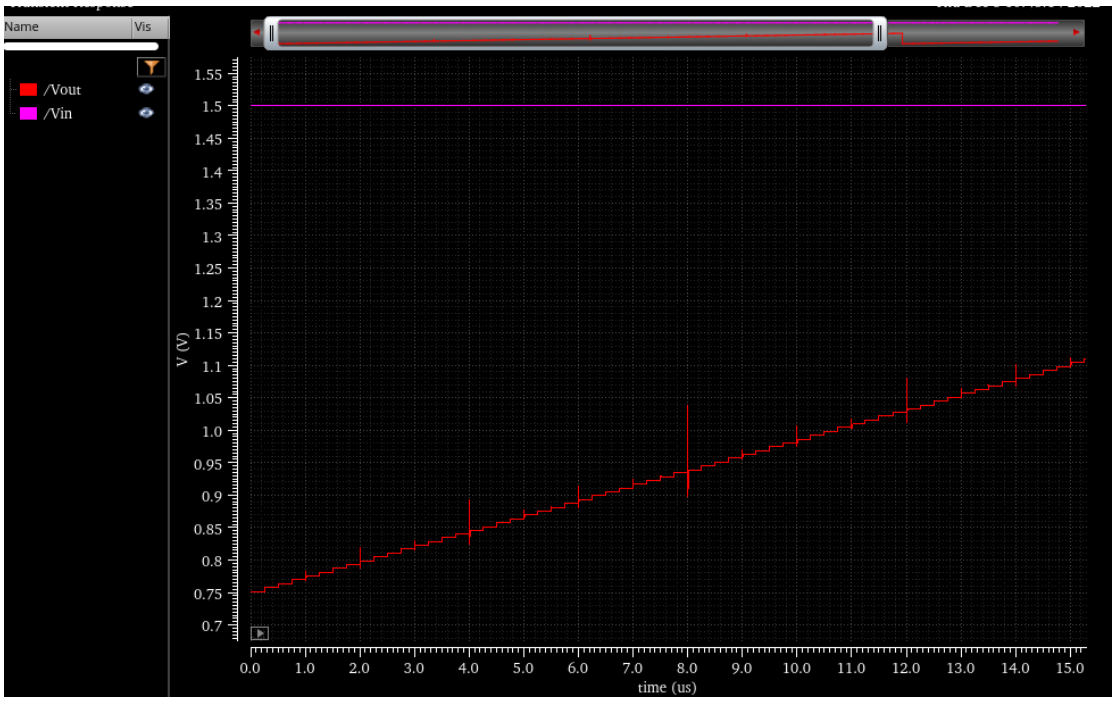

Fig.12: R-2R Ladder DAC output

E. SAR ADC

Fig.1 shows the block diagram of SAR ADC. First, analog signal is sampled by the SH circuit. Input signal S controls the sampling process and when it is low, SH circuit turns to hold mode. Then the ADC start to compare the hold voltage with the output of DAC, the comparing result will be used to verify whether the approximation is successful or not and change the digital approximate value. After 8 clock cycles, a 8-bit digital approximation for the analog signal is generated. Fig.12 shows how DAC signal makes preciser approximation bit by bit. Fig.13 shows the output change in this progress.

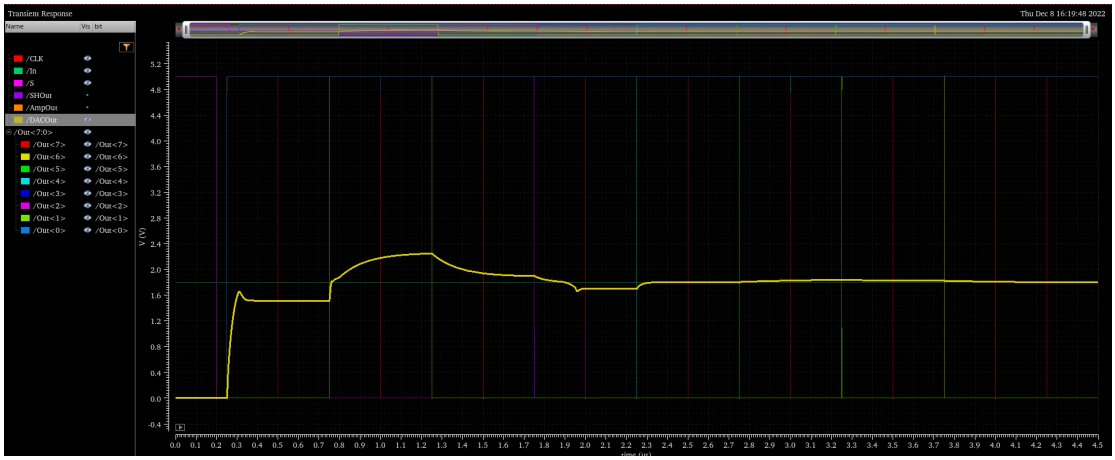

Fig.12: DAC comparing progress for SAR ADC

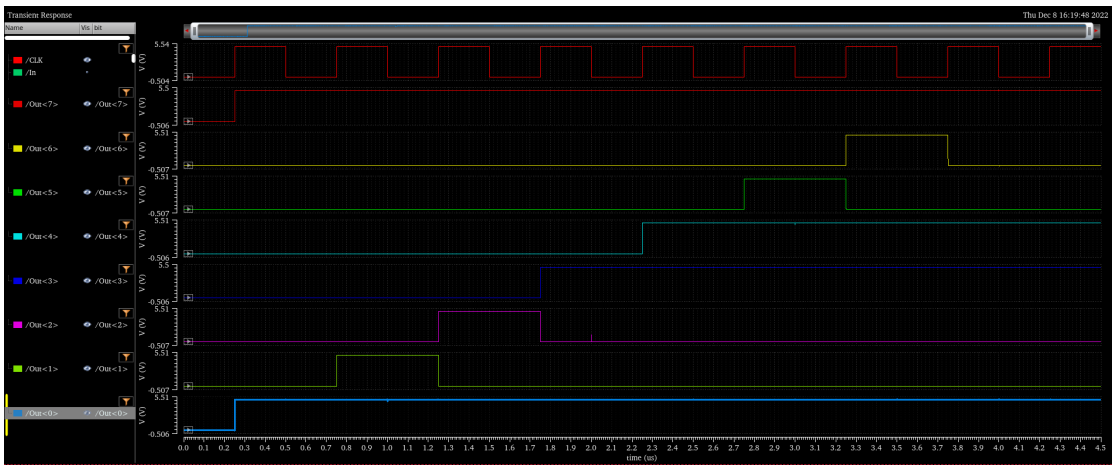

Fig.12: SAR ADC output

4. Discussion

The circuit meets almost all of the expected performance, except for input voltage range. The input range have the same range size, but the range shifts lower for 0.7V. This change decreases the current flow in Sampling and Hold circuit, which will save power. Besides, large voltage will significantly increase the leakage current and will cause obvious voltage drop in hold mode.

From the perspective of whole circuit, there are several questions which should be improved. First, there is no buffer to protect the Sampling and Hold circuit, so noise will strongly influence the signal which is held. One solution is that cascode Op Amp is not a good amplifier to be a unity-gain buffer, and it needs another folded cascode Op Amp to be the buffer, which need more schematic design. The second problem is that there is no reset structure recently, which means after every convertion, all bit should be set to 0 manually, another bunch of logic gates can be added into the control logic can solve this problem. The third problem is mentioned before, which is the 8th bit signal will be high at the beginning and cause some small error. A doubled converting time is a trade off to fix this small error, and I think which performance is more important should be decided based on the application scenario.

Reference

[1] S. Mortezapour and E. K. F. Lee, A 1-V, 8-bit successive approximation ADC in standard CMOS process, in IEEE Journal of Solid-State Circuits, vol. 35, no. 4, pp. 642-646, April 2000, doi: 10.1109/4.839925.

[2] Franco Maloberti, CMOS Sample and Hold, Data Converters, Springer Publishing Company, Incorporated, 2010, pp.213-217.

[3] D. Marche and Y. Savaria, Modeling R-2R Segmented-Ladder DACs, in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 57, no. 1, pp. 31-43, Jan. 2010, doi: 10.1109/TCSI.2009.2019396.