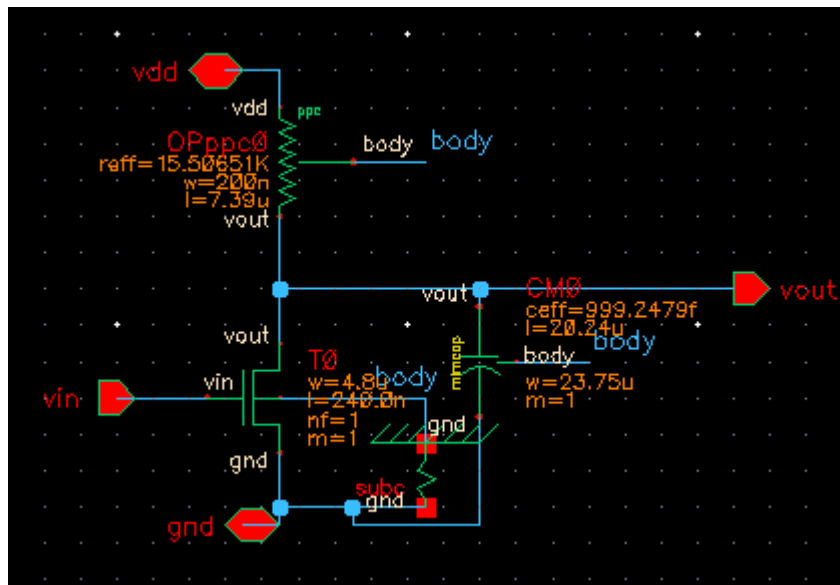


## 1. Schematic of circuit



## 2. Explanation of design process

assume  $I_D = 64.5 \mu A$ ,  $\therefore V_{GS} > V_{th}$  &  $V_{DS} \geq (V_{GS} - V_{th})$   
 $\Rightarrow V_{GS} = V_G - V_S = 0.4V$ ,  $V_{GS} - V_{th} = 0.1V$ ,  $V_{DS} = 0.2V$

$$I_D = \frac{1}{2} \mu_n C_{ox} \left( \frac{W}{L} \right) (V_{GS} - V_{th})^2$$

$$\Rightarrow 64.5 \mu A = \frac{1}{2} \times 645 \mu \times \left( \frac{W}{L} \right) (0.4 - 0.3)^2$$

$$\Rightarrow \left( \frac{W}{L} \right) = 20$$

$$R = \frac{V_{DD} - V_D}{I_D} = 15.5K \Omega$$

$$g_m = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th}) = 645 \times 10^{-6} \times 20 \times 0.1 = 1.29m$$

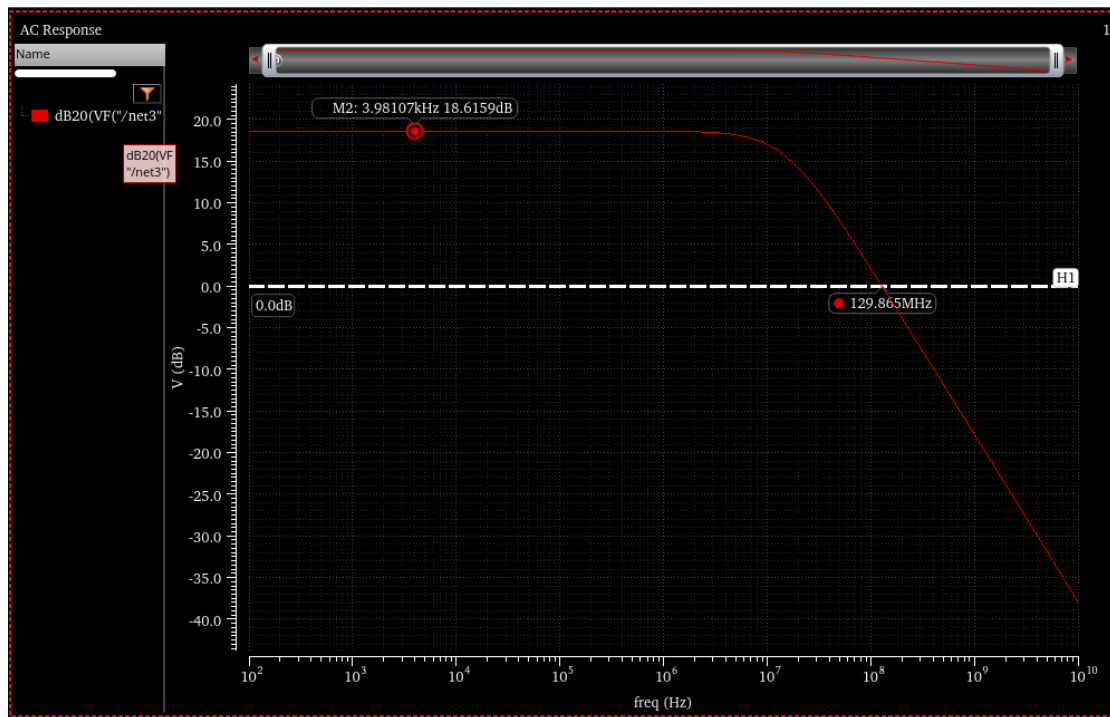
$$V_o = -g_m V_{GS} (R \parallel r_o)$$

$$r_o = \frac{1}{\lambda I_D} = 51.7K \Omega$$

$$\Rightarrow V_o = -645 \times 10^{-6} \times 20 \times 0.1 \times 11.9 \times 10^3 V_{GS} = -15.35 V_{GS}$$

$$\Rightarrow |A_v| = 20 \log 15.35 = 23.7dB$$

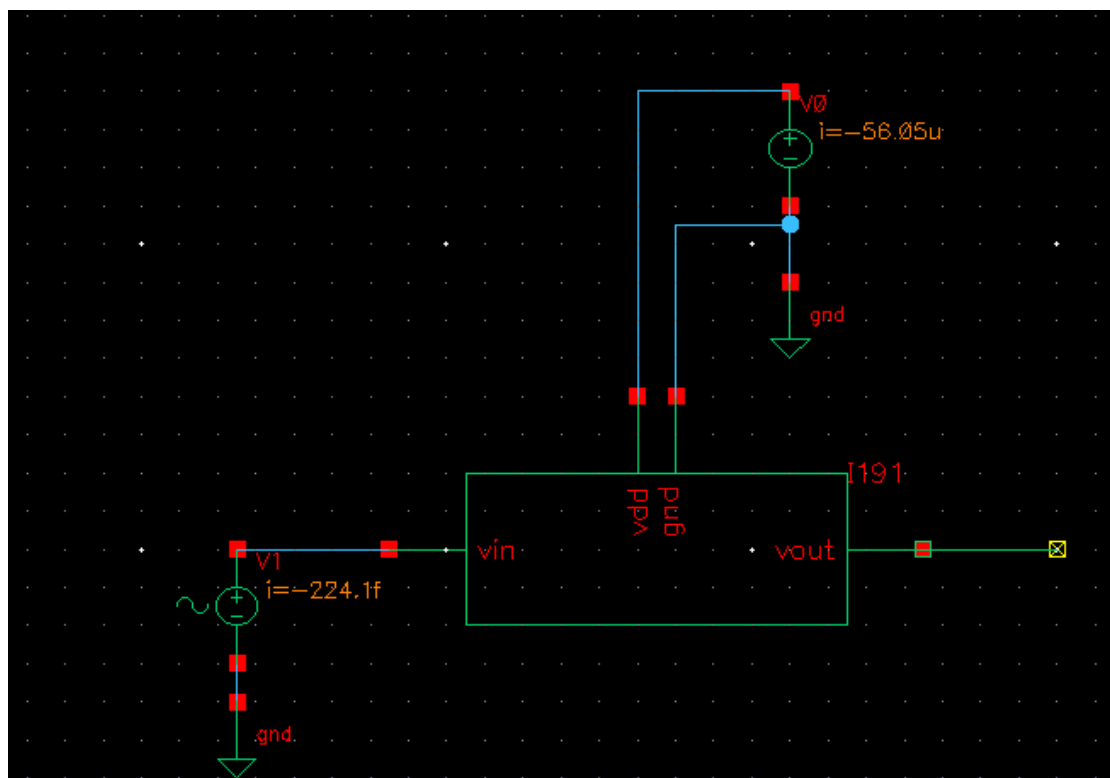
### 3. AC magnitude of schematic



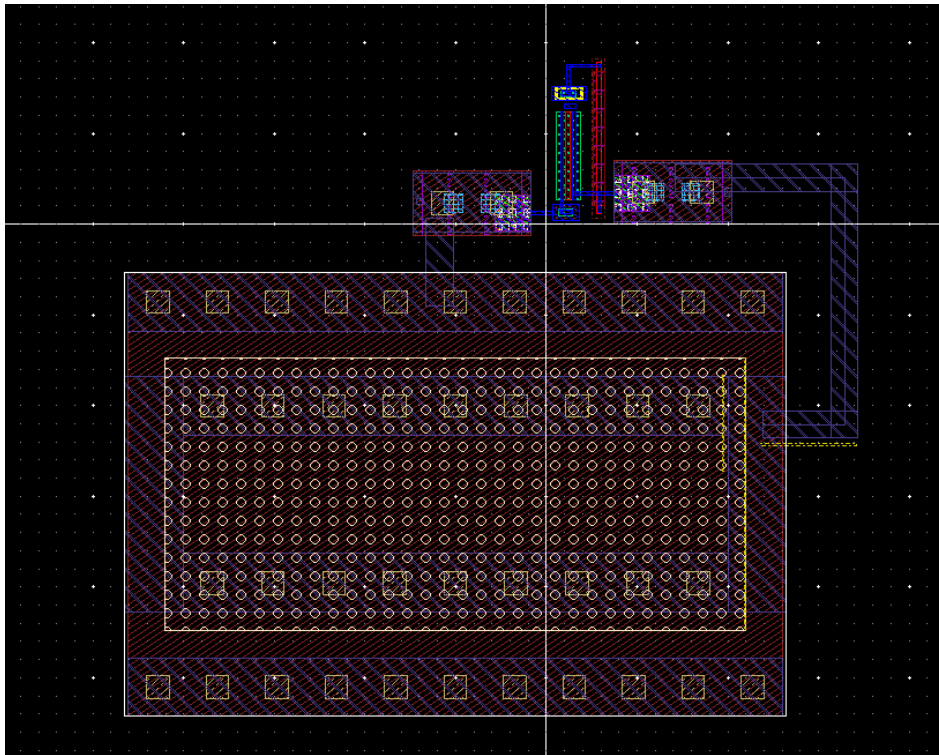
### 4. 3dB bandwidth of schematic

Expression	Value
1 bandwidth(VF"/net3")	15.27E6

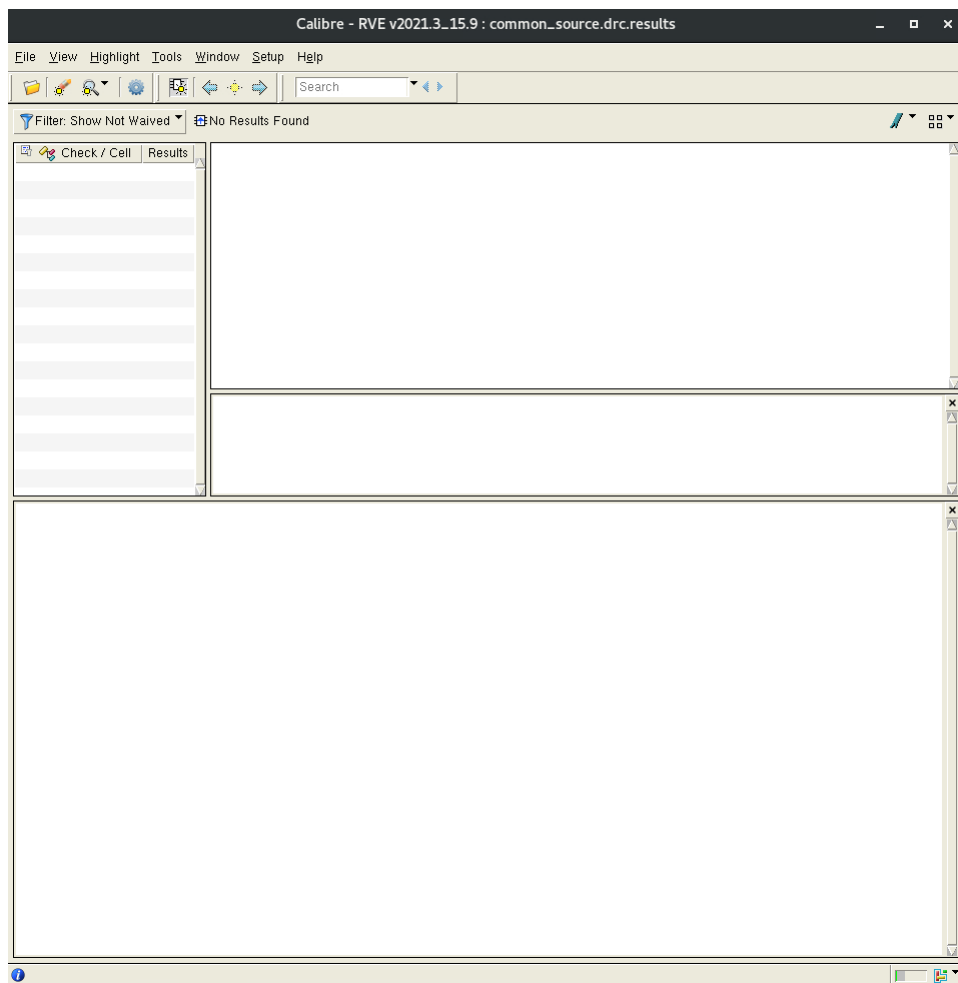
### 5. $I_D$ current of schematic



## 6. Layout



## 7. Clean DRC



## 8. Clean LVS

Calibre - RVE v2021.3\_15.9 : svdb common\_source

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Comparison Results

Layout Cell / Type	Source Cell	Nets	Instances	Ports
common_source	common_source	5L, 5S	4L, 4S	4L, 4S

Cell common\_source Summary (Clean)

CELL COMPARISON RESULTS ( TOP LEVEL )

#####  
# CORRECT #  
#####

LAYOUT CELL NAME: common\_source  
SOURCE CELL NAME: common\_source

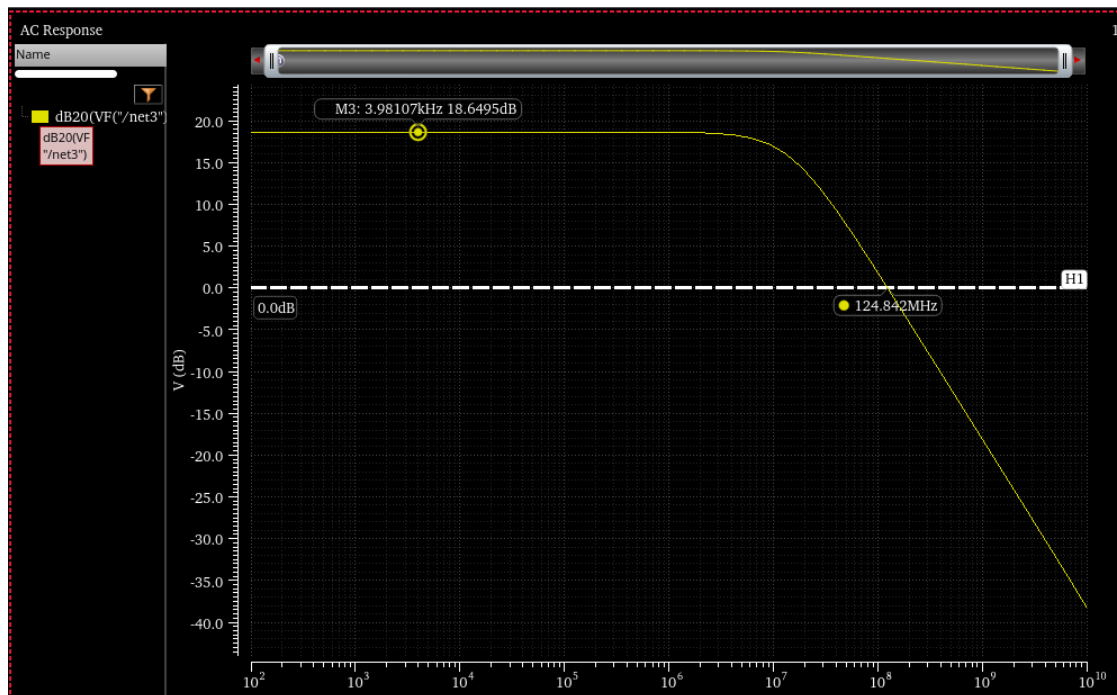
INITIAL NUMBERS OF OBJECTS

	Layout	Source	Component Type
Ports:	4	4	
Nets:	5	5	
Instances:	1	1	MN (4 pins)
	1	1	C (3 pins)
	1	1	R (3 pins)
	3	0	D (2 pins)
	1	1	subc (2 pins)
Total Inst:	7	4	

NUMBERS OF OBJECTS AFTER TRANSFORMATION

	Layout	Source	Component Type
Ports:	4	4	

## 9. AC magnitude of postpex



#### 10. 3dB bandwidth of postpex

	Expression	Value
1	bandwidth(VF"//...	14.68E6

#### 11. $I_D$ current of postpex

