Low-Subthreshold-Swing Tunnel Transistors

Qin Zhang, Wei Zhao, *Student Member, IEEE*, and Alan Seabaugh, *Fellow, IEEE*

Abstract—A formula is derived, which shows that the subthreshold swing of field-effect interband tunnel transistors is not limited to 60 mV/dec as in the MOSFET. This formula is consistent with two recent reports of interband tunnel transistors, which show lower than 60-mV/dec subthreshold swings and provides two simple design principles for configuring these transistors. One of these principles suggests placing the gate adjacent to the tunnel junction. Modeling of this configuration verifies that sub-60-mV/dec swing is possible.

Index Terms—Silicon-on-insulator (SOI), subthreshold swing, tunnel transistor.

I. INTRODUCTION

IN A FIELD-EFFECT transistor (FET), the minimum voltage swing needed to turn a transistor "ON" is an important figure of merit that ultimately sets the minimum power supply voltages and the minimum power dissipation of a technology. The subthreshold swing is defined as the gate voltage required to change the drain current by one order of magnitude, one decade. In the MOSFET, the subthreshold swing is limited to $(kT/q)\ln 10$ or 60 mV/dec at room temperature, and with scaling, the subthreshold swing increases [1] (k is Boltzmann's constant, q is the electron charge, and T is the temperature). This increase in subthreshold swing as gate length is decreased marks a significant fundamental limitation of conventional FETs. In this letter, we show analytically that: 1) certain interband tunnel transistors can have subthreshold swings below 60 mV/dec and 2) that the subthreshold swing is minimized by engineering the transistor geometry to enhance the gate control of the tunnel-junction bias-voltage and internal electric field.

In recent years, a growing number of transistors have been reported, which explore the use of the field effect to gate an interband tunneling current [2]–[7]. Several of these authors have characterized the subthreshold swing. In the carbon nanotube field-effect transistor of Appenzeller *et al.* [5], a subthreshold swing of 40 mV/dec was measured in a double-gated transistor in which interband tunnel current flows through an n-p-n channel modulated by a top gate. In simulations, Bhuwalka *et al.* [4] have shown in a vertical gated p-i-n Si/SiGe interband tunneling transistor that subthreshold swings of 44 mV/dec can be achieved. In a lateral embodiment of the p-i-n Si interband tunnel transistor, Wang *et al.* [3] have shown
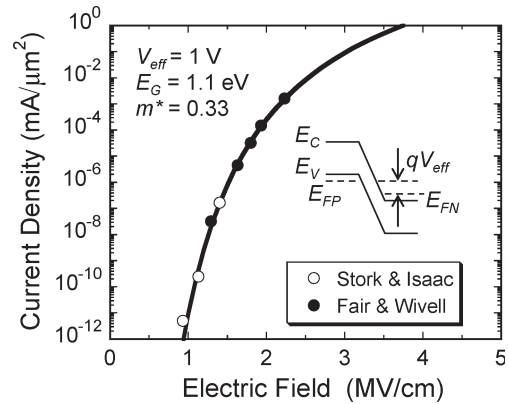
Fig. 1. Silicon tunneling current density versus electric field for a reverse-junction bias of 1 V showing the excellent experimental agreement between (1), solid line, and theory measurements (after Taur *et al.* [10]) using the data of Stork and Isaac [11] and Fair and Wivell [12]. The inset shows the p$^+$-n$^+$ tunnel-junction energy band diagram under bias V_{eff}.

by simulation that subthreshold swings of 15 mV/dec and even smaller are achievable and conclude that the subthreshold swing is not limited by kT/q. In this letter, we outline the reasons for the low subthreshold swing in tunnel transistors and analyze a new transistor configuration for low subthreshold swing transistor action.

II. SUBTHRESHOLD SWING OF TUNNEL TRANSISTORS

The subthreshold swing S of a FET is defined by $S = \ln 10 \, dV_{\text{GS}}/d(\ln I_D)$ [8], where V_{GS} is the transistor gate–source voltage and I_D is the drain current. In an interband tunneling transistor, the drain current flows across a degenerately doped p$^+$-n$^+$ tunnel junction, a transport mechanism that is particularly well described, in the reverse, Zener tunneling direction, by Sze [9]

$$I = aV_{\text{eff}}\xi \exp\left(-\frac{b}{\xi}\right) \tag{1}$$

where V_{eff} is the tunnel–junction bias (see the inset of Fig. 1), ξ is the electric field, and a and b are coefficients determined by the materials' properties of the junction and the cross-sectional area of the device A. Specifically, $a = Aq^3\sqrt{2m^*/E_g}/4\pi^2\hbar^2$ and $b = 4\sqrt{m^*}E_g^{3/2}/3q\hbar$, where m^* is the carrier effective mass, E_g is the energy band gap, and $\hbar$ is Planck's constant divided by 2π. This simple analytic expression for interband tunneling (1) is in phenomenal agreement with the measurements of reverse biased p$^+$-n$^+$ tunnel junctions [10]–[12]
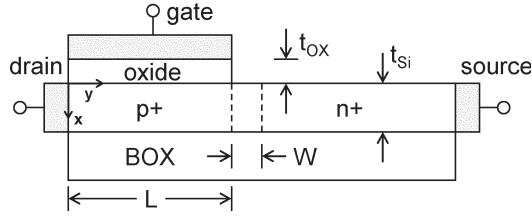
Fig. 2. Schematic cross section of an interband tunnel transistor where the ultrathin Si body is heavily doped to form a p^+-n^+ tunnel junction, and the gate is placed over the fully depleted p-side.
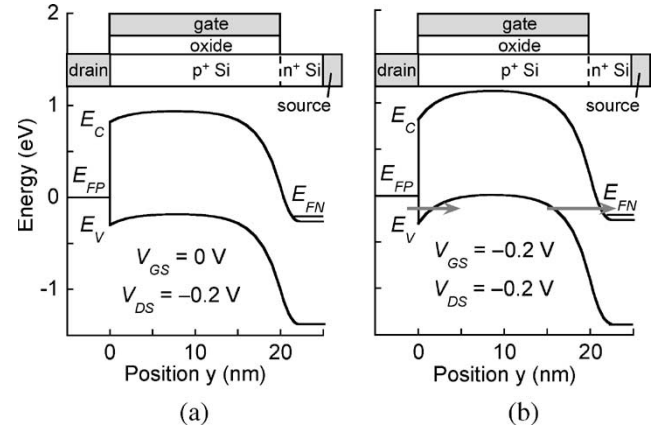

Fig. 3. Energy band diagrams at $x = 0$ for the Si interband tunneling transistor with (a) zero and (b) negative gate voltages. The simulated gate oxide thickness is 1 nm, the Si layer is 2 nm, the n and p net doping densities are $10^{20}/\mathrm{cm}^3$, and the gate length is 20 nm. Note that as the gate–source bias changes by 0.2 V, the electrostatic potential on the p-side shifts by approximately 0.2 V, i.e., $dV_{\mathrm{eff}}/dV_{\mathrm{GS}} \sim 1$. The gray arrows in (b) indicate the ON-state tunneling paths.

spanning eight orders of magnitude in current, as shown in Fig. 1, with effective mass as the sole fitting parameter.

The derivative of the tunneling current expression of (1) with respect to the gate–source voltage can be used to determine an expression for the subthreshold swing of a field-effect tunneling transistor.

$$S = \ln 10 \left[\frac{1}{V_{\mathrm{eff}}} \frac{dV_{\mathrm{eff}}}{dV_{\mathrm{GS}}} + \frac{\xi + b}{\xi^2} \frac{d\xi}{dV_{\mathrm{GS}}} \right]^{-1}. \qquad (2)$$

There are two terms in the denominator of (2), which can be maximized in order to achieve a low subthreshold swing, and these terms are not limited by kT/q. According to the first term, the transistor should be engineered so that the gate–source voltage directly controls the tunnel-junction bias V_{eff}; this suggests a transistor geometry with a thin and/or high-κ gate dielectric and an ultrathin body to assure that the gate field directly modulates the channel. For an equivalent oxide thickness approaching 1 nm, $dV_{\mathrm{eff}}/dV_{\mathrm{GS}} \approx 1$ and the first term in the denominator of (2) is approximately inversely related to V_{GS}. Accordingly, the subthreshold swing in a tunnel transistor increases with gate–source voltage, a characteristic that has been observed in both measurements [5] and simulations [3], [4].

A second way to lower the subthreshold voltage swing is described by the second term in the denominator of (2), which says that the derivative of the junction electric field on the gate–source voltage should be maximized. This is a primary basis for gate control in the interband tunnel transistor of Bhuwalka *et al.* [4]. In such a device, the gate–source voltage changes the tunneling width and increases the junction electric field. In practice, the tunnel-junction bias and the junction electric field are coupled and cannot be engineered independently.

III. LOW SUBTHRESHOLD-SWING DEVICE DESIGN

Using the design guidance of (2), we explore a new transistor geometry toward achieving low subthreshold-swing operation. A schematic cross section of the transistor is shown in Fig. 2 and is comprised of a silicon-on-insulator (SOI) structure in which a lateral p^+-n^+ tunnel junction is formed in an ultrathin semiconductor body; a gate is placed on the p-side. The gate is aligned to the junction on the p-side to facilitate control of the p-side electrostatic potential; the p region is fully depleted for zero gate bias.

This device geometry is amenable to an analytic solution for the potential profile using a two-dimensional (2-D) Poisson

equation, a solution method described by Young [13]. This analysis ignores the effects of statistical dopant fluctuations, which will become increasingly important as the transistor dimensions are minimized. On the p-side, the potential $\phi(x, y)$ is given by

$$\frac{d^2\phi(x,y)}{dx^2} + \frac{d^2\phi(x,y)}{dy^2} = \frac{qN_A}{\varepsilon_{\mathrm{Si}}}$$
$$\text{for} \quad 0 \le x \le t_{\mathrm{Si}} \quad \text{and} \quad 0 \le y \le L \quad (3)$$

where N_A is the acceptor doping concentration on the p-side, $\varepsilon_{\mathrm{Si}}$ is the Si dielectric constant, t_{Si} is the thickness of the Si layer, and L is the gate length. Using a parabolic approximation at low drain-to-source voltage V_{DS} gives $\phi(x, y) = c_0(y) + c_1(y)x + c_2(y)x^2$, where the coefficients c_0, c_1, and c_2 are functions of y only. The n-side is unmodulated by the gate and, therefore, can be treated as a one-dimensional (1-D) problem with the potential given by

$$\frac{d^2\phi(y)}{dy^2} = -\frac{qN_D}{\varepsilon_{\mathrm{Si}}} \qquad \text{for } 0 \le x \le t_{\mathrm{Si}} \text{ and } L \le y \le L + W$$
$$(4)$$

where N_D is the donor doping concentration on the n-side, and W is the depletion length on the n-side. Four boundary conditions are applied: 1) constant potential on the surface between the semiconductor and the gate oxide; 2) zero electric field in the x-direction on the surface between the semiconductor and the buried oxide; 3) continuous potential and electric field at the p-n junction; and 4) 0.3-eV Schottky barrier at the drain contact. Equations (3) and (4) can then be solved to obtain the surface potential and energy band diagrams versus drain–source and gate–source bias.

The transistor operation can be understood from the computed energy band diagrams in Fig. 3 for a drain–source bias of

TABLE I
CALCULATED SUBTHRESHOLD SWINGS FOR THE Si INTERBAND TUNNEL
TRANSISTOR OF FIG. 2 VERSUS GATE VOLTAGE

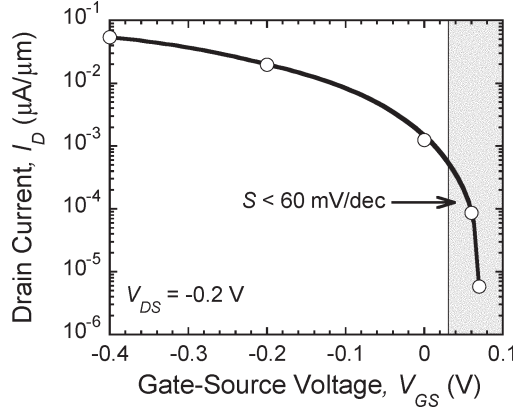| V_{GS} (mV)	ξ (MV/cm)	V_{eff} (mV)	S (mV/dec)
10	3.38	6	13.3
0	3.40	16	33.5
-10	3.42	26	56.4
-20	3.44	35	60.9
-30	3.47	45	81.4

Fig. 4. Simulated transfer characteristic of the proposed Si interband tunneling transistor using the Synopsys 2-D simulator.

-0.2 V; these band diagrams correspond to the surface of the SOI at $x = 0$. The transistor off condition is shown in Fig. 3(a); for a gate–source voltage of zero, the p-side is depleted and the interband tunneling probability is low. When a negative gate voltage is applied, the valence band on the p-side is raised above the Fermi level on the n-side turning the interband tunneling and the transistor ON [Fig. 3(b)]. In this transistor geometry, the gate screens the drain field enabling current saturation and isolation.

Using these energy band simulations and this transistor geometry to compute the derivatives in (2), the bias dependence of the subthreshold swing can be estimated, given that b is 33 MV/cm for Si, and V_{eff} and ξ are extracted from the simulated band diagrams [Table I]. The subthreshold swing is dependent on the applied gate–source bias, and it is apparent that this device can achieve smaller than 60 mV/dec over a small bias range near zero gate voltage. For the tunnel transistor, it is clear that the minimum subthreshold swing will not be the most important parameter. Rather, it will be necessary to define the minimum voltage swing needed to achieve a given ON-to-OFF current ratio.

The Synopsis device simulator [17] [former Integrated Systems Engineering (ISE)] is used to compute the 2-D energy band and channel electric-field profiles to verify agreement with the analytic model. The computed electric-field distribution is then used with (1) to determine the current distribution in the channel, allowing a comparison with our analytic calculations. The I_D–V_{GS} transfer characteristic, for the device geometry previously given, is shown in Fig. 4. The 2-D simulations are in good agreement with the analytic model; low subthreshold

swing $\sim$ 7 mV/dec occurs near $V_{GS} = 0.07$ V, and the low subthreshold swings can be kept within a small gate–source voltage, 40 mV, in reasonable agreement with the results shown in Table I. From Fig. 4, a voltage swing of 140 mV provides an ON-to-OFF current ratio of 10^3 compared to a MOSFET swing of 180 mV. The voltage swing of 140 mV in the tunnel transistor should be reduced by changing the channel materials to, e.g., Ge or InAs while increasing the current drive.

IV. DISCUSSION

Band-to-band Si tunnel transistors have been demonstrated with ON-state current density as high as 100 μA/μm [6], which is below the MOSFET's 1000 μA/μm (90-nm process node) [14]. Simulations indicate that higher interband current density (850 μA/μm) can be obtained using Ge channels [4]. Tunnel transistors have much lower off leakage, < 0.1 nA/μm [6], than the MOSFET, $\sim$ 150 nA/μm [15], for the same technology node, 90 nm, due to the high barrier imposed by the p-n junction and resulting in much lower static power dissipation. The low subthreshold swing of the tunnel transistor suggests low power applications; subthreshold logic circuits [16] are of particular relevance to this type of transistor.

V. CONCLUSION

An analytic expression was derived, which showed that the subthreshold swing of interband tunnel transistors was a function of the gate–source voltage and can beat the MOSFET limit of 60 mV/dec about certain gate biases. Based on this expression, a new SOI tunnel transistor was proposed and simulated, outlining some of the attributes of the low subthreshold swing in interband tunneling transistors.

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