Homework 2 Written

The pdf you submit must look exactly like this with the answers and all supporting works shown on the the page with the question.

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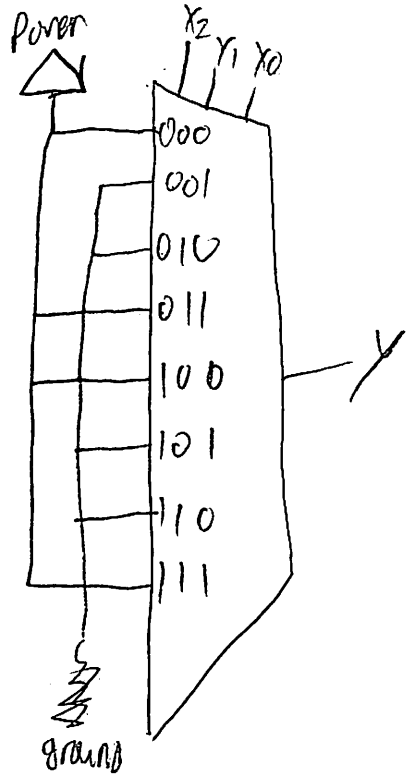
1. (4 points) Given only an 8-1 multiplexer and constants 0 and 1 implement a circuit that behaves like the following function: $m_0+m_3+m_4+m_7$ There are 3 input variables for this problem x_2, x_1, x_0 .

First draw a truth table

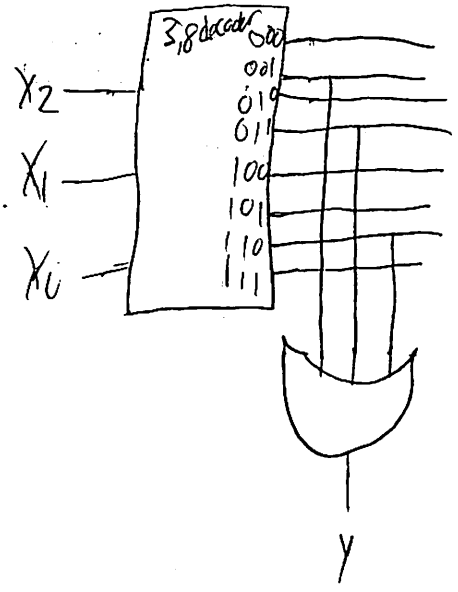
x_2	x_1	x_0	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1



2. (3 points) Given only an 3-8 one hot decoder and an OR gate implement a circuit that behaves like the following function: $m_1+m_3+m_6$ There are 3 input variables for this problem x_2, x_1, x_0 .

Truth table

X_2	X_1	X_0	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0



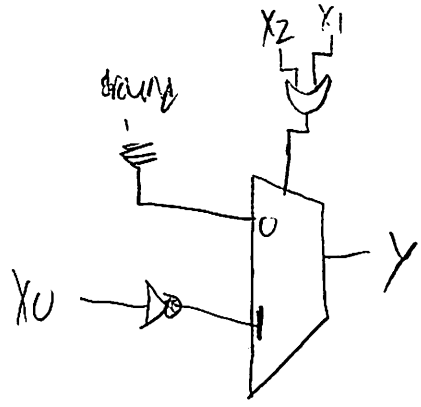
3. (3) Given only a mux, a not gate, and a 2 input OR gate implement a circuit that behaves like the following function: $M_2 \times M_4 \times M_6$ There are 3 input variables for this problem x_2, x_1, x_0 .

	X_2	X_1	X_0	Y
0	0	0	0	1
1	0	0	1	1
2	0	1	0	0
3	0	1	1	1
4	1	0	0	0
5	1	0	1	1
6	1	1	0	0
7	1	1	1	1

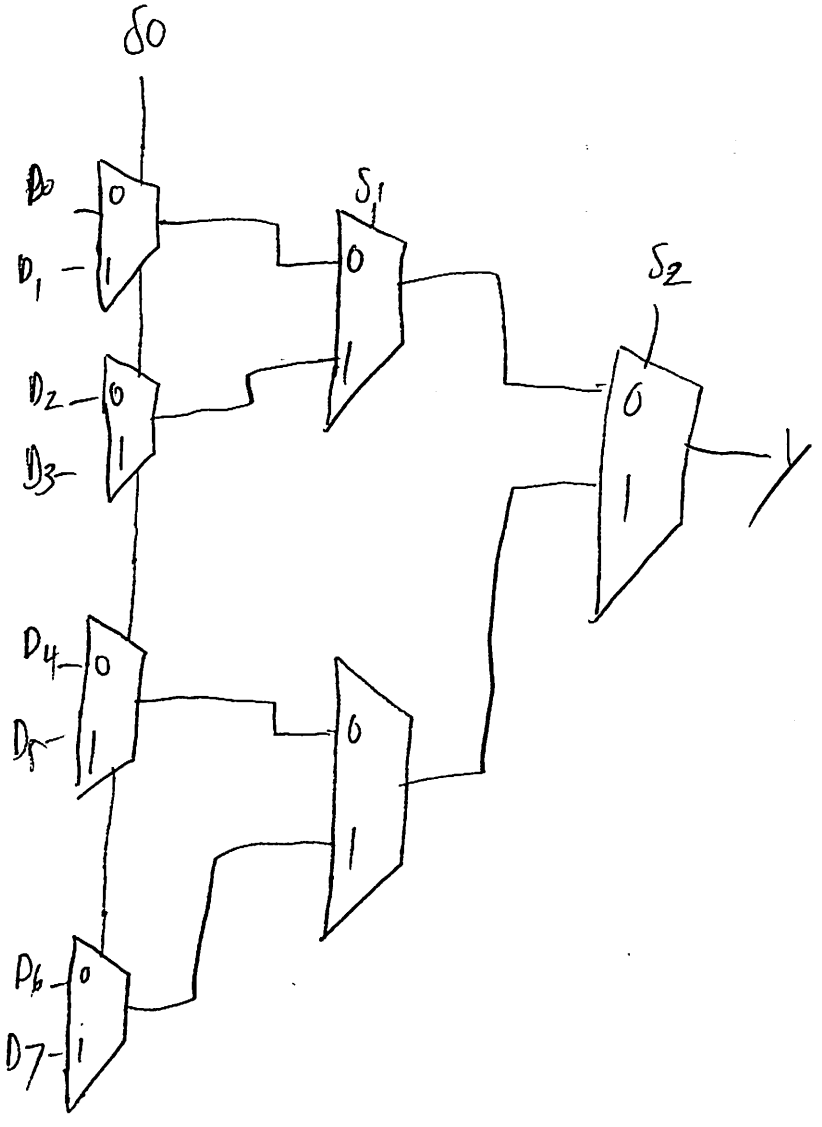
POS: $(X_0 + \bar{X}_1)(X_0 + \bar{X}_2)$

SOP: $\bar{X}_2 \bar{X}_1 + X_0$

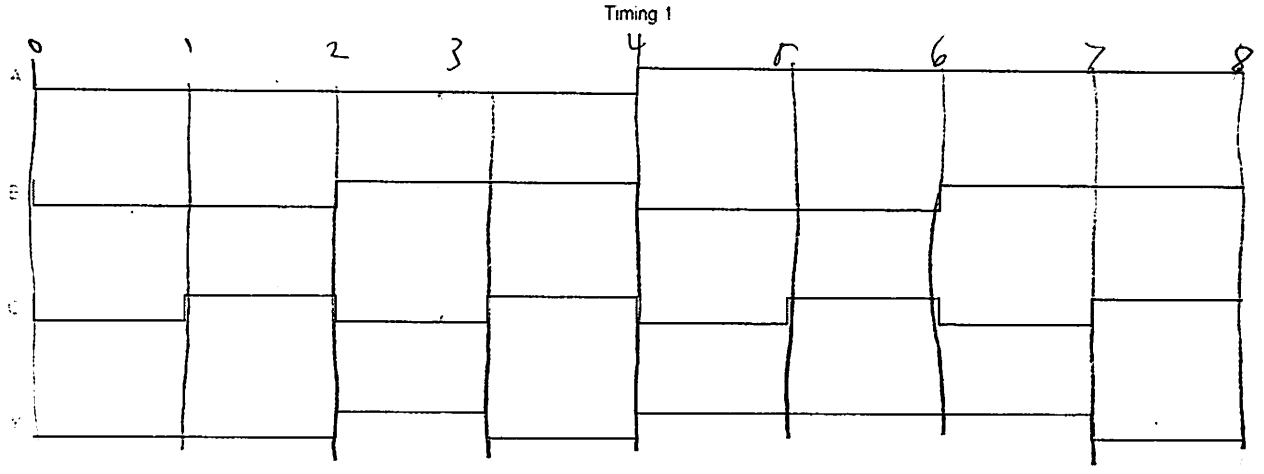
X_2	X_1	Y
0	1	$\bar{X}_0$
1	0	$\bar{X}_0$
1	1	$\bar{X}_0$



4. (3 points) Use only 2 – 1 multiplexers to create an 8-1 multiplexer.

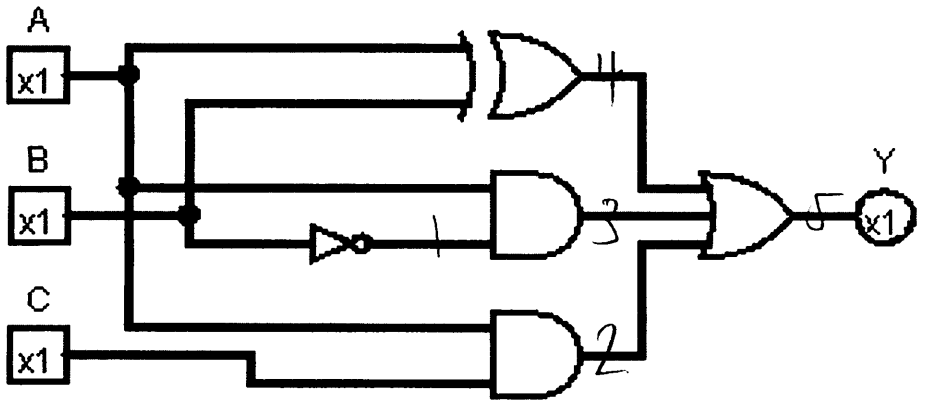


5. (4) Fill in the truth table based on the following timing diagram. Assume no delays in the circuit.



A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

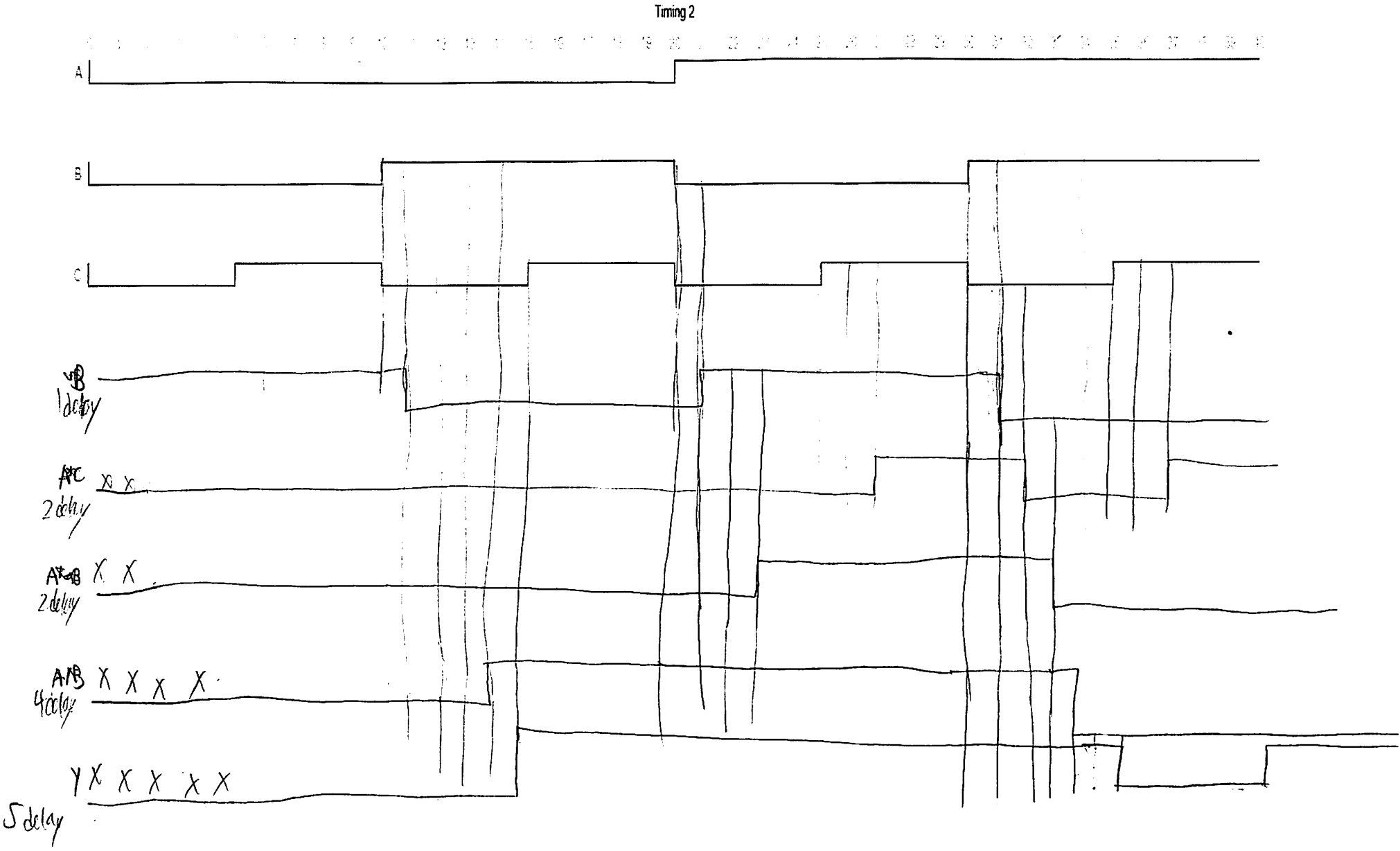
6. (8) Give the following circuit and delays complete the timing diagram.



Element	Delay
NOT	1
AND	2
XOR	4
OR	1

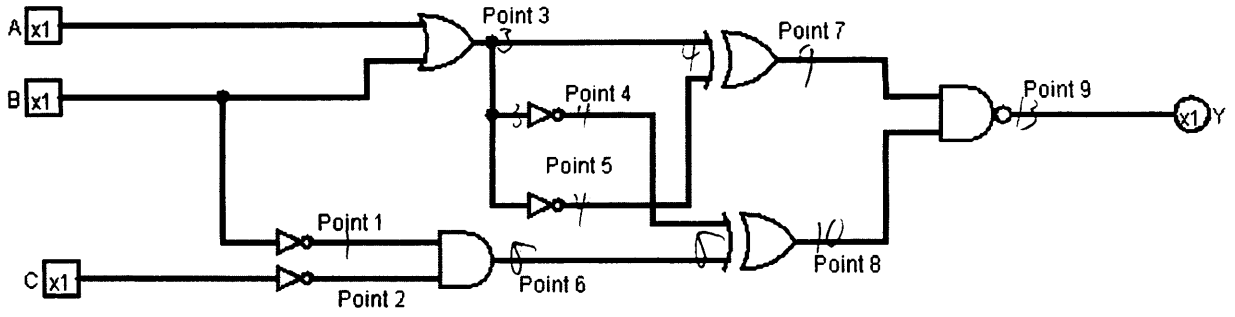
A	B	C	y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

$Y = (A \oplus B) + (\bar{B}A) + (AC)$


Timing 2
A
B
C
B
1 delay
AC
2 delay
AB
2 delay
A/B
4 delay
Y
5 delay

7. (4.5 points)Given the following circuit and the propagation delays in the following table, what are the propagation delays at each marked point? There are 9 separate points.

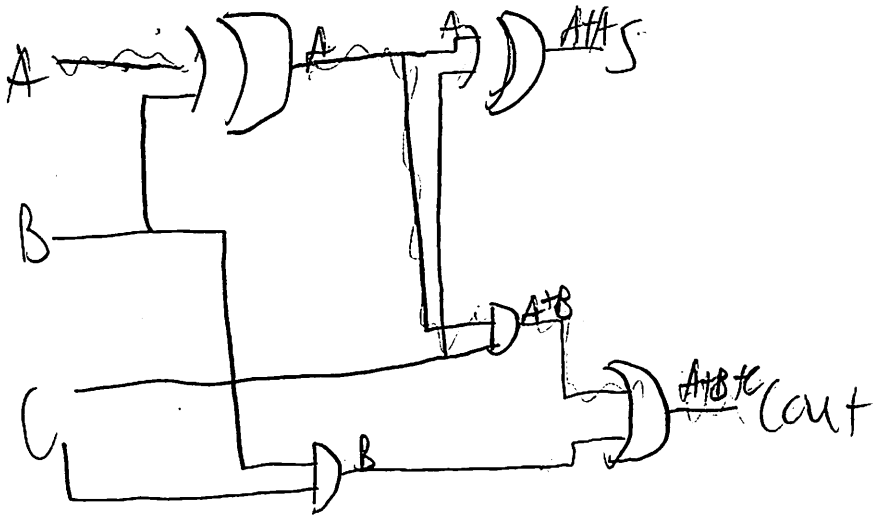
Component	Delay
Not	1 ns
OR	3 ns
XOR	5 ns
NAND	3 ns
AND	4 ns



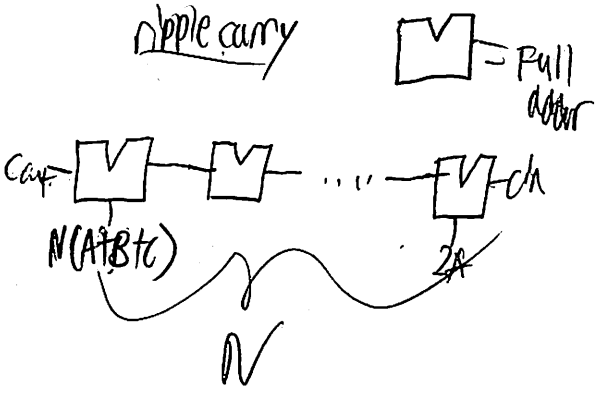
Point	Delay
1	1
2	1
3	3
4	4
5	4
6	5
7	9
8	10
9	13

8. (3 points) Given that each XOR gate has a delay of *A* ns, each AND gate has a delay of *B* ns, and each OR gate has a delay of C ns, what is the propagation delay of the worst case path in an N bit ripple carry adder? Assume that the delays between the elements are close enough that the worst case path is the one that contains the most elements along it.

For a full adder it has 2 XOR gates, 2 ands, and 1 OR gates. A ripple carry adder uses N full adders for it to work. To get the propagation delay we need to calculate the propagation delay for a Full adder, and multiply it by N.



XOR = A
AND = B
OR = C



N(A+B+C)