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Quiz #3

1. For a direct-mapped cache design with a 32-bit word address, the following bits of the address are used to access the cache.

Tag	**Index**	**Offset**
10-31	9-5	4-0

1.1 What is the cache block size(in words)? (8 points)
Solution:
$2^5 = 32$ (There are five Offset bits.)

1.2 How many entries does cache have? (8 points)
Solution:
$2^5 = 32$ (There are five Index bits.)

1.3 What is the ratio between total bits required for such a cache implementation over the data storage bits? (8 points)
Solution:
$\frac{valid+tag+data}{data} = ratio$

$\frac{1+22+32*32}{32*32} = 1.02$

Starting from power on, the following word-addressed cache references are recorded.

Address											
0	4	16	132	232	160	1024	30	140	3100	180	2180

1.4 How many blocks are replaced? (8 points)

Solution:
M.M Block Address : Address DIV/32
Tag : Address DIV/32
Index : Address MOD/32

Address	M.M Block Address	tag	index	Replace	Hit
0	0	0	0	N	N
4	0	0	0	N	Y
16	0	0	0	N	Y
132	4	0	4	N	N
232	7	0	7	N	N
160	5	0	5	N	N
1024	32	1	0	Y	N
30	0	0	0	Y	N
140	4	0	4	N	Y
3100	96	3	0	Y	N
180	5	0	5	N	Y
2180	68	2	4	Y	N

There are four blocks which are replaced.

1.5 What is the hit ratio? (8 points)
Solution:
4/12 = 0.33

1.6 List the final state of the cache, with each valid entry represented as a record of ⟨ index, tag, data ⟩. (10 points)
Solution:
⟨ index, tag, data ⟩
⟨ 00000, 00011, mem[96] ⟩
⟨ 00100, 00010, mem[68] ⟩
⟨ 00101, 00000, mem[5] ⟩
⟨ 00111, 00000, mem[7] ⟩

2. We will look at the different ways capacity affects overall performance. In general, cache access time is proportional to capacity. Assume that main memory accesses take 60ns and that memory accesses are 36% of all instructions. The following table shows data for L1 caches attached to each of two processors, P1 and P2.

	L1 Size	**L1 Miss Rate**	**L1 Hit Time**
P1	2 KiB	9.00%	0.66ns
P2	4 KiB	7.00%	0.90ns

2.1 Assuming that the L1 hit time determines the cycle times for P1 and P2, what are their respective clock rates? (8 points)
Solution:
P1 : $1/0.66n = 1.52GHz$ P2 : $1/0.90n = 1.11GHz$

2.2 What is the Average Memory Access Time for P1 and P2? (8 points)
Solution
AMAT = Hit time + Miss rate * Miss penalty

AMAT for $P1 = 0.66 + (9\% * 60) = 6.06ns$
AMAT for $P2 = 0.90 + (7\% * 60) = 5.10ns$

2.3 Assuming a base CPI of 1.0 without any memory stalls, what is the total CPI for P1 and P2? Which processor is faster? (8 points)
Solution:
CPI for P1 $= 1 + 0.36 * 0.09 * 60/0.66 = 3.95$
CPI for P2 $= 1 + 0.36 * 0.07 * 60/0.9 = 2.68$

performance $\propto$ (clock rate/CPI)
$1.52/3.95 = 0.38 < 1.11/2.68 = 0.41$
$\therefore$ P2 faster

For the next three problems, we will consider the addition of an L2 cache to P1 to presumably make up for its limited L1 cache capacity. Use the L1 cache capacities and hit times from the previous table when solving these problems. The L2 miss rate indicated is its local miss rate.

L2 Size	**L2 Miss Rate**	**L2 Hit Time**
1 MiB	90%	5.62ns

2.4 What is the AMAT for P1 with the addition of an L2 cache? Is the AMAT better or worse with the L2 cache? (8 points)
Solution:
AMAT = Hit time_{L1} + Miss rate_{L1} * (Hit time_{L2} +Miss rate_{L2} * Miss $\text{penalty}_{\text{L2}}$)

AMAT $= 0.66 + 0.09 * (5.62 + 0.90 * 60) = 6.03ns$ $(6.03 < 6.06)$
$\therefore$ AMAT is better with the L2 cache.

2.5 Assuming a base CPI of 1.0 without any memory stalls, what is the total CPI for P1 with the addition of an L2 cache? (8 points)
Solution:
CPI $= 1 + 0.36 * 0.09 * (5.62/0.66 + 0.9 * 60/0.66) = 3.93$

2.6 Which processor is faster, now that P1 has an L2 cache? If P1 is faster, what miss rate would P2 need in its L1 cache to match P1's performance? If P2 is faster, what miss rate would P1 need in its L1 cache to match P2's performance? (10 points)
Solution:
performance $\propto$ (clock rate/CPI)

$1.52/3.93 = 0.39 < 1.11/2.68 = 0.41$
$\therefore$ P2 is faster than P1.

$\frac{1.11}{2.68} = \frac{1.52}{1+0.36*MR*(5.62/0.66+0.9*60/0.66)}$

$MR = 8.2\%$