National Chung Cheng University
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Quiz #2 Solution

1. IEEE 754-2008 contains a half precision that is only 16 bits wide. The leftmost bit is still the sign bit, the exponent is 5 bits wide and has a bias of 15, and the mantissa is 10 bits long. A hidden 1 is assumed. Write down the bit pattern to represent -1.5625 $\times 10^{-1}$. (10 points)
   Solution:
   1.5625 $\times 10^{-1}$ (decimal) = 0.00101 (binary)

   Let's normalise now. First we bring the first '1' to the left of the '.' by multiplying by a non-zero exponent:

   $0.00101 = 1.01000 \times 2^{-3}$

   Next we get rid of the '1' before the '.' and we add 15 to the exponent:

   0.01×2^{12}

   We convert the exponent to binary as well:

   0.01×2^{1100}

   Finally we need to set the sign bit to '1' because the number is negative, so the result is:

   1 01100 0100000000

   where the first bit is the sign, the next 5 bits are the exponent, and the remaining 10 are the mantissa.

   The range and accuracy for this 16 bit format are less than single precision IEEE 754 format, for we have less bits for the exponent and the mantissa.

2. Assume that individual stages of the datapath have the following latencies: (30 points)

Instruction Fetch **(IF)**	Instruction Decode **(ID)**	Execute **(EX)**	Memory Access **(MEM)**	Register Write Back **(WB)**
200ps	300ps	150ps	400ps	150ps

a. What is the clock cycle time in a pipelined and non-pipelined processor? (10 points)

b. What is the total latency of an `lw` instruction in a pipelined and non-pipelined processor? (10 points)

c. If we can split one stage of the pipelined datapath into two new stages, each with half the latency of the original stage, which stage would you split and what is the new clock cycle time of the processor? (10 points)

Solution:

a. Pipelined: cycle time determined by longest latencies : 400ps
Non-pipelined: cycle time determined by sum of all stages: 200+300+150+400+150=1200ps.

b. `lw` instruction uses all 5 stages.
Pipelined processor takes 5 cycles at 400ps per cycle for total latency of 2000ps.
Non-pipelined processor takes 200+300+150+400+150=1200ps.

c. Split **(MEM)** stage into two stages of 200ps. New clock cycle time is 300ps.

3. The following sequence of instructions, and assume that it is executed on a 5-stage pipelined datapath: (30 points)

```
ADD   R5,  R2,  R1
LW    R3,  4(R5)
LW    R2,  0(R2)
OR    R3,  R5,  R3
SW    R3,  0(R5)
```

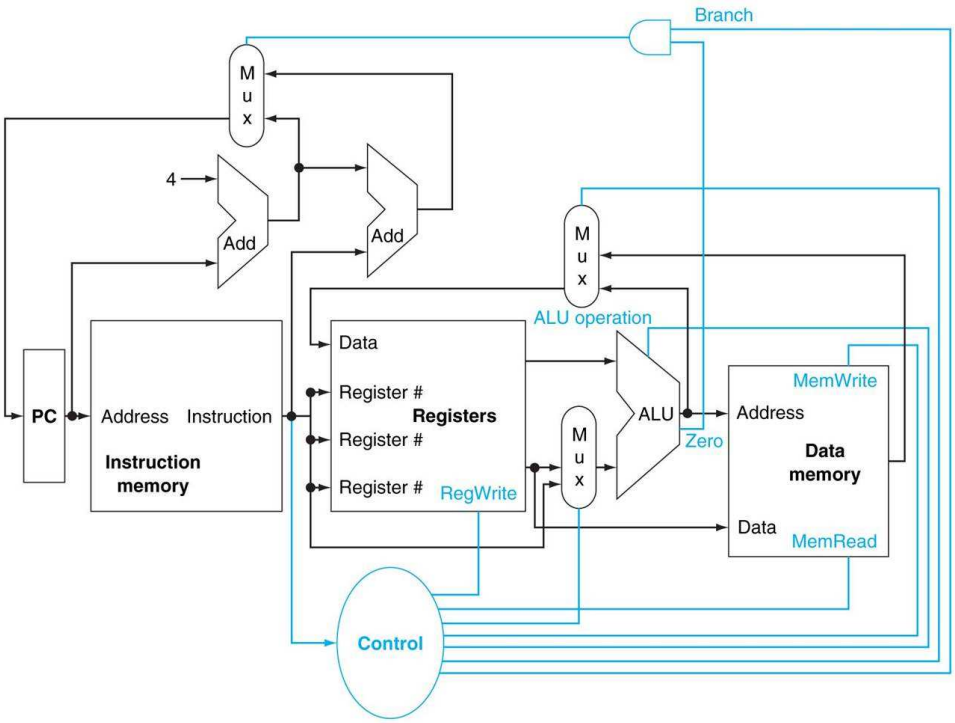
a. If there is no forwarding or hazard detection, insert `nop`s to ensure correct execution. (15 points)
Solution:

```
ADD   R5,  R2,  R1
NOP
NOP
LW    R3,  4(R5)
LW    R2,  0(R2)
NOP
OR    R3,  R5,  R3
NOP
NOP
SW    R3,  0(R5)
```

b. Repeat (a) but now use `nop`s only when a hazard cannot be avoided by changing or rearranging these instructions. You can assume register R7 can be used to hold temporary values in your modified code. (15 points)
Solution:
We can move up an instruction by swapping its place with another instruction that has no dependences with it, so we can try to fill some NOP slots with such instructions. We can also use R7 to eliminate WAW or WAR dependences so we can have more instructions to move up.

```
I1:   ADD   R5,  R2,  R1
I3:   LW    R2,  0(R2)     Move up to fill NOP slot
NOP
I2:   LW    R3,  4(R5)
NOP                        Had to add another NOP here,
NOP                        so there is no performance gain
I4:   OR    R3,  R5,  R3
NOP
NOP
I5:   SW    R3,  0(R5)
```

4. When processor designers consider a possible improvement to the processor datapath, the decision usually depends on the cost/performance trade-off. In the following three problems, where I-Mem, Add, Mux, ALU, Regs, D-Mem, and Control blocks have latencies of 500 ps, 100 ps, 50 ps, 180 ps, 220 ps, 350 ps, and 120 ps, respectively, and costs of 1000, 50, 20, 100, 200, 2000, and 500, respectively. (30 points)



Consider the addition of a multiplier to the ALU. This addition will add 350 ps to the latency of the ALU and will add a cost of 750 to the ALU. The result will be 40% fewer instructions executed since we will no longer need to emulate the MUL instruction.

a. Which is the clock cycle time with and without this improvement? (10 points)
Solution:

I-Mem	Add	Mux	ALU	Regs	D-Mem	Control blocks
500ps	100ps	50ps	180ps	220ps	350ps	120ps

I-Mem + Regs + Mux + ALU + D-Mem + Mux + Regs= 500 + 220 + 50 +180 + 350 + 50 + 220= 1570ps
1570ps + 350 = 1920ps

b. Which is the speedup achieved by adding this improvement? (10 points)
Solution:
Speedup = $\frac{1}{0.6} \times \frac{1570}{1920} = 1.36$

c. Compare the cost/performance ratio with and without this improvement. (10 points)
Solution:
I-Mem + Regs + Control + ALU + D-Mem + Add×2 + Mux×3 = 1000 + 200 + 500 + 100 + 2000 + 50×2 + 20×3 = 3960 (cost)
3960 + 750 = 4710 (newcost)
Relative cost = $\frac{4710}{3960} = 1.19$
Cost/performance = $\frac{1.19}{1.36} = 0.875$