Date: 2017/05/18

Student ID:

ANS Name:

The following MIPS code is executed on a processor with a 5-stage pipeline, full forwarding, and a predict-taken branch predictor.

lw r2, 0(r1)

label1: beq r2, r0, label2 # not taken once, then taken

lw r3, 0(r2)

beq r3, r0, label1 # taken

add r1, r3, r1

sw r1, 0(r2) label2

Draw the pipeline execution diagram for this code by assuming that branches execute in the EX stage.

X M W D IWY2 C3 F D & M W

beg 12

FDXMW (whong prediction)
G3 FD X MW
G3 FD & MW SWX IW Y3

beg 13

beg 12

SW Y1

F D X M W F D X M W