

Date: 2017/05/16

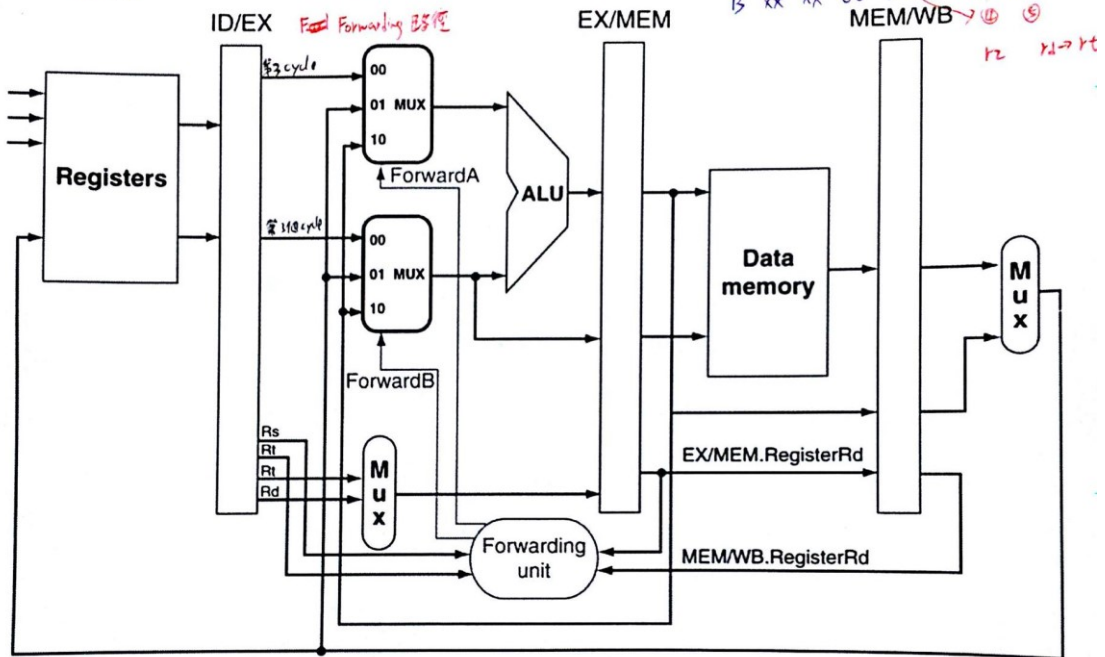
Student ID:

Name: *ANS*

Given the following sequence of instructions, if there's full forwarding in the MIPS pipelined processor, specify the signal values of "ForwardA" and "ForwardB" at each clock cycle (CC) from CC1 to CC7.

data dependency
 ① ② ③ ④ ⑤ ⑥ ⑦ clock cycle
 or r1, r2, r3 IF ID EX MEM WB
 or r2, r1, r4 F D *X* M W
 or r1, r1, r2 F ID *X* M W

id rs rt
 or r1, r2, r3
 or r2, r1, r4
 or r1, r1, r2
 Forward A
 B



① ② ③ ④ ⑤ ⑥ ⑦
 Forward A XX XX 00 10 01 XX XX
 B XX XX 00 00 10 XX XX