

Quiz #1

1. The Pentium 4 Prescott processor, released in 2004, had a clock rate of 3.6 GHz and voltage of 1.25 V. Assume that, on average, it consumed 10 W of static power and 90 W of dynamic power. The Core i5 Ivy Bridge, released in 2012, had a clock rate of 3.4 GHz and voltage of 0.9 V. Assume that, on average, it consumed 30 W of static power and 40 W of dynamic power.

- (a) For each processor find the average capacitive loads.(10%)

Solutions:

$$Power = Capacitiveload \times Voltage^2 \times Frequency$$

Pentium 4:

$$C_L = \frac{90}{1.25^2 \times 3.6 \times 10^9} = 16nF$$

Core i5:

$$C_L = \frac{40}{0.9^2 \times 3.4 \times 10^9} = 14.52nF$$

- (b) Find the percentage of the total dissipated power comprised by static power and the ratio of static power to dynamic power for each technology. (10%)

Solutions:

Pentium 4:

The percentage of the total dissipated power comprised by static power

$$\frac{10}{10+90} \times 100\% = 10\%$$

The ratio of static power to dynamic power for each technology

$$\frac{10}{90} = \frac{1}{9}$$

Core i5:

The percentage of the total dissipated power comprised by static power

$$\frac{30}{30+40} \times 100\% = 42.86\%$$

The ratio of static power to dynamic power for each technology

$$\frac{30}{40} = \frac{3}{4}$$

- (c) If the total dissipated power is to be reduced by 10%, how much should the voltage be reduced to maintain the same leakage current? Note: static power is defined as the product of voltage and current.(10%)

Solutions:

Pentium 4:

$$I = \frac{10}{1.25} = 8$$

$$\frac{P_{new}}{P_{old}} = \frac{V_{new} \times I + C_L \times (V_{new})^2 \times f}{100} = 0.9$$

$$\Rightarrow 8V_{new} + 1.6 \times 10^{-8}(V_{new})^2 \times 3.6 \times 10^9 = 90$$

$$\Rightarrow 57.6(V_{new})^2 + 8V_{new} - 90 = 0$$

$$\Rightarrow V_{new} = 1.182V$$

$$reduce \frac{V_{old} - V_{new}}{V_{old}} = \frac{1.25 - 1.182}{1.25} \times 100\% = 5.44\%$$

Core i5:

$$I = \frac{30}{0.9} = 33.33$$

$$\frac{P_{new}}{P_{old}} = \frac{V_{new} \times I + C_L \times (V_{new})^2 \times f}{70} = 0.9$$

$$\Rightarrow 33.33V_{new} + 1.452 \times 10^{-8}(V_{new})^2 \times 3.4 \times 10^9 = 63$$

$$\Rightarrow 49.368(V_{new})^2 + 33.33V_{new} - 63 = 0$$

$$\Rightarrow V_{new} = 0.841V$$

$$reduce \frac{V_{old} - V_{new}}{V_{old}} = \frac{0.9 - 0.841}{0.9} \times 100\% = 6.56\%$$

2. Section 1.10 cites as a pitfall the utilization of a subset of the performance equation as a performance metric. To illustrate this, consider the following two processors. P1 has a clock rate of 4 GHz, average CPI of 0.9, and requires the execution of 5.0E9 instructions. P2 has a clock rate of 3 GHz, an average CPI of 0.75, and requires the execution of 1.0E9 instructions.

- (a) One usual fallacy is to consider the computer with the largest clock rate as having the largest performance. Check if this is true for P1 and P2. (10%)

Solutions:

$$\text{P1 Execution time} = \frac{5 \times 10^9 \times 0.9}{4 \times 10^9} = 1.125s$$

$$\text{P2 Execution time} = \frac{1 \times 10^9 \times 0.75}{3 \times 10^9} = 0.25s$$

Although the clock rate of P1 is larger. the performance of P2 is better.

- (b) Another fallacy is to consider that the processor executing the largest number of instructions will need a larger CPU time. Considering that processor P1 is executing a sequence of 1.0E9 instructions and that the CPI of processors P1 and P2 do not change, determine the number of instructions that P2 can execute in the same time that P1 needs to execute 1.0E9 instructions. (10%)

Solutions:

$$\text{P1 Execution time} = \frac{1 \times 10^9 \times 0.9}{4 \times 10^9} = 0.225s$$

$$\text{P2 Execution time} = \frac{X \times 0.75}{3 \times 10^9} = 0.225s$$

$$\Rightarrow X = 9 \times 10^8$$

- (c) A common fallacy is to use MIPS (millions of instructions per second) to compare the performance of two different processors, and consider that the processor with the largest MIPS has the largest performance. Check if this is true for P1 and P2. (10%)

Solutions:

$$MIPS = \frac{Clockrate}{CPI \times 10^6}$$

$$\text{P1 : MIPS} = \frac{4 \times 10^9}{0.9 \times 10^6} = 4444.44$$

$$\text{P2 : MIPS} = \frac{3 \times 10^9}{0.75 \times 10^6} = 4000$$

Although the MIPS of P1 is larger. the performance of P2 is better.

3. Assume a program requires the execution of 50×10^6 FP instructions, 110×10^6 INT instructions, 80×10^6 L/S instructions, and 16×10^6 branch instructions. The CPI for each type of instruction is 2, 1, 5, and 3, respectively. Assume that the processor has a 2 GHz clock rate.

- (a) By how much must we improve the CPI of L/S instructions if we want the program to run two times faster?(15%)

Solutions:

$$\text{Clock cycle} = 50 \times 10^6 \times 2 + 110 \times 10^6 + 80 \times 10^6 \times 5 + 16 \times 10^6 \times 3 = 6.58 \times 10^8$$

$$\text{Execution time} = \frac{\text{clock}}{\text{clock}} \frac{\text{cycle}}{\text{rate}} = \frac{6.58 \times 10^8}{2 \times 10^9} = 0.329s$$

Time becomes half \rightarrow clock cycle becomes half

$$\frac{6.58 \times 10^8}{2} = 50 \times 10^6 \times 2 + 110 \times 10^6 + 80 \times 10^6 \times CPI_{L/S} + 16 \times 10^6 \times 3$$

$$\rightarrow CPI_{L/S} = \left(\frac{6.58 \times 10^8}{2} - (50 \times 10^6 \times 2 + 110 \times 10^6 + 16 \times 10^6 \times 3) \right) / 80 \times 10^6 = 0.8875$$

$$\text{reduce } \frac{5 - 0.8875}{5} \times 100\% = 82.25\%$$

- (b) By how much is the execution time of the program improved if the CPI of INT and FP instructions is reduced by 40% and the CPI of L/S and Branch is reduced by 30%?(15%)

Solutions:

$$\text{New clock cycle} = 50 \times 0.6 \times 10^6 \times 2 + 110 \times 0.6 \times 10^6 + 80 \times 0.7 \times 10^6 \times 5 + 16 \times 0.7 \times 10^6 \times 3$$

$$= 4.396 \times 10^8$$

$$\text{Execution time} = \frac{\text{clock}}{\text{clock}} \frac{\text{cycle}}{\text{rate}} = \frac{4.396 \times 10^8}{2 \times 10^9} = 0.2198s$$

$$\text{reduce } \frac{0.329 - 0.2198}{0.329} \times 100\% = 33.191\%$$

4. For the following C statement, what is the corresponding MIPS assembly code? Assume that the variables f, g, h, i, and j are assigned to registers \$s0, \$s1, \$s2, \$s3, and \$s4, respectively. Assume that the base address of the arrays A and B are in registers \$s6 and \$s7, respectively.(10%)

$B[5] = A[i - j];$

Solutions:

```
sub $t0,$s3,$s4
sll $t0,$t0,2
add $t0,$s6,$t0
lw  $t1,0($t0)
sw  $t1,20($s7)
```