2021 Spring, EE/CM Dept. Microelectronics II, Final, 06/22/2021

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注意事項：
- 不作弊，也不幫助作弊，否則成績以零分計，並須接受規定懲罰
- 可看書與任何紙本筆記；除了電子計算機之外，不可使用網路或任何電子設備作答
- 試卷總共有 2 頁，考題總共有 6 大題，總分是 120 分，考試時間有 75 分鐘
- 請將答案卷照像後上傳至 ecourse2 上才計分，請將題號標示清楚。可以用中文或英文作答，答案請寫清楚

1. (a)請敘述理想的運算放大器有哪些特點？ (10%)

   (b)請敘述實際的運算放大器在設計上有哪些項目要考量，並說明原因 (10%)

2. Assuming $\lambda = 0$ and considering only C_{in} and C_L, determine the input and output poles of the circuit shown in Fig. P2. (10%)
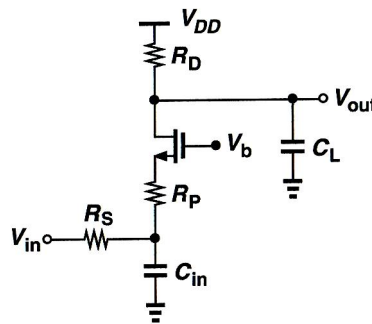

Fig. P2

3. It is required to design a cascode amplifier to provide a dc gain of 72 when driven with a low-resistance generator and utilizing NMOS transistors for which $V_A = 20$ V, $\mu_n C_{ox} = 200$ $\mu A/V^2$, $W/L = 10$, $C_{gd} = 0.1$ pF, and $C_L = 1$ pF.

   (a) Assuming that $R_L = R_{out}$, determine the over-drive voltage and the drain current at which the MOSFETs should be operated. (8%)

   (b) Find the unity-gain frequency (7%) and the 3-dB frequency. (10%)

4. Assume that A_1 has finite input resistance R_{id} and output resistance R_o. Analyze the circuit to determine its closed-loop gain $A_f = I_o/ V_s$ (10%), the input resistance of the feedback amplifier R_{if}, (5%), and the output resistance R_{of} (5%). The transistor Q_2 is operating in saturation region, and the output resistance of Q_2 is r_{o2}.
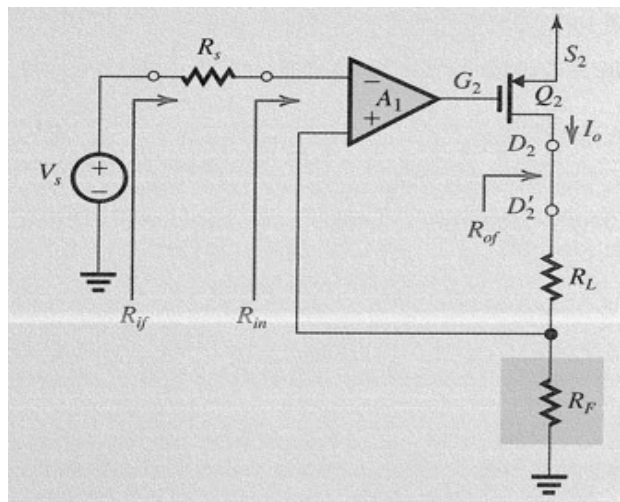

Fig. P4

5. It is required to design an amplifier to have a nominal closed-loop gain of 10 V/V using a battery-operated operational amplifier whose gain reduces to half its normal full-battery value over the life of the battery.

(a) If only 3% drop in closed-loop gain is desired, what nominal open-loop amplifier gain, A_o, must be used in the design? (5%)

(b) What value of β should be chosen? (5%)

(c) If component-value variation in the β network may produce as much as a $\pm 1\%$ variation in β, to what value must the open-loop amplifier gain, A_o, be raised to ensure the required minimum gain? (5%)

6. The circuit shown in Fig. P6 is an inexpensive audio amplifier. It consists of an operational amplifier driving a pair of complementary transistors (with $V_{BE} = 0.7$ V) operating in the class B mode. The open-loop gain of A1 is 10^4 V/V. Determine the root-mean-square power delivered to the load (10%), and the power dissipated in each transistor (10%), and calculate the power conversion efficiency (10%).
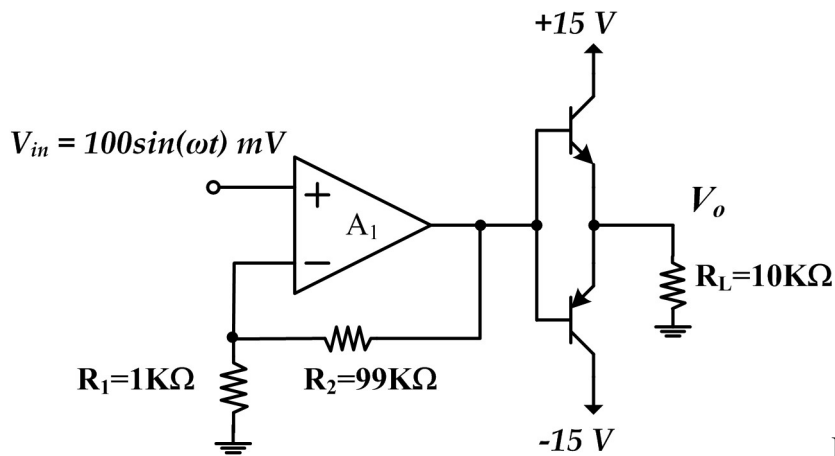

Fig. P6