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Schedule the following codes for a dual-issue MIPS processor with loop unrolling, where the loop index is a multiple of three. The processor can fetch one ALU/branch instruction and one load/store instruction at each clock cycle.

```
Loop:   lw    $t0, 0($s1)      # $t0=array element
        addu  $t0, $t0, $s2    # add scalar in $s2
        sw    $t0, 0($s1)      # store result
        addi  $s1, $s1,–4      # decrement pointer
        bne   $s1, $zero, Loop # branch $s1!=0
```

ALU/branch	Load/store	Cycle

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Loop Unrolling Example

	ALU/branch	Load/store	cycle
Loop:	addi $s1, $s1,-16	lw $t0, 0($s1)	1
	nop	lw $t1, 12($s1)	2
	addu $t0, $t0, $s2	lw $t2, 8($s1)	3
	addu $t1, $t1, $s2	lw $t3, 4($s1)	4
	addu $t2, $t2, $s2	sw $t0, 16($s1)	5
	addu $t3, $t3, $s2	sw $t1, 12($s1)	6
	nop	sw $t2, 8($s1)	7
	bne $s1, $zero, Loop	sw $t3, 4($s1)	8

- IPC = 14/8 = 1.75
  - Closer to 2, but at cost of registers and code size