National Chung Cheng University
Department of Electrical Engineering
Computer Organization, Spring 2017

June 6, 2017
Instructor: Mark P.-H. Lin
TAs: Guan-Hong Liou & Yan-Yu Su & Shuo-Hui Wang

Quiz #3

1. Assume that the breakdown of dynamic instructions into various instruction categories is as follows: (40 points)

R-Type	BEQ	JMP	LW	SW
40%	25%	5%	25%	5%

Also, assume the "Always-Taken" branch predictor accuracies is 45%

a. What is the extra CPI due to mispredicted branches with the "Always-Taken" predictor? Assume that branch outcomes are determined in the EX stage, that there are no data hazards, and that no delay slots are used. (20 points)

b. With the 2-bit predictor, what speedup would be achieved if we could convert half of the branch instructions in a way that replaces a branch instruction with an ALU instruction? Assume that correctly and incorrectly predicted instructions have the same chance of being replaced. (20 points)

Solution:

a. Each branch that is not correctly predicted by the "Always-Taken" predictor will cause 2 stall cycles, so we have: $2 \times (1\text{-}0.45) \times 0.25 = 0.275$

b. Correctly predicted branches had CPI of 1 and now they become ALU instructions whose CPI is also 1. Incorrectly predicted instructions that are converted also become ALU instructions with a CPI of 1, so we have:
Assume 2-bit predictor accuracies is 55%

CPI w/o conversion	CPI w/ conversion	Speed-up from conversion
1+2×(1-0.55)×0.25=1.225	1+2×(1-0.55)×0.25× 0.5=1.1125	1.225/1.1125=1.101

2. Caches are important to providing a high-performance memory hierarchy to processors. Bwlow is a list of 32-bit memory address references, given as word addresses. (30 points)

3,180,43,2,191,88,190,14,181,44,186,253

a. For each of these references, identify the binary address, the tag, and the index given a direct-mapped cache with 16 one-word blocks. Also list if each reference is a hit or a miss, assuming the cache is initially empty. (15 points)

b. For each of these references, identify the binary address, the tag, and the index given a direct-mapped cache with two-word blocks and a total size of 8 blocks. Also list if each reference is a hit or a miss, assuming the cache is initially empty. (15 points)

Solution:

Decimal	Binary address	Tag	Index	Hit or Miss
3	0000 0011	0000	0011	Miss
180	1011 0100	1011	0100	Miss
43	0010 1011	0010	1011	Miss
2	0000 0010	0000	0010	Miss
191	1011 1111	1011	1111	Miss
88	0101 1000	0101	1000	Miss
190	1011 1110	1011	1110	Miss
14	0000 1110	0000	1110	Miss
181	1011 0101	1011	0101	Miss
44	0010 1100	0010	1100	Miss
186	1011 1010	1011	1010	Miss
253	1111 1101	1111	1101	Miss

Decimal	Binary address	Tag	Index	Hit or Miss
3	0000 0011	0000	0001	Miss
180	1011 0100	1011	0010	Miss
43	0010 1011	0010	0101	Miss
2	0000 0010	0000	0001	Hit
191	1011 1111	1011	0111	Miss
88	0101 1000	0101	0100	Miss
190	1011 1110	1011	0111	Hit
14	0000 1110	0000	0111	Miss
181	1011 0101	1011	0010	Hit
44	0010 1100	0010	0110	Miss
186	1011 1010	1011	0101	Miss
253	1111 1101	1111	0110	Miss

3. For a direct-mapped cache design with a 32-bit address, the following bits of the address are used to access the cache. (30 points)

Tag	Index	Offset
31-12	11-5	4-0

a. What is the cache block size (in words)? (10 points)
Solution:
$2^5/4 = 32/4 = 8$ words

b. How many entries does the cache have? (10 points)
Solution:
$2^{11-5+1} = 2^7 = 128$

c. What is the ratio between total bits required for such a cache implementation over the data storage bits? (10 points)
Solution:
Number of bits in tag = 31-12+1 = 20 bits
Number of bits for each cache entry = 20 + (32×8) = 276
Number of bits for data storage = 32×8 = 256
ratio = 276/256 = 1.078

If valid bit is also considered, ratio become 277/256 = 1.082