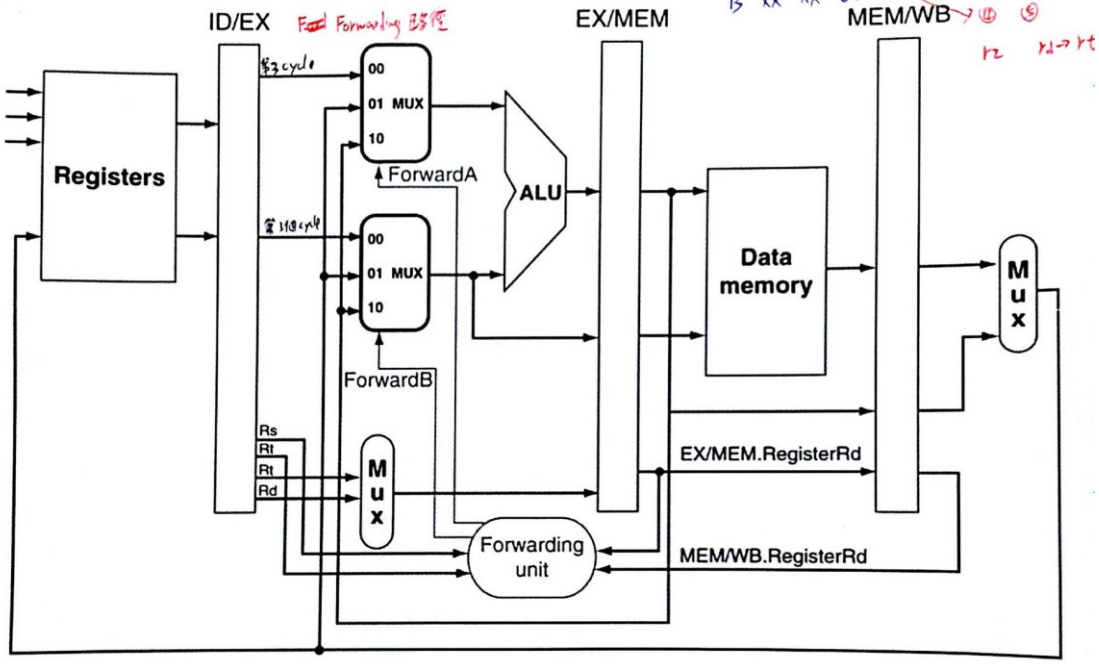
Date: 2017/05/16 Student ID: Name: ANS

Given the following sequence of instructions, if there's full forwarding in the MIPS pipelined processor, specify the signal values of "ForwardA" and "ForwardB" at each clock cycle (CC) from CC1 to CC7.

data dependency

or r1, r2, r3
or r2, r1, r4
or r1, r1, r2



	1	2	3	4	5	6	7
ForwardA	XX	XX	00	10	01	XX	XX
B	XX	XX	00	00	10	XX	XX