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The following MIPS code is executed on a processor with a 5-stage pipeline, full forwarding, and a predict-taken branch predictor.

```
        lw   r2, 0(r1)
label1: beq  r2, r0, label2   # not taken once, then taken
        lw   r3, 0(r2)
        beq  r3, r0, label1   # taken
        add  r1, r3, r1
label2  sw   r1, 0(r2)
```

Draw the pipeline execution diagram for this code by assuming that branches execute in the EX stage.