Postlab 2

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1. Why can't you use both pins PA0 and PC0 for external interrupts at the same time?

   All pins with the same number are connected to line with same number. They are multiplexed to one line. So we cannot use two pins on one line simultaneously. So we can only use only one pin at one time to handle interrupt from that line.

2. What software priority level gives the highest priority? What level gives the lowest?

   Highest priority is 0 and the lowest priority is 3. So the priority range is in between 0 to 3.

3. How many bits does the NVIC have reserved in its priority (IPR) registers for each interrupt including non-implemented bits)? Which bits in the group are implemented?

   The uppermost two bits from the 8bit regions are implemented, giving 4 possible configurable priority levels.

4. What was the latency between pushing the Discovery board button and the LED change (interrupt handler start) that you measured with the logic analyzer? Make sure to include a screenshot in the post-lab submission.

5. Why do you need to clear status flag bits in peripherals when servicing their interrupts?

   If we don't clear status flag bits, the handler is going to loop because the interrupt request never acknowledged.