PostLab3 Timer

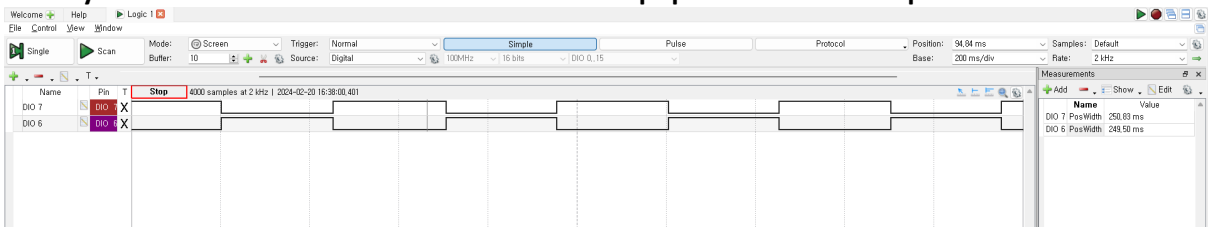
1. Using a timer clock source of 8 MHz, calculate PSC and ARR values to get a 60 Hz interrupt. This is tricky because precisely 60 Hz is impossible with our system; instead, think about the process and minimize the error. Many combinations of PSC and ARR values work—not just one!

I set ARR value to be 1000, and the corresponding PSC value turned out to be 132.3333, So when ARR is 1000, PSC will be 133, since the PSC should be an integer.

2. Look through the Table 14 "STM32F072x8/xB pin definitions" in the chip datasheet and list all pins that can have the timer 3 capture/compare channel 1 alternate function.
• If the pin is included on the LQFP64 package that we are using, list the alternate function number that you would use to select it.

Pin	LQFP64 Pin Number	Alternative Function Number
PE3	N/A	N/A
PA6	22	AF1
PC6	37	AF0
PB4	56	AF1

3. List your measured value of the timer UEV interrupt period from first experiment.



Based on this measurement, the PosWidth value of the DIO6, which is connected to PC6, pin is 250.83ms, and PosWidth of DIO7, which is connected to PC7 pin, is 249.50ms

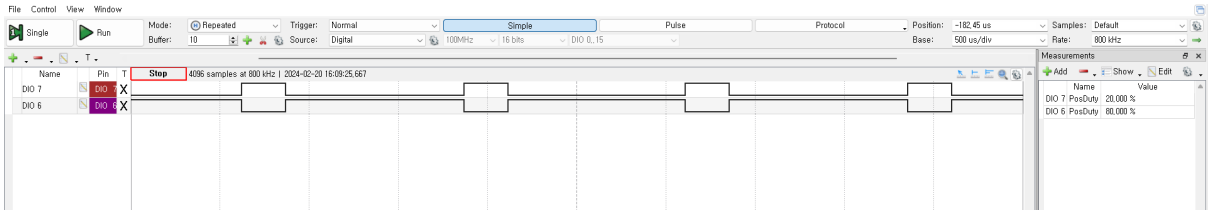
4. Describe what happened to the measured duty-cycle as the CCRx value increased in PWM mode 1.

The positive duty cycle of CCR2 value, that is connected to PWM mode 1 and PC7 pin, also increases when CCR2 value increases.

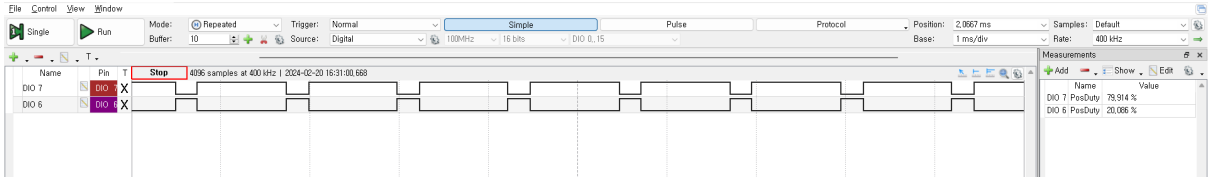
5. Describe what happened to the measured duty-cycle as the CCRx value increased in PWM mode 2.

The positive duty cycle of CCR1 value, that is connected to PWM mode 2 and PC6 pin, decreases when CCR1 value increases.

6. Include at least one logic analyzer screenshot of a PWM capture.



This measurement is when we set both CCR1 and CCR2 values to 250.



This measurement is when we set both CCR1 and CCR2 values to 1000.

7. What PWM mode is shown in figure 3.6 of the lab manual (PWM mode 1 or 2)?

Since the positive duty cycle of the PWM mode in figure 3.6 increases when CCRx value is decreasing, it should be PWM mode 2 with CCR1.