

VLSI-Infused Encryption in Master-Slave Drone Control

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Abstract:

The integrated system and host-side communication framework proposes a robust architecture for secure and efficient communication in Unmanned Aerial Vehicles (UAVs). The design provides data transfer efficiency, enhanced UAV control precision, and fortified security through encryption by utilizing fundamental components such as, UART, Encoders/Decoders, Encryption/Decryption, and Bluetooth,. This solution facilitates secure and seamless interactions between the host system and UAVs in varied scenarios.

Introduction:

In the advancing field of aerial technology, Unmanned Aerial Vehicles (UAVs) are expected to play a pivotal role in diverse applications. This research focuses on communication architecture, aiming to seamlessly integrate UAVs into various contexts, with the "master-slave" paradigm enhancing efficiency and fostering innovative solutions in areas like agriculture and disaster response.

Studies highlight the 'master – slave' approach's key role in military applications, including communication networking, reconnaissance, threat engagement, and surveillance. This model not only facilitates increased area coverage and collaborative data gathering but also extends its benefits to civilian fields. The adaptability of the

"master-slave" model offers opportunities for novel applications, showcasing the versatility of UAVs in diverse contexts such as entertainment, training, and research.

Literature review:

The research employs CoppeliaSimEDU, a 3D robot simulation software, to create a crucial 'master – slave' control-based UAV swarm model [1]. This simulation tool allows for effective pre-flight adjustments, optimizing parameters for real-world deployment. Emphasizing visualization, CoppeliaSimEDU enables a detailed examination of swarm behavior, ensuring a comprehensive understanding and enhancing real-world performance [1].

Furthermore, recent research delves into novel architectures for UAV swarms, proposing a cellular network UAV swarm architecture that leverages the strengths of both centralized and decentralized approaches while mitigating some of their weaknesses [2]. This hybrid architecture aims to enhance the overall performance and capabilities of UAV swarms, presenting a promising avenue for future exploration.

Block level design:

Figure 1 below shows the block level design of the unit. The proposed design leverages Bluetooth connectivity to establish efficient communication channels between the master and slave components. Specifically, the system focuses on expediting data collection from the Inertial Measurement Unit (IMU) on the drone, enabling real-time acquisition of crucial flight data. By consolidating both master and slave functionalities on a unified chip, the design aims to streamline communication processes, facilitating

rapid error correction in the drone's flight trajectory through the prompt issuance of corrective instructions. This integrated approach holds promise for enhancing responsiveness, reducing latency, and overall contributing to a more dynamic and error-correcting drone flight system, thereby advancing the state-of-the-art in unmanned aerial vehicle (UAV) technology.

In the intricate process of designing our system, a pivotal decision emerged during the development cycle that significantly impacted the architecture—specifically, the decision to defer the integration of the slave side of the chip. While our team successfully delivered the minimum required functionality, we encountered a series of challenges when attempting to incorporate the slave side into the device. A working top-level simulation in ModelSim showcased the synergy between the master and slave sides as seen in Figures 11 and 12; however, persistent Design Rule Check (DRC) and Layout versus Schematic (LVS) errors emerged, seemingly linked to area constraints. In response to these issues, a difficult but necessary choice was made to temporarily set aside the slave side, with the intention of revisiting its implementation given ample time for refinement. Given additional time, the intention was to address and rectify these issues, ultimately ensuring a comprehensive and secure end-product. However we did meet the minimum requirements we set out in our Project Proposal.

Simulated Results:

Add in the steps of modelsim and the behavior that was experienced there, ~24ms to deliver a packet to BLE module, ~25ms on slave to retrieve data from IMU and send packet back, and ~172ms to deliver packet back to host (50 MHz 9600 baud).

Figures 2, 3 and 4 present different views of the chip die, showcasing the meticulous layout and simulation conducted using Virtuoso from Cadence. In our design, the instance count is measured at 3,252, occupying a total area of 576,319.430 nm.

Moving to the simulation results depicted in Figure 4, a notable achievement is highlighted—the simulated arrival time outpaces the required time. Within the simulation, the overall process is executed with efficiency, completing in a swift 17.535 ns, while the stipulated required time stands at 20.002 ns. This yields a calculated slack time of 2.468 ns, underscoring a favorable margin in the temporal dynamics of the simulated process. These results affirm the robustness of our design and its adeptness in meeting or even surpassing the stipulated performance benchmarks.

Polyfill and Metafill

After the die was constructed with a clean DRC and LVS in the P&R stage, a seal ring was instantiated onto the design to protect the die from sawing and moisture. This procedure caused density issues that were fixed by performing polyfill and metafill as depicted in Figure 10. Additional density requirements were fulfilled by performing density correctness by hand, thus resulting in a clean DRC.

Conclusion

This research highlights the vital role of Unmanned Aerial Vehicles (UAVs) in diverse applications, emphasizing the effectiveness of the "master-slave" paradigm in communication architecture for enhanced efficiency. The block-level design, leveraging Bluetooth connectivity, promises real-time data acquisition and streamlined

communication. Despite challenges in integrating the slave side, a commitment to refinement is evident. Simulated results demonstrate the design's robustness in meeting or exceeding performance benchmarks, and techniques like polyfill and metafill corrects the density issues.

References:

- [1] M. Pyvoar, O. Pohudina, A. Pohudin, and O. Krtskaya, ‘Simulation of Flight Control of Two UAVs Based on the “Master-Slave” Model’, 02 2022, pp. 902–907.
- [2] M. Campion, P. Ranganathan, and S. Faruque, ‘A review and future directions of UAV swarm communication architectures’, in *2018 IEEE international conference on electro/information technology (EIT)*, 2018, pp. 0903–0908.

[Figure Section]

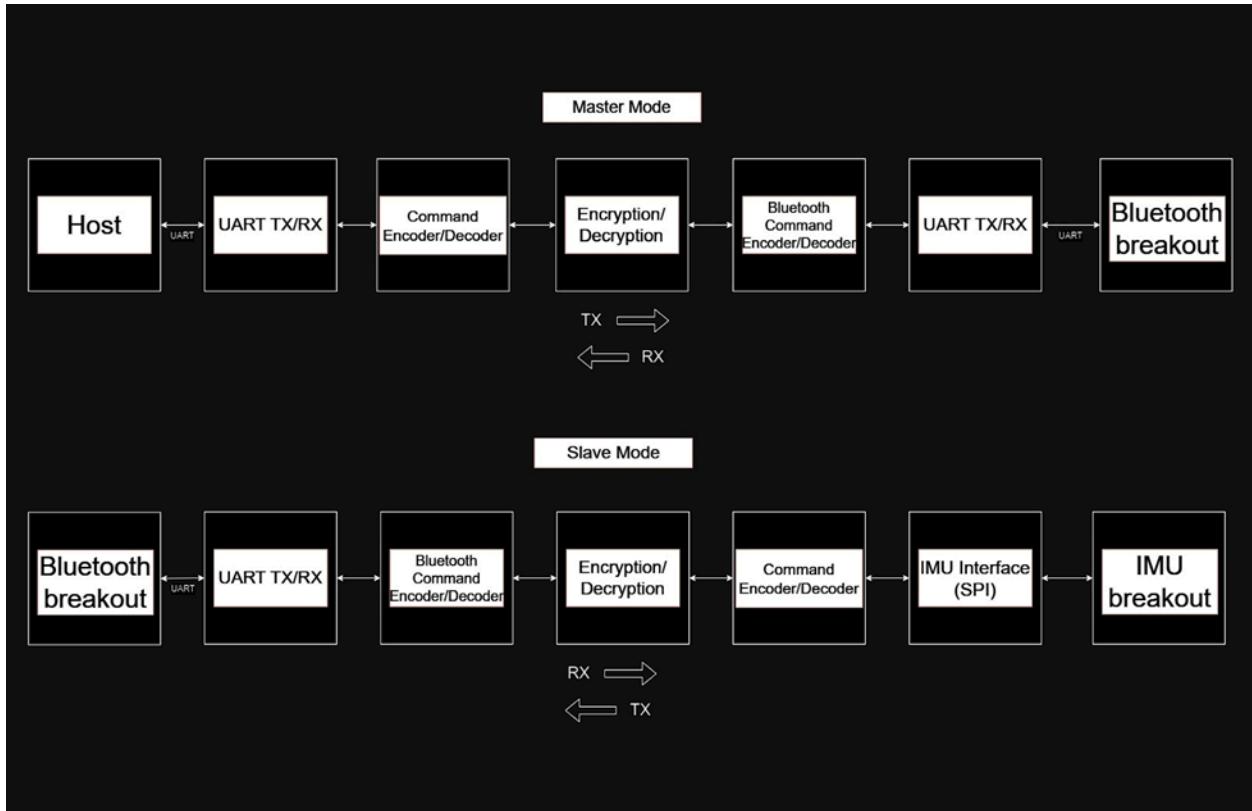


Fig. 1: Block diagram depicting the interconnected modules of the chip

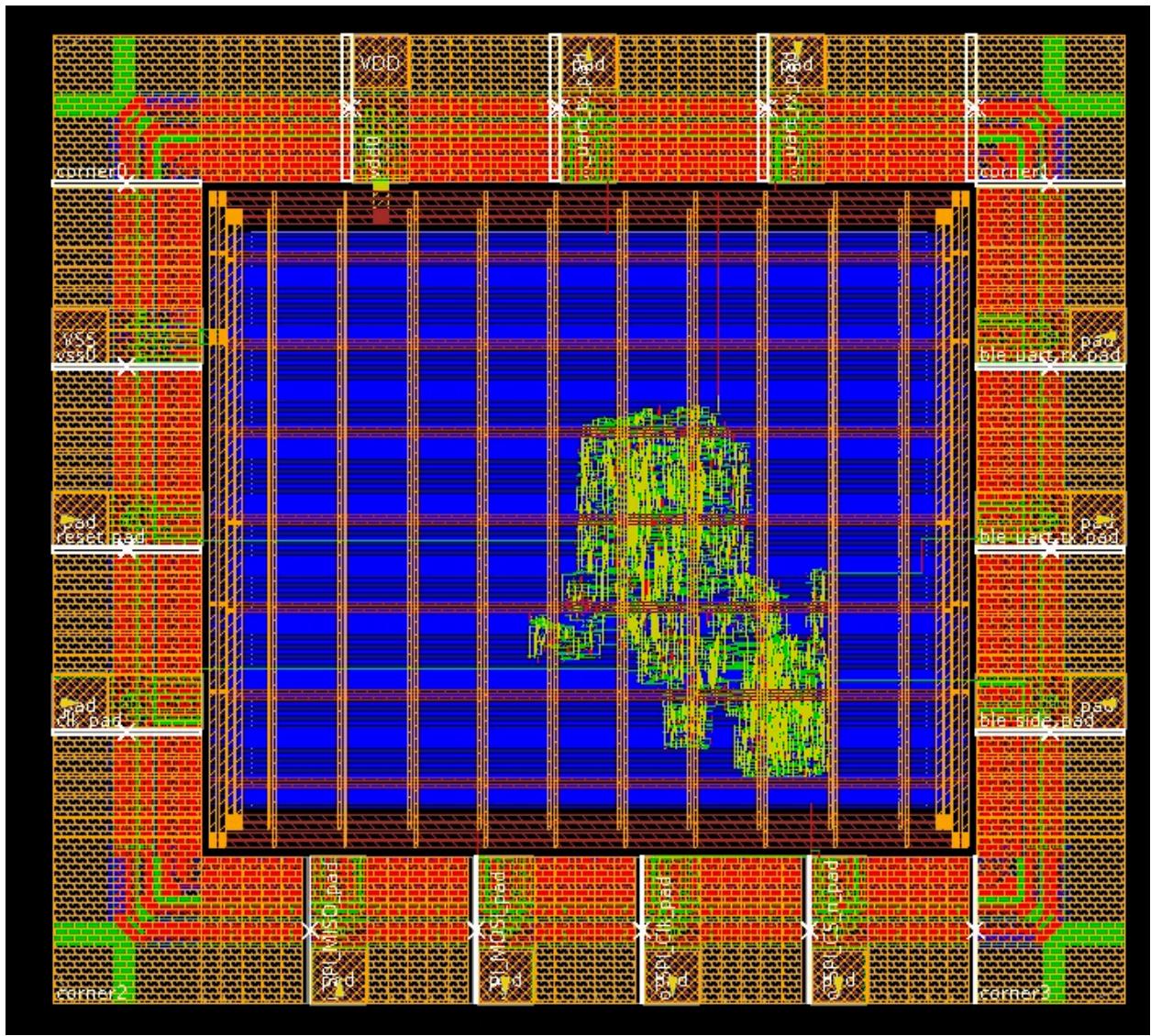


Fig 2: Photo of the die

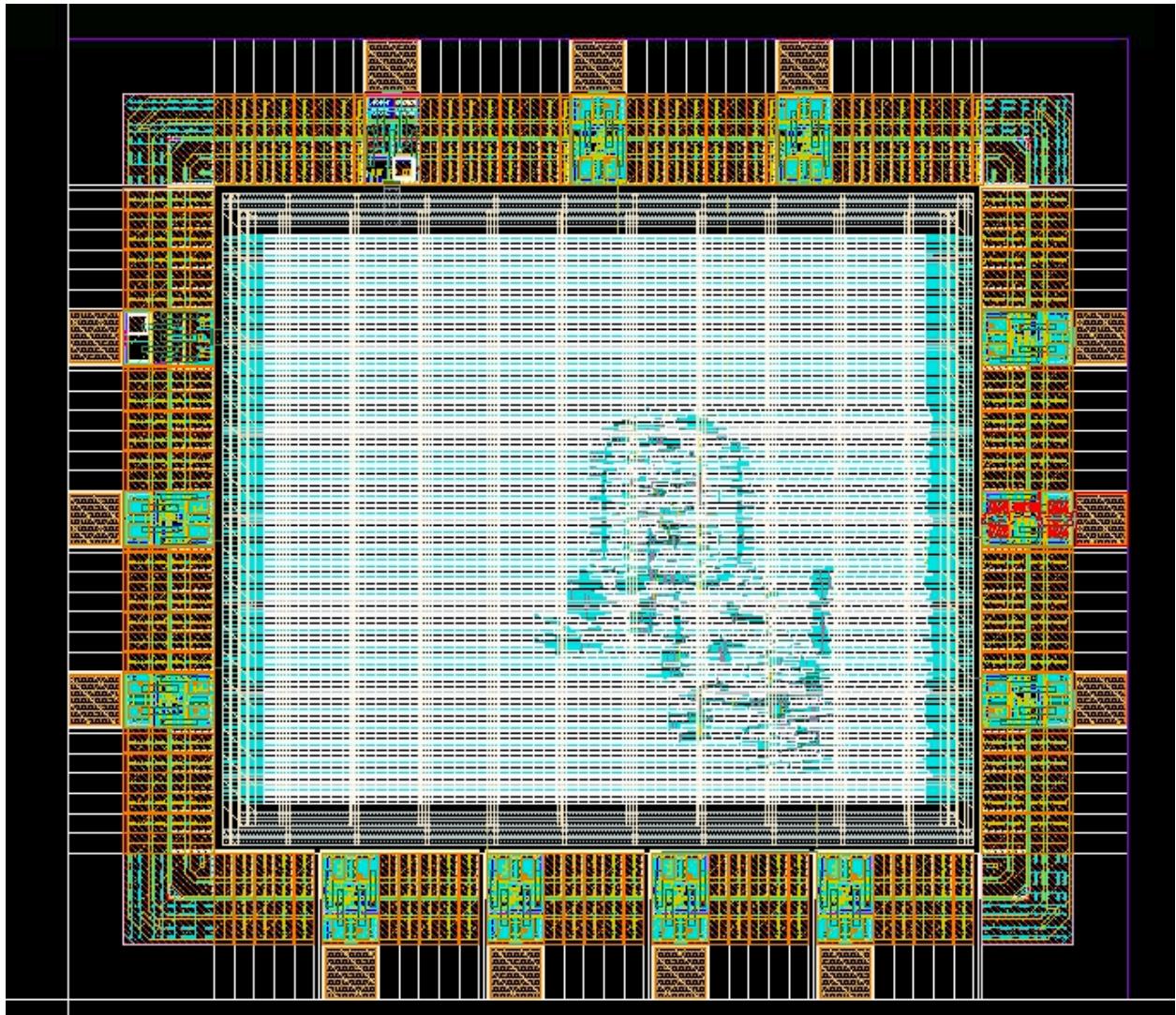


Fig 3: different die image

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Analysis View: wc
Other End Arrival Time      0.124
- Setup                      0.121
+ Phase Shift                20.000
= Required Time              20.002
- Arrival Time               17.535
= Slack Time                 2.468
Clock Rise Edge              0.000
+ Input Delay                0.000
= Beginpoint Arrival Time   0.000
+
+-----+
| Instance          | Arc           | Cell    | Delay | Arrival Time | Required Time |
+-----+
|                  | reset ^       |          |        |            |             |
| reset_pad        | pad ^ -> DataIn ^ | pad_in  | 0.225 | 0.225     | 2.468      |
| soc/g168216      | A ^ -> Z v    | INVX2   | 7.289 | 7.514     | 9.981      |
| soc/g167145      | C v -> Z ^   | NAND3X1 | 6.462 | 13.976    | 16.444      |
| soc/g167013      | B ^ -> Z v    | NOR2X1  | 0.563 | 14.539    | 17.007      |
| soc/g166609_1617 | A v -> Z ^   | NAND2X1 | 0.477 | 15.016    | 17.483      |
| soc/g166426_2398 | B ^ -> Z v    | NOR2X1  | 0.261 | 15.277    | 17.745      |
| soc/g166220_2398 | A v -> Z v    | AND2X1  | 0.524 | 15.801    | 18.269      |
| soc/g166089_1666 | A v -> Z ^   | NAND2X1 | 0.242 | 16.043    | 18.511      |
| soc/g165995_4733 | A ^ -> Z ^   | AND2X1  | 0.208 | 16.251    | 18.719      |
| soc/g165898_5122 | B ^ -> Z v    | NAND3X1 | 0.110 | 16.361    | 18.829      |
| soc/g165882_1666 | B v -> Z ^   | NOR2X1  | 0.108 | 16.469    | 18.937      |
| soc/g165855_7098 | A ^ -> Z v    | NAND3X1 | 0.132 | 16.601    | 19.069      |
| soc/g165840_5107 | B v -> Z ^   | NOR2X1  | 0.224 | 16.826    | 19.293      |
| soc/g165829_9315 | A ^ -> Z v    | NAND3X1 | 0.111 | 16.937    | 19.404      |
| soc/g165816_1705 | B v -> Z ^   | NOR2X1  | 0.249 | 17.186    | 19.654      |
| soc/g165796_9945 | A ^ -> Z v    | NAND3X1 | 0.118 | 17.304    | 19.772      |
| soc/g165794       | A v -> Z ^   | INVX2   | 0.103 | 17.407    | 19.874      |
| soc/g165785_5115 | A ^ -> Z v    | NAND3X1 | 0.128 | 17.534    | 20.002      |
| soc/ble_uart_tx_data_reg[1] | D v | DFFQX1 | 0.000 | 17.535 | 20.002 |
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Hinst Name	Module Name	Inst Count	Total Area
soc_top		3252	576345.773
soc	top_level	3235	85972.813

Fig. 4: Timing report summary

Category	Our Performance	Our Requirements
Power		
Area	576,345.773 nm	< 1.5mm by 1.5mm
Timing	17.535 ns	20.002 ns
Slack	2.468 ns	Positive Slack

Fig 5. Performance Summary

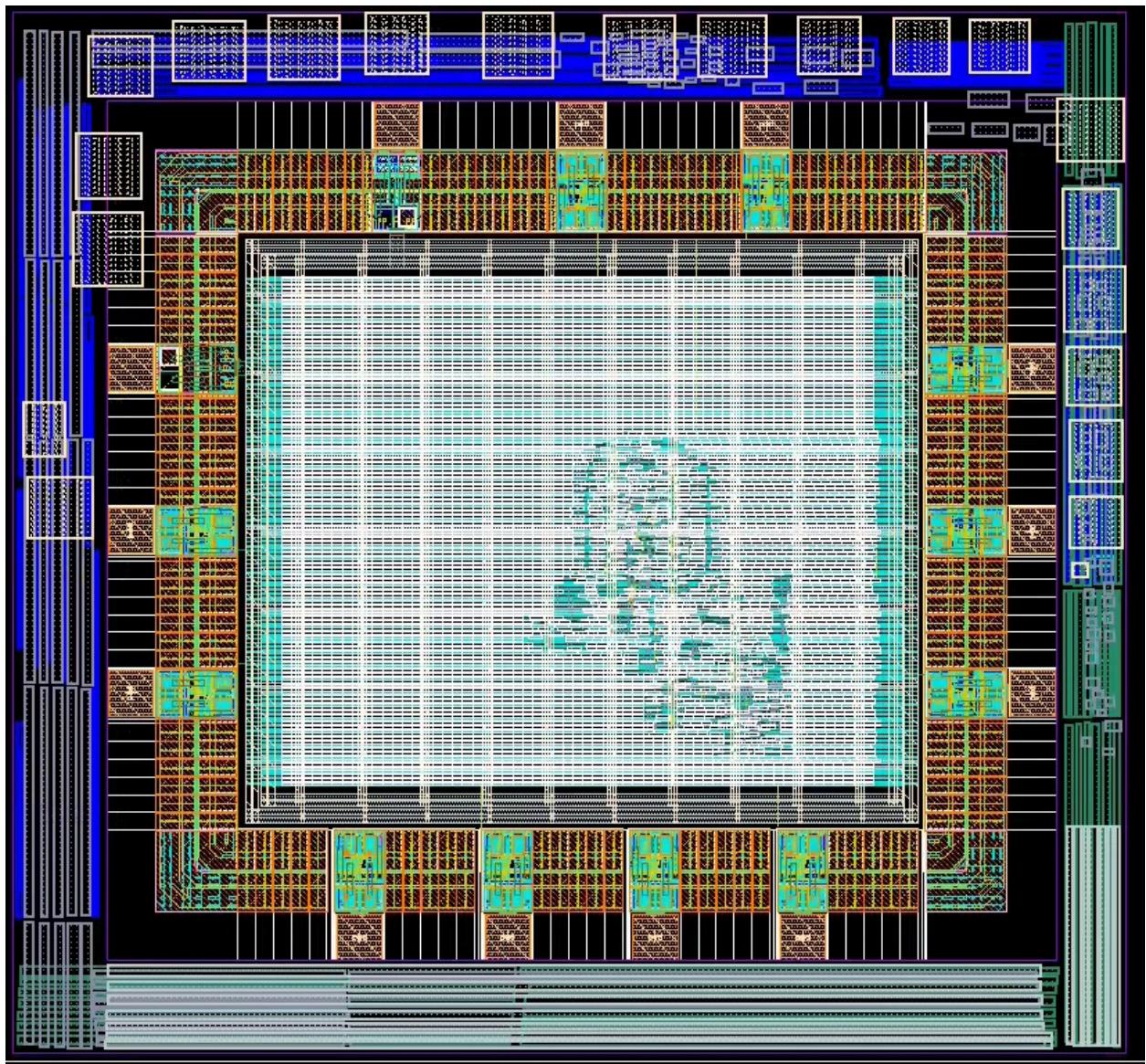


Figure 6. Die with the seal ring

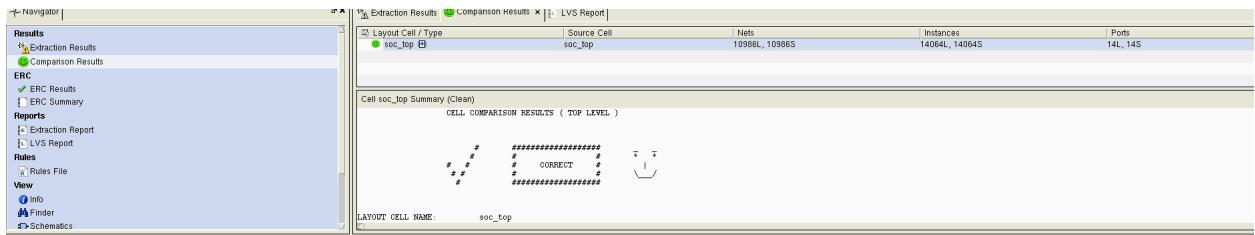


Figure 7 LVS

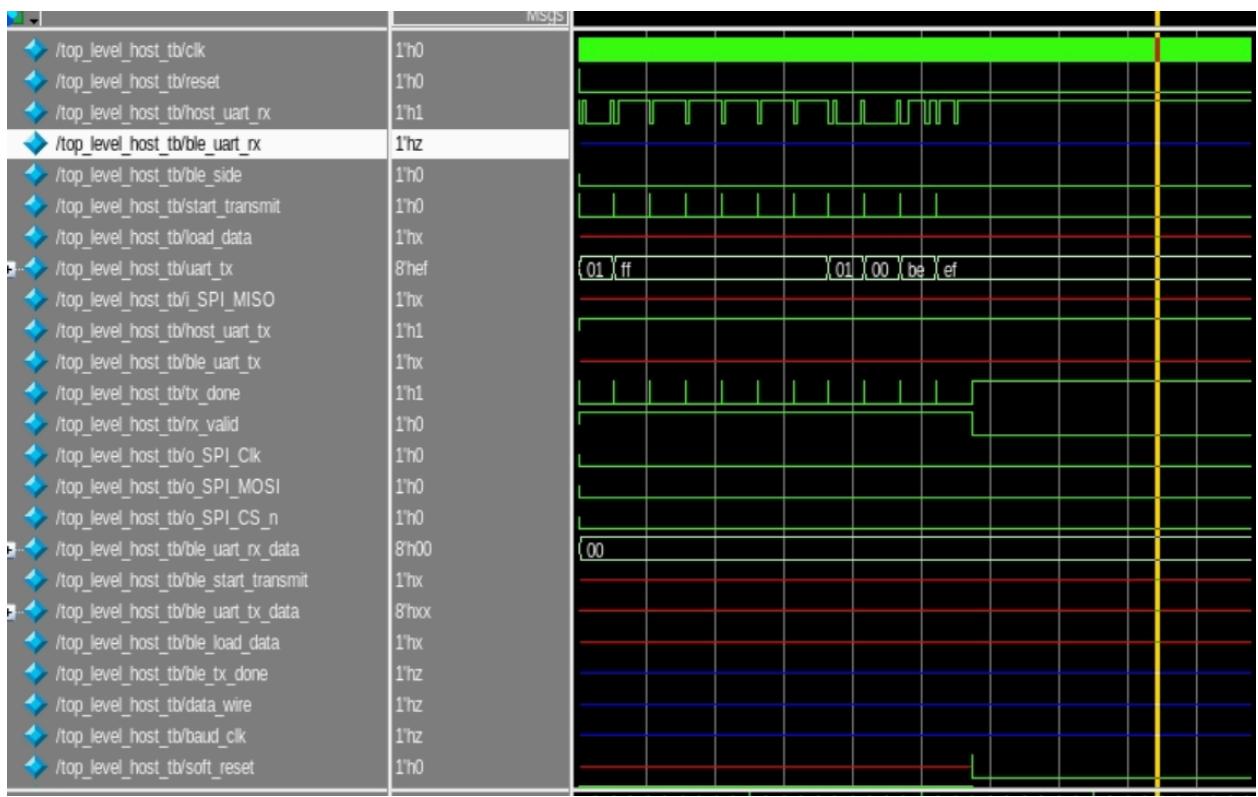


Figure 8 Post synthesis

Instance: /top_level					
Power Unit: W					
PDB Frames: /stim#0/frame#0					
Category	Leakage	Internal	Switching	Total	Row%
memory	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
register	1.68254e-07	8.75936e-04	1.31409e-04	1.00751e-03	56.34%
latch	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
logic	7.03804e-08	1.66566e-04	2.78694e-04	4.45330e-04	24.90%
bbox	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
clock	0.00000e+00	0.00000e+00	3.35437e-04	3.35437e-04	18.76%
pad	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
pm	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
Subtotal	2.38634e-07	1.04250e-03	7.45540e-04	1.78828e-03	100.00%
Percentage	0.01%	58.30%	41.69%	100.00%	100.00%

Figure 9: Genus Power analysis

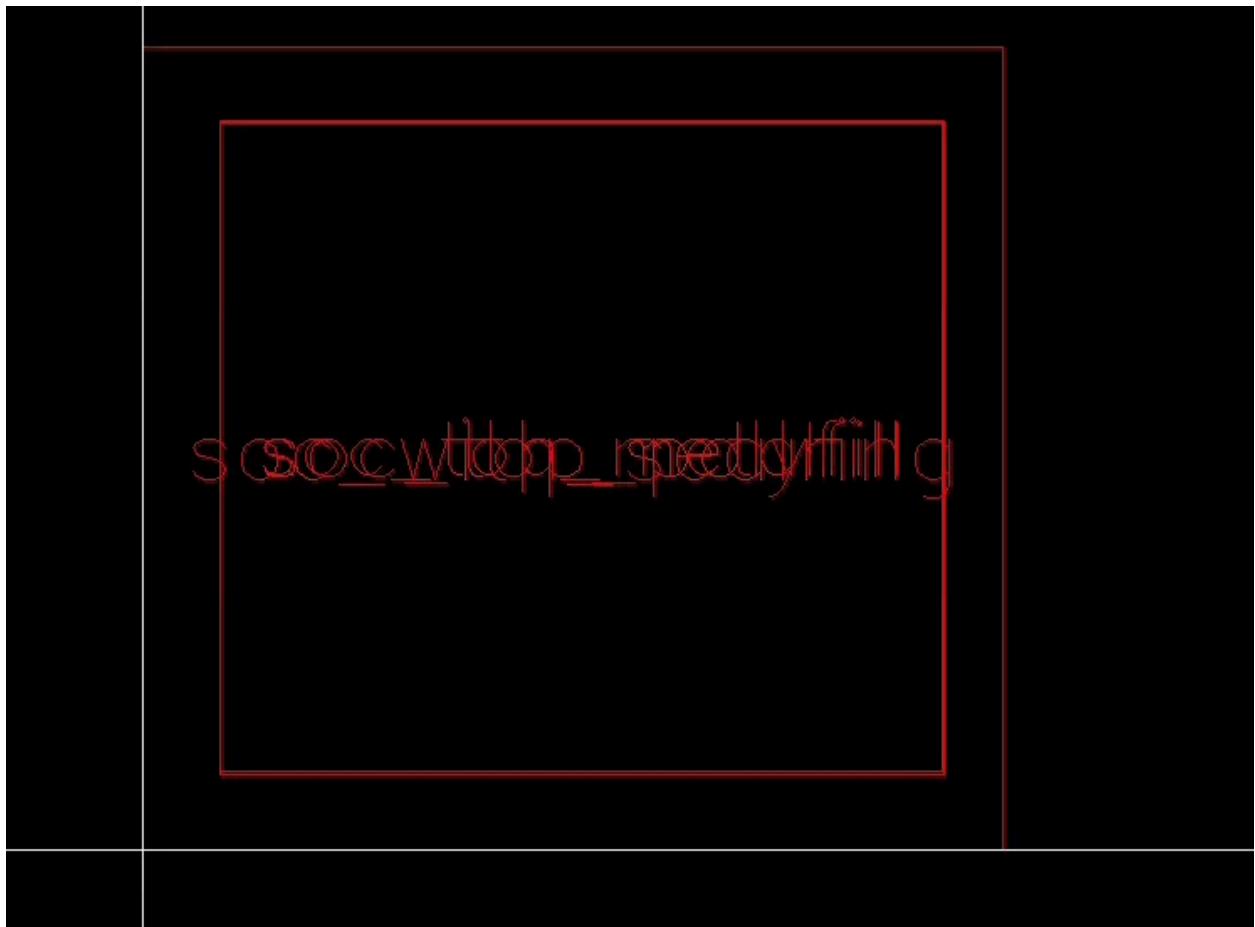


Figure 10: Polyfill and Metafill

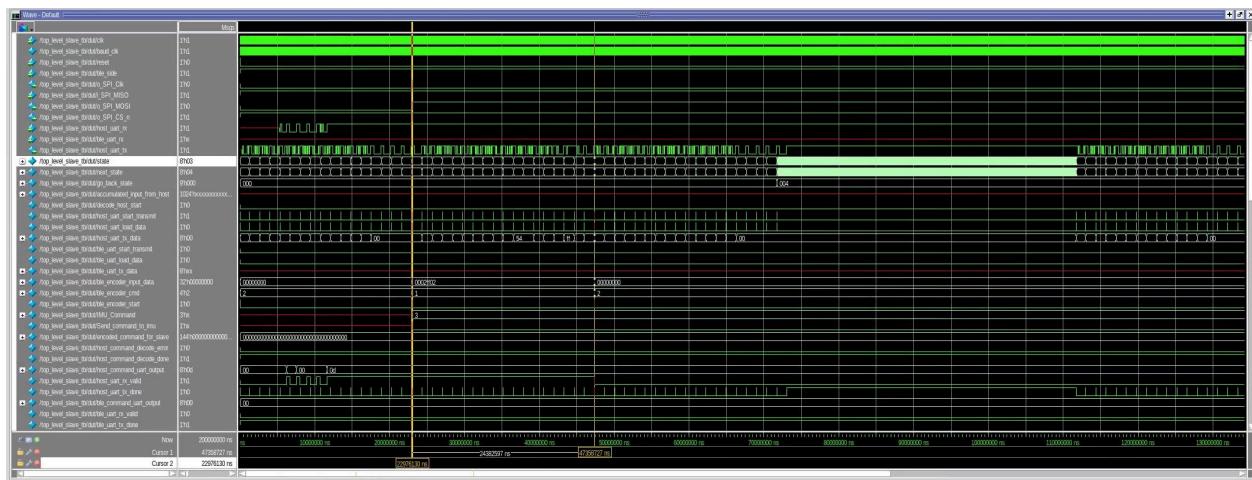


Figure 11: Host Side Pre Synthesis

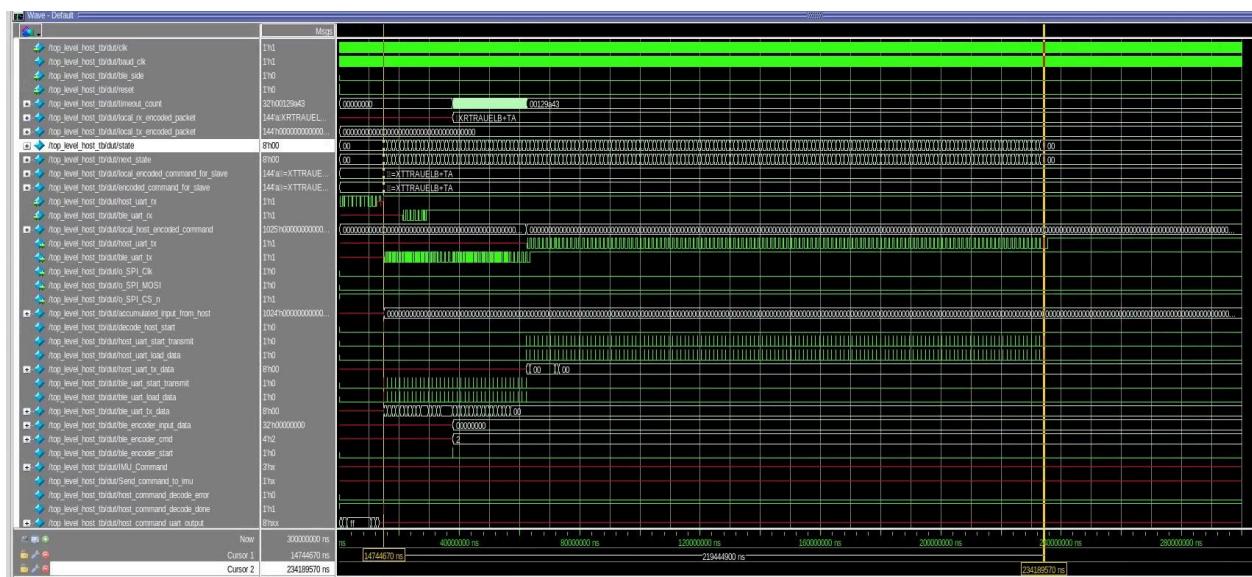


Figure 12: Slave Side Pre Synthesis