Table 2.1: Some of the pin functions on the PIC32

ANX (x = 0 to 15) AVDD, AVSS AVDD	Pin Label	Function
CXIN+, CXIN+, CXOUT (x = 1, 2) CXRX, CXTX (x = 1, 2) CXRX, CXTX (x = 1, 2) CXRX, CXTX (x = 1, 2) CXNX (x = 0 to 18)  CVREF-, CVREF+, CVREFOUT D+, D- ENVREG  CVREF-, CVREF+, CVREFOUT D+, D- ENVREG  CX (x = 1 to 5) INTX (x = 0 to 4) MCIR  OCX (x = 1 to 5) INTX (x = 0 to 4) MCIR  OCX (x = 1 to 5) OCFA, OCFB  OSC1, OSC2 PMAX (x = 0 to 15) PMDX (x = 0 to 15) PMDX (x = 0 to 15) PMENB, PMRD, PMWR Rxy (x = 8 to G, y = 0 to 15) RTCC  SCLx, SDAX (x = 1, 3, 4, 5) CSCLx, SDAX (x = 1, 3, 4, 5) SCKx, SDIX, SDOX (x = 2 to 4) T1CK UXCTS, UXRTS, UXRX, UXTX (x = 1 to 6) VDD VDD VDD VDD VDD VDD VDD VDD VDD VD	ANx (x = 0  to  15)	Analog-to-digital (ADC) inputs
CXN, CXTX (x = 1, 2) CLSI, CLKO CNx (x = 0 to 18) CNx (x = 0 to 18) CVREF-, CVREF+, CVREFOUT D+, D- ENVREG CNX (x = 1 to 5) INTX (x = 0 to 4) MCLR OCx (x = 1 to 5) INTX (x = 0 to 4) MCLR OCx (x = 1 to 5) OCFA, OCFB OCFA, OCFB OCFA, OCFB OCFA, OCFB SMAX (x = 0 to 15) PMDx (x = 0 to 15) PMENB, PMRD, PMWR RSy (x = B to G, y = 0 to 15) RTCC SCLx, SDAx (x = 1, 3, 4, 5) SCKx, SDIx, SDOx (x = 2 to 4) TTCK UXCT5, UXRT5, UXRX, UXTX (x = 1 to 6) VDDCAP VDDCAP VDDCAP VDDCAP VDDCAP VDDCAP VDDCAP VDDCAP VDDCAP VDBCS VBUS VUSB  CAN receive and transmit pins Clock input and output (for particular clock modes) Clock input and output (preference voltage low and high inputs, output USB communication; voltage changes on these pins can generate interrupts Comparator reference voltage low and high inputs, output USB communication lines interrupts Comparator reference voltage low and high inputs, output USB communication lines interrupts Ochange regulator that provides 1.8 V to internal core (on the NU32 beard it is set to VDD to enable the regulator) Input capture pins for measuring frequencies and pulse widths Voltage regulator that provides 1.8 V to internal 1.8 V regulator when ENVREG enabled External 1.8 V supply when ENVREG disabled Can be used as negative and positive limit for ADC Ground for logic and I/O Monitors USB bus power Power for USB transeciver	AVDD, AVSS	Positive supply and ground reference for ADC
CLKI, CLKO CNx (x = 0 to 18)  CNx (x = 0 to 18)  CNx (x = 0 to 18)  CNREF-, CVREF+, CVREFOUT D+, D- ENVREG  ENVREG  INTx (x = 0 to 4)  MCLR  OCX (x = 1 to 5)  INTX (x = 0 to 4)  MCLR  OCX (x = 1 to 5)  OCFA, OCFB  SOCI, OSC2  PMAx (x = 0 to 15)  PMDX (x = 0 to 15)  PMDX (x = 0 to 15)  PMDX (x = 0 to 15)  PMENB, PMRD, PMWR  Ray (x = 0 to 15)  RTCC  SCLx, SDJAx (x = 1, 3, 4, 5)  SCKx, SDJAx (x = 1, 3, 4, 5)  SCKx, SDJAx (x = 1 to 6)  T1CK  UXCTS, UXRTS, UXRX, UXTX (x = 1 to 6)  VDD  VDD  VDD  VDDCAP  VDDCAP  VDDCAP  VDDCAP  VDDCORE  VBUS  VOREF-, CVREF+, CVREFOUT D+, D-  Change notification; voltage changes on these pins can generate interrupts  Comparator reference voltage low and high inputs, output USB communication lines Enable for on-chip voltage regulator that provides 1.8 V to internal core (on the NU32 board it is set to VDD to enable the regulator)  Input capture pins for measuring frequencies and pulse widths Voltage changes on these pins can generate interrupts  Master clear reser pin, resets to VDD to enable the regulator)  Input capture pins for measuring frequencies and pulse widths Voltage changes on these pins can generate interrupts  Master clear reser pin, resets to VDD to enable the regulator)  Input capture pins for measuring frequencies and pulse widths Voltage changes on these pins can generate interrupts  Master clear reser pin, resets to VDD to enable the regulator)  Input capture pins for measuring frequencies and pulse widths Voltage changes on these pins can generate pulse set to VDD to enable the regulator)  Input capture pins for measuring frequencies and pulse widths Voltage changes on these pins can generate pulse set to VDD to enable the regulator  Input pin capture pins for measuring frequencies and pulse widths Voltage changes on these pins can generate pulse to send, receive input, and transmit output for UART modules  Positive voltage supply for peripheral digital logic and I/O pins (3.3 V on NU32)  Capacitor filter for internal 1.8 V regulator when ENVREG enabled  External 1.8	CxIN-, $CxIN+$ , $CxOUT(x = 1, 2)$	Comparator negative and positive input and output
CNx (x = 0 to 18)  CVREF-, CVREF+, CVREFOUT D+, D- ENVREG  ENVREG  (on the NU32 board it is set to VDD to enable the regulator) Input capture pins for measuring frequencies and pulse widths Voltage changes on these pins can generate interrupts  OCx (x = 1 to 5) INTx (x = 0 to 4) MCLR OCx (x = 1 to 5) OCFA, OCFB  OSC1, OSC2 PMAx (x = 0 to 15) PMDx (x = 0 to 7) PMENB, PMRD, PMWR Rsy (x = 8 to G, y = 0 to 15) RTCC SCLx, SDAx (x = 1, 3, 4, 5) CSCx, SDAx (x = 1, 3, 4, 5) CSCx, SDAx (x = 1 to 6) VDD  VDD  VDD  VDD  VDD  Change notification; voltage changes on these pins can generate interrupts Comparator reference voltage low and high inputs, output USB communication lines Enable for on-chip voltage regulator that provides 1.8 V to internal core (on the NU32 board it is set to VDD to enable the regulator) Input capture pins for measuring frequencies and pulse widths Voltage changes on these pins can generate Inster port loss and pulse in the regulator on the regulato	CxRX, $CxTx$ ( $x = 1, 2$ )	
interrupts  CVREF+, CVREF+, CVREFOUT D+, D- ENVREG  ENVREG  (on the NU32 board it is set to VDD to enable the regulator) Ilnput capture pins for measuring frequencies and pulse widths Voltage changes on these pins can generate interrupts Matter clear reset pin, resets PIC when low OCFA, OCFB  OCFA, OCFB  OCFA, OCFB  OSC1, OSC2 PMAx (x = 0 to 15) PMDX (x = 0 to 7) PMENB, PMRD, PMWR Rxy (x = 0 to 0.7) PMENB, PMRD, PMWR Rxy (x = 0 to 0.7) PMENB, PMRD, PMWR Rxy (x = 0 to 0.7) PSCLx, SDAx (x = 1, 3, 4, 5)  SCKx, SDIx, SDOx (x = 2 to 4) T1CK UxCTS, UxRTS, UxRX, UxTX (x = 1 to 6) VDD  VDDCAP VDDCAP VDDCAP VDDCAP VDDCAP VDDCAP VDDCAP VDDCAP VDDCAP VDBC VSS  VBUS  Input capture pins for measuring frequencies and pulse widths voloties end to reservate interrupts Matter clear reset pin, resets PIC when low Output compare pins, usually used to generate pulse trains (pulse-width modulation) or individual pulses Fault protection for output compare pins; if a fault occurs, they can be used to make OC outputs be high impedance (neither high nor low) Crystal or resonator connections for different clock modes Parallel master port address Parallel master port address Parallel master port address Parallel master port address Service and parallel master port Digital I/O pins Real-time clock alarm output 1°C serial clock, serial data in nout for SPI synchronous serial communication modules SSIA (x = 2 to 4) T1CK UxCTS, UxRTS, UxRX, UxTX (x = 1 to 6) VDD  NUST clear to send, request to send, receive input, and transmit output for UART modules Positive voltage supply for peripheral digital logic and I/O pins (3.3 V on NU32) Capacitor filter for internal 1.8 V regulator when ENVREG enabled External 1.8 V supply when ENVREG disabled Can be used as negative and positive limit for ADC Ground for logic and I/O Monitors USB bus power Power for USB transceiver	CLKI, CLKO	Clock input and output (for particular clock modes)
CVREF-, CVREF+, CVREFOUT D+, D- ENVREG ENABLES ENABLES ENABLES ENABLES ENABLES ENVREG  (on the NU32 board it is set to VDD to enable the regulator) Input capture pins for measuring frequencies and pulse widths Voltage changes on these pins can generate interrupts Master clear reset pin, resets PIC when low OCx (x = 1 to 5) OCFA, OCFB OCFA, OCFB  OCFA, OCFB  OSC1, OSC2 PMAx (x = 0 to 15) PMDx (x = 0 to 7) PMENB, PMRD, PMWR ENABLES ENABLE POR A CALL ENABLE COLOR ENABLE C	CNx (x = 0  to  18)	
D+, D- ENVREG  Enable for on-chip voltage regulator that provides 1.8 V to internal core (on the NU32 board it is set to VDD to enable the regulator)  IDCX (x = 1 to 5)  INTX (x = 0 to 4)  MCLR  OCX (x = 1 to 5)  OCFA, OCFB  OCFA, OCFB  OSC1, OSC2  PMAx (x = 0 to 15)  PMENB, PMRD, PMWR  RWy (x = 0 to 7)  PMENB, PMRD, PMWR  RWy (x = 0 to 0, y = 0 to 15)  RTCC  SCLx, SDAx (x = 1, 3, 4, 5)  SCKx, SDIx, SDOx (x = 2 to 4)  T1CK  T1CK	CVREF-, CVREF+, CVREFOUT	Comparator reference voltage low and high inputs, output
(on the NU32 board it is set to VDD to enable the regulator) Input capture pins for measuring frequencies and pulse widths  Voltage changes on these pins can generate interrupts  Master clear reset pin, resets PIC when low  OCx (x = 1 to 5)  OCFA, OCFB  OCFA, OCFB  OSC1, OSC2  PMAx (x = 0 to 15)  PMDx (x = 0 to 7)  PMENB, PMRD, PMWR  Rxy (x = 8 to G, y = 0 to 15)  PTCC  SCLx, SDAx (x = 1, 3, 4, 5)  SCKx, SDIx, SDOx (x = 2 to 4)  T1CK  T1CK  UXCTS, UXRTS, UXRX, UXTX (x = 1 to 6)  VDD  VDDCAP  VDDCAP  VDDCAP  VDDCAP  VDDCORE  VDDCAP  VDDCORE  VDBUS  VDBUS  VOltage changes on these pins can generate interrupts  Master robrate pins for measuring frequencies and pulse widths  Voltage changes on these pins can generate interrupts  Master clear reset pin, resets PIC when low  Output compare pins, usually used to generate pulse trains (pulse-width modulation) or individual pulses  Fault protection for output compare pins; if a fault occurs, they can be used to make OC outputs be high impedance (neither high nor low)  Crystal or resonator connections for different clock modes  Parallel master port address  Parallel master port address  Parallel master port data  Enable and read/write strobes for parallel master port  Digital I/O pins  Real-time clock alarm output  I²C serial clock and data input/output for I²C synchronous serial communication modules  Serial clock, serial data in, out for SPI synchronous serial communication modules  Slave select (active low) for SPI communication  Input pin for counter/timer 1 when counting external pulses  UART clear to send, request to send, receive input, and transmit output for UART modules  Positive voltage supply for peripheral digital logic and I/O pins (3.3 V on NU32)  Capacitor filter for internal 1.8 V regulator when ENVREG enabled External 1.8 V supply when ENVREG disabled  Can be used as negative and positive limit for ADC  Ground for logic and I/O  Monitors USB bus power  Power for USB transceiver	D+, D-	USB communication lines
Voltage changes on these pins can generate interrupts  Master clear reset pin, resets PIC when low  Output compare pins, usually used to generate pulse trains (pulse-width modulation) or individual pulses  Fault protection for output compare pins; if a fault occurs, they can be used to make OC outputs be high impedance (neither high nor low)  OSC1, OSC2  PMAx (x = 0 to 15)  PMDx (x = 0 to 7)  PMENB, PMRD, PMWR  Rxy (x = B to G, y = 0 to 15)  RTCC  SCLx, SDAx (x = 1, 3, 4, 5)  CCKx, SDIx, SDOx (x = 2 to 4)  T1CK  UXCTS, UXRTS, UXRX, UXTX  (x = 1 to 6)  VDD  VDD  VDD  VOD  Voltage changes on these pins can generate interrupts  Master clear reset pin, resets PIC when low  Output compare pins, usually used to generate pulse trains (pulse-width modulation) or individual pulses  Fault protection for output compare pins; if a fault occurs, they can be used to make OC outputs be high impedance (neither high nor low)  Crystal or resonator connections for different clock modes  Parallel master port address  Parallel master port address  Parallel master port data  Enable and read/write strobes for parallel master port  Digital I/O pins  Real-time clock alarm output  I²C serial clock and data input/output for I²C synchronous serial communication modules  Serial clock, serial data in, out for SPI synchronous serial communication modules  Slave select (active low) for SPI communication  Input pin for counter/timer 1 when counting external pulses  UART clear to send, request to send, receive input, and transmit output for UART modules  Positive voltage supply for peripheral digital logic and I/O pins (3.3 V on NU32)  VDDCAP  VDDCAP  VDDCAP  VDDCAP  VDDCAP  Capacitor filter for internal 1.8 V regulator when ENVREG enabled  External 1.8 V supply when ENVREG disabled  Can be used as negative and positive limit for ADC  Ground for logic and I/O  Monitors USB bus power  Power for USB transceiver	ENVREG	
MCLR OCx (x = 1 to 5) OCFA, OCFB OCFA, OCFB OCSC1, OSC2 PMAx (x = 0 to 15) PMDx (x = 0 to 7) PMENB, PMRD, PMWR Rxy (x = B to G, y = 0 to 15) RTCC SCLx, SDAx (x = 1, 3, 4, 5) SCKx, SDIx, SDOx (x = 2 to 4) T1CK UXCTS, UXRTS, UXRX, UXTX (x = 1 to 6) VDD  VDDCAP VDDCAP VDDCAP VDDCAP VDDCAP VDDCAP VDDCAP VDBCS  VCFA, OCFB  Master clear reset pin, resets PIC when low Output compare pins, usually used to generate pulse trains (pulse-width modulation) or individual pulses Fault protection for output compare pins; if a fault occurs, they can be used to make OC outputs be high impedance (neither high nor low) Crystal or resonator connections for different clock modes Parallel master port address Parallel master port data Enable and read/write strobes for parallel master port Digital I/O pins Real-time clock alarm output I²C serial clock alarm output I²C serial clock and data input/output for I²C synchronous serial communication modules Serial clock, serial data in, out for SPI synchronous serial communication modules UXCTS, UXRTS, UXRX, UXTX (x = 1 to 6) VDD VDCAP VDCAP VDCAP VDCAP VDCAP VDCAP VDCAP VDCAP VDCORE VREF+, VREF+ VSS VBUS VUSB  Master clear reset pin, resets PIC when low Output compare pins, usually used to generate pulse trains (pulse-width modulation) for output compare pins, is daily used to generate pulses fault procurs of fifter for internal 1.8V regulator when ENVREG enabled External 1.8V supply when ENVREG disabled Can be used as negative and positive limit for ADC Ground for logic and I/O Monitors USB bus power Power for USB transceiver	ICx (x = 1  to  5)	Input capture pins for measuring frequencies and pulse widths
OCx (x = 1 to 5)  Output compare pins, usually used to generate pulse trains (pulse-width modulation) or individual pulses  Fault protection for output compare pins; if a fault occurs, they can be used to make OC outputs be high impedance (neither high nor low)  OSC1, OSC2  PMAx (x = 0 to 15)  PMDx (x = 0 to 7)  PMENB, PMRD, PMWR  Ray (x = B to G, y = 0 to 15)  RTCC  SCLx, SDAx (x = 1, 3, 4, 5)  SCKx, SDIx, SDOx (x = 2 to 4)  T1CK  UXCTS, UXRTS, UXRX, UXTX (x = 1 to 6)  VDD  VDDCAP  VDDCAP  VDDCAP  VDDCAP  VDDCAP  VDDCAP  VDDCAP  VBUS  VBUS  VBUS  Output compare pins, usually used to generate pulse trains (pulse-width modulation) or individual pulses  Fault protection for output compare pins; if a fault occurs, they can be used to make OC outputs compare pins; if a fault occurs, they can be used to make OC output compare pins; if a fault occurs, they can be used to make OC output compare pins; if a fault occurs, they can be used to make OC output compare pins; if a fault occurs, they can be used to make OC output output compare pins; if a fault occurs, they can be used to make OC output output for ilow) for ilow)  Crystal or resonator connections for different clock modes  Parallel master port data  Enable and read/write strobes for parallel master port  Digital I/O pins  Real-time clock alarm output  I <sup>2</sup> C serial clock and data input/output for I <sup>2</sup> C synchronous serial communication modules  Serial clock, serial data in, out for SPI synchronous serial communication modules  Slave select (active low) for SPI communication  Input pin for counter/timer 1 when counting external pulses  UART clear to send, receive input, and transmit output for UART modules  Positive voltage supply for peripheral digital logic and I/O pins (3.3 V on NU32)  Capacitor filter for internal 1.8 V regulator when ENVREG enabled  External 1.8V supply when ENVREG disabled  Can be used as negative and positive limit for ADC  Ground for logic and I/O  Monitors USB bus power  Power for USB transceiver	INTx(x=0  to  4)	Voltage changes on these pins can generate interrupts
modulation) or individual pulses  OCFA, OCFB  Fault protection for output compare pins; if a fault occurs, they can be used to make OC outputs be high impedance (neither high nor low)  Crystal or resonator connections for different clock modes  PMAX (x = 0 to 15)  PMENB, PMRD, PMWR  Ry (x = B to G, y = 0 to 15)  RTCC  SCLx, SDAx (x = 1, 3, 4, 5)  SCKx, SDIx, SDOx (x = 2 to 4)  T1CK  UXCTS, UXRTS, UXRX, UXTX (x = 1 to 6)  VDD  VDDCAP  VDDCAP  VDDCAP  VDDCAP  VDDCORE  VREF-, VREF+  VSS  VBUS  VBUS  Monitors USB tushed  Tind in put compare pins; if a fault occurs, they can be used to make OC outputs be high impedance (neither high nor low)  Crystal or resonator connections for different clock modes  Parallel master port data  Enable and read/write strobes for parallel master port  Digital I/O pins  Real-time clock alarm output  I²C serial clock and data input/output for I²C synchronous serial communication modules  Serial clock, serial data in, out for SPI synchronous serial communication modules  Slave select (active low) for SPI communication  Input pin for counter/timer 1 when counting external pulses  UART clear to send, request to send, receive input, and transmit output for UART modules  Positive voltage supply for peripheral digital logic and I/O pins (3.3 V on NU32)  Capacitor filter for internal 1.8 V regulator when ENVREG enabled  External 1.8 V supply when ENVREG disabled  Can be used as negative and positive limit for ADC  Ground for logic and I/O  Monitors USB bus power  Power for USB transceiver	MCLR	Master clear reset pin, resets PIC when low
OCFA, OCFB  Salt protection for output compare pins; if a fault occurs, they can be used to make OC outputs be high impedance (neither high nor low)  Crystal or resonator connections for different clock modes  PMAX (x = 0 to 15)  PMDX (x = 0 to 7)  PMENB, PMRD, PMWR  Ray (x = B to G, y = 0 to 15)  RTCC  SCLx, SDAx (x = 1, 3, 4, 5)  CSCLx, SDIx, SDOx (x = 2 to 4)  T1CK  UXCTS, UXRTS, UXRX, UXTX  (x = 1 to 6)  VDD  VDDCAP  VDDCAP  VDDCAP  VDDCAP  VDDCORE  VREF-, VREF+  VREF- VUSB  Fault protection for output compare pins; if a fault occurs, they can be used to make OC outputs be high impedance (neither high nor low)  Crystal or resonator connections for different clock modes  Parallel master port address  Parallel master port data  Parallel master port data  Enable and read/write strobes for parallel master port  Digital I/O pins  Real-time clock alarm output  I <sup>2</sup> C serial clock and data input/output for I <sup>2</sup> C synchronous serial communication modules  Serial clock, serial data in, out for SPI synchronous serial communication  Input pin for counter/timer 1 when counting external pulses  UART clear to send, request to send, receive input, and transmit output for UART modules  Positive voltage supply for peripheral digital logic and I/O pins (3.3 V on NU32)  Capacitor filter for internal 1.8 V regulator when ENVREG enabled  External 1.8 V supply when ENVREG disabled  Can be used as negative and positive limit for ADC  Ground for logic and I/O  Monitors USB bus power  Power for USB transceiver	OCx (x = 1  to  5)	
OSC1, OSC2 PMAx (x = 0 to 15) PMDx (x = 0 to 7) PMENB, PMRD, PMWR Ray (x = B to G, y = 0 to 15) RTCC SCLx, SDAx (x = 1, 3, 4, 5) SCKx, SDIx, SDOx (x = 2 to 4) T1CK UXCTS, UXRTS, UXRX, UXTX (x = 1 to 6) VDD VDCAP VDDCAP VDCAP	OCFA, OCFB	Fault protection for output compare pins; if a fault occurs, they can be
PMAx (x = 0 to 15) PMDx (x = 0 to 7) PMENB, PMRD, PMWR Rxy (x = B to G, y = 0 to 15) RTCC SCLx, SDAx (x = 1, 3, 4, 5) SCKx, SDIx, SDOx (x = 2 to 4) T1CK UXCTS, UXRTS, UXRX, UXTX (x = 1 to 6) VDD VDCAP VDDCAP VDDCAP VDDCAP VDDCAP VDDCAP VDDCAP VDDCAP VDBCAP VBUS VUSB Parallel master port address Parallel master port data Enable and read/write strobes for parallel master port Digital I/O pins Real-time clock alarm output I²C serial clock and data input/output for I²C synchronous serial communication modules Serial clock, serial data in, out for SPI synchronous serial communication Input pin for counter/timer 1 when counting external pulses UART clear to send, request to send, receive input, and transmit output for UART modules Positive voltage supply for peripheral digital logic and I/O pins (3.3 V on NU32) Capacitor filter for internal 1.8 V regulator when ENVREG enabled External 1.8 V supply when ENVREG disabled Can be used as negative and positive limit for ADC VSS Ground for logic and I/O Monitors USB bus power Power for USB transceiver	OSC1, OSC2	
PMDx (x = 0 to 7) PMENB, PMRD, PMWR Rxy (x = B to G, y = 0 to 15) RTCC SCLx, SDAx (x = 1, 3, 4, 5)  SCKx, SDIx, SDOx (x = 2 to 4)  T1CK UXCTS, UXRTS, UXRX, UXTX (x = 1 to 6) VDD VDDCAP VDDCAP VDDCAP VDDCAP VDDCAP VDDCAP VDDCAP VDDCAP VBUS VUSB Parallel master port data Enable and read/write strobes for parallel master port Digital I/O pins Real-time clock alarm output I²C serial clock and data input/output for I²C synchronous serial communication modules Serial clock, serial data in, out for SPI synchronous serial communication modules Slave select (active low) for SPI communication Input pin for counter/timer 1 when counting external pulses UART clear to send, request to send, receive input, and transmit output for UART modules Positive voltage supply for peripheral digital logic and I/O pins (3.3 V on NU32) Capacitor filter for internal 1.8V regulator when ENVREG enabled External 1.8V supply when ENVREG disabled Can be used as negative and positive limit for ADC VSS Ground for logic and I/O Monitors USB bus power Power for USB transceiver		•
PMENB, PMRD, PMWR Rxy (x = B to G, y = 0 to 15) RTCC  SCLx, SDAx (x = 1, 3, 4, 5)  SCKx, SDIx, SDOx (x = 2 to 4)  T1CK  UXCTS, UXRTS, UXRX, UXTX (x = 1 to 6)  VDD  VDD  VDDCAP  VDCAP  Capacitor filter for internal 1.8 V regulator when ENVREG enabled  External 1.8 V supply when ENVREG disabled  Can be used as negative and positive limit for ADC  Ground for logic and I/O  Monitors USB bus power  Power for USB transceiver		
Rxy (x = B to G, y = 0 to 15) RTCC  SCLx, SDAx (x = 1, 3, 4, 5)  SCKx, SDAx (x = 1, 3, 4, 5)  SCKx, SDIx, SDOx (x = 2 to 4)  SCKx, SDIx, SDOx (x = 2 to 4)  T1CK  UxCTS, UxRTS, UxRX, UxTX (x = 1 to 6)  VDD  VDDCAP  VDDCAP  VDDCAP  VDDCAP  VDDCORE  VREF-, VREF+  VSS  VBUS  VUSB  Digital I/O pins  Real-time clock alarm output  I²C serial clock and data input/output for I²C synchronous serial communication modules  Serial clock, serial data in, out for SPI synchronous serial communication modules  Slave select (active low) for SPI communication  Input pin for counter/timer 1 when counting external pulses  UART clear to send, request to send, receive input, and transmit output for UART modules  Positive voltage supply for peripheral digital logic and I/O pins (3.3 V on NU32)  Capacitor filter for internal 1.8 V regulator when ENVREG enabled  External 1.8 V supply when ENVREG disabled  Can be used as negative and positive limit for ADC  Ground for logic and I/O  Monitors USB bus power  Power for USB transceiver	, ,	
RTCC  SCLx, SDAx (x = 1, 3, 4, 5)  SCKx, SDIx, SDOx (x = 2 to 4)  SCKx, SDIx, SDOx (x = 2 to 4)  T1CK  UxCTS, UxRTS, UxRX, UxTX (x = 1 to 6)  VDD  VDDCAP  VDDCAP  VDDCAP  VDDCORE  VREF-, VREF+  VSS  VBUS  VUSB  Real-time clock alarm output  I²C serial clock, and data input/output for I²C synchronous serial communication modules  Serial clock, serial data in, out for SPI synchronous serial communication modules  Slave select (active low) for SPI communication  Input pin for counter/timer 1 when counting external pulses  UART clear to send, receive input, and transmit output for UART modules  Positive voltage supply for peripheral digital logic and I/O pins (3.3 V on NU32)  Capacitor filter for internal 1.8 V regulator when ENVREG enabled  External 1.8 V supply when ENVREG disabled  Can be used as negative and positive limit for ADC  Ground for logic and I/O  Monitors USB bus power  Power for USB transceiver		Digital I/O pins
SCLx, SDAx (x = 1, 3, 4, 5)  SCKx, SDIx, SDOx (x = 2 to 4)  SCKx, SDIx, SDOx (x = 2 to 4)  T1CK  UxCTS, UxRTS, UxRX, UxTX (x = 1 to 6)  VDD  VDDCAP  VDDCAP  VDDCAP  VDDCORE  VREF-, VREF+  VSS  VBUS  VUSB  I²C serial clock and data input/output for I²C synchronous serial communication modules  Serial clock, serial data in, out for SPI synchronous serial communication modules  Slave select (active low) for SPI communication  Input pin for counter/timer 1 when counting external pulses  UART clear to send, request to send, receive input, and transmit output for UART modules  Positive voltage supply for peripheral digital logic and I/O pins (3.3 V on NU32)  Capacitor filter for internal 1.8 V regulator when ENVREG enabled  External 1.8 V supply when ENVREG disabled  Can be used as negative and positive limit for ADC  VSS  VBUS  VMONITORS  Monitors USB bus power  Power for USB transceiver	RTCC	Real-time clock alarm output
modules  SSx (x = 2 to 4)  T1CK  UxCTS, UxRTS, UxRX, UxTX  (x = 1 to 6)  VDD  VDD  VDD  VDD  VDD  VDD  VDD  V	SCLx, SDAx (x = 1, 3, 4, 5)	I <sup>2</sup> C serial clock and data input/output for I <sup>2</sup> C synchronous serial
T1CK UxCTS, UxRTS, UxRX, UxTX (x = 1 to 6)  VDD  VDD  VDD  VDD  VDD  VDD  VDD  V	SCKx, SDIx, SDOx $(x = 2 \text{ to } 4)$	•
T1CK UxCTS, UxRTS, UxRX, UxTX (x = 1 to 6)  VDD  VDD  VDD  VDD  VDD  VDD  VDD  V	$\overline{SSx}$ (x = 2 to 4)	
UxCTS, UxRTS, UxRX, UxTX (x = 1 to 6)  VDD  VDD  VDD  VDD  VDD  VDD  VDD  V		
(x = 1 to 6)for UART modulesVDDPositive voltage supply for peripheral digital logic and I/O pins (3.3 V on NU32)VDDCAPCapacitor filter for internal 1.8 V regulator when ENVREG enabledVDDCOREExternal 1.8 V supply when ENVREG disabledVREF-, VREF+Can be used as negative and positive limit for ADCVSSGround for logic and I/OVBUSMonitors USB bus powerVUSBPower for USB transceiver		
VDDCAP VDDCORE VREF-, VREF+ VSS VBUS VUSB  NU32) Capacitor filter for internal 1.8 V regulator when ENVREG enabled External 1.8 V supply when ENVREG disabled Can be used as negative and positive limit for ADC Ground for logic and I/O Monitors USB bus power Power for USB transceiver		for UART modules
VDDCAP  VDDCORE  VREF-, VREF+  VSS  VBUS  VUSB  Capacitor filter for internal 1.8 V regulator when ENVREG enabled  External 1.8 V supply when ENVREG disabled  Can be used as negative and positive limit for ADC  Ground for logic and I/O  Monitors USB bus power  Power for USB transceiver	VDD	
VDDCORE VREF-, VREF+ Can be used as negative and positive limit for ADC VSS Ground for logic and I/O VBUS Monitors USB bus power VUSB Power for USB transceiver	VDDCAP	
VREF-, VREF+  VSS  Can be used as negative and positive limit for ADC  Ground for logic and I/O  VBUS  Monitors USB bus power  VUSB  Power for USB transceiver		
VSS Ground for logic and I/O VBUS Monitors USB bus power VUSB Power for USB transceiver		
VBUS Monitors USB bus power VUSB Power for USB transceiver	I	6
VUSB Power for USB transceiver		
		USB on-the-go (OTG) detect

See Section 1 of the Data Sheet for more information.