ME333 Introduction to Mechatronics
2022 Quiz 4: Chapter 3

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1. The PIC32 has four types of memory: data RAM, program flash, SFRs, and boot flash. Which is cacheable, which is not? Why?

   Cacheable: boot flash, program flash, data RAM. These are all instructions we can store in the cache for fast access.

   Not cacheable: SFRs. We can't reuse a cached sensor reading, for example, meaning it doesn't make sense to cache data from SFRs - and the PIC32 doesn't allow you to.

2. For the following SFR, how many implemented bitfields are there? After reset, which bitfields are initially set?

6080	TRISC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISC15	TRISC14	TRISC13	TRISC12	—	—	—	—	—	—	—	TRISC4	TRISC3	TRISC2	TRISC1	—	F00F

   For the TRISC SFR, 8 bitfields are implemented: TRISCx (where x = 1,2,3,4,12,13,14,15).

   The reset value is 0xF00F = 0b1111 0000 0000 1111. This means TRISC 15,14,13,12, 3,2,1 are initially set upon reset (but not TRISC4, for some reason).

3. What is the function of the `processor.o` file?

   processor.o is stored in a folder labeled with our specific version of the PIC32. In our case, we get processor.o from PIC32MX795F512H (or whatever our model # is).

   The function of processor.o is to get addresses for things in memory on our specific model of the PIC32. In particular, the memory addresses of SFRs will be different for diff. models of the PIC32. So processor.o tells us what memory location each SFR is stored at.

4. The prefetch module has a 128 bit wide path to Flash memory, but the rest of the bus matrix inside the PIC32 is only 32 bits wide. Why?

   The prefetch module has a 128-bit wide path to Flash memory so that it can retrieve the same amount of instructions as a 32-bit wide path at 4x the speed. So given that the prefetch cache can load instructions from Flash memory at 30MHz and can load 4 instructions at a time, we can stay ahead of the rate of execution of instructions at 80MHz if our code is perfectly linear.