CS 472 Final

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Introduction to IA-32, ARM, and PowerPC

IA-32 refers to the third generation of the x86 architecture. The IA-32 architecture was first implemented in the Intel 80386 microprocessors, and was a 32-bit extension of x86. This architecture remained the basis of many microprocessors, and later generations have become faster. Intel supplies the most IA-32 processors, although other companies such as AMD supply IA-32 processors.

ARM Holdings was founded by Acorn Computers, Apple Computers, and VLSI technology. Acorn Computers Ltd. first built the BCC microcomputer, which was based on the 8-bit 6502 and used in British high schools. The second generation ARM was a 32-bit microprocessor built with 20,000 transistors. ARM licenses its core processors, rather than actually building chips. ARM's success can be demonstrated by the processors found in various netbooks, tablets, and cell phones.

PowerPC was born out of an alliance between Apple, IBM, and Motorola. IBM had a RISC architecture called POWER that needed to be used for a wider range of computing. Motorola wanted to compete in the RISC workstation market, and needed a better RISC microprocessor. Apple's motivation was that it needed a CPU for its computers that was backwards compatible with the 68K and performed well. In 12 months, IBM and Motorola were able to launch the PowerPC 601, which had a full-featured RISC design. The 603 was later launched, and used in low end Apple products since it was not good at emulating legacy 68k code. Next was the 604, which was Apples high end desktop processor.

Instruction set design of IA-32, ARM, and PowerPC

IA-32 is a Complex Instruction Set Computer (CISC) architecture. Instructions in IA-32 have two operands, with the first being the source and the second being a source or destination. There is a wide variety of addressing modes in IA-32, with a combination of the base register, displacement, and scaled index register. The displacement can be 8, 16, or 32 bit values, and the scale for the index register can be 1, 2, 4, or 8. IA-32 is similar to many CISC architectures, in that it uses status flags to keep track of conditions like carries and overflow. There are many instructions, including floating point arithmetic instructions and instructions for operations on data elements packed into words. Instructions vary in size from 1 to 15 bytes, and the encodings can become convoluted.

ARM utilizes Reduced Instruction Set Computer (RISC) architecture. ARM includes many different addressing modes. The most straightforward is literal addressing. Register indirect addressing, where the location of an operand is held in a register, can be used with an optional offset. Autoindexing, both pre-indexed and post-indexed, are used to read sequential data in structures. PC relative addressing can be used, which uses the program counter as a pointer register to access the operand. Load and store encoding instructions are another mode, and can be conditionally executed. Current ARM cores support 32-bit address space and 32-bit arithmetic. Newer ARM architecture will begin to support 64-bit.

As the PowerPC acronym (Performance Optimization With Enhanced RISC - Performance Computing) suggests, PowerPC is a RISC architecture. A single addressing mode exists for load and store instructions, which is register plus displacement. In order to access any 32-bit address, two instructions must be used. The high and low 16 bits are separately placed into a register that will hold the desired 32-bit address. In PowerPC architecture, memory operands can be bytes, half words, words, or double words. The PowerPC7400 had three fully pipelined cycles. The pipeline in the 7450 allowed integer and memory instructions to flow around instructions stuck in the execute stage to improve the amount of instructions being executed. Static and dynamic branch prediction was used to reduce branch-related pipeline bubbles.

Datapath design

Modern IA-32 processors have eight general purpose registers. Many register names had historical meaning that has lost purpose, although the stack pointer and base pointer are reserved. Superscalar architecture first appeared in the P5 Pentium for the IA-32 architecture. This allowed multiple instructions to be executed at the same time during a single clock cycle. In 1989, a five-stage pipeline was added to the i486. Each stage of the pipeline could have an instruction, which double performance compared to a 386 processor. The first stage

fetches an instruction, the second decodes, the third translates memory addresses and displacements, the fourth executes instructions, and the fifth writes results back. The Pentium later added a second superscalar pipeline, that ran instructions such as integer operations in parallel. The Pentium Pro processor in 1995 had an out-of-order execution processing core. The out-of-order pipeline allows the decoder to detect when a large branch is about to happen, and can then begin loading appropriate instructions. The pipeline in this Pentium Pro had 12 stages, and could execute several instructions at once. In the next iteration of the IA-32 architecture, more registers were added, and changes were made to the pipeline to boost performance. Many CPUs with IA-32 architecture have writable microcode. The advantage of writable microcode is that bugs can be fixed by changing the software rather than the hardware.

ARM has 13 general-purpose registers, a Stack Pointer, a Link Register, Program Counter, and a Program Status Registers. All of these registers are 32-bit. The Link Register gets the return address from the PC when a Branch and Link is executed. The pipeline for ARMv7TDMI has 3 stages, for fetch, decode, and execute. Multiple cycles could be executed for load/stores. Later versions added 5 state pipeline, then 8 states, then 10 stages. The ARM1176JZF-S also added hardware branch prediction. Arm does not have microcode, which contributes to the simplicity of the architecture.

PowerPC has 32 general purpose registers, which are either 32 or 64 bits. Some of these registers are specifically regarded as the return value and the arguments for a function. The PowerPC 601 has a typical four stage pipeline, with fetch, decode, execute, and writeback stages. One thing to note is that multicycle integer instructions are not fully pipelined, although the most common integer instructions are single-cycle instructions. The 603e has a four stage pipeline, but is only capable of decoding and dispatching two instructions per cycle. A dedicated load-store unit allows the integer unit to be freed from handling memory traffic, so it can focus on integer arithmetic and improve performance that way. The 603e pipeline is different from the 601 because the 603e has an additional execute stage and one less decode stage. A deeper six stage pipeline is found in the 604, which adds dispatch and complete stages. These new stages allow for out-of-order execution. Also, each pipeline stage is simpler which results in a shorter CPU clock cycle time. PowerPC supports microcode, to execute microprograms in place of PowerPC instructions that did not fit into the pipeline design very well.

Memory subsystem

IA-32 architecture in general has caches, with specific implementations having different cache designs. P6 implementations have a small L1 code and data caches, and unified L2 cache. Some architectures implemented a large trace cache instead of the L1 instructions cache. Implementations like the Pentium D and Core have the P6 style small L1 cache. IA-32 divides memory into segments, which raises hardware exceptions on invalid access. Virtual addresses are used, which translate into physical addresses in the RAM or disk. Page tables are used for this translation. Modern implementations of IA-32 architecture have a 3 memory model. This includes the use of paging, segmentation, and direct mapping (no virtual memory). The paging has a 3 level hierarchy, which includes the page directory, the page table, and pages which are continous blocks of memory.

ARM architecture have caches, with separate instruction and data caches to further improve performance. Many different cache sizes are supported, and can be selected independently. ARM implements a memory management unit defined by the virtual memory system. Page table entries have permission for read/writes based on factors including privilege and cacheability information.

The PowerPC 601 has a single 32KB unified L1 cache, which is much larger than the comparable pentium architecture. The lower powered 603e has a smaller 16k split L1 cache. At the initial release, the 604 had a 32K split L1 cache, then a 64K split L1 cache. The larger cache in the 604 helped the longer pipeline to function properly.

Interesting features of the system

One feature of IA-32 architecture that is notable is the backwards compatibility. CISC instructions lead to a lower code size, and enables the instruction cache to be used efficiently.

ARM processors have an advantage when it comes to power consumption, which makes them more useful in devices that run on batteries. Predication for instructions was added before Intel added it. Another intesting point is the Thumb instruction set that has 16 bit instructions that are compact versions of some 32 bit instructions.

PowerPC supports both big endian and little endian modes. The traditional paged memory managment system was replaced by a new memory managment architecture named Book-E. Some instructions were removed to their complexity, which were conditional moves, load/stores for certain data types, and string instructions.

How features of the system might boost performance

A dedicated floating point processor is used in IA-32 architecture to improve performance of floating point operations. Modern implemenations include a SIMD-unit that allows instructions to work in parallel on larger words.

The ARM Thumb instructions mentioned in the previous section help improve code density and performance. Instructions to insert and extract bits allow packed data structures more effectively. Bit reversal instructions can reverse bits without using an extra register, which is useful for certain algorithms. Extensive branch prediction is used is some implementations in order to improve performance of conditional instructions.

PowerPC uses branch prediction to determine if a conditional branch is likely to be taken. A conditional branch that branches to a lower address is likely to be taken, as loops will branch back to the beginning of the loop many times. On the other hand, conditional branches with positive displacements are not likely to be taken. Finally, conditional branches to an address in the link or count registers are predicted not to be taken. A suffix can be added to branch instructions by the programmer, if they know if the branch is likely to be taken.

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