Random-access memory

Random-access memory (**RAM** /ræm/) is a form of computer memory that can be read and changed in any order, typically used to store working data and machine code.[1][2] A random-access memory device allows data items to be read or written in almost the same amount of time irrespective of the physical location of data inside the memory. In contrast, with other direct-access data storage media such as hard disks, CD-RWs, DVD-RWs and the older magnetic tapes and drum memory, the time required to read and write data items varies significantly depending on their physical locations on the recording medium, due to mechanical limitations such as media rotation speeds and arm movement.

Example of writable volatile random-access memory: Synchronous Dynamic RAM modules, primarily used as main memory in personal computers, workstations, and servers.

RAM contains multiplexing and demultiplexing circuitry, to connect the data lines to the addressed storage for reading or writing the entry. Usually more than one bit of storage is accessed by the same address, and RAM devices often have multiple data lines and are said to be "8-bit" or "16-bit", etc. devices.

In today's technology, random-access memory takes the form of integrated circuit (IC) chips with MOS (metal-oxide-semiconductor) memory cells. RAM is normally associated with volatile types of memory (such as dynamic random-access memory (DRAM) modules), where stored information is lost if power is removed, although non-volatile RAM has also been developed.[3] Other types of non-volatile memories exist that allow random access for read operations, but either do not allow write operations or have other kinds of limitations on them. These include most types of ROM and a type of flash memory called *NOR-Flash*.

8GB DDR3 RAM stick with a white heatsink

The two main types of volatile random-access semiconductor memory are static random-access memory (SRAM) and dynamic random-access memory (DRAM). Commercial uses of semiconductor RAM date back to 1965, when IBM introduced the SP95 SRAM chip for their System/360 Model 95 computer, and Toshiba used DRAM memory cells for its Toscal BC-1411 electronic calculator, both based on bipolar transistors. Commercial MOS memory, based on MOS transistors, was developed in the late 1960s, and has since been the basis for all commercial semiconductor memory. The first commercial DRAM IC chip, the Intel 1103, was introduced in October 1970. Synchronous dynamic random-access memory (SDRAM) later debuted with the Samsung KM48SL2000 chip in 1992.

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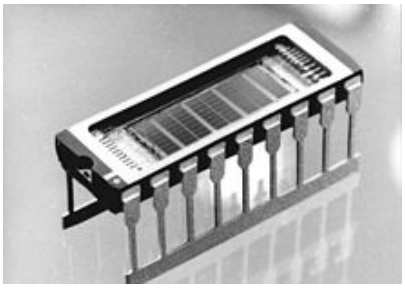
History

Early computers used relays, mechanical counters[4] or delay lines for main memory functions. Ultrasonic delay lines were serial devices which could only reproduce data in the order it was written. Drum memory could be expanded at relatively low cost but efficient retrieval of memory items required knowledge of the physical layout of the drum to optimize speed. Latches built out of vacuum tube triodes, and later, out of discrete transistors, were used for smaller and faster memories such as registers. Such registers were relatively large and too costly to use for large amounts of data; generally only a few dozen or few hundred bits of such memory could be provided.

These IBM tabulating machines from the mid-1930s used mechanical counters to store information

The first practical form of random-access memory was the Williams tube starting in 1947. It stored data as electrically charged spots on the face of a cathode ray tube. Since the electron beam of the CRT could read and write the spots on the tube in any order, memory was random access. The capacity of the Williams tube was a few hundred to around a thousand bits, but it was much smaller, faster, and more power-efficient than using individual vacuum tube latches. Developed at the University of Manchester in England, the Williams tube provided the medium on which the first electronically stored program was implemented in the Manchester Baby computer, which first successfully ran a program on 21 June 1948.[5] In fact, rather than the Williams tube memory being designed for the Baby, the Baby was a testbed to demonstrate the reliability of the memory.[6][7]



1 Megabit (MiBit) chip, one of the last models developed by VEB Carl Zeiss Jena in 1989

Magnetic-core memory was invented in 1947 and developed up until the mid-1970s. It became a widespread form of random-access memory, relying on an array of magnetized rings. By changing the sense of each ring's magnetization, data could be stored with one bit stored per ring. Since every ring had a combination of address wires to select and read or write it, access to any memory location in any sequence was possible. Magnetic core memory was the standard form of computer memory system until displaced by solid-state MOS (metal-oxide-silicon) semiconductor memory in integrated circuits (ICs) during the early 1970s.[8]

Prior to the development of integrated read-only memory (ROM) circuits, *permanent* (or *read-only*) random-access memory was often constructed using diode matrices driven by address decoders, or specially wound core rope memory planes.

Semiconductor memory began in the 1960s with bipolar memory, which used bipolar transistors. While it improved performance, it could not compete with the lower price of magnetic core memory.[9]

MOS RAM

The invention of the MOSFET (metal-oxide-semiconductor field-effect transistor), also known as the MOS transistor, by Mohamed M. Atalla and Dawon Kahng at Bell Labs in 1959,[10] led to the development of metal-oxide-semiconductor (MOS) memory by John Schmidt at Fairchild Semiconductor in 1964.[8][11] In addition to higher performance, MOS semiconductor memory was cheaper and consumed less power than magnetic core memory.[8] The development of silicon-gate MOS integrated circuit (MOS IC) technology by Federico Faggin at Fairchild in 1968 enabled the production of MOS memory chips.[12] MOS memory overtook magnetic core memory as the dominant memory technology in the early 1970s.[8]

An integrated bipolar static random-access memory (SRAM) was invented by Robert H. Norman at Fairchild Semiconductor in 1963.[13] It was followed by the development of MOS SRAM by John Schmidt at Fairchild in 1964.[8] SRAM became an alternative to magnetic-core memory, but required six MOS transistors for each bit of data.[14] Commercial use of SRAM began in 1965, when IBM introduced the SP95 memory chip for the System/360 Model 95.[9]

Dynamic random-access memory (DRAM) allowed replacement of a 4 or 6-transistor latch circuit by a single transistor for each memory bit, greatly increasing memory density at the cost of volatility. Data was stored in the tiny capacitance of each transistor, and had to be periodically refreshed every few milliseconds before the charge could leak away. Toshiba's Toscal BC-1411 electronic calculator, which was introduced in 1965,[15][16][17] used a form of capacitive bipolar DRAM, storing 180-bit data on discrete memory cells, consisting of germanium bipolar transistors and capacitors.[16][17] While it offered improved performance over magnetic-core memory, bipolar DRAM could not compete with the lower price of the then dominant magnetic-core memory.[18]

MOS technology is the basis for modern DRAM. In 1966, Dr. Robert H. Dennard at the IBM Thomas J. Watson Research Center was working on MOS memory. While examining the characteristics of MOS technology, he found it was capable of building capacitors, and that storing a charge or no charge on the MOS capacitor could represent the 1 and 0 of a bit, while the MOS transistor could control writing the charge to the capacitor. This led to his development of a single-transistor DRAM memory cell.[14] In 1967, Dennard filed a patent under IBM for a single-transistor DRAM memory cell, based on MOS technology.[19] The first commercial DRAM IC chip was the Intel 1103, which was manufactured on an 8 μm MOS process with a capacity of 1 Kibit, and was released in 1970.[8][20][21]

Synchronous dynamic random-access memory (SDRAM) was developed by Samsung Electronics. The first commercial SDRAM chip was the Samsung KM48SL2000, which had a capacity of 16 Mibit.[22] It was introduced by Samsung in 1992,[23] and mass-produced in 1993.[22] The first commercial DDR SDRAM (double data rate SDRAM) memory chip was Samsung's 64 Mibit DDR SDRAM chip, released in June 1998.[24] GDDR (graphics DDR) is a form of DDR SGRAM (synchronous graphics RAM), which was first released by Samsung as a 16 Mibit memory chip in 1998.[25]

Types

The two widely used forms of modern RAM are static RAM (SRAM) and dynamic RAM (DRAM). In SRAM, a bit of data is stored using the state of a six-transistor memory cell, typically using six MOSFETs (metal-oxide-semiconductor field-effect transistors). This form of RAM is more expensive to produce, but is generally faster and requires less dynamic power than DRAM. In modern computers, SRAM is often used as cache memory for the CPU. DRAM stores a bit of data using a transistor and capacitor pair (typically a MOSFET and MOS capacitor, respectively),[26] which together comprise a DRAM cell. The capacitor holds a high or low charge (1 or 0, respectively), and the transistor acts as a switch that lets the control circuitry on the chip read the capacitor's state of charge or change it. As this form of memory is less expensive to produce than static RAM, it is the predominant form of computer memory used in modern computers.

Both static and dynamic RAM are considered *volatile*, as their state is lost or reset when power is removed from the system. By contrast, read-only memory (ROM) stores data by permanently enabling or disabling selected transistors, such that the memory cannot be altered. Writeable variants of ROM (such as EEPROM and flash memory) share properties of both ROM and RAM, enabling data to persist without power and to be updated without requiring special equipment. These persistent forms of semiconductor ROM include USB flash drives, memory cards for cameras and portable devices, and solid-state drives. ECC memory (which can be either SRAM or DRAM) includes special circuitry to detect and/or correct random faults (memory errors) in the stored data, using parity bits or error correction codes.

In general, the term *RAM* refers solely to solid-state memory devices (either DRAM or SRAM), and more specifically the main memory in most computers. In optical storage, the term DVD-RAM is somewhat of a misnomer since, unlike CD-RW or DVD-RW it does not need to be erased before reuse. Nevertheless, a DVD-RAM behaves much like a hard disc

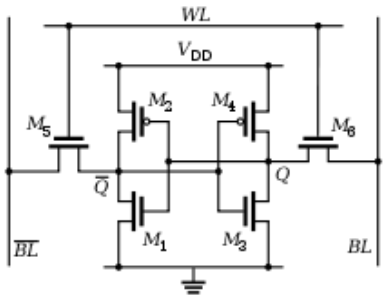
drive if somewhat slower.

Memory cell

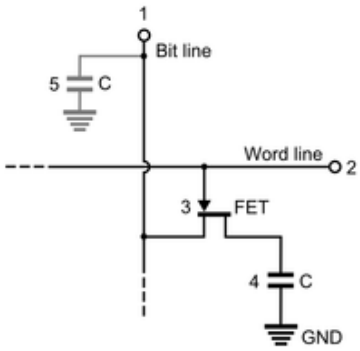
The memory cell is the fundamental building block of computer memory. The memory cell is an electronic circuit that stores one bit of binary information and it must be set to store a logic 1 (high voltage level) and reset to store a logic 0 (low voltage level). Its value is maintained/stored until it is changed by the set/reset process. The value in the memory cell can be accessed by reading it.

In SRAM, the memory cell is a type of flip-flop circuit, usually implemented using FETs. This means that SRAM requires very low power when not being accessed, but it is expensive and has low storage density.

A second type, DRAM, is based around a capacitor. Charging and discharging this capacitor can store a "1" or a "0" in the cell. However, the charge in this capacitor slowly leaks away, and must be refreshed periodically. Because of this refresh process, DRAM uses more power, but it can achieve greater storage densities and lower unit costs compared to SRAM.



SRAM Cell (6 Transistors)



DRAM Cell (1 Transistor and one capacitor)

Addressing

To be useful, memory cells must be readable and writeable. Within the RAM device, multiplexing and demultiplexing circuitry is used to select memory cells. Typically, a RAM device has a set of address lines A0... An, and for each combination of bits that may be applied to these lines, a set of memory cells are activated. Due to this addressing, RAM devices virtually always have a memory capacity that is a power of two.

Usually several memory cells share the same address. For example, a 4 bit 'wide' RAM chip has 4 memory cells for each address. Often the width of the memory and that of the microprocessor are different, for a 32 bit microprocessor, eight 4 bit RAM chips would be needed.

Often more addresses are needed than can be provided by a device. In that case, external multiplexors to the device are used to activate the correct device that is being accessed.

Memory hierarchy

One can read and over-write data in RAM. Many computer systems have a memory hierarchy consisting of processor registers, on-die SRAM caches, external caches, DRAM, paging systems and virtual memory or swap space on a hard drive. This entire pool of memory may be referred to as "RAM" by many developers, even though the various subsystems can have very different access times, violating the original concept behind the *random access* term in RAM. Even within a hierarchy level such as DRAM, the specific row, column, bank, rank, channel, or interleave organization of the components make the access time variable, although not to the extent that access time to rotating storage media or a tape is

variable. The overall goal of using a memory hierarchy is to obtain the highest possible average access performance while minimizing the total cost of the entire memory system (generally, the memory hierarchy follows the access time with the fast CPU registers at the top and the slow hard drive at the bottom).

In many modern personal computers, the RAM comes in an easily upgraded form of modules called memory modules or DRAM modules about the size of a few sticks of chewing gum. These can quickly be replaced should they become damaged or when changing needs demand more storage capacity. As suggested above, smaller amounts of RAM (mostly SRAM) are also integrated in the CPU and other ICs on the motherboard, as well as in hard-drives, CD-ROMs, and several other parts of the computer system.

Other uses of RAM

In addition to serving as temporary storage and working space for the operating system and applications, RAM is used in numerous other ways.

A SO-DIMM stick of laptop RAM, roughly half the size of desktop RAM.

Virtual memory

Most modern operating systems employ a method of extending RAM capacity, known as "virtual memory". A portion of the computer's hard drive is set aside for a *paging file* or a *scratch partition*, and the combination of physical RAM and the paging file form the system's total memory. (For example, if a computer has 2 GiB (1024^3 B) of RAM and a 1 GiB page file, the operating system has 3 GiB total memory available to it.) When the system runs low on physical memory, it can "swap" portions of RAM to the paging file to make room for new data, as well as to read previously swapped information back into RAM. Excessive use of this mechanism results in thrashing and generally hampers overall system performance, mainly because hard drives are far slower than RAM.

RAM disk

Software can "partition" a portion of a computer's RAM, allowing it to act as a much faster hard drive that is called a RAM disk. A RAM disk loses the stored data when the computer is shut down, unless memory is arranged to have a standby battery source.

Shadow RAM

Sometimes, the contents of a relatively slow ROM chip are copied to read/write memory to allow for shorter access times. The ROM chip is then disabled while the initialized memory locations are switched in on the same block of addresses (often write-protected). This process, sometimes called *shadowing*, is fairly common in both computers and embedded systems.

As a common example, the BIOS in typical personal computers often has an option called “use shadow BIOS” or similar. When enabled, functions that rely on data from the BIOS's ROM instead use DRAM locations (most can also toggle shadowing of video card ROM or other ROM sections). Depending on the system, this may not result in increased performance, and may cause incompatibilities. For example, some hardware may be inaccessible to the operating system if shadow RAM is used. On some systems the benefit may be hypothetical because the BIOS is not used after booting in favor of direct hardware access. Free memory is reduced by the size of the shadowed ROMs.[27]

Recent developments

Several new types of *non-volatile* RAM, which preserve data while powered down, are under development. The technologies used include carbon nanotubes and approaches utilizing Tunnel magnetoresistance. Amongst the 1st generation MRAM, a 128 KiB (128×2^{10} bytes) chip was manufactured with 0.18 µm technology in the summer of 2003. In June 2004, Infineon Technologies unveiled a 16 MiB (16×2^{20} bytes) prototype again based on 0.18 µm technology. There are two 2nd generation techniques currently in development: thermal-assisted switching (TAS)[28] which is being

developed by Crocus Technology, and spin-transfer torque (STT) on which Crocus, Hynix, IBM, and several other companies are working.[29] Nantero built a functioning carbon nanotube memory prototype 10 GiB (10×2^{30} bytes) array in 2004. Whether some of these technologies can eventually take significant market share from either DRAM, SRAM, or flash-memory technology, however, remains to be seen.

Since 2006, "solid-state drives" (based on flash memory) with capacities exceeding 256 gigabytes and performance far exceeding traditional disks have become available. This development has started to blur the definition between traditional random-access memory and "disks", dramatically reducing the difference in performance.

Some kinds of random-access memory, such as "EcoRAM", are specifically designed for server farms, where low power consumption is more important than speed.[30]

Memory wall

The "memory wall" is the growing disparity of speed between CPU and memory outside the CPU chip. An important reason for this disparity is the limited communication bandwidth beyond chip boundaries, which is also referred to as *bandwidth wall*. From 1986 to 2000, CPU speed improved at an annual rate of 55% while memory speed only improved at 10%. Given these trends, it was expected that memory latency would become an overwhelming bottleneck in computer performance.[31]

CPU speed improvements slowed significantly partly due to major physical barriers and partly because current CPU designs have already hit the memory wall in some sense. Intel summarized these causes in a 2005 document.[32]

> First of all, as chip geometries shrink and clock frequencies rise, the transistor leakage current increases, leading to excess power consumption and heat... Secondly, the advantages of higher clock speeds are in part negated by memory latency, since memory access times have not been able to keep pace with increasing clock frequencies. Third, for certain applications, traditional serial architectures are becoming less efficient as processors get faster (due to the so-called Von Neumann bottleneck), further undercutting any gains that frequency increases might otherwise buy. In addition, partly due to limitations in the means of producing inductance within solid state devices, resistance-capacitance (RC) delays in signal transmission are growing as feature sizes shrink, imposing an additional bottleneck that frequency increases don't address.

The RC delays in signal transmission were also noted in "Clock Rate versus IPC: The End of the Road for Conventional Microarchitectures"[33] which projected a maximum of 12.5% average annual CPU performance improvement between 2000 and 2014.

A different concept is the processor-memory performance gap, which can be addressed by 3D integrated circuits that reduce the distance between the logic and memory aspects that are further apart in a 2D chip.[34] Memory subsystem design requires a focus on the gap, which is widening over time.[35] The main method of bridging the gap is the use of caches; small amounts of high-speed memory that houses recent operations and instructions nearby the processor, speeding up the execution of those operations or instructions in cases where they are called upon frequently. Multiple levels of caching have been developed to deal with the widening gap, and the performance of high-speed modern computers relies on evolving caching techniques.[36] There can be up to a 53% difference between the growth in speed of processor speeds and the lagging speed of main memory access.[37]

Solid-state hard drives have continued to increase in speed, from ~400 Mbit/s via SATA3 in 2012 up to ~3 GB/s via NVMe/PCIe in 2018, closing the gap between RAM and hard disk speeds, although RAM continues to be an order of magnitude faster, with single-lane DDR4 3200 capable of 25 GB/s, and modern GDDR even faster. Fast, cheap, non-volatile solid state drives have replaced some functions formerly performed by RAM, such as holding certain data for immediate availability in server farms - 1 terabyte of SSD storage can be had for $200, while 1 TiB of RAM would cost thousands of dollars.[38][39]

Timeline

SRAM

Static random-access memory (SRAM)

Date of introduction	Chip name	Capacity (bits)	Access time	SRAM type	Manufacturer(s)	Process	MOSFET	Ref
March 1963	N/A	1-bit	*?*	Bipolar (cell)	Fairchild	N/A	N/A	[9]
1965	*?*	8-bit	*?*	Bipolar	IBM	*?*	N/A	
	SP95	16-bit	*?*	Bipolar	IBM	*?*	N/A	[40]
	?	64-bit	*?*	MOSFET	Fairchild	*?*	PMOS	[41]
1966	TMC3162	16-bit	*?*	Bipolar (TTL)	Transitron	*?*	N/A	[8]
	?	*?*	*?*	MOSFET	NEC	*?*	*?*	[42]
1968	*?*	64-bit	*?*	MOSFET	Fairchild	*?*	PMOS	[42]
		144-bit	*?*	MOSFET	NEC	*?*	NMOS	
		512-bit	*?*	MOSFET	IBM	*?*	NMOS	[41]
1969	*?*	128-bit	*?*	Bipolar	IBM	*?*	N/A	[9]
	1101	256-bit	850 ns	MOSFET	Intel	12,000 nm	PMOS	[43][44][45][46]
1972	2102	1 Kibit	*?*	MOSFET	Intel	*?*	NMOS	[43]
1974	5101	1 Kibit	800 ns	MOSFET	Intel	*?*	CMOS	[43][47]
	2102A	1 Kibit	350 ns	MOSFET	Intel	*?*	NMOS (depletion)	[43][48]
1975	2114	4 Kibit	450 ns	MOSFET	Intel	*?*	NMOS	[43][47]
1976	2115	1 Kibit	70 ns	MOSFET	Intel	*?*	NMOS (HMOS)	[43][44]
	2147	4 Kibit	55 ns	MOSFET	Intel	*?*	NMOS (HMOS)	[43][49]
1977	*?*	4 Kibit	*?*	MOSFET	Toshiba	*?*	CMOS	[44]
1978	HM6147	4 Kibit	55 ns	MOSFET	Hitachi	3,000 nm	CMOS (twin-well)	[49]
	TMS4016	16 Kibit	*?*	MOSFET	Texas Instruments	*?*	NMOS	[44]
1980	*?*	16 Kibit	*?*	MOSFET	Hitachi, Toshiba	*?*	CMOS	[50]
		64 Kibit	*?*	MOSFET	Matsushita			
1981	*?*	16 Kibit	*?*	MOSFET	Texas Instruments	2,500 nm	NMOS	[50]
October 1981	*?*	4 Kibit	18 ns	MOSFET	Matsushita, Toshiba	2,000 nm	CMOS	[51]
1982	*?*	64 Kibit	*?*	MOSFET	Intel	1,500 nm	NMOS (HMOS)	[50]
February 1983	*?*	64 Kibit	50 ns	MOSFET	Mitsubishi	*?*	CMOS	[52]
1984	*?*	256 Kibit	*?*	MOSFET	Toshiba	1,200 nm	CMOS	[50][45]
1987	*?*	1 Mibit	*?*	MOSFET	Sony, Hitachi, Mitsubishi, Toshiba	*?*	CMOS	[50]
December 1987	*?*	256 Kibit	10 ns	BiMOS	Texas Instruments	800 nm	BiCMOS	[53]
1990	*?*	4 Mibit	15–23 ns	MOSFET	NEC, Toshiba, Hitachi, Mitsubishi	*?*	CMOS	[50]
1992	*?*	16 Mibit	12–15 ns	MOSFET	Fujitsu, NEC	400 nm		
December 1994	*?*	512 Kibit	2.5 ns	MOSFET	IBM	*?*	CMOS	[54]

							(SOI)	
1995	***?***	4 Mibit	6 ns	Cache (SyncBurst)	Hitachi	100 nm	CMOS	[55]
		256 Mibit	***?***	MOSFET	Hyundai	***?***	CMOS	[56]

DRAM

Dynamic random-access memory (DRAM)

Date of introduction	Chip name	Capacity (bits)	DRAM type	Manufacturer(s)	Process	MOSFET	Area	Ref
1965	N/A	1-bit	DRAM (cell)	Toshiba	N/A	N/A	N/A	[16][17]
1967	N/A	1-bit	DRAM (cell)	IBM	N/A	MOS	N/A	[19][42]
1968	?	256-bit	DRAM (IC)	Fairchild	?	PMOS	?	[8]
1969	N/A	1-bit	DRAM (cell)	Intel	N/A	PMOS	N/A	[42]
1970	1102	1 Kibit	DRAM (IC)	Intel, Honeywell	?	PMOS	?	[42]
	1103	1 Kibit	DRAM	Intel	8,000 nm	PMOS	10 mm²	[57][58][20]
1971	μPD403	1 Kibit	DRAM	NEC	?	NMOS	?	[59]
	?	2 Kibit	DRAM	General Instrument	?	PMOS	13 mm²	[60]
1972	2107	4 Kibit	DRAM	Intel	?	NMOS	?	[43][61]
1973	?	8 Kibit	DRAM	IBM	?	PMOS	19 mm²	[60]
1975	2116	16 Kibit	DRAM	Intel	?	NMOS	?	[62][8]
1977	?	64 Kibit	DRAM	NTT	?	NMOS	35 mm²	[60]
1979	MK4816	16 Kibit	PSRAM	Mostek	?	NMOS	?	[63]
	?	64 Kibit	DRAM	Siemens	?	VMOS	25 mm²	[60]
1980	?	256 Kibit	DRAM	NEC, NTT	1,000–1,500 nm	NMOS	34–42 mm²	[60]
1981	?	288 Kibit	DRAM	IBM	?	MOS	25 mm²	[64]
1983	?	64 Kibit	DRAM	Intel	1,500 nm	CMOS	20 mm²	[60]
		256 Kibit	DRAM	NTT	?	CMOS	31 mm²	
January 5, 1984	?	8 Mibit	DRAM	Hitachi	?	MOS	?	[65][66]
February 1984	?	1 Mibit	DRAM	Hitachi, NEC	1,000 nm	NMOS	74–76 mm²	[60][67]
				NTT	800 nm	CMOS	53 mm²	[60][67]
1984	TMS4161	64 Kibit	DPRAM (VRAM)	Texas Instruments	?	NMOS	?	[68][69]
January 1985	μPD41264	258 Kibit	DPRAM (VRAM)	NEC	?	NMOS	?	[70][71]
June 1986	?	1 Mibit	PSRAM	Toshiba	?	CMOS	?	[72]
1986	?	4 Mibit	DRAM	NEC	800 nm	NMOS	99 mm²	[60]
				Texas Instruments, Toshiba	1,000 nm	CMOS	100–137 mm²	
1987	?	16 Mibit	DRAM	NTT	700 nm	CMOS	148 mm²	[60]
October 1988	?	512 Kibit	HSDRAM	IBM	1,000 nm	CMOS	78 mm²	[73]
1991	?	64 Mibit	DRAM	Matsushita, Mitsubishi, Fujitsu, Toshiba	400 nm	CMOS	?	[50]
1993	?	256 Mibit	DRAM	Hitachi, NEC	250 nm	CMOS	?	

1995	***?***	4 Mibit	DPRAM (VRAM)	Hitachi	***?***	CMOS	***?***	[55]
January 9, 1995	***?***	1 Gibit	DRAM	NEC	250 nm	CMOS	***?***	[74][55]
				Hitachi	160 nm	CMOS	***?***	
1996	***?***	4 Mibit	FRAM	Samsung	***?***	NMOS	***?***	[75]
1997	***?***	4 Gb	QLC	NEC	150 nm	CMOS	***?***	[50]
1998	***?***	4 Gibit	DRAM	Hyundai	***?***	CMOS	***?***	[56]
June 2001	TC51W3216XB	32 Mibit	PSRAM	Toshiba	***?***	CMOS	***?***	[76]
February 2001	***?***	4 Gibit	DRAM	Samsung	100 nm	CMOS	***?***	[50][77]

SDRAM

Synchronous dynamic random-access memory (SDRAM)

Date of introduction	Chip name	Capacity (bits)	SDRAM type	Manufacturer(s)	Process	MOSFET	Area	Ref
1992	KM48SL2000	16 Mb	SDR	Samsung	?	CMOS	?	[78][22]
1996	MSM5718C50	18 Mb	RDRAM	Oki	?	CMOS	325 mm²	[79]
	N64 RDRAM	36 Mb	RDRAM	NEC	?	CMOS	?	[80]
	?	1 Gb	SDR	Mitsubishi	150 nm	CMOS	?	[50]
1997	?	1 Gb	SDR	Hyundai	?	SOI	?	[56]
1998	MD5764802	64 Mb	RDRAM	Oki	?	CMOS	325 mm²	[79]
March 1998	Direct RDRAM	72 Mb	RDRAM	Rambus	?	CMOS	?	[81]
June 1998	?	64 Mb	DDR	Samsung	?	CMOS	?	[82][83][84]
1998	?	64 Mb	DDR	Hyundai	?	CMOS	?	[56]
		128 Mb	SDR	Samsung	?	CMOS	?	[85][83]
1999	?	128 Mb	DDR	Samsung	?	CMOS	?	[83]
		1 Gb	DDR	Samsung	140 nm	CMOS	?	[50]
2000	GS eDRAM	32 Mb	eDRAM	Sony, Toshiba	180 nm	CMOS	279 mm²	[86]
2001	?	288 Mb	RDRAM	Hynix	?	CMOS	?	[87]
		?	DDR2	Samsung	100 nm	CMOS	?	[84][50]
2002	?	256 Mb	SDR	Hynix	?	CMOS	?	[87]
2003	EE+GS eDRAM	32 Mb	eDRAM	Sony, Toshiba	90 nm	CMOS	86 mm²	[86]
	?	72 Mb	DDR3	Samsung	90 nm	CMOS	?	[88]
		512 Mb	DDR2	Hynix	?	CMOS	?	[87]
				Elpida	110 nm	CMOS	?	[89]
		1 Gb	DDR2	Hynix	?	CMOS	?	[87]
2004	?	2 Gb	DDR2	Samsung	80 nm	CMOS	?	[90]
2005	EE+GS eDRAM	32 Mb	eDRAM	Sony, Toshiba	65 nm	CMOS	86 mm²	[91]
	Xenos eDRAM	80 Mb	eDRAM	NEC	90 nm	CMOS	?	[92]
	?	512 Mb	DDR3	Samsung	80 nm	CMOS	?	[84][93]
2006	?	1 Gb	DDR2	Hynix	60 nm	CMOS	?	[87]
2008	?	?	LPDDR2	Hynix	?			
April 2008	?	8 Gb	DDR3	Samsung	50 nm	CMOS	?	[94]
2008	?	16 Gb	DDR3	Samsung	50 nm	CMOS	?	
2009	?	?	DDR3	Hynix	44 nm	CMOS	?	[87]
		2 Gb	DDR3	Hynix	40 nm			
2011	?	16 Gb	DDR3	Hynix	40 nm	CMOS	?	[95]
		2 Gb	DDR4	Hynix	30 nm	CMOS	?	[95]
2013	?	?	LPDDR4	Samsung	20 nm	CMOS	?	[95]
2014	?	8 Gb	LPDDR4	Samsung	20 nm	CMOS	?	[96]
2015	?	12 Gb	LPDDR4	Samsung	20 nm	CMOS	?	[85]

2018	?	8 Gb	LPDDR5	Samsung	10 nm	FinFET	?	[97]
		128 Gb	DDR4	Samsung	10 nm	FinFET	?	[98]

SGRAM and HBM

Synchronous graphics random-access memory (SGRAM) and High Bandwidth Memory (HBM)

Date of introduction	Chip name	Capacity (bits)	SDRAM type	Manufacturer(s)	Process	MOSFET	Area	Ref
November 1994	HM5283206	8 Mibit	SGRAM (SDR)	Hitachi	350 nm	CMOS	58 mm²	[99][100]
December 1994	µPD481850	8 Mibit	SGRAM (SDR)	NEC	?	CMOS	280 mm²	[101][102]
1997	µPD4811650	16 Mibit	SGRAM (SDR)	NEC	350 nm	CMOS	280 mm²	[103][104]
September 1998	?	16 Mibit	SGRAM (GDDR)	Samsung	?	CMOS	?	[82]
1999	KM4132G112	32 Mibit	SGRAM (SDR)	Samsung	?	CMOS	?	[105]
2002	?	128 Mibit	SGRAM (GDDR2)	Samsung	?	CMOS	?	[106]
2003	?	256 Mibit	SGRAM (GDDR2)	Samsung	?	CMOS	?	[106]
			SGRAM (GDDR3)					
March 2005	K4D553238F	256 Mibit	SGRAM (GDDR)	Samsung	?	CMOS	77 mm²	[107]
October 2005	?	256 Mibit	SGRAM (GDDR4)	Samsung	?	CMOS	?	[108]
2005	?	512 Mibit	SGRAM (GDDR4)	Hynix	?	CMOS	?	[87]
2007	?	1 Gibit	SGRAM (GDDR5)	Hynix	60 nm			
2009	?	2 Gibit	SGRAM (GDDR5)	Hynix	40 nm			
2010	K4W1G1646G	1 Gibit	SGRAM (GDDR3)	Samsung	?	CMOS	100 mm²	[109]
2012	?	4 Gibit	SGRAM (GDDR3)	SK Hynix	?	CMOS	?	[95]
2013	?	?	HBM					
March 2016	MT58K256M32JA	8 Gibit	SGRAM (GDDR5X)	Micron	20 nm	CMOS	140 mm²	[110]
June 2016	?	32 Gibit	HBM2	Samsung	20 nm	CMOS	?	[111][112]
2017	?	64 Gibit	HBM2	Samsung	20 nm	CMOS	?	[111]
January 2018	K4ZAF325BM	16 Gibit	SGRAM (GDDR6)	Samsung	10 nm	FinFET	?	[113][114][115]

See also

- CAS latency (CL)
- Hybrid Memory Cube
- Multi-channel memory architecture

- Registered/buffered memory
- RAM parity
- Memory Interconnect/RAM buses
- Memory geometry
- Chip creep
- Read-mostly memory (RMM)
- Electrochemical random-access memory

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