128-bit

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Computer architecture bit widths

Bit

- 1
- 2
- 4
- 8
- 12
- 16
- 18
- 24
- 26
- 31
- 32
- 36
- 48
- 60
- 64
- 128
- 256
- 512

Application

- 8
- 16
- 32
- 64

Binary floating-point precision

- 16
- 32
- 40

- 64
- 80
- 128
- 256

- ×½
- ×1
- ×2
- ×4
- ×8

Decimal floating-point precision

- 32
- 64
- 128

- v
- t
- e

In computer architecture, **128-bit** integers, memory addresses, or other data units are those that are 128 bits (16 octets) wide. Also, 128-bit CPU and ALU architectures are those that are based on registers, address buses, or data buses of that size.

While there are currently no mainstream general-purpose processors built to operate on **128-bit** *integers* or addresses, a number of processors do have specialized ways to operate on 128-bit chunks of data. The IBM System/370 could be considered the first simple 128-bit computer, as it used 128-bit floating-point registers. Most modern CPUs feature single-instruction multiple-data (SIMD) instruction sets (Streaming SIMD Extensions, AltiVec etc.) where 128-bit vector registers are used to store several smaller numbers, such as four 32-bit floating-point numbers. A single instruction can then operate on all these values in parallel. However, these processors do not operate on individual numbers that are 128 binary digits in length; only their registers have the size of 128 bits.

The DEC VAX supported operations on 128-bit integer ('O' or octaword) and 128-bit floating-point ('H-float' or HFLOAT) datatypes. Support for such operations was an upgrade option rather than being a standard feature. Since the VAX's registers were 32 bits wide, a 128-bit operation used four consecutive registers or four longwords in memory.

The ICL 2900 Series provided a 128-bit accumulator, and its instruction set included 128-bit floating-point and packed decimal arithmetic.

In the same way that compilers emulate e.g. 64-bit integer arithmetic on architectures with register sizes less than 64 bits, some compilers also support 128-bit integer arithmetic. For example, the GCC C compiler 4.6 and later has a 128-bit integer type `__int128` for some architectures.[1] For the C programming language, this is a compiler-specific extension, as C11 itself does not guarantee support for 128-bit integers.

A 128-bit register can store 2^{128} (over 3.40×10^{38}) different values. The range of integer values that can be stored in 128 bits depends on the integer representation used. With the two most common representations, the range is 0 through 340,282,366,920,938,463,463,374,607,431,768,211,455 ($2^{128} - 1$) for representation as an (unsigned) binary number, and −170,141,183,460,469,231,731,687,303,715,884,105,728 (-2^{127}) through 170,141,183,460,469,231,731,687,303,715,884,105,727 ($2^{127} - 1$) for representation as two's complement.

Uses

- The free software used to implement RISC-V architecture is defined for 32, 64 and 128 bits of integer data width.
- Universally Unique Identifiers (UUID) consist of a 128-bit value.
- IPv6 routes computer network traffic amongst a 128-bit range of addresses.
- ZFS is a 128-bit file system.
- GPU chips commonly move data across a 128-bit bus.[2]
- 128 bits is a common key size for symmetric ciphers and a common block size for block ciphers in cryptography.
- 128-bit processors could be used for addressing directly up to 2^{128} (over 3.40×10^{38}) bytes, which would greatly exceed the total data stored on Earth as of 2010, which has been estimated to be around 1.2 zettabytes (1.42×10^{21} bytes).[3]
- Quadruple precision (128-bit) floating-point numbers can store 64-bit fixed point numbers or integers accurately without losing precision.
- The AS/400 virtual instruction set defines all pointers as 128-bit. This gets translated to the hardware's real instruction set as required, allowing the underlying hardware to change without needing to recompile the software. Past hardware was 48-bit CISC, while current hardware is 64-bit PowerPC. Because pointers are defined to be 128-bit, future hardware may be 128-bit without software incompatibility.
- Increasing the word size can speed up multiple precision mathematical libraries. Applications include cryptography, and potentially speed up algorithms used in complex mathematical processing (numerical analysis, signal processing, complex photo editing and audio and video processing).
- MD5 algorithm is a widely used hash function producing a 128-bit hash value.
- Apache Avro uses a 128-bit random number as synchronization marker for efficient splitting of data files.[4]

History

A 128-bit multicomparator was described by researchers in 1976.[5]

A CPU with 128-bit multimedia extensions was designed by researchers in 1999.[6]

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- **v**
- **t**
- **e**

Processor technologies

Models

- Turing machine
  - Universal
  - Post–Turing
  - Quantum
- Belt machine
- Stack machine
- Finite-state machine
  - with datapath
  - Hierarchical
  - Queue automaton
- Register machines
  - Counter
  - Pointer
  - Random-access
  - Random-access stored program

Architecture

- Von Neumann
- Harvard
  - modified

- Dataflow
- Transport-triggered
- Cellular
- Endianness
- Memory access
  - NUMA
  - HUMA
  - Load/store
  - Register/memory
- Cache hierarchy
- Memory hierarchy
  - Virtual memory
  - Secondary storage
- Heterogeneous
- Fabric
- Multiprocessing
- Cognitive
- Neuromorphic

Instruction set architectures

Types

- CISC
- RISC
- Application-specific
- EDGE
  - TRIPS
- VLIW
  - EPIC
- MISC
- OISC
- NISC
- ZISC
- comparison
  - addressing modes

- x86
- ARM
- MIPS
- Power
  - PowerPC
- SPARC
- Itanium
- Unicore
- MicroBlaze
- RISC-V
- others

Execution

Instruction pipelining

- Pipeline stall
- Operand forwarding
- Classic RISC pipeline

Hazards

- Data dependency
- Structural
- Control
- False sharing

Out-of-order

- Tomasulo algorithm
  - Reservation station
  - Re-order buffer
- Register renaming

Speculative

- Branch prediction
- Memory dependence prediction

Parallelism

Level

- Bit
  - Bit-serial
  - Word
- Instruction
- Pipelining
  - Scalar
  - Superscalar
- Task
  - Thread
  - Process
- Data
  - Vector
- Memory
- Distributed

Multithreading

- Temporal
- Simultaneous
  - Hyperthreading
- Speculative
- Preemptive
- Cooperative

Flynn's taxonomy

- SISD
- SIMD
  - SWAR
- SIMT
- MISD
- MIMD
  - SPMD

Processor Performance

- Transistor count
- Instructions per cycle (IPC)
  - Cycles per instruction (CPI)
- Instructions per second (IPS)

		Floating-point operations per second (FLOPS) Transactions per second (TPS) Synaptic updates per second (SUPS) Performance per watt (PPW) Cache performance metrics Computer performance by orders of magnitude
		Central processing unit (CPU) Graphics processing unit (GPU) GPGPU Vector Barrel Stream Coprocessor ASIC FPGA CPLD Multi-chip module (MCM) System in package (SiP)
Types	**By application**	Microprocessor Microcontroller Mobile Notebook Ultra-low-voltage ASIP
	Systems on Chip	System-on-Chip (SoC) Multiprocessor (MPSoC) Programmable (PSoC) Network-on-Chip (NoC)
	Hardware accelerators	AI accelerator Vision processing unit (VPU) Physics processing unit (PPU) Digital signal processor (DSP) Tensor processing unit (TPU) Secure cryptoprocessor Network processor Baseband processor
Word size		1-bit 2-bit 4-bit 8-bit 16-bit 32-bit

- 48-bit
- 64-bit
- 128-bit
- 256-bit
- 512-bit
- others
  - variable

Core count

- Single-core
- Multi-core
- Manycore
- Heterogeneous architecture

Components

- Core
- Cache
  - CPU cache
  - replacement policies
  - coherence
- Bus
- Clock rate
- FIFO

Functional units

- Arithmetic logic unt (ALU)
- Address generation unit (AGU)
- Floating-point unit (FPU)
- Memory management unit
  - Load–store unit
  - Translation lookaside buffer (TLB)

Logic

- Combinational
- Sequential
- Glue
- Logic Gate
  - Quantum
  - Array

Registers

- Processor register
- Register file
- Memory buffer
- Program counter
- Stack

Control unit

- Instruction unit
- Data buffer
- Write buffer
- Microcode ROM

- Counter

Datapath

- Multiplexer
- Demultiplexer
- Adder
- Multiplier
  - CPU
- Binary decoder
  - Address decoder
  - Sum addressed decoder
- Barrel shifter

Circuitry

- Integrated circuit
  - 3D
  - Mixed signal
  - Power management
- Boolean
- Digital
- Analog
- Quantum
- Switch

Power management

- PMU
- APM
- ACPI
- Dynamic frequency scaling
- Dynamic voltage scaling
- Clock gating
- Performance per watt (PPW)

Related

- History of general-purpose CPUs
- Microprocessor chronology
- Processor design
- Digital electronics
- Hardware security module

Categories:

- Data unit

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- Talk
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- Create account
- Log in

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- Talk

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- Edit
- View history

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- Português
- Русский
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