# 128-bit

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In [computer architecture](https://en.wikipedia.org/wiki/Computer_architecture), **128-bit** [integers](https://en.wikipedia.org/wiki/Integer_(computer_science)), [memory addresses](https://en.wikipedia.org/wiki/Memory_address), or other [data](https://en.wikipedia.org/wiki/Data" \l "Uses_of_data_in_computing) units are those that are 128 [bits](https://en.wikipedia.org/wiki/Bit) (16 octets) wide. Also, 128-bit [CPU](https://en.wikipedia.org/wiki/Central_processing_unit) and [ALU](https://en.wikipedia.org/wiki/Arithmetic_logic_unit) architectures are those that are based on [registers](https://en.wikipedia.org/wiki/Processor_register), [address buses](https://en.wikipedia.org/wiki/Address_bus), or [data buses](https://en.wikipedia.org/wiki/Bus_(computing)) of that size.

While there are currently no mainstream general-purpose processors built to operate on **128-bit** *integers* or addresses, a number of processors do have specialized ways to operate on 128-bit chunks of data. The [IBM System/370](https://en.wikipedia.org/wiki/IBM_System/370) could be considered the first simple 128-bit computer, as it used 128-bit [floating-point](https://en.wikipedia.org/wiki/Floating-point) registers. Most modern CPUs feature [single-instruction multiple-data](https://en.wikipedia.org/wiki/Single_instruction,_multiple_data) (SIMD) instruction sets ([Streaming SIMD Extensions](https://en.wikipedia.org/wiki/Streaming_SIMD_Extensions), [AltiVec](https://en.wikipedia.org/wiki/AltiVec) etc.) where 128-bit vector registers are used to store several smaller numbers, such as four 32-bit floating-point numbers. A single instruction can then operate on all these values in parallel. However, these processors do not operate on individual numbers that are 128 binary digits in length; only their [registers](https://en.wikipedia.org/wiki/Processor_register) have the size of 128 bits.

The DEC [VAX](https://en.wikipedia.org/wiki/VAX) supported operations on 128-bit integer ('O' or octaword) and 128-bit floating-point ('H-float' or HFLOAT) datatypes. Support for such operations was an upgrade option rather than being a standard feature. Since the VAX's registers were 32 bits wide, a 128-bit operation used four consecutive registers or four longwords in memory.

The [ICL 2900 Series](https://en.wikipedia.org/wiki/ICL_2900_Series) provided a 128-bit accumulator, and its instruction set included 128-bit floating-point and [packed decimal](https://en.wikipedia.org/wiki/Packed_decimal) arithmetic.

In the same way that compilers emulate e.g. 64-bit integer arithmetic on architectures with register sizes less than 64 bits, some compilers also support 128-bit integer arithmetic. For example, the [GCC C compiler](https://en.wikipedia.org/wiki/GNU_Compiler_Collection) 4.6 and later has a 128-bit integer type \_\_int128 for some architectures.[[1]](https://en.wikipedia.org/wiki/128-bit" \l "cite_note-1) For the [C programming language](https://en.wikipedia.org/wiki/C_programming_language), this is a compiler-specific extension, as [C11](https://en.wikipedia.org/wiki/C11_(C_standard_revision)) itself does not guarantee support for 128-bit integers.

A 128-bit register can store 2128 (over 3.40 × 1038) different values. The range of [integer](https://en.wikipedia.org/wiki/Integer) values that can be stored in 128 bits depends on the [integer representation](https://en.wikipedia.org/wiki/Integer_(computer_science)" \l "Value_and_representation) used. With the two most common representations, the range is 0 through 340,282,366,920,938,463,463,374,607,431,768,211,455 (2128 − 1) for representation as an ([unsigned](https://en.wikipedia.org/wiki/Signedness)) [binary number](https://en.wikipedia.org/wiki/Binary_number), and −170,141,183,460,469,231,731,687,303,715,884,105,728 (−2127) through 170,141,183,460,469,231,731,687,303,715,884,105,727 (2127 − 1) for representation as [two's complement](https://en.wikipedia.org/wiki/Two's_complement).

## Uses

* The [free software](https://en.wikipedia.org/wiki/Free_software) used to implement [RISC-V](https://en.wikipedia.org/wiki/RISC-V) [architecture](https://en.wikipedia.org/wiki/CPU_architecture) is defined for 32, 64 and 128 bits of integer data width.
* [Universally Unique Identifiers](https://en.wikipedia.org/wiki/Universally_Unique_Identifier) (UUID) consist of a 128-bit value.
* [IPv6](https://en.wikipedia.org/wiki/IPv6) routes computer network traffic amongst a 128-bit range of addresses.
* [ZFS](https://en.wikipedia.org/wiki/ZFS) is a 128-bit file system.
* [GPU](https://en.wikipedia.org/wiki/GPU) chips commonly move data across a 128-bit bus.[[2]](https://en.wikipedia.org/wiki/128-bit" \l "cite_note-2)
* 128 bits is a common [key size](https://en.wikipedia.org/wiki/Key_size) for [symmetric ciphers](https://en.wikipedia.org/wiki/Symmetric_cipher) and a common block size for [block ciphers](https://en.wikipedia.org/wiki/Block_cipher) in [cryptography](https://en.wikipedia.org/wiki/Cryptography).
* 128-bit processors could be used for addressing directly up to 2128 (over 3.40 × 1038) bytes, which would greatly exceed the total data stored on Earth as of 2010, which has been estimated to be around 1.2 [zettabytes](https://en.wikipedia.org/wiki/Zettabyte) (1.42 × 1021 bytes).[[3]](https://en.wikipedia.org/wiki/128-bit" \l "cite_note-3)
* [Quadruple precision](https://en.wikipedia.org/wiki/Quadruple_precision) (128-bit) [floating-point](https://en.wikipedia.org/wiki/Floating-point) numbers can store 64-bit [fixed point](https://en.wikipedia.org/wiki/Fixed-point_arithmetic) numbers or [integers](https://en.wikipedia.org/wiki/Integer_(computer_science)) accurately without losing [precision](https://en.wikipedia.org/wiki/Accuracy_and_precision).
* The [AS/400](https://en.wikipedia.org/wiki/AS/400) virtual instruction set defines all pointers as 128-bit. This gets translated to the hardware's real instruction set as required, allowing the underlying hardware to change without needing to recompile the software. Past hardware was 48-bit [CISC](https://en.wikipedia.org/wiki/Complex_instruction_set_computing), while current hardware is 64-bit [PowerPC](https://en.wikipedia.org/wiki/PowerPC). Because pointers are defined to be 128-bit, future hardware may be 128-bit without software incompatibility.
* Increasing the word size can speed up [multiple precision](https://en.wikipedia.org/wiki/Arbitrary-precision_arithmetic) mathematical libraries. Applications include [cryptography](https://en.wikipedia.org/wiki/Cryptography), and potentially speed up algorithms used in complex mathematical processing ([numerical analysis](https://en.wikipedia.org/wiki/Numerical_analysis), [signal processing](https://en.wikipedia.org/wiki/Signal_processing), complex [photo editing](https://en.wikipedia.org/wiki/Photo_manipulation) and [audio](https://en.wikipedia.org/wiki/Audio_signal_processing) and [video processing](https://en.wikipedia.org/wiki/Video_processing)).
* [MD5](https://en.wikipedia.org/wiki/MD5) algorithm is a widely used hash function producing a 128-bit hash value.
* [Apache Avro](https://en.wikipedia.org/wiki/Apache_Avro) uses a 128-bit random number as synchronization marker for efficient splitting of data files.[[4]](https://en.wikipedia.org/wiki/128-bit" \l "cite_note-4)

## History

A 128-bit [multicomparator](https://en.wikipedia.org/wiki/Multicomparator) was described by researchers in 1976.[[5]](https://en.wikipedia.org/wiki/128-bit" \l "cite_note-5)

A CPU with 128-bit multimedia extensions was designed by researchers in 1999.[[6]](https://en.wikipedia.org/wiki/128-bit" \l "cite_note-6)

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