VLSI Homework 2

110612008 沈昱翔

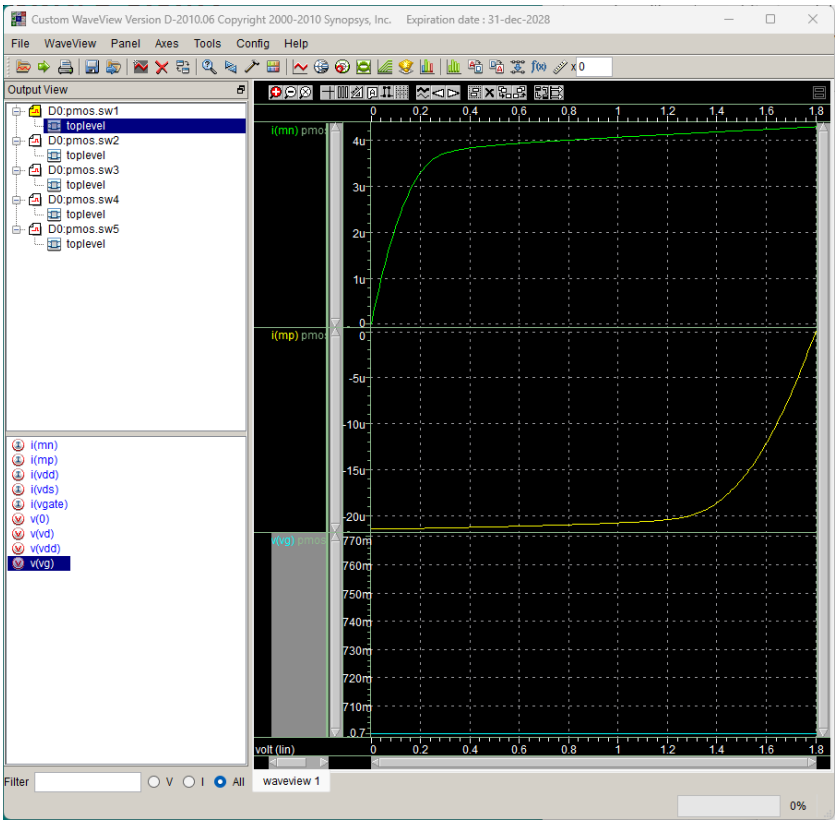
1.

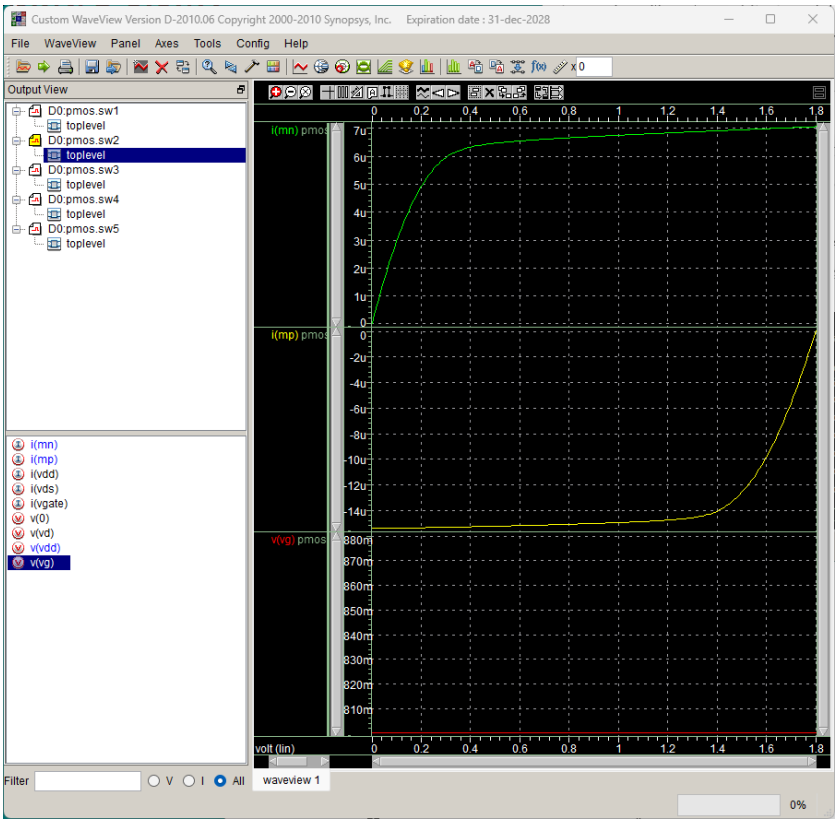
1)

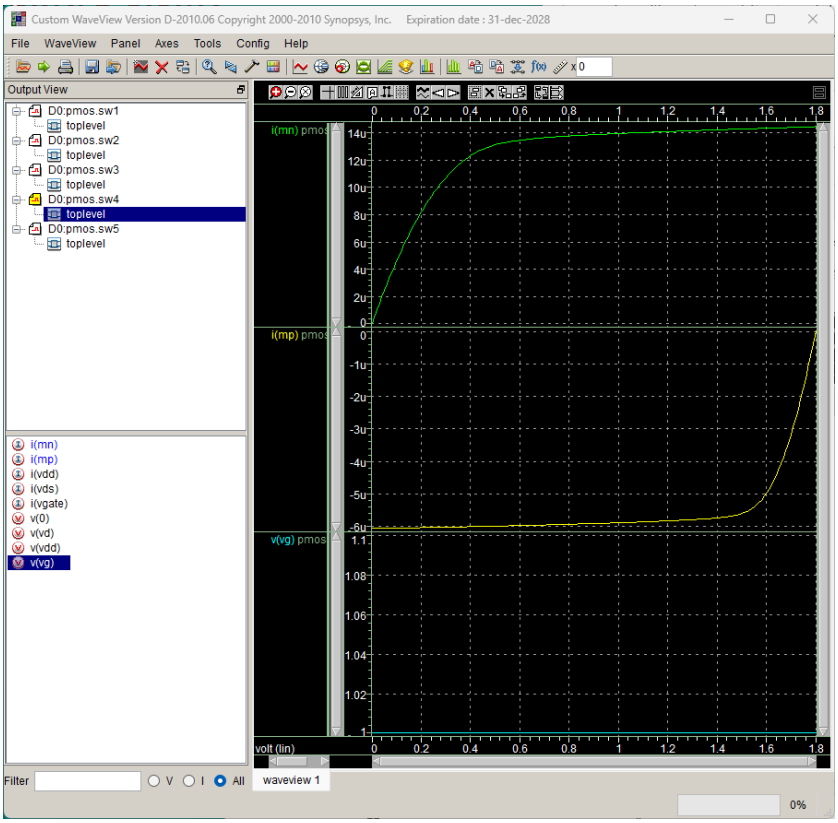
MN	vd	vg	gnd	gnd	n_18	W=0.29783u	L=1u	m=1
MP	vd	vg	vdd	vdd	p_18	W=1.0962u	L=1u	m=2

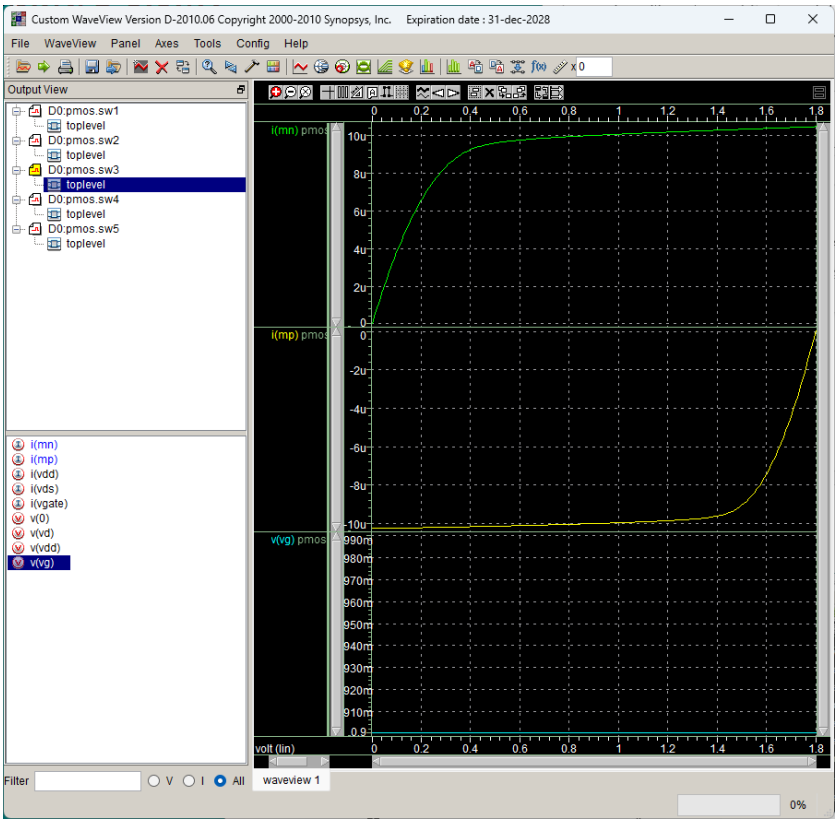
$$(\frac{W}{L})_n = 0.29783$$
$$(\frac{W}{L})_p = 1.09620$$

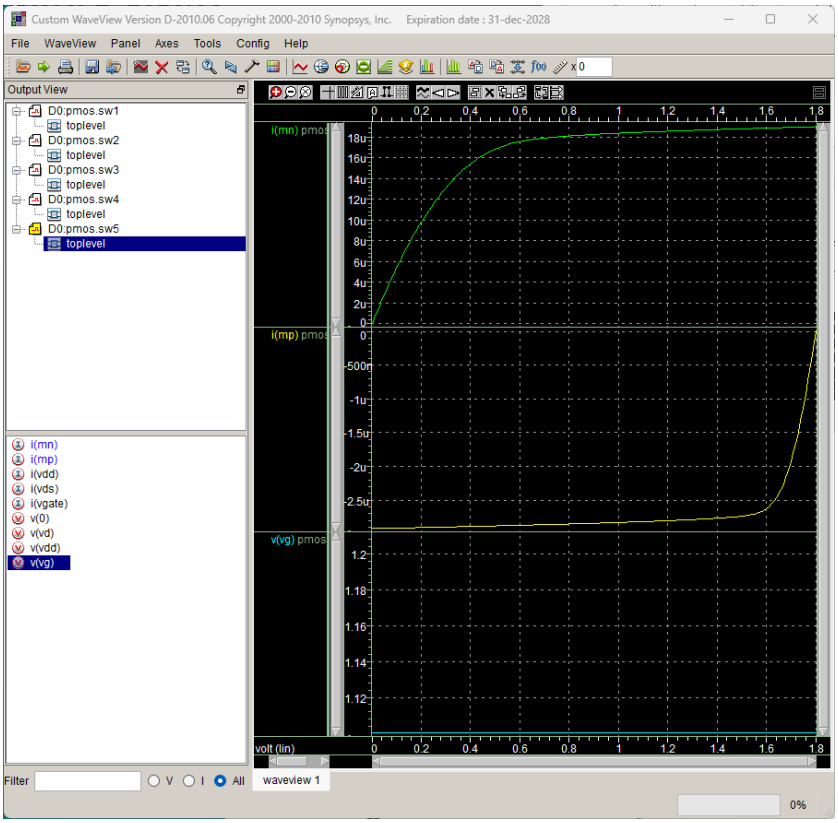
2)




Custom WaveView Version D-2010.06 Copyright 2000-2010 Synopsys, Inc. Expiration date : 31-dec-2028
File WaveView Panel Axes Tools Config Help
Output View
D0:pmos.sw1
toplevel
D0:pmos.sw2
toplevel
D0:pmos.sw3
toplevel
D0:pmos.sw4
toplevel
D0:pmos.sw5
toplevel
i(mn)
i(mp)
i(vdd)
i(vds)
i(vgate)
v(0)
v(vd)
v(vdd)
v(vg)
i(mn) pmos
i(mp) pmos
v(vg) pmos
volt (lin)
Filter
V I All
waveview 1
0%


Custom WaveView Version D-2010.06 Copyright 2000-2010 Synopsys, Inc. Expiration date : 31-dec-2028
File WaveView Panel Axes Tools Config Help
Output View
D0:pmos.sw1
toplevel
D0:pmos.sw2
toplevel
D0:pmos.sw3
toplevel
D0:pmos.sw4
toplevel
D0:pmos.sw5
toplevel
i(mn)
i(mp)
i(vdd)
i(vds)
i(vgate)
v(0)
v(vd)
v(vdd)
v(vg)
i(mn) pmos
i(mp) pmos
v(vg) pmos
volt (lin)
Filter
V I All
waveview 1
0%


Custom WaveView Version D-2010.06 Copyright 2000-2010 Synopsys, Inc. Expiration date : 31-dec-2028
File WaveView Panel Axes Tools Config Help
Output View
D0:pmos.sw1
toplevel
D0:pmos.sw2
toplevel
D0:pmos.sw3
toplevel
D0:pmos.sw4
toplevel
D0:pmos.sw5
toplevel
i(mn)
i(mp)
i(vdd)
i(vds)
i(vgate)
v(0)
v(vd)
v(vdd)
v(vg)
i(mn) pmos
i(mp) pmos
v(vg) pmos
volt (lin)
Filter
V I All
waveview 1
0%

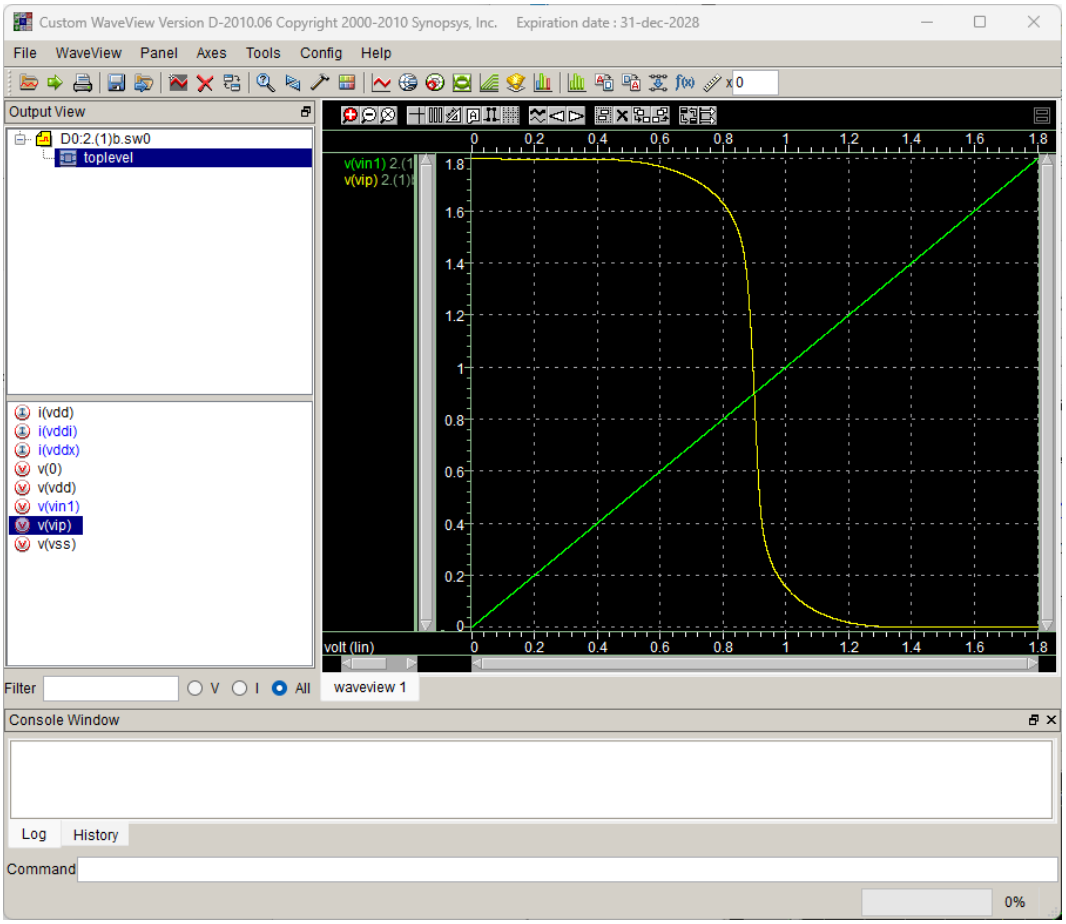

Custom WaveView Version D-2010.06 Copyright 2000-2010 Synopsys, Inc. Expiration date : 31-dec-2028
File WaveView Panel Axes Tools Config Help
Output View
D0:pmos.sw1
toplevel
D0:pmos.sw2
toplevel
D0:pmos.sw3
toplevel
D0:pmos.sw4
toplevel
D0:pmos.sw5
toplevel
i(mn)
i(mp)
i(vdd)
i(vds)
i(vgate)
v(0)
v(vd)
v(vdd)
v(vg)
i(mn) pmos
i(mp) pmos
v(vg) pmos
volt (lin)
Filter
V I All
waveview 1
0%

1.

1) M1 vip vin1 vss vss n_18 W=0.29u L=430.00n m=1
M2 vip vin1 vdd vdd p_18 W=0.29u L=196.00n m=2
ix1= 2.0019E-05
ix2= -1.9967E-05

$$(\frac{W}{L})_n = 0.67442$$

$$(\frac{W}{L})_p = 1.47959$$



M1 vip vin1 vss vss n_18 W=0.29u L=980.00n m=1

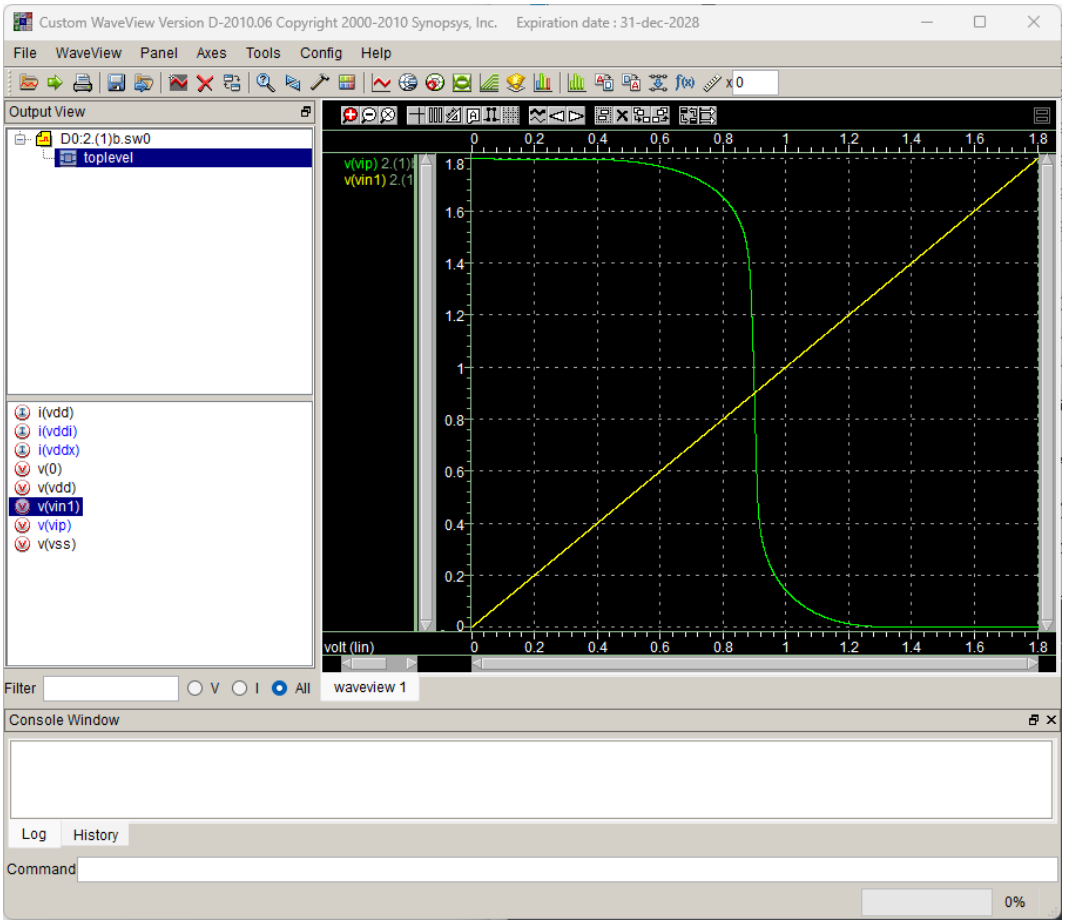
M2 vip vin1 vdd vdd p_18 W=0.29u L=302.00n m=2

ix1= 1.0005E-05

ix2= -1.0021E-05

$$(\frac{W}{L})_n = 0.29592$$

$$(\frac{W}{L})_p = 0.96026$$



M1 vip vin1 vss vss n_18 W=0.49u L=430.00n m=1

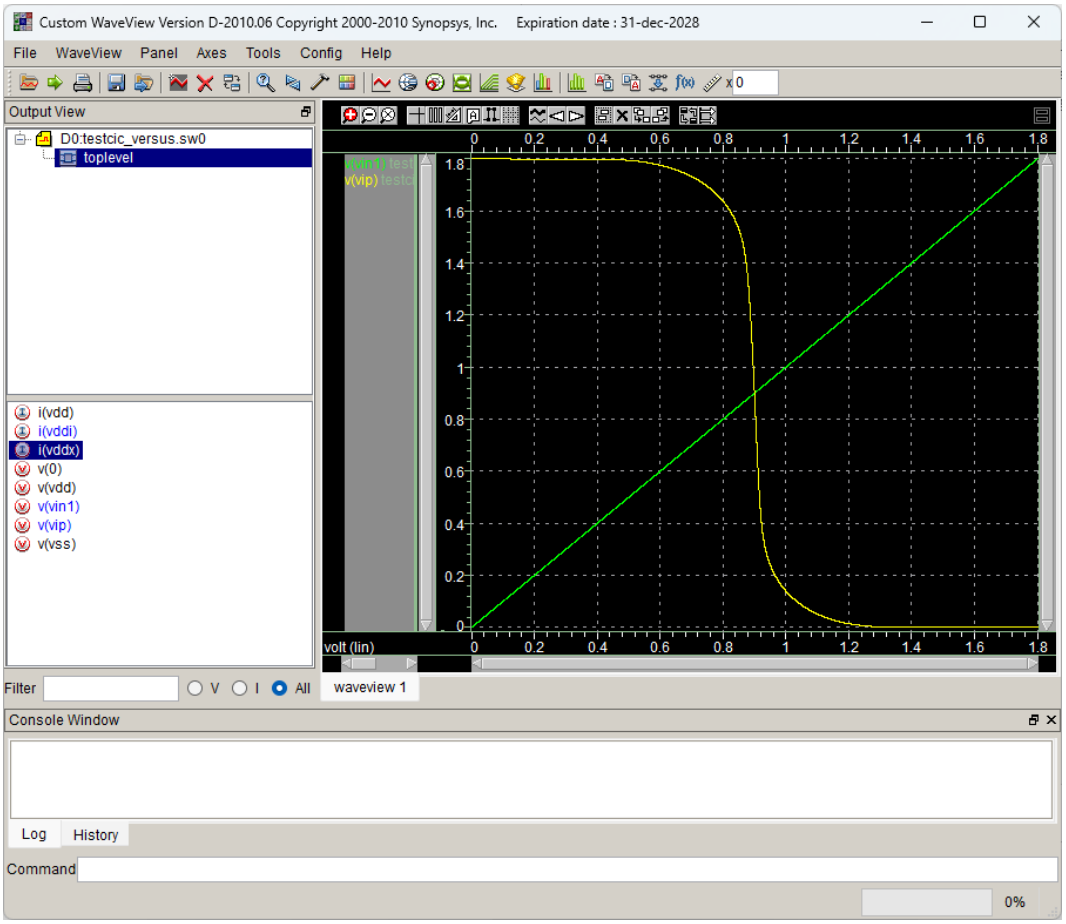
M2 vip vin1 vdd vdd p_18 W=0.45u L=196.00n m=2

ix1= 2.9864E-05

ix2= -2.9959E-05

$$(\frac{W}{L})_n = 1.13953$$

$$(\frac{W}{L})_p = 2.29592$$



(To analyze the output response, we need to sweep the input voltage. Therefore, we set vddi (input) as 0 at first, then sweep it after we define vin1 explicitly.)

設計步驟: 會是先調整 pmos, nmos 的 W,L 來讓 Io 符合預期，再將調整完成的規格帶入 sweep Vin。可以觀察到 Vo 隨著 Vi sweep 在不同的 Io 沒有明顯的差別，Vo, Vi 都會在 sweep 到 0.9V 的時候相交。

2) vdi vin1 gnd 0.7

M1 vip vin1 vss vss n_18 W=0.49u L=231.00n m=1

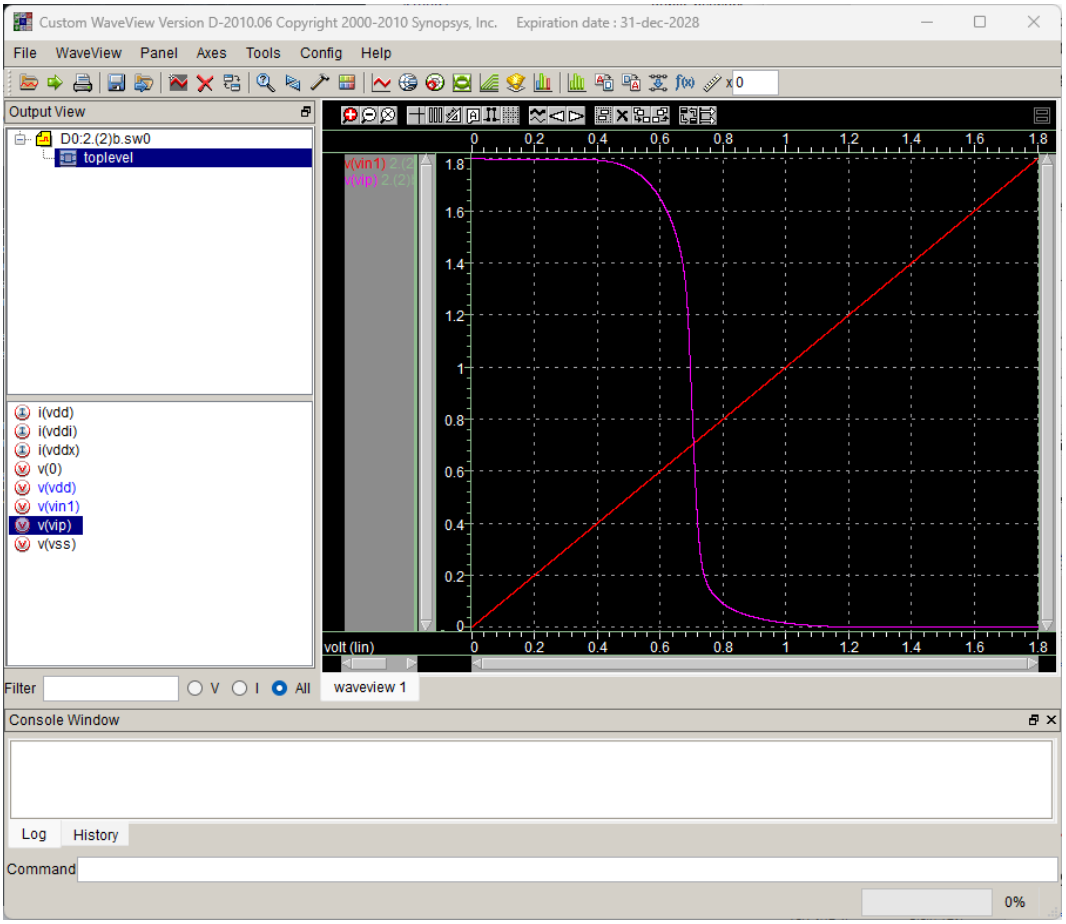
M2 vip vin1 vdd vdd p_18 W=0.49u L=480.00n m=2

ix1= 2.0015E-05

ix2= -1.9982E-05

$$(\frac{W}{L})_n = 0.48125$$

$$(\frac{W}{L})_p = 1.02083$$



vdi vin1 gnd 0.8

M1 vip vin1 vss vss n_18 W=0.49u L=409.00n m=1

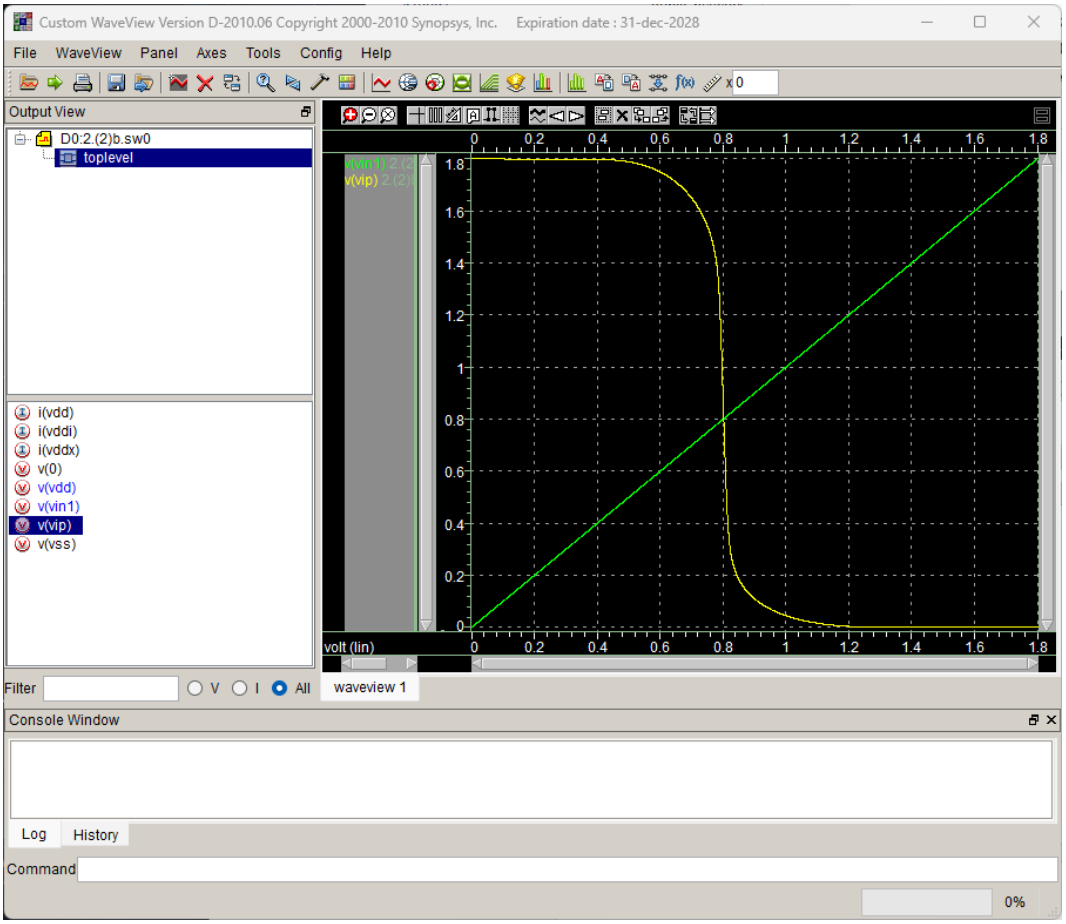
M2 vip vin1 vdd vdd p_18 W=0.49u L=353.00n m=2

ix1= 1.9974E-05

ix2= -1.9974E-05

$$(\frac{W}{L})_n = 1.19804$$

$$(\frac{W}{L})_p = 1.35977$$



vdi vin1 gnd 0.9

M1 vip vin1 vss vss n_18 W=0.29u L=430.00n m=1

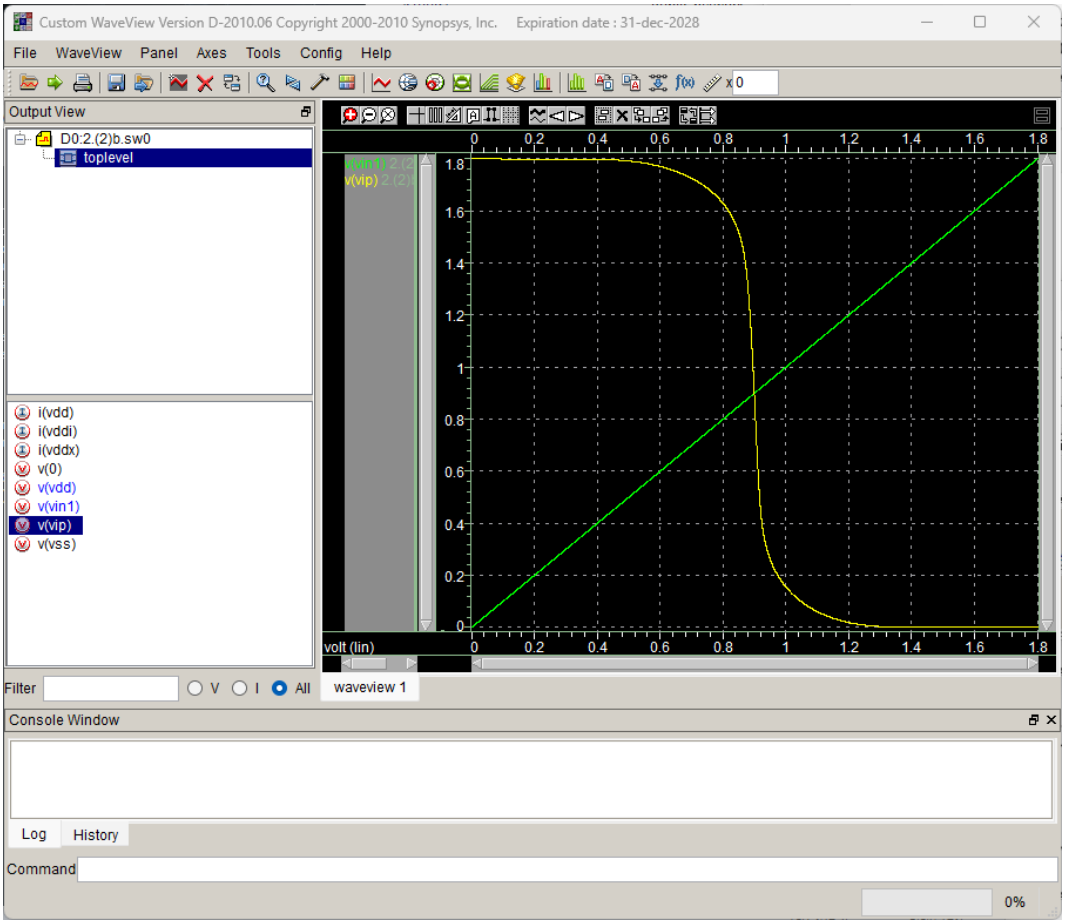
M2 vip vin1 vdd vdd p_18 W=0.29u L=196.00n m=2

ix1= 2.0019E-05

ix2= -1.9967E-05

$$(\frac{W}{L})_n = 0.67442$$

$$(\frac{W}{L})_p = 1.47959$$



vdi vin1 gnd 1.0

M1 vip vin1 vss vss n_18 W=0.49u L=1095.00n m=1

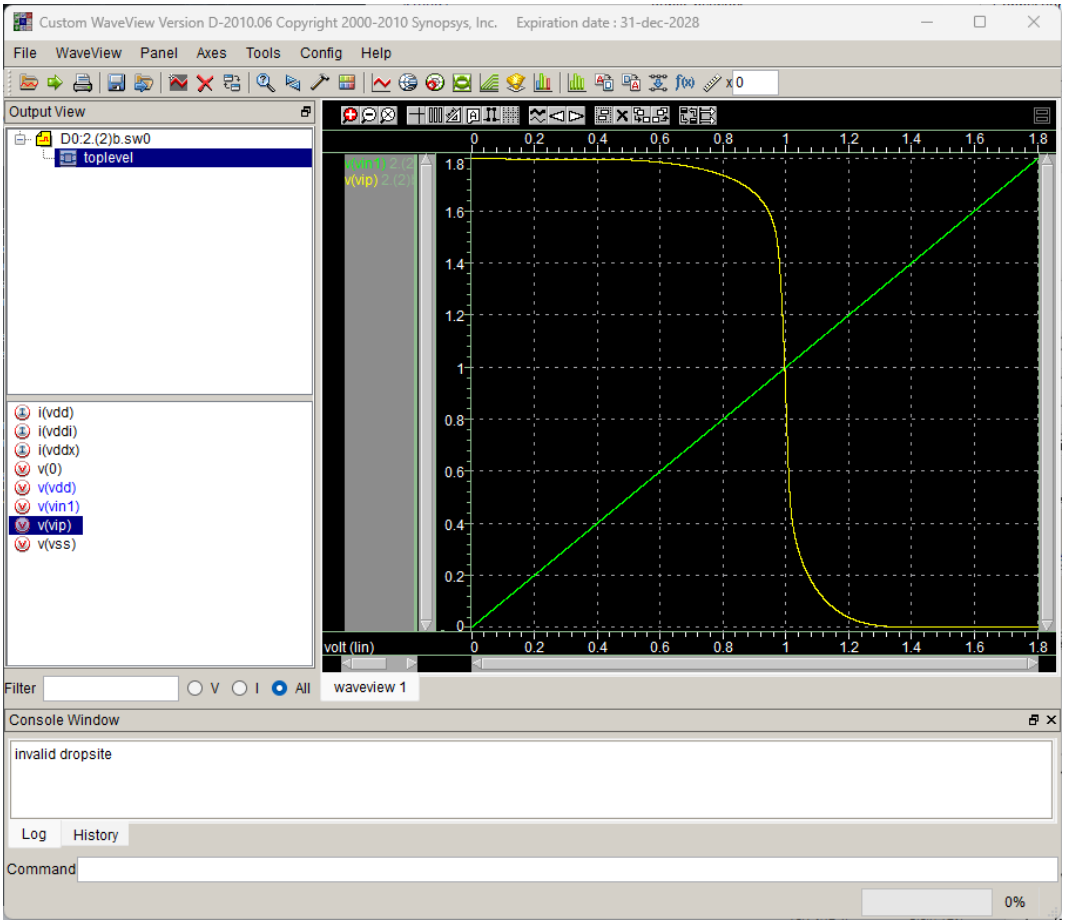
M2 vip vin1 vdd vdd p_18 W=0.49u L=195.00n m=2

ix1= 1.9993E-05

ix2= -1.9938E-05

$$(\frac{W}{L})_n = 0.67442$$

$$(\frac{W}{L})_p = 1.47959$$



vdi vin1 gnd 1.1

M1 vip vin1 vss vss n_18 W=0.49u L=1519.00n m=1

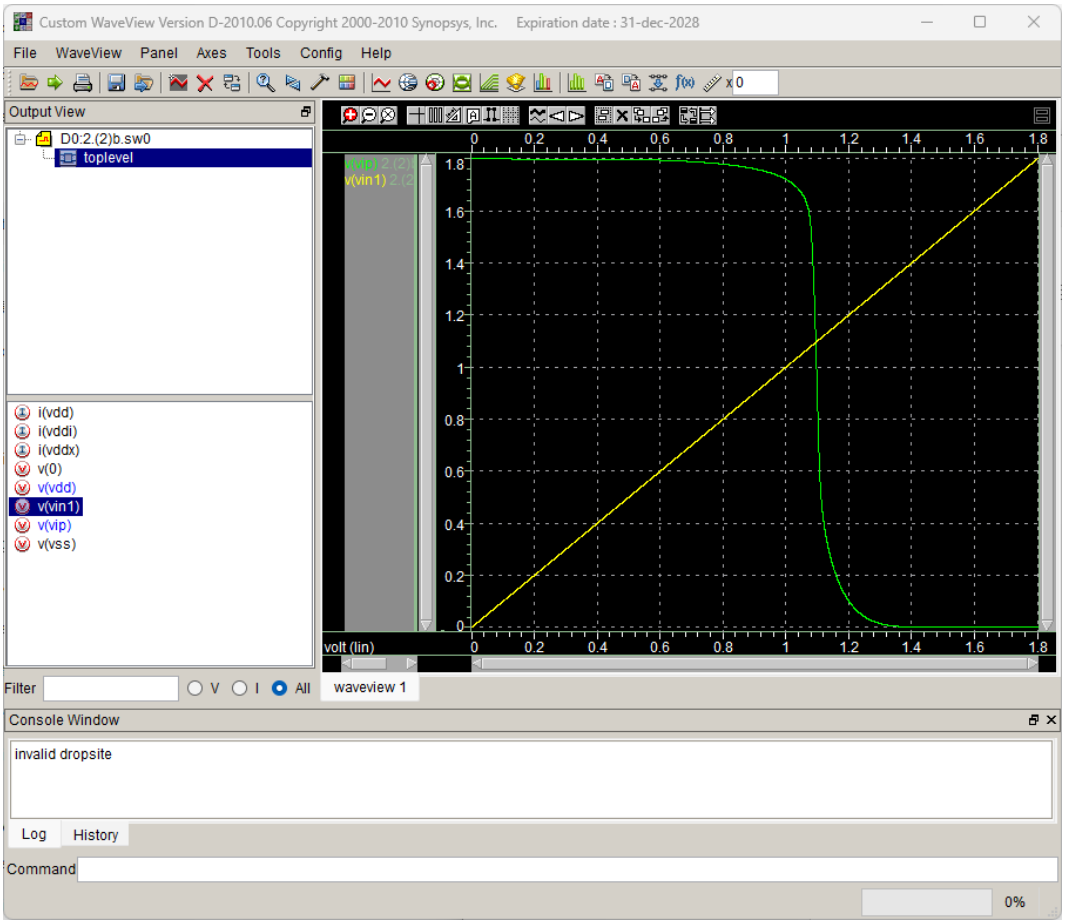
M2 vip vin1 vdd vdd p_18 W=1.19u L=199.80n m=2

ix1= 1.9997E-05

ix2= -2.0010E-05

$$(\frac{W}{L})_n = 0.32258$$

$$(\frac{W}{L})_p = 5.95596$$



(To analyze the output response, we need to sweep the input voltage. Therefore, we set vddi (input) as 0 at first, then sweep it after we define vin1 explicitly.)

設計步驟: 會是先調整 pmos, nmos 的 W,L 來讓 Io 符合預期，再將調整完成的規格帶入 sweep Vin。

隨著 Vi 的變化設計出來的 cmos sweep Vi 所產生的 output (vip)曲線，會和 Vi 相交於原本第 a 小題 cmos 所規定的 Vi。