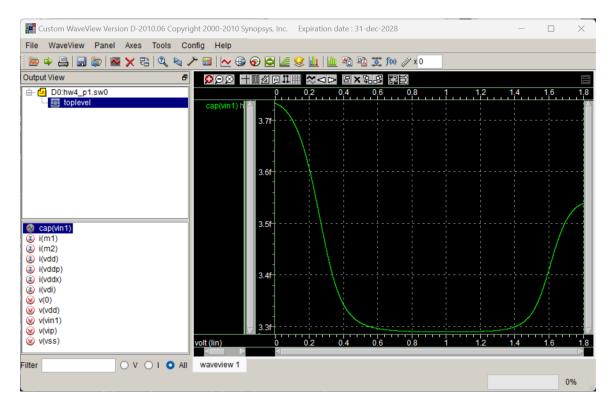
Introduction to VLSI Design HW4

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1.

```
◀ ► HW4_P1.sp
     ******Inverter Design***
     .temp 27
     .option list node post
     .lib "cic018.l" tt
      .unprotect
      .option captab=1
      .option dccap=1
     vdd vdd gnd 1.8
     vddx vss gnd 0
     vddp vip gnd 0.9
     vdi vin1 gnd 0.9
           vip vin1 vss vss n_18 W=0.29u
vip vin1 vdd vdd p_18 W=0.29u
     M1
                                                                  L=977.00n m=1
     M2
                                                                L=303.00n m=2
      ********************
     ******************
     .dc vddp 0 1.8v 0.0001
     .probe dc i(M2) i(M1)
.meas dc ix1 find i(M1) at = 0.9
      .meas dc ix2 find i(M2) at = 0.9
    .meas dc cp find cap(vin1) at=0.9
     .end
*** mosfet element parameters
name rd eff rs eff cdsat cssat vto
7.17 7.17 1.3e-16 1.3e-16 534.23m 140.84u 3.59 3.59 1.6e-16 1.6e-16 -446.36m 752.46u
 ****** dc transfer curves thom= 25.000 temp= 27.000 ***** ixl= 1.0002E-05 ix2= -1.0005E-05 cp= 3.2897E-15
      ***** job concluded
```



Three inverter add with a 16*cp capacitance:

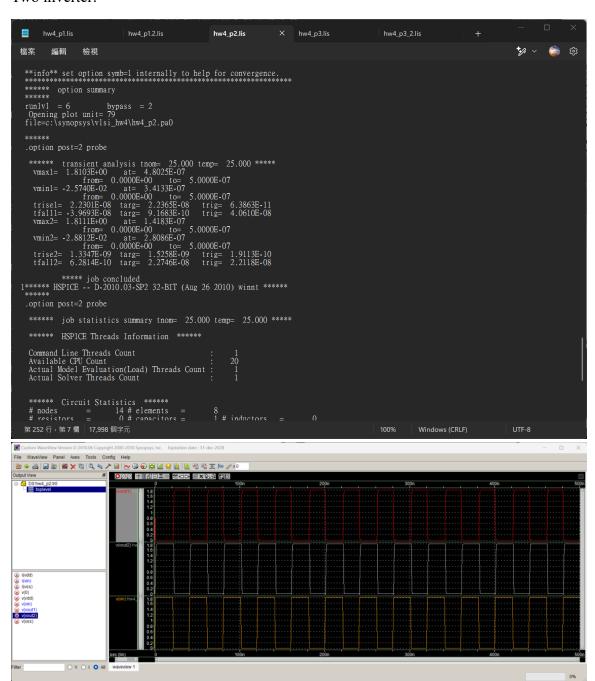
```
C:\synopsys\VLSI_hw4\HW4_P1.2.sp - Sublime Text (UNREGISTERED)
File Edit Selection Find View Goto Tools Project Preferences Help
                        HW4_P1.2.sp
       .option post=2 probe
       .lib "cic018.1" tt
      Vdd vdd 0 1.8
       Vss vss 0 0
      Vin vin 0 PULSE(0 1.8 On 0.5ns 0.5ns 50ns 100ns)
       .param Cp=3.2897E-15
       .param g=4
       .subckt inverter in out vdd vss Wp=0.29u Lp=303n Wn=0.29u Ln=977n
      M1 out in vdd vdd p_18 W=Wp L=Lp
M2 out in vss vss n_18 W=Wn L=Ln
       .ends inverter
      Xinv1 vin vout1 vdd vss inverter Wp=0.29u Lp=303n Wn=0.29u Ln=977n
      Xinv2 vout1 vout2 vdd vss inverter Wp=1.16u Lp=303n Wn=1.16u Ln=977n
      Xinv3 vout2 vout3 vdd vss inverter Wp=4.64u Lp=303n Wn=4.64u Ln=977n
      Cl vout3 0 5.2635E-14
       .tran 0.01ns 500ns
       .probe v(*)
       .end
```



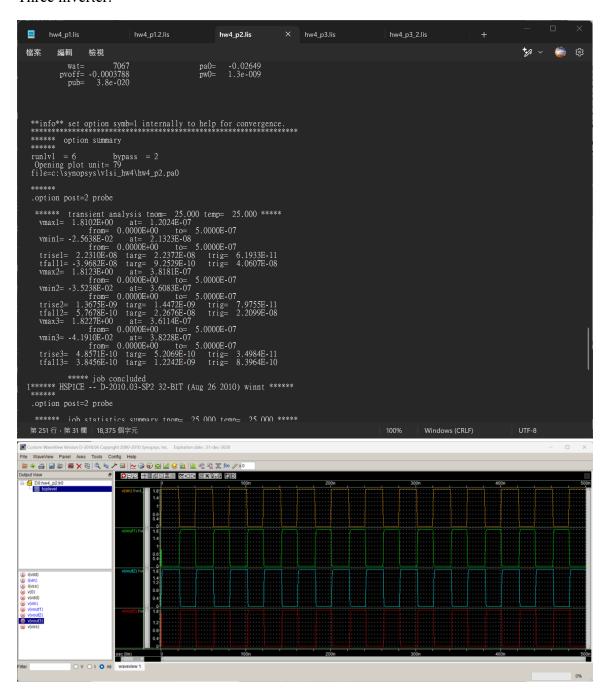
2.

One inverter:

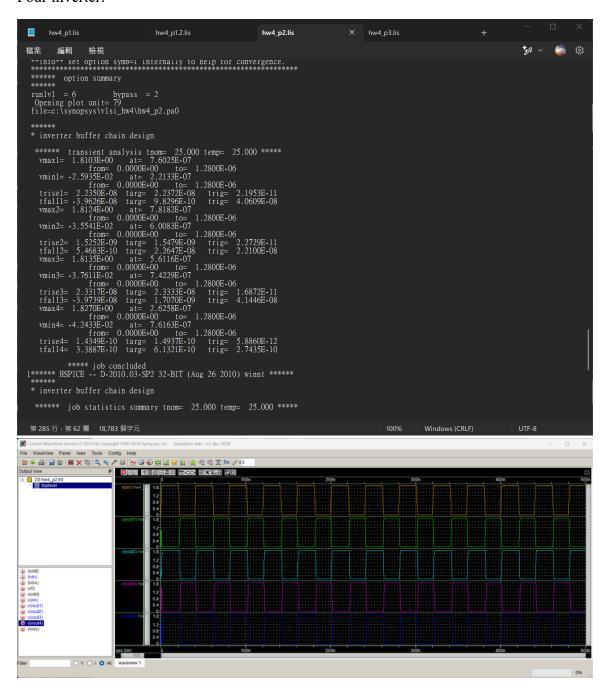
Two inverter:



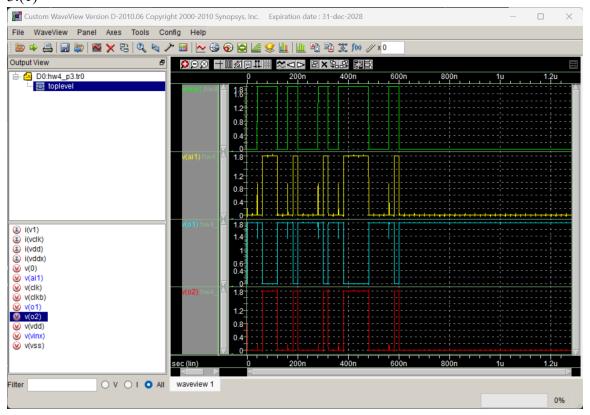
Three inverter:



Four inverter:



3.(1)



(2)

For others I for example:
$$\overline{A}$$
 \overline{b} $\overline{$

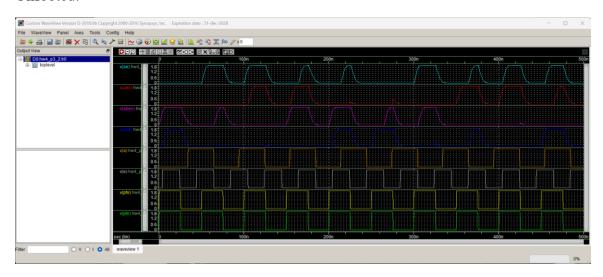
波形設定:

Vphi phi 0 PULSE(0 1.8 0n 0.5ns 0.5ns 25ns 50ns)

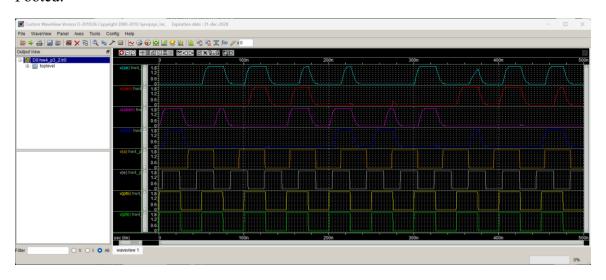
VA A 0 PULSE(0 1.8 34ns 0.5ns 0.5ns 30ns 60ns)

VE E 0 PULSE(0 1.8 4ns 0.5ns 0.5ns 20ns 40ns)

Unfooted:



Footed:



ae:AE

abe: $\bar{A}E$

aen: $A\bar{E}$

aben: $\bar{A}\bar{E}$