Sean William **Carroll**

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Skills

Programming	Modern C++, Python, Rust, SystemVerilog/UVM, Haskell
Tools	git, cmake, gdb, valgrind, svn, vcs, dve, verdi, bazel, perforce
Deep Learning Frameworks	TensorFlow, PyTorch
Python Libraries	pandas, numpy, duckdb, dash, dask, PyQt

Experience

AMD | Aug. 2022 - Present

Boxborough, MA

MTS Silicon Design Engineer

- Leading case studies using variety of proprietary models at different levels of abstraction to balance the needs for rapid prototyping as well as accurately predicting bottlenecks and architectural inefficiencies, models written in C++11 and Python3
- Creating lightweight and flexible data collection library to enhance ability to quickly collect and collate data simulations using modern C++11 and Rust
- Building coprocessor module for proprietary performance modeling simulator in C++11 while extending and refactoring existing modules for greater reuse and reduction of technical debt
- Synthesizing and interpreting performance data for case study presentations to designers to forecast next generation of coprocessors using pandas, duckdb, and plotly Python libraries
- Two papers accepted to internal conference concerning increasing efficiency and efficacy of methods used in performance modeling

Redpoint Positioning Corporation | Jan. 2022 - Aug. 2022

Boston, MA

Algorithm Engineer

- Reduced time to RTLS (Real-Time Location System) deployments through creation of newly designed GUI tool written in Python and leveraging pandas, numpy, and PyQt libraries
- Visualized the health of our RTLS deployments through development of a data-driven dashboard written in Python and leveraging pandas, numpy, dask, and dash libraries
- Introduced automation and testing methodologies to reduce technical debt with the creation of a CI flow for three projects, including linting and testing stages

Apple | Aug. 2021 - Jan. 2022

Cambridge, MA

Design Verification Engineer for Analog/Mixed Signal Group

- Verified firmware-based component using SystemVerilog Assertions

Lightelligence | Nov. 2019 - Aug. 2021

Boston, MA

Computer Architect | Mar. 2020 - Aug. 2021

- Wrote a proprietary microarchitectural simulator in modern C++ using event-driven and OO programming paradigms with a Python front end
- Co-designed the final microarchitecture using a novel photonic network-on-chip of a linear algebra accelerator for ML workloads

Design Verification Engineer | Nov. 2019 - Mar. 2020

- Promoted efficiency through increased abstraction and automation by writing an extensible Python framework to generate RTL, DV, and C-based driver collateral from industry standard SystemRDL

Marvell Semiconductor (formerly Cavium) | Sep. 2017 - Nov. 2019

Marlborough, MA

Design Verification Engineer

- Executed block level verification of the virtual resource manager coprocessor with the focus on the scoreboard in SystemVerilog/UVM
- Verified integration and function of distributed support-blocks in all SOC coprocessors at the full chip level by co-writing a simple OS framework and associated test suite in C and SystemVerilog

Education

Georgia Institute of Technology

Atlanta, GA

M.S. in Computer Science

Jan. 2018 - May 2021

- Cum. GPA: 4.0
- Machine Learning Specialization

Cornell University

Ithaca, NY

B.S. in Computer Science, Electrical and Computer Engineering

Aug. 2013 - May 2017

- Cum. GPA: 3.871 - *Magna Cum Laude*
- Vector Completed in Systems/Databases (OS Track)