ZHENGRONG WANG

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EDUCATION

University of California, Los Angeles, *Department of Computer Science* — Los Angeles, U.S.
Ph.D. in Computer Science — *Aug. 2018 - Jul. 2024* (Expected)

University of California, Los Angeles, *Department of Computer Science* — Los Angeles, U.S.
Master of Science in Computer Science — *Sep. 2016 - Jul. 2018*

Tsinghua University, *Department of Electronic Engineering* — Beijing, P.R. China
Bachlor of Engineering in Electronic Engineering, GPA: 91/100 — *Aug. 2012 - Jul. 2016*

ETH Zürich, *Department of Information Technology* — Zürich, Switzerland
Exchange Student, International Academic Program, GPA: 5.50/ 6.00 — *Sept. 2014 - Feb. 2015*

PUBLICATION

Z. Wang, C. Liu, A. Arora, L. John, T. Nowatzki.
Infinity Stream: Portable and Programmer-Friendly In-/Near-Memory Fusion. *ASPLOS '23*, Vancouver, Canada.

Z. Wang, J. Weng, S. Liu, T. Nowatzki.
Near-Stream Computing: General and Transparent Near-Cache Acceleration. *HPCA '22*, Seoul, South Koera.

Best Paper Runner-Up: Z. Wang, J. Weng, J. Lowe-Power, J. Gaur, T. Nowatzki.
Stream Floating: Enabling Proactive and Decentralized Cache Optimizations. *HPCA '21*, Seoul, South Koera.

Z. Wang, T. Nowatzki.
Stream-Based Memory Access Specialization for General Purpose Processors. *ISCA '19*, Phoenix, USA.

Z. Wang, C. Liu, T. Nowatzki.
Infinity Stream: Enabling Transparent and Automated In-Memory Computing. *IEEE CAL, vol. 21, 2022*.

IEEE Micro Top Picks Honorable Mention: J. Weng*, S. Liu*, V. Dadu, **Z. Wang**, P. Shah, T. Nowatzki.
DSAGEN: Synthesizing Programmable Spatial Accelerators. *ISCA '20*, virtual.

J. Weng*, S. Liu*, D. Kupsh, A. Sohrabizadeh, **Z. Wang**, et al.
OverGen: Improving FPGA Usability through Domain-specific Overlay Generation. *MICRO '22*, Chicago, USA.

J. Weng, S. Liu, **Z. Wang**, V. Dadu, T. Nowatzki.
A Hybrid Systolic-Dataflow Architecture for Inductive Matrix Algorithms. *HPCA '20*, San Diego, USA.

J. Lowe-Power, ..., **Z. Wang**, et al.
The gem5 Simulator: Version 20.0+. *arXiv:2007.03152v2*.

Z. Wang, F. Qiao, Z. Liu, Y. Shan, X. Zhou, L. Luo, and H. Zhong.
Optimizing Convolutional Neural Network on FPGA under Heterogeneous Computing Framework with OpenCL. *TENCON '16*.

AWARDS AND HONORS

IEEE HPCA 2021 Best Paper Runner-Up (Stream Floating, in *HPCA '21*), *IEEE* — *Feb. 2021*
IEEE Micro Top Picks 2020 Honorable Mention (DSAGEN, in *ISCA '20*), *IEEE* — *Jan. 2021*
2021 Dongguan Entrepreneur Scholarship, *Dongguan Entrepreneurs Federation* — *Nov. 2021*
Second-class Scholarship for Excellent Freshmen, *Tsinghua University* — *Oct. 2012*
Wang Zhaosheng Scholarship for Excellent Studeng from Dongguan, *Wang Zhaosheng Fundation* — *Oct. 2012*
Second Prize in 30^{th} Chinese National Physics Contest (Non-Physical Group A) — *Dec. 2013*
Ranked No.5 in National Matriculation Test(Science), Guangdong Province (5/600,000) — *Jun. 2012*

SELECTED PROJECTS & INTERNSHIPS

GemForge Framework — *Jan. 2018 - Present*

- Research project of full-stack trace-based simulation for stream-specialized systems.
- Implement LLVM passes to recognize streams and transform program with new stream instructions.
- End-to-End execution-based simulation in gem5.
- Results published in ISCA' 19, HPCA' 21, HPCA '22 and ASPLOS '23. More in submission.
- Repo: https://github.com/PolyArch/gem-forge-framework

Gem5-AVX *Jan. 2019 - Present*

- Add AVX-512 support to gem5 simulator, extensively used in research.
- Faithfully model the microarchiecture of vectorized instructions, including microops.
- Detailed tutorials on how to support new instructions.
- Repo: https://github.com/seanzw/gem5-avx

OpenCL@FPGA (Undergraduate Thesis) *Sep. 2015 - Jun. 2016*

- Supervised by Assoc. Prof. Fei Qiao, Tsinghua University
- Use OpenCL to implement CNN on Xilinx Alpha Data FPGA, and accelerate with pipeline.
- Paper on TENCON 16: Optimizing Convolutional Neural Network on FPGA under Heterogeneous Computing Framework with OpenCL

MicroPython on FPGA, Dept. EEE, Imperial College London *Jul. 2015 - Aug. 2015*

- Supervised by Prof. Peter Y. K. Cheung, Head of Dept. EEE.
- Port MicroPython on Altera DE0-Nano-SoC FPGA.
- Build FFT example with DMA.
- Repo: https://github.com/seanzw/MicroPythonFPGA

Software Engineering Internship, Facebook, Menlo Park *Jun. 2017 - Sep. 2017*

- Work in the infrasturcture team to build an offline back test system.
- Reprocess all Ads classficiation streams to detect any regression.

Professional & Personal Skills

Mathematic: Familiar with calculus, linear algebra, probability theory, discrete mathematics, algorithms.

Computer Capability: Skilled at C/C++, Python, MATLAB.

Language Proficiency: English: Toefl 114; German: B1 Level(MCER).

Experience

Courses in CS

- Compilers by Alex Aiken, Stanford University
- Operating System Engineering, MIT
- Programming Languages by Dan Grossman, University of Washington
- Machine Learning by Andrew Ng, Stanford University
- Algorithms Part I & II by Robert Sedgewick, Princeton University
- Introduction to Computer Science and Programming, MIT
- Introduction to Probability, MIT
- Advanced Computer Graphics, Tsinghua University
- Computer Networks, Tsinghua University
- Software Engineering, Tsinghua University
- Computer Graphics (5.25/6), ETH Zurich
- Computer Vision (5.5/6), ETH Zurich

Children Education Program Volunteer, *Dream a Dream, Bangalore, India* *Jul. 2013 - Sept. 2013*