

# Predictable Virtualization on Memory Protection Unit-based Microcontrollers

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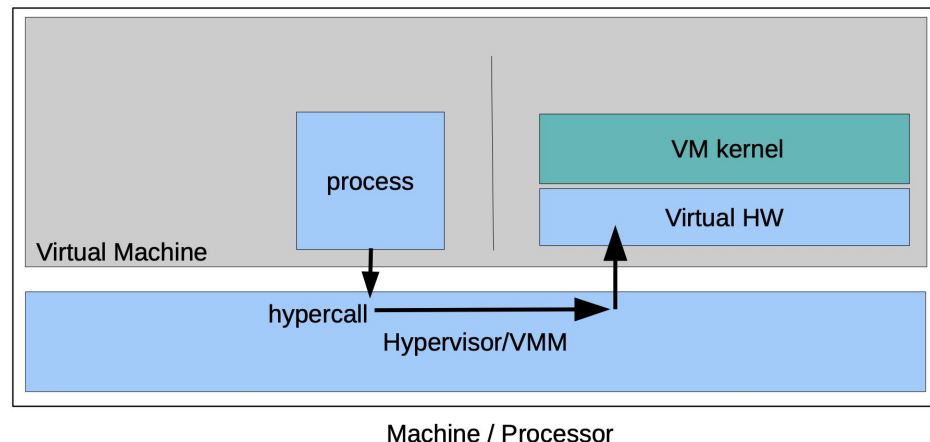
Presented by: Sam Frey

# Virtualization

...is the process of running a virtual instance of a computer system in a layer abstracted from the actual hardware.

Each virtual instance *thinks* that it has complete control over a resource.

This is largely due to address space virtualization.

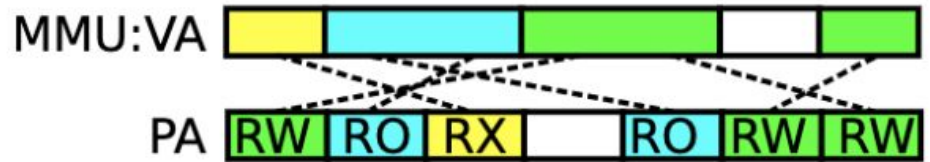


# Memory Management Unit

...is what actually provides address virtualization by translating an instance's virtual addresses into physical memory addresses.

Virtual addresses can be mapped anywhere in physical memory, **and they don't need to be contiguous.**

Translating virtual addresses is expensive.



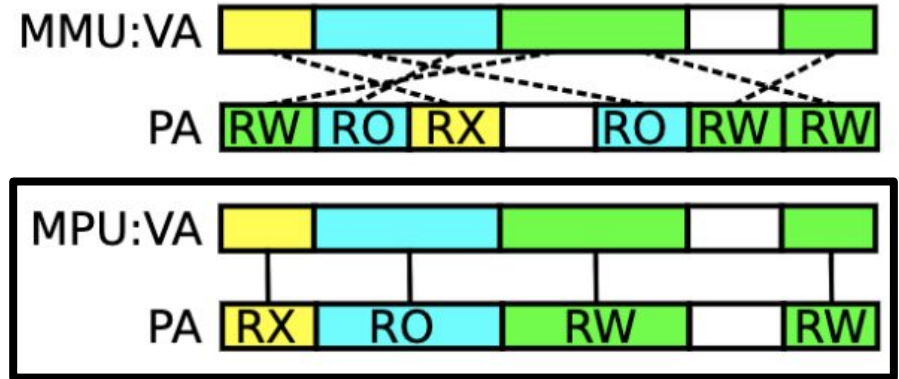
# Memory Protection Unit

...provides protection over a region of memory with a given size and starting address.

With a MPU, the OS must run with a single address space (SASOS), and **regions must be mapped contiguously**.

MPUs require a static allocation of memory.

MPUs can only protect a limited number of regions.



# The Problem

SASOS leave much to be desired when it comes to security and reliability.

Can isolation of each RTOS on the system be achieved using virtualization within the constraints of an MPU?

Can virtualization be achieved with a low enough cost to make the increased overhead worthwhile?

# The Solution

- Pre-planned static memory layout
- Capability-based memory access protections
- Virtualize microcontroller hardware protections to provide multi-tenancy

This was accomplished using FreeRTOS for each VM and Composite OS as the virtual machine manager and host OS.

# Memory Layout

Meeting MPU constraints requires a static memory layout.

Initial algorithm attempts used Satisfiability Modulo Theory, but took too long.

A greedy heuristic was added to shorten runtime.

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## Algorithm 1: Memory Address Assignment Heuristic

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**Input:**  $C$ : Set of components,  $A$ : Set of SRAM arenas

```
1 while  $|\{c \in C \mid \text{num\_allocated\_regions}(c) > |\mathcal{R}| - 1\}| > 0$  do
2    $\text{collapsable} = \{c \in C \mid \exists a \in A \text{ is\_enabled}(a, c)\}$ 
3   if  $|\text{collapsable}| = 0$  then
4     return None
5    $c = \arg \max_{c \in \text{collapsable}} \text{num\_allocated\_regions}(c)$ 
6    $a_0 = \arg \max_{a \in \text{accessible\_enabled\_arenas}(c)} |\text{users}(a)|$ 
7    $\mathcal{O} = \text{accessible\_enabled\_arenas}(c) \setminus a_0$ 
8    $\text{partners} = \{a \in \mathcal{O} \mid \text{subregions}(a) + \text{subregions}(a_0) \leq S\}$ 
9   if  $|\text{partners}| = 0$  then
10     $\text{disable\_arena}(c, a_0)$ 
11    continue
12    $a_1 = \arg \max_{a \in \text{partners}} |\text{users}(a_0) \cap \text{users}(a)|$ 
13    $a_{\text{merged}} = \text{merge\_arenas}(a_0, a_1)$ 
14    $A = (A - \{a_0, a_1\}) \cup \{a_{\text{merged}}\}$ 
15    $\text{reenable\_all\_arenas}()$ 
16 end
17 return  $\text{assign\_addresses}(A)$ 
```

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# The Algorithm

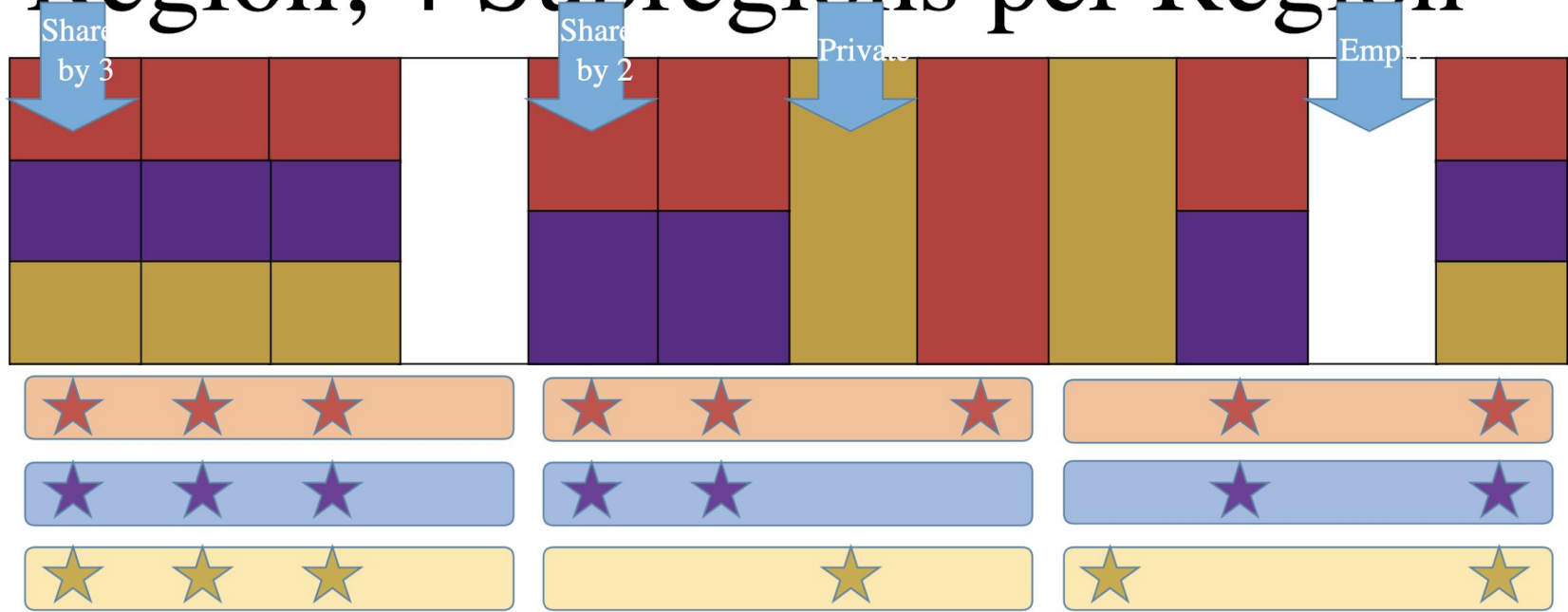
Goal: Use as few memory regions as possible.

➡ Maximize use within each region

➡ Move similar subregions into the same memory region.

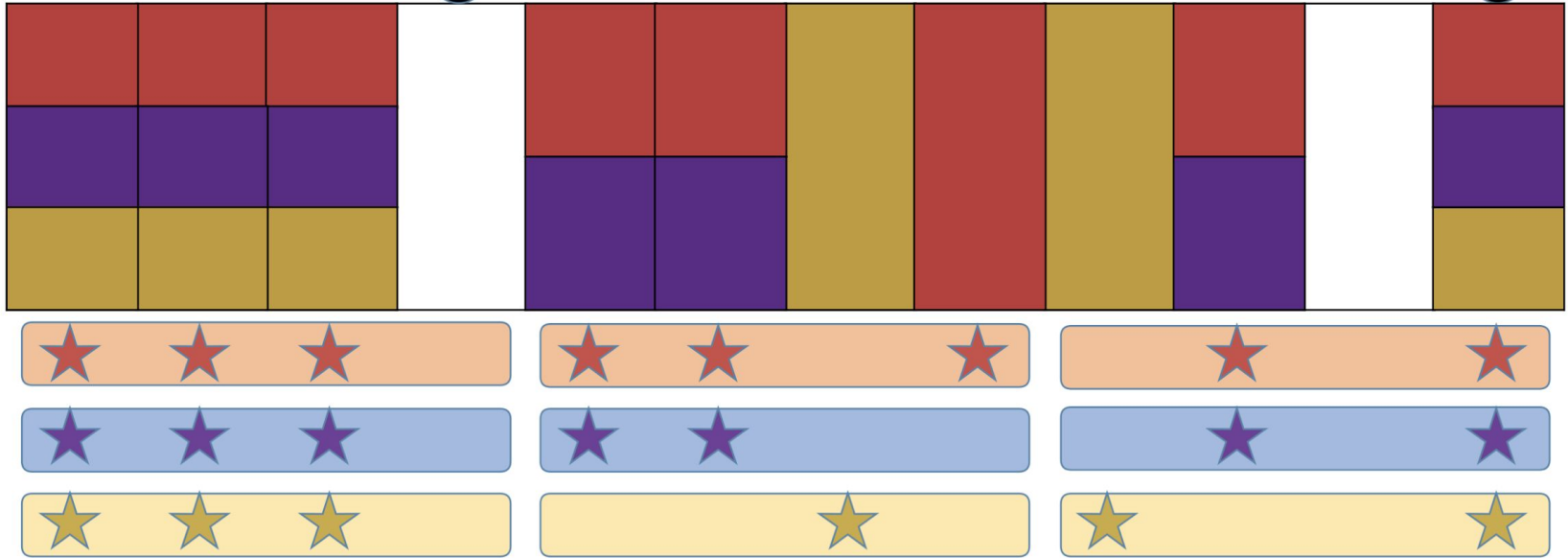


# 2 Region, 4 Subregions per Region



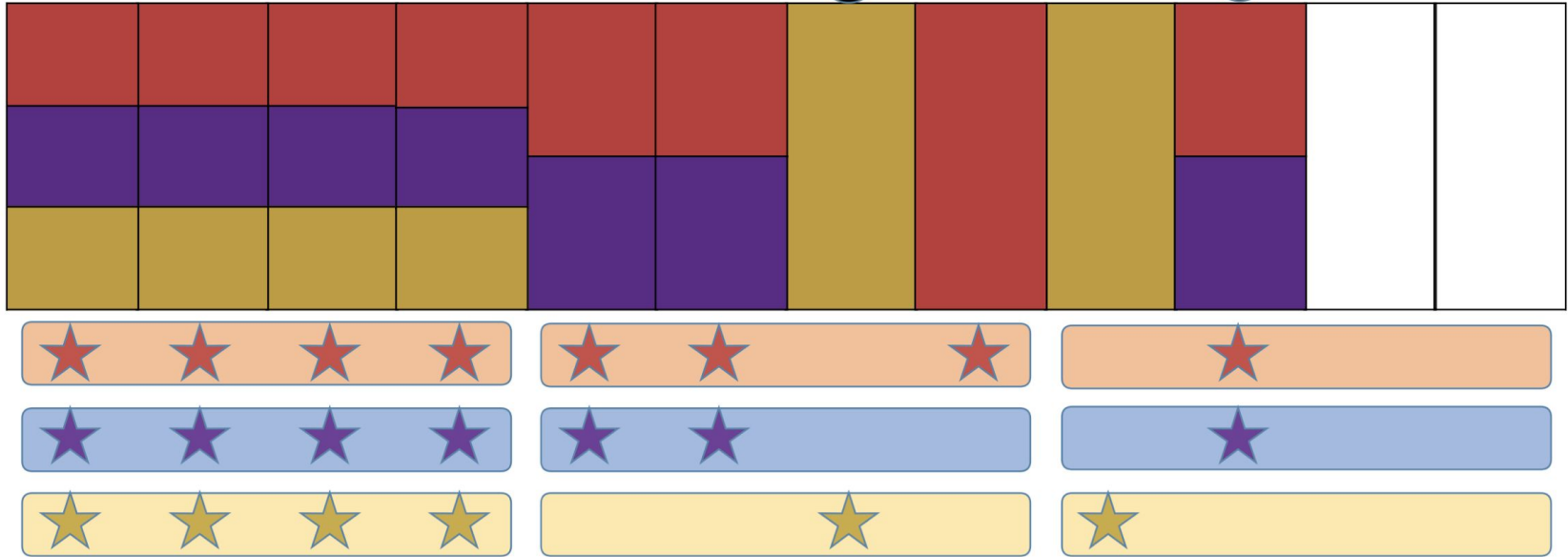
Requires 3 regions - Ran out of regions!

# 2 Region, 4 Subregions per Region



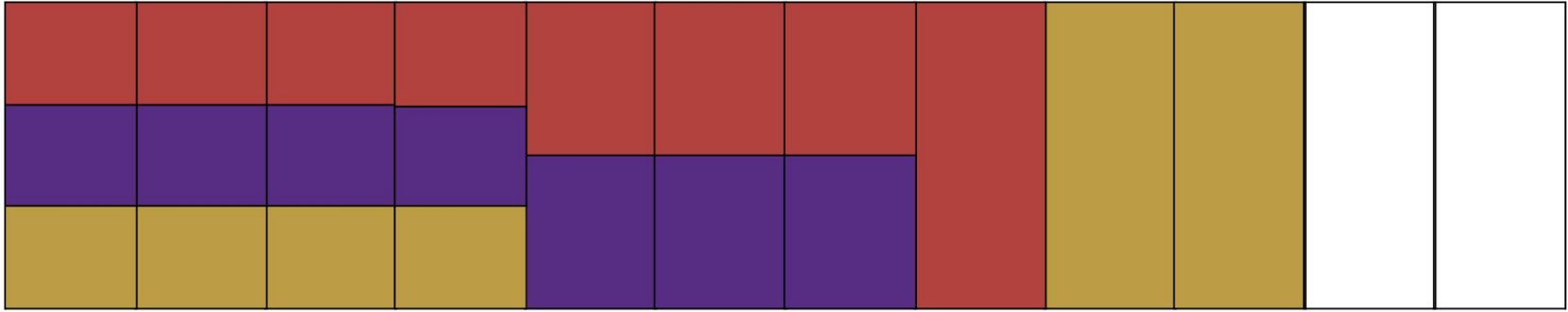
Requires 3 regions - Ran out of regions!

# 2 Region, 4 Subregions per Region



Requires 3 regions - Ran out of regions!

# 2 Region, 4 Subregions per Region



Requires 2 regions - Placement feasible!

# Memory Isolation

No MMU means no virtual addresses.

Security and access control are provided by **capabilities**, unforgeable tokens that reference system resources.

They refer to a value that references an object along with an associated set of access rights.

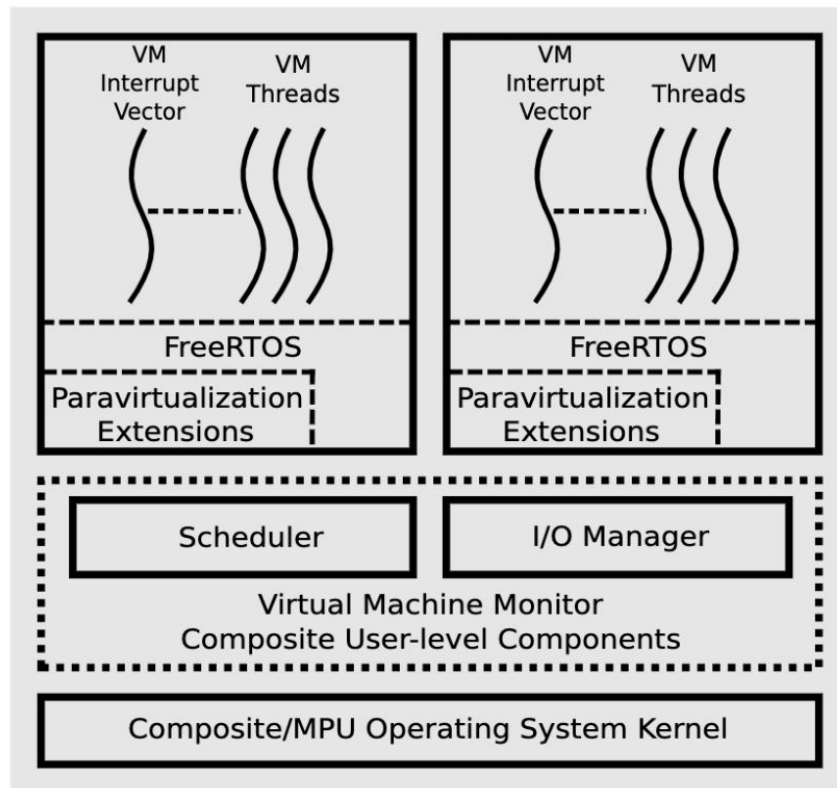
	Mem 1	Mem 2	Mem 3	Sensor	Actuator
VM 1	e	r/w		r	r/w
VM 2		r	e		r
VM 3		r/w	e	r	r/w

# Virtualization

The host OS and each VM all have their own scheduler.

VMs make device data requests through the I/O manager.

The I/O manager multiplexes the devices required by multiple VMs.

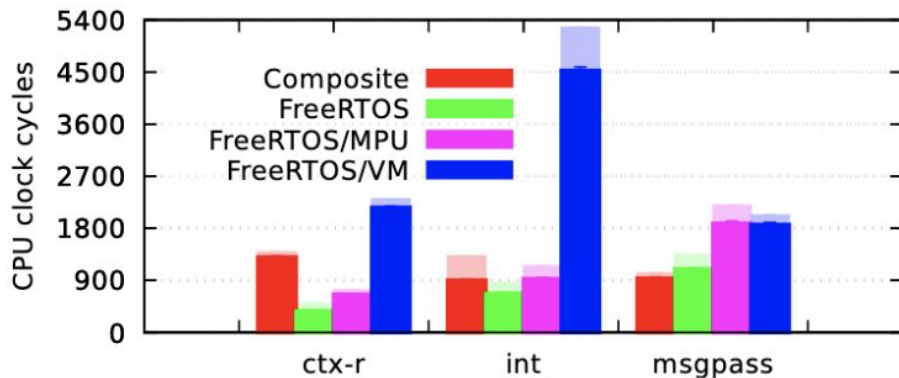


# Evaluation

Memory overhead was far higher than the average overhead for power-of-two allocations.

Overhead increased reasonably given the added isolation of each VM.

But what about interrupts?



# Critique

Can you multiplex an actuator?

Why is all of this necessary?

More specifically, why virtual machines?



# Discussion (from Github)

Where / Why does memory fragmentation occur?

Where is this applicable in the real world?

Why is it always necessary to switch back to a scheduler thread?