Computation II: embedded system design (5EIB0)

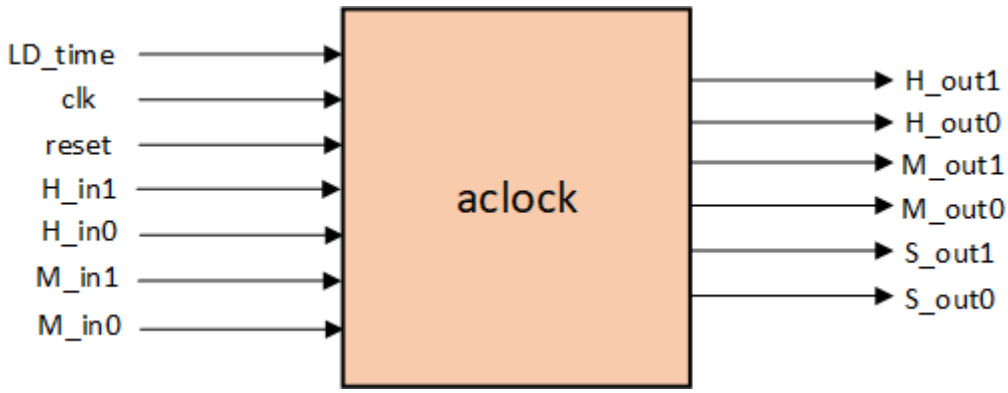
Description | Submission view

Part 2f: 2019-07-03 Design a Real Time Clock - 5pt

Due date: Wednesday, 3 July 2019, 9:05 PM
Requested files: clock.v (Download)
Type of work: Individual work

Introduction

In this exercise, you will create a verilog implementation of a **Real Time Clock (RTC)**. The top level block diagram of the RTC system is shown below:



As shown in the diagram above, the RTC system consists of a module named **aclock.** It consists of 7 input signals and 6 output signals. The functionality of the signals are explained below:

- **clk (1 bit) -** A 1Hz input clock. This signal is used to generate each real-time second.
- **LD_time (1 bit) -** If LD_time=1, the time should be set to the values on the inputs H_in1, H_in0, M_in1, a nd M_in0. The seconds time should be set to 0.If LD_time=0, the clock should act normally.
- **reset (1 bit) -** An active high synchronous reset. It resets the time of the clock to 00:00:00[HH:MM:SS]
- **H_in1 (2 bits) -** A 2-bit input used to set the most significant hour digit of the clock (if LD_time=1). Valid v alues are 0 to 2.
- **H_in0 (4 bits) -** A 4-bit input used to set the least significant hour digit of the clock (if LD_time=1). Valid v alues are 0 to 9.
- **M_in1 (4 bits) -** A 4-bit input used to set the most significant minute digit of the clock (if LD_time=1). Valid values are 0 to 5.
- **M_in0 (4 bits) -** A 4-bit input used to set the least significant minute digit of the clock (if LD_time=1). Valid values are 0 to 9.
- **H_out1 (2 bits) -** The most significant digit of the hour. Valid values are 0 to 2**.**
- **H_out0 (4 bits)** - The least significant digit of the hour. Valid values are 0 to 9.
- **M_out1 (4 bits)** - The most significant digit of the minute. Valid values are 0 to 5.
- **M_out0 (4 bits)** - The least significant digit of the minute. Valid values are 0 to 9.
- **S_out1 (4 bits) -** The most significant digit of the second. Valid values are 0 to 5.
- **S_out0 (4 bits)** - The least significant digit of the second. Valid values are 0 to 9.

Assignment

In this assignment, you have to write the module named **aclock** which will perform the functionality of a **Real-Time Clock (RTC)**. All output assignments should be synchronous with the **clk**.

Use the template given below for desiging the system:

```
`timescale 1ms / 1us
module aclock (
        input reset,
        input clk,
        input [1:0] H_in1,
        input [3:0] H_in0,
        input [3:0] M_in1,
        input [3:0] M_in0,
        input LD_time,
        output [1:0]  H_out1,
        output [3:0]  H_out0,
        output [3:0]  M_out1,
        output [3:0]  M_out0,
        output [3:0]  S_out1,
        output [3:0]  S_out0
 );
     <<Enter the Logic for Real Time Clock>>

endmodule
```

Debug

Click on the symbol marked below to see the waveforms produced by your design. Please note that if your code has an error that prevents it being simulated it will not produce any waveforms.

Run

Click on the symbol marked below to run your implemented design without waveforms. This option also gives debug messges on the console.

Note: After clicking on the run button, type **all** on the console to see the debug messages.

Requested files

clock.v

```
1   `timescale 1ms / 1us
2   module aclock (
3       input reset,
4       input clk,
5       input [1:0] H_in1,
6       input [3:0] H_in0,
7       input [3:0] M_in1,
8       input [3:0] M_in0,
9       input LD_time,
10      output [1:0]  H_out1,
11      output [3:0]  H_out0,
12      output [3:0]  M_out1,
13      output [3:0]  M_out0,
14      output [3:0]  S_out1,
15      output [3:0]  S_out0
16    );
17
18     //<<Enter the logic for Real time clock >>
19
20  endmodule
```

VPL

◄ Part 2e: 2019-07-03 Add Alarm Functionality to a Real Time Clock - 6pt EDITABLE

Part 2f: 2019-07-03 Design a Real Time Clock - 5pt EDITABLE ►

Return to: Re-exam 2019-07...