# Computation II: embedded system design (5EIB0)



**Available from**: Friday, 5 April 2024, 2:00 PM
**Requested files**: zero.v (Download)
**Type of work**: Individual work

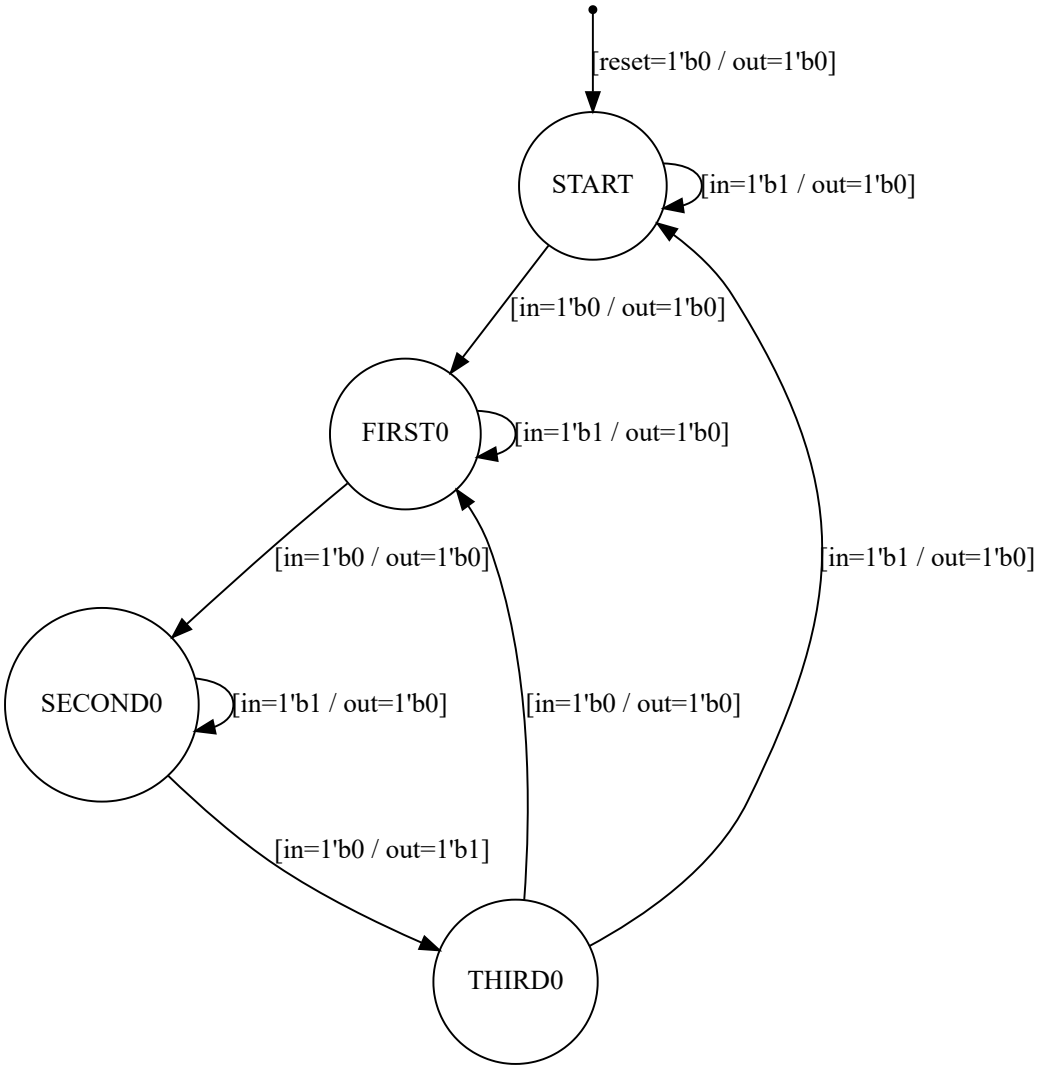
## Assignment

In this assignment, you will create a Verilog implementation of a Mealy Finite State Machine (FSM) which detects the accumulation of three zeroes.

Example input/output behavior:

```
in   :    0 0 1 0 1 1 0 1 1 1 0 1 0 ...
out  :    0 0 0 1 0 0 0 0 0 0 0 0 1 ...
```

The FSM has the following specifications. Including the clock (clk) and reset signals, the implemented FSM will have 3 input signals and 1 output signal.




The clk input signal is 1-bit wide, the reset input signal is 1-bit wide and the in input signal is 1-bit wide. The state elements of the FSM are to capture their inputs on the positive clock (clk) edge and reset their state when the synchronous reset signal is high. A reset can be asserted (synchronously) at any time causing all state elements to reset and hence a transtion to the initial state.

The out output signal is 1-bit wide. Initial values of the output signals upon reset are shown in the FSM diagram.

Your solution will be tested using bounded model checking against a golden reference implementation. The model checking software will stop at the earliest moment that your implementation diverges from the behaviour of the golden reference implementation. If a divergence takes place, a waveform will be created showing a trace of the module signals resulting in the divergent state. This waveform also shows the behaviour of the golden reference (REF) so that you can see what your implementation (DUT) should have done differently.

Please note that the golden reference implementation supersedes all other implementation descriptions. If the output from your solution implementation does not diverge from the golden reference implementation then your solution is marked as correct. Otherwise, your solution is incorrect and you should use the waveform that is produced to assist you to correct your implementation.

## Debug

Click on the symbol marked below to see the waveforms produced by your design. Please note that if your code has an error that prevents it being simulated it will not produce any waveforms.


VPL

You are logged in as Thomas Stirling Valdez (Log out)
5EIB0

Data retention summary