Computation II: embedded system design (5EIB0)

Part 2f - 2024-04-12 Implement UART Re-transmission Module (6pt)

Description Submission view

Grade

Reviewed on Monday, 15 April 2024, 4:02 PM by Automatic grade
Grade: 0.00 / 6.00

Assessment report [-]
[+]**Test 1: Meets Reference Specification**
[+]**Summary of tests**
Submitted on Friday, 12 April 2024, 4:29 PM (Download)

uart_retrans.v

```
module uart_retrans(
            input clk,
            input reset,
            input ack,
            input signal,
            output trigger,
            output valid,
            output error,
            output request_resend,
            output[4:0] resend_count);
    reg [4:0] out;


    timer timer_inst(
         .clk(clk),
         .reset(reset),
         .enable(1),
         .value(5'h8),
         .valid(valid),
         .count(count),
         .trigger(trigger));


    uart_retrans_fsm uart_retrans_fsm_inst(
         .clk(clk),
         .reset(reset),
         .ack(ack),
         .frame_valid(frame_valid),
         .parity_error(parity_error),
         .timeout(timeout),
         .error(error),
         .request_resend(request_resend),
         .valid(valid));


    uart_parity_even uart_parity_even_inst(
         .clk(clk),
         .reset(reset),
         .signal(signal),
         .error(error),
         .valid(valid));

    assign count = out;
    assign complete = ~(|out);

    assign MUX1 = (~complete & enable)?(out - 'd1):(out);
    assign MUX2 = (valid)?(value):(MUX1);
    assign out_next = (reset)?(5'h0):(MUX2);

    always @(posedge clk) begin
        out <= out_next;
    end
endmodule

```

uart_retrans_fsm.v

```
module uart_retrans_fsm(
            input clk,
            input reset,
            input ack,
            input ,
            input ,
            input ,
            output error,
            output request_resend,
            output valid);

    reg [2:0] state, state_next;
    parameter WAIT_ = 'd0;
    parameter WAIT_RESEND1 = 'd1;
    parameter WAIT_RESEND2 = 'd2;
    parameter ERROR = 'd3;
    parameter RELEASE_ = 'd4;

    always @(posedge clk) begin
        if(reset & ~(valid &) begin
            state <= IDLE;
        end else begin
            state <= state_next;
        end
    end

    always @(*) begin
        state_next = state;

        case(state)
            WAIT_: begin
                if((enable==0) & (complete==0)) begin
                    state_next = PAUSED;
                end else if((enable==1) & (complete==0)) begin
                    state_next = COUNTING;
                end
            end
            WAIT_RESEND1: begin
                if((enable==0) & (complete==1)) begin
                    state_next = IDLE;
                end else if((enable==1) & (complete==1)) begin
                    state_next = DONE;
                end else if((enable==0) & (complete==0)) begin
                    state_next = PAUSED;
                end
            end
            WAIT_RESEND2: begin
                if((enable==1) & (complete==1)) begin
                    state_next = DONE;
                end else if((enable==1) & (complete==0)) begin
                    state_next = COUNTING ;
                end else if((enable==0) & (complete==1)) begin
                    state_next = IDLE;
                end
            end
            ERROR: begin
                if(complete==1) begin
                    state_next = IDLE;
                end else if((enable==1) & (complete==0)) begin
                    state_next = COUNTING;
                end else if((enable==0) & (complete==0)) begin
                    state_next = PAUSED;
                end
            end
            RELEASE_: begin
                if(complete==1) begin
                    state_next = IDLE;
                end else if((enable==1) & (complete==0)) begin
                    state_next = COUNTING;
                end else if((enable==0) & (complete==0)) begin
                    state_next = PAUSED;
                end
            end
        endcase
    end
endmodule

```

VPL

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Data retention summary