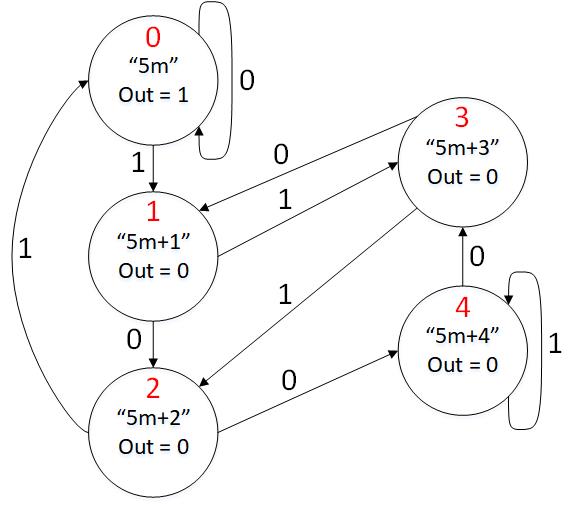
Introduction

The figure below shows the state transition diagram of a Finite State Machine(FSM) which checks the obtained sequence for divisibility by 5. The output is set to 1 whenever the input sequence is divisible by 5.  For example,a sequence "**011110101**" goes through  states  **0=>1=>3=>2=>0=>1=>2=>0**. The corresponding ouput trace will be **1=>0=>0=>0=>1=>0=>0=>1**.



The diagram above illustrates the transitions of the FSM that should be implemented to achieve this. It shows a Moore Machine where the output is defined by the state. The machine has five states (that are numbered in red).  Each state in the above diagram is represented as 5m+x, where m is an interger and x is the remainder obtained when divided by 5.

#### Assignment

You will be provided with a buggy implementation of the above fsm. You need to find the bug and change it to make it working as per the state transition diagram given above. The FSM module you will modify is named [**div**](https://exam.oncourse.tue.nl/exam-2019/pluginfile.php/5888/mod_vpl/intro/div5.v)**5. It** takes three input signals **clk, reset, in** and produces two output signals **out**and**state\_display**. The **reset**input always makes a transition to the **5m** state.  Assume all input and output signals to be 1 bit wide except state\_display which is 3 bits wide and little endian. The **state\_display** must output the number of the current state using the same numbers as the states in the FSM diagram above (shown in red).

Debug

Click on the symbol marked below to see waveforms.