Lab 3: Superscalar PARCv2 Processor

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Abstract

Design

Objective 1: Two-Wide Superscalar Processor with Dual Fetch, Single Issue

Objective 2: Two-Wide Superscalar Processor

No extensions were implemented.

Testing Methodology

Evaluation

The three versions of the pipelined processor were tested using the following benchmarks: vector add, complex multiply, masked filter, and binary search. The cycle counts and IPC for each benchmark are shown below in the format, cycle count / IPC.

Benchmark	pv2dualfetch	pv2ssc	pv2byp

Discussion

Figures