EENG 420 - Computer Architecture - Lab 1 Report

Bryan SebaRaj

Professor Abhishek Bhattacharjee

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Abstract

Simple arithmetic operations are taken for granted in modern computing from the perspective of the common software engineer. However, at the hardware level, these operations are non-trivial to implement. This lab focused on the implementation of a iterative multiplication and division module; Verilog was employed as the HDL to construct the multiplication and divison submodules, which each took in two 32-bit inputs and yielded a 64-bit output to be parsed as the product, quotient, or remainder. The submodules were integrated into a compound module, and the entire system was tested using a testbench. The results of the simulation were analyzed to determine the cycle count of the system.

After confirming the correctness of the multiplication and division modules, and

Design

Starting with the multiplication module, the prescribed datapath was followed. However, rather than relying solely on structural components, such as multiplexers, to construct the data path, behavioral Verilog was employed to partially define the flow of data.

Testing Methodology

Evaluation

The simulation results are as follows:

Register A	Operation	Register B	Result	Number of Cycles
0xdeadbeef	*	0x1000000	0xfdeadbeef0000000	33
0xf5fe4fbc	/	0x00004eb6	0xffffdf75	33
0x0a01b044	%	0xffffb14a	0x00003372	33
0xf5fe4fbc	/u	0x00004eb6	0x00032012	33
0x0a01b044	%u	0xffffb14a	0x0a01b044	33

See Appendix A for a screenshot of the simulation results.

Appendix A