Final Project

Due dates: See individual parts

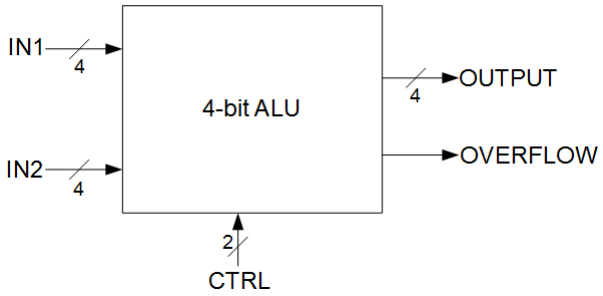
In this project, you will create a 4-bit arithmetic logic unit (ALU). While real ALUs perform numerous arithmetic and logical operations, ours will perform four:

1. Bitwise AND of two 4-bit values,
2. Bitwise exclusive-OR (XOR) of two 4-bit values,
3. Addition of two positive 4-bit numbers,
4. Subtraction of two positive 4-bit numbers.

Your design will use standard cells (semi-custom), as opposed to full custom. You must follow the general floorplan that is provided. However, within this framework, optimization of area, power consumption, and speed will be rewarded. **Extra credit** will be awarded for several performance metrics. The same team can win all three. The overall grading scheme is detailed at the end of this document.

1 Background

Fig. 1(a) shows the highest level block diagram of what you are going to make, along with the high level truth table in Fig. 1(b). In order to make this, you will need several standard cells: 4 logic gates (NOT, AND, OR, XOR), a 4-to-1 (or a 2-1) multiplexor (MUX), and a Full Adder (FA). Fig. 2 shows a possible block diagram implementation of the ALU, where the 4-1 MUX is implemented as two 2-1 MUXs, and the least significant bit (LSB) of the control signal chooses between addition and subtraction. For each of these components, there are many possible implementations. For example, you can implement a MUX using NAND gates, AND and OR gates, or pass-gate logic altogether. You can choose any method you want.



(a)

CTRL1	CTRL0	OUTPUT
0	0	IN1 **AND** IN2
0	1	IN1 **XOR** IN2
1	0	IN1 **+** IN2
1	1	IN1 **-** IN2

(b)

Figure 1: High level block diagram of ALU

NOTE: For the FA, each input will be a 4-bit two's complement positive number (i.e. the three LSBs are the value from 0 to 7, and the MSB is the sign). OVERFLOW = 1 when both IN1 and IN2 have the same sign, but the output has a different sign. For example, 0111 (7) + 0110 (6) = 1101 (-3). The Boolean function is OVERFLOW = $(\overline{\text{IN1}_3})(\overline{\text{IN2}_3})(\text{OUTPUT}_3) + (\text{IN1}_3)(\text{IN2}_3)(\overline{\text{OUTPUT}_3})$, where the subscript 3 indicates the MSB of a 4-bit number.

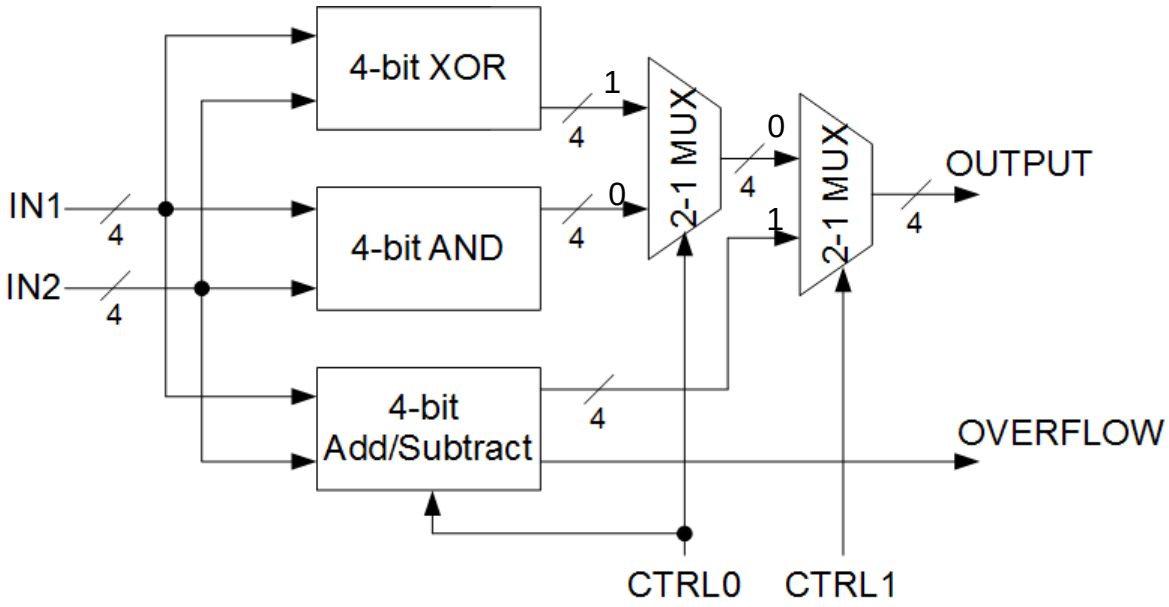


Figure 2: Detailed block diagram of ALU

2 Milestones

Part 1 (due 02-17)

Design standard cells for 1-bit NOT, AND, OR, and XOR gates. The main idea of standard cells is that they can be easily put together into more complicated circuits. For learning purposes, however, I will not impose too much structure, as I want you to figure out good and bad ideas on your own. As an example, look at Lecture 4, page 5. These are the guidelines:

1. There must be a power rail on top and a ground rail on the bottom.
2. The gates must be the same height.
3. The gates should be sized so as to make the propagation delays symmetrical.

To give you an idea of where this is headed, your design will have to be arranged in a grid like the one shown in Fig. 3. *Note*: Your gates must fit into the areas labeled "Logic". The distance between the power and ground rails of a given row of logic is called the "pitch". I will not specify the pitch for this project; it is up to you.

DELIVERABLES: Print out and hand in.

1. Schematic and layout of each cell.
2. Width and height (pitch) of each cell.
3. Extracted timing diagram of each cell, with propagation delays labeled.

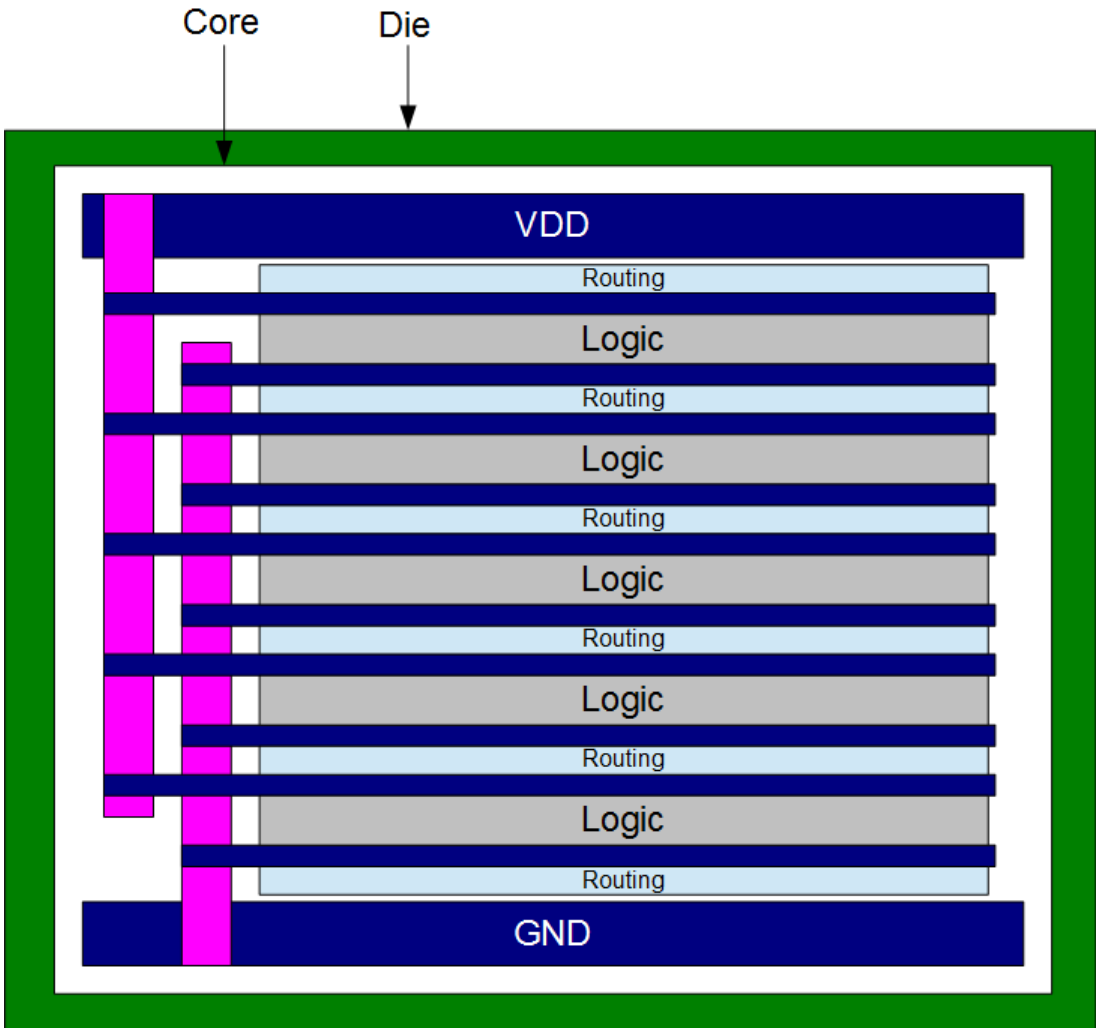


Figure 3: Layout floorplan.

Part 2 (due 02-24)

Design standard cells for the MUX and FA with the same pitch as your other standard cells. In addition, sketch a rough floorplan (using approximate actual sizes of your cells) like the one in Fig. 3, showing where your logic fits in. *Note*: Your cells can be taller than the pitch of your floorplan, but they have to be able to fit in the design. For example, your FA can be broken up into two parts (with interconnections), each of which has the right pitch, which can be stacked vertically in the layout.

DELIVERABLES: Print out and hand in.

1. Schematic and layout of MUX and FA cells.
2. Width and height (pitch) of MUX and FA cells.
3. Extracted timing diagram of MUX and FA cells, with propagation delays labeled.
4. Floorplan sketch.

Part 3 (due 03-03)

Implement the ALU. Here are the specifications for your layout:

- The pitch of your cells must be consistent.
- For routing:
  - Use poly for intra-cell signal routing.
  - Use metal for inter-cell signal routing.
  - Alternate directions for metal layers (e.g. M1 horizontal, M2 vertical, M3 horizontal, etc.).
- All inputs and outputs must be available at the boundaries of the die.

DELIVERABLES: Do not hand anything in, but must show either Ilya or Joseph.

1. Schematic of ALU.
2. Most of layout complete.
3. Be ready to answer why the routing should be as stated above.

Part 4 (due 03-12)

Write a report and prepare a 5 minute presentation.

In the report, include at least the following:

- Layout of final design.
- Discussion of your design choices.
- If given the chance to start over, what would you do differently this time?
- What was the greatest source of frustration in this project?
- Include a timing diagram with some typical inputs.
- What was your area, your power consumption, and your propagation delay?
- Include any relevant figures for your discussion.

There are no page guidelines as long as everything is addressed. Keep in mind, though, that including everything you can possibly include will not get you a higher grade. In fact, for most reports in life (journal publications or project findings for your boss), brevity is valued.

In the presentation, include the following:

- A figure of your schematic.
- A figure of your layout.
- A timing diagram.
- A brief discussion of your design choices.

DELIVERABLES:

1. Report.
2. Presentation.

3 Grading — 100 points

- **Part 1** — **15 points**
  - Proper standard cells — 10 points
  - Extracted simulation — 5 points
- **Part 2** — **20 points**
  - Proper standard cells — 10 points
  - Extracted simulation — 5 points
  - Floorplan — 5 points
- **Part 3** — **20 points**
  - Schematic with functioning simulation — 10 points
  - Layout with few errors on LVS and DRC — 10 points
- **Part 4** — **45 points**
  - Report — 35 points
  - Presentation — 10 points
- **Extra credit** — **Up to 20 points**
  - Smallest area-delay product — +5 points
  - Smallest power-delay product — +5 points
  - Smallest power-area-delay product — +10 points