UNIVERSITÄT PADERBORN

Die Universität der Informationsgesellschaft

Crossing the Styx: Variation of Operating Parameters and Fault Behavior of a Platform FPGA

Student Worker Project Plan

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Table of Contents

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1 Introduction

A recent bachelor thesis studied the magnitude of operating parameter margins build into frequency and temperature specifications of FPGAs. The results showed that one specific FPGA could be overclocked by 74.77% and overheated by 45.88%. Additionally, interesting effects in clock generation have been observed.
These results encourage further research. More series of measurements are needed to complete the understanding of parameter variation in FPGAs. At first additional measurements with a broader range of parameters shall be conducted. Then, variation of the supply voltage shall be integrated into the testbed. Eventually the measurement framework shall be extended to assess any arbitrary circuit, to make it a testbed for fault-tolerant designs.

This work shall eventually lead to scientific publications and give a better understanding of FPGA behavior to the scientific community.

2 Current Status

This project is based on a completed bachelor thesis. The thesis generated interesting insights into the magnitude of operating parameter margins and error behavior of FPGAs. Illustration 1 shows the top level schematic of the circuits implemented in the FPGA.

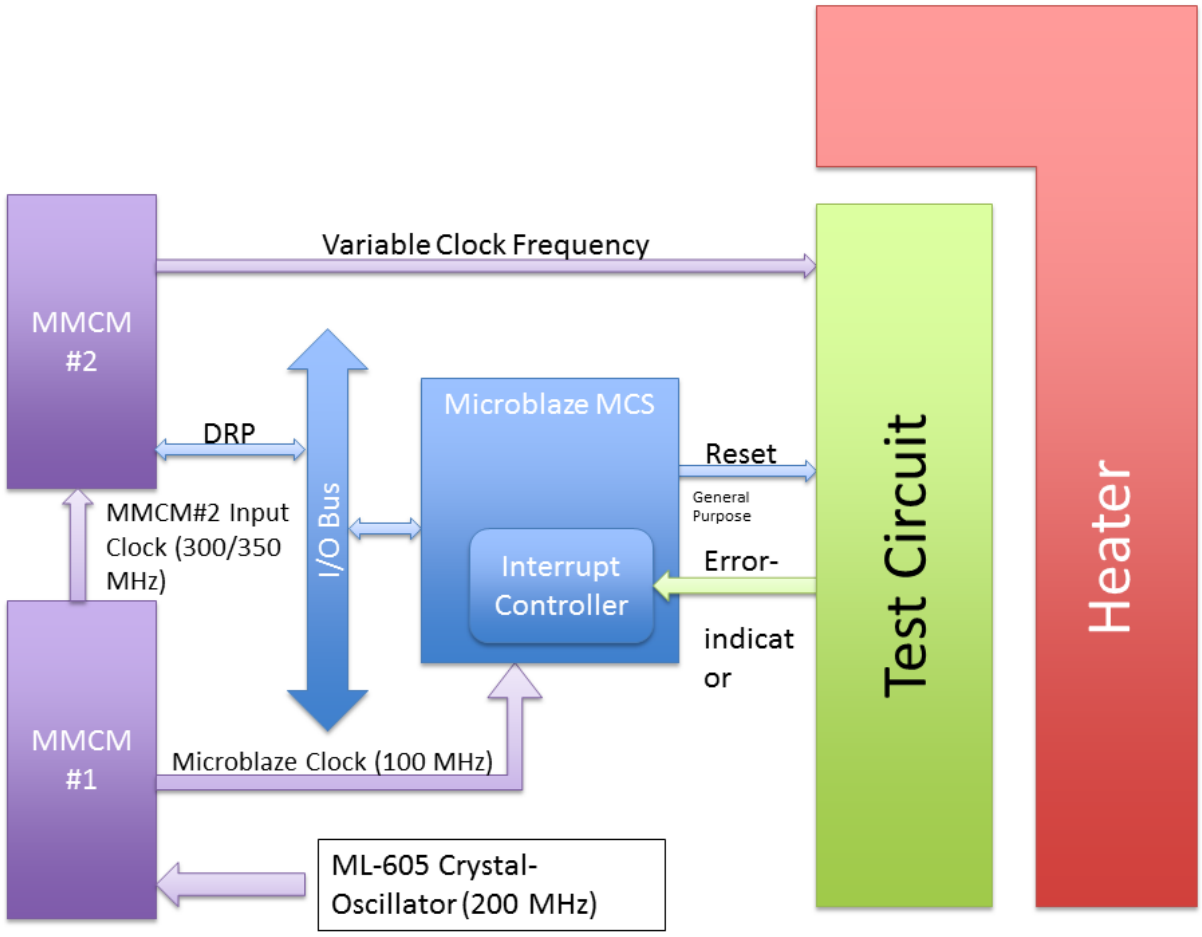

Illustration 1: Top Level Circuit Schematic

The main components are two cascaded Mixed-Mode Clock Managers (MMCM), a MicroBlaze MicroController System (MCS), the test circuit and heaters. The Microblaze MCS observes the test-circuit for errors via a 1 bit wide error indication signal and is able to perform a reset on the test-circuit for error recovery. Additionally the MCS is connected to the second MMCM's Dynamic Reconfiguration Port (DRP). Via this port it is able to set the test-circuits operating frequency.
The heaters have been specially designed to generate heat and raise the operating temperature of the FPGA. Currently they are *not* controlled by the MCS, but have to be loaded from an external computer to the FPGA via run-time reconfiguration.

With this setup, several series of measurement have been conducted. A brief abstract of results is given in the next chapter.

3 Results

The reported measurements comprise temperature and frequency measurements.

3.1 Temperature Measurements

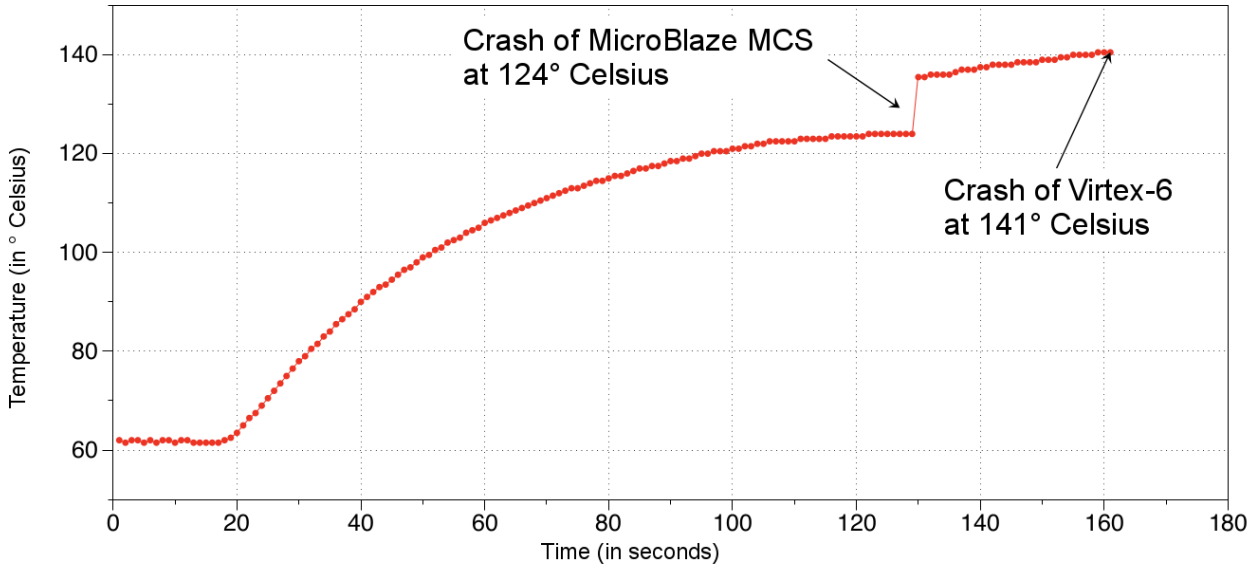

Illustration 2: Results of Temperature Sweep

Illustration 2 shows the results of a temperature sweep, obtained by using a hairdryer. (The internal heater circuits do not reach higher temperatures than 100 °C). Temperature was read via the internal temperature diode, which is integrated into the FPGA. The main results are:

- No errors of the test circuit were observed, but
- at 124°C measurement system (MicroBlaze) failed
- at 141°C whole FPGA failed: connection to the Systemmonitor for temperature reading failed. Only removal and reconnection of power supply reactivated the FPGA.

3.2 Frequency Measurements

Frequency measurements were done in two steps: first a coarse frequency sweep was done to identify the “interesting” frequency range, where errors happen. Then, the identified frequency range from approximately 360 MHz to 388 MHz was tested more thoroughly. The main results are depicted in Illustration 3. The critical path of the test-circuit was set to 202.55 Mhz at a specific place on the FPGA and MMCM#2 was fed with 300 MHz.

Errors were observed from 354.0 MHz (1st error in 24h test) up to a saturation point of around 83500 errors per second.

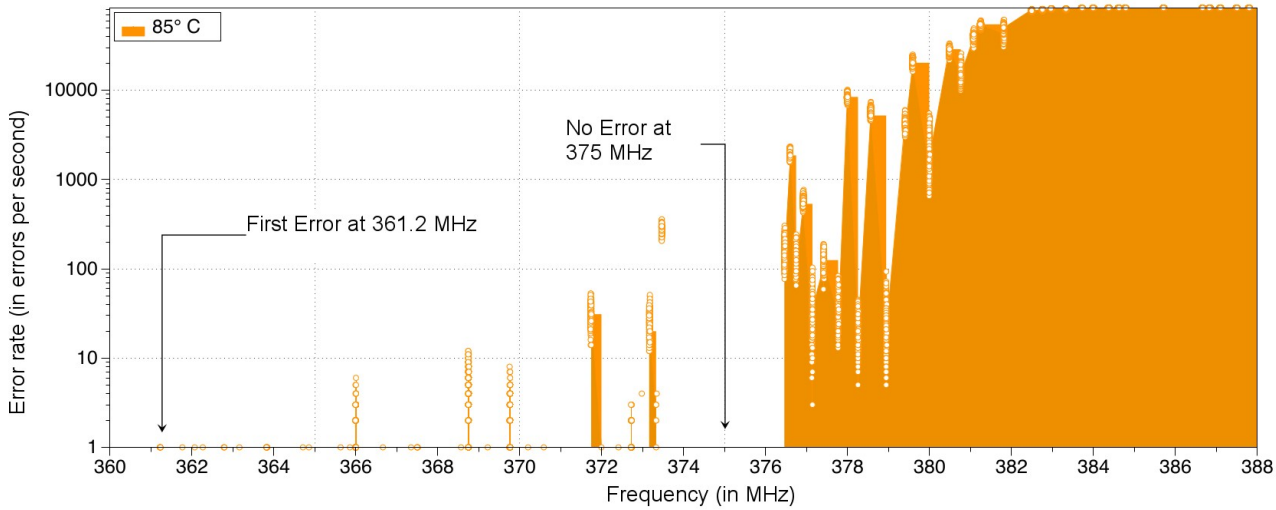

Illustration 3: Frequency Sweep at 300 MHz Input Frequency of MMCM#2

At 300MHz input to MMCM#2 a “Hill-Valley-Effect” was identified: the increase in error-rate was not continuous; sudden drops of error-rate between frequencies was observable. To investigate this effect, another frequency sweep with a different input frequency to MMCM#2 was done. The results are shown in Illustration 4. Here, no “Hill-Valley-Effect” was identified.

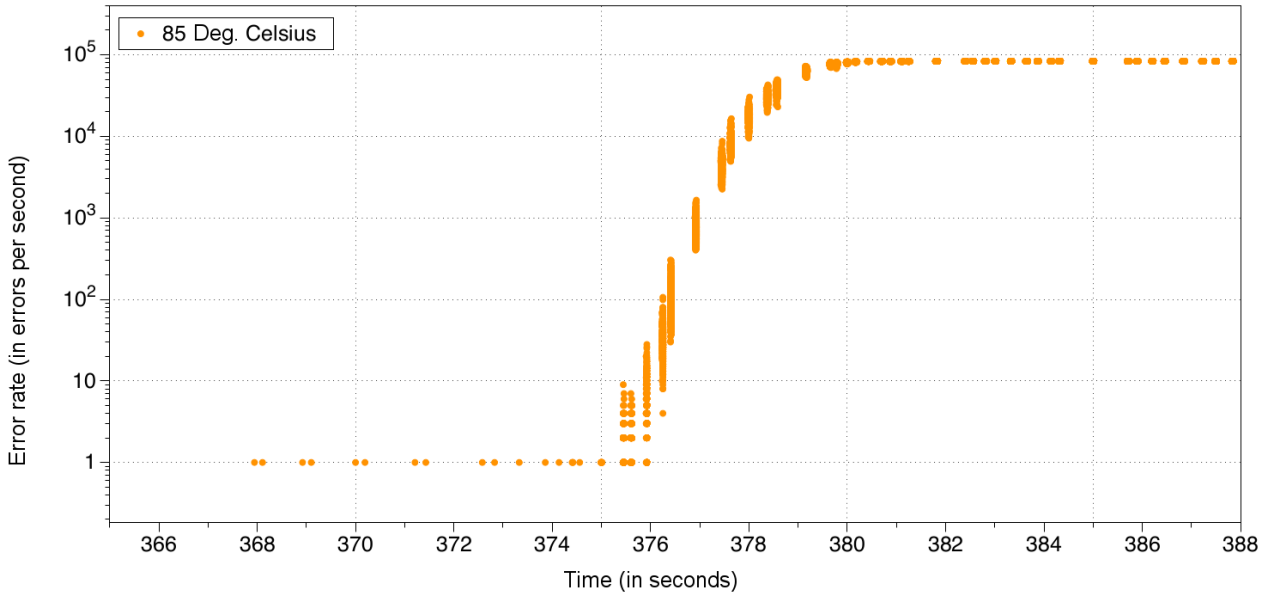

Illustration 4: Frequency Sweep at 350 MHz Input Frequency of MMCM#2

4 Project Objectives

For a scientific publication, these results have to be extended to make sure they are not singular for the given setup and additional measurements have to be made to better understand strange effects like the Hill-Valley-Effect. The list of improvements comprises:

- Test several ML605 boards, to make sure *all* FPGAs behave similar.
- Test boards of older generations to be able to estimate the development in the future
- Test at different parameterizations of the test-circuit (placement, length of critical-path)
- Test at different frequency inputs to the second MMCM, to research the Hill-Valley-Effect
- Add voltage variations to test setup

5 Project Plan

Phase	Months	Contents
Phase 1: Learn the ropes	1	• Synthesize the whole system again • Master partial reconfiguration • Repeat Measurements • Expected Results: ◦ Understanding of measurement system and ability to extend and modify it
Phase 2: Extend the Measurements	2 – 3	• Improve error counting, remove count limit. • Test several ML605 Boards • Create better statistics: average, median, standard deviation etc. • Place test-circuit at different positions on the FPGA. • Test at more input frequencies to MMCM2: confirm hill-valley effect • Expected Results: ◦ Rich set of statistics and graphs, showing the behavior of the FPGA over a wide frequency and temperature spectrum. • Bonus: Port system to older boards and make measurements on them

Phase 3: Voltage Variation and Fault injection (on contract extension)	4+	• We have an adapter to the power controller on the ML605 Board
		  ◦ Learn how to use it
		  ◦ Make measurements under different supply voltages
		  ◦ Test if more heaters can be activated with a higher supply voltage
		• Setup a more complicated system for fault injection experiments.
		  ◦ Compare complex system with simpler test-circuit
		• Test a fault tolerant version: does it produce less errors?