A 640×512 CMOS Image Sensor with Ultra Wide Dynamic Range Floating-Point Pixel-Level ADC

David X.D. Yang, Abbas El Gamal, Boyd Fowler, and Hui Tian

Information Systems Laboratory

Electrical Engineering Department

Stanford University

Stanford CA 94305

email: dyang@isl.stanford.edu, abbas@isl.stanford.edu, fowler@isl.stanford.edu

huitian@isl.stanford.edu

Phone: 1-650-723-3473 FAX: 1-650-723-8473

Session Number: 17

November 1, 1998

Abstract

A 640×512 CMOS image sensor with an 8b bit-serial Nyquist rate ADC per 4 pixels achieves 10.5×10.5 μm pixel size at 29% fill factor in 0.35 μm CMOS technology. Binary floating point output with measured dynamic range of of $65536 : 1$ is achieved by multiple sampling at exponentially increasing exposure times.

Dynamic range, defined as the ratio of the largest nonsaturating signal to the standard deviation of the noise under dark conditions, is a critical figure of merit for image sensors. The dynamic range of an image sensor is often not wide enough to capture scenes with both high lights and dark shadows. This is especially the case for CMOS sensors, which, in general, have lower dynamic range than CCDs. Several approaches have been proposed to enhance the dynamic range of a CMOS APS. In [1] dynamic range is enhanced by increasing well capacity one or more times during exposure time. Another approach, which achieves consistently higher SNR, is multiple sampling. Here the scene is imaged several times at different exposure times and the data is combined to construct a high dynamic range image. For this approach to work at reasonable capture times, readout must be performed at speeds much higher than normal APS speeds. In [2] an APS with two column parallel signal chains is presented. The sensor can simultaneously read out two images, one after a short exposure time T and the other after a much longer exposure time, e.g. $32T$. Two images, however, may not be sufficient to represent the areas of the scene that are too dark to be captured in the first image and too bright to be captured in the second. It is difficult to extend the scheme to simultaneously capture more than two images, since more column parallel signal chains must be added at considerable area penalty.

In this paper we demonstrate, using a 640×512 image sensor with Nyquist rate pixel level ADC implemented in a 0.35μm CMOS technology, how pixel level ADC enables a highly flexible and efficient implementation of multiple sampling. Since pixel values are available to the ADCs at all times, the number and timing of the samples as well as the number of bits obtained from each sample can be freely selected without the long readout time of APS. Typically, hundreds of nanoseconds of settling time per row are required for APS readout. In contrast, using pixel level ADC, digital data is read out at fast SRAM speeds. This demonstrates yet another fundamental advantage of pixel level ADC — the ability to programmably widen dynamic range with no loss in SNR.

The 640×512 sensor employs the MCBS ADC technique described in [3]. Each 2×2 block of pixels share a 1-bit comparator/latch pair. The signals required to operate the ADCs are globally generated by off chip DAC and digital control circuitry. The ADC is bit

serial and each bit is generated by peforming a set of comparisons between the pixel values and a **RAMP** signal. The bits are generated independently and in any order, and the data is read out as bit planes [3].

We consider the implementation of multiple sampling for exponentially increasing exposure times T, $2T$, $4T, \ldots$ 2^kT. Each sample is digitized to m bits. The digitized samples for each pixel are combined into an $m+k$ bit binary number with floating point resolution. The number can be converted to a floating point number with exponent ranging from 0 to k and an m bit mantissa in the usual way. This increases the sensor dynamic range by a factor of 2^k, while providing m bits of resolution for each exponent range of illumination. An important advantage of this scheme, over other dynamic range enhancement schemes [1], is that the combined digital output is linear in illumination. This not only provides more information about the scene, but also makes it possible to perform color processing in the standard way.

To illustrate how our sensor implements this scheme, consider an example with $k = 2$ and $m = 2$. Figure 1 plots the output pixel voltage versus time for three constant illuminations I_1, I_2, and I_3, assuming linear photon to voltage response, and saturation voltage V_{max}. The voltage is sampled after exposure times T, $2T$, and $4T$. Each sample is digitized to 2 bits using binary code as shown in the figure. The first sample is digitized to x_1x_2, e.g. 11 for I_1. The second is also digitized to 2 bits. Since the second sample is twice the value of the first, the 2 bits are x_2x_3 if the sample is not saturated, i.e. $< V_{max}$, and 11 if it is. In either case, the ADC only needs to generate the least significant bit x_3. Similarly, for the third sample at $4T$ only the least significant bit x_4 needs to be generated. Table 1 lists the bit values for each illumination and the corresponding binary floating point representation. This scheme can be easily extended to any exponent k and mantissa m. The first sample is digitized to m bits, then only the least significant bit is generated from each consecutive sample. Thus as long as the sensor photon to voltage response is linear only $m+k$ bits need to be read out, which is the minimum required. This further reduces readout time. Often more bits need to be read out from the samples to correct for sensor nonlinearity, offset, and noise.

A schematic of four pixels sharing a 1-bit comparator/latch pair, and the column sense amplifier is shown in Figure 2(a). The comparator/latch circuit is described in [3]. An anti-

blooming transistor is connected to each photodetector to avoid blooming during multiple sampling. The sense amp is designed for high speed, low noise and power. A charge amplifier is used to minimize bitline voltage swing. To sense the bitline, capacitor Mc is first reset, and the current from the pixel and transistor M7 is integrated. The sensed bit is latched using a flip flop. The tristate inverter is part of a 10:1 mux.

A scene is imaged one quarter frame at a time as illustrated in Figure 2(b). Before capturing a quarter frame the sensor is reset. Sample and hold is used to ensure that the signal does not change during ADC. Each quarter sample image is read out one bit plane at a time [3]. The quarter images are, then, combined to form a quarter frame, and the quarter frames merged into a high dynamic range frame.

A photomicrograph of the sensor is provided in Figure 6. Table 2 summarizes the main sensor chip characteristics. Figure 3 plots the pixel output voltage vs. time under constant illumination. Note that it is quite linear. A scene with measured dynamic range $\geq 10^4$ is illustrated in Figures 4 and 5. The scene was sampled 9 times, at $T = 3.3$ms, $2T, \ldots$, and $256T$, and a 16-bit image was reconstructed. Since we cannot print gray scale images of more than 8 bits, in Figure 4 we display four 8-bit slices of the image. The first is a plot of the 8 most significant bits of the 16-bit image, where only the roof and the front of the dollhouse is seen. The 2nd was obtained by brightening the image by 8x. Several objects inside the house are revealed. These objects become more visible in the 3rd image, after the original image was brightened by 32x. The 4th image was obtained by brightening the image by 256x. A table and a man hiding in the dark area next to the house appear. Figure 5 is an 8-bit plot of the log of the 16-bit image.

Acknowledgments:

The authors acknowledge the support of HP, Intel, Kodak, Canon, and Interval Research and the assistance of X. Liu, and M. Godfrey.

References

[1] S. Decker et al., "A 256x256 CMOS imaging array with wide dynamic range pixels and column–parallel digital output," *ISSCC Digest of Technical Papers*, Feb. 1998, pp. 176–177.

[2] O. Yadid-Pecht et al., "Wide Intrascene Dynamic Range CMOS APS Using Dual Sampling," *IEEE Trans. Elec. Dev.*, vol. 44, no. 10, pp. 1721–23, Oct. 1997.

[3] D. Yang et al., "A Nyquist Rate Pixel Level ADC for CMOS Image Sensors," *Proc. IEEE CICC*, May 1998, pp. 237–240.

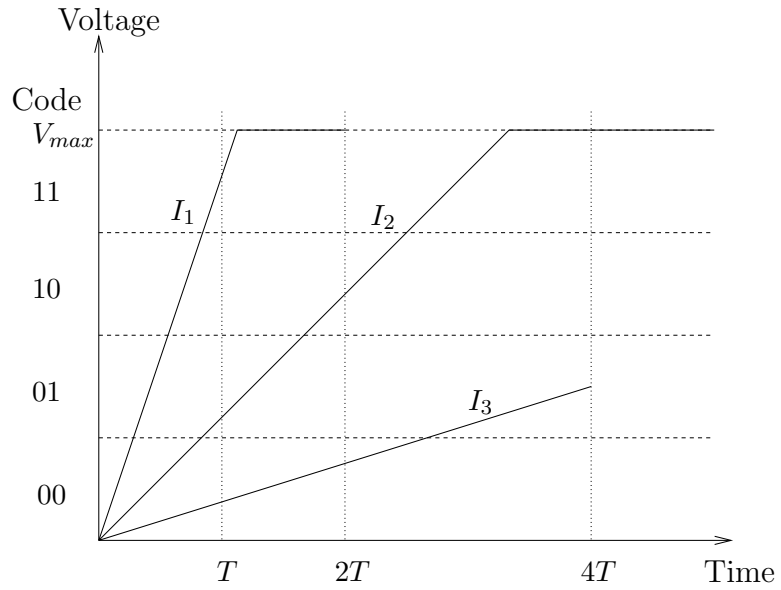
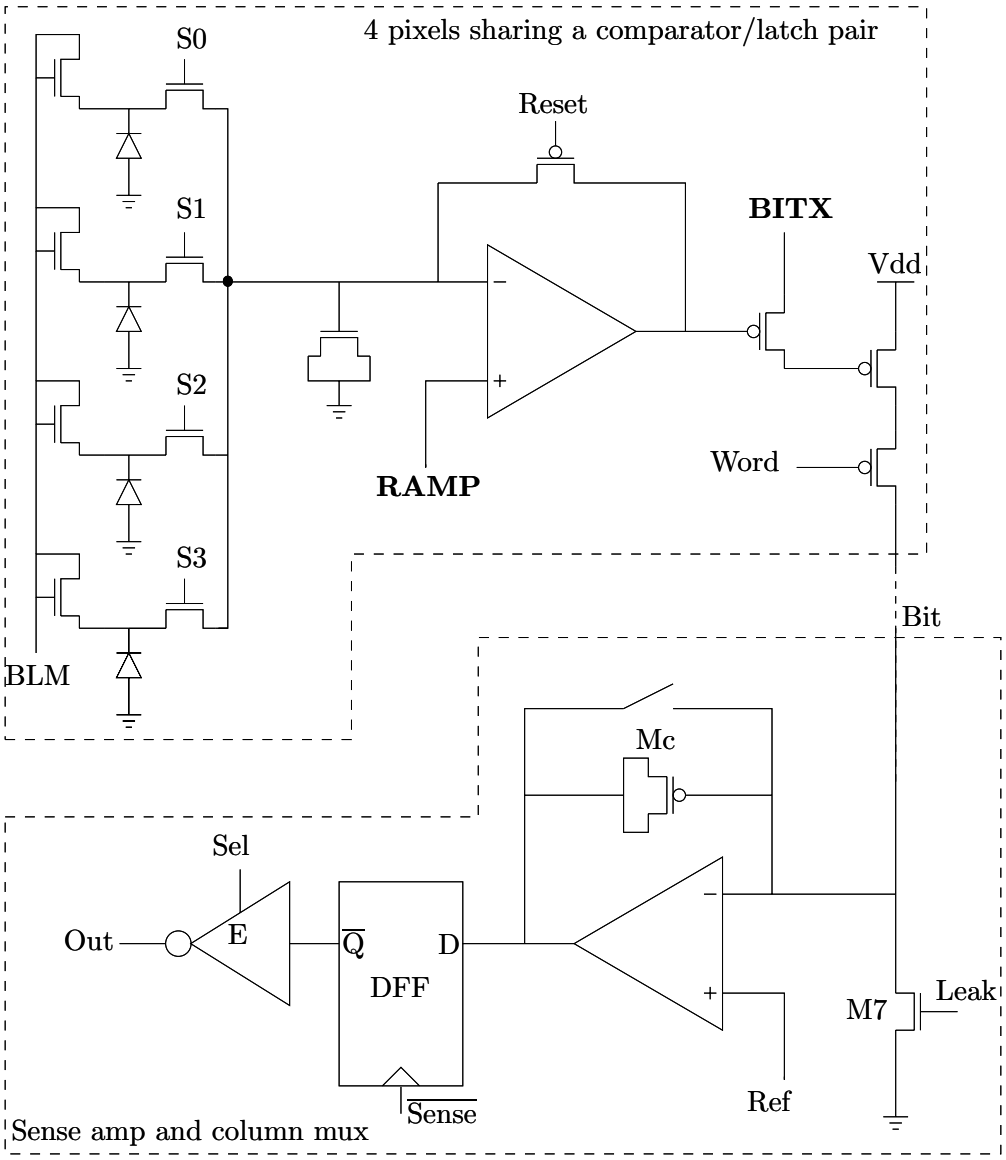


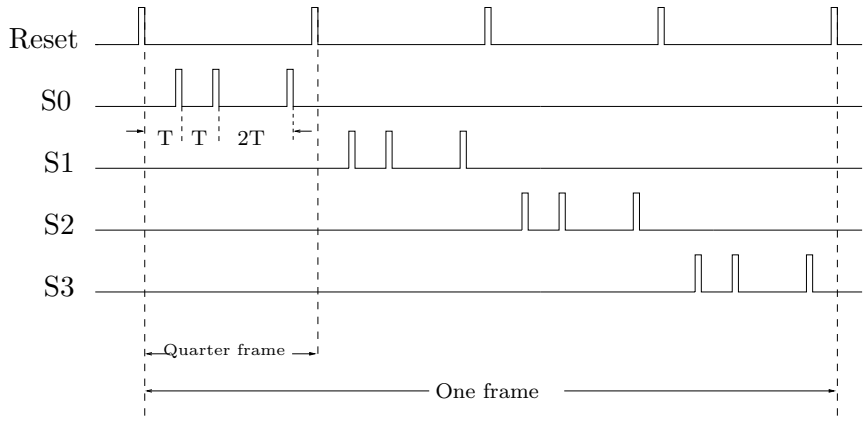
Figure 1: Pixel output voltage and its digitized value vs. time.

Illumination	$x_1x_2x_3x_4$	Exponent	Mantissa
I_1	1 1 1 1	2	11
I_2	0 1 0 1	1	10
I_3	0 0 0 1	0	01

Table 1: Digitized values for three illumination levels.



(a)



(b)

Figure 2: (a) Pixel block and column sense amplifier circuit. (b) Timing diagram for multiplexed multiple sampling.

Technology	0.35 μm, 4-layer metal, 1-layer poly, nwell CMOS
Sensor size	640×512 pixels
Pixel size	$10.5\,\mu\text{m} \times 10.5\,\mu\text{m}$
Photodetector	n-well to p-sub diode
Sensor area	$6720\,\mu\text{m} \times 5376\,\mu\text{m}$
Fill Factor	29%
Transistors per pixel	5.5 (22 per four pixels)
Package	180 pin PGA
Supply Voltage	3.3V
Signal swing	0.5–2.5V
Sensitivity	4.1 μV/e$^-$
Maximum frame rate	250 frames/s (@ 8-bit resolution)
Fixed pattern noise	$< 0.2\%$ (dark) at 25°C
Dark current	1.3 mV/sec (160 pA/cm^2) at 25°C
Digital dynamic range:	65536:1 measured

Table 2: Main Characteristics of 640x512 Area Image Sensor.

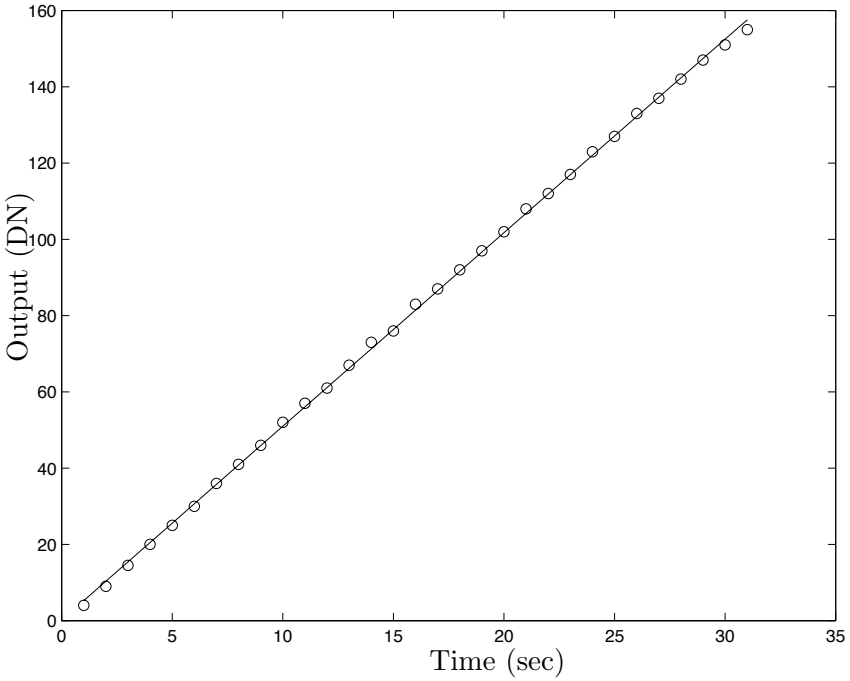


Figure 3: ADC output vs. time at constant illumination.

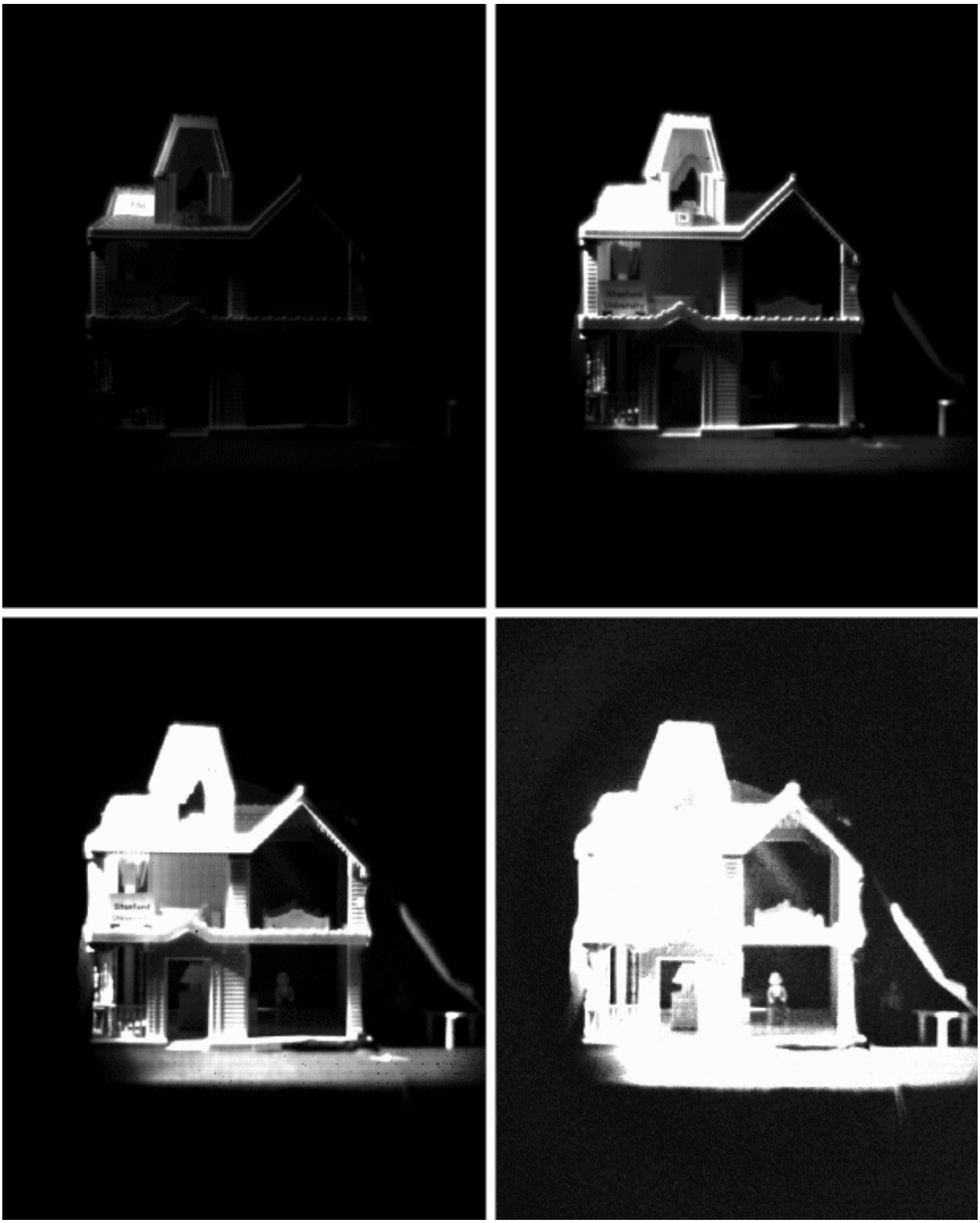


Figure 4: Four slices of the 16-bit image. (Upper left) Most significant 8-bit. (Upper right) Image brightened 8x. (Lower left) Image brightened 32x. (Lower right) Image brightened 256x.

Figure 5: Log the 16-bit image.

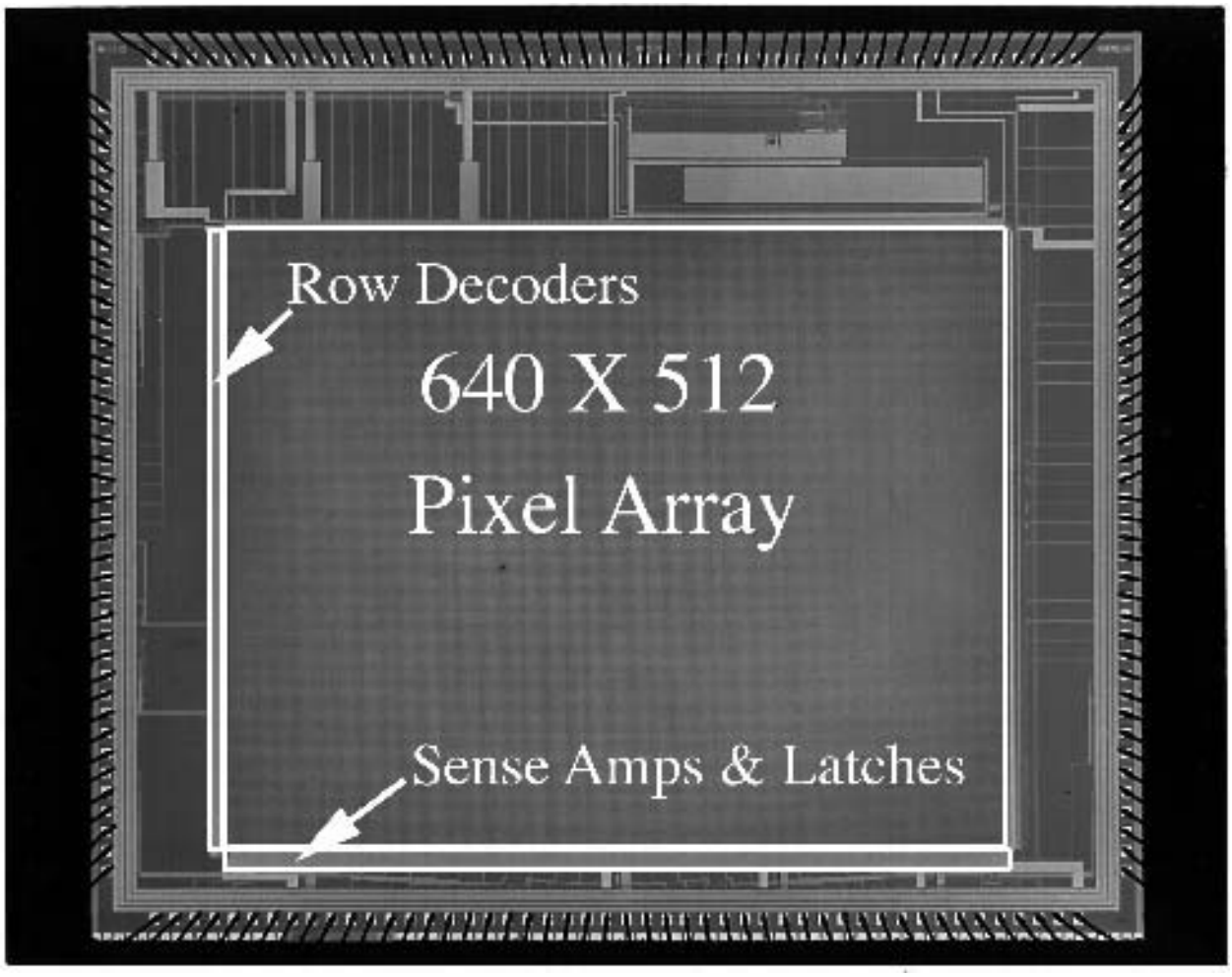


Figure 6: Die micrograph of 640×512 image sensor.