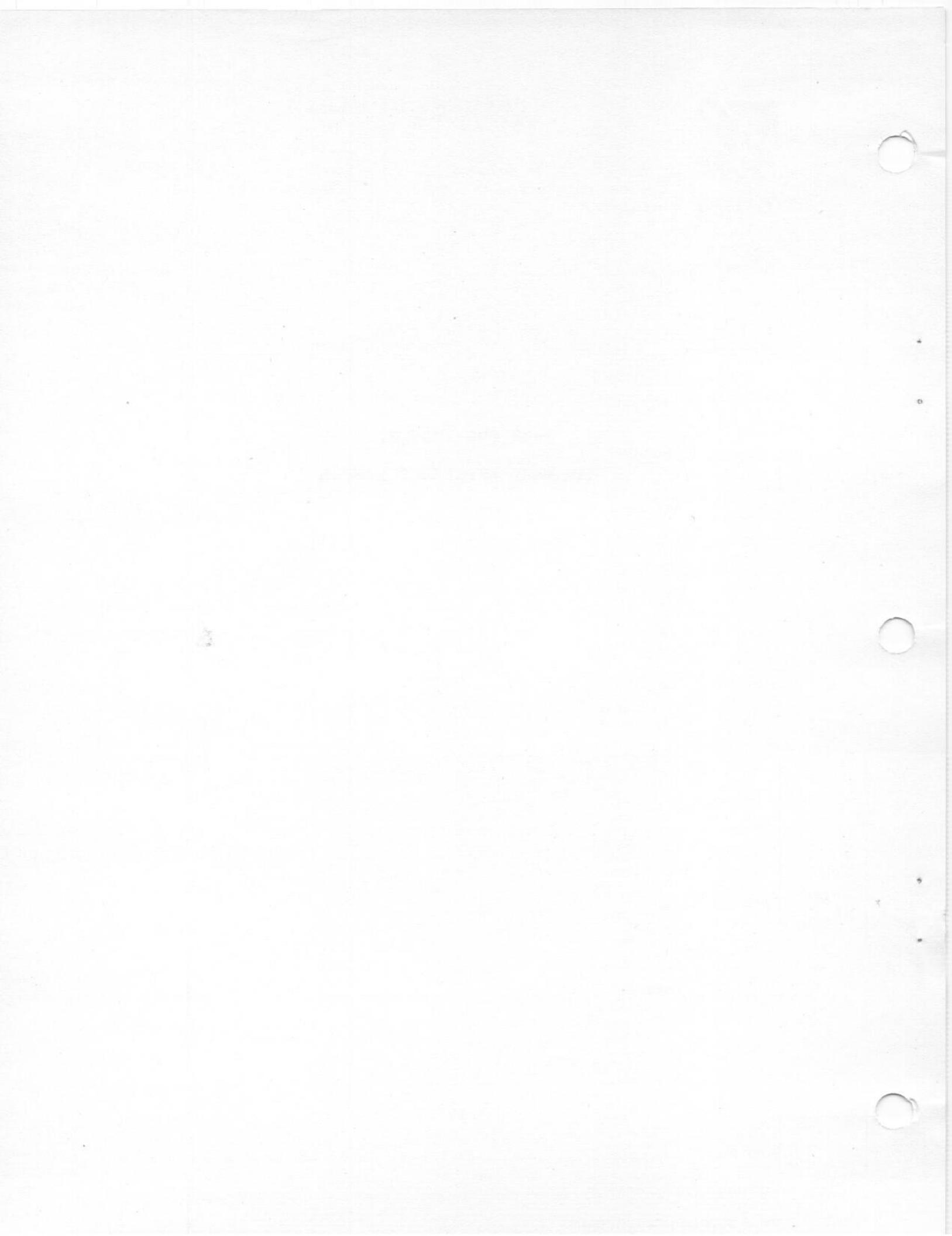


**Z-80 MDC (MDC/E)**

**HARDWARE REFERENCE MANUAL**





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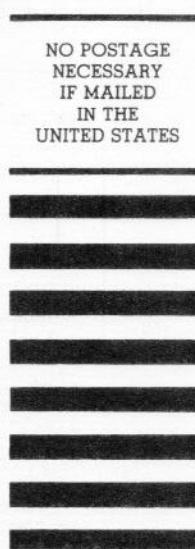
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## SECTION 1

### INTRODUCTION

#### 1.1 General Description

The Zilog Z-80 MDC (Memory Disk Controller) and the MDC/E (European Version) are part of the Zilog MCB Series of OEM cards and systems. The MDC directly interfaces to all other boards in the MCB Series and provides optional 12K, 16K, 32K, or 48K bytes of dynamic RAM memory for program or data storage, plus a floppy disk controller that is capable of handling up to eight floppy disk drives. The 12K version (assembled with 4K dynamic RAM devices) is separated into three pages of 4K bytes each. The starting address for each of the 4K byte pages may be set by programmable read only memory (PROM) to begin on any of up to sixteen page boundaries. The other three versions are assembled using 16K dynamic RAM devices. For each version, the address decode PROM determines the starting address for the four segments of the 64K address space. The standard version, which the following discussion applies, consists of 48K bytes.

A block diagram of the complete board is shown in Figure 1-1. A voltage converter is included on the board to convert the signal +5 volt input to the +12 and -5 volts required by the dynamic memory array. The upper address bits from the CPU are provided to a memory page decoder PROM. The starting address for each 4K block of memory can be set to any of sixteen possible starting locations. The page decoder output is then supplied, along with A0 through A13, to a memory address multiplexer to provide the proper address signals, along with the CAS and RAS control signals, to the memory array. The memory array utilizes 16-pin, 16K-bit dynamic RAMs, although strapping options allow 4K-bit RAMs also to be used. The data that is written to or read from the memory is passed through the set of data bus buffers.

The bottom half of the diagram is the disk controller. This disk controller is very simple because all of the disk formatting and control is actually provided by the CPU under program control. The Z-80 PIO is used by the Z-80 CPU to latch disk control information and to sample disk status information. Thus, control and status information from the disk is passed between the CPU and the disk via the Z-80 PIO. The data handling is provided by the blocks in the bottom part of the diagram. Data from the disk is provided to a data separator where the clock and data are separated into two distinct signals.

During READ operations, this data is then fed into the parallel/serial register. The shift clock during this operation is provided by the separated clock. While data is being supplied

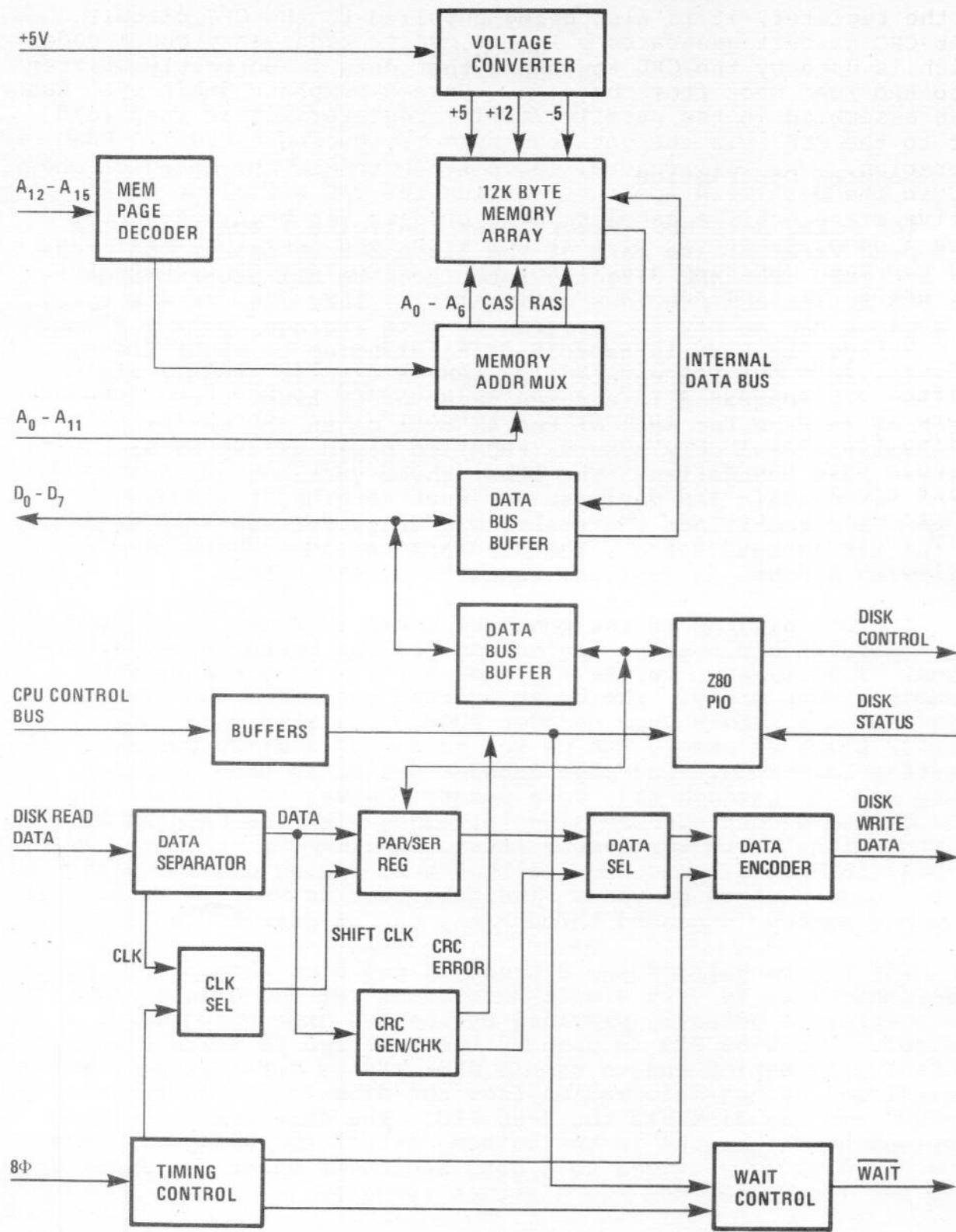
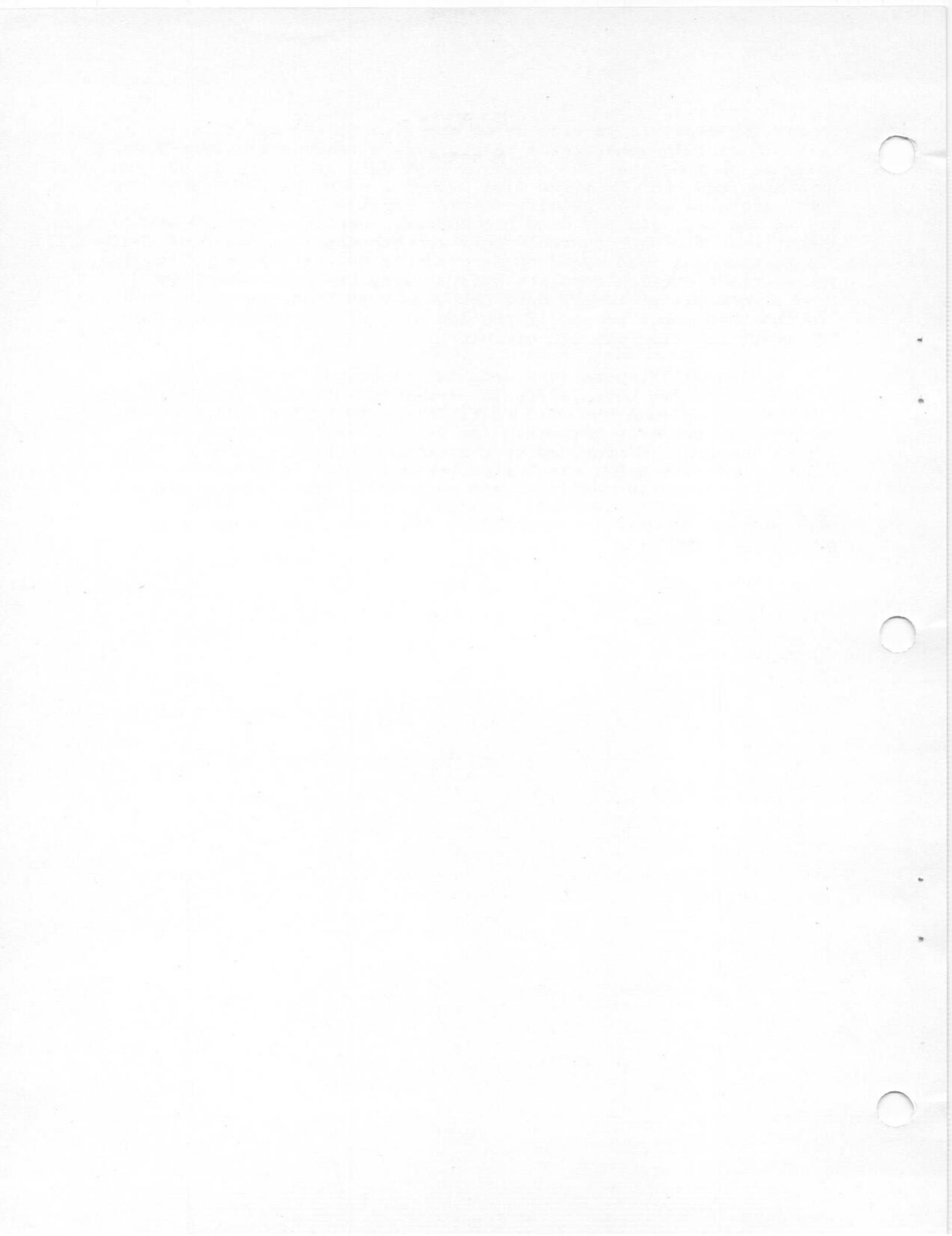


Figure 1-1. MDC Block Diagram

to the register, it is also being supplied to the CRC circuit. This CRC circuit generates a 16-bit cyclic redundancy check code which is used by the CPU to insure that data is correctly written onto and read back from the disk. Once a complete 8-bit byte has been assembled in the parallel/serial register, it is then read out to the CPU, via the data bus buffers, during a CPU I/O READ operation. The WAIT control logic synchronizes the speed of the CPU to the disk read speed by setting the CPU WAIT line to an active state until a complete byte of data has been assembled. Once a complete sector of data has been read from the disk, the CPU can then check to see if the CRC was correct by reading the CRC error bit from the CRC circuitry.

During WRITE operations data is loaded, via the data bus buffers, into the parallel/serial register. From there, it is shifted out through the data multiplexer and to the data encoder, where it is properly formatted for writing onto the disk. The timing for this is provided by the timing control circuit. This circuit uses the 8 PHI clock from the MCB Board to generate a shift clock for the register, and to provide other timing signals to properly encode the data. Again, during this operation, a WAIT control is used to synchronize the CPU to the proper disk operating speed.



## SECTION 2

### MDC BOARD SCHEMATICS

#### **2.1 Detailed Description Of Board Schematics**

The following sections describe in detail, the function of each separate sheet of the MDC Board Schematics.

#### **2.2 Power Supply And Control Buffers (Sheet 1)**

Sheet 1 contains the DC to DC voltage converter. This circuit is used to convert the +5 power input to the -5 and +12 voltages which are required for the memory. Also contained on Sheet 1 are bus buffers to isolate the CPU control signals, and selected address bits from the system bus.

#### **2.3 Memory Address Multiplexor (Sheet 2)**

Sheet 2 contains the control logic for the memory page decoders and memory address multiplexer. The 74LS75 circuit latches the four upper address bits from the CPU during MREQ-. The 7603 PROM decodes these bits into sixteen possible memory segment-selects, allowing the user to select the starting locations for the memory. These selects are then used to generate the three RAS signals, which are provided to the three banks of memory. A fourth PROM output is supplied to the low power inverter chain to generate the CAS signal. After two gates of delay, this signal is used to control the 74LS157 address multiplexers. These two address multiplexers then take the address bits A0 through A13 and properly time them and multiplex them as seven bits of address to the dynamic memories.

#### **2.4 Memory Array (Sheet 3)**

Sheet 3 of this schematic contains the 24 memory elements that are used in the memory array. The memory elements utilized in the standard board are 16K dynamic RAMs, however, 4K bit dynamic RAMs can also be utilized with proper strapping.

#### **2.5 Data Bus Buffers (Sheet 4)**

Sheet 4 contains the buffers that are used to separate the data bus into the internal data busses that are required by the disk controller and the memory array. The top two devices are used to separate the data bus into data input and data output for

the memory array. The bottom two devices are used to buffer and isolate the system data bus from the disk controller internal bus. The 6306 PROM on the bottom of the schematic is used to control the direction of the data bus buffers. This PROM recognizes when one of the devices on the MDC card must drive onto the system data bus and provides this control signal. Figure 2 identifies the state of the PROM output for the associated input. The five most significant input lines are shown in binary format along the vertical axis. The four least significant address inputs (XXXX on the vertical axis) are identified in hexadecimal notation along the horizontal axis. For each unique address input, the corresponding hex code for the output is found at the crosspoints between the two axis.

## 2.6 Parallel/Serial Register (Sheet 5)

Sheet 5 of the schematic illustrates the parallel/serial register that is used during both disk READ and WRITE operations. During disk WRITE operations, data from the internal data bus is latched into the register and shifted out on the serial WRITE data line. During READ operations, the decoded data from the data separator is shifted into this register, then read out to the internal data bus and through the data bus buffers, and back to the CPU. The select logic located below the registers is used to control the register shift mode and to provide the proper clocking signals.

## 2.7 PIO (Sheet 6)

Sheet 6 of the schematic contains the Z-80 PIO, which is used to latch control data for the disk and to sample status data from the disk. The Z-80 CPU bus connects to the PIO and is used for transfer of information between the two. The disk status signals are READY, TRACK 0, SECTOR MARKER, and WRITE PROTECT. These signals are terminated with 220 ohm and 330 ohm pull-up and pull-down resistors, respectively. The CRC error indicator from the CRC circuit is also provided to the PIO for CPU status checking. The PIO is also used to latch the control information for the disk drive. The control signals, DIRECTION, STEP, and four DISK SELECT lines are provided as outputs with open collector buffering. There are three other control signals that are required by the disk controller that must be separately timed, and the 74LS175 is used for this function. The READ, WRITE, and ENABLE CRC signals are latched by the PIO, but are separately timed by the strobe signal from the timing generator to insure proper timing.

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00000XXXX	08	08	08	08	08	-00-	08	08	08	08	08	08	08	08	08	08
00010XXXX	08	08	08	08	08	08	08	08	08	08	08	08	08	08	08	08
00100XXXX	08	08	08	08	08	-00-	08	08	08	-00-	08	08	08	08	08	08
00110XXXX	08	08	08	08	08	08	08	08	08	-00-	08	08	08	08	08	08
01000XXXX	08	08	08	08	08	-00-	08	08	08	08	08	08	08	08	08	08
01010XXXX	08	08	08	08	08	08	08	08	08	08	08	08	08	08	08	08
01100XXXX	08	08	08	08	08	-00-	08	08	08	08	08	08	08	08	08	08
01110XXXX	08	08	08	08	08	08	08	08	08	08	08	08	08	08	08	08
10000XXXX	08	08	08	08	08	08	08	08	08	08	08	08	08	08	08	08
10010XXXX	08	08	08	08	08	-00-	08	08	08	08	08	08	08	08	08	08
10100XXXX	08	08	08	08	08	08	08	08	08	-00-	08	08	08	08	08	08
10110XXXX	08	08	08	08	08	-00-	08	08	08	-00-	08	08	08	08	08	08
11000XXXX	08	08	08	08	08	08	08	08	08	08	08	08	08	08	08	08
11010XXXX	08	08	08	08	08	-00-	08	08	08	08	08	08	08	08	08	08
11100XXXX	08	08	08	08	08	08	08	08	08	08	08	08	08	08	08	08
11110XXXX	08	08	08	08	08	-00-	08	08	08	08	08	08	08	08	08	08

OUTPUT ENABLE-

IORQ-

M1-

RD-

GND

PORT DECODE

IEI.MDC.PIO

IEO.MDC.PIO

GP4-

FIGURE 2-1. MDC2 Bus Control PROM at Location A54

## **2.8 Timing Generator And Wait Control Logic (Sheet 7)**

Sheet 7 contains the circuitry that is used to generate the timing pulses that are required during the WRITE operations. Sheet 7 also contains the logic that is used to control the WAIT signal, which is used during both READ and WRITE operations. The four counter circuits (74LS161) are used to divide the 8 PHI clock into the proper timing signals. Strapping options are provided for use with mini-disk drives. The 74LS51 multiplexer is used to select between the timing pulse from the timing chain while in the WRITE mode, and the decoder clock from the data separator in READ mode. This clock is then provided as a shift clock to the parallel/serial register. The WAIT logic is centered around a single 74LS74 flip flop. Each time a disk data read or data write operation is requested by the MCB Board, the flip flop which pulls the WAIT-line low is set, and the CPU is stopped. This WAIT state is then held until such time as the DONE- signal is generated by the timing generator. This signal indicates that the parallel/serial register has been completely filled during READ operations or emptied during WRITE operations, and is ready for a new character. Thus, using this simple technique, the CPU speed is exactly synchronized to the disk operating speed.

## **2.9 CRC And Data Separator (Sheet 8)**

Sheet 8 of this schematic includes the CRC circuit which is used during both READ and WRITE operations. During WRITE operations, the data that is being written onto the disk is also clocked into this circuit. This data is then used to generate a 16-bit CRC word, which is to be appended to the end of the WRITE data. Multiplexer logic provided by the 74LS51 circuit selects between the actual SERIAL WRITE DATA and the CRC chip output. This circuit is also used during READ operations. During these operations, the READ DATA is clocked into the CRC chip so that at the end of every block of READ DATA, the generated CRC word can be compared with the CRC word that is received from the disk drive. If an error occurs, the CRC circuit will generate the CRC error flag, which can be read into the CPU via the PIO. The ENABLE CRC signal, which is used by the multiplexer during WRITE operations, is provided by the CPU via the PIO. Below this is the data separator. This circuit uses a oneshot to separate the clock and the data from the disk drive into a data signal and a clock signal, which will then be provided to the serial/parallel register. The data separator also contains a start bit detector which looks for the first logic 1 written after the READ mode is enabled. This start bit detector is used for formatting disks as described in Section 3.

## SECTION 3

### DISK DATA FORMATTING

#### 3.1 Introduction

All formatting of data onto the disk is accomplished under the control of the Z-80 CPU on the MCB board. Thus, this disk controller can operate with a variety of floppy disk drive configurations. Zilog, however, offers PROM-based software that can be used to control up to four Shugart 800 Floppy Disk drives. This software assumes that 32 hard sectors are utilized per track and 77 tracks are utilized per disk. The software provides all control functions for the disk and does all data transfer.

#### 3.2 Sector Data Format

As stated above, the Z-80 CPU controls all formatting of data onto a disk. Figure 3-1 represents the formatting structure: sixteen bytes of all zeroes for the preamble; one byte for sector address with the first bit being a start bit; one byte for the track address; then 128 bytes of data; four bytes of linkage (forward/backward) for file maintenance; two bytes of CRC; and then, a postamble of all zeroes.

In this format, the user may record up to 32 sectors (records) per track. Each track is started by a physical index pulse, and each sector is started by a physical sector pulse. This type of recording is called hard sectoring.

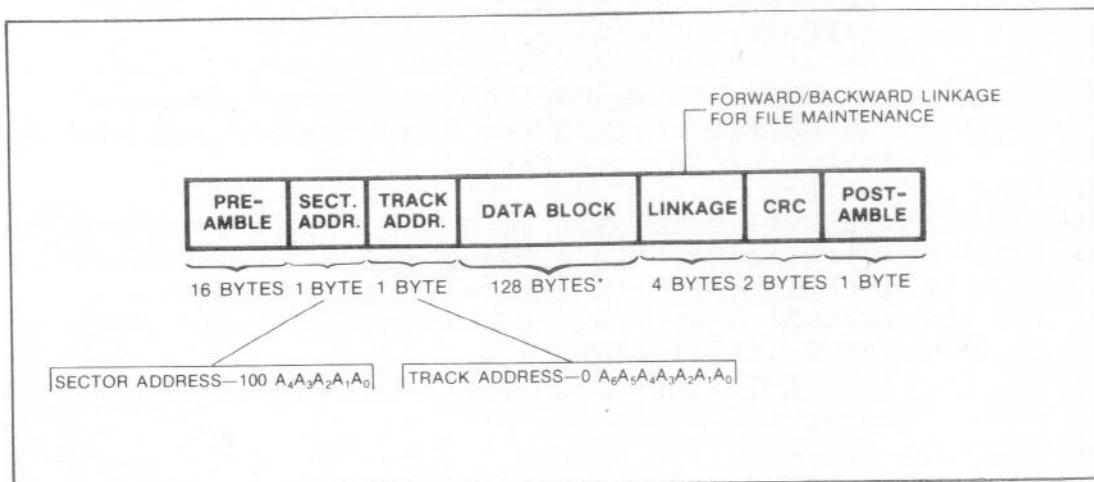
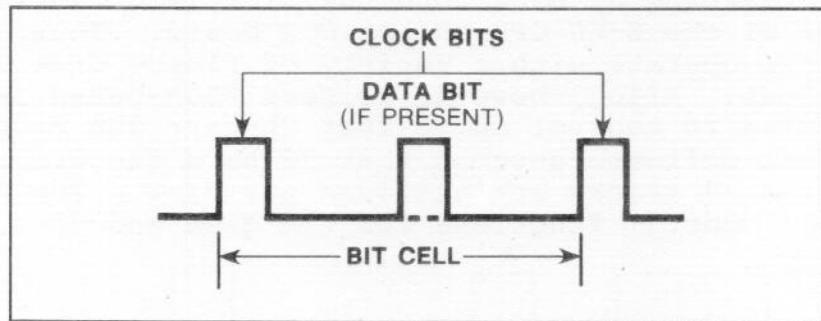


Figure 3-1. Disk Format

**BIT CELL:** As shown in Figure 3-2, the clock bits and data bits (if present) are interleaved. By definition, a bit cell is the period between the leading edge of one clock bit and the leading edge of the next clock bit.



**Figure 3-2. Bit Cell**

**BYTE:** A byte, when referring to serial data (being written onto or read from the disk drive) is defined as eight consecutive bit cells. The least significant bit cell is defined as bit cell 0 and the most significant bit cell is defined as bit cell 7. When reference is made to a specific data bit (i.e., data bit 3), it is with respect to the corresponding bit cell (bit cell 3).

During the write operation, bit cell 7 of each byte is transferred to the disk drive first with bit cell 0 being transferred last.

When data is read back from the drive, bit cell 7 of each byte will be transferred first with bit cell 0 last. As with writing, the most significant byte will be transferred first from the drive to the user.

### 3.3 Recording Format

Data is written on the diskette using frequency modulation as the recording mode, i.e., each data bit recorded on the diskette has an associated clock bit recorded with it. This is referred to as FM. Data written on and read back from the diskette takes the form shown in Figure 3-3. The binary data pattern shown represents a 101.

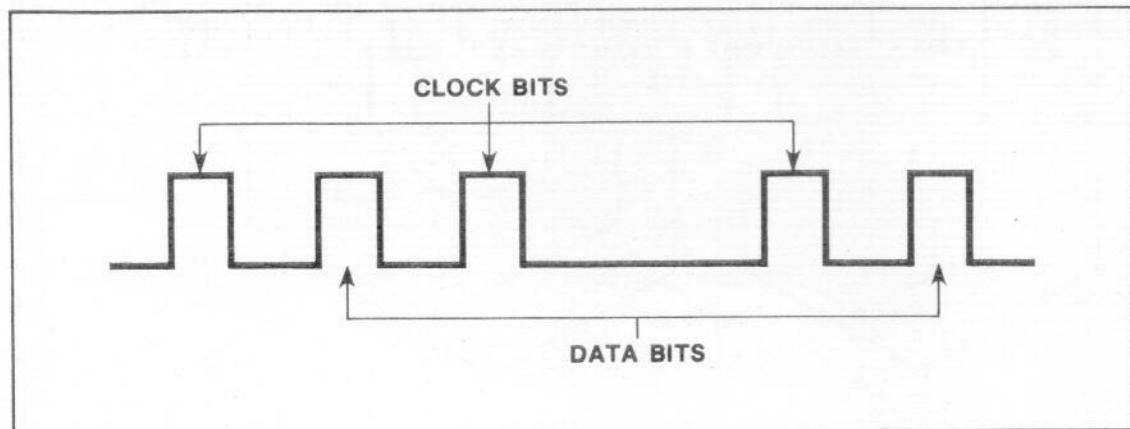
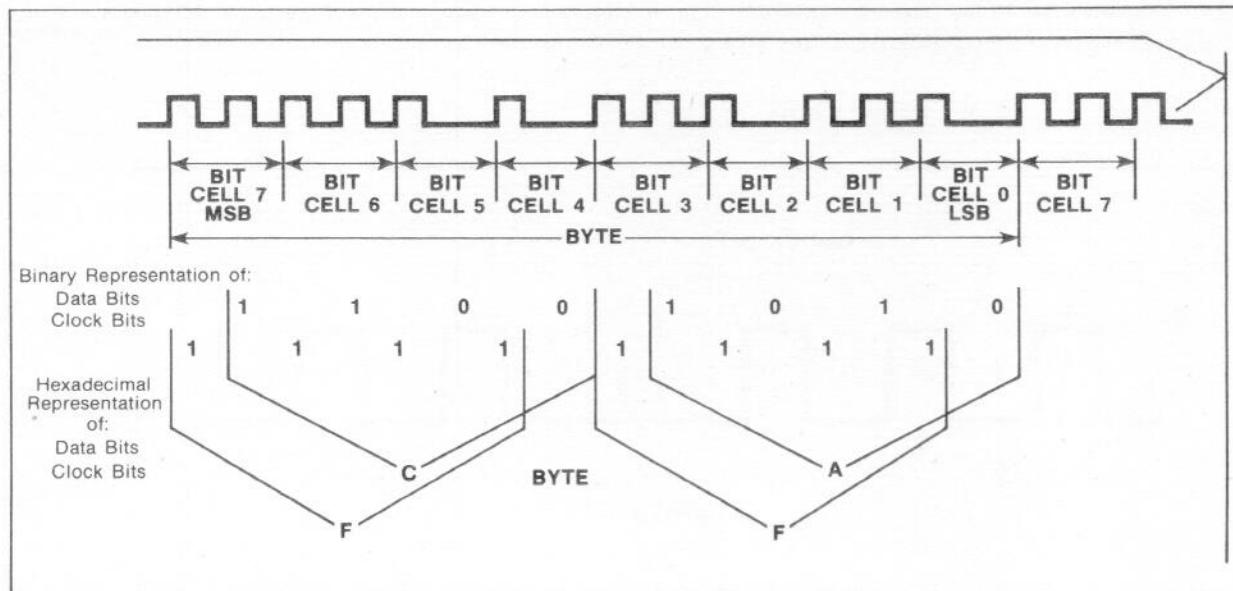
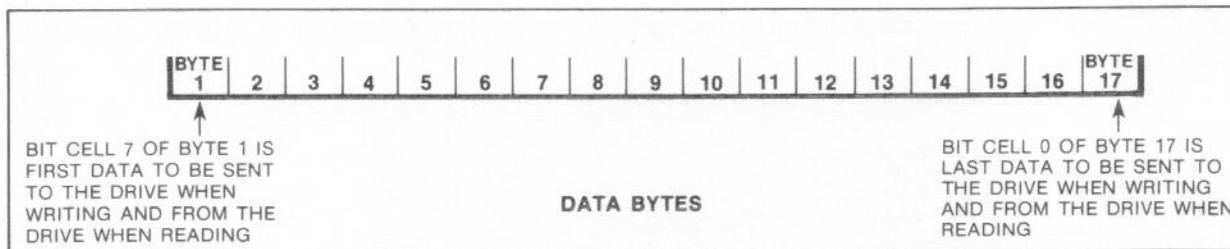


Figure 3-3. Data Pattern

Figure 3-4. illustrates the relationship of the bits with a byte, and Figure 3-5. illustrates the relationship of the bytes for READ and WRITE data.



**Figure 3-4. Bits Within A Byte**



**Figure 3-5. Data Byte Relationships**

## SECTION 4

### MDC MEMORY ADDRESS PROGRAMMING

#### 4.1 Introduction

The addresses associated with the memories on the MDC are programmed by a combination of a jumper wire plug and a 32 by 8 bit bipolar PROM. The jumper wires are used to program the address multiplexer for either 4K or 16K dynamic RAMs. The PROM is used to define which 4K page of memory will respond to a given memory address. This scheme allows a wide range of memory configurations to be implemented very easily.

As shown in Sheet 2 of the MDC logic diagram, inputs and outputs of the memory address PROM (A3) are defined as follows:

INPUTS	A0 = Address bit 12 A1 = Address bit 13 A2 = Address bit 14 A3 = Address bit 15 A4 = RFSH- (memory refresh signal from CPU)
OUTPUTS	01 = Not used    05 = CAS- 02 = Not used    06 = RAS0- 03 = Not used    07 = RAS1- 04 = Not used    08 = RAS2-

The PROM is enabled only when MREQ- is low to prevent output spiking. The PROM is programmed to output a zero on all RAS lines when RFSH- is low and to output a zero on CAS- and the appropriate RAS- line when address bits 12 through 15 are addressing a 4K memory block on the MDC.

#### **4.2 Programming For 4K RAMS**

Wiring for the 4K jumper plug is listed below:

FROM	J1-8	TO	J1-9, J1-10	(GND)
	J1-11		J1-13	(AB0)
	J1-12		J1-14	(AB6)

The following table shows the standard programming of A3 for use with 4K RAMs.

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00	1F															
10	FF	FF	CF	AF	6F	FF										

This programming places the RAMs in the address space 2000H to 4FFFH.

#### **4.3 Programming For 16K RAMS**

Wiring for the 16K jumper plug is listed below:

FROM	J1-11	TO	J1-13	(AB0)
	J1-1		J1-12	(AB12)
	J1-9		J1-14	(AB6)
	J1-2		J1-10	(AB13)

The table below shows the standard programming of A3 for use with 16K RAMs.

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00	1F															
10	FF	CF	CF	CF	FF	FF	FF	FF	CF	AF	AF	AF	AF	6F	6F	6F

This programming places the MDC RAM in the memory spaces 1000 to 4000H and 8000H to FFFFFH.

**APPENDIX A**  
**MDC PARTS LIST**

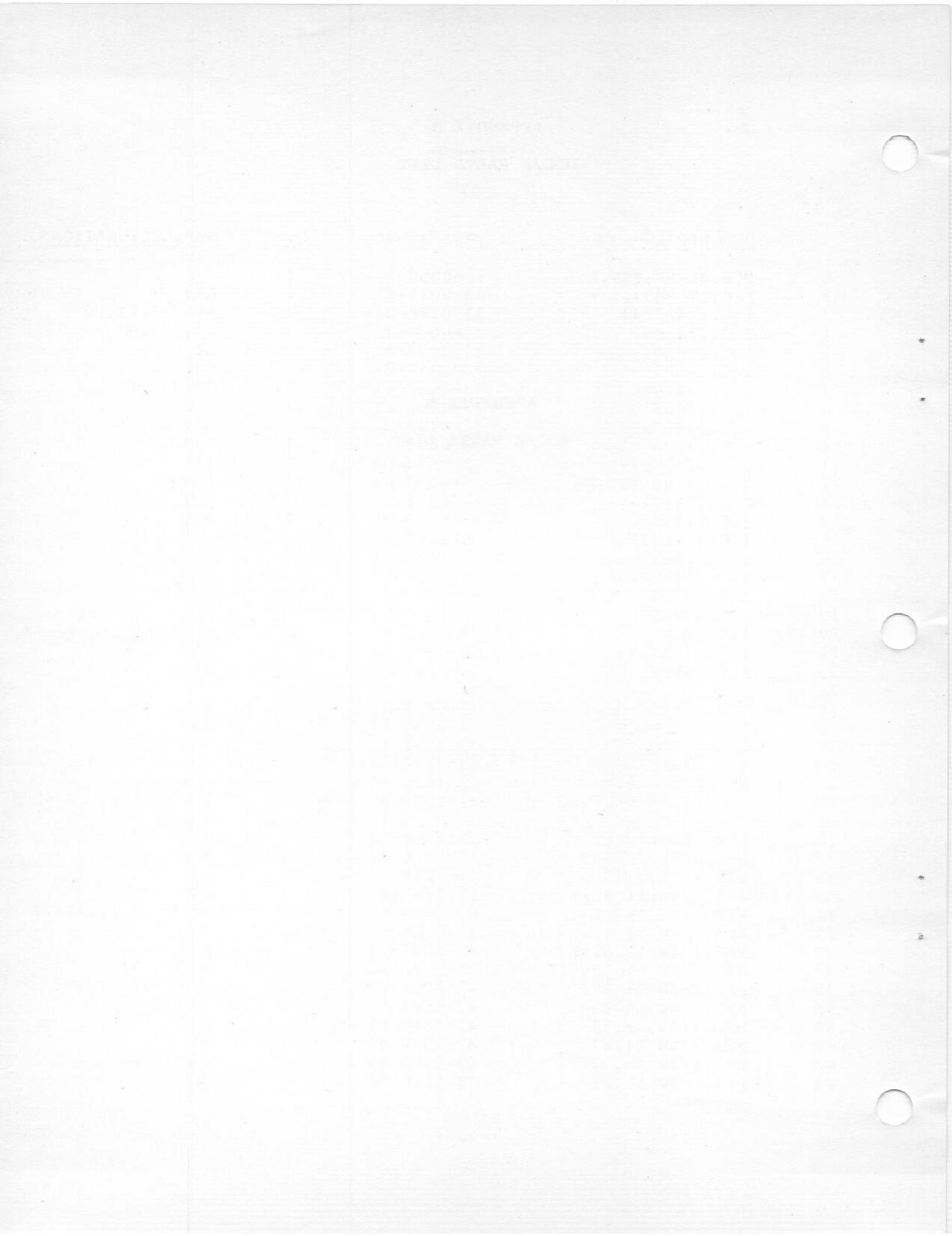


**APPENDIX A**  
**MDC PARTS LIST**

	<u>DESCRIPTION</u>	<u>PART NUMBER</u>	<u>QTY</u>	<u>REF. DESIGNATIONS</u>
1	PCB, BLANK, REV.A.B	10-0050-01	1	
2	I.C., TL-497	33-0075-01	1	A33
3	I.C., 74LS241	33-0178-01	4	A56,57,61,62
4	I.C., 74LS02	33-0046-01	3	A3,19,20
5	I.C., 74L04	33-0018-01	1	A4
6	I.C., 7406	33-0019-01	1	A53
7	I.C., 74LS00	33-0058-01	3	A2,21,22
8	I.C., 74LS10	33-0060-01	1	A18
9	I.C., 74LS243	33-0180-01	2	A59,60
10	I.C., PROM, 6306	33-0053-16	1	A24
11	I.C., 74LS299	33-0074-01	1	A58
12	I.C., Z-80 PIO, PS, 2.5MHZ	33-0057-01	1	A54
13	I.C., 74LS161	33-0071-01	4	A17,34,48,55
14	I.C., 74LS51	33-0065-01	1	A35
15	I.C., 74LS32	33-0062-01	1	A49
16	I.C., 74LS74	33-0066-01	2	A36,50
17	I.C., 74LS125	33-0067-01	1	A23
18	I.C., 9401	33-0042-01	1	A1
19	I.C., 74LS38	33-0064-01	1	A38
20	I.C., RAM	33-0049-00	24	A9-16,25-32,40-47
21	I.C., 74LS175	33-0072-01	1	A37
22	I.C., PROM, 7603	33-0164-02	1	A6
23				
24	I.C., 74157	33-0003-01	2	A7,8
25	I.C., 74LS221	33-0073-01	1	A51
26	I.C., 74LS145	33-0181-01	1	A52
27	I.C., 74LS75	33-0100-01	1	A5
28	SOCKET, 40-PIN	21-1000-01	1	A54
29	SOCKET, 16-PIN	21-1000-02	27	A6,9-16,25-32,40-4 24,J1
30	COMP., CARRIER	33-0173-22	1	J1
31	RES, NET, 220/330	47-0000-02	1	A39
32	RES, 1/2W, 0.27-OHM	47-2000-06	1	R1
33	RES, 1/4W, 5%, 9.1K	47-1001-02	1	R2
34	RES, 1/4W, 5%, 1K	47-1000-63	8	R3,7,12,13,15,25-2
35	RES, 1/4W, 5%, 220	47-1000-47	1	R4
36	RES, 1/4W, 5%, 2.4K	47-1000-72	1	R14
37	RES, 1/4W, 5%, 330	47-1000-51	1	R16
38	RES, 1/4W, 5%, 390	47-1000-53	8	R17-24
39	RES, 1/4W, 5%, 33K	47-1001-15	1	R28
40	RES, 1/4W, 5%, 51	47-1000-32	1	R5
41	RES, 1/4W, 5%, 270	47-1000-49	1	R6
42	RES, 1/4W, 5%, 510	47-1000-56	3	R8,9,10
43	RES, 1/4W, 5%, 2K	47-1000-70	1	R11

	<u>DESCRIPTION</u>	<u>PART NUMBER</u>	<u>QTY</u>	<u>REF. DESIGNATIONS</u>
44	INDUCTOR, 0.27MH	15-9000-01	1	L1
45	DIODE, 1N914	48-1002-01	2	CR1,2
46	DIODE, 1N5231B	48-1001-02	1	CR3
47	DIODE, 1N4001	48-1000-01	1	CR5
48	XISTOR, 2N6288	48-0004-01	1	Q1
49	DIODE, 1N4934	48-1003-01	1	CR4
50	CAP, 150-UF, 15V	15-0003-23	2	C3,7
51	CAP, 470-PF, 500V, CER	15-0000-24	1	C6
52	CAP, 6.8-UF, 16V	15-0003-19	2	C4,5
53	CAP, 22-UF, 15V, AXIAL	15-0003-25	2	C1,2
54	CAP, 120-PF, 500V	15-0001-14	1	C8
55	CAP, 0.1-UF, 50V	15-0000-50	63	C9-C71
56	EJECTOR, ENGRAVED	24-0002-19	1	
57	EJECTOR, BLANK	24-0001-01	1	
58	PIN, EJECTOR	91-3000-01	2	
59	SCREW, 4-40x3/8	98-0000-02	1	
60	NUT, HEX, SS, 4-40	98-3000-01	1	
61	WASHER, LOCK, SS, #4	98-2001-01	1	

**APPENDIX B**  
**MDC/E PARTS LIST**



**APPENDIX B**  
**MDC/E PARTS LIST**

	<u>DESCRIPTION</u>	<u>PART NUMBER</u>	<u>QTY</u>	<u>REF. DESIGNATIONS</u>
1	PCB, BLANK, REV.A.B	10-0050-01	1	
2	I.C., TL-497	33-0075-01	1	A33
3	I.C., 74LS241	33-0178-01	4	A57, 57, 61, 62
4	I.C., 74LS02	33-0046-01	3	A3, 19, 20
5	I.C., 74L04	33-0018-01	1	A4
6	I.C., 7406	33-0019-01	1	A53
7	I.C., 74LS00	33-0058-01	3	A2, 21, 22
8	I.C., 74LS10	33-0060-01	1	A18
9	I.C., 74LS243	33-0180-01	2	A59, 60
10	I.C., PROM.6306	33-0053-16	1	A24
11	I.C., 74LS299	33-0074-01	1	A58
12	I.C., Z-80 PIO, PS, 2.5MHZ	33-0057-01	1	A54
13	I.C., 74LS161	33-0071-01	4	A17, 34, 48, 55
14	I.C., 74LS51	33-0065-01	1	A35
15	I.C., 74LS32	33-0062-01	1	A49
16	I.C., 74LS74	33-0066-01	2	A36, 50
17	I.C., 74LS125	33-0067-01	1	A23
18	I.C., 9401	33-0042-01	1	A1
19	I.C., 74LS38	33-0064-01	1	A38
20	I.C., RAM	33-0049-00	24	A9-16, 25-32, 40-47
21	I.C., 74LS175	33-0072-01	1	A37
22	I.C., PROM, 7603	33-0164-02	1	A6
23				
24	I.C., 74157	33-0003-01	2	A7, 8
25	I.C., 74LS221	33-0073-01	1	A51
26	I.C., 74LS145	33-0181-01	1	A52
27	I.C., 74LS75	33-0100-01	1	A5
28	SOCKET, 40-PIN	21-1000-01	1	A54
29	SOCKET, 16-PIN	21-1000-02	27	A6, 9-16, 25-32, 40-4 24, J1
30	COMP. CARRIER	33-0173-22	1	J1
31	RES, NET, 220/330	47-0000-02	1	A39
32	RES, 1/2W, 0.27-OHM	47-2000-06	1	R1
33	RES, 1/4W, 5%, 9.1K	47-1001-02	1	R2
34	RES, 1/4W, 5%, 1K	47-1000-63	8	R3, 7, 12, 13, 25-27
35	RES, 1/4W, 5%, 220	47-1000-47	1	R4
36	RES, 1/4W, 5%, 2.4K	47-1000-72	1	R14
37	RES, 1/4W, 5%, 330	47-1000-51	1	R16
38	RES, 1/4W, 5%, 390	47-1000-53	8	R17-24
39	RES, 1/4W, 5%, 33K	47-1001-15	1	R28
40	RES, 1/4W, 5%, 51	47-1000-32	1	R5
41	RES, 1/4W, 5%, 270	47-1000-49	1	R6
42	RES, 1/4W, 5%, 510	47-1000-56	3	R8, 9, 10
43	RES, 1/4W, 5%, 2K	47-1000-70	1	R11

	<u>DESCRIPTION</u>	<u>PART NUMBER</u>	<u>QTY</u>	<u>REF. DESIGNATIONS</u>
44	INDUCTOR, 0.27MH	15-9000-01	1	L1
45	DIODE, 1N914	48-1002-01	2	CR1, 2
46	DIODE, 1N5231B	48-1001-02	1	CR3
47	DIODE, 1N4001	48-1000-01	1	CR5
48	XISTOR, 2N6288	48-0004-01	1	Q1
49	DIODE, 1N4934	48-1003-01	1	CR4
50	CAP, 150-UF, 15V	15-0003-23	2	C3, 7
51	CAP, 470-PF, 500V	15-0003-24	2	C6
52	CAP, 6.8-UF, 16V	15-0003-19	2	C4, 5
53	CAP, 22-UF, 15V, AXIAL	15-0003-25	1	C1
54	CAP, 120-PF, 500V	15-0001-14	1	C8
55	CAP, 0.1-UF, 50V, DIP.	15-0005-79	77	C9-85
	GUARD			
56	SCREW, 4-40	98-0000-01	1	
57	NUT, SELF-LOCKING	98-3005-01	1	
58	CONNECTOR, 50.PIN	21-5000-01	2	P1, 2
59	SCREW, 2-56X3/8	98-0011-02	4	
60	WASHER, 2-56	98-2003-01	4	
61	WASHER, LOCK	98-2001-06	4	
62	NUT, 2-56	98-3007-01	4	

**APPENDIX C**  
**MDC SIGNAL LIST**

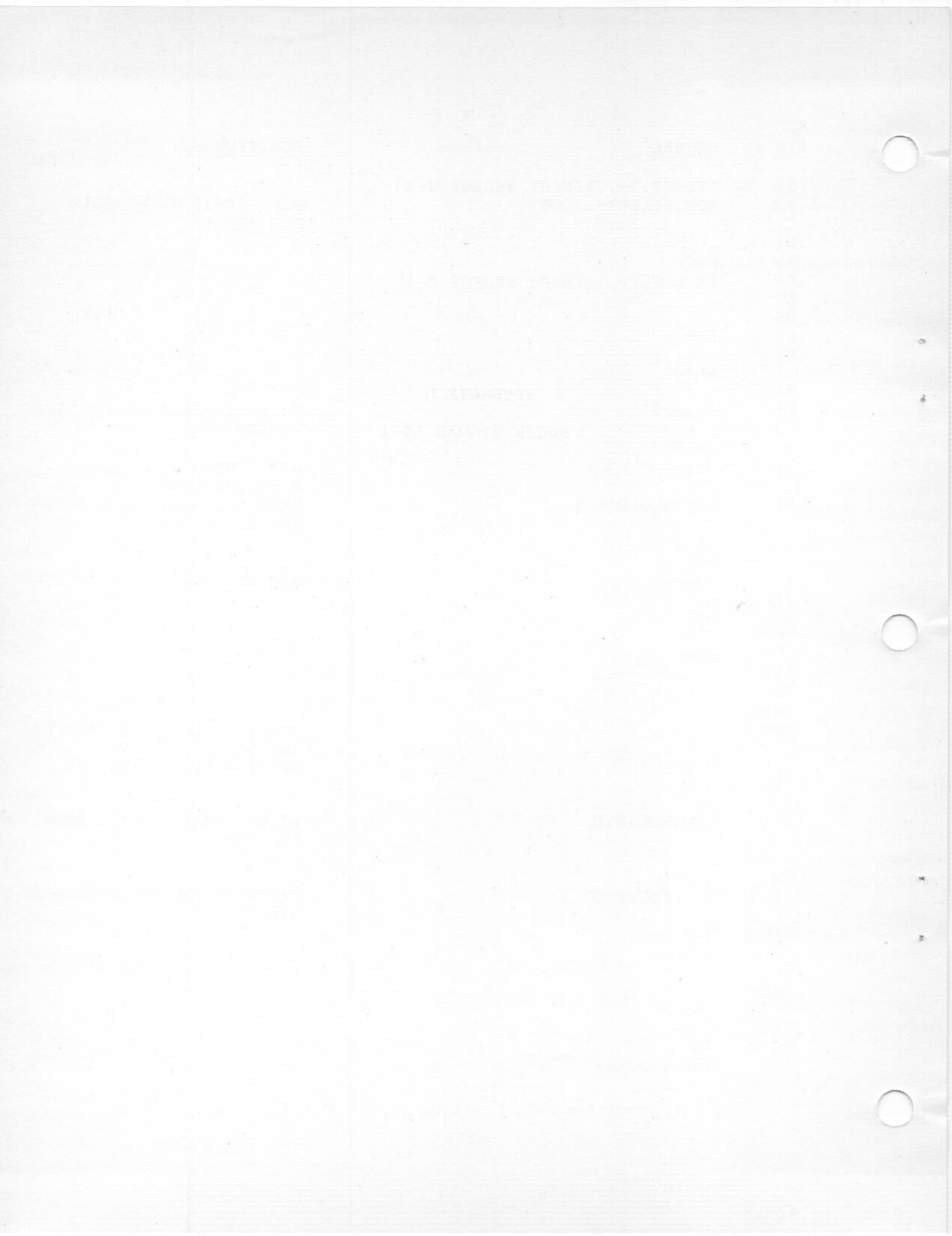


**APPENDIX C**  
**MDC SIGNAL LIST**

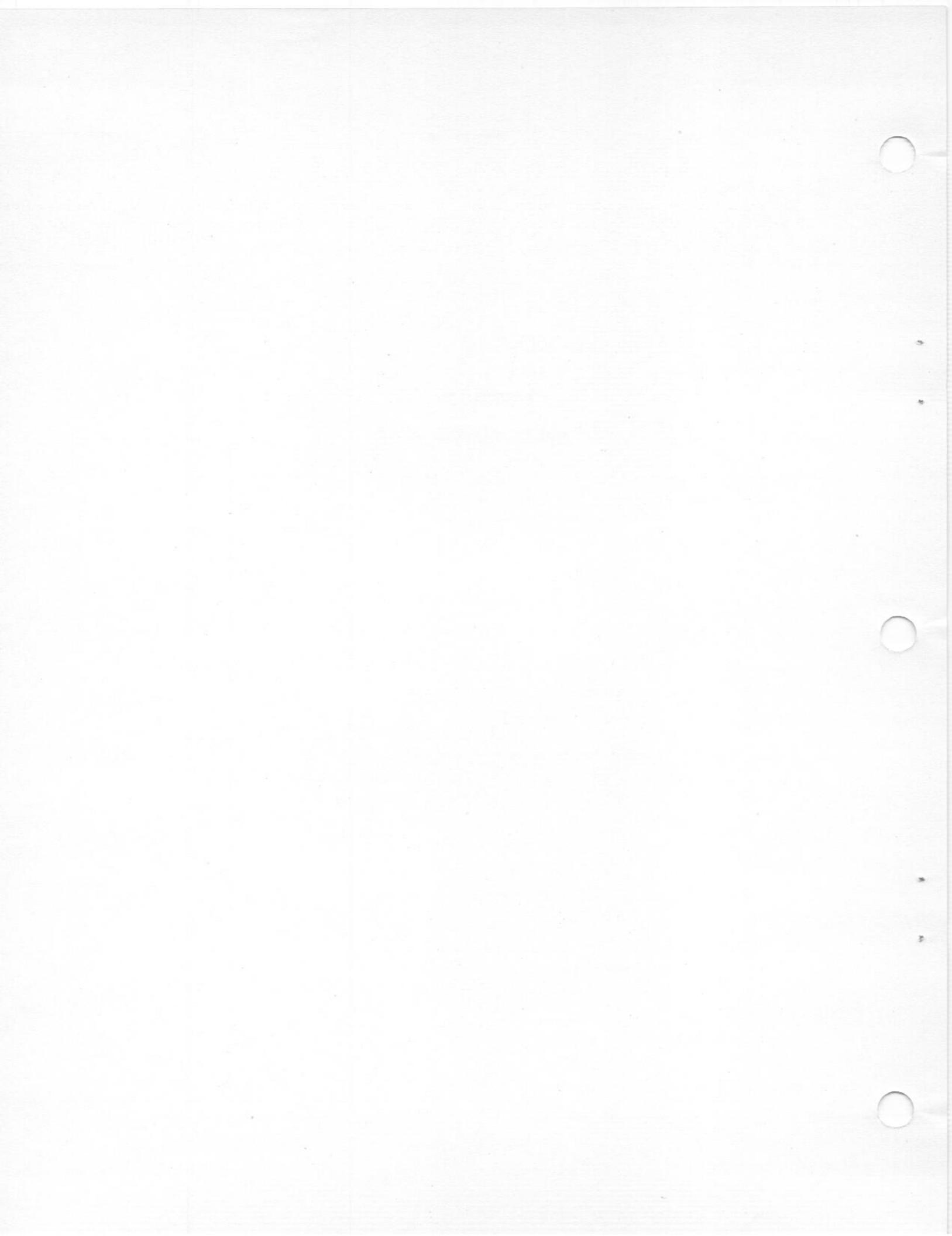
<u>MDC PIN #</u>	<u>SIGNAL NAME</u>	<u>FUNCTION</u>
1	+5V	VCC SUPPLY
2	+5V	
3	+5V	
4	IORQ-	
5	DB5	
6	.	
7	DR7-. (RADIAL SELECT 7-)	
8	DB3	
9	STEP-	
10	SELECT.3-. (BINARY SELECT : ENABLE-)	
11	WRITE.GATE-	
12	DB6	
13	DB0	
14	DR6-. (RADIAL SELECT 6-)	
15	DR5-. (RADIAL SELECT 5-)	
16	.	
17	DISK. (C/T.O)	COMPOSITE SECTOR AND INDEX MARKS
18	DR0-. (RADIAL SELECT 0-)	SYSTEM DISK RADIAL SELECT LINE
19	INDEX00-	SIGNAL TO MCB CTC FOR SECTOR TIMING
20	.	
21	.	
22	.	
23	WR-	
24	.	
25	.	
26	AB7	
27	AB8	
29	AB5	
30	AB6	
31	.	
32	AB15	
33	READY-	INDICATES INDEX MARKS & DOOR SHUT
34	DRIVE.PRESENT-	GND LINE ON DISK PULLS THIS LOW
35	RFSH-	
36	AB13	
37	AB11	
38	.	
39	.	

MDC	<u>PIN #</u>	<u>SIGNAL</u>	<u>FUNCTION</u>
	40	.	
	41	.	
	42	.	
	43	.	
	44	.	
	45	.	
	46	.	
	47	.	
	48	.	
	49	.	
	50	.	
	51	.	
	52	.	
	53	.	
	54	.	
	55	.	
	56	.	
	57	.	
	58	.	
	59	+5V	VCC SUPPLY
	60	+5V	
	61	+5V	
	62	GND	
	63	GND	
	64	GND	
	65	.	
	66	RAW.READ.DATA-	UNPROCESSED DATA FROM DISK
	67	TRACK.0-	INDICATES HEAD AT OUTER- MOST TRACK
	68	DB4	
	69	SPARE.OUT-	UNUSED PIO OUTPUT
	70	DIRECTION-	HIGH=OUT
	71	DB2	
	72	VIDEO.DISABLE-	DISABLES VIDEO DURING DISK ACCESS
	73	DB7	
	74	DR3-.(RADIAL SELECT 3-)	
	75	DB1	
	76	DR2-.(RADIAL SELECT 2-)	USER DISK RADIAL SELECT LINE
	77	ENCODED.WRITE.DATA-	FM ENCODED DATA TO DISK
	78	DR1-.(RADIAL SELECT 1-)	
	79	INT-	OPEN DRAIN SYSTEM INTER- RUPT LINE
	80	SELECT.1-.(BINARY SELECT 1-)	
	81	DR4-.(RADIAL SELECT 4-)	

MDC	<u>PIN #</u>	<u>SIGNAL</u>	<u>FUNCTION</u>
	82	SELECT.0-. (BINARY SELECT 0-)	
	83	ROM.SELECT-. (OUT)	MCB OUTPUT TO DISABLE MDC MEMORY
	84	.	
	85	MRQ-	
	86	SELECT.2-. (BINARY SELECT 2-)	
	87	.	
	88	.	
	89	AB9	
	90	.	
	91	AB10	
	92	.	
	93	8.PHI-	8X SYSTEM CLOCK FOR DISK TIMING
	94	AB14	
	95	SG3-	SUBGROUP 3 FOR DISK SYNCHRONIZATION
	96	WRITE.PROTECT-	INDICATES WRITE PROTECT TAB IS MISSING
	97	AB12	
	98	AB4	
	99	PHI-	SYSTEM CLOCK
	100	AB3	
	101	AB2	
	102	AB1	
	103	AB0	
	104	.	
	105	.	
	106	.	
	107	GP3-	GROUP 3 FOR DISK SYNCHRON- IZATION
	108	GP4-	MDC PIO GROUP DECODE
	109	.	
	110	.	
	111	IEO.MDC.PIO	DAISY CHAIN OUTPUT FROM MDC PIO
	112	.	
	113	.	
	114	IEI.MDC.PIO	DAISY CHAIN INPUT TO MDC PIO
	115	M1-	
	116	RD-	
	117	.	
	118	.	
	119	WAIT-	
	120	GND	
	121	GND	
	122	GND	



**APPENDIX D**  
**MDC/E SIGNAL LIST**



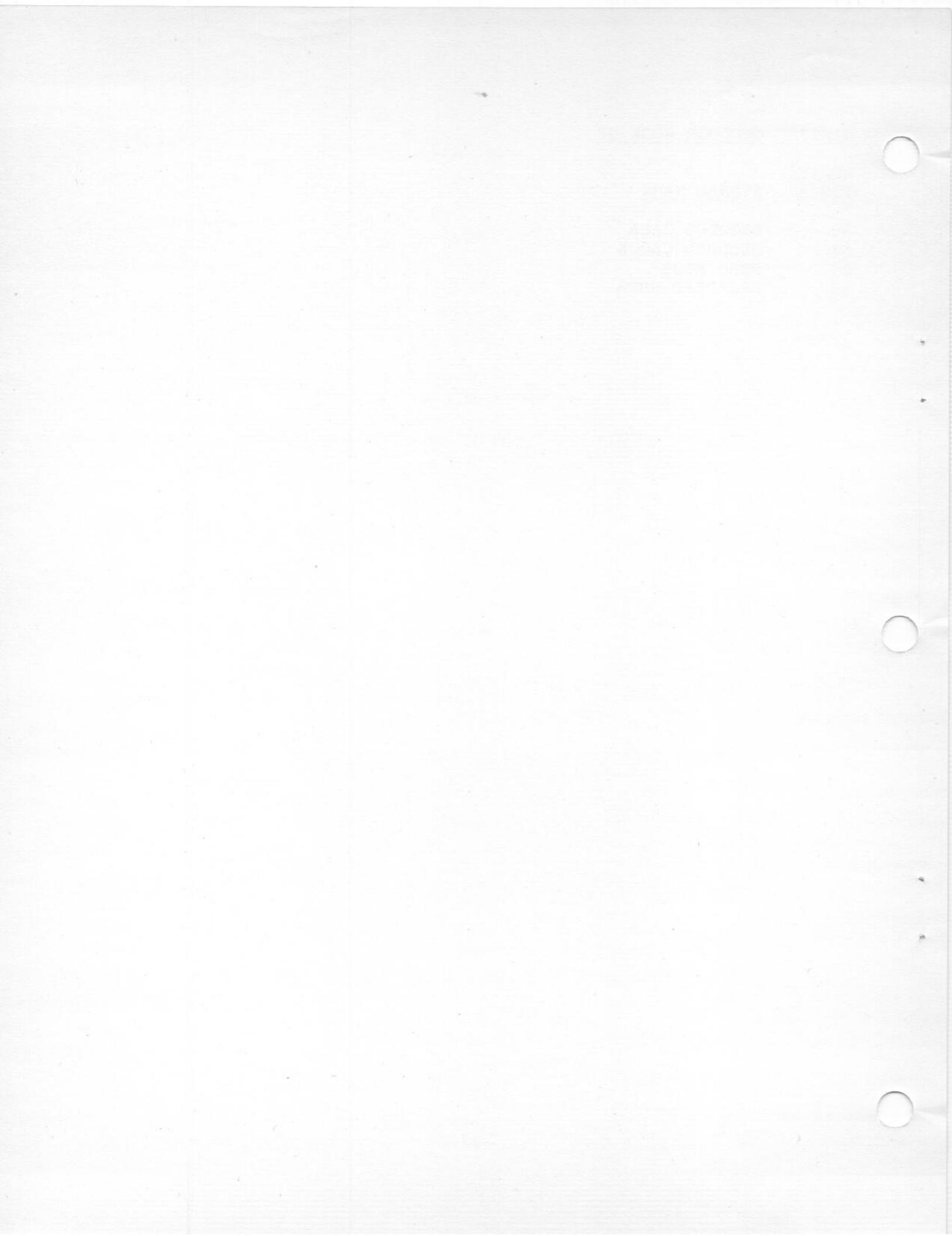
**APPENDIX D**  
**MDC/E SIGNAL LIST**

<u>MDC/E</u>	<u>PIN #</u>	<u>SIGNAL NAME</u>	<u>FUNCTION</u>
P1A1		+5V	VCC SUPPLY
P1A1		+5V	
P1A1		+5V	
P1C4		IORQ-	
P1A12		DBA	
P2A9		DR7-. (RADIAL SELECT 7-)	
P1A13		DB3	
P2C3		STEP-	
P2C12		SELECT.3-. (BINARY SELECT : ENABLE-)	
P2A3		WRITE.GATE-	
P1C26		DB6	
P1C28		DB0	
P2C9		DR6-. (RADIAL SELECT 6-)	
P2C10		DR5-. (RADIAL SELECT 5-)	
P2A2		DISK. (C/T.O.)	COMPOSITE SECTOR AND INDEX MARKS
P2C15		DRO-. (RADIAL SELECT 0-)	SYSTEM DISK RADIAL SELECT LINE
P2A4		INDEX00-	SIGNAL TO MCB CTC FOR SECTOR TIMING
P1A4		WR-	
P1A27		AB7	
P1C25		AB8	
P1A28		AB5	
P1C27		AB6	
P1A19		AB15	
P2C6		READY-	INDICATES INDEX MARKS AND DOOR SHUT
P2A7		DRIVE.PRESENT-	GND LINE ON DISK PULLS THIS LOW
P1A22		RFSH-	
P1C19		AB13	
P1A20		AB11	
P1C1		+5V	VCC SUPPLY
P1C1		+5V	
P1C1		+5V	
P1A32		GND	
P1A32		GND	
P1C32		GND	
P2C24		RAW.READ.DATA-	UNPROCESSED DATA FROM DISK
P2C5		TRACK.0-	INDICATES HEAD AT OUTER-MOST TRACK

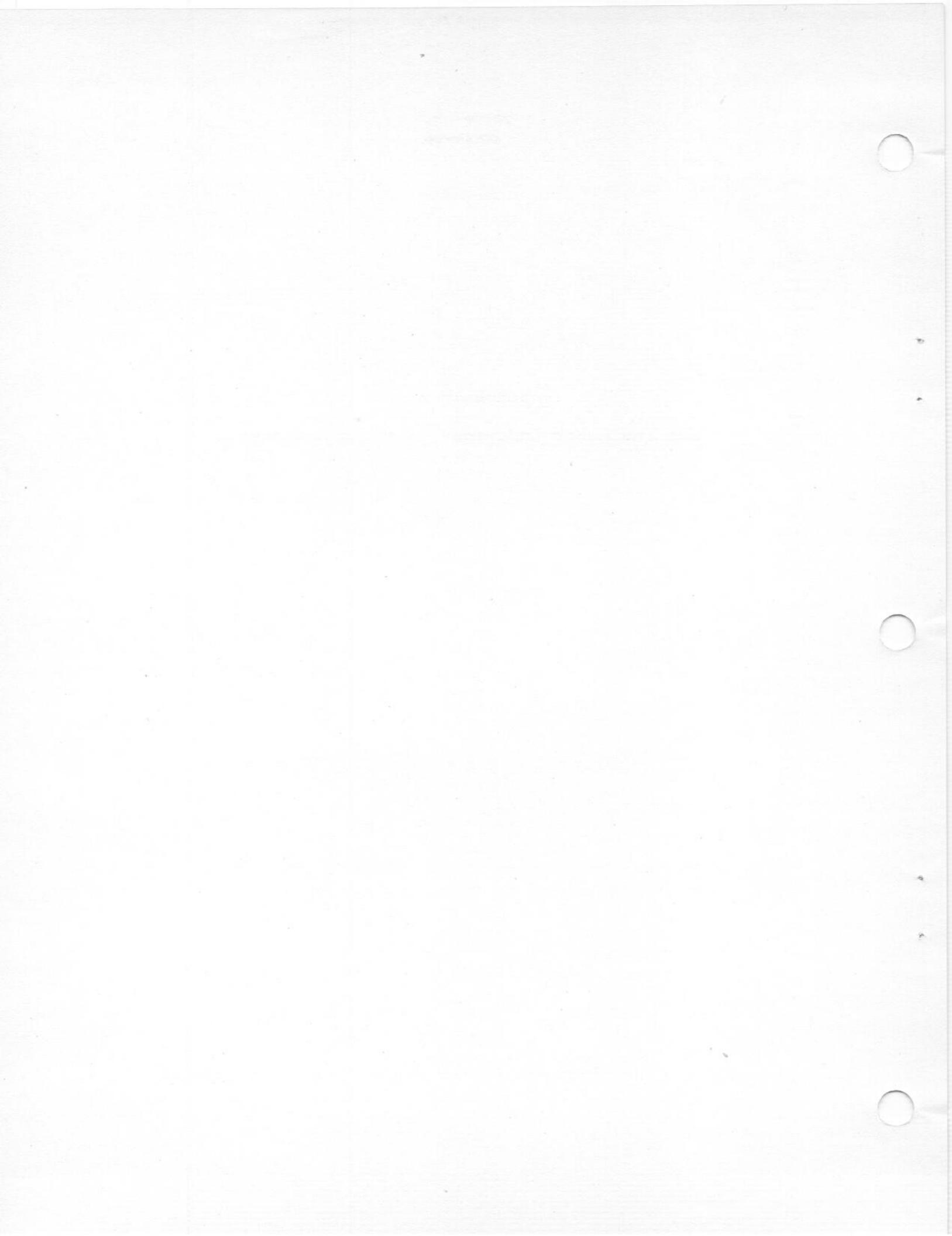
<u>MDC/E</u>	<u>PIN #</u>	<u>SIGNAL NAME</u>	<u>FUNCTION</u>
	P1C11	DB4	
	P2C7	SPARE.OUT-	UNUSED PIO OUTPUT
	P2C2	DIRECTION-	HIGH=OUT
	P1C13	DB2	
	P2C22	VIDEO.DISABLE-	DISABLES VIDEO DURING DISK ACCESS
	P1A26	DB7	
	P2C13	DR3-. (RADIAL SELECT 3-)	
	P1A29	DB1	
	P2A13	D42-. (RADIAL SELECT 2-)	USER DISK RADIAL SELECT LINE
	P2A8	ENCODED.WRITE.DATA-	FM ENCODED DATA TO DISK
	P2C14	DR1-. (RADIAL SELECT 1-)	
	P1C9	INT-	OPEN DRAIN SYSTEM INTERRUPT LINE
	P2A5	SELECT.1-. (BINARY SELECT 1-)	
	P2A10	DR4-. (RADIAL SELECT 4-)	
	P2C11	SELECT.0-. (BINARY SELECT 0-)	
	P1A18	MRQ-	
	P2A12	SELECT.2-. (BINARY SELECT 2-)	
	P1A25	AB9	
	P1C20	AB10	
	P1A30	8.PHI-	8X SYSTEM CLOCK FOR DISK TIMING
	P1C18	AB14	
	P2C23	SG3-	SUBGROUP 3 FOR DISK SYNCHRONIZATION
	P2C4	WRITE.PROTECT-	INDICATES WRITE PROTECT TAB IS MISSING
	P1C16	AB12	
	P1C24	AB4	
	P1C10	PHI-	SYSTEM CLOCK
	P1C23	AB3	
	P1C17	~B2	
	P1C14	AB1	
	P1A17	ABP	
	P2C26	GP3-	
	P2A25	GP4-	GROUP 3 FOR DISK SYNCHRONIZATION
	P2A6	IEO.MDC.PIO	MDC PIO GROUP DECODE DAISY CHAIN OUTPUT FROM MDC PIO
	P2A5	IEI.MDC.PIO	DAISY CHAIN INPUT TO MDC PIO
	P1C15	M1-	
	P1A5	RD-	
	P1A9	WAIT-	
	P2A1	GND	
	P2A1	GND	
	P2C1	GND	

DIGITAL DECODER HOOK-UP

<u>MDC/E</u>	
<u>PIN #</u>	<u>SIGNAL NAME</u>
50	DECODED DATA
52	DECODED CLOCK
54	READ MODE
65	RAW READ DATA



**APPENDIX E**  
**MDC COMPONENT LOCATION AND TRACE DIAGRAMS**



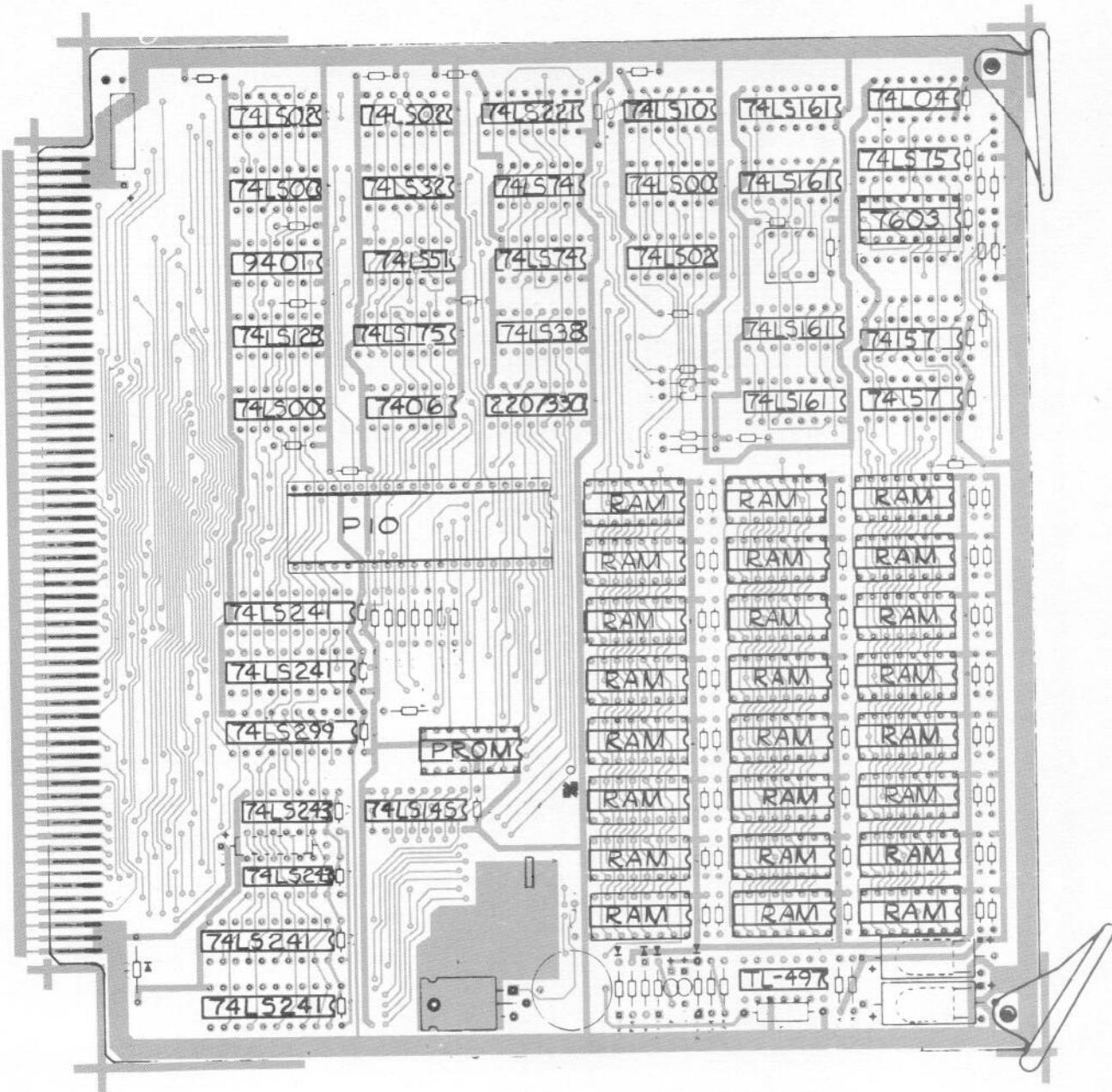


Figure E-1. MDC Printed Circuit Board, Component Location

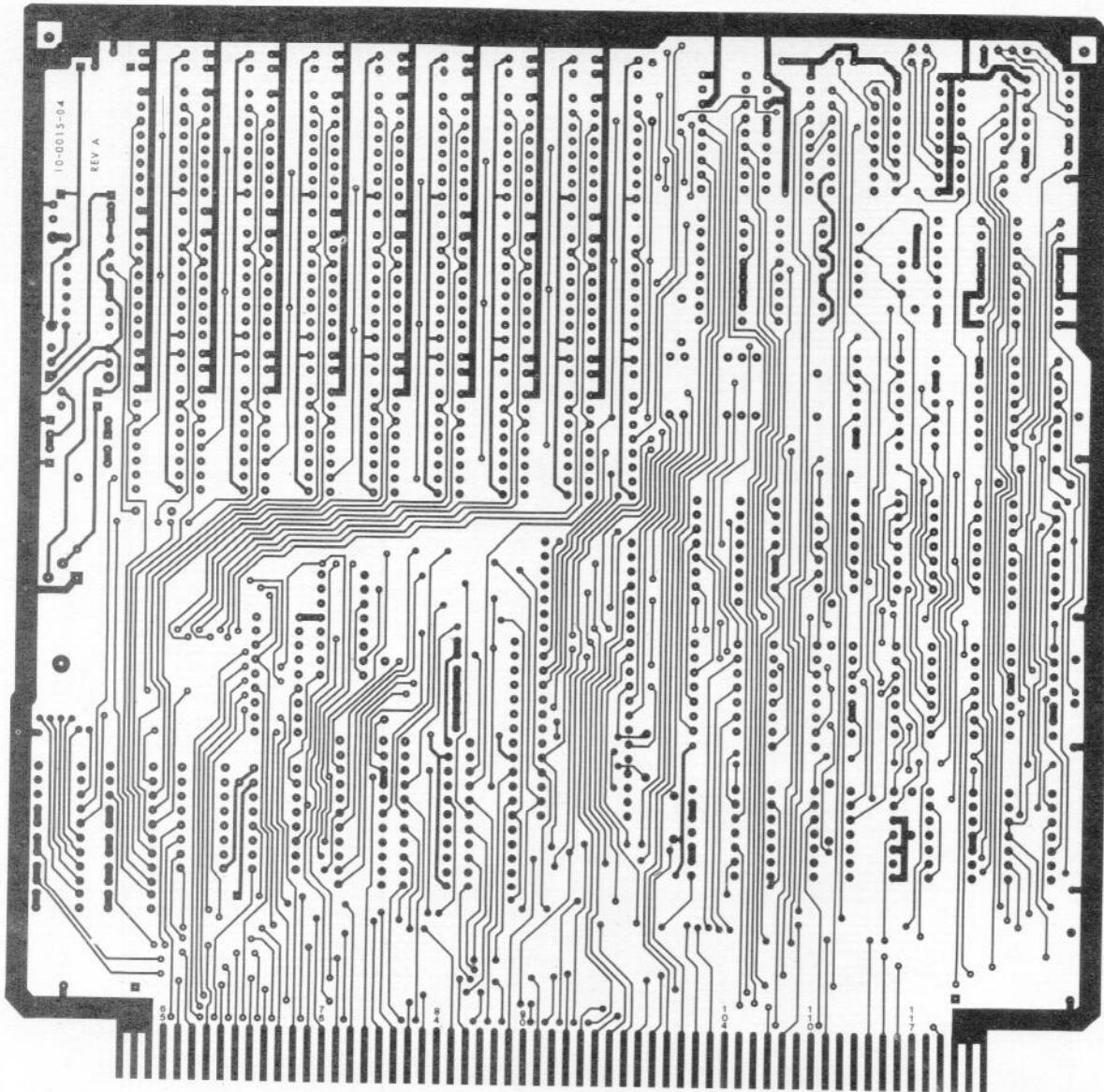
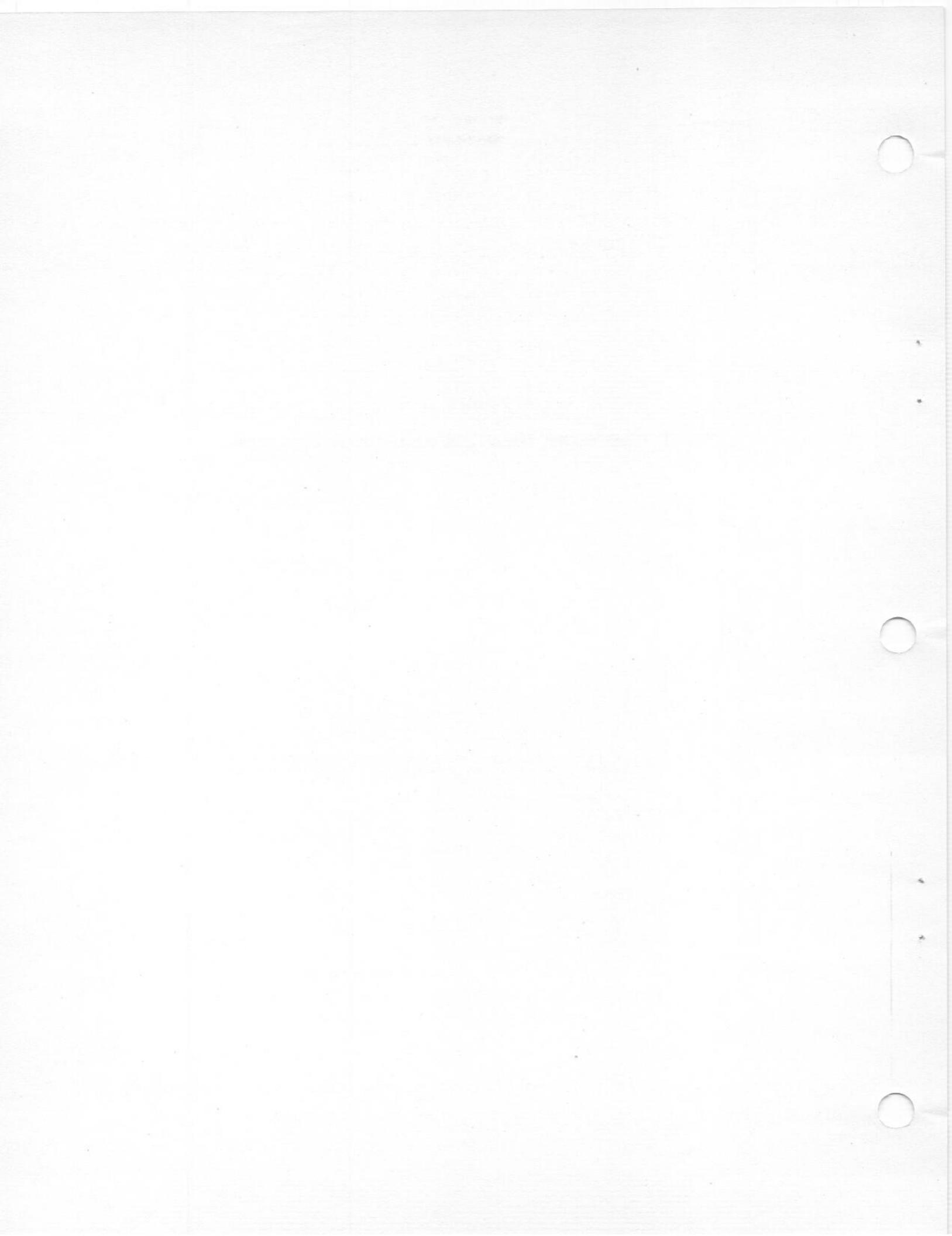


Figure E-2. MDC Printed Circuit Board, Solder Side Traces

**APPENDIX F**  
**MDC/E COMPONENT LOCATION AND TRACE DIAGRAMS**



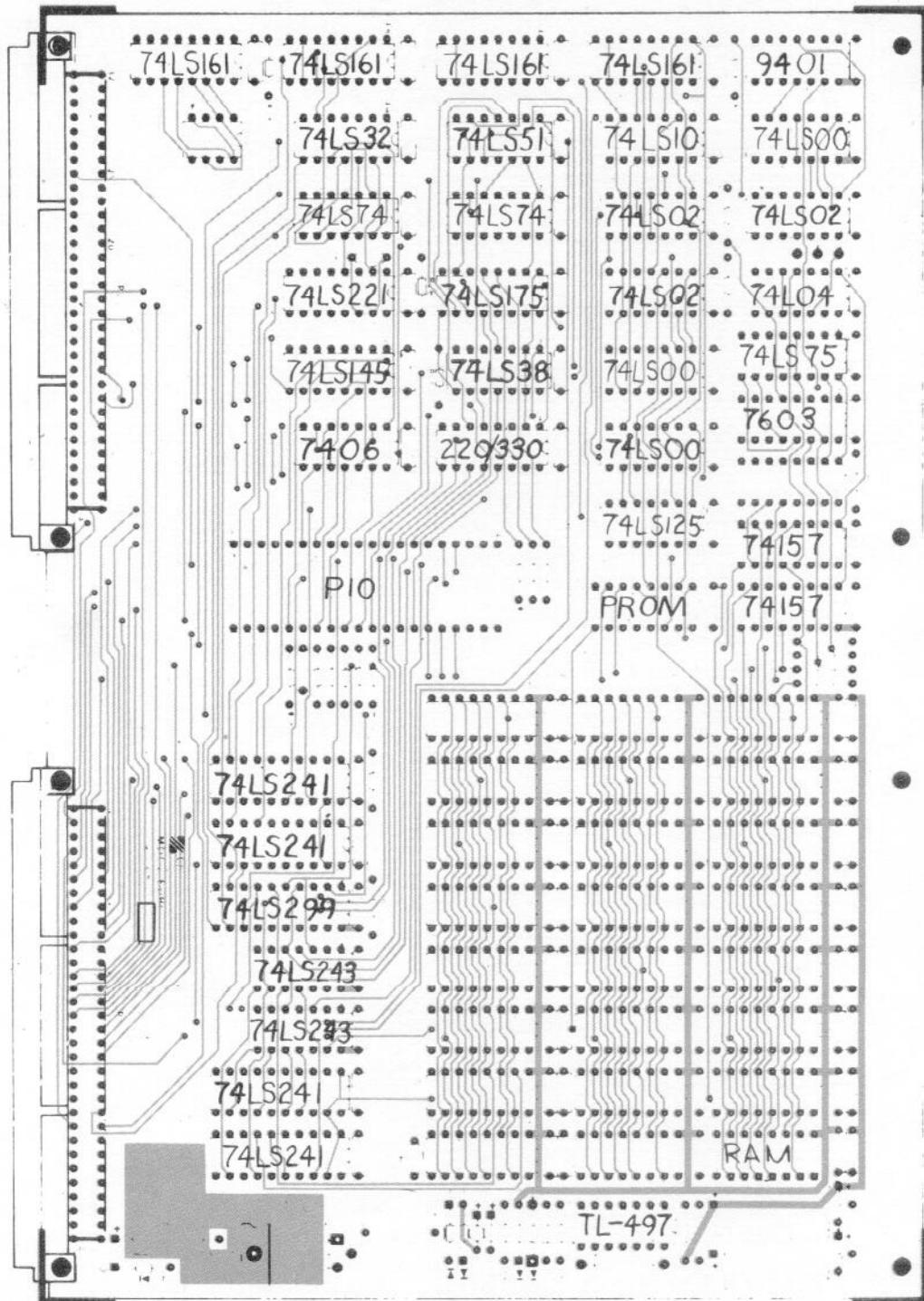


Figure F-1. MDC/E Printed Circuit Board, Component Location

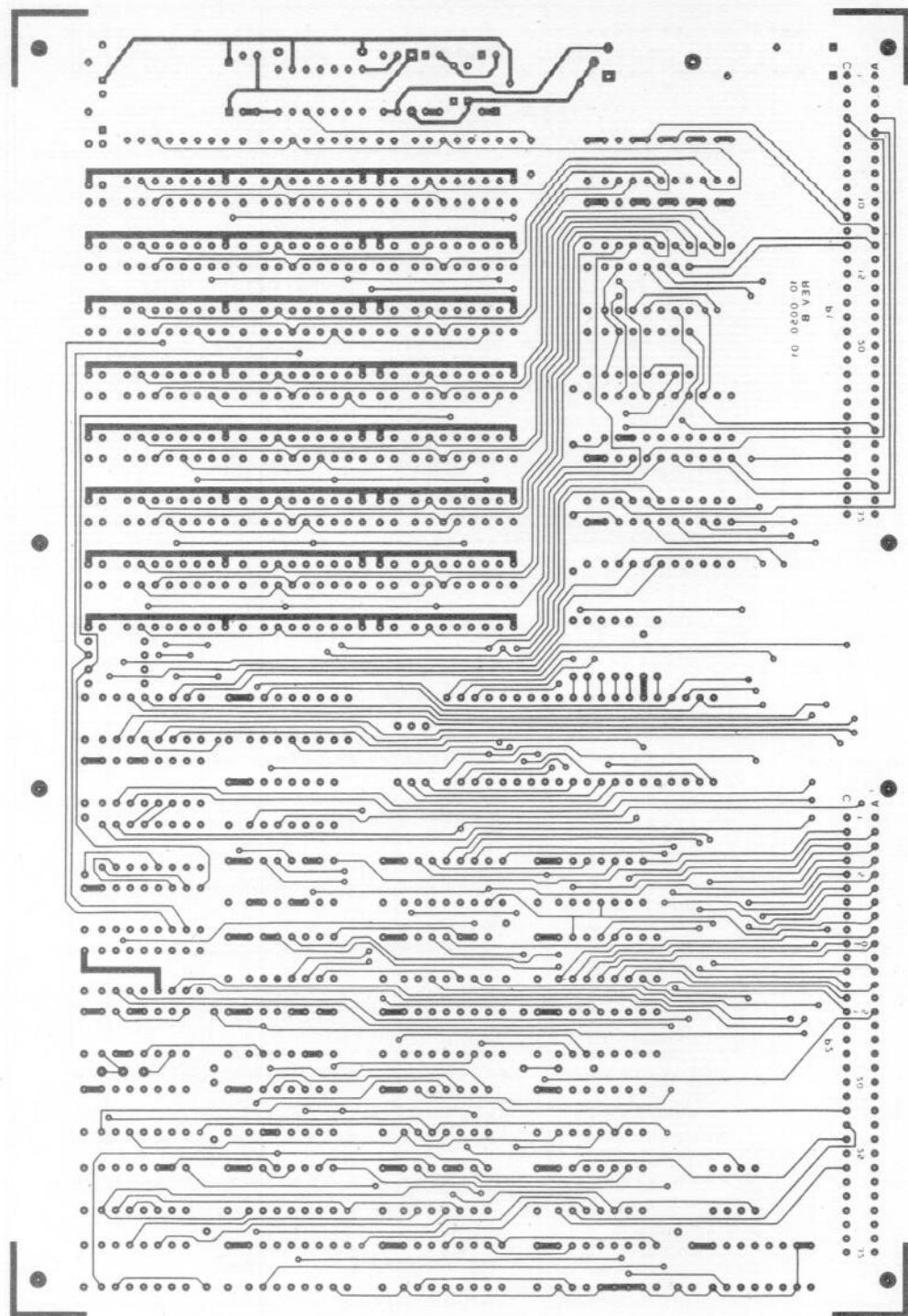
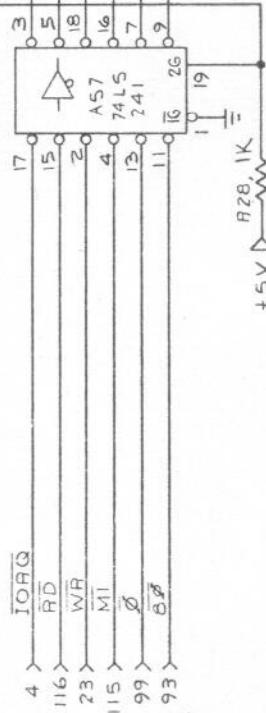
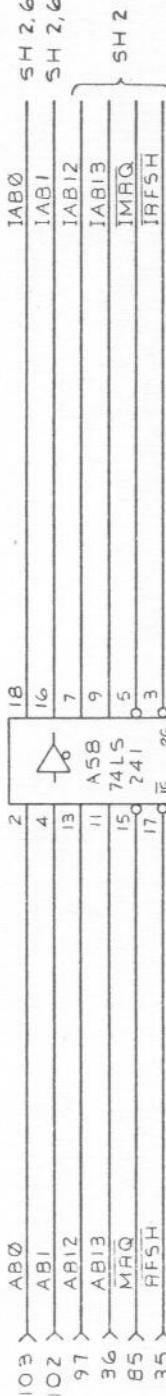
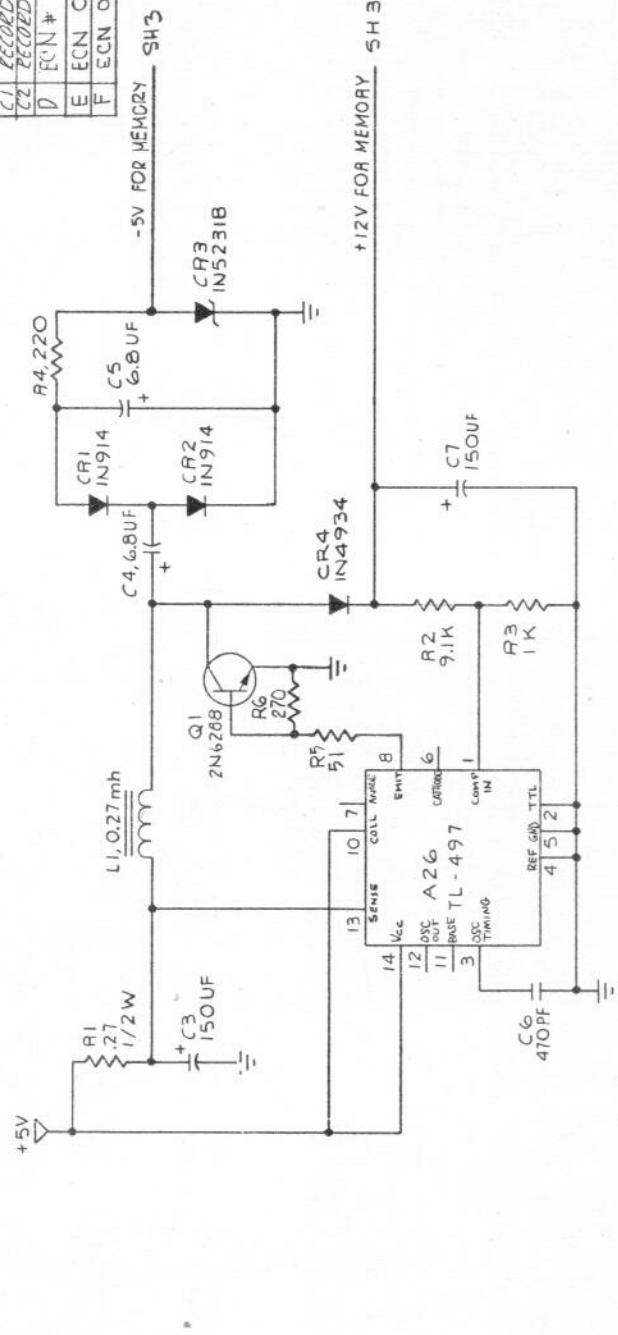


Figure F-2. MDC/E Printed Circuit Board, Solder Side Traces

**APPENDIX G**  
**MDC SCHEMATICS**



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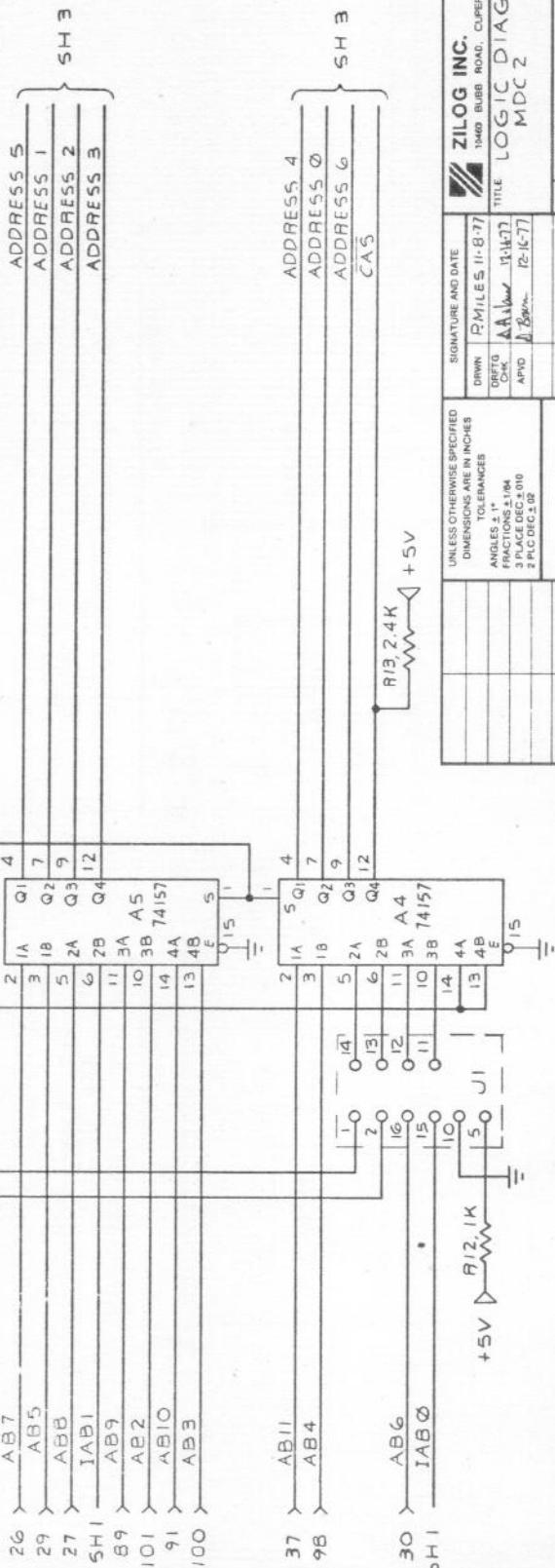
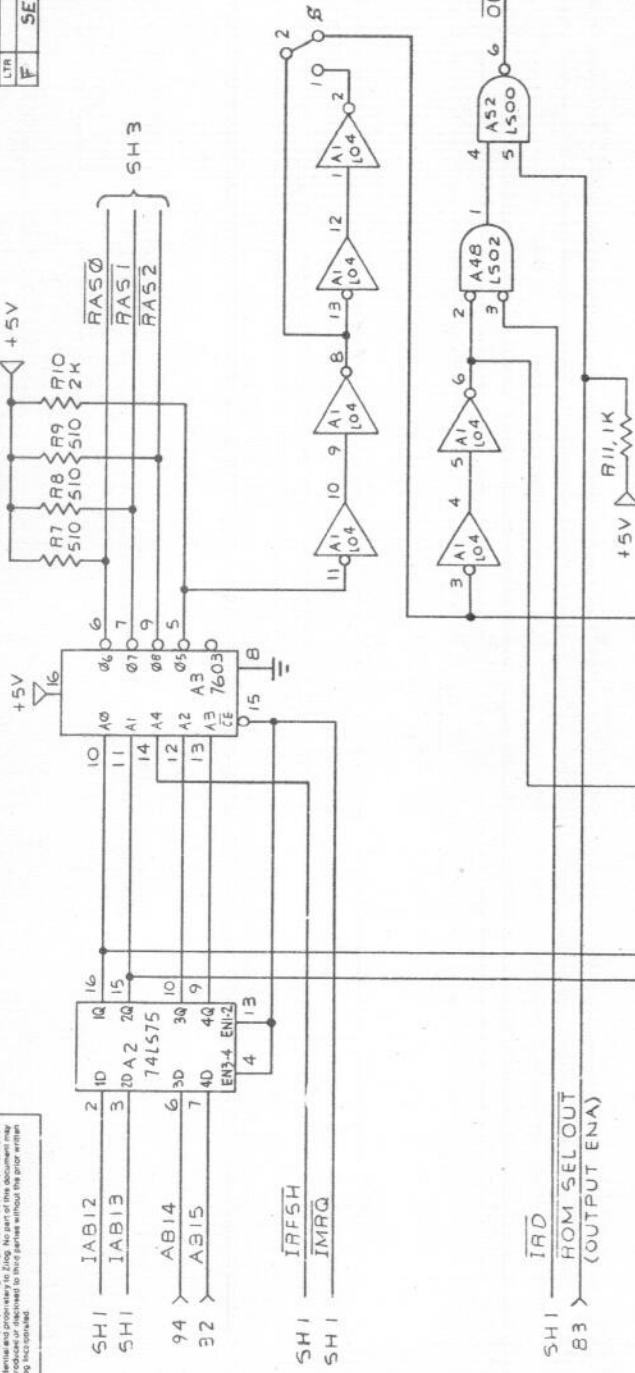


UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES		SIGNATURE AND DATE	ZILOG INC.	
ANGLES FRONT 45°, BACK 45° 3 PLACE DEC. ± .1 MM 2 PLACE DEC. ± .010 2 DEC. ± .002		DRAHN DEPT C DRAFTING APV/P 12-16-77 P-16-77	10460 BURB ROAD, CUPERTINO, CALIFORNIA 95014 TITLE LOGIC DIAGRAM MDC 2	ISSUE
			SIZE DRAWING NO. C	SD 1 OF 6
		FINISH	SCALE INCALTE	

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REVISIONS  
DESCRIPTION  
SEE SHEET

CTR DATE APPROVED  
F SEE SHEET 1 5-8-79 (2D)



SH1 IAB12	2	10	16	+5V
SH1 IAB13	3	11	17	
94 A814	6	12	18	R7 510
32 A915	7	13	19	R8 510
	8	14	20	R9 510
	9	15	21	R10 2K
	10	16	22	
	11	17	23	RAS0
	12	18	24	RAS1
	13	19	25	RAS2
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REVISONS

DESCRIPTION

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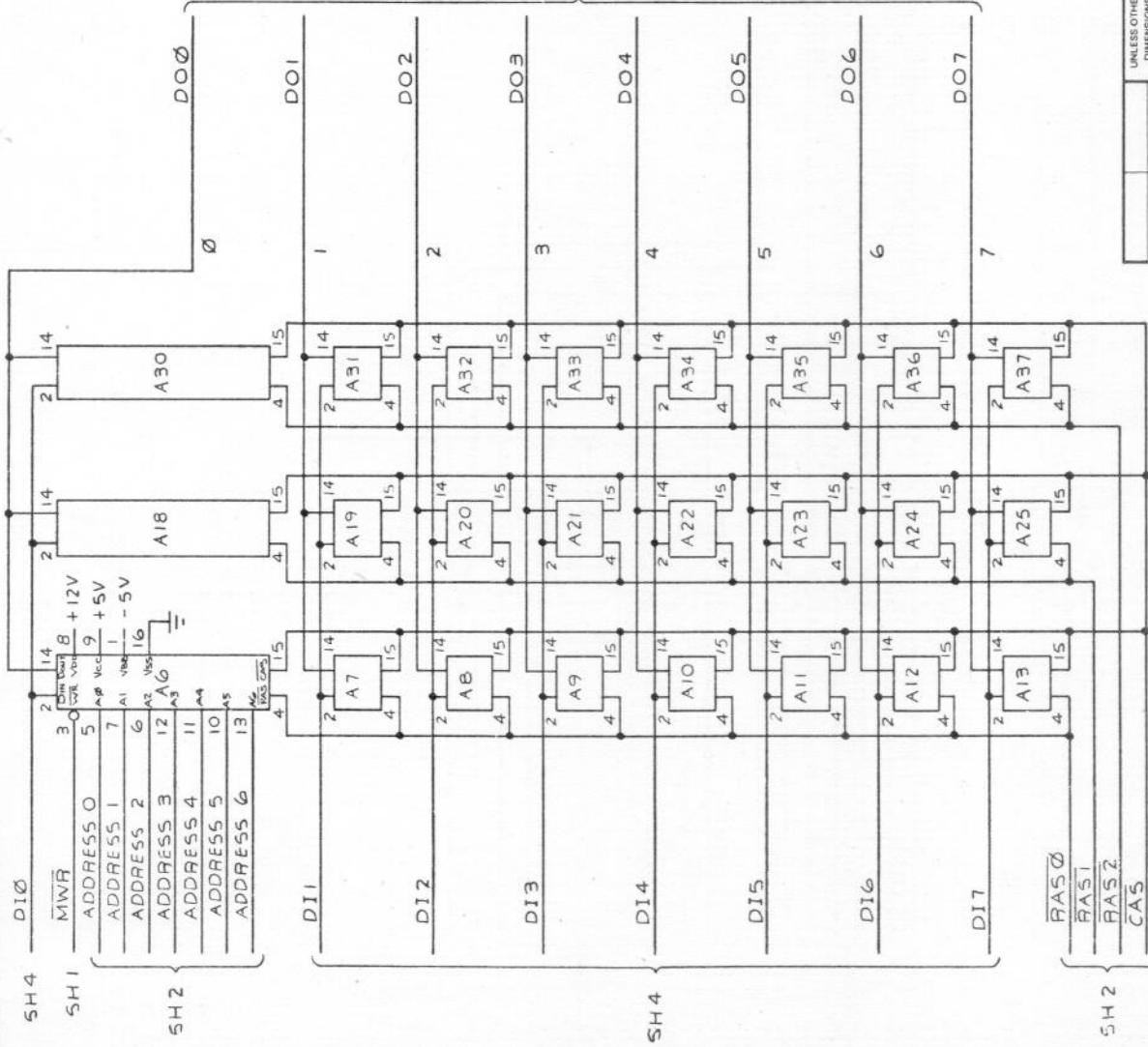
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NOTES:  
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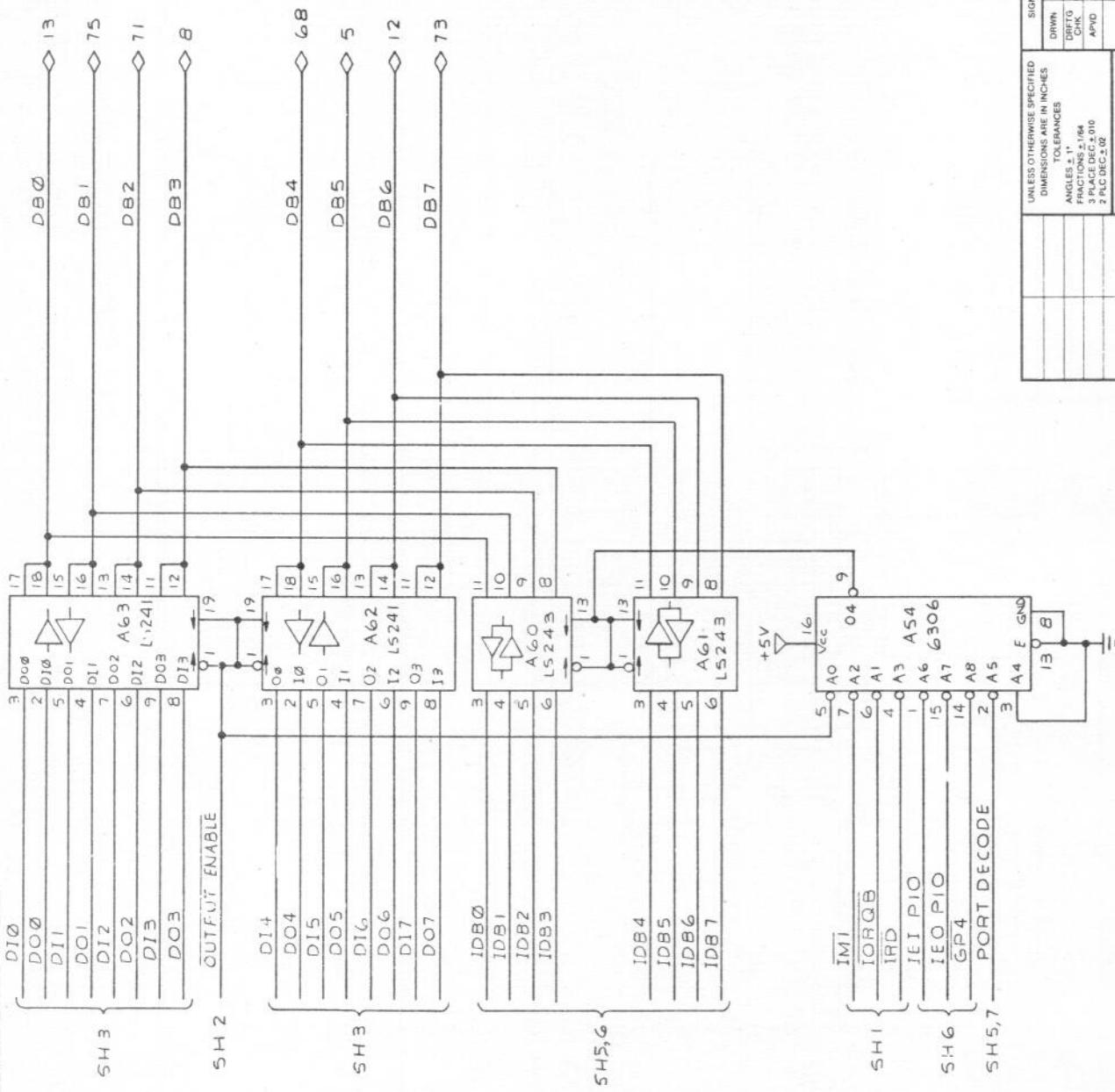
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ZILLOG INC.		SIGNATURE AND DATE
		DRAWN BY MILES H. BROWN 12-16-77
		DEPTG CHK APPROV
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		SIZE DRAWING NO. C FINISH
		NEUT ASY USED ON MATER
		APPLICATION
		SCALE _____
		NOTE D2 - 0015 - 04 F
		HEET 3 OF 8

UNLESS OTHERWISE SPECIFIED  
DIMENSIONS ARE IN INCHES  
ANGLES  $\pm 1^\circ$   
TOLERANCES  
FRACTIONS  $\frac{1}{16}$ ,  
3 PLACE DEC.  $.000$ ,  
4 PLACE DEC.  $.0000$

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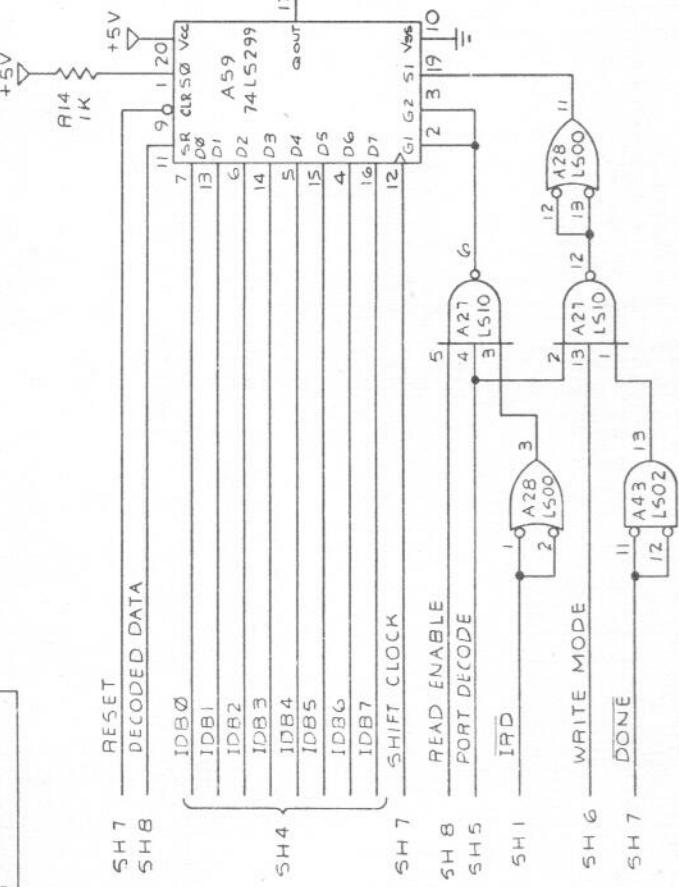
LTR	DESCRIPTION	REF ID: C-45	DATE	APPROVED
E	SEE SHT.		S.O. 79	ERD G.C.



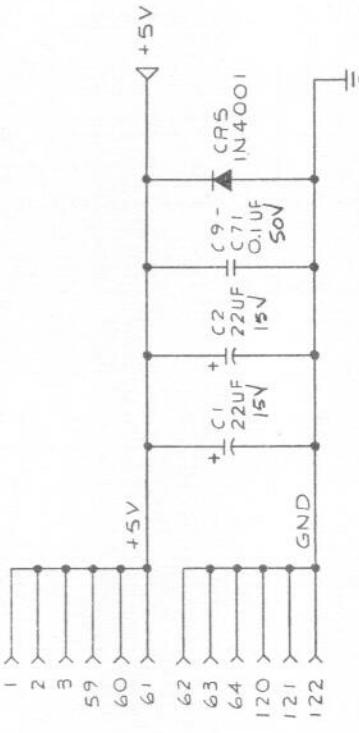
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES		<b>ZILOG INC.</b>	
ANGLES $\pm 1^\circ$ FRACTIONS $\pm 1/64$ 3 PLACE DEC. 2.010 2 PLC DEC. 2.02		10460 BUBB ROAD, CUPERTINO, CALIFORNIA 95014	REF ID:
DRFTG CIRK APD	12-41-1 12-4-77	TITLE <b>LOGIC DIAGRAM</b> <b>MDC2</b>	
		SIZE <b>C</b>	DRAWING NO <b>DZ-0015-04</b>
NEXT ASSY	USED ON	MATERIAL	FINISH

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LTR  
F SEE SH<sub>T</sub> I  
REVISIONS  
APPROVED  
DATE  
5.8.79 ERD



DISK DATA PORT: CF1c



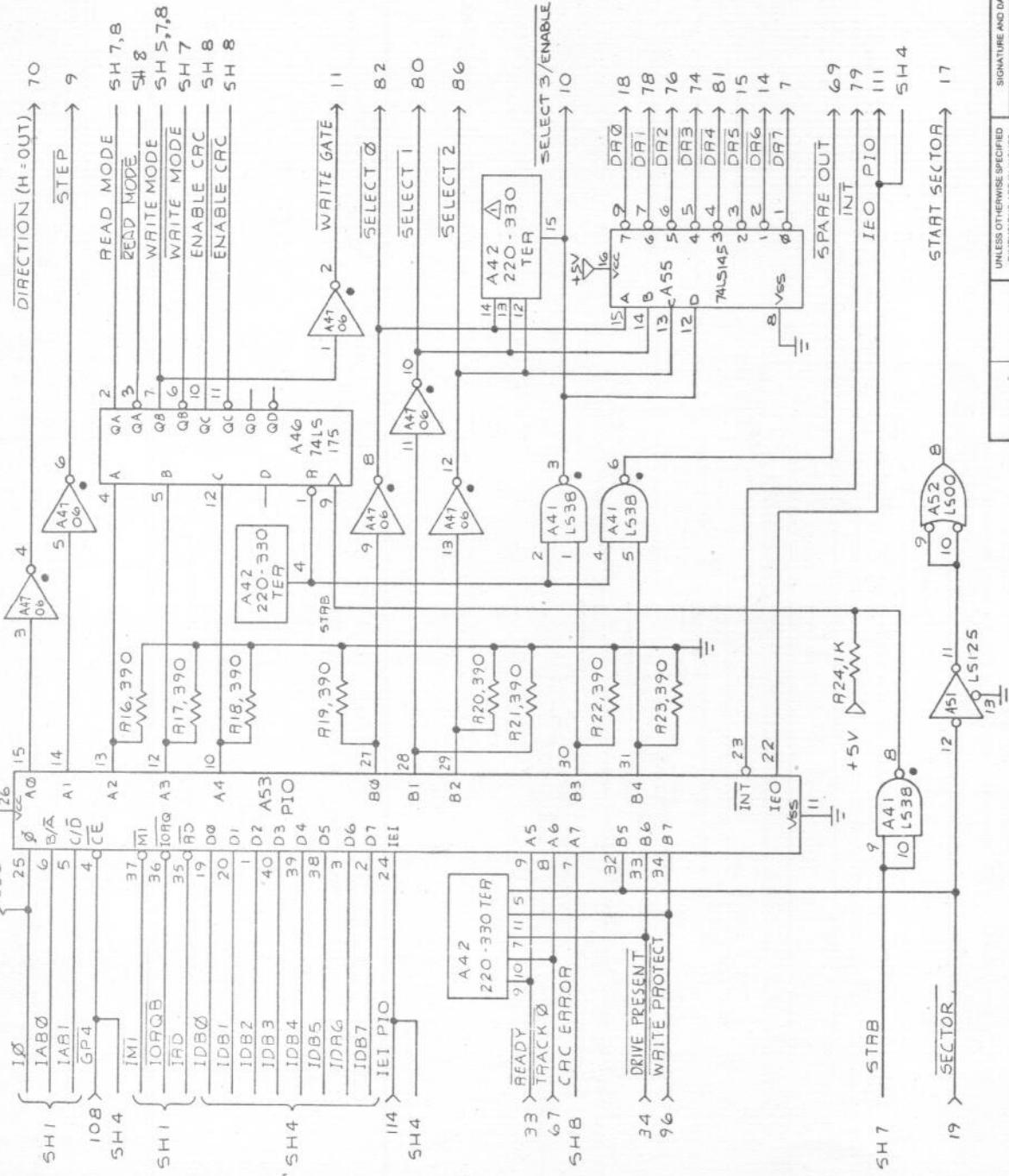
UNLESS OTHERWISE SPECIFIED		DIMENSIONS ARE IN INCHES	
		ANGLES $\pm 1^\circ$	
		FRACTIONS $\frac{1}{16}$ $\frac{1}{8}$ $\frac{1}{4}$ $\frac{3}{8}$ $\frac{5}{16}$ $\frac{1}{2}$ $\frac{7}{16}$ $\frac{9}{16}$	
		3 PLACE DEC. 0.010	
		2 PLAC DEC. 0.001	
DRAWING NO.		MILE 5	
DRAFTG CHK		11-11-11	
APPROV		A. Boppe [Signature]	
TITLE		LOGIC DIAGRAM	
SIZE		MDC 2	
DRAWING NO.		C	
FINISH		NOTE	
NEXT ASSN		USED ON	
APPLICATION		SCALE	
		SHEET 5 OF 8	

**ZILOG INC.**  
1040 BUBB ROAD, CUPERTINO, CALIFORNIA 95014  
LOGIC DIAGRAM  
MDC 2

C D2 - CO 5 - O4 F

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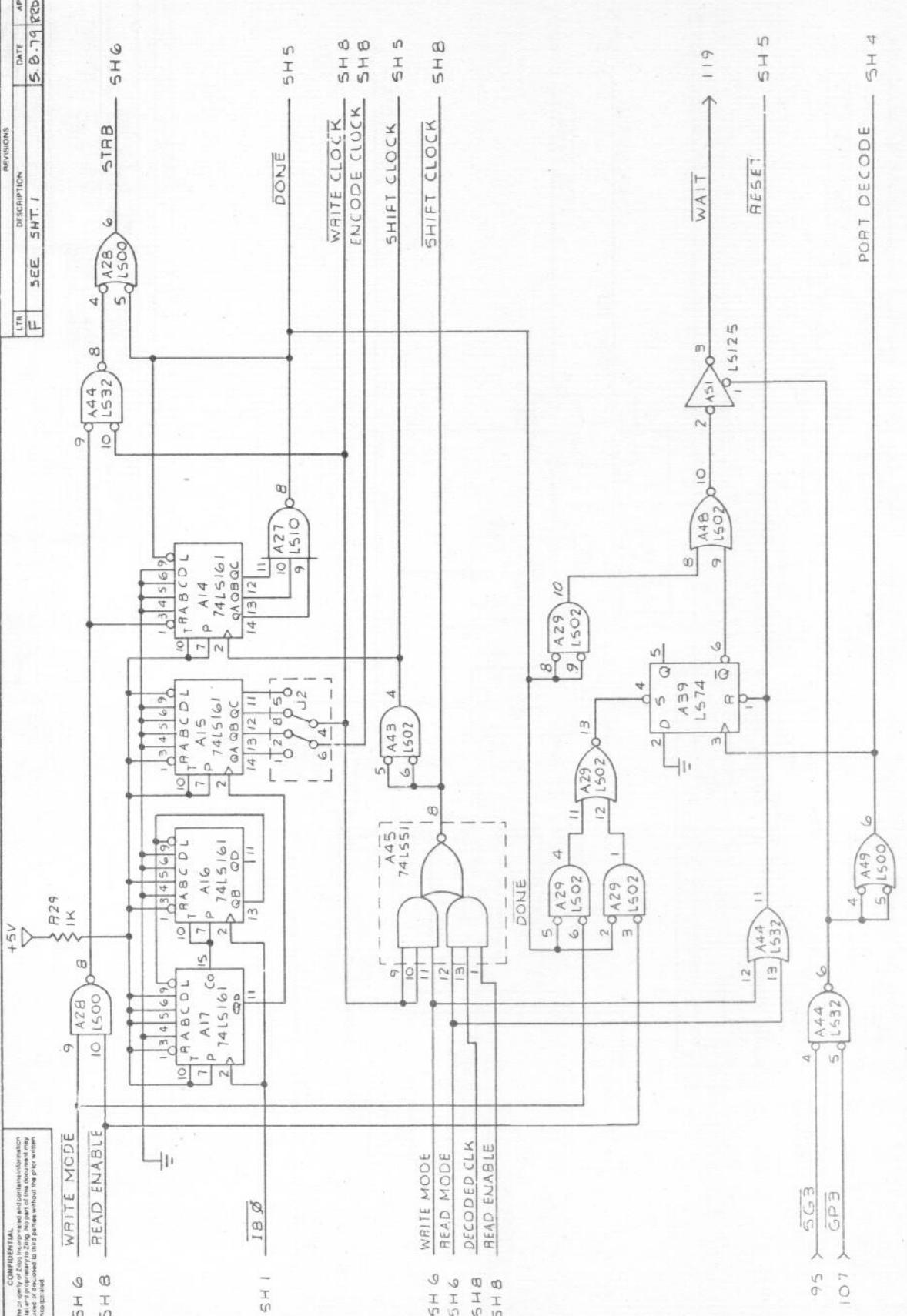
LTR	DESCRIPTION	REVISIONS	DATE	APPROVED
F	SEE SHT. I		5-8-79	R2D C



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REVISIONS

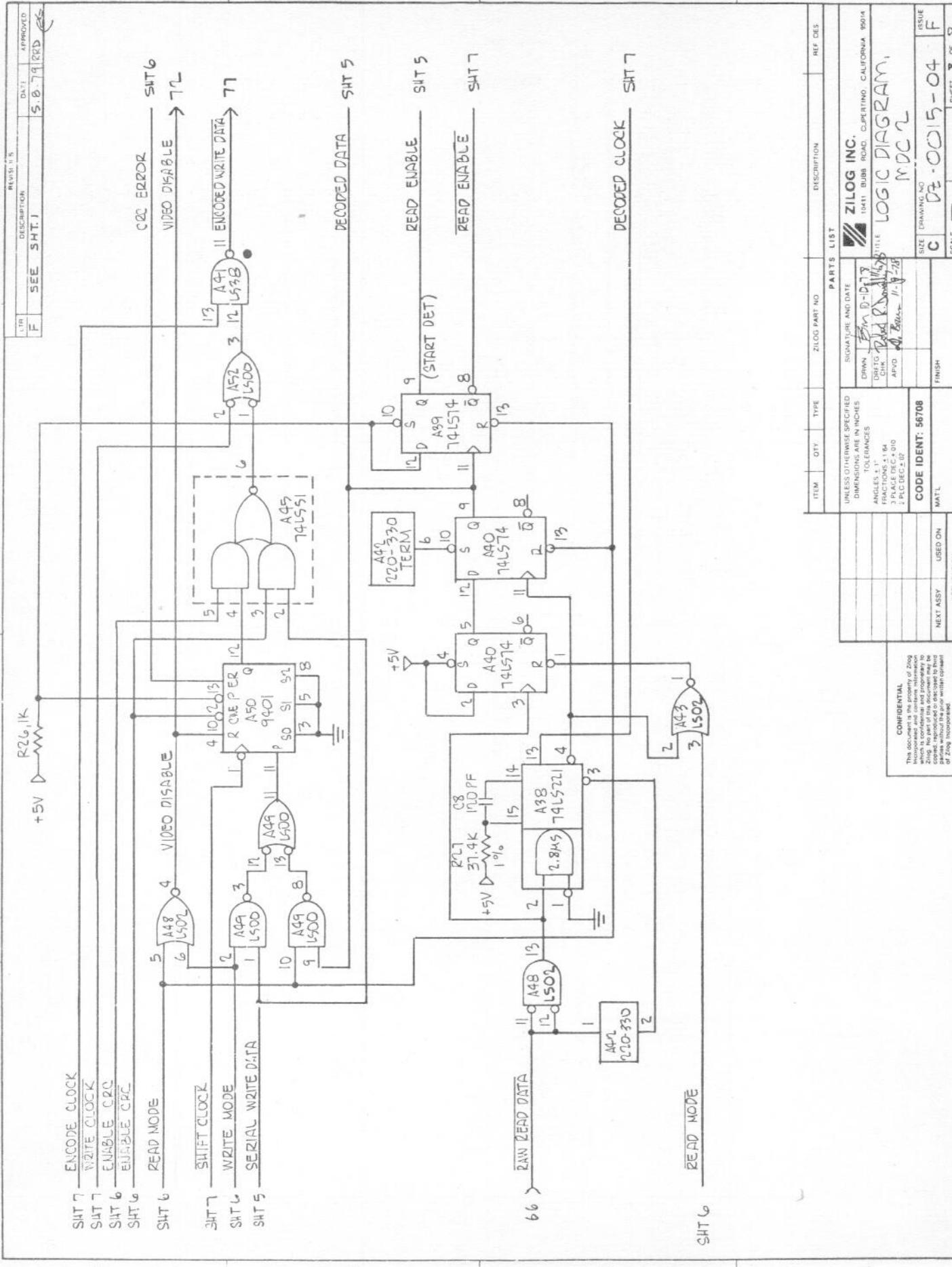
LTR	DESCRIPTION	DATE
F	SEE SHT. I	5.0.79 REC'D



DATA RATE = 517.3 KBS	1-6, 2-4
DATA RATE = 258.7 KBS	2-6, 8-4
DATA RATE = 129.3 KBS	8-6, 5-4
NOTE: FOR RATES OTHER THAN 258.7 KBS THE C OF THE DATA SEPARATOR (SHT 8) MUST BE CHANGED	

SIGNATURE AND DATE	
DRWNSH P. MILES	12/1/77
TELEGS CMK	12/1/77
APVO J. Bremm	12/1/77
TITLE LOGIC DIAGRAM MDC2	
SIZE DRAWING NO	C D2 - 0015 - 04
SCALE	1:1
APPLICABILITY	
NEXT ASSY	USED ON
MATERIAL	FINISH
SHEET 7 OF 8	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	
ANGLES: +1°/-0°	FRAC TOL: 1/16
3 PLACE DEC: 0.00	2 PLAC DEC: 0.00
ZILOG INC. 1000 BLDG ROAD, CUPERTINO, CALIFORNIA 95014	



1

2

3

4

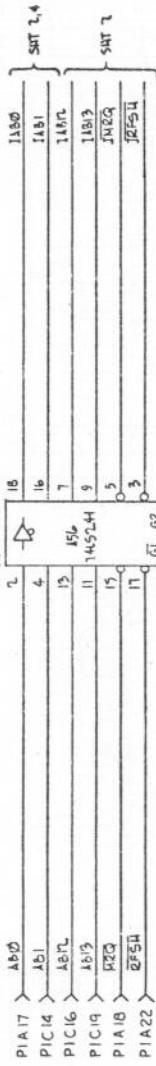
1

**APPENDIX H**  
**MDC/E SCHEMATICS**

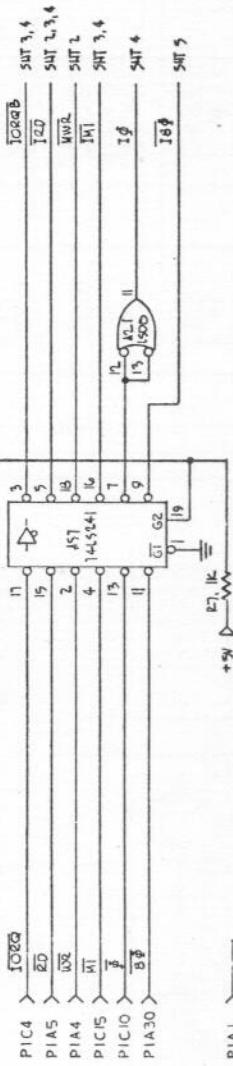


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Revision		Date	
A	ECN 00415	3-78	A
B		9-16-75	TEP

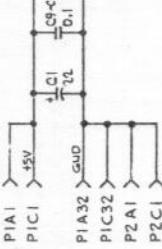


Z80



NOTES:

1. UNLESS OTHER SPECIFIED:  
RESISTORS ARE CARBON, %W, 1%.  
CAPACITORS ARE IN MICROFARADS.
2. 10-115, 115-151, 140-180 TO BE WIRED TIP TO 19.



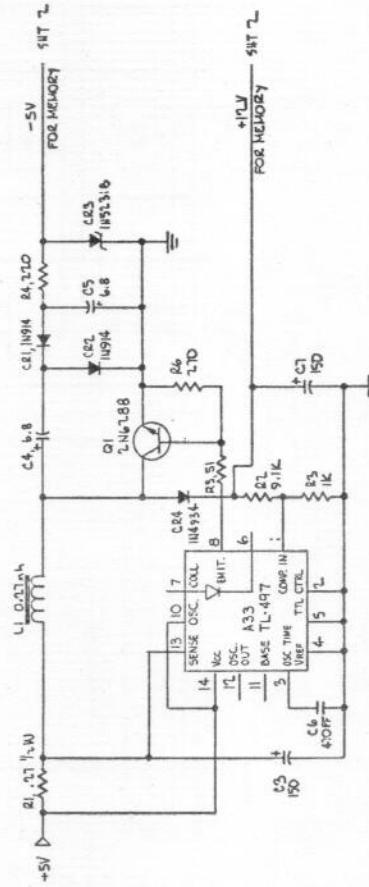
NOTES:

1. UNLESS OTHER SPECIFIED:  
RESISTORS ARE CARBON, %W, 1%.  
CAPACITORS ARE IN MICROFARADS.
2. 10-115, 115-151, 140-180 TO BE WIRED TIP TO 19.

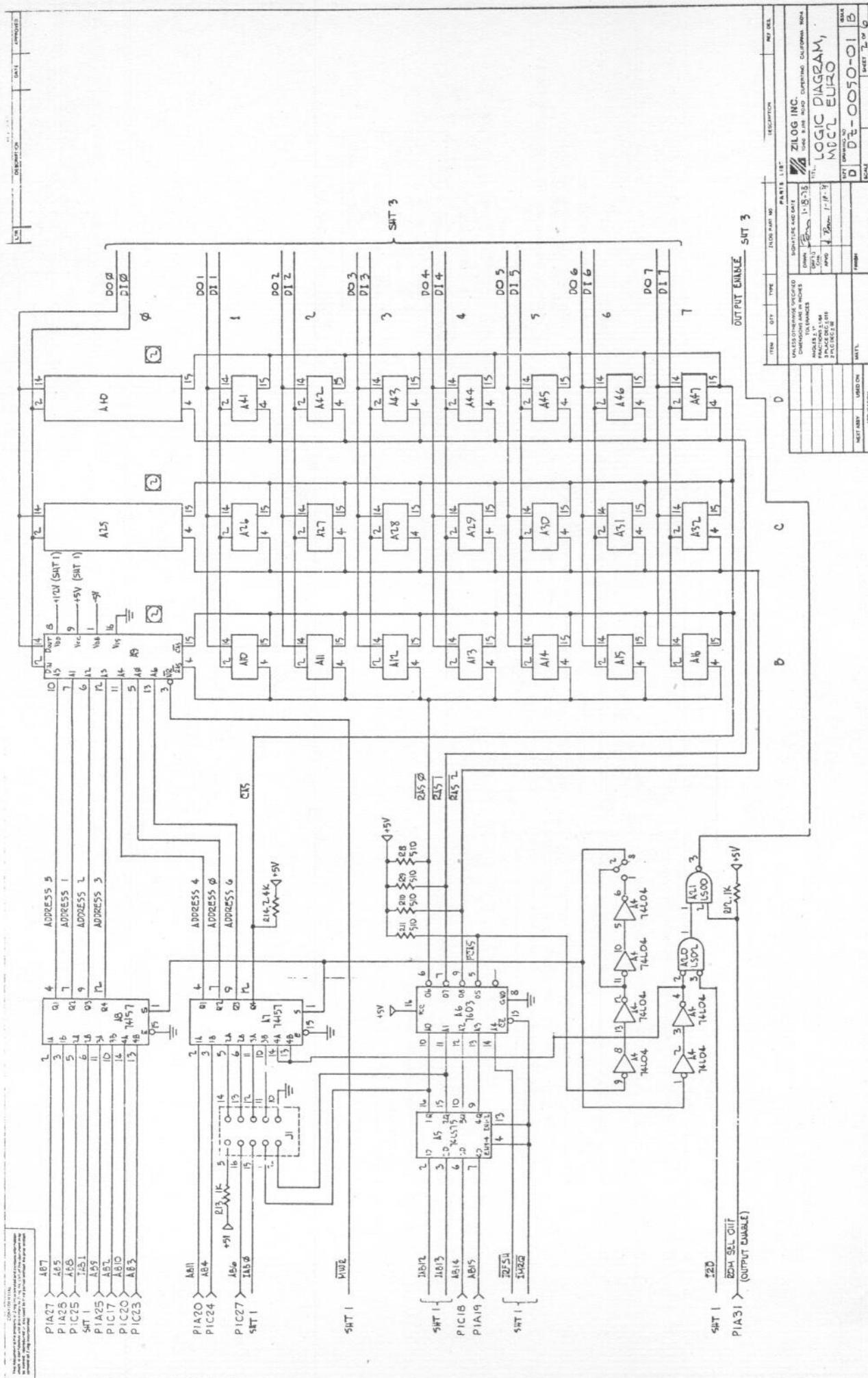
NOTES:

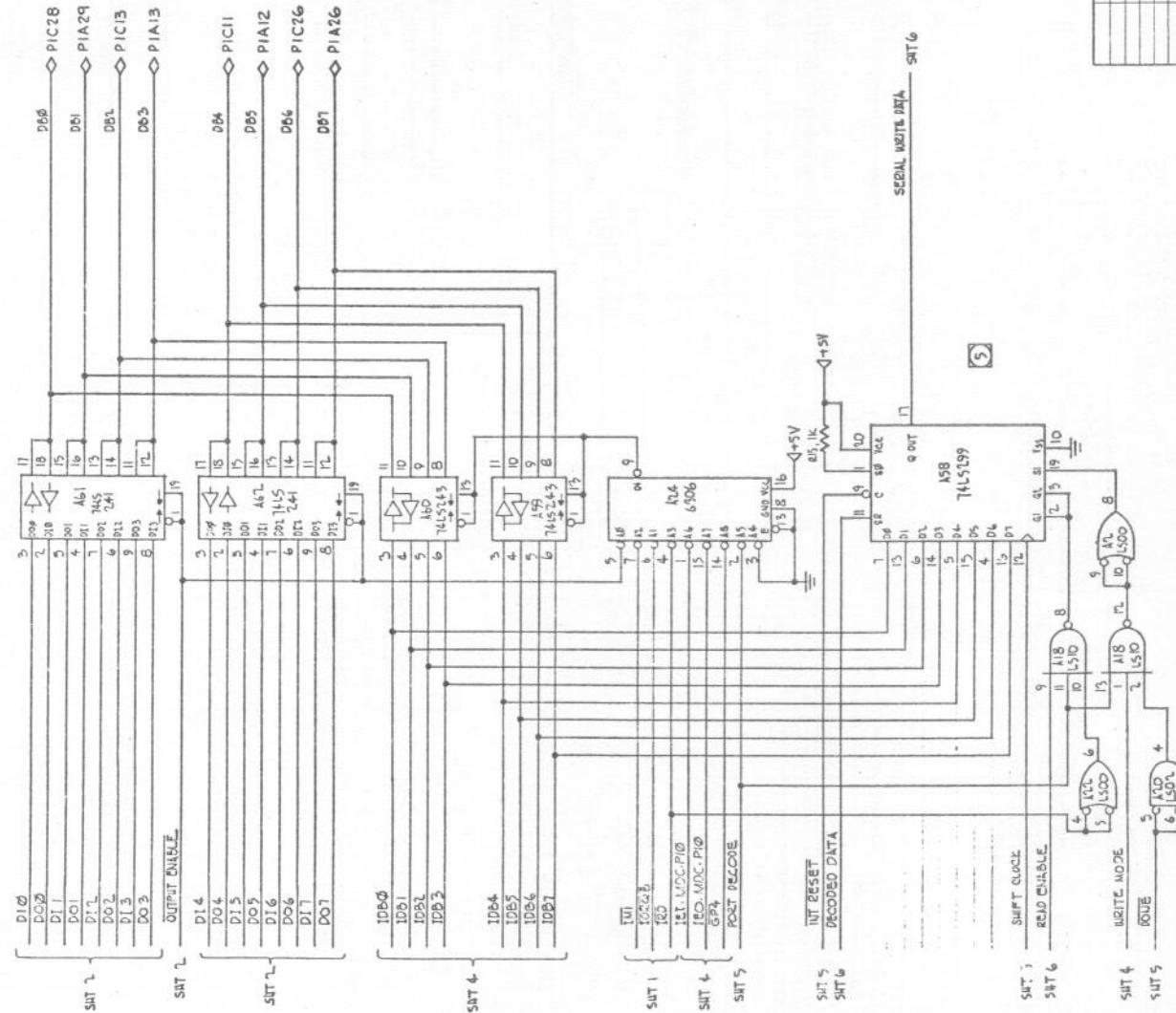
1. UNLESS OTHER SPECIFIED:  
RESISTORS ARE CARBON, %W, 1%.  
CAPACITORS ARE IN MICROFARADS.
2. 10-115, 115-151, 140-180 TO BE WIRED TIP TO 19.

3. PIO PORTS  
A DATA - D0-16  
B CONTROL - D1-16  
C DATA - D2-16  
D CONTROL - D3-16
4.  $\phi_0 = 15.6608 \text{ MHz}$   
DATA RATE 511.3 kbs | -4, -5, -6  
DATA RATE 219.1 kbs | -7, -8, -9  
DATA RATE 109.5 kbs | -10, -11, -12  
FOR RATES OTHER THAN  
15.61 KBS THE DC OF THE DATA  
SEPARATOR (S1116) MUST BE CHANGED
5. DISK DATA PORT = CF16

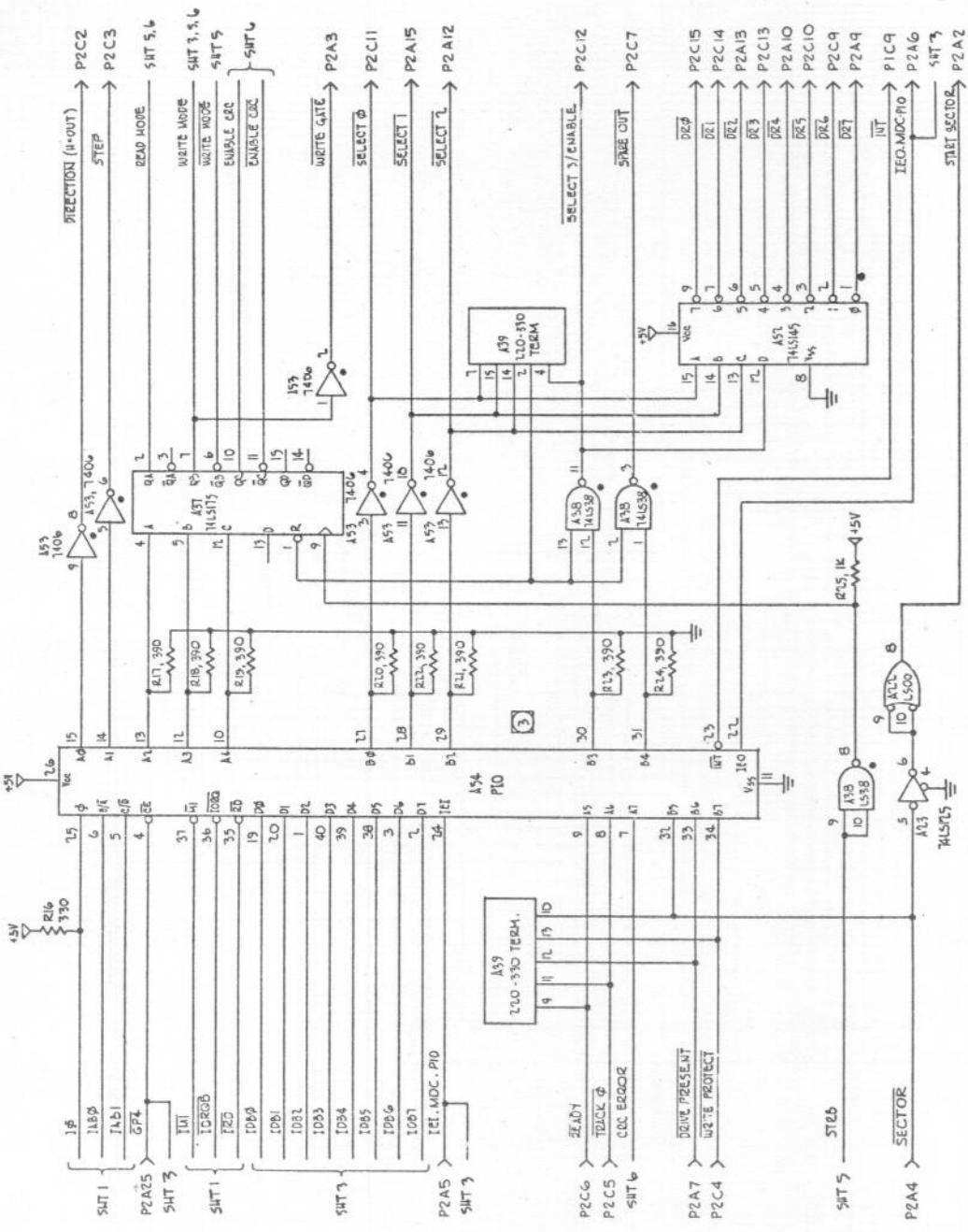


ITEM	QTY	TYPE	INVENTOR NO.	INFORMATION	REF. NO.
<i>NOTES: UNLESS OTHERWISE SPECIFIED RESISTORS ARE CARBON, %W, 1%. CAPACITORS ARE IN MICROFARADS.</i>					
1	1	DISK DATA PORT	CF16		
2	1	LOGIC DIAGRAM	Z80		
3	1	DISK DATA PORT	D2-0050-D1		
4	1	DISK DATA PORT	D2-0050-D1		



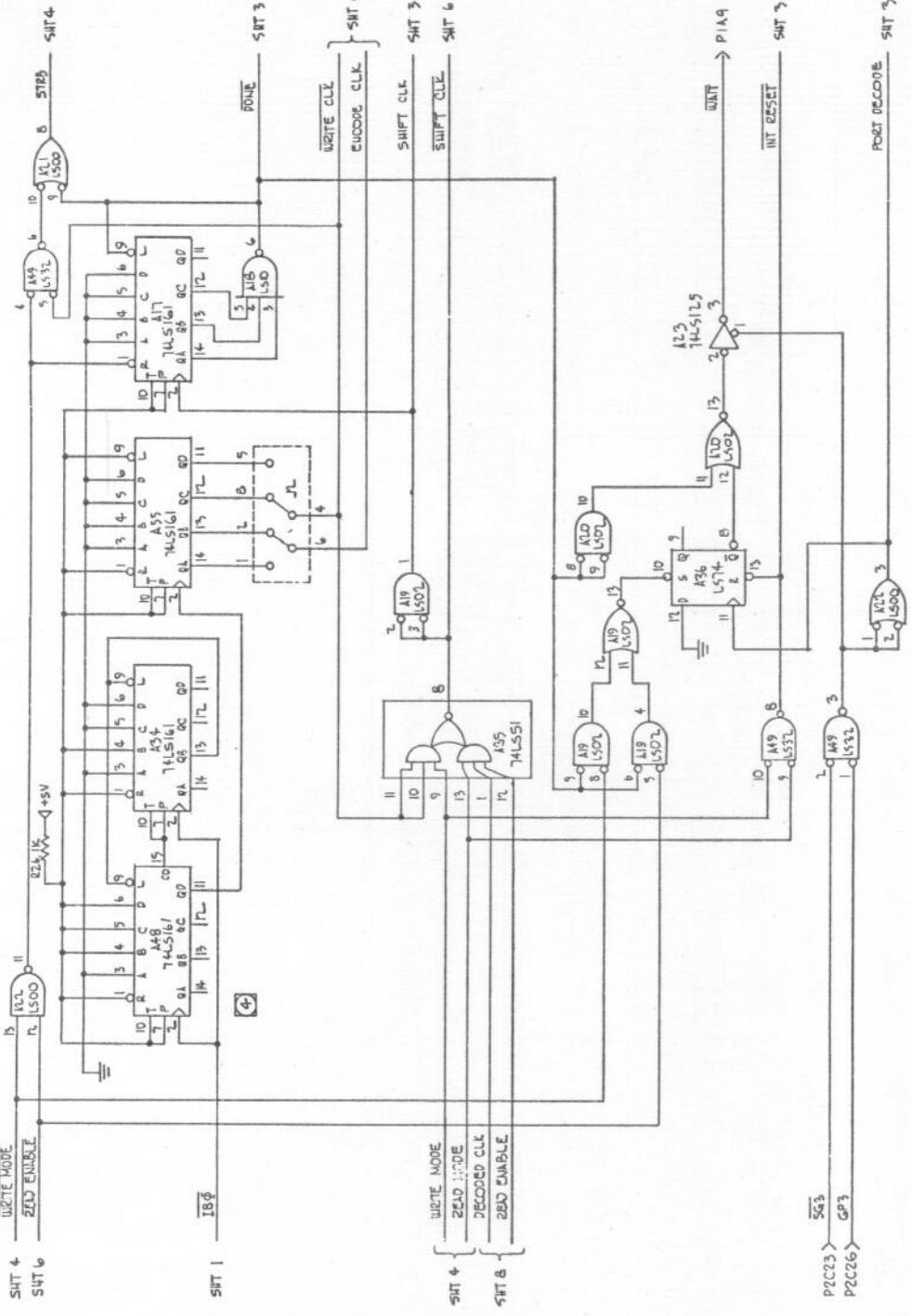


CD-97-0247-12A.

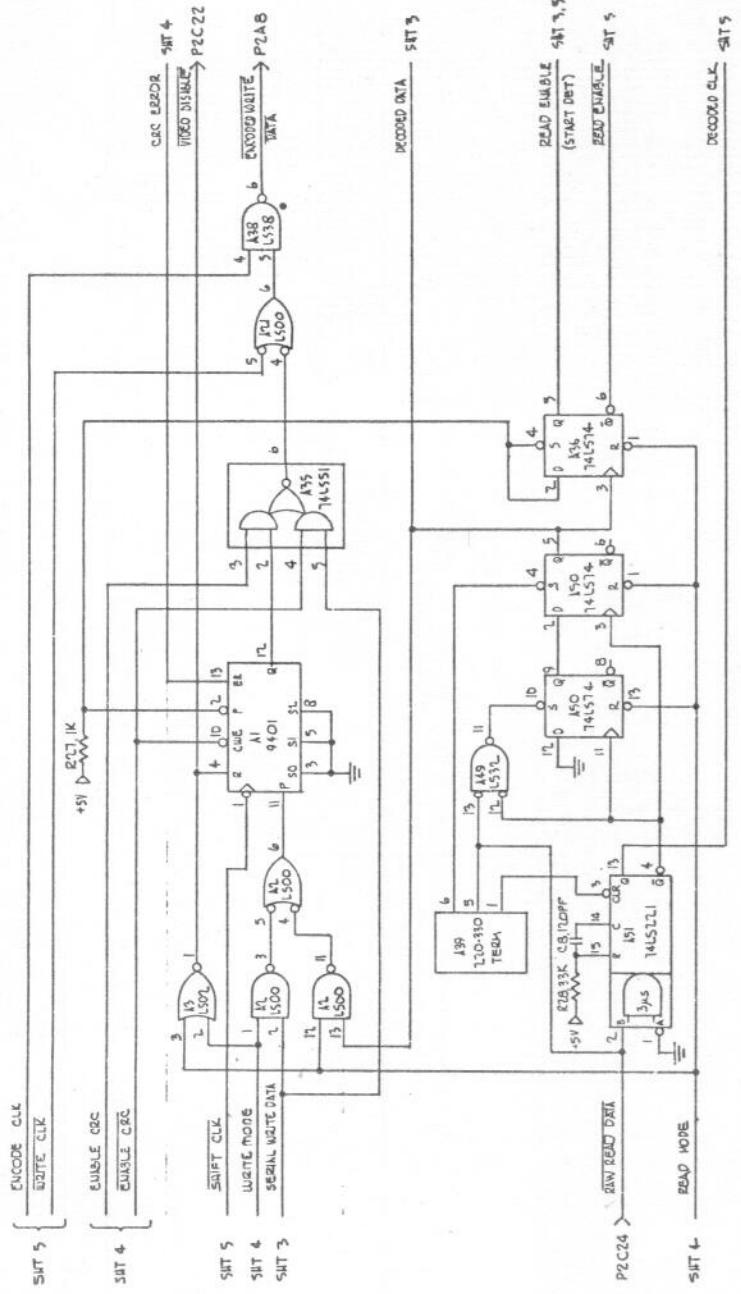


ITEM	QTY	TYPE	ITEM NO.		DESCRIPTION	REF. DES.
			PARTS	LIST		
UNLESS OTHERWISE SPECIFIED DRAWINGS AND MACHINING INSTRUCTIONS ARE IN APPLICABLE AS OF FACILITY 2/1948 EXC. 2/1948 EXC. 2/1948					ZILOG INC. Code 8000 NO. 100 DARINHO, CALIFORNIA, USA	
LOGIC DIAGRAM, WORD PROCESSOR	1	PRINT	1	1	LOGIC DIAGRAM, WORD PROCESSOR	
NEXT ACTV. USED ON	MATERIAL					
APP. EDITION						

With this edition, *Shay's 20th* remains the most widely used program throughout the country. The book also includes information about state laws, rules, and regulations, as well as information on how to become a registered dietitian.



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ITEM	CITY	TYPE	ZINC PART NO.	PART LIST	DEFINITION	REV. DATE
100-101	DUBLIN, CALIFORNIA	STANDARD	10000-101	ZINC PLATE 100-101	ZINC PLATE 100-101	100-101

**GOOD WITH IT.** *It's good to be the good guy at work. It's good to be the good guy at home. It's good to be the good guy everywhere you go. It's good to be the good guy. It's good to be the good guy.*

