

**DOUBLE-DENSITY
DISK CONTROLLER
and
Z-67 INTERFACE**

Model WH-8-37 595-2859

**OPERATION/SERVICE
MANUAL**



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Heathkit® Manual

for the

DOUBLE-DENSITY DISK CONTROLLER and Z-67 INTERFACE

Model WH-8-37 595-2859

**HEATH COMPANY
BENTON HARBOR, MICHIGAN 49022**

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INTRODUCTION

The WH-8-37 Double-Density Disk Controller and Z-67 Interface connects the following disk systems to your H-8 series Computer:

- Z-67** Winchester Disk System with 9.76 Megabytes and 1.022 Megabytes (one Winchester disk and one 77-track, double-density 8" diskette).

It also connects one of the following to your Computer:

- H-17** Floppy Disk System with up to 480 Kilobytes (up to three 40-track, single-side, double-density, soft-sectored H-17-1 disk drives; or three 80-track, double-sided, double-density, soft-sectored H-17-4 disk drives).
- H-77/Z-87** Floppy Disk System with up to 320 Kilobytes (up to two 40-track, single-side, double-density, soft-sectored H-17-1 disk drives).
- H/Z-37** Dual-Sided Disk System with up to 1.28 Megabytes (up to two 80-track, double-side, double-density, soft-sectored H-17-4 disk drives).

The WH-8-37 Double-Density Disk Controller and Z-67 Interface operates under the following Disk Operating Systems:

HDOS version 2.0 and later for use with the floppy disk controller portion only. Requires update HOS-5-UP. (Available on request at no cost to HDOS 2.0 owners. Contact Heath Customer Service.)

CP/M* version 2.2.03 and later for use with the Z-67 portion and the floppy disk controller portion.

SPECIFICATIONS

Note: The following specifications apply to the hardware only and not to software supported by Heath Company.

Floppy Disk System (Z-37)

Drive Size	5-1/4"
Tracks	48 or 96 tracks per inch
Density	Single or double
Sides	Single or double
Number of drives	Four
Heath Type	H-17-1 or H-17-4
Controller	1797

Hard Disk Interface (Z-67)

Controller Supported

Data Technology MRX 101D

HOST COMPUTER REQUIREMENTS

HARDWARE

To run your system with a WH-8-37 Double-Density Disk Controller and Z-67 Interface, your Model H-8 Computer must have a Model HA-8-6 CPU Z80 Circuit Board in place of the 8080 CPU board that was supplied with it.

To use a disk based operating system effectively, you will also need at least 48K bytes of RAM.

FIRMWARE

The following changes and additions must be made on your Model HA-8-6 Z80 CPU Circuit Board (See "Installation" for instructions):

1. Boot ROM (part number 444-70) moved from location U13 to location U19.
2. Boot ROM 2 (part number 444-140) installed at location U13 (supplied).
3. Eight-to-three line priority encoder (74LS148) removed from location U38 (this is placed at location U43 of the WH-8-37 Circuit Board).
4. Jumper wire installed between hole 36 and pin 9 of U38.
5. Jumper installed between holes 24 and 26.
6. Jumper from hole 28 and hole 29 removed and one installed between holes 28 and 27.

DIP SWITCH SETTINGS

The CPU switch settings are detailed in the "HA-8-6 Configuration" section on Page 17.

COMPATIBILITY WITH OTHER INTERFACES

The WH-8-37 Double-Density Disk Controller and Z-67 Interface is compatible with the following interfaces (within the limits of the H-8 Computer system):

- H-8-2 Three-Port Parallel Interface.
- H-8-4 and WH-8-4 Four-Port RS-232C Serial Interfaces.
- H-8-5 and WH-8-5 9600 Baud Serial/1200 Baud Cassette Interfaces.
- WH-8-47 Z-47 Disk Interface.
- H-17 Floppy Disk System Controller Board.

INSTALLATION

UNPACKING

Check the parts you received against this Parts List. Any part that is packed in an individual envelope with a part number on it should not be removed from its envelope until it is called for in a step. Do not discard any packing materials until all parts are accounted for.

HEATH Part No.	QTY.	DESCRIPTION
181-3774	1	Assembled circuit board
134-1241	1	Flat 16-conductor 14" cable assembly
134-1243	1	Flat 34-conductor 14" cable assembly
134-1244	1	Flat 40-conductor 14" cable assembly
134-1269	1	Flat 34-conductor cable assembly
173-53	1	Set of two 5-1/4" floppy diskettes
250-56	2	6-32 × 1/4" machine screw
331-6	1	Solder
344-167	1	4" wire
390-2333	1	Keytop label set
444-140	1	Boot ROM 2
462-1023	16	Keytop
490-111	1	IC puller
490-185	1	Desolder braid
	1	Manual (See Page 1 for part number)
	1	PAM-37 Operations Manual (See Page 1 for part numbers.)

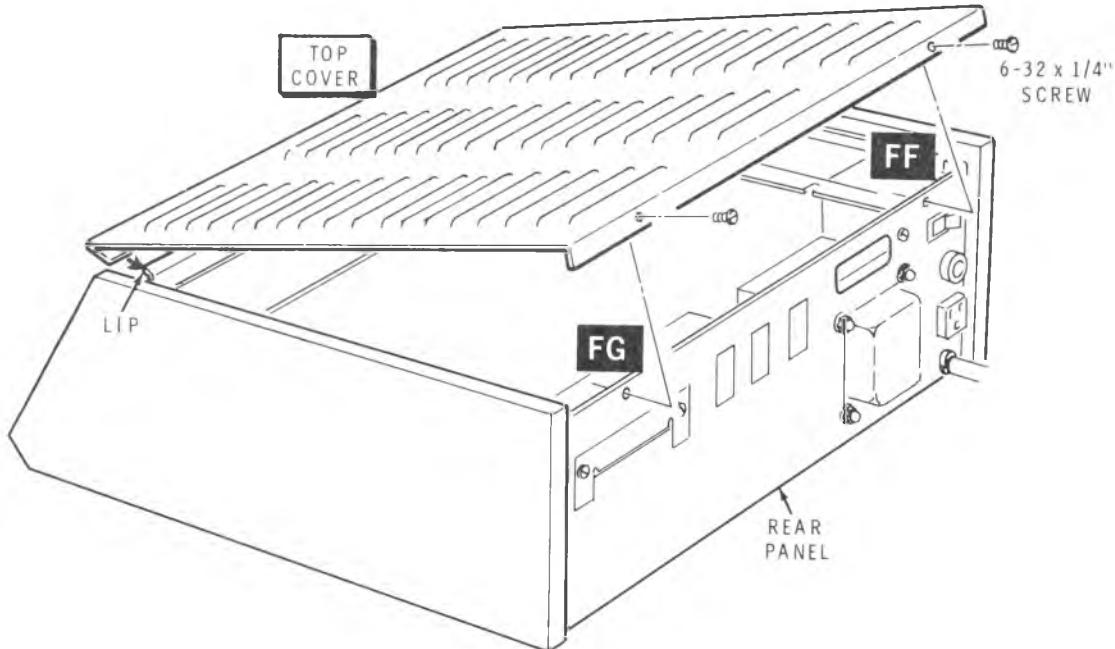
NOTICE

If the container in which this unit was shipped shows any evidence of rough handling, inspect the circuit board very carefully. Any shipping damage must be reported to the carrier at once.

DISASSEMBLY

NOTE: Do not discard any screws or hardware that you remove from your Computer. You will need them when you install the circuit boards and replace the top cover.

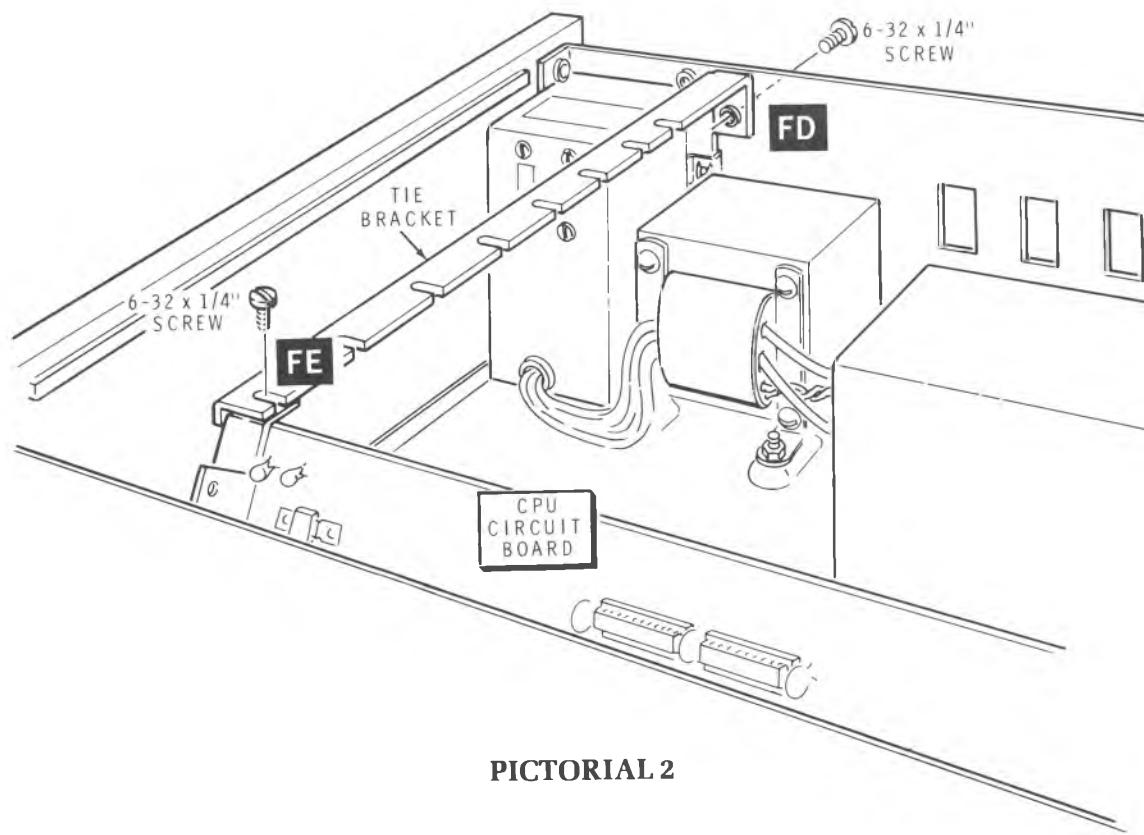
- () Be sure your Computer is turned off.
- () Refer to Pictorial 1 and remove the two 6-32 × 1/4" screws at FF and FG that secure the top cover to the rear panel of the Computer. Then remove the top cover and set it aside.



PICTORIAL 1

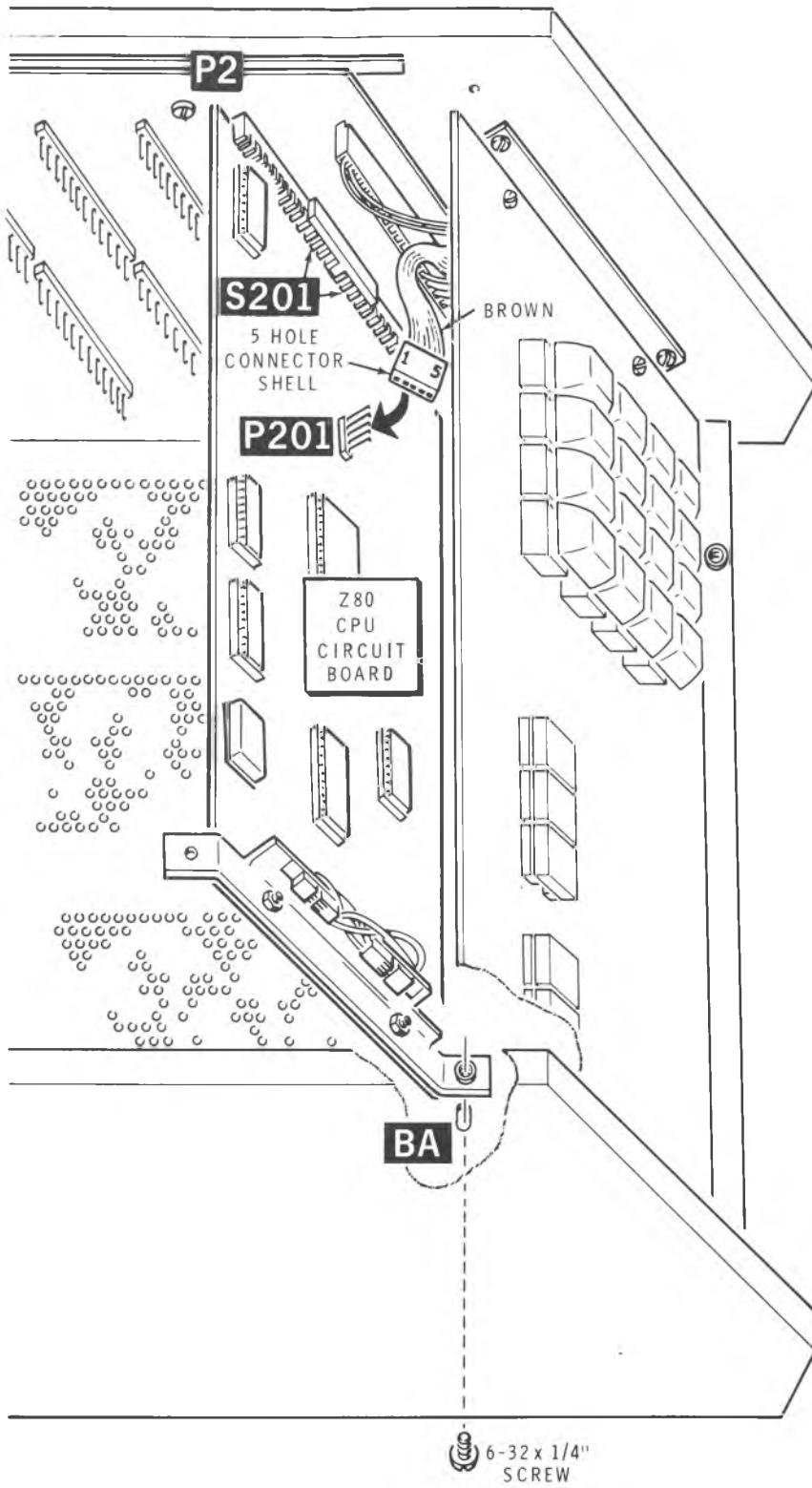
() Refer to Pictorial 2 and loosen the screw at FE that holds the CPU board to the tie bracket. Then loosen any screws that hold other circuit boards to the tie bracket.

() Remove the screw at FD on the rear panel. Then remove the tie bracket and set it aside.



Refer to Pictorial 3 and perform the following steps.

- () Remove the 6-32 × 1/4" screw at BA on the cabinet bottom.
- () Carefully unplug the CPU board from the mother board.
- () Remove the 5-hole connector shell from P201 on the CPU board. Then remove the CPU board and set the Computer aside.



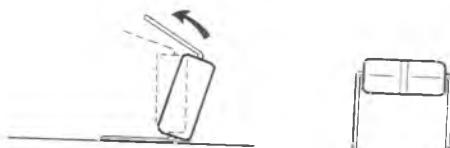
PICTORIAL 3

HA-8-6 Z80 CPU MODIFICATION

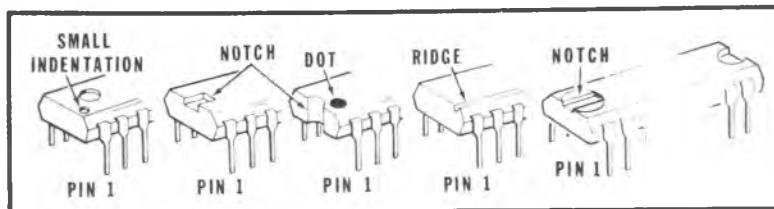
CAUTION: Integrated circuits (ICs) are complex electronic devices that perform many complicated functions in the circuit. These devices can be damaged during installation or removal. Read all of the following information before you install or remove any ICs.



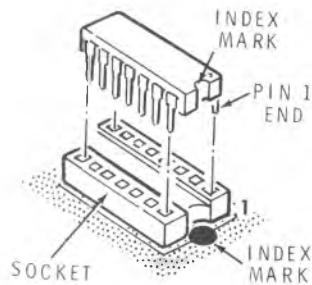
The pins on the ICs may be bent out at an angle, so they do not line up with the holes in the IC socket. **Do not** try to install an IC without first bending the pins as described below. To do so may damage the IC pins or the socket, causing intermittent contact.



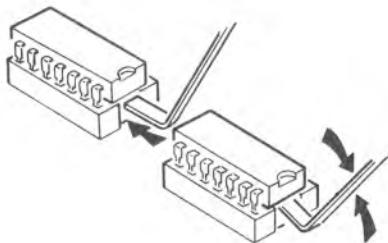
Before you install an IC, lay it down on its side as shown above and very carefully roll it toward the pins to bend the lower pins into line. Then turn the IC over and bend the pins on the other side in the same manner.



Make sure that the pin 1 end of the IC is positioned over the index mark on the circuit board (see the detail below). Also make sure that all of the pins are started into the socket. Then press the IC firmly into the socket. NOTE: An IC pin can become bent under the IC and it will appear as though it is correctly installed in the socket.



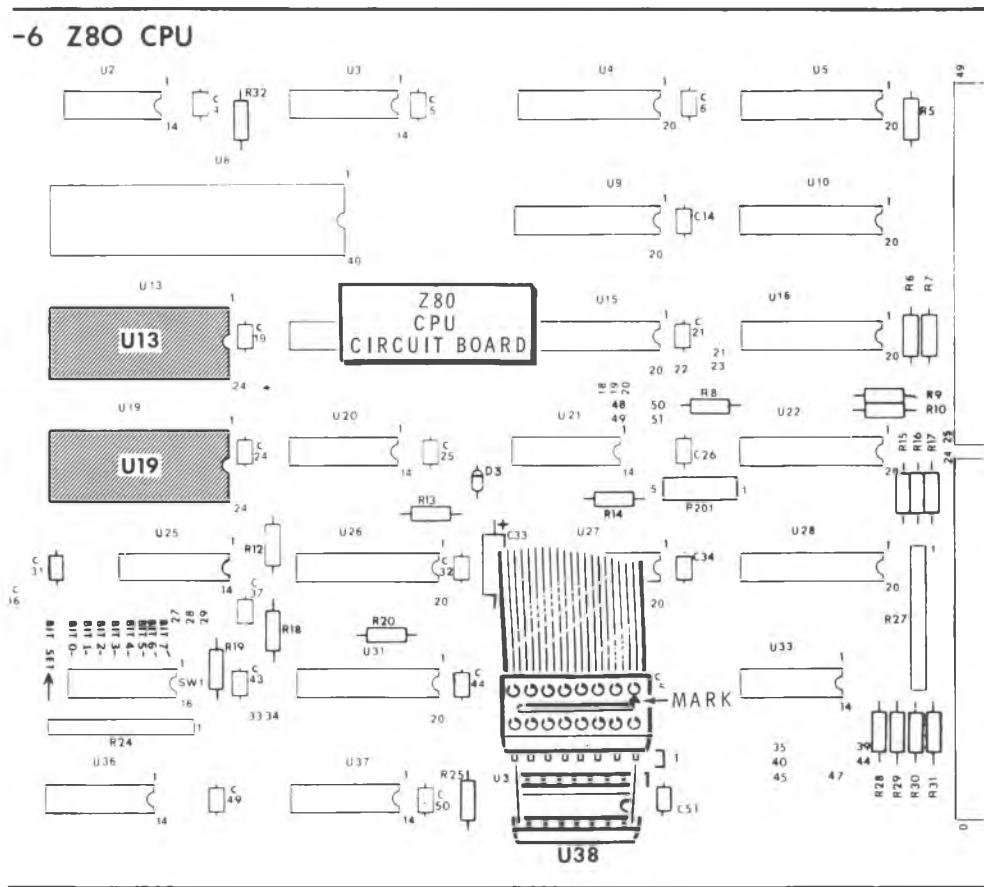
Many ICs are metal-oxide semiconductors (MOS), and they can be damaged by static electricity. Once you remove an IC from its protective foam packing, **do not** lay the IC down or let go of it until it is installed in its socket. When you bend the leads of an IC, hold the IC in one hand and place your other hand on your work surface before you touch the IC to your work surface. This will equalize the static electricity between the work surface and the IC.



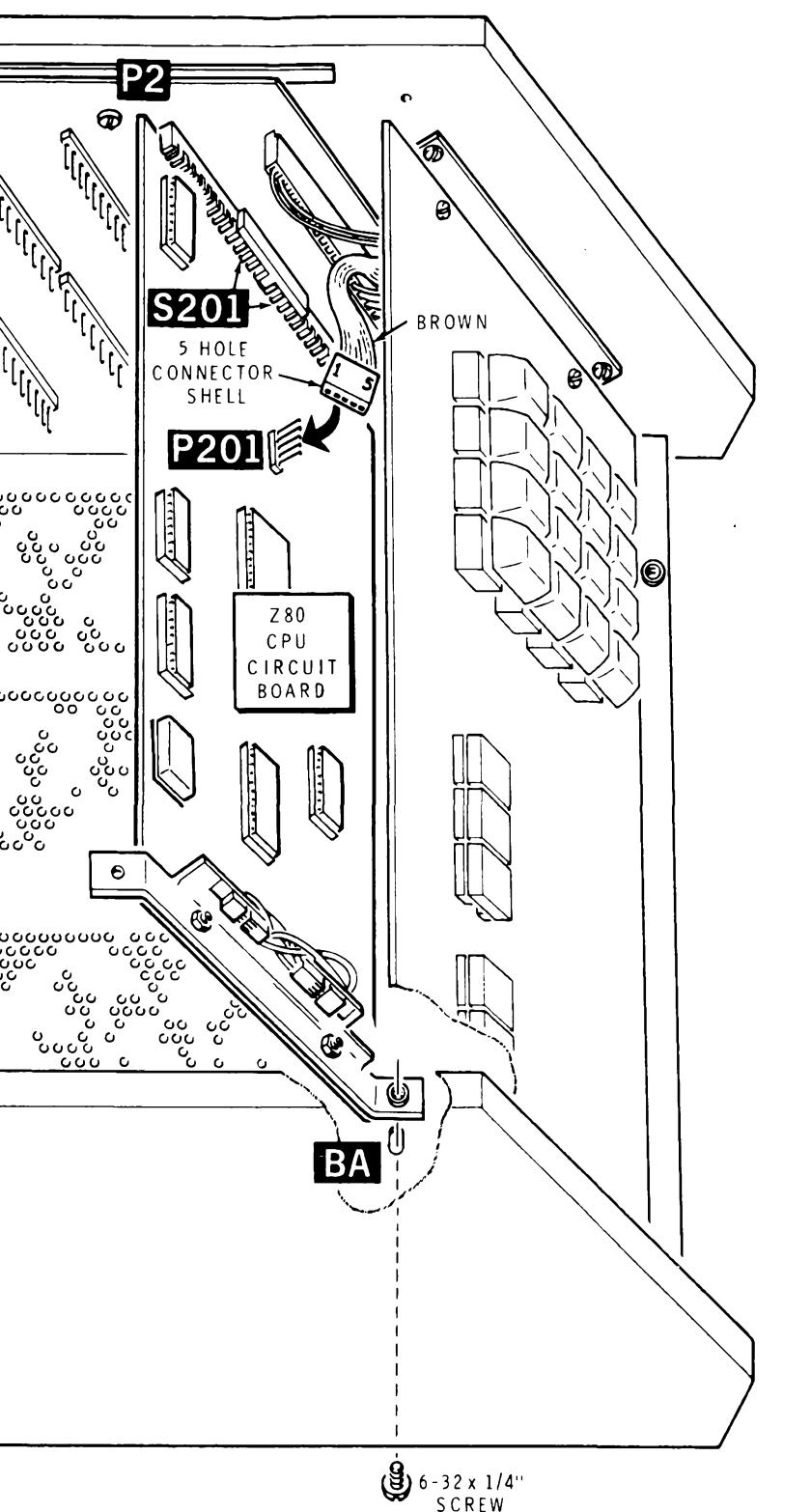
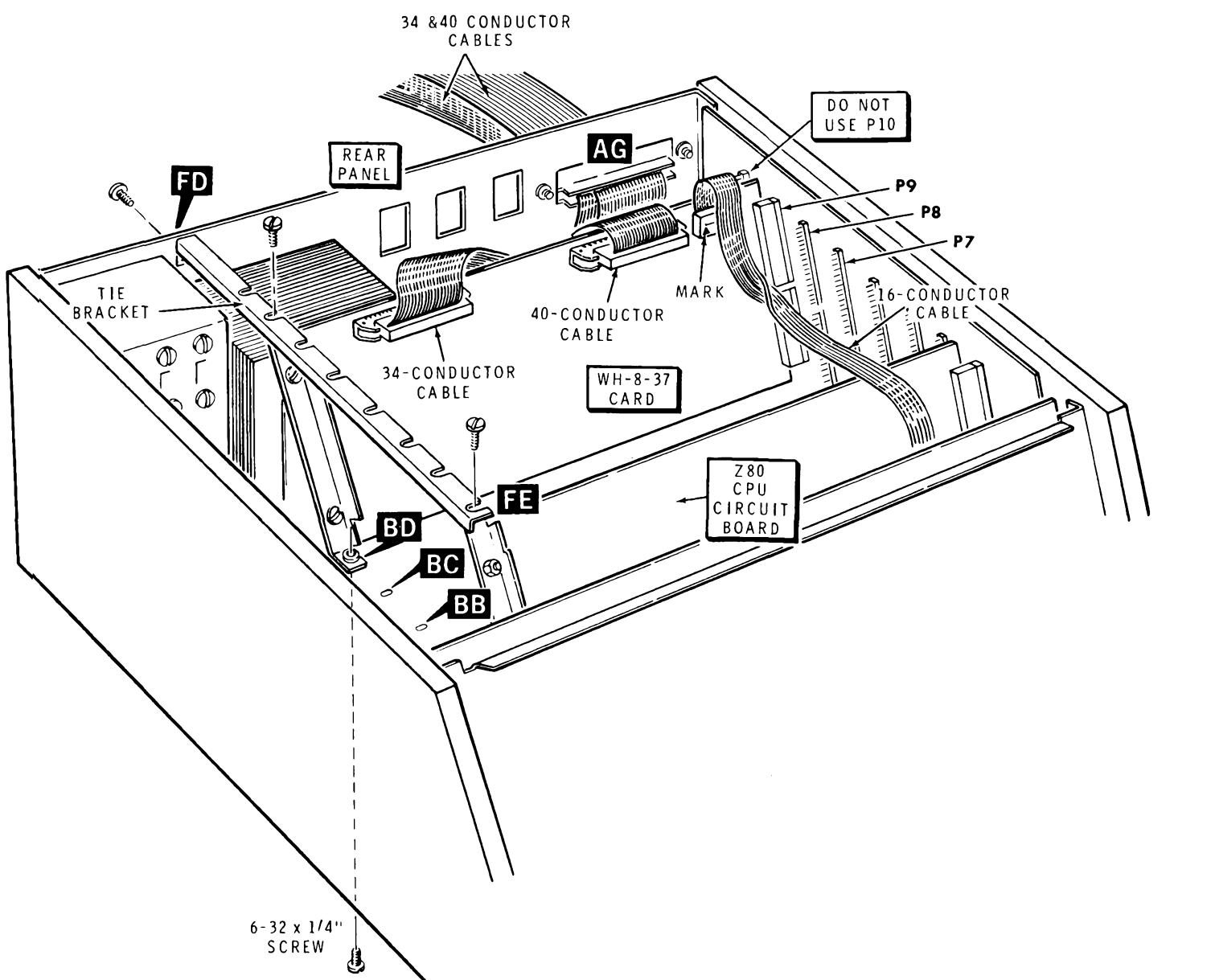
An IC puller has been supplied for convenience in removing ICs. Whenever you remove an IC from its socket, be careful that you do not bend any pins of the IC.

Refer to Pictorial 4 and perform the following steps.

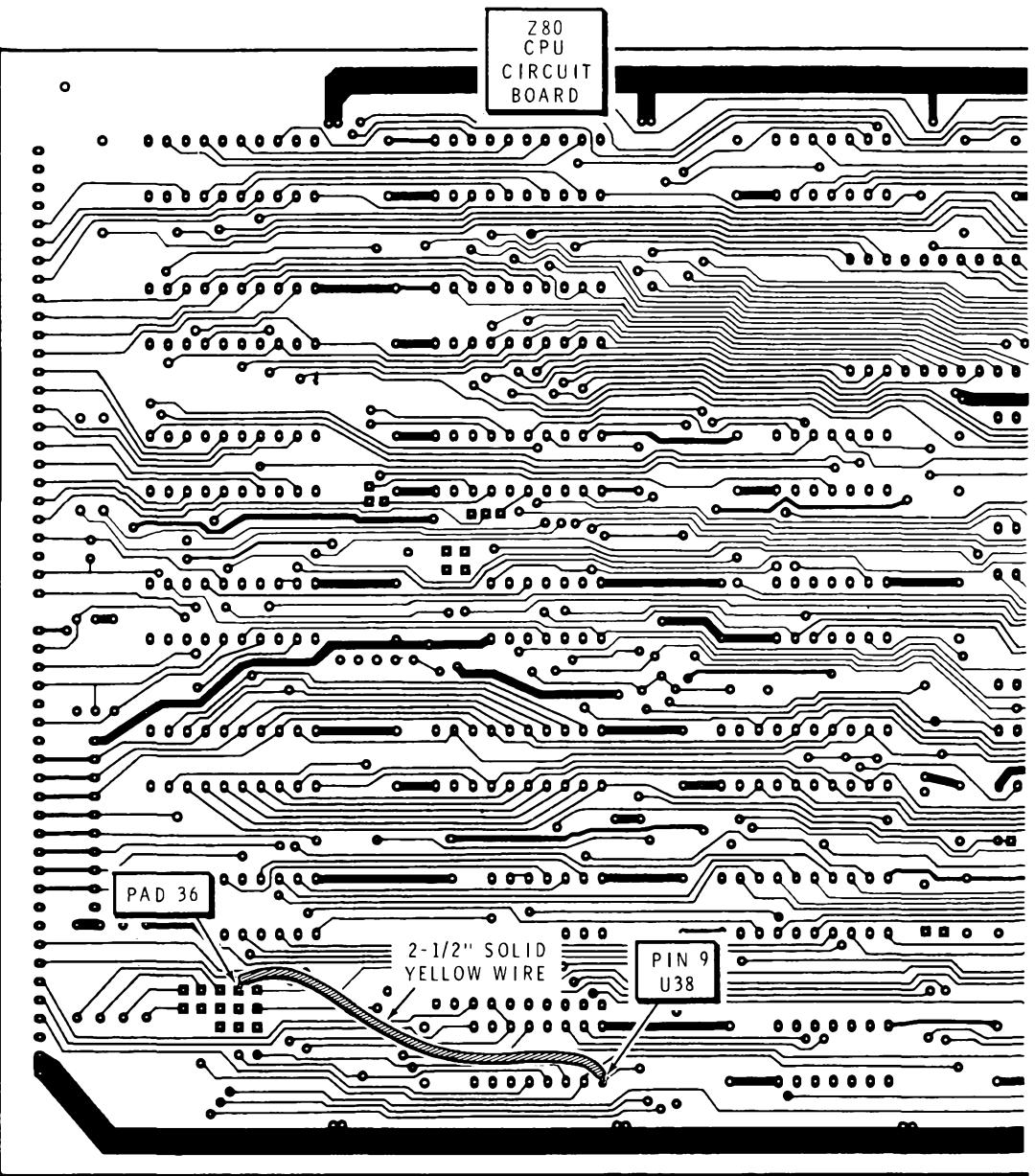
- () Position the CPU board as shown in the Pictorial.
- () Carefully remove IC U38 from its socket on the circuit board and store the IC in conductive foam for use later in the installation.
- () Carefully remove IC U13 from its socket on the circuit board.
- () Reinstall the IC at U19. Make sure you position the pin 1 end toward the index mark on the circuit board.
- () Install the BOOT ROM 2 IC (#444-140) at U13. Make sure you position the pin 1 end toward the index mark on the circuit board.



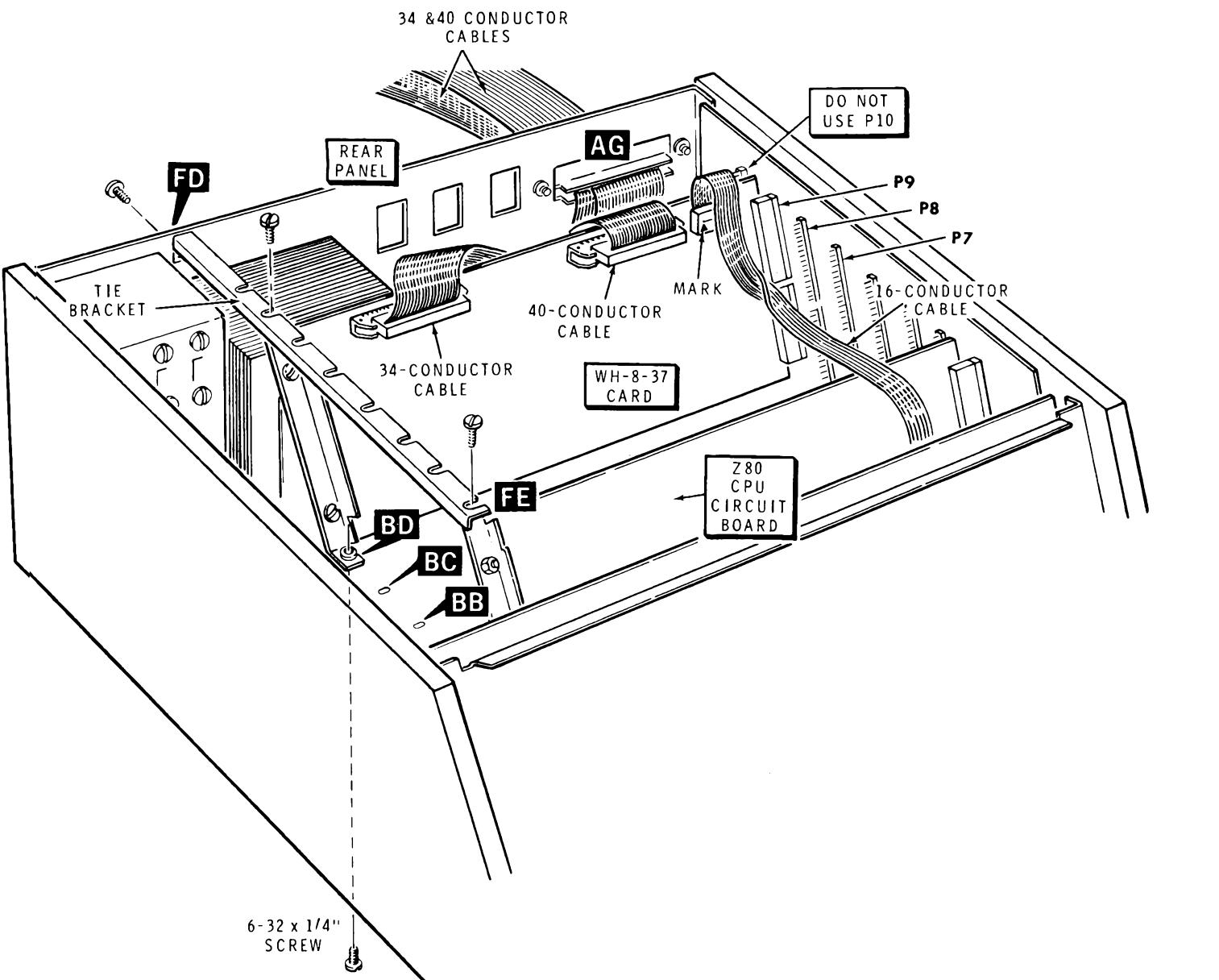
PICTORIAL 4



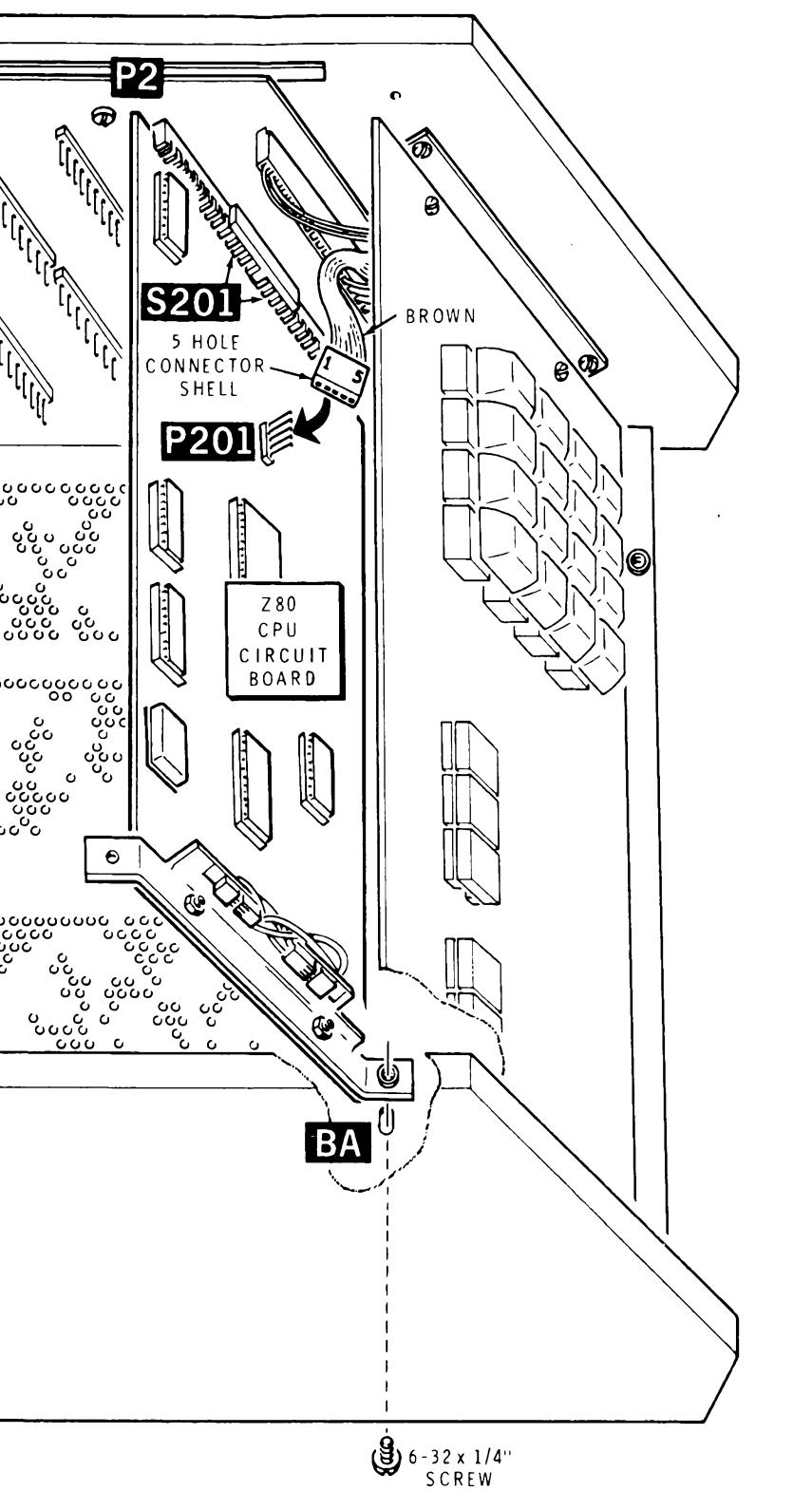
PICTORIAL 9



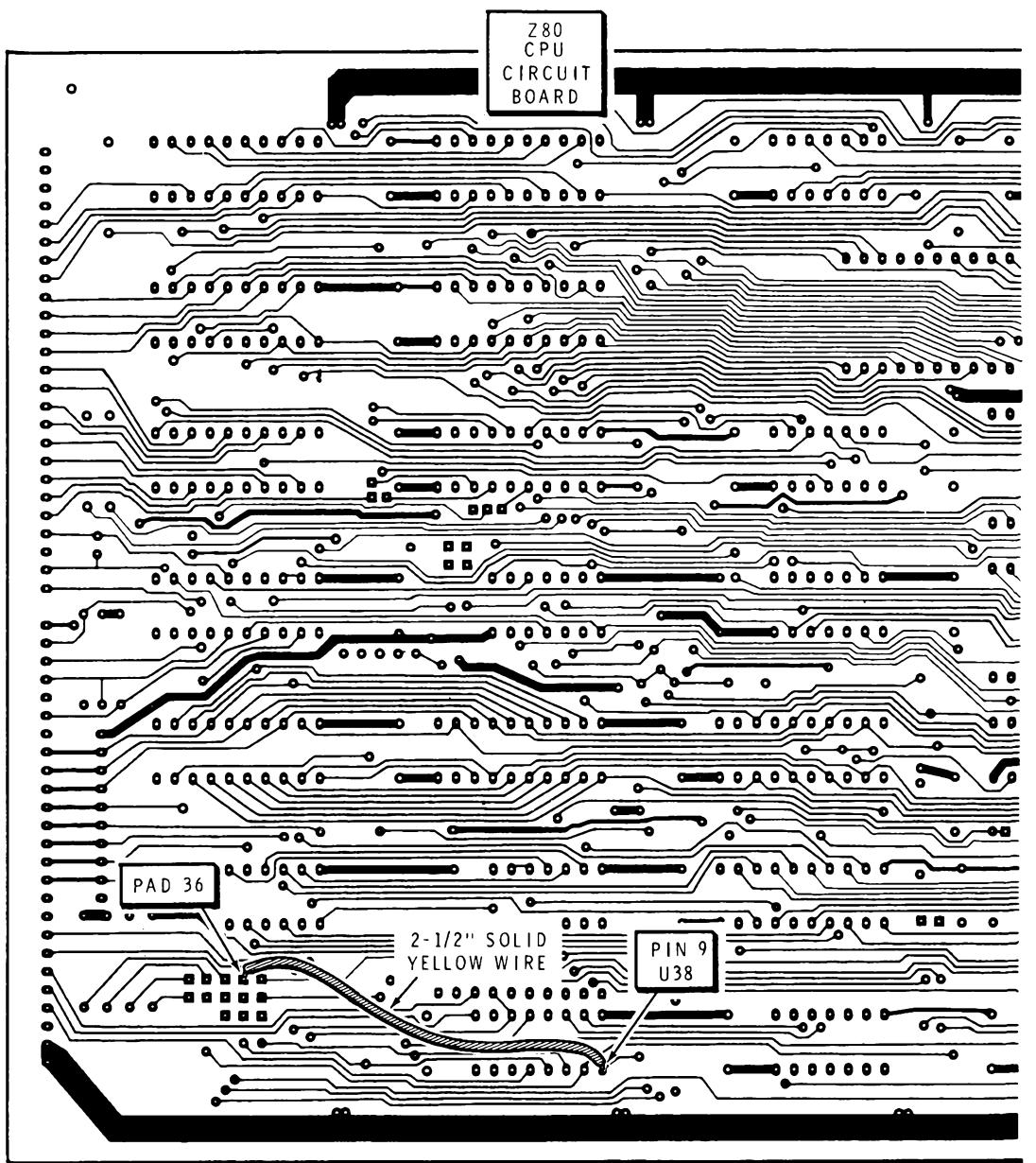
- () Refer to Pictorial 6. Turn the Z80 CPU circuit board over so that you are looking at the reverse (non-component) side.
- () On the non-component side of the board, connect the 2-1/2" solid yellow wire from hole 36 to pin 9 of U38. Solder the wire at both ends, then check to make sure that you did not form any solder bridges when you soldered the wire to the circuit board.



PICTORIAL 10



PICTORIAL 9



PICTORIAL 6



- () Refer to Pictorial 4. Turn the board back over to the component side.
- () Remove the protective cover from one end of the 16-conductor flat cable (134-1241).
- () Install the DIP connector at position U38 of the HA-8-6 Z80 CPU Circuit Board. Make sure that the marked pin lines up with pin number one of the IC socket. If the cable does not feed as illustrated in Pictorial 4, remove the connector and use the other end of the cable.

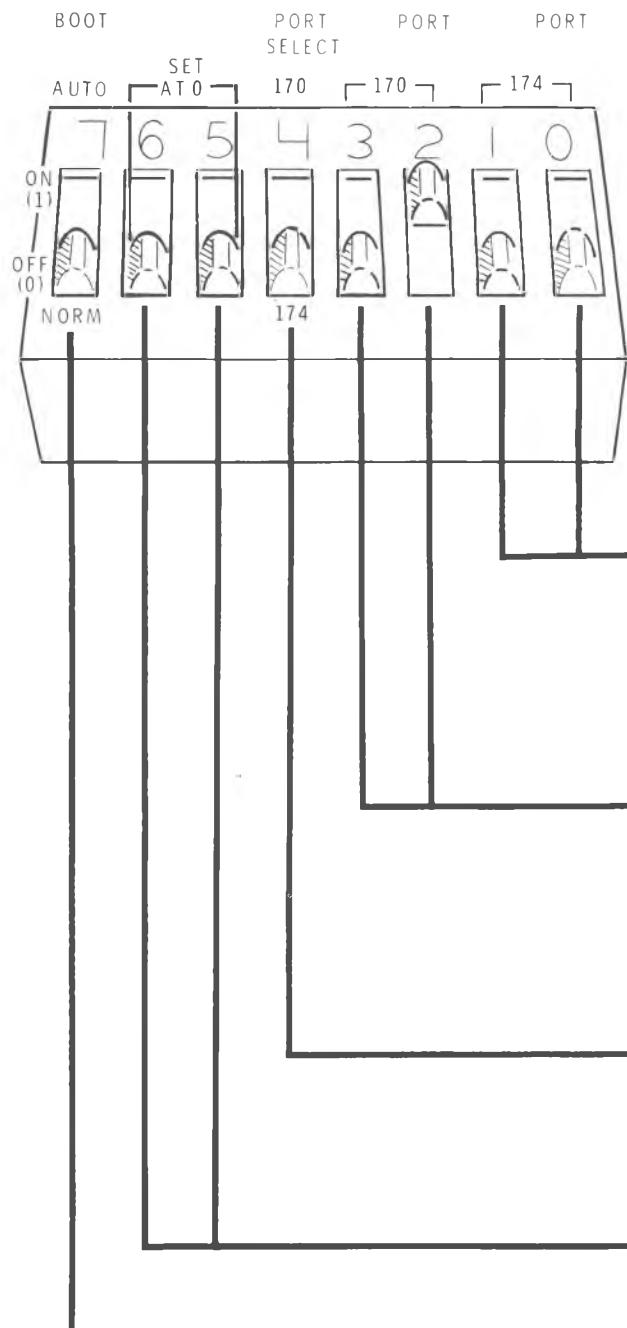
HA-8-6 CONFIGURATION

The addition of the WH-8-37 Double Density Disk Controller and Z-67 Interface brings new power and flexibility to your H-8 Computer. (By using ports 270 and 274, up to **four** mass storage devices may be used by a single H-8 Computer. As distributed, both HDOS and CP/M do not support such use. However, you can implement such a system by modifying the operating system software.) While you can control up to four different drive types with the H-8, current software from Heath and Zenith Data Systems only supports two types at any one time. When you configure your system, please consider the following legal combinations with respect to HDOS and CP/M:

- If you have an H-17 Disk Controller, the H-17 device must be assigned to port 174. With the addition of the WH-8-37, port 170 may be assigned either to the H/Z-37 or to the Z-67 device, but not both.
- If you have an H-47 Disk Controller, the H-47 device may be assigned either to port 170 (normal) or to port 174 when used by itself. Or, when the H-47 Controller is used with the WH-8-37 and a Z-37 device or a Z-67 device, the H-47 device must be assigned to port 174 and the Z-37 or Z-67 device assigned to port 170.
- If you are using the WH-8-37 by itself and only one device (Z-37 or Z-67), either may be assigned to port 170.
- If you are using the WH-8-37 by itself and both devices are active, the Z-37 device must be assigned to port 170 and the Z-67 device assigned to port 174.

Heath/Zenith CP/M HDOS version 2.0 or later, and some user programs will interrogate the status port to determine system configuration on boot-up.

Pictorial 7 shows the 8-section status port switch and defines the function of each section. Set these switches according to your system configuration before you reinstall the Z80 CPU board in your Computer.

**PICTORIAL 7**

Selects the device located at port 174 (Octal). The settings of these two sections are:

- 00 — H-17 Controller.
- 01 — H-47 8" Disk Controller.
- 10 — Z-67 Winchester Interface.
- 11 — No controller.

Selects the device located at port 170 (Octal). The settings of these two sections are:

- 00 — Z-37 Controller.
- 01 — H-47 8" Disk Controller.
- 10 — Z-67 Winchester Interface.
- 11 — No controller.

Determines whether the primary boot device is at port 170 or 174 (Octal). The setting is:

- 0 — Primary boot from port 174.
- 1 — Primary boot from port 170.

These two sections are not used by the H-8 Computer at this time.

Determines whether boot is automatically invoked on power up or not.

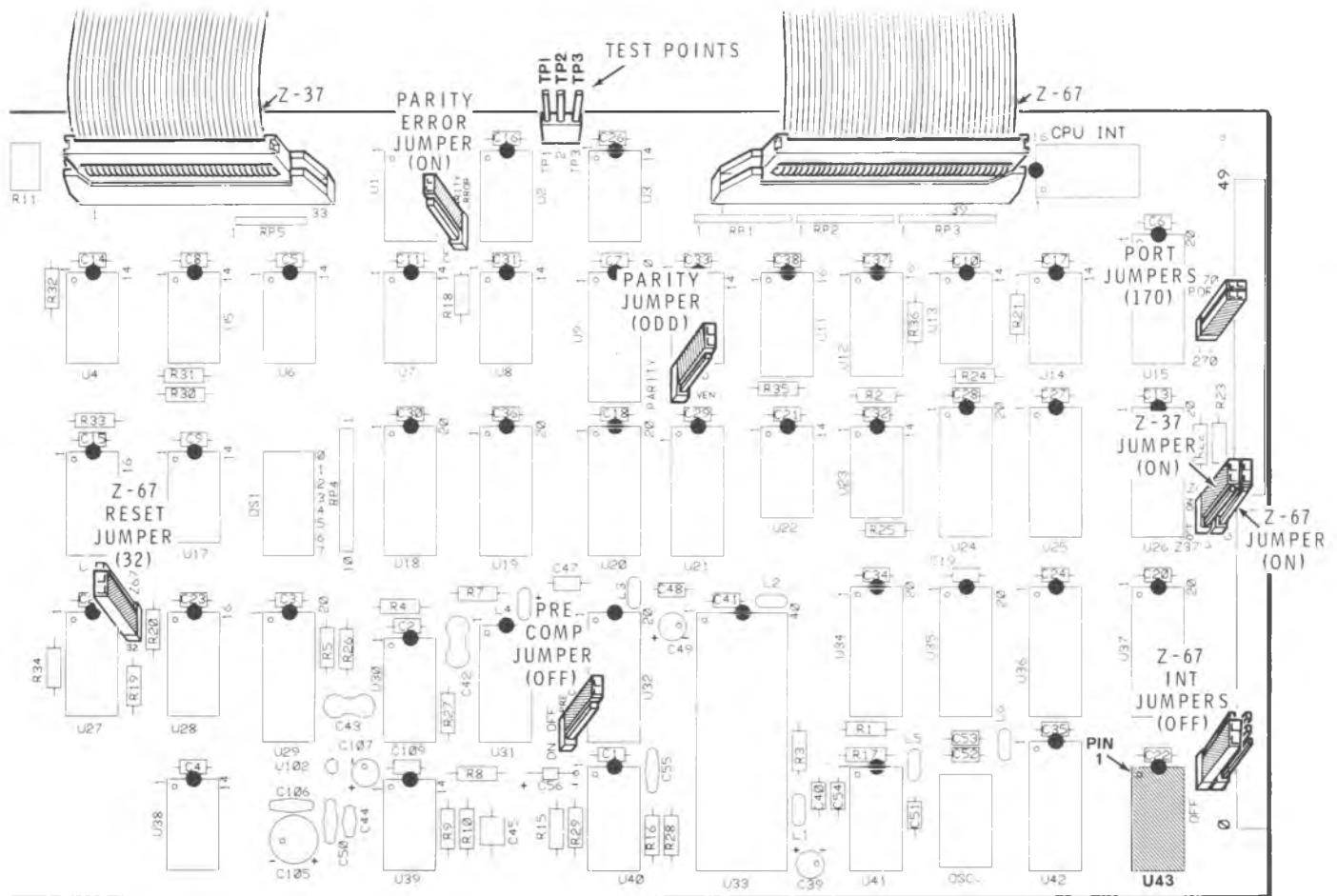
- 0 — Normal boot.
- 1 — Auto boot on power up.

() Set the CPU Z80 circuit board aside for now.

WH-8-37 CIRCUIT BOARD

Refer to Pictorial 8 for the following steps.

- () Position your WH-8-37 circuit board as shown in the Pictorial.
- () Install the 74LS148 IC (that was previously at location U38 on the Z80 CPU circuit board) into the socket at location U43. Make sure you position the pin 1 end toward the index mark on the circuit board.

**PICTORIAL 8**

WH-8-37 CONFIGURATION

The following jumpers are shown installed in their recommended positions.

- () Port jumpers: Position two jumpers horizontally (as shown) for port base address 170 octal (normal). If you want to use port base address 270 octal, position the two jumpers vertically.
- () Z-67 jumper: Position one jumper in the upper (ON) position as shown if the WH-8-37 will be connected to a Z-67. Otherwise, position this jumper in the lower position (OFF).
- () Z-37 jumper: Position one jumper in the upper (ON) position as shown if the WH-8-37 will be connected to any 5-1/4" floppy disk drive or system (H-17-1, H-17-4, H-17, H/Z-37, H-77, or Z-87). Otherwise, position this jumper in the lower (OFF) position.
- () Z-67 INT jumper: Position one jumper in the vertical position as shown in the Pictorial. This is the normal "OFF" (no interrupts) position; the Z-67 does not generate interrupts in this sense. If you want to allow interrupts to be passed to the Computer, position a jumper horizontally in one of the three available positions:

NOTE that:

- * INT 3 is used by the Console.
- * INT 4 is used by the Z-37 when running.
- * INT 5 is normally unused.

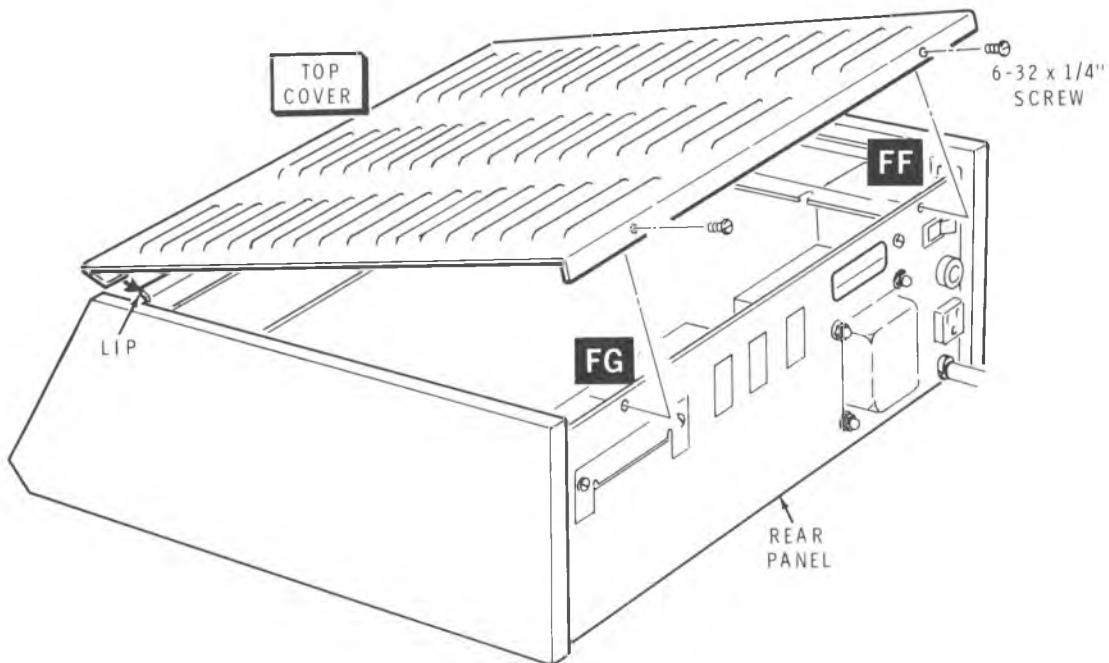
- () PARITY jumper: Position one jumper in the upper position (as shown) for odd parity generation and checking. This is the normal position for Heath and Zenith Data Systems software. For even parity generation and checking, position the jumper in the lower position.
- () PARITY ERROR jumper: Position one jumper in the upper position (normal) for parity error checking. If you do not want parity error detection, position the jumper in the lower (normal) position as shown.
- () PRE COMP jumper: Precompensation may be needed for proper operation by some disk drives. Check with your dealer for information regarding non-Heath/Zenith disk drives (Heath/Zenith disk drives normally do not require precompensation). If you have 48 tpi drives that require precompensation on all tracks or 96 tpi drives that require precompensation on tracks 43 and higher, position one jumper in the lower position; otherwise, position it in the upper (normal) position for no precompensation.
- () Z-67 RESET jumper: Position one jumper in the lower position ($32 \mu s$) as shown for normal operation with a Z-67. If you need to use the shorter pulse width ($4 \mu s$), use the upper position.
- () If you are going to use a 5-1/4" disk drive or system with your WH-8-37 Board, install the 34-connector cable (134-1243) at position Z-37. Make sure that the cable exits from the top of the board as shown in the Pictorial. Two cables are supplied: one for connection directly to an H-17-4 (which may be mounted inside an H-17 cabinet), and the other for connection to an H/Z-37 system.
- () If you are going to use a Z-67 Winchester Disk System with your WH-8-37, install the 40-conductor cable (134-1244) at position Z-67. Make sure that the cable exits from the top of the board as shown in the Pictorial.

CIRCUIT BOARD INSTALLATION

- () Refer to Pictorial 9 (Fold-out from Page 16) and carefully place the HA-8-6 Z80 CPU Circuit Board in your H-8 Computer. Use position P2.
- () Connect the 5-hole connector shell to P201 on the CPU board.
- () Carefully plug the HA-8-6 into the H-8 mother board.
- () Secure the HA-8-6 into the H-8 by using a 6-32 × 1/4" screw at BA on the cabinet bottom.
- () Refer to Pictorial 10 (Fold-out from Page 16) and carefully place the WH-8-37 Board in your Computer. Use one of the rear positions (P7, P8, or P9).
- () Carefully plug the WH-8-37 board into the H-8 mother board.
- () Secure the WH-8-37 board into the H-8 Computer by using a 6-32 × 1/4" screw at BB (if the WH-8-37 is plugged into P7), BC (if the WH-8-37 is plugged into P8), or BD (if the WH-8-37 is plugged into P9) on the cabinet bottom.
- () Replace the tie bracket and secure it with a 6-32 × 1/4" screw at FD on the rear panel.
- () Secure the top of the CPU board to the tie bracket with a 6-32 × 1/4" screw at FE.
- () Secure the top of the WH-8-37 board to the tie bracket with a 6-32 × 1/4" screw.
- () Secure all remaining circuit boards in the H-8 to the tie bracket by tightening the remaining 6-32 × 1/4" screws.
- () Route the 16-conductor cable from the HA-8-6 CPU Circuit Board to the WH-8-37 board and plug the loose end into the DIP socket marked CPU INT. Be sure that the mark on the plug lines up with pin number one of the socket.
- () Route the Z-37 34-conductor cable from the WH-8-37 board out hole AG on the back panel of the H-8 Computer.
- () Route the Z-67 40-conductor cable from the WH-8-37 board out hole AG on the back panel of the H-8 Computer.

- () Refer to Pictorial 11. Hook the front of the top cover over the lip on the front panel of your H-8 Computer. Then push the rear of the top cover down onto the edge of the rear panel.
- () Secure the top cover to the rear panel with 6-32 × 1/4" screws at FF and FG.
- () Connect your disk drives to their respective cables.

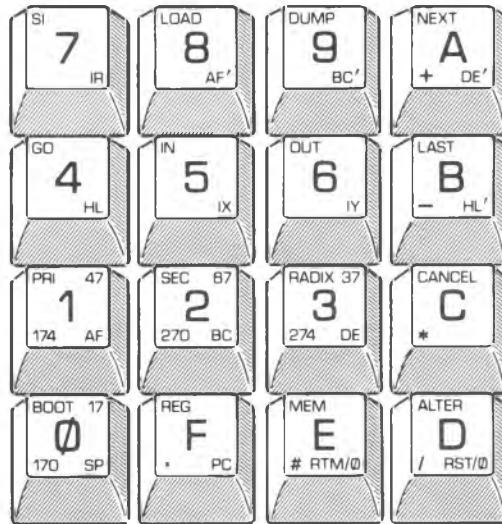
This completes the installation of your new WH-8-37 Double-Density Controller Board and Z-67 Interface into your H-8 Computer.



PICTORIAL 11

FRONT PANEL MODIFICATION

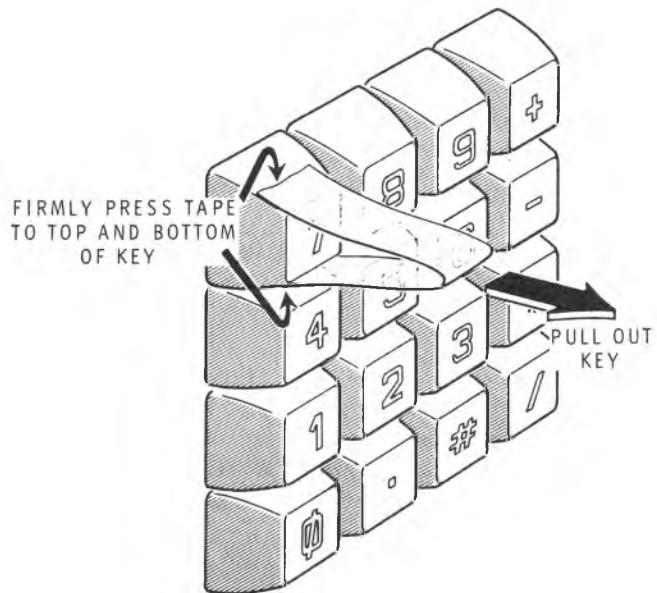
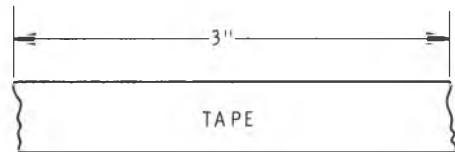
The new Boot ROM that you installed allows one step booting from the Z-37 or Z-67 sections of the WH-8-37 Double-Density Disk Controller and Z-67 Interface and their respective disk drive. Refer to Pictorial 12 for the following steps.



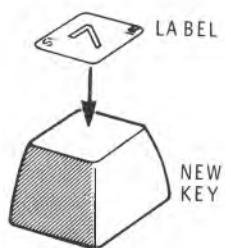
PICTORIAL 12

- () Refer to Detail 12A and remove the sixteen keytops from your H-8 Computer by using the following method on each key:
 1. Attach one end of a 3" piece of tape to the top of the key you want to remove.
 2. Attach the other end of the tape to the bottom of the same key.
 3. Pull the tape and key straight out from the front panel. The key should come off easily. If it does not, use a fresh piece of tape and try again, making sure that the tape is firmly attached to the key.
- () Refer to Detail 12B and install each new keytop label onto a key.
- () Install each of the sixteen keytops onto the keyboard. The arrangement is shown in Pictorial 12.

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Detail 12A



Detail 12B

DISK DRIVE CONFIGURATION

Various programs and operating systems refer to numbers (called "hardware unit numbers") and letters (called "disk drive names") that your Computer uses to recognize each individual drive. The association between a particular drive name and a hardware unit number is determined by the following three conditions:

1. The program jumper on the 5-1/4" disk drive.
2. The programming of the WH-8-37 and HA-8-6 circuit boards.
3. Which drive device (of two) is used to boot the system. (A drive device is classified as a complete system, for example, an H-17, H/Z-37, H/Z-47, or Z-67).

The disk drive names expressed in the chart apply during normal boot of a primary device: the boot device (whether H-17, H/Z-37, H/Z-47, or Z-67) will have SY0:—SY2: or A:—C: drive specifications and the second system will have DK0:—DK2: or D:—F: drive specifications. (NOTE: the H/Z-47 Disk System will use A:-B: and the secondary device C:-E: when the H/Z-47 is used as the primary (boot) device.)

Assignment of drive names may vary if you boot on other than drive 0 of the primary device, or if the hardware unit numbers are numbered other than as illustrated in the chart. Refer to your HDOS or CP/M Manuals.

Primary (Boot) System (Disk Drive Name)	Hardware Unit Number (5-1/4")		Secondary System (Disk Drive Name)	
<u>HDOS</u>	<u>CP/M</u>	<u>Programmed Jumper</u>	<u>HDOS</u>	<u>CP/M</u>
SY0:	A:	0	DK0:	D:
SY1:	B:	1	DK1:	E:
SY2:	C:	2	DK2:	F:

You may wish to alter the drive configuration of your 5-1/4" drives, but it is not necessary unless hardware unit numbers conflict within the same device or you do not have a unit 0 connected to your WH-8-37 Controller Board.

Although the hardware (WH-8-37 circuit board) does accommodate up to **four** 5-1/4" disk drives, Heath and Zenith Data Systems do not support the fourth drive.

Drive programming for 5-1/4" disk drives is illustrated in Pictorials 13, 14, and 15 (Fold-out from Page 26). Pictorial 13 shows 48 tpi drives programmed to be used with the H-17 Controller Board, Pictorial 14 shows 48 tpi drives programmed to be used with the WH-8-37 Board, and Pictorial 15 shows 96 tpi drives programmed to be used with the WH-8-37 Board. NOTE: When they are used with the WH-8-37, drives must be programmed as illustrated in Pictorial 14 or 15.

There were some early 48 tpi drives which are different than those shown. If you have one or more of these drives, they will be covered in your H-17 manuals.

If you purchased a Dual-Drive Z-37 Disk System, they come preprogrammed as hardware unit zero and hardware unit one.

You can program your disk drives by physically interchanging preprogrammed drives, interchanging the programming plugs, cutting the programming plugs (if presently uncut); or by replacing the programming plug with a properly set DIP switch.

MEDIA

96 tpi drives should ONLY be used with media certified for 96 or 100 tpi service; double-density recording should only be done on diskettes that are certified for such use; and double-sided diskettes should always be used in double-sided disk drives (H-17-4).

OPERATION

The new ROM, PAM-37, contains the code necessary to boot an operating system from the H-17 (with the H-17 Controller Board), H/Z-37, H/Z-47 (with the WH-8-47 Disk Interface), or Z-67.

There are four methods you can use to boot your system: Primary, Secondary, Universal, and Auto. Primary and Secondary Boot allow you to boot from a primary or secondary drive system with one keystroke. The Universal Boot allows you to boot your system from any drive in any device. Auto Boot allows **turnkey** operation from drive 0 of the primary device when you turn the power on.

APPLYING POWER TO THE H-8

With your HA-8-6 Z80 CPU Circuit Board, modified and installed back into your H-8 Computer and your new WH-8-37 board properly installed, you are ready to apply power to your Computer.

- () Turn on the power to your Computer. You will hear a beep and your front panel display will show all four indicator lights on (ION, MON, RUN, and PWR) and:

n77377xxx

The **n** will be 0 for 16K of memory, 1 for 32K of memory, 2 for 48K of memory, and 3 for 64K of memory. The **xxx** will be a random number, usually zero. If your Computer does **not** show this display, press **both** the **0** and the **D** keys at the same time. Your Computer should beep once and show the proper display.

Note that the above display is **not** necessary for the proper operation of the H-8. It will, however, serve as a quick check for the proper operation of the new ROM. If you cannot obtain the display at power up, refer to "In Case Of Difficulty" on Page 68.



PRIMARY OPERATION

Select the primary device by setting switch SW1 on the HA-8-6 Z80 CPU Circuit Board (Refer to Page 17, "HA-8-6 Configuration"). To Boot from this device, Press the **1** key. The display will show:

Pri xxx

The **xxx** will display the device name: H17, H37, H47, or H67.

To cancel this boot command, press the **C** key (Cancel).

SECONDARY OPERATION

Select the secondary device by setting switch SW1 on the HA-8-6 Z80 CPU Circuit Board (Refer to Page 17, "HA-8-6 Configuration"). To Boot from this device, Press the **2** key. The display will show:

Sec xxx

The **xxx** will display the device name: H17, H37, H47, or H67.

To cancel this boot command, press the "C" key (Cancel).

UNIVERSAL OPERATION

Primary and secondary operation provide one-key-boot operations from drive 0 of a device. To boot from another drive on a device when it is configured according to the legal specifications set forth on Pages 17 and 24 of this Manual, follow these steps:

- () Press the **0** key (Boot). The display will show:

dEU ("Device")

- () Press one of the following keys to indicate the device: **0** for H-17, **1** for H-47, **2** for H-67 (Z-67), or **3** for H-37 (Z-37). The display will show:

xxx Por ("Port")

The **xxx** will be the device name (H17, H37, H47, or H67).

- () Press the key which corresponds to the port address: **0** is for port 170, **1** is for port 174, **2** is for port 270, and **3** is for port 274. The display will show:

xxx ppp Uni ("Unit")

The **xxx** is the device name (as specified in step 2) and the **ppp** is the port address in Octal (170 for 0, 174 for 1, 270 for 2, and 274 for 3).

- () Press the key which corresponds to the hardware unit number of the disk drive (**0**, **1**, **2**, or **3**). The display will show:

Uni xxx

The **xxx** will be the device name (H17, H37, H47, or H67).

The disk unit will be activated, and the initial boot routine will be read from disk into memory. If an error occurs, the Computer will beep and the display will show:

Err or xxx

Again, the **xxx** will be the device name. To cancel the error or stop the operation, press the **C** key (Cancel).

NOTE: By using ports 270 and 274, up to **four** mass storage devices may be used by a single H-8 Computer. As distributed, both HDOS and CP/M do not support such use. However, you can implement such a system by modifying the operating system software.

AUTO OPERATION

If section 7 of Switch SW1 on the HA-8-6 Z80 CPU Circuit Board is set to 1, the system will automatically boot from hardware unit 0 on the primary device when you turn the power on or perform a master clear (by pressing both the **O** and the **D** keys).

NOTE: We do not recommend auto-booting (from a floppy disk system) with diskettes in any drives and the doors closed at power up. The diskette could be accidentally erased during the power-up sequence inside the Computer. Rather, power up the H-8 and the peripherals (including the disk drives) first, and then insert the diskette and close the drive door. If you do this within 15 seconds of turning on the H-8's power, the auto-boot function will perform normally.

Z-67 WINCHESTER DISK DRIVE PREPARATION

The Z-67 Winchester Disk System is supplied with an 8" diskette containing software utilities that provide for a unique and innovative approach to rigid (Winchester) disk allocation and management. By using these utilities, you will be able to define the partition allocation of the disk and specify which operating system will manage each allocated portion.

The 8" diskette is labeled, "Winchester Disk Utilities" and is distributed in "bootable" form. That is, your H-8 monitor can read in and "boot" the operating system and program without any additional software.

- () To boot the Z-67 Software Utilities disk, turn your Computer and Z-67 on.
- () Place the diskette containing the utilities in the 8" disk drive and close the door. Make sure the diskette label is to the left as illustrated in your Z-67 Operation Manual.
- () In the Z-67, the 8" floppy disk drive is not wired as hardware unit zero. Therefore, to boot from the floppy, you must use the Universal boot procedure. Press the **0** key. The display will show:

dEU

- () Press the **2** key. The display will now show:

H67 Por

- () If your Z-67 is connected to port 170, press the **0** key. The display will show:

H67 170 Uni

If your Z-67 is connected to port 174, press the **1** key. The display will show:

H67 174 Uni

- () Press the **1** key. The display will show the following and the 8" disk will be booted into the system:

Uni H67

After a few moments, your terminal will display:

H/Z-67 PARTITIONING/PREPARATION MENU

A - WINCHESTER DISK PARTITIONING UTILITY
B - WINCHESTER DISK DIAGNOSTIC/PREPARATION UTILITY
C - EXIT

SELECTION ?

To use either of the disk utilities, respond to the "SELECTION ?" prompt by typing either an **A** or **B**, and then pressing the RETURN key. Both utilities will return to this menu once they have finished. Selection of **C** will return control to the H-8 monitor.

NOTE: It should not be necessary to run Selection **B**, as this test is performed at the factory prior to shipment.

Sections two and three of the H/Z-67 Software Utilities Manual fully describe the partitioning utility (PART) and the preparation utility (PREP67), respectively.

- () Follow the instructions in section two of the H/Z-67 Software Utilities Manual and partition your Winchester Disk Drive.
- () Refer to your operating system Manual for instructions for using the Z-67 Winchester Disk System.

THE Z-37 DOUBLE-DENSITY CONTROLLER

Diagnostic Routines

The diagnostic routines supplied with your WH-8-37 Double-Density Disk Controller and Z-67 Interface allow you to "check out" and test your 5-1/4" soft-sectored disk system and diskettes.

They are supplied on two 5-1/4" bootable diskettes, labeled "Soft-Sectored" and "Hard-Sectored." The programs contained on the two diskettes are identical; the only difference is the type of media. Hard-sectored diskettes are used by your H-17 Controller Board and associated disk drive(s); soft-sectored diskettes are used by the Z-37 portion of the WH-8-37 and associated disk drive(s). You can use either diskette to perform the diagnostic routines, but be sure to use the diskette labeled "Soft-Sectored" in disk drives that are connected to the WH-8-37 circuit board, and the diskette labeled "Hard-Sectored" in disk drives that are connected to the H-17 Controller Board.

To perform the diagnostics, you will need at least two blank, 5-1/4", soft-sectored diskettes. It does not matter whether these diskettes are single- or double-density, nor whether they are single- or double-sided.

STARTING THE DIAGNOSTIC PROGRAMS

To start the diagnostic programs, boot up the system using **either** the hard- or soft-sectored Diagnostic diskette in the proper drive. The following procedure outlines how you should boot-up.

1. Turn on the power to your Computer and disk drive(s). You will hear a beep and your front panel display will show all four indicator lights on (ION, MON, RUN, and PWR) and:

n77377020

The **n** will be 0 for 16K of memory, 1 for 32K of memory, 2 for 48K of memory, and 3 for 64K of memory. If your Computer fails to display the above, press both the **0** and **D** keys at the same time to perform a reset. If your Computer still fails to show the proper display, refer to your H-8 Manual for assistance.

2. Determine which drive is the boot drive by following the procedure in step 4 **without** putting a diskette in any drive. The red light on one and only one drive should come on after you press the appropriate key. Then reset the computer by simultaneously pressing both the **O** key and the **DD** key. Now insert the diagnostic diskette into the boot drive as follows:
 - Place the diskette labeled "Soft-Sectored" in the boot drive if it is connected to the WH-8-37.
 - Place the diskette labeled "Hard-Sectored" in the boot drive if it is connected to the H-17 Controller Board.
 - If none of the drive lights turn on, or if more than one turns on, it will be necessary to refer to the "Disk Drive Configuration" section to define one and only one boot drive. (NOTE: If NO lights turned on, be sure power was applied to the drive(s) before you assume that you will have to reconfigure the drives. Also check to be sure that your WH-8-37 Circuit Board is properly seated in the H-8 and the disk drive cables are properly connected.)
3. Close the disk drive door.
- 4A. If the boot drive is connected to the WH-8-37 and section 4 of SW-1 on your HA-8-6 Circuit board is in position 1, press the **1** key on your Computer's front panel. The display will show:

Pri H37

The drive light will come on and the display will flash as the data is read into your Computer's memory.

- 4B. If the boot drive is connected to the H-17 Controller Board and section 4 of SW-1 on your HA-8-6 Circuit Board is in position 0, press the **0** key. The display will show:

Pri H17

You will hear some clicking noises from the disk drive and its light will turn on and then off again. This is normal. You will hear clicking noises whenever your Computer is reading from or writing to the diskette. The clicks will continue for about 15 seconds. If the terminal does not automatically display the following message, press both the right SHIFT key and RESET key at the same time and then release them. Your terminal will display:

ZENITH DATA SYSTEMS Z37 SUPPORT SYSTEM

ENTER THE NUMBER CORRESPONDING TO THE TYPE
OF THE PROGRAM YOU WISH TO RUN.

1. DISK CONTROLLER CHECKOUT
2. GENERAL DRIVE/CONTROLLER DIAGNOSTIC

YOUR CHOICE ->

From this main menu, you can select either diagnostic utility. To select an option, simply type the number which corresponds to the option on the terminal. When you are finished running either of these two options, the system will return you to this main menu.

Also, you can safely remove all diskettes and turn off the power whenever the main menu is displayed.

OPTION 1: DISK CONTROLLER CHECKOUT

The Disk Controller Checkout is used to verify the operation of the Z-37 Double-Density Disk Controller portion of the WH-8-37 Circuit Board. This diagnostic program turns on the disk drive motors, loads the disk drive read/write heads as a program would if it were trying to read from or write to the disk, and then tries to position and reposition the read/write head. If the program can successfully complete all these tests, it will display a message which indicates that the controller works properly. If the program cannot successfully complete any test, it will display an error message that tells you how to correct the problem.

The Disk Controller Checkout diagnostic will refer to various drive numbers. These numbers are the drive hardware unit numbers, and they range from 0 (zero) through 2. Pay close attention to which drive number the program associates with a drive as it activates it. This "drive hardware unit number" will be referred to frequently throughout these diagnostics.

To run the Disk Controller Checkout, select diagnostic programs' main menu option 1. The terminal will display:

DETAILED CONTROLLER CHECKOUT.

THIS PROGRAM ATTEMPTS TO VERIFY THE OPERATION
OF THE H37 DISK CONTROLLER BOARD.

PLEASE ANSWER THE FOLLOWING QUESTIONS WITH 'Y'
FOR YES AND 'N' FOR NO. BY LOOKING AT YOUR
DISK DRIVES AND VERIFYING PROPER OPERATION.

ARE ALL DRIVE MOTORS TURNING?

Before you respond, open the doors of your soft-sectored 5-1/4" disk drive(s). On the right-hand side of the drive, about two inches back from the drive door, there is a metal cylinder about an inch in diameter. Make sure this cylinder is turning in each of the 5-1/4" disk drive(s) connected to your WH-8-37 Circuit Board. It **does not matter** whether this cylinder is turning in any drives connected to an H-17 Controller Board.

If the drives are not turning, proceed with the following steps; otherwise, respond by pressing the **Y** key and continue with the next section and test drive zero.

1. Check to make sure that the power to the drive is on.
2. If the power is on, check the connection of the ribbon cable on the circuit board (at location Z-37), the connection between the ribbon cable from the circuit board (Z-37) and the ribbon cable from the disk drive, and the connection of the disk drive cable to the disk drive.
3. If the cable is connected correctly, check the jumper selection on the WH-8-37 board and make sure that the Z-37 jumper is in the correct position (ON).
4. If the jumper is correct, check the port select jumper and make sure that they are in a horizontal position as shown in Pictorial 8 (Port 170).
5. Repeat the test.

If you are still experiencing difficulty, refer to the "In Case of Difficulty" section on Page 68.



If you responded by pressing the **Y** key to the preceding question, the terminal will display:

SELECTING DRIVE ZERO.

IF THIS IS A NON-EXISTENT DRIVE FOR YOUR SYSTEM,
ANSWER 'Y' TO THE FOLLOWING QUESTION.

IS DRIVE SELECT LIGHT ON AND HEAD LOADED?

Note that this "Drive Zero" is the drive that you will normally use to boot up, unless you are booting from a hard-sectored diskette that is connected to the H-17 Controller Board or if you are using the Z-67 or H/Z-47 system to boot up.

Check to make sure the red light on drive 0 is glowing. If it is, press the **Y** key, continue with the next section, and test drive one. Otherwise, check the following:

1. Be sure that the drive is jumpered for the proper drive select as discussed in the "Disk Drive Configuration" section on Page 26.
2. Be sure that the ribbon cables are properly connected and are tight.
3. Be sure that the 8-section status port switch on the HA-8-6 Z80 CPU board is set correctly as discussed in the "HA-8-6 Configuration" section.
4. Repeat the test.

If you still experience difficulty, refer to the "In Case of Difficulty" section on Page 68.

If you have responded by pressing the **Y** key to the preceding question, the terminal will display:

SELECTING DRIVE ONE.

IF THIS IS A NON-EXISTENT DRIVE FOR YOUR SYSTEM,
ANSWER 'Y' TO THE FOLLOWING QUESTION.

IS DRIVE SELECT LIGHT ON AND HEAD LOADED?

Check to make sure the red light on drive 1 is glowing. If it is, press the Y key, continue with the next section, and test drive two. Otherwise, check the following:

1. Be sure that the drive is jumpered for the proper drive select, as discussed in the "Disk Drive Configuration" section on Page 26.
2. Be sure that the ribbon cables are properly connected and are tight.
3. Be sure that the 8-section status port switch on the HA-8-6 Z80 CPU board is set correctly as discussed in the "HA-8-6 Configuration" section.
4. Repeat the test.

If you still experience difficulty, refer to the "In Case of Difficulty" section on Page 68.

The program will activate the drive in this way for drive two. You should respond by pressing the Y key if the drive exists and the red light glows, and check the above only if the drive exists but the drive light does not come on.

If all the drive motors work properly and the program was able to successfully select all the drives, the system will now display:

VERIFYING HEAD POSITIONING SYSTEM. STAND BY...

The program will now attempt to position the disk drive zero's read/write head, much as it would as if it were reading from or writing to a diskette. If this test is successful, the program will display:

YOUR CONTROLLER APPEARS TO BE OK. PLEASE CONTINUE
ON TO SELECTION 2 TO MAKE FURTHER CHECKS.

If you do not receive this message, and there is no track indication, call Heath or Zenith Technical Consultation for assistance.

OPTION 2: GENERAL DRIVE/CONTROLLER DIAGNOSTIC

The General Drive/Controller Diagnostic (called "TEST") is a diagnostic utility used to test soft-sectorized 5-1/4" diskettes and disk drives. TEST verifies the drive rotation speed, step rate, read/write mechanism, and the quality of the recording surface of the diskette used for the tests.

You must use the F option (format disk) before you run the tests and format the disk for the diagnostic routines. After you use the diskette to perform "TEST," use an operating system disk formatting program (CP/M FORMAT or HDOS INIT) before you use the diskette for data or program storage.

The amount of time you need to run the tests varies with the number of sides and the density of the media under test. It will take about two hours to run all tests using a single-sided, single-density diskette. It will take about four and a half hours to run all tests using a double-sided, double-density diskette.

Initialiazing the Diagnostic

To run TEST, boot up your system using the Diagnostic Utilities diskette and select the main menu option 2. Your Terminal will display:

```
TEST
VERSION: 2.0
ISSUE #50.07.00
```

```
THIS PROGRAM TESTS YOUR DISK SYSTEM. CERTAIN TESTS
DESTROY THE DATA ON THE VOLUME UNDER TEST. THIS VOLUME MUST
HAVE BEEN INITIALIZED AT LEAST ONCE, AND MAY HAVE TO BE
REINITIALIZED BEFORE BEING USED FOR ANYTHING ELSE.
```

PROCEED (YES/NO)?

If you type YES and press the RETURN key, the program will continue. If you type NO and press the RETURN key, TEST will return you to the diagnostic programs main menu.

If you choose to continue proceed with the following:

1. Remove all diskettes from your disk drives. The terminal will display:

WHICH DRIVE (0/1/2/3)?

2. Now enter the hardware unit number of the drive that you want to test and press the RETURN key. If this is your first time through the test, we recommend that you test drive 0. After you have selected a drive number between 0 and 2 (3 may be selected but it is **not** supported by any other Heath or Zenith software), your Computer's terminal will display the following menu:

FUNCTIONS AVAILABLE:

T - DISPLAY DRIVE ROTATIONAL SPEED	U - SELECT ANOTHER DRIVE UNIT
D - GENERAL DRIVE CHECKOUT	E - EXIT TO BOOT PROGRAM
M - MEDIA CHECK (SECTOR VALIDITY)	A - ALIGN DRIVE HEAD
S - PERFORM SEEK TIME CHECKOUT	F - FORMAT DISK

CTRL-C CANCELS THE TEST IN PROGRESS. OPTION:

To start any test, type the letter that precedes the name of the test in the menu and press the RETURN key. Since you must format the diskette before performing any tests, select menu option **F** by pressing the F key and then press the RETURN key.

Option F: Format Disk

This option prepares a soft-sectorized diskette for use with these diagnostics. However, any data on the diskette will be destroyed, so use a diskette that is new (blank) or one that does **not** contain valuable data.

The option begins by instructing you to insert a diskette into the drive. For instance, if you selected drive 0, the terminal will display:

INSERT THE VOLUME YOU WISH TO FORMAT INTO DRIVE 0,
REMEMBER, ANY DATA ON THIS VOLUME WILL BE DESTROYED.

HIT RETURN WHEN READY.



Insert the diskette into drive 0. If you selected another drive, insert the diskette into that drive, as instructed by the display. Then press the RETURN key. The terminal will now display:

DOUBLE DENSITY <YES>?

If you want to format your disk in double-density (it must be certified for double-density use), press the RETURN key; if you want to format the diskette in single-density, type NO and press the RETURN key. The terminal will display:

DOUBLE SIDED <YES>?

To create a double-sided diskette (it must be certified for double-side use), press the RETURN key. However, you **must** have drives that are capable of double-sided operation, such as H-17-4 disk drives or the Z-37. If you want a single-sided diskette, type NO and press the RETURN key. Your terminal will display:

80 TRACKS <YES>?

To create an 80 track diskette (it must be certified for 96 tpi or 80-track use), you must have the proper drive, such as an H-17-4 or Z-37 system. Press the RETURN key for 80 tracks or type NO, and press the RETURN key for 40 tracks.

The disk drive will come on and you will hear a regular clicking sound as the read/write head steps across the diskette while it is being formatted. When the drive is finished, the terminal will display the TEST menu.

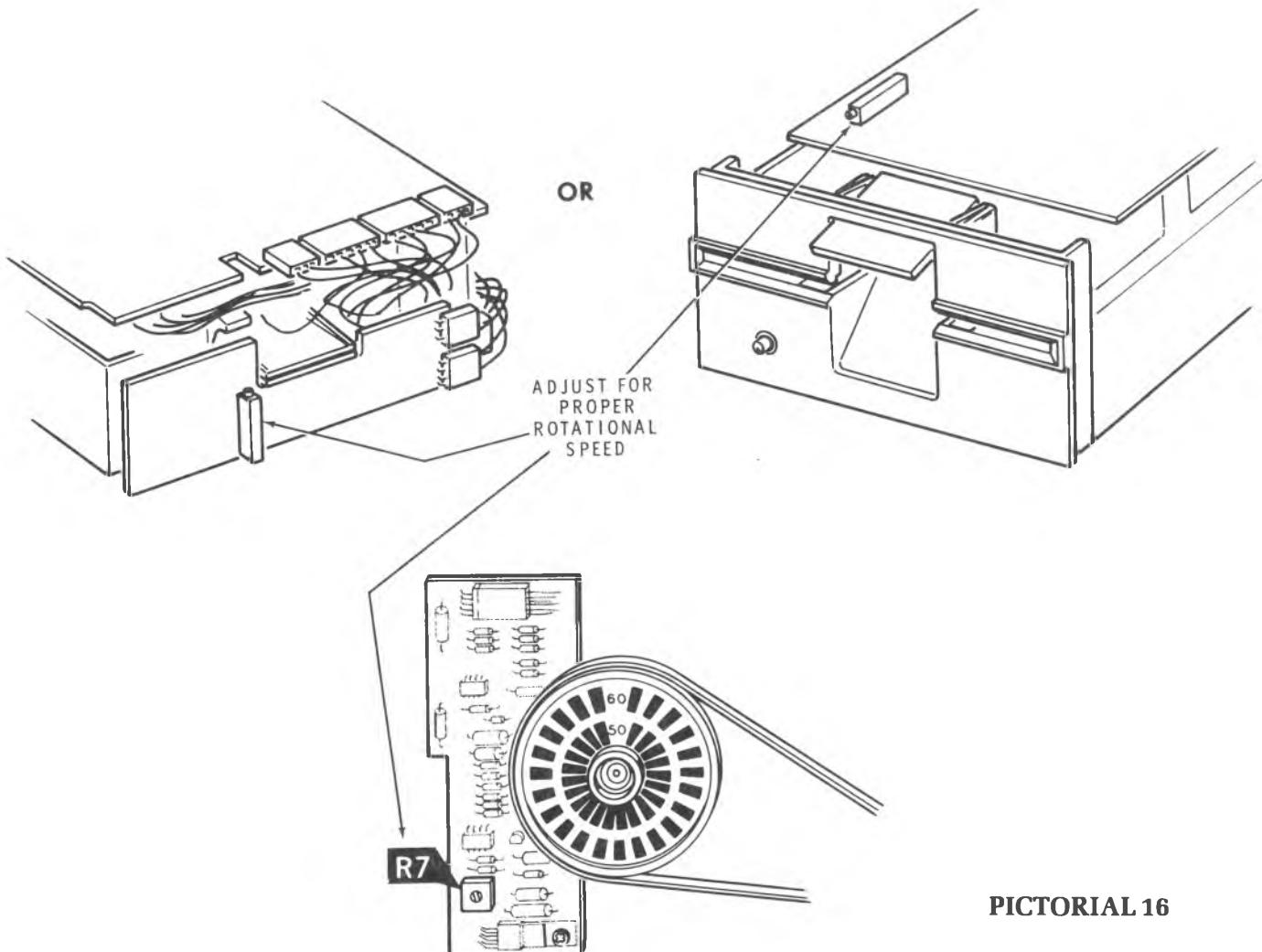
Each time you want to format a diskette for use by the TEST program, use the F option at the TEST menu.

Option T: Display Drive Rotational Speed

The drive speed test checks the speed at which the disk rotates in the selected disk drive. During this test, the relative rotational speed of the drive under test will be shown by displaying a series of decimal numbers, which should be close to 1.000. Since the acceptable speed tolerance is one percent, the final value may safely range anywhere from 0.990 to 1.010. It is not necessary to adjust the speed of any drive unless it is out of tolerance. Allow the test to run for 30 seconds; then press CTRL-C to return to the TEST menu.

If the speed of your disk drive(s) are out of tolerance, the numbers displayed will be either less than 0.990 or greater than 1.010. Using Pictorial 16 as a guide to locate the speed adjustment control on your disk drive, carefully adjust the control with a small screwdriver until the number is within tolerance. The speed adjustment control may be extremely sensitive, so if an adjustment is necessary, do not turn it far in either direction.

You may wish to perform this test periodically, depending on how heavily you use your drive(s). The linear servo loop (which regulates the drive speed) makes the speed stable. But as the drive bearings begin to wear (after many hours of use), the speed may change slightly. Fluctuations within acceptable speeds are normal and are generally attributed to variations in temperature and humidity.



Option D: General Drive Checkout

The purpose of the General Drive Checkout is to verify that your system is reading from — and writing to — the diskette properly. Each sector on the diskette is tested a number of times with various patterns that test the head seek mechanism and the read/write head itself. The test is repeated three times.

Do not be alarmed if this test takes a long time to finish. It is a very thorough test, and requires from 45 minutes to 1-1/2 hours to complete. The duration of the test will depend on the format you used on the diskette under test. Run this test only if you suspect problems in your system.

If you selected drive 0 for your tests, your terminal will display:

INSERT THE DISKETTE YOU WISH TO USE FOR THIS TEST

INTO DRIVE 0, AND HIT RETURN.

READY?

After you have inserted the diskette and pressed the RETURN key, the terminal will display:

3 PASS GENERAL DRIVE TEST FOR UNIT 0

While each pass is being executed, the program will print the letters "ABCDEFG", one after the other, at intervals of a few minutes. These letters indicate the various phases of the test and give you an idea of how far it has progressed.

The program will print an "END OF PASS" message at the end of each test cycle. If everything proceeded normally, without any system or diskette errors, the output for the first pass will read:

ABCDEFG END OF PASS 1

However, if the test discovers any problems on the current pass, the output will include the number of "hard" and "soft" errors, and the display will be similar to:

ABCDE 001/005 FG END OF PASS 1

In this example, test E failed with 1 "hard" error and 5 "soft" errors. The tests corresponding to each letter are:

- A = Write all zeroes
- B = Read all zeroes
- C = Write all ones
- D = Read all ones
- E = Write identification pattern
- F = Read identification pattern
- G = Random read/write test

Let the program run through all three test cycles, even if it discovers errors.

Soft errors usually indicate that the disk drive temporarily had difficulty reading from or writing to the diskette. They may be caused by dust, noise, static electricity, and so forth. Soft errors are nothing to be concerned about as long as they do not exceed one or two an hour; you may correct them by simply repeating the failed test.

If, after you perform ten retries (in an attempt to correct a soft error), the program still cannot perform the read or write operation, TEST reclassifies the soft error as a hard error. Hard errors are usually caused by malfunctions in the electronic or electro-mechanical hardware and/or a defective diskette.

If you have any hard errors, the best approach is to exit this program (type E at the option menu), format another diskette, and repeat the entire TEST procedure. If this approach is successful, it is probably because the first diskette had one or more bad sectors, possibly caused by dust, dirt, or mishandling. If replacing the diskette corrects the hard errors, continue through the other TEST options and then use the U option to restart TEST. Insert the bad diskette and perform a "Media Check" test to identify bad sectors. If the diskette contains bad sectors, discard it. Do not use a defective diskette to store data or programs.

Hard errors that occur on the inside (high numbered) tracks will usually be caused by using diskettes that have not been certified for double-density, double-sided, 80-track use. Format the diskette for single-density, single-sided, 40-track use and test it under the "Media Check" test. A diskette that does not pass the "Media Check" test with a double-density, double-sided, 80-track format, will usually pass as a single-density, single-sided, 40-track diskette, unless it has been physically damaged.

If you are getting both hard and excessive soft errors (more than one or two an hour), and "Media Check" finds nothing wrong with the "bad" disk, you may have a hardware problem.

If changing the diskette does not correct the problem, or if you do suspect that you have hardware problems, refer to the "In Case of Difficulty" section.



Option M: Media Check (Sector Validity)

The media check option will examine the diskette under test for defects in its magnetic oxide coating. If you had any hard or soft errors during the General Drive Checkout, defects in the diskette coating could be the cause. If the media check finds any bad sectors, the bad sector numbers will be listed at the end of the test. Run this test on all new diskettes to confirm the quality of the coating.

The Media Check will take anywhere from 20 to 45 minutes. At the end of the test, the following message will be printed:

nnnn BAD SECTORS LOCATED

The number "nnnn", which can range from 0 to 2560, will show how many of the sectors on the diskette are defective. The bad sector numbers will be listed and should be recorded for future reference. If the media check discovers a bad sector, try using a less demanding format (single-density versus double-density, 40 tracks versus 80, etc.) and run the test again. If media errors still occur when it has been formatted as a single-density, single-sided, 40-track diskette, then throw it away. Do not use it to store data or programs.

Option S: Perform Seek Time Checkout

This test will determine your drive's highest reliable track- to-track (seek time) speed. The H-17-1 drive assemblies are guaranteed to perform reliably with a seek time of 30 milliseconds per track, and H-17-4 drive assemblies are guaranteed to perform reliably with a seek time of 6 milliseconds per track.

The maximum seek speed may change as the drive unit "ages" slightly. If frequent read errors occur with one of your drives, you should rerun this test to check for possible changes in the drive speed.

The program will attempt descending step rates of 30, 20, 12, and 6 milliseconds per track until it has determined your drive's fastest reliable track seek time. The program will print what speed is being attempted as the test is being run. For each successful pass, the program will print the message "OK!" to indicate that the drive performs reliably at that speed. A typical display for an H-17-4 disk drive (Z-37, hardware unit 0) will show:

SEEK TIMING TEST:
SEE THE MANUAL BEFORE RUNNING THIS TEST.

```
*****  
*****  
** NOTE: **  
** 96 T.P.I. DRIVES ARE SPECIFIED TO STEP **  
** AT 6 MS/TRACK, AND 48 T.P.I. DRIVES **  
** ARE SPECIFIED TO STEP AT 30 MS/TRACK. **  
** OCCASIONALLY, DRIVES STEP FASTER THAN **  
** THE SPECIFIED RATE. THIS TEST DETER- **  
** MINES THE MINIMUM STEP RATE FOR YOUR **  
** PARTICULAR DRIVE. HOWEVER, HEATH/ZENITH **  
** DOES NOT GUARANTEE THAT ANY DRIVE WILL **  
** STEP FASTER THAN THE SPECIFIED RATE. **  
**  
** THE H/Z-37 CONTROLLER SUPPORTS STEP **  
** RATES OF: 30 MS, 20 MS, 12 MS, AND 6 MS **  
** PER TRACK.  
*****  
*****
```

PROCEED (YES/NO)? YES

```
TRYING 30 MILLISECONDS PER TRACK - OK!  
TRYING 20 MILLISECONDS PER TRACK - OK!  
TRYING 12 MILLISECONDS PER TRACK - OK!  
TRYING 6 MILLISECONDS PER TRACK  
DRIVE PERFORMS RELIABLY AT 6 MILLISECONDS PER TRACK.
```

When the seek time test is complete, the message "DRIVE PERFORMS RELIABLY AT nn MILLISECONDS PER TRACK." will be printed, where "nn" is the optimum seek time of your drive. Record this number for future reference.

Note that if TEST attempts a pass at 6 milliseconds per track, it may not print the "DRIVE PERFORMS RELIABLY..." message, but instead may "hang up" and stop execution. If the test attempts a speed of 6 milliseconds per track but fails to print the "DRIVE PERFORMS RELIABLY..." message, the fastest reliable seek time is 12 milliseconds per track. If the test stops executing without printing any message, type CTRL-C before you proceed to the next test.

You will probably want to perform this test on your other drives in order to determine the seek speed for all drives in the system. To do this, use the U TEST menu option to change the drive to be tested; then run the seek time test again. Set your operating system seek speed to that of the slowest drive in your system unless the operating system has the ability to use different speeds for different drives.

Option A: Align Drive Head

NOTE: Do not attempt to align the read/write heads of your disk drive(s) unless you are qualified to do so. The read/write heads are aligned at the factory and will seldom, if ever, need realignment.

The align menu option is used when you align the disk drive's read/write head. To use this option you will need an alignment diskette (not included) and the service tools mentioned on Page 49 (also not included). This option causes the disk drive's read/write head to read a track, that you specify, on the disk. The drive will continue to read that track while you adjust the alignment. You can then specify a different track number, and continue the adjustment procedure until the tracks on the alignment diskette produce the desired displays on the oscilloscope. Be sure to read the disk drive manufacturer's instructions and the alignment disk manufacturer's instructions before using this program.

To use the align option, enter **A** and press the RETURN key when the TEST menu is displayed. The program will display (for drive 0):

```
RADIAL HEAD ALIGNMENT:  
WARNING -- CHECK YOUR MANUAL BEFORE PROCEEDING!  
INSERT THE ALIGNMENT DISKETTE IN DRIVE 0.  
HIT RETURN WHEN READY?
```

To begin the alignment procedure, insert the alignment diskette into the drive whose hardware unit number appears in the message and press the RETURN key. The program will display:

```
ENTER TRACK NUMBER <0>
```

At this point, enter the first track number (as directed by the manual provided with the alignment disk) and press the RETURN key. The system will display:

```
ENTER SIDE NUMBER <0>
```

Enter the side number (as per the directions provided with the alignment diskette and/or disk drive) and press the RETURN key. The system will display:

CTRL-C -- REQUEST ANOTHER TRACK
CTRL-C -- RETURN TO MENU

This message instructs you to type CTRL-C once to change the track number which you entered above, or twice in succession to return to the TEST menu.

You will probably need to change the track number at least twice, but this will vary, and you should follow the alignment disk and disk drive manufacturer's instructions. To change the current track number, type CTRL-C once. The program will display:

ENTER TRACK NUMBER <0>

Now enter the new track number and press the RETURN key. The system will again display:

CTRL-C -- REQUEST ANOTHER TRACK
CTRL-C -- RETURN TO MENU

When you have selected all tracks designated in the manufacturer's instructions, and achieved the desired oscilloscope displays for all designated tracks, type CTRL-C twice in succession to return to the TEST menu.

Option U: Select Another Drive Unit

The option will let you select another drive to be tested, or to insert a new diskette. After you have typed U and pressed the RETURN key, TEST will restart itself. When you are asked which drive you want to test, enter the hardware unit number of the drive you want to test. Then you can change diskettes. If you are inserting a new diskette, be sure to use TEST menu option F to format the diskette before you perform any tests.

Note that using the U option will enable you to alternate among your drives for as long as you wish to test them.

Option E: Exit To Boot Program

To exit TEST, type E and press the RETURN key. This will return you to the diagnostic program's main menu.

Calibration

You will need the following equipment to calibrate the Z-37 portion of your WH-8-37 circuit board.

1. A Digital Volt Meter (DVM) with a 3-1/2 digit readout.
2. A calibrated dual-trace oscilloscope with algebraic-add capability and with sweep speeds of 100 ns/cm and 200 ns/cm, and an operating scale of 5V peak-to-peak.
3. (Optional) A frequency counter capable of measuring 2.00 MHz.
4. HDOS with INIT or CP/M with FORMAT software.

If you cannot obtain the proper results in the following steps, refer to the "In Case of Difficulty" section of this manual and correct any difficulties before you proceed.

Refer to Pictorial 8 for the location of the test points when you perform this calibration.

VCO BIAS ADJUSTMENT

Warm up the Computer for a minimum of 15 minutes with the lid closed.

Connect your DVM (positive lead) to test point 1 (TP1) on the WH-8-37 board and connect the negative lead to ground. The reading should be 1.38 to 1.42V (this is the VCO bias voltage). If you do not obtain the proper voltage, adjust control R11.

Disconnect the DVM.

VCO CENTER FREQUENCY ADJUSTMENT (With Frequency Counter)

This is the preferred method of adjusting the VCO's center frequency.

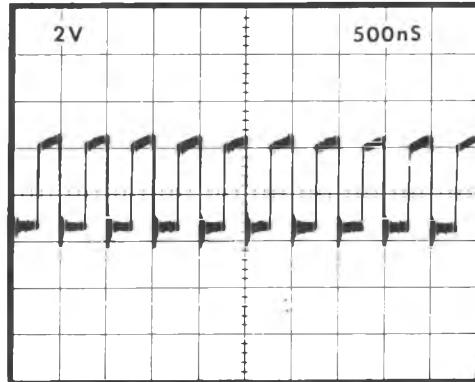
Connect the frequency counter to test point 2 (TP2) on the board. Set the counter to the 100 ms time base. The counter should read from 1975 to 2025 kHz. If it does not, adjust control R13.

Disconnect the counter.

VCO CENTER FREQUENCY ADJUSTMENT (With Oscilloscope)

Connect the oscilloscope's input lead to test point 2 (TP2).

Set the oscilloscope's sweep to 500 ns/cm. The period of the square wave displayed on the screen should be 493 to 506 ns. If it is not, adjust control R13 until you obtain a display similar to Pictorial 17.

PICTORIAL 17

Disconnect the oscilloscope.

PRECOMPENSATION ADJUSTMENT

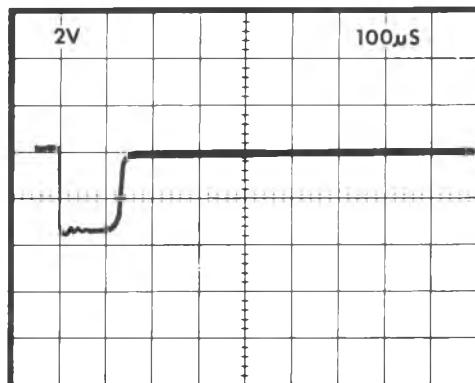
Connect the oscilloscope to test point 3 (TP3).

Set the oscilloscope's sweep to 100 ns/cm.

Using your system's software (INIT in HDOS or FORMAT in CP/M), write on the disk in double-density mode. The period of the pulse displayed on the screen should be 125 to 150 μ s. If it is not, adjust control R6 until you obtain a display similar to Pictorial 18.

Disconnect the oscilloscope.

This completes the calibration of the Z-37 portion of the WH-8-37 circuit board.

PICTORIAL 18

Circuit Description

The Model WH-8-37 Double-Density Disk Controller and Z-67 Interface circuit board allows the H-8 Computer to store and retrieve large quantities of data and programs. The Controller Circuit Board selects the correct drive when two or more drives are used for a write or a read operation and properly handles the flow of data to or from the drive or system. All data and address exchanges between the Controller Circuit Board and the H-8 bus are buffered to protect the H-8 bus from spurious signals.

The Controller Circuit Board contains a soft-sector, double-density disk controller for 5-1/4" disk drives (H-17-1 or H-17-4) and an interface for the Z-67 Winchester Disk Drive. Enabling and control signals from the H-8 Computer are used to select either the Z-37 Controller or the Z-67 Interface by the control decoder (U26). The Z-67 portion of the circuit description is on Page 53.

Refer to the Block Diagram (fold out) of the WH-8-37 Circuit Board, while you read the following description of the Controller.

THEORY OF OPERATION

The Controller's function is to translate and transmit the instructions of the processor to the disk drives. To illustrate this operation, assume that you have instructed the processor to write on disk drive number one. First, the processor sends the proper enabling and control signals over the control lines. These signals are made compatible with the 1797 disk controller by the control decoder and inverter. The controller then blocks all interrupts to the processor (except its own by sending a "block interrupts" signal to the interrupt control ICs). This prevents another peripheral from interfering with the transfer of data between the processor and the disk drive. The controller also signals the buffer direction control IC to allow input from the processor to pass through the data buffer to the controller.

The interface control latch then starts the motor(s) of the disk drive(s) by translating the drive control signals from the processor. The data from the processor is now sent over the data bus, through the 1797, the support logic and disk interface logic, and to drive number one over the serial disk data line (the support logic and disk interface logic help the 1797 disk controller communicate with the drive electronics). The function of each individual IC is described on Page 63.

The read process is similar to the write process. First, the processor sends the proper enabling and control signals over the control lines, just as before (but this time the signals enable the disk controller board to read instead of write). The signals are made compatible with the 1797 disk controller by the control decoder and inverter. The 1797 controller again blocks all interrupts (except its own) to the processor by sending a "block interrupts" signal to the interrupt control ICs, preventing another peripheral from interfering with the transfer of data. The controller also signals the buffer direction control IC to allow output to the processor to pass through the data buffer from the controller. The interface control latch then starts the motor(s) of the disk drive(s) by translating the drive control signals from the processor. Then the data from the disk is sent over the drive serial line, through the disk interface logic, the support logic, the 1797 disk controller, the data buffer, and data bus to the processor.

The phase lock loop (PLL), which is part of the support logic along with the variable control oscillator (VCO), track the frequency of data read from the disk. This tracking generates a read clock (RCLK) signal that tells the disk controller how fast to read the data. (The speed of the incoming data changes due to variations in the rotating speed of the disk and the position of the data on the disk.)

THE Z-67 INTERFACE

Software Theory of Operation

The Z-67 Interface portion of the WH-8-37 Circuit Board has five functions:

1. Input data buffering
2. Output data buffering
3. Status buffering
4. Parity generation and checking
5. Control buffering

This section provides programmers with software information to access the WH-8-37 Z-67 interface and the Z-67 Winchester Disk Drive.

A command is executed in the following manner:

The device driver builds a Command Descriptor Block (CDB) in system memory. The driver then writes the address of the first byte of the CDB into the Command I/O Pointer Block (CIOPB) of the command driver routine. The Data Address (DAD) is also set up if a data transfer is required. Commands requiring data transfers are READ, WRITE, REQUEST SENSE, and REQUEST SYNDROME. The driver now performs a GETCON routine that determines if the controller is busy. If it is not busy, the GETCON routine asserts the SELECT line until the controller responds with a busy. When the controller responds to the Z-67 interface by asserting BUSY, the driver shifts to the OUTCON routine.

In response to the REQ (request) bit in the BSTAT, the driver passes the command a byte at a time to the controller. The controller verifies that the command is correct and begins the command execution phase. At this time, the data is transferred to or from the Z-67 interface and into or out of the main memory. The data transfer may be initiated by an interrupt on receipt of the first REQ after the interrupt enable bit is set in the command register.

After the data transfer is completed, the controller enters the command completion phase. The controller sends a one-byte status to the Z-67 interface, indicating whether or not an error occurred during command execution. This is handled by the CMPSTAT routine. Finally, the controller sends the message byte (of zeros) and the operation is complete.

At this time, the controller enters the idle mode, awaiting another command. If the controller encountered an error, the CMPSTAT routine returns with it in the Y register. It is the responsibility of the device driver to issue a REQUEST SENSE command to request any detailed information about the error.

Interface Register Definition

The registers on the interface board are listed below. The address given assumes the board is jumpered for Port 170. If the board is jumpered for Port 270, add 100 octal to the address given. If the Z-67 is addressed at 174 (or 274), add 4 (or 104) to the address given.

Address Hex Octal	Register
— —	
78 170	Data In/Out Register (DAR)
79 171	Control Register — Write Only (CNR)
	Status Register — Read Only (BSTAT)
7A 172	DIP Switches
Control Register (CNR)	Output Address (79 hex, 171 octal)
Bit 7	Not used
Bit 6	SEL — Assert Select and Data Bit 0 used to access a controller.
Bit 5	INTEN — Interrupt Enable — Causes interrupt if REQ present.
Bit 4	Reset
Bit 3	Not Used
Bit 2	Not Used
Bit 1	Data Enable
Bit 0	Not Used

Bus Status	Input Address (79 Hex, 171 Octal)
Bit 7	REQ — Indicates the controller in the Z-67 either requests data or has data for the interface.
Bit 6	IN/OUT (referenced to controller) — Low indicates data to interface board. High indicates data to controller.
Bit 5	MSG — Indicates last byte in data or command string.
Bit 4	COM/DTA — Is high when a command is being sent to the controller, and is low when data is being sent.
Bit 3	BUSY — Indicates status of busy signal.
Bit 2	PARITY ERROR — Indicates bad parity.
Bit 1	INT IN PROGRESS — Verifies that interrupt has been activated. Reading status port resets interrupt.
Bit 0	ACK — Acknowledges request for data.

Z-67 Interface Bus Pin Assignment

The Z-67 interface is connected to the Z-67 controller through a 40-pin connector.

The pin assignments are as follows:

<u>Signal</u>	<u>Pin No.</u>
DATA0	2
DATA1	4
DATA2	6
DATA3	8
DATA4	10
DATA5	12
DATA6	14
DATA7	16
PARITY	18
_____	20 (spare)
_____	22 (key)
_____	24 (spare)
BUSY	26
ACK	28
RST	30
MSG	32
SEL	34
C/D	36
REQ	38
I/O	40

NOTE: All signals are active low and all odd pins are connected to ground. The signal lines are terminated with 220 ohms to 5 volts and 330 ohms to ground.

Commands

An I/O request to the Z-67 disk controller is performed by passing a command descriptor block (CDR) to the Z-67 Winchester Drive. The first byte of a CDR is the command class and opcode. The remaining bytes specify the drive logical unit number (LUN), block address, control bytes, and number of blocks to transfer. The controller performs an implied seek and verify when it is commanded to access a block.

Refer to your Z-67 Manual for more specific information about the Z-67 disk controller.

COMMAND FORMAT

Commands Requiring 6 Bytes:

Command Byte 0	XXXX
Command Byte 1	XXXX+1
Command Byte 2	XXXX+2
Command Byte 3	XXXX+3
Command Byte 4	XXXX+4
Command Byte 5	XXXX+5

XXXX is the address that is stored in CIOPB.

Commands Requiring 10 Bytes:

Command Byte 0	XXXX
Command Byte 1	XXXX+1
Command Byte 2	XXXX+2
Command Byte 3	XXXX+3
Command Byte 4	XXXX+4
Command Byte 5	XXXX+5
Command Byte 6	XXXX+6
Command Byte 7	XXXX+7
Command Byte 8	XXXX+8
Command Byte 9	XXXX+9

XXXX is the address that is stored in CIOPB.

REQUEST SYNDROME COMMAND

The REQUEST SYNDROME command returns two bytes of information. The data returned for the REQUEST SYNDROME command is listed as follows:

Data Byte 0	XXXX
Data Byte 1	XXXX+1

XXXX is the address that is stored in the DMA location.

DRIVE AND CONTROLLER SENSE INFORMATION

When the REQUEST SENSE command is executed, the controller returns four bytes of information in the following format (refer to the Z-67 Manual for detailed information about these bytes):

Data Byte 0	XXXX
Data Byte 1	XXXX+1
Data Byte 2	XXXX+2
Data Byte 3	XXXX+3

XXXX is the address that is stored in the DMA location.

NOTE: Data that is received from the controller as well as data that is sent to the controller is transferred in the above order.

OTHER COMMANDS

The Z-67 interface uses programmed I/O, taking advantage of the fact that the Z-67 Drive has a built-in sector buffer. The control lines of the interface bus are available to the CPU through the Bus Status and Control registers. Data and commands are transmitted through the interface bus by a simple handshake procedure outlined in this Manual and the Z-67 Manual.

The following types of commands are available to the programmer:

STATUS (Sends drive status from controller to interface)

TEST DRIVE READY
REQUEST SENSE
REQUEST SYNDROME

MOTION CONTROL (Moves heads without read/write operation)

SEEK
RECALIBRATE

R/W (Read/Write Operations)

READ
WRITE
COPY

FORMAT (Formats drive or tracks with specified standard format)

FORMAT TRACK
FORMAT BAD SECTOR
FORMAT DRIVE

COMMAND SEQUENCE

Status Commands:

GET CONTROLLER
SEND COMMANDS (to controller)
READ STATUS DATA
READ COMPLETION STATUS

Motion Control:

GET CONTROLLER
SEND COMMANDS (to controller)
LOAD DATA
READ COMPLETION STATUS

Read/Write Sectors:

GET CONTROLLER
SEND COMMANDS (to controller)
WAIT FOR REQ
READ/WRITE DATA
READ COMPLETION STATUS

Copy:

GET CONTROLLER
SEND COMMANDS (to controller)
READ COMPLETION STATUS

PROGRAMMING

Some definitions (NOTE: Addresses given assume installation at Port 170. Add four for Port 174, 100 for Port 270, and 104 for Port 274.)

BASE	equals	Base I/O Address (78 Hex, 170 Octal)
DATAIN	equals	BASE
DATAOUT	equals	BASE
BCON	equals	BASE + 1 (Bus Control)
BSTAT	equals	BASE + 1 (Bus Status)
CIOPB	is	Command Address
DMA	is	Data Address

Some sample assembly programs follow.

Get Controller

```

GETCON: IN     BSTAT    ; input from status port
        ANI    08H      ; select bit 3 (busy)
        JNZ    GETCON   ; if busy wait in GETCON loop
        MVI    A, 40H   ; get ready to assert SEL and DATA0
        OUT    BCON     ; to get attention of controller
CBUSY:  IN     BSTAT    ; input from bus status
        ANI    08H      ; again look at busy - arrived at
        JZ     CBUSY    ; "Controller Attention" else loop
        MVI    A, 02H   ; get ready to allow data enable
        OUT    BCON     ; done
        RET

```

Output Commands

```

OUTCOM: LHLD   CIOPB    ; load pointer to command queue
COMREQ: IN      BSTAT    ; input from bus status
        MOV    C, A     ; store in C
        ORA    A         ; set flags
        JP     COMREQ   ; wait for REQ
        ANI    10H      ; check for command/data
        RZ
        MOV    A, C     ; also see if controller switched
        ANI    40H      ; direction
        RZ
        MOV    A, M     ; move commands from queue to accumulator
        OUT    DATAOUT   ; write commands to controller
        INX    H         ; increment pointer
        JMP    COMREQ   ; loop as long as commands are requested
                           ; from controller

```

Write Data to Z-67 Winchester Drive

```

WRITE: LHLD DMA ; load pointer to data
DAREQ: IN BSTAT ; input from bus status
        MOV C,A ; store
        ANI 80H ; set flags
        JZ DAREQ ; wait for REQ
        ANI 10H ; check for COM
        JNZ CMPSTAT ; on receipt of command completion status
                      ; is present
        MOV A,M ; move data into accumulator
        OUT DATAOUT ; output to controller
        INX H ; increment pointer
        JMP DAREQ ; go back for another byte
CMPSTAT: IN DATAIN ; input completion status
        MOV C,A ; place in C for further use
LREQ:   IN BSTAT ; looking for last REQ
        MOV B,A ; save for checking
        ANI 80H ; check for REQ
        JZ LREQ ; loop until found
        IN DATAIN ; input last byte
        ORA A ; see if last byte is non-zero
        JNZ BADBYTE ; if last byte is non-zero
        MOV A,C ; now check completion status
        ORA A ; to see if it is zero
        JNZ BADSTAT ; if not zero
        MOV A,B ; now check last bus status
        ANI 10H ; for parity error
        JNZ BADPAR ; high is bad parity
        XRA A ; zero accumulator
        RET ; return

```

Read Data from Z-67 Winchester Drive

```

READ:  LHLD DMA ; load data pointer
RDREQ: IN BSTAT ; input bus status
        MOV C,A ; store for further checking
        ANI 80H ; look for REQ
        JZ RDREQ ; else loop
        MOV A,C
        ANI 10H ; check for COM
        JNZ CMPSTAT ; if COM present must be completion
                      ; status
        IN DATAIN ; input data from controller
        MOV M,A ; move data to pointer
        INX H ; increment pointer
        JMP RDREQ

```

Circuit Description

The Model WH-8-37 Double-Density Disk Controller and Z-67 Interface circuit board allows the H-8 Computer to store and retrieve large quantities of data and programs. The controller circuit board selects the correct drive when two or more drives are used for a write or a read operation and properly handles the flow of data to or from the drive or system. All data and address exchanges between the controller circuit board and the H-8 bus are buffered to protect the H-8 bus from spurious signals.

The Controller Circuit Board contains a soft-sector, double-density disk controller for 5-1/4" disk drives (H-17-1 or H-17-4) and an interface for the Z-67 Winchester Disk Drive. Enabling and control signals from the H-8 Computer are used to select either the Z-37 controller or the Z-67 interface by the control decoder (U26). The Z-37 portion is described on Page 51.

Refer to the Block Diagram (fold out) of the WH-8-37 Circuit Board, while you read the following description of the Interface.

HARDWARE THEORY OF OPERATION

Data is read and written through the bidirectional data buffer, the read/write data latches, and the data transceivers. The data transceivers communicate with the Z-67 transition and controller boards (in the Z-67).

Read/Write control, status buffering, and resets are accomplished by the control signal decoder, interrupt logic, status buffer, control latch, and reset/acknowledge latch and generator. These circuits communicate with the Z-67 Winchester Disk Drive through the control line drive and receive buffers.

Parity generation and checking is accomplished by the data parity generator/checker. When a write is performed, the WH-8-37 Controller Circuit Board sends a parity bit to the Z-67 drive along with the data word. When a read is performed, the interface checks the parity bit sent from the Winchester Disk Drive to determine if the data is correct.

The positions of the DIP switches are read through the DIP switch buffer and data bus, although they are not currently used by Heath or Zenith Data Systems software.

Please refer to the schematic (fold-out) as you read the following description.

Reset Operation

When the Computer is turned on, it sends a reset signal to the WH-8-37 Controller Board Z-67 interface circuits. This reset clears whatever state the circuits happen to be in. The reset signal comes in at pin 29, is buffered by U24, and resets control latch U16, interrupt logic U5A and U5B, and divide-by-eight counter U27.

Read Operation

When the Computer wants to read data from the Winchester Disk Drive, it sends control signals to the disk drives through U35 and U36, the bidirectional buffers (which are normally set to allow input from the Computer rather than input from the drives). The control signals travel over the internal data bus to control latch U16, which passes the SEL (drive select) control signal to the drives through the buffer U1 and the Z-67 cable.

When the proper drive receives the select signal, it responds with a BUSY signal, which the Computer reads from status buffer U19 by changing the direction of buffers U35 and U36 with a IORD signal. The Computer then removes the select signal from the line by resetting control latch U16. The Winchester drive responds with a REQ, or request, signal. This signal is ANDed with a 67 REQ INT EN (Z-67 request interrupt enable) at U7B to produce an interrupt to the Computer via buffer U6B (The REQ INT EN comes from the U16 control latch).

The other control signals are ACK hold (Acknowledge hold) and REQ INT EN (request interrupt enable). The first is used to prevent the Z-67 controller from asserting a REQ to the interface, while the latter allows the drives to interrupt the Computer (However, in the standard system software, interrupts are not used, so REQ INT EN is ignored).

Another control signal that comes from the data bus is the software controllable reset signal (data bit 4). This data bit is routed directly to reset latch U4A. From there, the reset is strobed by counter U27 to buffer U1B, where it is passed on to the drives.

To continue the read process after receiving an interrupt, the Computer sends an IORD (I/O Read) through U25 into U26 where RD DATA is generated when the proper port is addressed by signals from the Computer (decoded by ICs U15, U25, and U14). RD DATA causes data to be read from the appropriate disk drive (or partition), while RD SWITCH allows the DIP switch DS1 to be read.

RD DATA enables the read latch U9. RD DATA also sets the acknowledge flip flop U8B (through OR gate U7A), sending an acknowledge signal to the Z-67 Winchester drive (by means of buffer U1C) that tells it that the interrupt was received.

Data can now be transmitted from the Z-67 Winchester Disk Drive unit to the H-8 Computer.

Write Operation

When the Computer needs to write data to the Winchester Drive, it sends control signals to the disk drives through U35 and U36. The drives respond with the same handshaking procedure as before. However, instead of receiving an IORD, an IOWR is received by the Controller Board at pin 21.

The IOWR (I/O write) signal is received and decoded in the same manner as the IORD. The resulting signal activates the LD DATA (load data) and LD CON (load control) lines from U26. LD DATA enables the write latch U21 and the acknowledge flip flop U8B (through or gate U7A). The acknowledgment tells the Winchester that data will now be written onto the drive that was selected.

CIRCUIT FUNCTION DESCRIPTIONS

IC Function Descriptions

U1 Open Collector Buffer (Z-67) -- U1 buffers control signals acknowledge, reset, select, and data bit 0.

U2 NAND Gates (Z-67) -- U2 combines (NAND's) signals (in the parity and acknowledge circuits) that must be present together for an operation to occur. (U2D is not used.)

U3 Buffer Inverter (Z-67) -- U3 performs the double function of inverting and isolating the PARITY, I/O, REQ, and RST signal lines to and from the Z-67.

U4 Reset Flip-Flop (Z-67) -- U4 generates a reset under software control. The reset is strobed by the divide-by-eight counters to the Computer. (U4B is not used.)

U5 Interrupt Flip-Flops (Z-67) -- U5, in conjunction with U6B and U7B, determines if a request interrupt from the Winchester Drive may occur.

U6 and U7 NAND Gates (Z-67) -- U6 and U7 combines (NAND's) signals that must be present for an operation to occur. (U6A and U6C are not used.)

U8 Parity and Acknowledge Flip-Flops (Z-67) -- U8A latches the parity signal from the parity checker (U10) and sends it to the status buffer (U19), through which the condition of legal parity may be checked by the Computer. U8B latches the request signal from the Winchester Disk Drive and sends back an acknowledge, unless the acknowledge hold signal from control latch (U16) is active.

U9 Read Latch (Z-67) -- U9 latches data signals from the transceivers U11 and U12. The latched signals are sent to the bidirectional buffers (U35 and U36) on the internal data bus for transmission to the Computer during a RD DATA cycle.

U10 Parity Generator/Checker (Z-67) -- U10 generates a parity bit on a write cycle and checks parity on a read cycle. It checks for even or odd parity, depending on where the PARITY ODD/EVEN jumper is set. Normally, PARITY ODD is set, producing odd parity.

U11 and U12 Tranceivers (Z-67) -- U11 and U12 are line drivers/receivers that accept write data from U21 and read data from the Z-67 transmission cable.

U13 Write Delay Flip-Flop -- U13 provides a necessary two-step delay of the leading edge of the IOWR signal.

U14 Port Address NAND Gate -- U14 combines (NAND's) address lines A3 through A7 to produce a signal indicating port 170 through 177 (or 270 through 277 depending upon the port jumper position) has been addressed. The port jumper is normally in the 170 base address position.

U15 Bus Buffers -- The address bus and the data bus on the H8 mother board use inverted logic signals. The inverters in U15 complement and buffer the address lines A3 through A7. (U15H is not used.)

U16 Control Latch (Z-67) -- U16 latches the select control signals from the Computer to the Winchester Drive. U16 also latches the acknowledge hold and request interrupt control signals from the Computer to the rest of the Z-67 interface on the Controller Board.

U17 Disk Drive Interface Buffers (Z-37) -- The disk drive interface ICs buffer all signals to and from the disk drive electronics by means of open collector drivers. (U17E is not used.)

U18 Read Data DIP Switch Buffer (Z-67) -- U18 buffers the DIP switch condition on the read cycle only. It is enabled by the SWITCH (read switch) line.

U19 Status Buffer (Z-67) -- U19 buffers the status lines from the Winchester Drive to the internal data bus.

U20 Interface Control Latch (Z-37) -- U20 latches the high speed processor signals for the 1797 disk controller (U33) and support circuitry (U31 and U32). Some commands, such as MOTOR, go directly from U20 to the disk drive interface ICs, U17, U29, and U38, rather than through the 1797.

U21 Write Latch (Z-67) -- U21 latches the data signals from the internal data bus and sends them to the transceivers (U11 and U12).

U22A Reset Pulse Latch (Z-37) -- The address control latch helps call up the registers in the 1797 — either the track and sector registers or the C/S and data registers, depending on how data bit 0 is set on the interface control latch (U20).

U22B Buffer Direction Control (Z-37) -- An additional 8-bit data buffer (U34) is provided between the internal data bus and the 1797. The direction of the buffer is controlled by U22B.

U23 Open Collector NAND Gates (Z-37) -- These four gates invert: the processor system clock for use by the 1797, the interrupts from the 1797 to the processor, and the addressing information from the processor to all parts of the Z-37 controller section of the board. (U23D is not used.)

U24 Control Decoder and Inverter (Z-37) -- U24 is designed to decode address and read and write conditions for the Z-37 portion of the Controller Board. Using addresses A0, A1, and A2, it determines whether the board is being addressed, which register is being addressed, and whether the signal is a read-enabled or write-enable signal.

U25 Inverter Bus Buffers -- U25 complements and buffer the control lines A0, A1, IORD, IOWR, and the CPU clock 02. (U25H is not used.)

U26 Control Decoder -- U26 enables the Z-37 controller circuits or the Z-67 interface circuits depending upon the setting of the status port switch on the Z80 CPU Circuit Board and the Z-37 and Z-67 jumpers. The control decoder provides the direction control signals to the U35 and U36 bidirectional data buffers and it also decodes the read and write signals from the Computer and produces RD DATA, LD DATA, RD STATUS, LD CON, and RD SWITCH signals for the Z-67 circuits.

U27 and U28 Divide-by-Eight Counters (Z-67) -- U27 and U28 divide the Computer's system clock signal to help U4A generate the reset signal.

U29 Disk Drive Buffers (Z-37) -- U29 buffers and inverts the write protect (WRPT), track (TROO), sector index (INDEX) and data (READ DATA) signals coming from the 5-1/4" disk drives to the 1797. (U29E, U29F, U29G, and U29H are not used.)

U30A Raw Read Monostable (Z-37) -- U30A lengthens the raw read pulse from the disk drive electronics to a size readable by the 1797 (U33).

U30B Write Data Monostable (Z-37) -- U30B lengthens and shapes the write pulse to a size usable by the disk drive.

U31, U32, and U39 Phase-Lock-Loop Tracking and Precompensation (Z-37) -- U32 supplies U39 with either a pull-up (PU) or pull-down (PD) signal. This signal is then filtered by C45 and R9 and called FC (frequency control). The Voltage Control Oscillator (VCO), U39, raises its frequency with a PU signal and lowers it with a PD signal. The change in frequency produces a corresponding change in the rotation speed of the 5-1/4" disk drive.

Variable resistor R11 is used to bias the PU and PD output at 1.4 volts (this means that PU/PD are 1.4 volts when the phase lock is inactive). This allows the phase lock to more quickly lock on to the data being read. Variable resistor R13 is used to adjust the VCO's center frequency to 2 MHz.

The VCO's output is divided down by U32 to become the read clock (RCLK) signal used by the 1797 to separate disk data and disk clock signals.

U32 also strobes the early and late signals for data precompensation. These internally latched signals determine which phase of a four-phase clock generator, U31, will be used for the precompensation process. All phases are identical in pulse width (+ or - 50 nsec). The phase delay time is set by R6.

Precompensation, used for 80-track, double-density disk write operations, places data properly on the disk so that it can be read back with minimum error. Error is introduced by the shifting of old data that is adjacent to new data as it is written, due to the nature of the magnetic medium of the diskette.

U31, the precompensation clock generator, provides the clock signals needed for the precompensation of the write signals.

U33 1797-02 Disk Controller (Z-37) -- The internal logic of the 1797 disk controller is discussed in Appendices A and B on Pages A-1 and B-1. Refer to the appendices for information about the 1797's operation.

U34 Data Buffer (Z-37) -- The data buffer is a bidirectional, eight-bit buffer between the internal data bus and the 1797 disk controller whose direction is controlled by U22B, the buffer direction control.

U35 and U36 Bidirectional Data Buffers -- The U35 and U36 buffer allows data to pass either as input or output between the Computer and the internal (on board) data bus, depending on the condition of the IOWR write line or IORD read line. In other words, if the IOWR write line is enabled, U35 and U36 will admit only input from the Computer. If the IORD read line is enabled, U35 and U36 will admit only output to the Computer.

U37, U42, and U43 Interrupt Control (Z-37) -- U43 is taken from the processor CPU board. This is the processor's interrupt channel and is relocated onto the Z-37 portion of the disk controller board so that the disk controller can block all other interrupts to the processor except its own. U42 screens the interrupt signals to the processor under U20's direction. U43 turns the eight-bit interrupts to the processor into three-bit interrupt signals. The three-bit interrupt becomes part of an eight-bit data instruction via U37. U37 supplies five other hardwired bits. For more information about U37, consult the HA-8-6 Manual.

U38 Drive Buffer (Z-37) -- U38 buffers the control and data signals to the disk drive.

U39 Voltage-Controlled Oscillator (Z-37) -- U39 provides a variable clock frequency to control the speed of the disk drive. Refer to the discussion under "U31, U32, and U39 Phase-Lock-Loop Tracking and Precompensation."

U40A Head Load Delay (Z-37) -- U40A is a monostable multivibrator that delays the controller's response to commands. This allows the drive head to settle after it is selected.

U40B Reset Pulse Delay (Z-37) -- The reset pulse from the processor does not meet the minimum reset pulse requirements of the 1797. To correct this, U40B lengthens the reset pulse to an interval sufficient to meet the 1797's specifications.

U41 Disk Controller Clock (Z-37) -- U41 is fed by the 16 MHz clock oscillator which divides the input by 16, producing a 1 MHz clock signal with a 50% duty cycle.

U42 and U43 (Z-37) -- U42 and U43 are part of the interrupt control. Refer to "U37, U42, and U43 Interrupt Control."

Power Supply

With the exception of the WD 1697 controller chip (U33), all circuits on the controller circuit board are powered by 5-volts DC. The 8-volt unregulated input from the H-8 bus is regulated by three 5-volt regulators, U101, U102, and U103. Capacitors C101, C102, C103, C104, C105, C106, C107, and C108 ensure that the regulators remain stable.

The unregulated +18-volt input from the H-8 bus is regulated by the 12-volt regulator, U103. Capacitors C109 and C110 ensure that the regulator remains stable.

IN CASE OF DIFFICULTY

Troubleshooting Information

The WH-8-37 Interface Board was not designed to be user-serviceable. If it does not function properly, or if the Computer does not boot or read disks, check the jumpers on the Interface Board for the following settings:

Parity	Odd
Parity Error	On
Pre Comp	Off
Z-67 Reset	32
Port	170
Z-67	On (If connected)
Z-37	On (If connected)
Z-67 INT	Off

DIP switch (DS1) settings are defined by your software needs. Consult your operating system manual for proper switch settings. If your system does not read the DIP switch, you can leave the switch in any position.

Make sure the correct ROM's and ROM jumpers are installed on the CPU board.

Make sure the WH-8-37 and HA-8-6 boards are seated correctly on the backplane and are not installed a pin or two off.

Make sure the data cable between the HA-8-6 and WH-8-37 boards are properly connected and that pin 1 (marked with a triangle) is lined up with the notch on the DIP socket.

Make sure the cables to your disk drives are secure and properly lined up.

Make sure the configuration of the 8-section status port switch is properly set.

If you have a Z-67, make sure that it has been properly prepared. This means that you may have to run the PREP program prior to partitioning the hard disk for use. Also be aware that CP/M requires that partitions (other than the first) be assigned each time the Z-67 is started from a cold boot (unless the partition is used as the boot partition).

To boot from the floppy drive in the Z-67, you must follow the Universal boot procedure. Although the Z-67 (during single key primary or secondary boot procedure) will only boot from the Winchester Disk, the floppy drive is considered (under CP/M) as the third hardware unit in the system.

Refer to the following chart to see if the problem you are having is listed. If it is, check the items in the "Possible Cause" column to help you locate the area of trouble.

PROBLEM	POSSIBLE CAUSE
Drive access light does not turn on when disk is booted.	<ol style="list-style-type: none"> 1. Check for proper connection of cables inside the computer. 2. Be sure the disk drive unit(s) are turned on. 3. Check U13 on the CPU circuit board for proper part and installation. 4. Check for proper installation of jumper wires on CPU circuit board. 5. Check for proper installation of the jumpers on the WH-8-37.
All disk access lights turn on and remain on.	A cable is connected with the marked edge on the wrong side.
Two drives turn on when a boot operation is selected.	Two drives have their disk selection jumpers programmed the same. See "Disk Drive Configuration" on Page 26.
The disk appears to boot but the terminal screen remains blank except for the cursor in the upper left-hand corner of the screen.	<ol style="list-style-type: none"> 1. Terminal is "Off Line." 2. The terminal has not been reset (press the right SHIFT key and RESET at the same time).

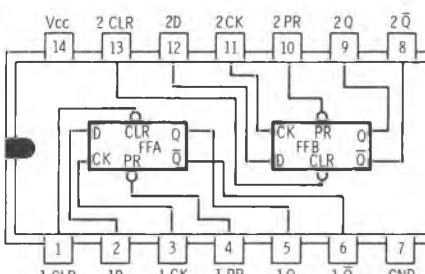
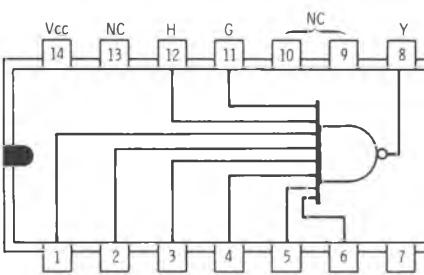
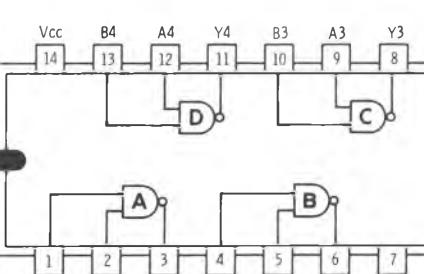
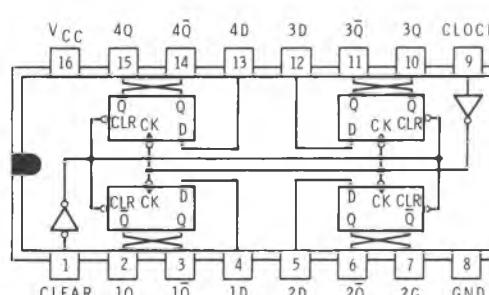
If your Interface Board needs servicing, call the nearest Heathkit Customer Center. **IMPORTANT:** Be prepared to furnish the following information. It will be helpful in diagnosing and repairing your unit.

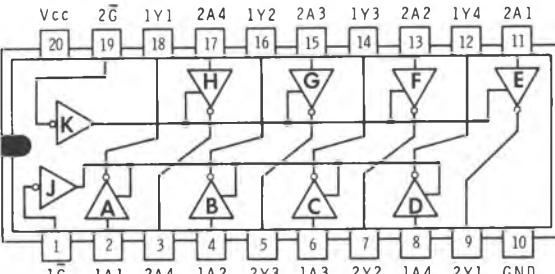
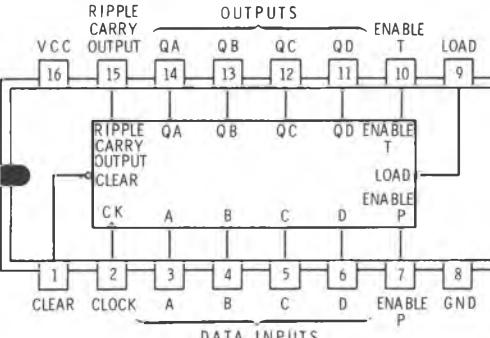
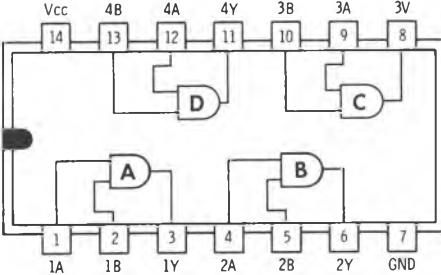
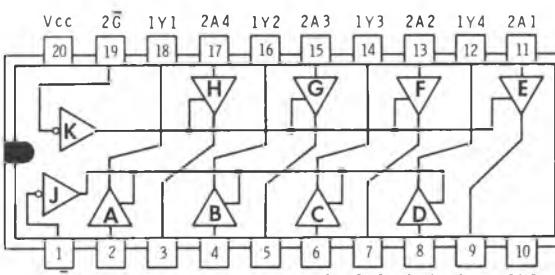
1. The problem you are having.
2. Name and model of your computer system.
3. Baud rate.
4. System configuration.
5. Any additional information that will help describe your system.

PARTS IDENTIFICATION**Semiconductor Identification Charts**

CIRCUIT COMPONENT NUMBER	HEATH PART NUMBER	CIRCUIT COMPONENT NUMBER	HEATH PART NUMBER
U1	443-77	U25	443-754
U2	443-792	U26	444-117
U3	443-872	U27	443-757
U4	443-730	U28	443-757
U5	443-730	U29	443-791
U6	443-77	U30	443-90
U7	443-780	U31	443-1000
U8	443-730	U32	443-998
U9	443-863	U33	443-997
U10	443-1001	U34	443-885
U11	443-819	U35	443-754
U12	443-819	U36	443-754
U13	443-730	U37	443-791
U14	443-732	U38	443-73
U15	443-754	U39	443-999
U16	443-752	U40	443-1040
U17	443-73	U41	443-757
U18	443-791	U42	444-82
U19	443-754	U43	443-912
U20	443-805	U101	442-54
U21	443-805	U102	442-627
U22	443-730	U103	442-644
U23	443-745	U104	442-54
U24	444-81		

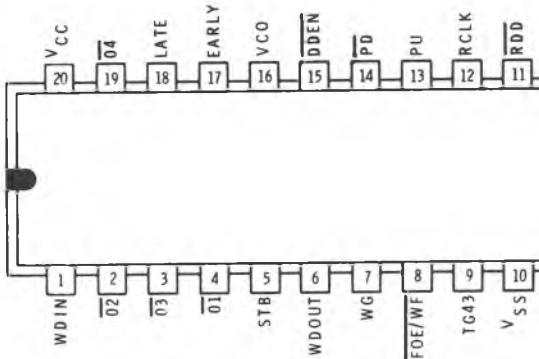
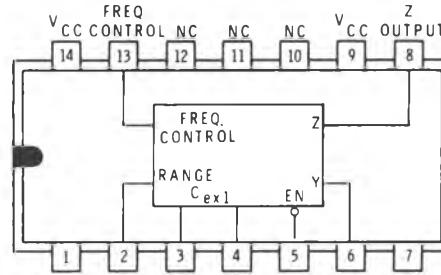
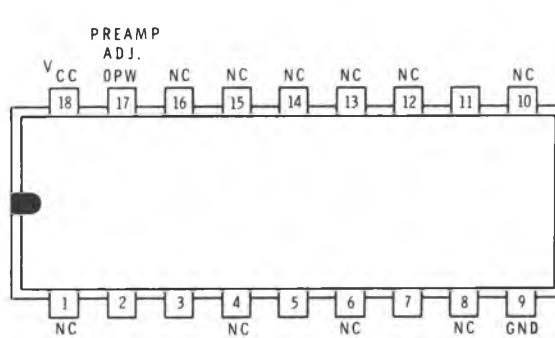
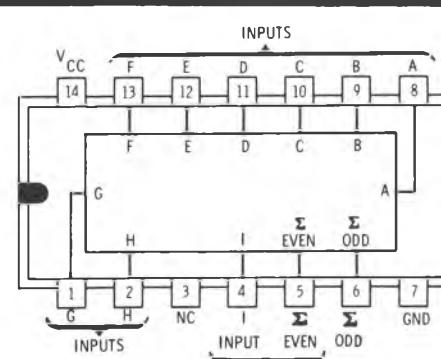
HEATH ID PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	
442-54	UA7805	5V VOLTAGE REGULATOR	
442-627	78L05	5V VOLTAGE REGULATOR	
442-644	LM78L12	+12V VOLTAGE REGULATOR	
443-73	SN7416N	HEX BUFFER (open collector)	
443-77	SN7438N	QUAD 2-INPUT NAND GATE (open collector)	
443-90	SN74123N	MULTIVIBRATOR RETRIGGER	

HEATH ID PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	
443-730	74LS74	DUAL D FLIP FLOP	
443-732	74LS30	8-INPUT NAND GATE	
443-745	74LS03P	QUAD LATCH	
443-752	74LS175	QUAD D FLIP FLOP	

HEATH ID PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	
443-754	74LS240	INVERTING OCTAL BUFFER 3-STATE	
443-757	74LS161	SYNCHRONOUS DIVIDE BY 16 COUNTER	
443-780	74LS08	QUAD 2-INPUT AND GATE	
443-791	74LS244	NON-INVERTING OCTAL BUFFER 3-STATE	

HEATH ID PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	
443-792	74LS132	QUAD 2-INPUT SCHMITT TRIGGER	
443-805	74LS273	8 BIT LATCH	
443-819	DS8838	QUAD BUS TRANSCEIVER (open collector)	
443-863	74LS374	8 BIT 3-STATE LATCH	

HEATH ID PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	
443-872	74LS14	HEX SCHMITT TRIGGER INVERTER	
443-885	74LS245	NON-INVERTING, 3-STATE, OCTAL BUS TRANSCEIVER	
443-912	74LS148	ENCODER	
443-997	FD1797B02	DISK CONTROLLER	

HEATH ID PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	
443-998	1691WD	PHASE LOCK LOOP	
443-999	LS 7468624	VCO	
443-1000	2143-01	FOUR PHASE CLOCK	
443-1001	74LS280	PARTY GENERATOR/CHECKER	

HEATH ID PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	
443-1040	96LS02	MULTIVIBRATOR	
444-81	N/A	LOGIC ARRAY U24	
444-82	N/A	LOGIC ARRAY U42	
444-117	N/A	LOGIC ARRAY U26	

Replacement Parts List

CIRCUIT Comp. No.	HEATH Part No.	DESCRIPTION
RESISTORS		
R1-R3	6-103-12	10 k ohm 1/4-watt
R4-R5	6-1002-12	10 k ohm 1/4-watt 1%
R6	10-1138	10 k ohm 3/4-watt control
R7	6-222-12	2200 ohm 1/4-watt
R8	6-473-12	47 k ohm 1/4-watt
R9	6-680-12	68 ohm 1/4-watt
R10	6-473-12	47 k ohm 1/4-watt
R11	10-1180	100 k ohm 1/2-watt control
R12	6-103-12	10 k ohm 1/4-watt
R13	10-1154	10 k ohm 1/2-watt control
R14	6-103-12	10 k ohm 1/4-watt
R15	6-124-12	120 k ohm 1/4-watt
R16	6-104-12	1000 ohm 1/4-watt
R17	6-332-12	3300 ohm 1/4-watt
R18-R36	6-102-12	1000 ohm 1/4-watt
RP1-RP3	9-123	220/330 ohm (6) resistor pack
RP4	9-119	10 k ohm (8) resistor pack
RP5	9-120	150 ohm (5) resistor pack

CAPACITORS

C1-C38	21-769	.01 µF, 50 V ceramic
C39	25-925	4.7 µF, 50 V electrolytic
C40-C41	21-769	.01 µF, 50 V ceramic
C42	20-188	30 pF, 500 V mica
C43	20-148	100 pF, 500 V mica
C44	21-744	82 pF, 50 V ceramic
C45	27-217	.68 µF, 100 V mylar
C46	25-925	4.7 µF, 50 V electrolytic
C47-C48	21-769	.01 µF, 50 V ceramic
C49	25-925	4.7 µF, 50 V electrolytic
C50	21-192	.1 µF, 50 V ceramic
C51-C54	21-769	.01 µF, 50 V ceramic
C55	21-141	.0033 µF, 100 V ceramic
C56	25-197	1.0 µF, 25 V tantalum
C101-C104	25-924	2.2 µF, 50 V electrolytic
C105	25-883	47 µF, 35 V electrolytic
C106	21-192	.1 µF, 50 V ceramic
C107	25-924	2.2 µF, 50 V electrolytic
C108	21-769	.01 µF, 50 V ceramic
C109-C110	25-924	2.2 µF, 50 V electrolytic

INDUCTORS

L1-L6	235-229	35 µH, RF Choke
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CIRCUIT Comp. No.	HEATH Part No.	DESCRIPTION

INTEGRATED CIRCUITS

See "Semiconductor Identification Chart"

CABLE

134-1241	16-conductor ribbon cable
134-1243	34-conductor ribbon cable
134-1244	40-conductor ribbon cable
134-1269	34-conductor ribbon cable

MISCELLANEOUS

DS1	60-621	8-section DIP switch
OSC	150-107	16 MHz crystal oscillator
	204-2308	H-8 heat sink bracket
	250-56	6-32 x 1/4" pan head screw
	252-3	6-32 nut
	254-1	#6 lockwasher
	266-966	H-8 bus connector key
	432-1041	Female Berg connector (65474-001)
	432-1063	Male Molex connector (08-50-0114)
	432-1076	Female crimp Molex connector (22-16-2251)
	432-1080	Female shell Molex connector (10-17-2032)
	432-1102	Male Molex connector (22-10-2031)
	432-1121	Male connector (3M-3432-2002)
	432-1171	Male Molex connector (22-10-2021)
	434-253	40-pin socket
	434-298	14-pin socket
	434-299	16-pin socket
	434-310	18-pin socket
	434-311	20-pin socket
	434-320	Socket (3M-3431-2002)
	434-310	18-pin socket
	434-311	20-pin socket
	434-320	Socket (3M-3431-2002)

Appendix A

FD179X DATA INFORMATION

The following pages are reprinted with the permission of Western Digital Corporation.

WESTERN DIGITAL
C O R P O R A T I O N

FD179X-02 FLOPPY DISK FORMATTER/CONTROLLER FAMILY

FEATURES

- TWO VFO CONTROL SIGNALS — RG & VFOE
- SOFT SECTOR FORMAT COMPATIBILITY
- AUTOMATIC TRACK SEEK WITH VERIFICATION
- ACCOMMODATES SINGLE AND DOUBLE DENSITY FORMATS
 - IBM 3740 Single Density (FM)
 - IBM System 34 Double Density (MFM)
 - Non IBM Format for Increased Capacity
- READ MODE
 - Single/Multiple Sector Read with Automatic Search or Entire Track Read
 - Selectable 128, 256, 512 or 1024 Byte Sector Lengths
- WRITE MODE
 - Single/Multiple Sector Write with Automatic Sector Search
 - Entire Track Write for Diskette Formatting
- SYSTEM COMPATIBILITY
 - Double Buffering of Data 8 Bit Bi-Directional Bus for Data, Control and Status
 - DMA or Programmed Data Transfers
 - All Inputs and Outputs are TTL Compatible
 - On-Chip Track and Sector Registers/Comprehensive Status Information

- PROGRAMMABLE CONTROLS
 - Selectable Track to Track Stepping Time
 - Side Select Compare
- WRITE PRECOMPENSATION
- WINDOW EXTENSION
- INCORPORATES ENCODING/DECODING AND ADDRESS MARK CIRCUITRY
- FD1792/4 IS SINGLE DENSITY ONLY
- FD1795/7 HAS A SIDE SELECT OUTPUT

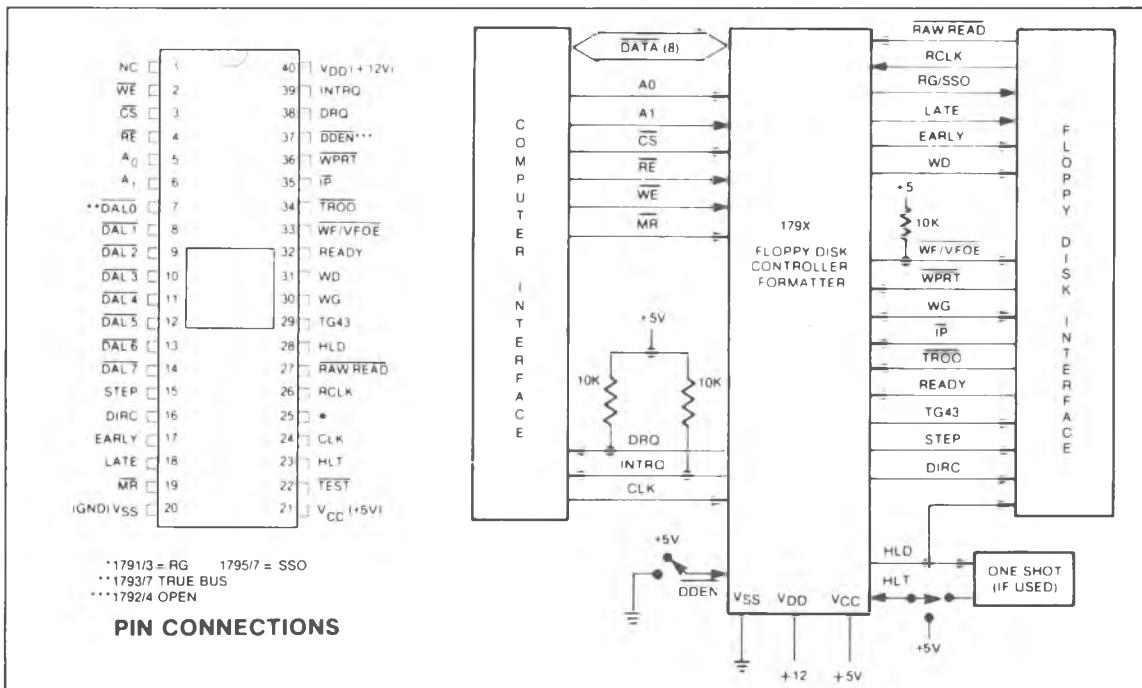
AUGUST, 1981

179X-02 FAMILY CHARACTERISTICS

FEATURES	1791	1792	1793	1794	1795	1797
Single Density (FM)	X	X	X	X	X	X
Double Density (MFM)	X		X		X	X
True Data Bus			X	X		X
Inverted Data Bus	X	X			X	
Write Precomp	X	X	X	X	X	X
Side Selection Output					X	X

APPLICATIONS

8" FLOPPY AND 5 1/4" MINI FLOPPY CONTROLLER
SINGLE OR DOUBLE DENSITY
CONTROLLER/FORMATTER



FD179X SYSTEM BLOCK DIAGRAM

PIN OUTS

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION																									
1	NO CONNECTION	NC	Pin 1 is internally connected to a back bias generator and must be left open by the user.																									
19	MASTER RESET	MR	A logic low (50 microseconds min.) on this input resets the device and loads HEX 03 into the command register. The Not Ready (Status Bit 7) is reset during MR ACTIVE. When MR is brought to a logic high a RESTORE Command is executed, regardless of the state of the Ready signal from the drive. Also, HEX 01 is loaded into sector register.																									
20	POWER SUPPLIES	Vss	Ground																									
21		Vcc	+ 5V ± 5%																									
40		Vdd	+ 12V ± 5%																									
COMPUTER INTERFACE:																												
2	WRITE ENABLE	WE	A logic low on this input gates data on the DAL into the selected register when CS is low.																									
3	CHIP SELECT	CS	A logic low on this input selects the chip and enables computer communication with the device.																									
4	READ ENABLE	RE	A logic low on this input controls the placement of data from a selected register on the DAL when CS is low.																									
5,6	REGISTER SELECT LINES	A0, A1	These inputs select the register to receive/transfer data on the DAL lines under RE and WE control: <table> <thead> <tr> <th>CS</th> <th>A1</th> <th>A0</th> <th>RE</th> <th>WE</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>Status Reg</td> <td>Command Reg</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>Track Reg</td> <td>Track Reg</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>Sector Reg</td> <td>Sector Reg</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>Data Reg</td> <td>Data Reg</td> </tr> </tbody> </table>	CS	A1	A0	RE	WE	0	0	0	Status Reg	Command Reg	0	0	1	Track Reg	Track Reg	0	1	0	Sector Reg	Sector Reg	0	1	1	Data Reg	Data Reg
CS	A1	A0	RE	WE																								
0	0	0	Status Reg	Command Reg																								
0	0	1	Track Reg	Track Reg																								
0	1	0	Sector Reg	Sector Reg																								
0	1	1	Data Reg	Data Reg																								
7-14	DATA ACCESS LINES	DAL0-DAL7	Eight bit Bidirectional bus used for transfer of data, control, and status. This bus is receiver enabled by WE or transmitter enabled by RE. Each line will drive 1 standard TTL load.																									
24	CLOCK	CLK	This input requires a free-running 50% duty cycle square wave clock for internal timing reference, 2 MHz ± 1% for 8" drives, 1 MHz ± 1% for mini-floppies.																									
38	DATA REQUEST	DRQ	This open drain output indicates that the DR contains assembled data in Read operations, or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR in Read or Write operations, respectively. Use 10K pull-up resistor to +5.																									
39	INTERRUPT REQUEST	INTRQ	This open drain output is set at the completion of any command and is reset when the STATUS register is read or the command register is written to. Use 10K pull-up resistor to +5.																									
FLOPPY DISK INTERFACE:																												
15	STEP	STEP	The step output contains a pulse for each step.																									
16	DIRECTION	DIRC	Direction Output is active high when stepping in, active low when stepping out.																									
17	EARLY	EARLY	Indicates that the WRITE DATA pulse occurring while Early is active (high) should be shifted early for write precompensation.																									
18	LATE	LATE	Indicates that the write data pulse occurring while Late is active (high) should be shifted late for write precompensation.																									

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
22	TEST	TEST	This input is used for testing purposes only and should be tied to +5V or left open by the user unless interfacing to voice coil actuated steppers.
23	HEAD LOAD TIMING	HLT	When a logic high is found on the HLT input the head is assumed to be engaged. It is typically derived from a 1 shot triggered by HLD.
25	READ GATE (1791, 1792, 1793, 1794)	RG	This output is used for synchronization of external data separators. The output goes high after two Bytes of zeros in single density, or 4 Bytes of either zeros or ones in double density operation.
25	SIDE SELECT OUTPUT (1795, 1797)	SSO	The logic level of the Side Select Output is directly controlled by the 'S' flag in Type II or III commands. When U = 1, SSO is set to a logic 1. When U = 0, SSO is set to a logic 0. The SSO is compared with the side information in the Sector I.D. Field. If they do not compare Status Bit 4 (RNF) is set. The Side Select Output is only updated at the beginning of a Type II or III command. It is forced to a logic 0 upon a MASTER RESET condition.
26	READ CLOCK	RCLK	A nominal square-wave clock signal derived from the data stream must be provided to this input. Phasing (i.e. RCLK transitions) relative to RAW READ is important but polarity (RCLK high or low) is not.
27	RAW READ	RAW READ	The data input signal directly from the drive. This input shall be a negative pulse for each recorded flux transition.
28	HEAD LOAD	HLD	The HLD output controls the loading of the Read-Write head against the media.
29	TRACK GREATER THAN 43	TG43	This output informs the drive that the Read/Write head is positioned between tracks 44-76. This output is valid only during Read and Write Commands.
30	WRITE GATE	WG	This output is made valid before writing is to be performed on the diskette.
31	WRITE DATA	WD	A 200 ns (MFM) or 500 ns (FM) output pulse per flux transition. WD contains the unique Address marks as well as data and clock in both FM and MFM formats.
32	READY	READY	This input indicates disk readiness and is sampled for a logic high before Read or Write commands are performed. If Ready is low the Read or Write operation is not performed and an interrupt is generated. Type I operations are performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7.
33	WRITE FAULT VFOE ENABLE	WF/VFOE	This is a bi-directional signal used to signify writing faults at the drive, and to enable the external PLO data separator. When WG = 1, Pin 33 functions as a WF input. If WF = 0, any write command will immediately be terminated. When WG = 0, Pin 33 functions as a VFOE output. VFOE will go low during a read operation after the head has loaded and settled (HLT = 1). On the 1795/7, it will remain low until the last bit of the second CRC byte in the ID field. VFOE will then go high until 8 bytes (MFM) or 4 bytes (FM) before the Address Mark. It will then go active until the last bit of the second CRC byte of the Data Field. On the 1791/3, VFOE will remain low until the end of the Data Field. This pin has an internal 100K Ohm pull-up resistor.
34	TRACK 00	TR00	This input informs the FD179X that the Read/Write head is positioned over Track 00.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
35	INDEX PULSE	IP	This input informs the FD179X when the index hole is encountered on the diskette.
36	WRITE PROTECT	WPRT	This input is sampled whenever a Write Command is received. A logic low terminates the command and sets the Write Protect Status bit.
37	DOUBLE DENSITY	DDEN	This input pin selects either single or double density operation. When DDEN = 0, double density is selected. When DDEN = 1, single density is selected. This line must be left open on the 1792/4.

GENERAL DESCRIPTION

The FD179X are N-Channel Silicon Gate MOS LSI devices which perform the functions of a Floppy Disk Formatter/Controller in a single chip implementation. The FD179X, which can be considered the end result of both the FD1771 and FD1781 designs, is IBM 3740 compatible in single density mode (FM) and System 34 compatible in Double Density Mode (MFM). The FD179X contains all the features of its predecessor the FD1771, plus the added features necessary to read/write and format a double density diskette. These include address mark detection, FM and MFM encode and decode logic, window extension, and write precompensation. In order to maintain compatibility, the FD1771, FD1781, and FD179X designs were made as close as possible with the computer interface, instruction set, and I/O registers being identical. Also, head load control is identical. In each case, the actual pin assignments vary by only a few pins from any one to another.

The processor interface consists of an 8-bit bi-directional bus for data, status, and control word transfers. The FD179X is set up to operate on a multiplexed bus with other bus-oriented devices.

The FD179X is TTL compatible on all inputs and outputs. The outputs will drive ONE TTL load or three LS loads. The 1793 is identical to the 1791 except the DAL lines are TRUE for systems that utilize true data busses.

The 1795/7 has a side select output for controlling double sided drives, and the 1792 and 1794 are "Single Density Only" versions of the 1791 and 1793 respectively. On these devices, DDEN must be left open.

ORGANIZATION

The Floppy Disk Formatter block diagram is illustrated on page 5. The primary sections include the parallel processor interface and the Floppy Disk interface.

Data Shift Register — This 8-bit register assembles serial data from the Read Data input (RAW READ) during Read operations and transfers serial data to the Write Data output during Write operations.

Data Register — This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command the Data Register holds the address of the desired Track position. This register is loaded from the DAL and gated onto the DAL under processor control.

Track Register — This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write, and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when the device is busy.

Sector Register (SR) — This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR) — This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the new command is a force interrupt. The command register can be loaded from the DAL, but not read onto the DAL.

Status Register (STR) — This 8-bit register holds device Status information. The meaning of the Status bits is a function of the type of command previously executed. This register can be read onto the DAL, but not loaded from the DAL.

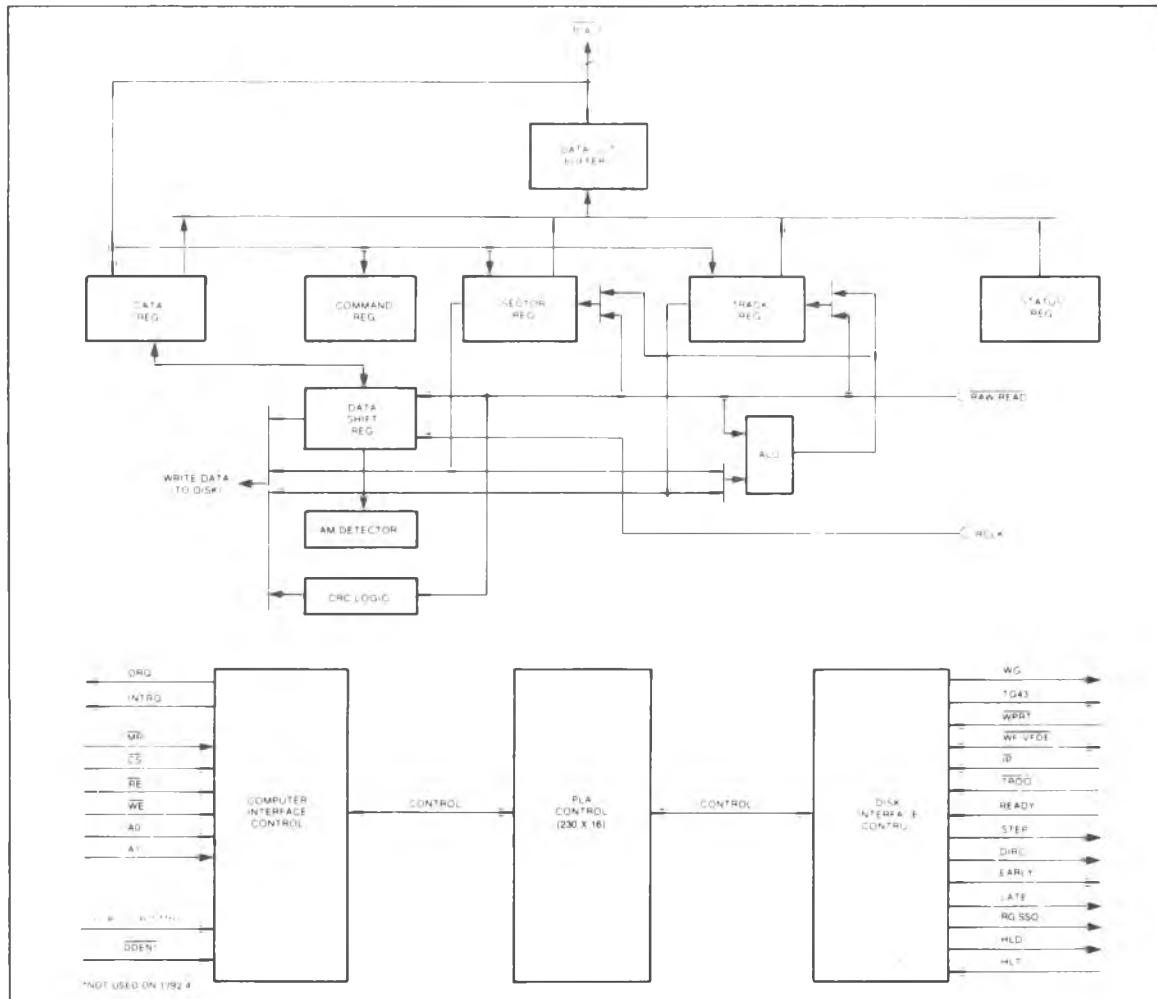
CRC Logic — This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is: $G(x) = x^8 + x^{12} + x^5 + 1$.

The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

Arithmetic/Logic Unit (ALU) — The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.

Timing and Control — All computer and Floppy Disk Interface controls are generated through this logic. The internal device timing is generated from an external crystal clock.

The FD179X has two different modes of operation according to the state of DDEN. When DDEN = 0 double density (MFM) is assumed. When DDEN = 1, single



FD179X BLOCK DIAGRAM

density (FM) is assumed. 1792 & 1794 are single density only.

AM Detector — The address mark detector detects ID, data and index address marks during read and write operations.

PROCESSOR INTERFACE

The interface to the processor is accomplished through the eight Data Access Lines (DAL) and associated control signals. The DAL are used to transfer Data, Status, and Control words out of, or into the FD179X. The DAL are three state buffers that are enabled as output drivers when Chip Select (CS) and Read Enable (RE) are active (low logic state) or act as input receivers when CS and Write Enable (WE) are active.

When transfer of data with the Floppy Disk Controller is required by the host processor, the device address is decoded and CS is made low. The address bits A1 and A0, combined with the signals RE during a Read operation or WE during a Write operation are interpreted as selecting the following registers:

A1 - A0	READ (RE)	WRITE (WE)
0 0	Status Register	Command Register
0 1	Track Register	Track Register
1 0	Sector Register	Sector Register
1 1	Data Register	Data Register

During Direct Memory Access (DMA) types of data transfers between the Data Register of the FD179X and the processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost, by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.

On Disk Write operations the data Request is activated when the Data Register transfers its contents to the Data

Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

At the completion of every command an INTRQ is generated. INTRQ is reset by either reading the status register or by loading the command register with a new command. In addition, INTRQ is generated if a Force Interrupt command condition is met.

The 179X has two modes of operation according to the state of DDEN (Pin 37). When DDEN = 1, single density is selected. In either case, the CLK input (Pin 24) is at 2 MHz. However, when interfacing with the mini-floppy, the CLK input is set at 1 MHz for both single density and double density.

GENERAL DISK READ OPERATIONS

Sector lengths of 128, 256, 512 or 1024 are obtainable in either FM or MFM formats. For FM, DDEN should be placed to logical "1." For MFM formats, DDEN should be placed to a logical "0." Sector lengths are determined at format time by the fourth byte in the "ID" field.

Sector Length Table*	
Sector Length Field (hex)	Number of Bytes in Sector (decimal)
00	128
01	256
02	512
03	1024

*1795/97 may vary — see command summary.

The number of sectors per track as far as the FD179X is concerned can be from 1 to 255 sectors. The number of tracks as far as the FD179X is concerned is from 0 to 255 tracks. For IBM 3740 compatibility, sector lengths are 128 bytes with 26 sectors per track. For System 34 compatibility (MFM), sector lengths are 256 bytes/sector with 26 sectors/track; or lengths of 1024 bytes/sector with 8 sectors/track. (See Sector Length Table)

For read operations in 8" double density the FD179X requires RAW READ Data (Pin 27) signal which is a 200 ns pulse per flux transition and a Read clock (RCLK) signal to indicate flux transition spacings. The RCLK (Pin 26) signal is provided by some drives but if not it may be derived externally by Phase lock loops, one shots, or counter techniques. In addition, a Read Gate Signal is provided as an output (Pin 25) on 1791/92/93/94 which can be used to inform phase lock loops when to acquire synchronization. When reading from the media in FM, RG is made true when 2 bytes of zeroes are detected. The FD179X must find an address mark within the next 10 bytes; otherwise RG is reset and the search for 2 bytes of zeroes begins all over again. If an address mark is found within 10 bytes, RG remains true as long as the FD179X is deriving any useful information from the data stream. Similarly for MFM, RG is made active when 4 bytes of "00" or "FF" are detected. The FD179X must find an address mark within the next 16 bytes, otherwise RG is reset and search resumes.

During read operations (WG = 0), the VFOE (Pin 33) is provided for phase lock loop synchronization. VFOE will go active low when:

- a) Both HLT and HLD are True
- b) Settling Time, if programmed, has expired
- c) The 179X is inspecting data off the disk

If WF/VFOE is not used, leave open or tie to a 10K resistor to +5.

GENERAL DISK WRITE OPERATION

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the FD179X before the Write Gate signal can be activated.

Writing is inhibited when the Write Protect input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set. The Write Fault input, when activated, signifies a writing fault condition detected in disk drive electronics such as failure to detect write current flow when the Write Gate is activated. On detection of this fault the FD179X terminates the current command, and sets the Write Fault bit (bit 5) in the Status Word. The Write Fault input should be made inactive when the Write Gate output becomes inactive.

For write operations, the FD179X provides Write Gate (Pin 30) and Write Data (Pin 31) outputs. Write data consists of a series of 500 ns pulses in FM (DDEN = 1) and 200 ns pulses in MFM (DDEN = 0). Write Data provides the unique address marks in both formats.

Also during write, two additional signals are provided for write precompensation. These are EARLY (Pin 17) and LATE (Pin 18). EARLY is active true when the WD pulse appearing on (Pin 30) is to be written EARLY. LATE is active true when the WD pulse is to be written LATE. If both EARLY and LATE are low when the WD pulse is present, the WD pulse is to be written at nominal. Since write precompensation values vary from disk manufacturer to disk manufacturer, the actual value is determined by several one shots or delay lines which are located external to the FD179X. The write precompensation signals EARLY and LATE are valid for the duration of WD in both FM and MFM formats.

READY

Whenever a Read or Write command (Type II or III) is received the FD179X samples the Ready input. If this input is logic low the command is not executed and an interrupt is generated. All Type I commands are performed regardless of the state of the Ready input. Also, whenever a Type II or III command is received, the TG43 signal output is updated.

COMMAND DESCRIPTION

The FD179X will accept eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The one exception is the Force Interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types. Commands and types are summarized in Table 1.

TABLE 1. COMMAND SUMMARY

A. Commands for Models: 1791, 1792, 1793, 1794

B. Commands for Models: 1795, 1797

Type	Command	Bits								Bits							
		7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r1	r0	0	0	0	0	h	V	r1	r0
I	Seek	0	0	0	1	h	V	r1	r0	0	0	0	1	h	V	r1	r0
I	Step	0	0	1	T	h	V	r1	r0	0	0	0	1	T	h	V	r1
I	Step-in	0	1	0	T	h	V	r1	r0	0	1	0	T	h	V	r1	r0
I	Step-out	0	1	1	T	h	V	r1	r0	0	1	1	1	T	h	V	r1
II	Read Sector	1	0	0	m	S	E	C	0	1	0	0	m	L	E	U	0
II	Write Sector	1	0	1	m	S	E	C	a0	1	0	1	m	L	E	U	a0
III	Read Address	1	1	0	0	0	E	0	0	1	1	0	0	0	E	U	0
III	Read Track	1	1	1	0	0	E	0	0	1	1	1	0	0	E	U	0
III	Write Track	1	1	1	1	0	E	0	0	1	1	1	1	0	E	U	0
IV	Force Interrupt	1	1	0	l1	l3	l2	l1	l0	1	1	0	1	l3	l2	l1	l0

TABLE 2. FLAG SUMMARY

FLAG SUMMARY

Command Type	Bit No(s)	Description																				
I	0, 1	r1 r0 = Stepping Motor Rate See Table 3 for Rate Summary																				
I	2	V = Track Number Verify Flag V = 0, No verify V = 1, Verify on destination track																				
I	3	h = Head Load Flag h = 0, Load head at beginning h = 1, Unload head at beginning																				
I	4	T = Track Update Flag T = 0, No update T = 1, Update track register																				
II & III	0	a0 = Data Address Mark a0 = 0, FB (DAM) a0 = 1, F8 (deleted DAM)																				
II	1	C = Side Compare Flag C = 0, Disable side compare C = 1, Enable side compare																				
II & III	1	U = Update SSO U = 0, Update SSO to 0 U = 1, Update SSO to 1																				
II & III	2	E = 15 MS Delay E = 0, No 15 MS delay E = 1, 15 MS delay																				
II	3	S = Side Compare Flag S = 0, Compare for side 0 S = 1, Compare for side 1																				
II	3	L = Sector Length Flag <table border="1"><tr><td></td><td colspan="4">LSB's Sector Length in ID Field</td></tr><tr><td></td><td>00</td><td>01</td><td>10</td><td>11</td></tr><tr><td>L = 0</td><td>256</td><td>512</td><td>1024</td><td>128</td></tr><tr><td>L = 1</td><td>128</td><td>256</td><td>512</td><td>1024</td></tr></table>		LSB's Sector Length in ID Field					00	01	10	11	L = 0	256	512	1024	128	L = 1	128	256	512	1024
	LSB's Sector Length in ID Field																					
	00	01	10	11																		
L = 0	256	512	1024	128																		
L = 1	128	256	512	1024																		
II	4	m = Multiple Record Flag m = 0, Single record m = 1, Multiple records																				
IV	0-3	lx = Interrupt Condition Flags l0 = 1 Not Ready To Ready Transition l1 = 1 Ready To Not Ready Transition l2 = 1 Index Pulse l3 = 1 Immediate Interrupt, Requires A Reset l3-l1 = 0 Terminate With No Interrupt (INTRQ)																				

*NOTE: See Type IV Command Description for further information.

TYPE I COMMANDS

The Type I Commands include the Restore, Seek, Step, Step-In, and Step-Out commands. Each of the Type I Commands contains a rate field ($f_0 f_1$), which determines the stepping motor rate as defined in Table 3.

A $2\ \mu s$ (MFM) or $4\ \mu s$ (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the direction output. The chip will step the drive in the same direction it last stepped unless the command changes the direction.

The Direction signal is active high when stepping in and low when stepping out. The Direction signal is valid $12\ \mu s$ before the first stepping pulse is generated.

The rates (shown in Table 3) can be applied to a Step-Direction Motor through the device interface.

TABLE 3. STEPPING RATES

CLK	2 MHz	2 MHz	1 MHz	1 MHz	2 MHz	1 MHz
DDEN	0	1	0	1	x	x
R1 R0	TEST=1	TEST=1	TEST=1	TEST=1	TEST=0	TEST=0
0 0	3 ms	3 ms	6 ms	6 ms	$184\mu s$	$368\mu s$
0 1	6 ms	6 ms	12 ms	12 ms	$190\mu s$	$380\mu s$
1 0	10 ms	10 ms	20 ms	20 ms	$198\mu s$	$396\mu s$
1 1	15 ms	15 ms	30 ms	30 ms	$208\mu s$	$416\mu s$

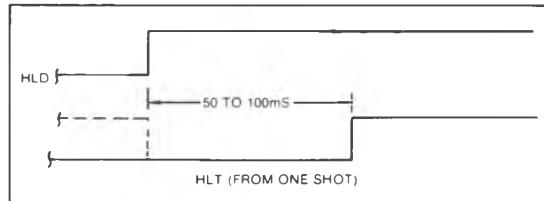
After the last directional step an additional 15 milliseconds of head settling time takes place if the Verify flag is set in Type I commands. Note that this time doubles to 30 ms for a 1 MHz clock. If TEST = 0, there is zero settling time. There is also a 15 ms head settling time if the E flag is set in any Type II or III command.

When a Seek, Step or Restore command is executed an optional verification of Read-Write head position can be performed by setting bit 2 ($V = 1$) in the command word to a logic 1. The verification operation begins at the end of the 15 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete and an INTRQ is generated with no errors. If there is a match but not a valid CRC, the CRC error status bit is set (Status bit 3), and the next encountered ID field is read from the disk for the verification operation.

The FD179X must find an ID field with correct track number and correct CRC within 5 revolutions of the media; otherwise the seek error is set and an INTRQ is generated. If $V = 0$, no verification is performed.

The Head Load (HLD) output controls the movement of the read/write head against the media. HLD is activated at the beginning of a Type I command if the h flag is set ($h = 1$), at the end of the Type I command if the verify flag ($V = 1$), or upon receipt of any Type II or III command. Once HLD is active it remains active until either a Type I command is received with ($h = 0$ and $V = 0$); or if the FD179X is in an idle state (non-busy) and 15 index pulses have occurred.

Head Load timing (HLT) is an input to the FD179X which is used for the head engage time. When $HLT = 1$, the FD179X assumes the head is completely engaged. The head engage time is typically 30 to 100 ms depending on drive. The low to high transition on HLD is typically used to fire a one shot. The output of the one shot is then used for HLT and supplied as an input to the FD179X.



HEAD LOAD TIMING

When both HLD and HLT are true, the FD179X will then read from or write to the media. The "and" of HLD and HLT appears as status Bit 5 in Type I status.

In summary for the Type I commands: if $h = 0$ and $V = 0$, HLD is reset. If $h = 1$ and $V = 0$, HLD is set at the beginning of the command and HLT is not sampled nor is there an internal 15 ms delay. If $h = 0$ and $V = 1$, HLD is set near the end of the command, an internal 15 ms occurs, and the FD179X waits for HLT to be true. If $h = 1$ and $V = 1$, HLD is set at the beginning of the command. Near the end of the command, after all the steps have been issued, an internal 15 ms delay occurs and the FD179X then waits for HLT to occur.

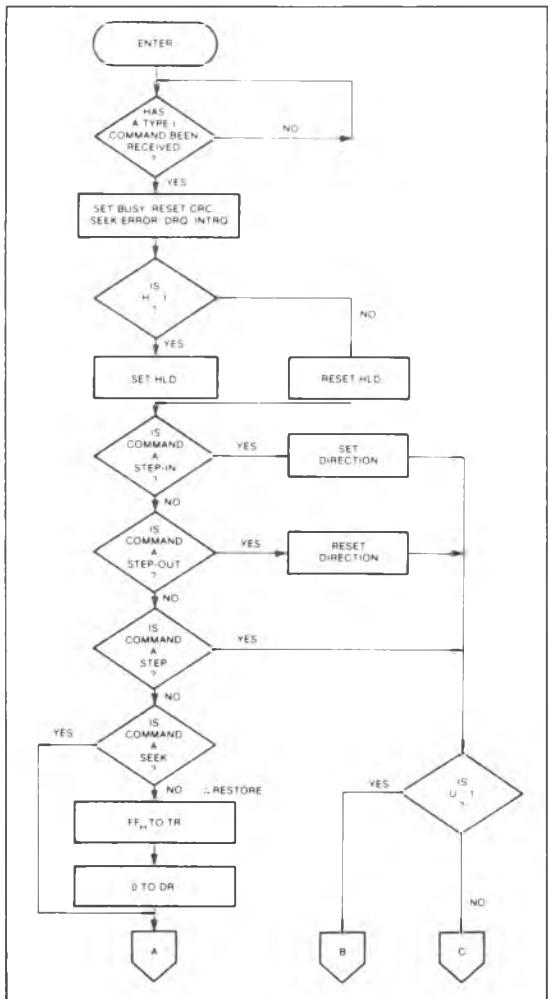
For Type II and III commands with E flag off, HLD is made active and HLT is sampled until true. With E flag on, HLD is made active, an internal 15 ms delay occurs and then HLT is sampled until true.

RESTORE (SEEK TRACK 0)

Upon receipt of this command the Track 00 (TR00) input is sampled. If TR00 is active low indicating the Read-Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If TR00 is not active low, stepping pulses (pins 15 to 16) at a rate specified by the $f_1 f_0$ field are issued until the TR00 input is activated. At this time the Track Register is loaded with zeroes and an interrupt is generated. If the TR00 input does not go active low after 255 stepping pulses, the FD179X terminates operation, interrupts, and sets the Seek error status bit. A verification operation takes place if the V flag is set. The h bit allows the head to be loaded at the start of command. Note that the Restore command is executed when MR goes from an active to an inactive state and that the DRQ pin stays low.

SEEK

This command assumes that the Track Register contains the track number of the current position of the Read-Write head and the Data Register contains the desired track number. The FD179X will update the Track register and issue stepping pulses in the appropriate direction until the contents of the Track register are equal to the contents of



TYPE I COMMAND FLOW

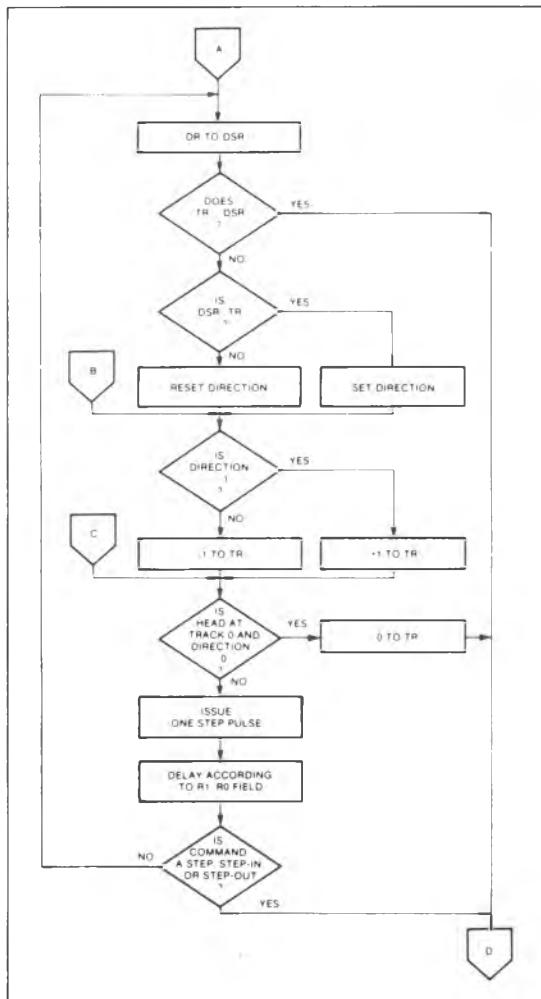
the Data Register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command. Note: When using multiple drives, the track register must be updated for the drive selected before seeks are issued.

STEP

Upon receipt of this command, the FD179X issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r1f0 field, a verification takes place if the V flag is on. If the U flag is on, the Track Register is updated. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-IN

Upon receipt of this command, the FD179X issues one stepping pulse in the direction towards track 76. If the U



TYPE I COMMAND FLOW

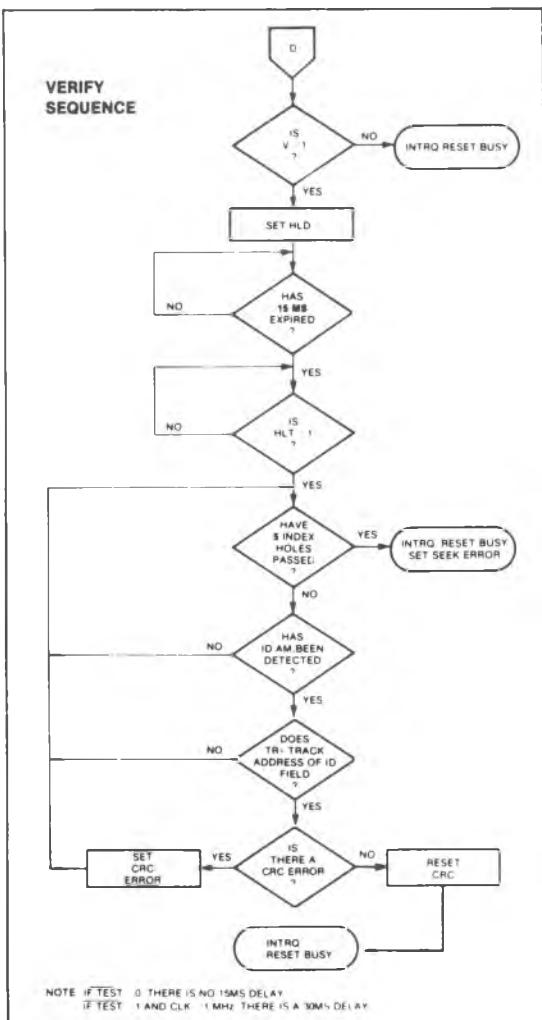
flag is on, the Track Register is incremented by one. After a delay determined by the r1f0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-OUT

Upon receipt of this command, the FD179X issues one stepping pulse in the direction towards track 0. If the U flag is on, the Track Register is decremented by one. After a delay determined by the r1f0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

EXCEPTIONS

On the 1795/7 devices, the SSO output is not affected during Type 1 commands, and an internal side compare does not take place when the (V) Verify Flag is on.



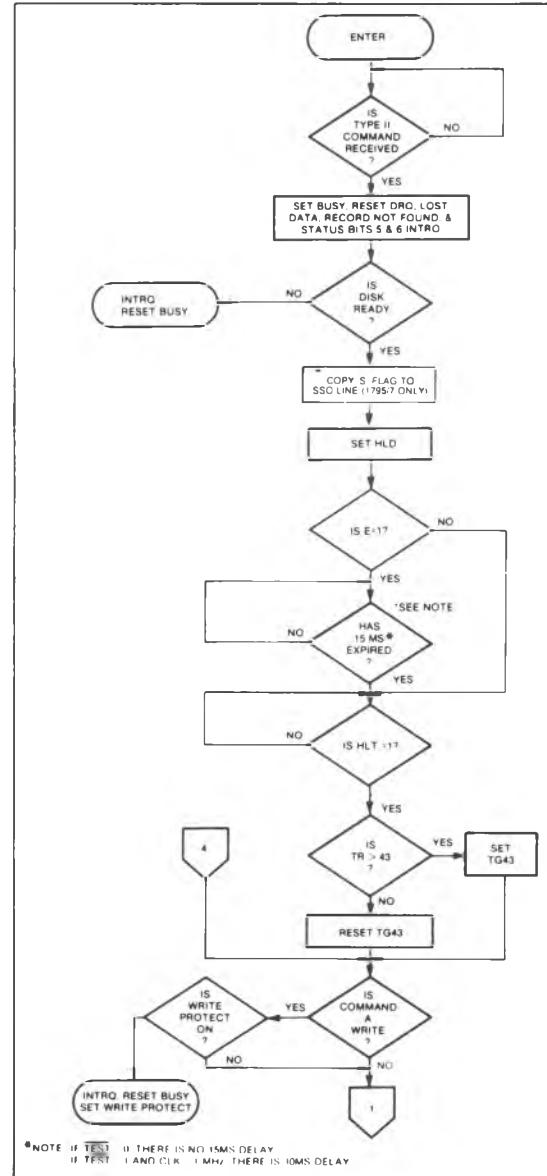
TYPE I COMMAND FLOW

TYPE II COMMANDS

The Type II Commands are the Read Sector and Write Sector commands. Prior to loading the Type II Command into the Command Register, the computer must load the Sector Register with the desired sector number. Upon receipt of the Type II command, the busy status Bit is set. If the E flag = 1 (this is the normal case) HLD is made active and HLT is sampled after a 15 msec delay. If the E flag is 0, the head is loaded and HLT sampled with no 15 msec delay. The ID field and Data Field format are shown on page 13.

When an ID field is located on the disk, the FD179X compares the Track Number on the ID field with the Track Register. If there is not a match, the next encountered ID field is read and a comparison is again made. If there was a match, the Sector Number of the ID field is compared with the Sector Register. If there is not a Sector match, the next encountered ID field is read off the disk and comparisons

again made. If the ID field CRC is correct, the data field is then located and will be either written into, or read from depending upon the command. The FD179X must find an ID field with a Track number, Sector number, side number, and CRC within four revolutions of the disk; otherwise, the Record not found status bit is set (Status bit 3) and the command is terminated with an interrupt.



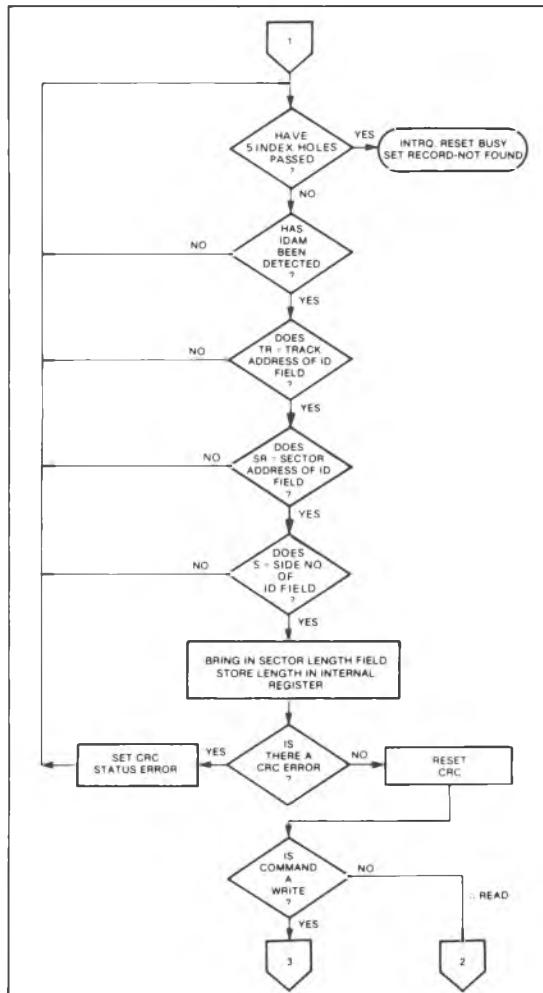
TYPE II COMMAND

Each of the Type II Commands contains an (m) flag which determines if multiple records (sectors) are to be read or written, depending upon the command. If m = 0, a single sector is read or written and an interrupt is generated at the

completion of the command. If $m = 1$, multiple records are read or written with the sector register internally updated so that an address verification can occur on the next record. The FD179X will continue to read or write multiple records and update the sector register in numerical ascending sequence until the sector register exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the Command Register, which terminates the command and generates an interrupt.

For example: If the FD179X is instructed to read sector 27 and there are only 26 on the track, the sector register exceeds the number available. The FD179X will search for 5 disk revolutions, interrupt out, reset busy, and set the record not found status bit.

The Type II commands for 1791-94 also contain side select compare flags. When $C = 0$ (Bit 1) no side comparison is made. When $C = 1$, the LSB of the side number is read off the ID Field of the disk and compared with the contents of the (S) flag (Bit 3). If the S flag compares with the side number recorded in the ID field, the FD179X continues with the ID search. If a comparison is not made within 5 index



TYPE II COMMAND

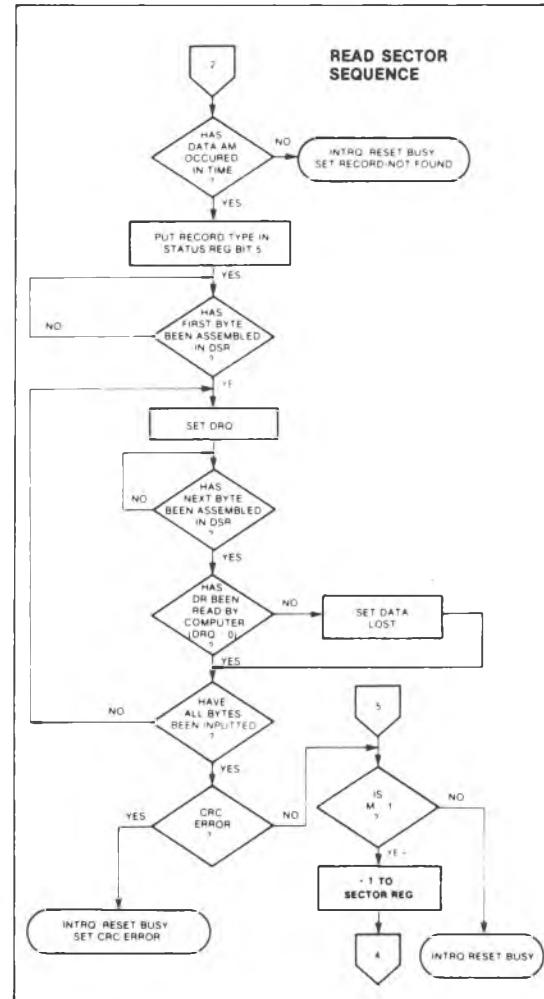
pulses, the interrupt line is made active and the Record-Not-Found status bit is set.

The Type II and III commands for the 1795-97 contain a side select flag (Bit 1). When $U = 0$, SSO is updated to 0. Similarly, $U = 1$ updates SSO to 1. The chip compares the SSO to the ID field. If they do not compare within 5 revolutions the interrupt line is made active and the RNF status bit is set.

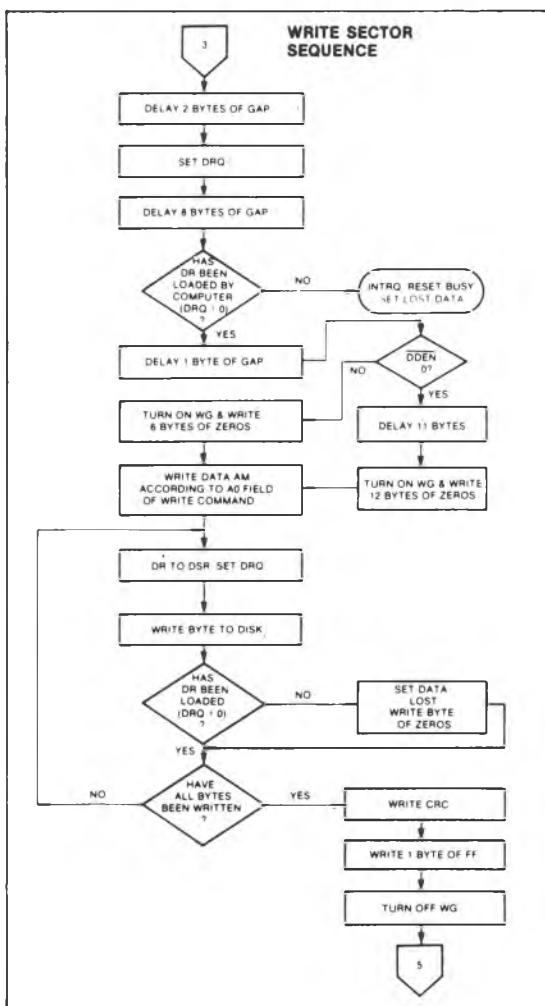
The 1795/7 READ SECTOR and WRITE SECTOR commands include a 'L' flag. The 'L' flag, in conjunction with the sector length byte of the ID Field, allows different byte lengths to be implemented in each sector. For IBM compatibility, the 'L' flag should be set to a one.

READ SECTOR

Upon receipt of the Read Sector command, the head is loaded, the Busy status bit set, and when an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, the data field is presented to the computer. The Data Address



TYPE II COMMAND

**TYPE II COMMAND**

Mark of the data field must be found within 30 bytes in single density and 43 bytes in double density of the last ID field CRC byte; if not, the Record Not Found status bit is set and the operation is terminated.

When the first character or byte of the data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the Computer has not read the previous contents of the DR before a new character is transferred that character is lost and the Lost Data Status bit is set. This sequence continues until the complete data field has been inputted to the computer. If there is a CRC error at the end of the data field, the CRC error status bit is set, and the command is terminated (even if it is a multiple record command).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bit 5) as shown :

**STATUS
BIT 5**

1	Deleted Data Mark
0	Data Mark

WRITE SECTOR

Upon receipt of the Write Sector command, the head is loaded (HLD active) and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, a DRQ is generated. The FD179X counts off 11 bytes in single density and 22 bytes in double density from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeroes in single density and 12 bytes in double density are then written on the disk. At this time the Data Address Mark is then written on the disk as determined by the a_0 field of the command as shown below:

a_0	Data Address Mark (Bit 0)
1	Deleted Data Mark
0	Data Mark

The FD179X then writes the data field and generates DRQ's to the computer. If the DRQ is not serviced in time for continuous writing the Lost Data Status Bit is set and a byte of zeroes is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte of logic ones in FM or in MFM. The WG output is then deactivated. For a 2 MHz clock the INTRQ will set 8 to 12 μ sec after the last CRC byte is written. For partial sector writing, the proper method is to write the data and fill the balance with zeroes. By letting the chip fill the zeroes, errors may be masked by the lost data status and improper CRC Bytes.

TYPE III COMMANDS**READ ADDRESS**

Upon receipt of the Read Address command, the head is loaded and the Busy Status Bit is set. The next encountered ID field is then read in from the disk, and the six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown below:

TRACK ADDR	SIDE NUMBER	SECTOR ADDRESS	SECTOR LENGTH	CRC 1	CRC 2
1	2	3	4	5	6

Although the CRC characters are transferred to the computer, the FD179X checks for validity and the CRC error status bit is set if there is a CRC error. The Track Address of the ID field is written into the sector register so that a comparison can be made by the user. At the end of the operation an interrupt is generated and the Busy Status is reset.

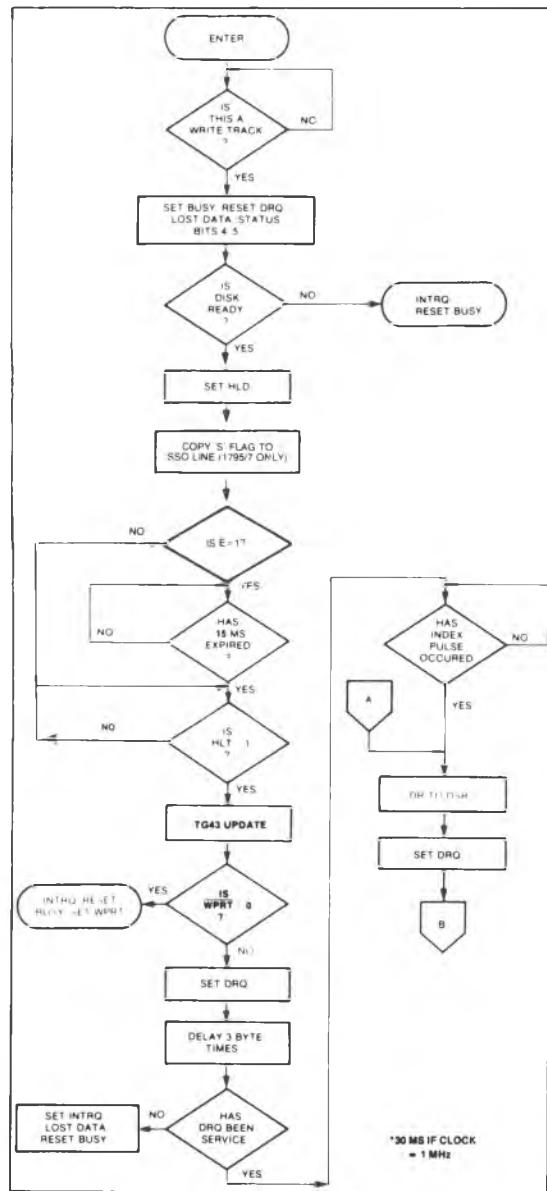
READ TRACK

Upon receipt of the READ track command, the head is loaded, and the Busy Status bit is set. Reading starts with the leading edge of the first encountered index pulse and continues until the next index pulse. All Gap, Header, and data bytes are assembled and transferred to the data register and DRQ's are generated for each byte. The accumulation of bytes is synchronized to each address mark encountered. An interrupt is generated at the completion of the command.

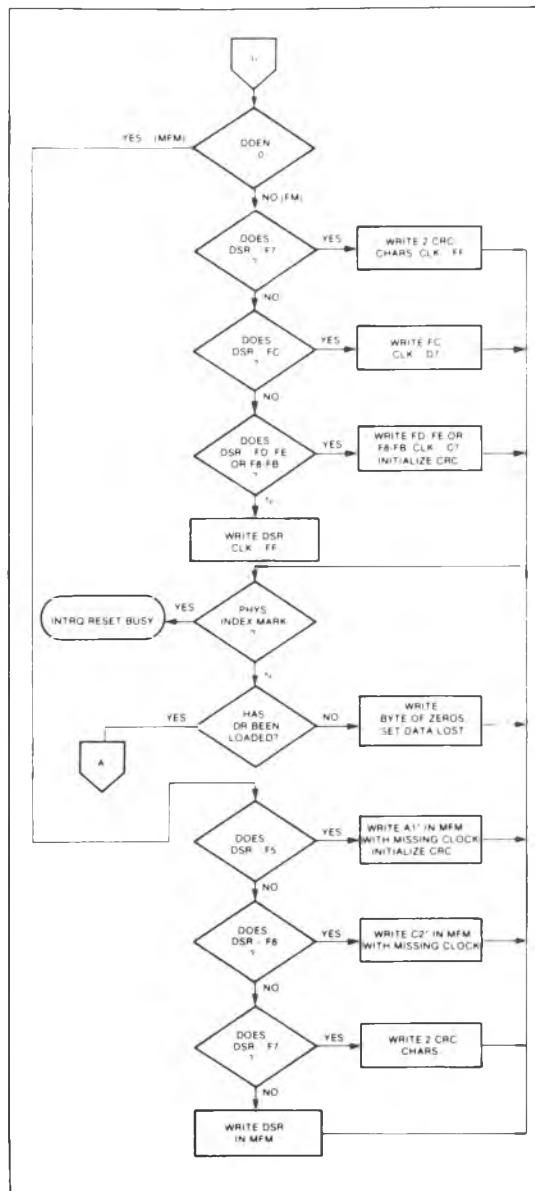
This command has several characteristics which make it suitable for diagnostic purposes. They are: the Read Gate

is not activated during the command; no CRC checking is performed; gap information is included in the data stream; the internal side compare is not performed; and the address mark detector is on for the duration of the command. Because the A.M. detector is always on, write splices or noise may cause the chip to look for an A.M. If an address mark does not appear on schedule the Lost Data status flag is set.

The ID A.M., ID field, ID CRC bytes, DAM, Data, and Data CRC Bytes for each sector will be correct. The Gap Bytes may be read incorrectly during write-splice time because of synchronization.



TYPE III COMMAND WRITE TRACK



TYPE III COMMAND WRITE TRACK

CONTROL BYTES FOR INITIALIZATION

DATA PATTERN IN DR (HEX)	FD179X INTERPRETATION IN FM ($\overline{DDEN} = 1$)	FD1791/3 INTERPRETATION IN MFM ($\overline{DDEN} = 0$)
00 thru F4	Write 00 thru F4 with CLK = FF	Write 00 thru F4, in MFM
F5	Not Allowed	Write A1* in MFM, Preset CRC
F6	Not Allowed	Write C2** in MFM
F7	Generate 2 CRC bytes	Generate 2 CRC bytes
F8 thru FB	Write F8 thru FB, CLK = C7, Preset CRC	Write F8 thru FB, in MFM
FC	Write FC with CLK = D7	Write FC in MFM
FD	Write FD with CLK = FF	Write FD in MFM
FE	Write FE, CLK = C7, Preset CRC	Write FE in MFM
FF	Write FF with CLK = FF	Write FF in MFM

*Missing clock transition between bits 4 and 5

**Missing clock transition between bits 3 & 4

WRITE TRACK FORMATTING THE DISK

(Refer to section on Type III commands for flow diagrams.)

Formatting the disk is a relatively simple task when operating programmed I/O or when operating under DMA with a large amount of memory. Data and gap information must be provided at the computer interface. Formatting the disk is accomplished by positioning the R/W head over the desired track number and issuing the Write Track command.

Upon receipt of the Write Track command, the head is loaded and the Busy Status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered the operation is terminated making the device Not Busy, the Lost Data Status Bit is set, and the Interrupt is activated. If a byte is not present in the DR when needed, a byte of zeroes is substituted.

This sequence continues from one index mark to the next index mark. Normally, whatever data pattern appears in the data register is written on the disk with a normal clock pattern. However, if the FD179X detects a data pattern of F5 thru FE in the data register, this is interpreted as data address marks with missing clocks or CRC generation.

The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR in FM or by receipt of F5 in MFM. An F7 pattern will generate two CRC characters in FM or MFM. As a consequence, the patterns F5 thru FE must not appear in the gaps, data fields, or ID fields. Also, CRC's must be generated by an F7 pattern.

Disk may be formatted in IBM 3740 or System 34 formats with sector lengths of 128, 256, 512, or 1024 bytes.

TYPE IV COMMANDS

The Forced Interrupt command is generally used to terminate a multiple sector read or write command or to in-

sure Type I status in the status register. This command can be loaded into the command register at any time. If there is a current command under execution (busy status bit set) the command will be terminated and the busy status bit reset.

The lower four bits of the command determine the conditional interrupt as follows:

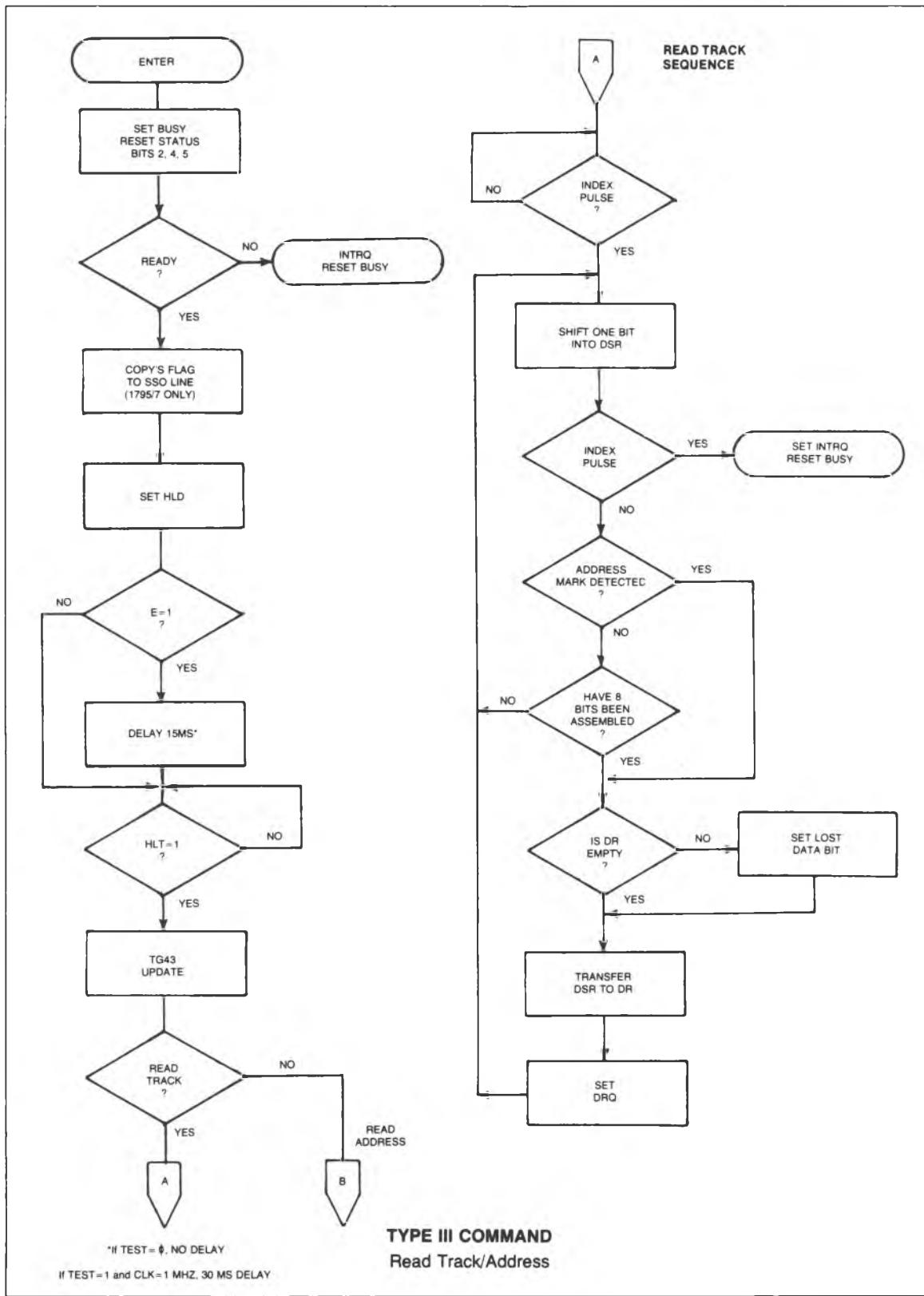
- I0 = Not-Ready to Ready Transition
- I1 = Ready to Not-Ready Transition
- I2 = Every Index Pulse
- I3 = Immediate Interrupt

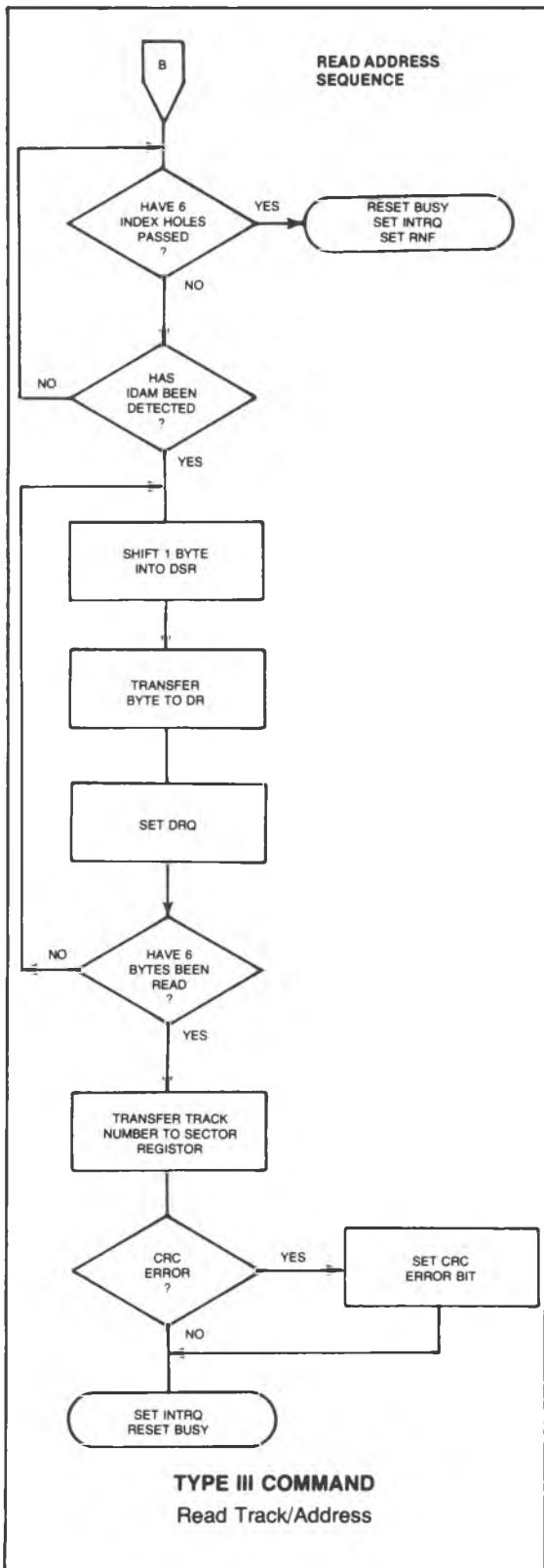
The conditional interrupt is enabled when the corresponding bit positions of the command (I3 - I0) are set to a 1. Then, when the condition for interrupt is met, the INTRQ line will go high signifying that the condition specified has occurred. If I3 - I0 are all set to zero (HEX D0), no interrupt will occur but any command presently under execution will be immediately terminated. When using the immediate interrupt condition (I3 = 1) an interrupt will be immediately generated and the current command terminated. Reading the status or writing to the command register will not automatically clear the interrupt. The HEX D0 is the only command that will enable the immediate interrupt (HEX D8) to clear on a subsequent load command register or read status register operation. Follow a HEX D8 with D0 command.

Wait 8 micro sec (double density) or 16 micro sec (single density before issuing a new command after issuing a forced interrupt (times double when clock = 1 MHz). Loading a new command sooner than this will nullify the forced interrupt.

Forced interrupt stops any command at the end of an internal micro-instruction and generates INTRQ when the specified condition is met. Forced interrupt will wait until ALU operations in progress are complete (CRC calculations, compares, etc.).

More than one condition may be set at a time. If for example, the READY TO NOT-READY condition (I1 = 1) and the Every Index Pulse (I2 = 1) are both set, the resultant command would be HEX "DA". The "OR" function is performed so that either a READY TO NOT-READY or the next Index Pulse will cause an interrupt condition.



**STATUS REGISTER**

Upon receipt of any command, except the Force Interrupt command, the Busy Status bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt Command is received when there is a current command under execution, the Busy status bit is reset, and the rest of the status bits are unchanged. If the Force Interrupt command is received when there is not a current command under execution, the Busy Status bit is reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

The user has the option of reading the status register through program control or using the DRQ line with DMA or interrupt methods. When the Data register is read the DRQ bit in the status register and the DRQ line are automatically reset. A write to the Data register also causes both DRQ's to reset.

The busy bit in the status may be monitored with a user program to determine when a command is complete, in lieu of using the INTRQ line. When using the INTRQ, a busy status check is not recommended because a read of the status register to determine the condition of busy will reset the INTRQ line.

The format of the Status Register is shown below:

(BITS)							
7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

Status varies according to the type of command executed as shown in Table 4.

Because of internal sync cycles, certain time delays must be observed when operating under programmed I/O. They are: (times double when clock = 1 MHz)

Operation	Next Operation	Delay Req'd.	
		FM	MFM
Write to Command Reg.	Read Busy Bit (Status Bit 0)	12 µs	6 µs
Write to Command Reg.	Read Status Bits 1-7	28 µs	14 µs
Write Any Register	Read From Diff. Register	0	0

IBM 3740 FORMAT — 128 BYTES/SECTOR

Shown below is the IBM single-density format with 128 bytes/sector. In order to format a diskette, the user must issue the Write Track command, and load the data register with the following values. For every byte to be written, there is one Data Request.

NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
40	FF (or 00)*
6	00
1	FC (Index Mark)
• 26	FF (or 00)*
6	00
1	FE (ID Address Mark)
1	Track Number
1	Side Number (00 or 01)
1	Sector Number (1 thru 1A)
1	00 (Sector Length)
1	F7 (2 CRC's written)
11	FF (or 00)*
6	00
1	FB (Data Address Mark)
128	Data (IBM uses E5)
1	F7 (2 CRC's written)
27	FF (or 00)*
247**	FF (or 00)*

*Write bracketed field 26 times

**Continue writing until FD179X interrupts out.

Approx. 247 bytes.

1-Optional '00' on 1795/7 only.

IBM SYSTEM 34 FORMAT-

256 BYTES/SECTOR

Shown below is the IBM dual-density format with 256 bytes/sector. In order to format a diskette the user must

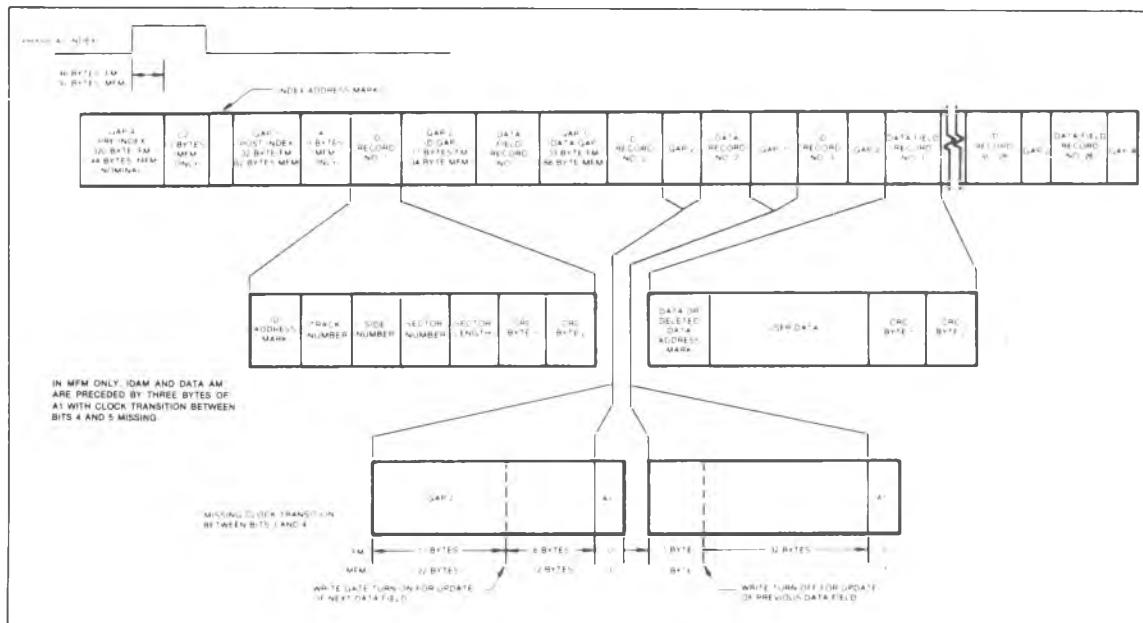
issue the Write Track command and load the data register with the following values. For every byte to be written, there is one data request.

NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
80	4E
12	00
3	F6 (Writes C2)
1	FC (Index Mark)
• 50	4E
12	00
3	F5 (Writes A1)
1	FE (ID Address Mark)
1	Track Number (0 thru 4C)
1	Side Number (0 or 1)
1	Sector Number (1 thru 1A)
1	01 (Sector Length)
1	F7 (2 CRCs written)
22	4E
12	00
3	F5 (Writes A1)
1	FB (Data Address Mark)
256	DATA
1	F7 (2 CRCs written)
54	4E
598**	4E

*Write bracketed field 26 times

**Continue writing until FD179X interrupts out.

Approx. 598 bytes.



IBM TRACK FORMAT

1. NON-IBM FORMATS

Variations in the IBM formats are possible to a limited extent if the following requirements are met:

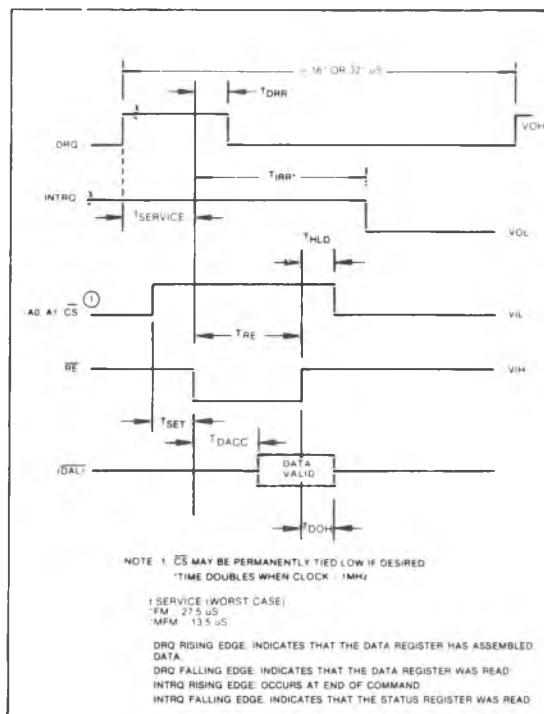
- 1) Sector size must be 128, 256, 512 or 1024 bytes.
- 2) Gap 2 cannot be varied from the IBM format.
- 3) 3 bytes of A1 must be used in MFM.

In addition, the Index Address Mark is not required for operation by the FD179X. Gap 1, 3, and 4 lengths can be as short as 2 bytes for FD179X operation, however PLL lock up time, motor speed variation, write-splice area, etc. will add more bytes to each gap to achieve proper operation. It is recommended that the IBM format be used for highest system reliability.

	FM	MFM
Gap I	16 bytes FF	32 bytes 4E
Gap II	11 bytes FF	22 bytes 4E
•	6 bytes 00	12 bytes 00
•		3 bytes A1
Gap III**	10 bytes FF 4 bytes 00	24 bytes 4E 8 bytes 00 3 bytes A1
Gap IV	16 bytes FF	16 bytes 4E

*Byte counts must be exact.

**Byte counts are minimum, except exactly 3 bytes of A1 must be written.



READ ENABLE TIMING

TIMING CHARACTERISTICS

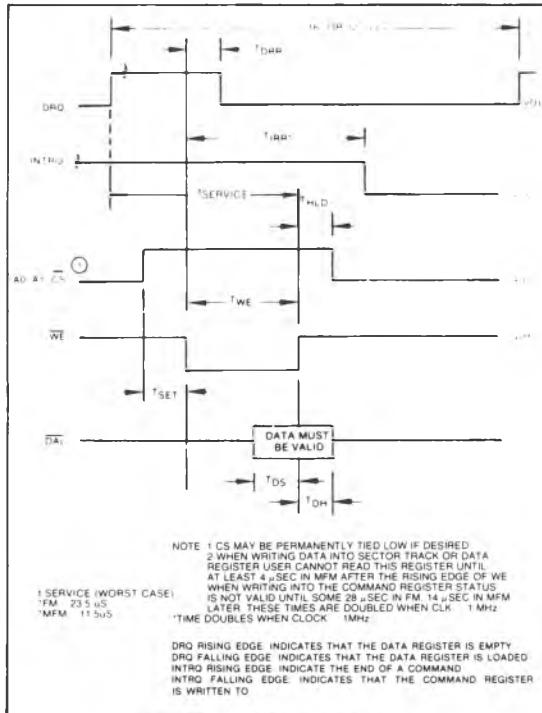
$T_A = 0^\circ C$ to $70^\circ C$, $V_{DD} = +12V \pm .6V$, $V_{SS} = 0V$, $V_{CC} = +5V \pm .25V$

READ ENABLE TIMING (See Note 6, Page 21)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TSET	Setup ADDR & CS to \overline{RE}	50			nsec	
THLD	Hold ADDR & CS from \overline{RE}	10			nsec	
TRE	\overline{RE} Pulse Width	400			nsec	$C_L = 50 \text{ pf}$
TDRR	DRQ Reset from \overline{RE}		400	500	nsec	
TIRR	INTRQ Reset from \overline{RE}		500	3000	nsec	See Note 5
TDACC	Data Access from \overline{RE}				nsec	$C_L = 50 \text{ pf}$
TDOH	Data Hold From \overline{RE}	50		150	nsec	$C_L = 50 \text{ pf}$

WRITE ENABLE TIMING (See Note 6, Page 21)

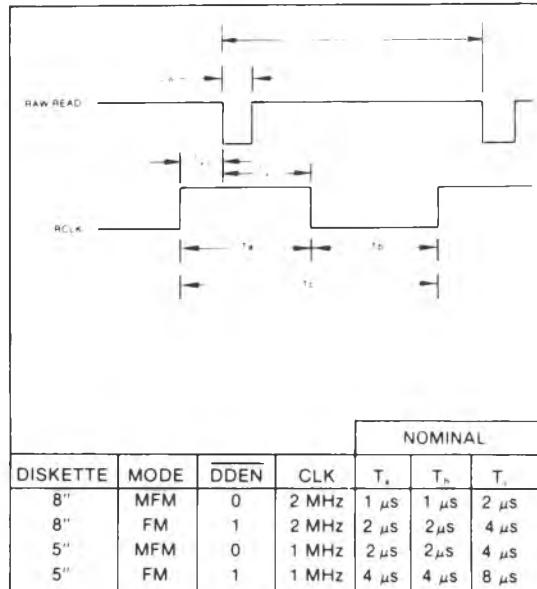
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TSET	Setup ADDR & CS to \overline{WE}	50			nsec	
THLD	Hold ADDR & CS from \overline{WE}	10			nsec	
TWE	\overline{WE} Pulse Width	350			nsec	
TDRR	DRQ Reset from \overline{WE}		400	500	nsec	
TIRR	INTRQ Reset from \overline{WE}		500	3000	nsec	See Note 5
TDS	Data Setup to \overline{WE}	250			nsec	
TDH	Data Hold from \overline{WE}	70			nsec	

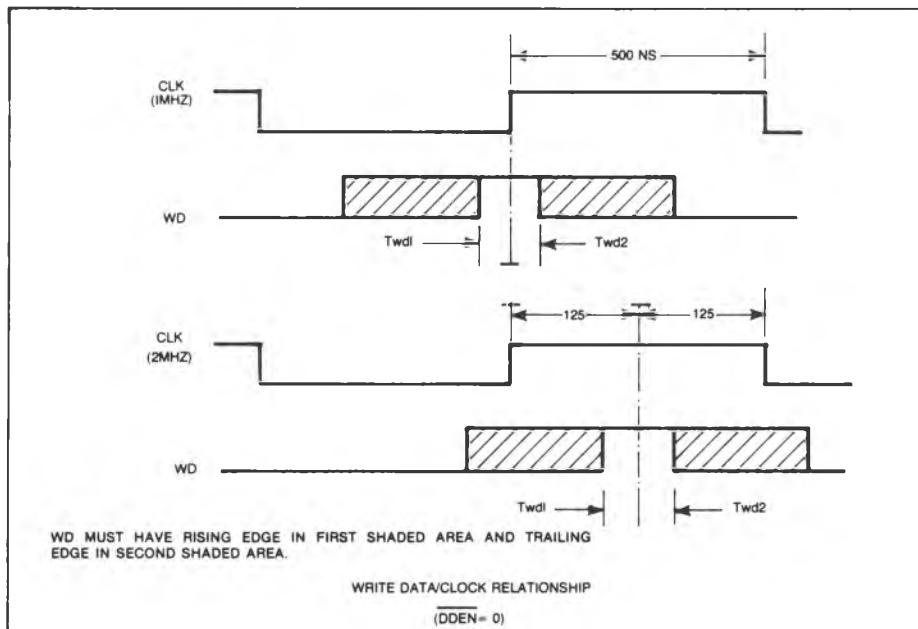
**WRITE ENABLE TIMING****INPUT DATA TIMING:**

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Tpw	Raw Read Pulse Width	100	200		nsec	See Note 1
tbc	Raw Read Cycle Time	1500	2000		nsec	1800 ns @ 70°C
Tc	RCLK Cycle Time	1500	2000		nsec	1800 ns @ 70°C
Tx1	RCLK hold to Raw Read	40			nsec	See Note 1
Tx2	Raw Read hold to RCLK	40			nsec	See Note 1

WRITE DATA TIMING: (ALL TIMES DOUBLE WHEN CLK = 1 MHZ) (See Note 6, Page 21)

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Twp	Write Data Pulse Width	450	500	550	nsec	FM
Twg	Write Gate to Write Data	150	200	250	nsec	MFM
Tbc	Write data cycle Time					FM
Ts	Early (Late) to Write Data	125	2, 3, or 4		μsec	MFM
Th	Early (Late) From Write Data	125			nsec	MFM
Twf	Write Gate off from WD		2		μsec	FM
Twdl	WD Valid to Clk	100			nsec	CLK=1 MHZ
		50			nsec	CLK=2 MHZ
Twd2	WD Valid after CLK	100			nsec	CLK=1 MHZ
		30			nsec	CLK=2 MHZ

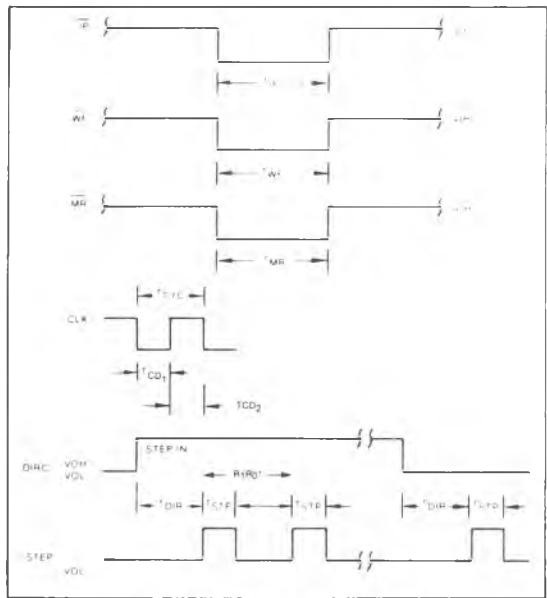
**INPUT DATA TIMING**



WRITE DATA TIMING

MISCELLANEOUS TIMING: (Times Double When Clock = 1 MHz) (See Note 6, Page 21)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TCD ₁	Clock Duty (low)	230	250	20000	nsec	
TCD ₂	Clock Duty (high)	200	250	20000	nsec	
TSTP	Step Pulse Output	2 or 4			μsec	
TDIR	Dir Setup to Step		12		μsec	
TMR	Master Reset Pulse Width	50			μsec	
TIP	Index Pulse Width	10			μsec	
TWF	Write Fault Pulse Width	10			μsec	See Note 5



MISCELLANEOUS TIMING

*FROM STEP RATE TABLE

NOTES:

- Pulse width on RAW READ (Pin 27) is normally 100-300 ns. However, pulse may be any width if pulse is entirely within window. If pulse occurs in both windows, then pulse width must be less than 300 ns for MFM at CLK = 2 MHz and 600 ns for FM at 2 MHz. Times double for 1 MHz.
- A PPL Data Separator is recommended for 8" MFM.
- tbc should be 2 μ s, nominal in MFM and 4 μ s nominal in FM. Times double when CLK = 1 MHz.
- RCLK may be high or low during RAW READ (Polarity is unimportant).
- Times double when clock = 1 MHz.
- Output timing readings are at V_{OL} = 0.8v and V_{OH} = 2.0v.

Table 4. STATUS REGISTER SUMMARY

BIT	ALL TYPE I COMMANDS	READ ADDRESS	READ SECTOR	READ TRACK	WRITE SECTOR	WRITE TRACK
S7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
S6	WRITE PROTECT	0	0	0	WRITE PROTECT	WRITE PROTECT
S5	HEAD LOADED	0	RECORD TYPE	0	WRITE FAULT	WRITE FAULT
S4	SEEK ERROR	RNF	RNF	0	RNF	0
S3	CRC ERROR	CRC ERROR	CRC ERROR	0	CRC ERROR	0
S2	TRACK 0	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX PULSE	DRQ	DRQ	DRQ	DRQ	DRQ
S0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

STATUS FOR TYPE I COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the Ready input and logically 'ored' with MR.
S6 PROTECTED	When set, indicates Write Protect is activated. This bit is an inverted copy of WRPT input.
S5 HEAD LOADED	When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals.
S4 SEEK ERROR	When set, the desired track was not verified. This bit is reset to 0 when updated.
S3 CRC ERROR	CRC encountered in ID field.
S2 TRACK 00	When set, indicates Read/Write head is positioned to Track 0. This bit is an inverted copy of the TROO input.
S1 INDEX	When set, indicates index mark detected from drive. This bit is an inverted copy of the IP input.
S0 BUSY	When set command is in progress. When reset no command is in progress.

STATUS FOR TYPE II AND III COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and 'ored' with MR. The Type II and III Commands will not execute unless the drive is ready.
S6 WRITE PROTECT	On Read Record: Not Used. On Read Track: Not Used. On any Write: It indicates a Write Protect. This bit is reset when updated.
S5 RECORD TYPE/ WRITE FAULT	On Read Record: It indicates the record-type code from data field address mark. 1 = Deleted Data Mark. 0 = Data Mark. On any Write: It indicates a Write Fault. This bit is reset when updated.
S4 RECORD NOT FOUND (RNF)	When set, it indicates that the desired track, sector, or side were not found. This bit is reset when updated.
S3 CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2 LOST DATA	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1 DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read Operation or the DR is empty on a Write operation. This bit is reset to zero when updated.
S0 BUSY	When set, command is under execution. When reset, no command is under execution.

ELECTRICAL CHARACTERISTICS**Absolute Maximum Ratings**V_{DD} with respect to V_{SS} (ground): + 15 to - 0.3VVoltage to any input with respect to V_{SS} = + 15 to - 0.3VI_{CC} = 60 mA (35 mA nominal)I_{DD} = 15 mA (10 mA nominal)

Dissipation = 0.6 W

C_{IN} & C_{OUT} = 15 pF max with all pins grounded except one under test.

Operating temperature = 0°C to 70°C

Storage temperature = - 55°C to + 125°C

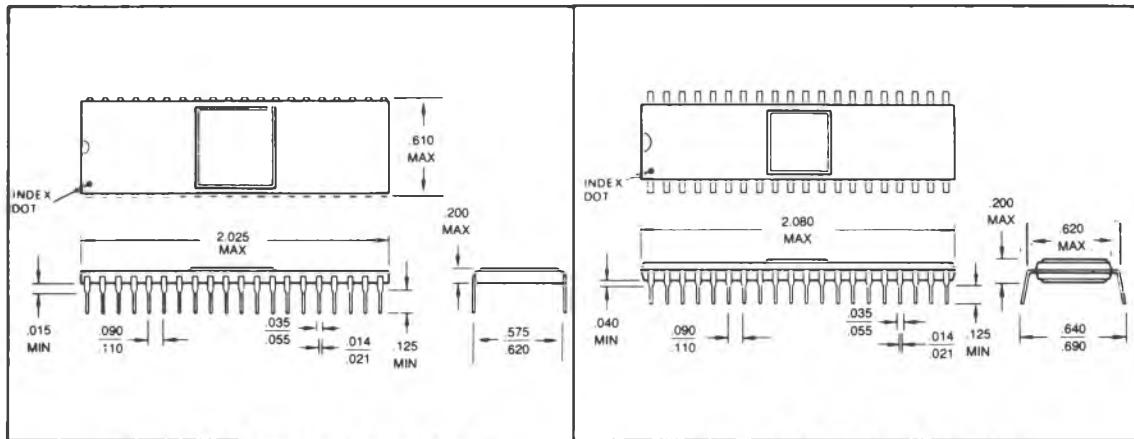
OPERATING CHARACTERISTICS (DC)TA = 0°C to 70°C, V_{DD} = + 12V ± .6V, V_{SS} = 0V, V_{CC} = + 5V ± .25V

SYMBOL	CHARACTERISTIC	MIN.	MAX.	UNITS	CONDITIONS
I _{IL}	Input Leakage		10	µA	
I _{OL}	Output Leakage		10	µA	
V _{IH}	Input High Voltage	2.6		V	
V _{IL}	Input Low Voltage		0.8	V	
V _{OH}	Output High Voltage	2.8		V	I _O = - 100 µA
V _{OL}	Output Low Voltage		0.45	V	I _O = 1.6 mA*
P _D	Power Dissipation		0.6	W	

*1792 and 1794 I_O = 1.0 mA

**Leakage conditions are for input pins without internal pull-up resistors.

NOTES



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Appendix B

FD179X APPLICATION NOTES

The following pages are reprinted with the permission of Western Digital Corporation.



FD179X Application Notes

NOVEMBER, 1980

INTRODUCTION

Over the past several years, the Floppy Disk Drive has become the most popular on-line storage device for mini and microcomputer systems. Its fast access time, reliability and low cost-per-bit ratio enables the Floppy Disk Drive to be the solution in mass storage for microprocessor systems. The drive interface to the Host system is standardized, allowing the OEM to substitute one drive for another with minimum hardware/ software modifications.

Since Floppy Disk Data is stored and retrieved as a self-clocking serial data stream, some means of separating the clock from the data and assembling this data in parallel form must be accomplished. Data is stored on individual Tracks of the media, requiring control of a stepper motor to move the Read/Write head to a predetermined Track. Byte synchronization must also be accomplished to insure that the parallel data is properly assembled. After all the design considerations are met, the final controller can consist of 40 or more TTL packages.

To alleviate the burden of Floppy Disk Controller design, Western Digital has developed a Family of LSI Floppy Disk controller devices. Through its own set of macro commands, the FD179X Controller Family will perform all the functions necessary to read and write data to the drive. Both the 8" standard and 5 1/4" mini-floppy are supported with single or double density recording techniques. The FD179X is compatible with the IBM 3740 (FM) data format, or the System 34 (MFM) standards. Provisions for non-standard formats and variable sector lengths have been included to provide more storage capability per track. Requiring standard +5, +12 power supplies the FD179X is available in a standard 40 pin dual-in-line package.

The FD179X Family consists of 6 devices. The differences between these devices is summarized in Figure 1. The 1792 and 1794 are "single density only" devices, with the Double Density Enable pin (DDEN) left open by the user. Both True and inverted Data bus devices are available. Since the 179X can only drive one TTL Load, a true data bus system may use the 1791 with external inverting buffers to arrive at a true bus scheme. The 1795 and 1797 are identical to the 1791 and 1793, except a side select output has been added that is controlled through the Command Register.

SYSTEM DESIGN

The first consideration in Floppy Disk Design is to determine which type of drive to use. The choice ranges from single-density single sided mini-floppy to the 8" double-density double-sided drive. Figure 2 illustrates the various drive and data capacities associated with each type. Although the 8" double-density drive offers twice as much storage, a more complex data separator and the addition of Write Precompensation circuits are mandatory for reliable data transfers. Whether to go with 8" double-density or not is dependent upon PC board space and the additional circuitry needed to accurately recover data with extreme bit shifts. The byte transfer time defines the nominal time required to transfer one byte of data from the drive. If the CPU used cannot service a byte in this time, then a DMA scheme will probably be required. The 179X also needs a few microseconds for overhead, which is subtracted from the transfer time. Figure 3 shows the actual service times that the CPU must provide on a byte-by-byte basis. If these times are not met, bytes of data will be lost during a read or write operation. For each byte transferred, the 179X generates a DRQ (Data Request) signal on Pin 38. A bit is provided in the status register which is also set upon receipt of a byte from the Disk. The user has the option of reading the status register through program control or using the DRQ Line with DMA or interrupt schemes. When the data register is read, both the status register DRQ bit and the DRQ Line are automatically reset. The next full byte will again set the DRQ and the process continues until the sector(s) are read. The Write operation works exactly the same way, except a WRITE to the Data Register causes a reset of both DRQ's.

RECORDING FORMATS

The FD179X accepts data from the disk in a Frequency-Modulated (FM) or Modified-Frequency-Modulated (MFM) Format. Shown in Figures 4A and 4B are both these Formats when writing a Hexadecimal byte of 'D2'. In the FM mode, the 8 bits of data are broken up into "bit cells." Each bit cell begins with a clock pulse and the center of the bit cell defines the data. If the data bit = 0, no pulse is written; if the data = 1, a pulse is written in the center of the cell. For the 8" drive, each clock is written 4 microseconds apart.

In the MFM mode, clocks are decoded into the data stream. The byte is again broken up into bit cells, with the data bit written in the center of the bit cell if data = 1. Clocks are only written if both surrounding data bits are zero. Figure 4B shows that this occurs only once between Bit cell 4 and 5. Using this encoding scheme, pulses can occur 2, 3 or 4 microseconds apart. The bit cell time is now 2 microseconds; twice as much data can be recorded without increasing the Frequency rate due to this encoding scheme.

The 179X was designed to be compatible with the IBM 3740 (FM) and System 34 (MFM) Formats. Although most users do not have a need for data exchange with IBM mainframes, taking advantage of these well studied formats will insure a high degree of system performance. The 179X will allow a change in gap fields and sector lengths to increase usable storage capacity, but variations away from these standards is not recommended. Both IBM standards are soft-sector format. Because of the wide variation in address marks, the 179X can only support soft-sectorized media. Hard sectored diskettes have continued to lose popularity, mainly due to the unavailability of a standard and the limitation of sector lengths imposed by the physical sector holes in the diskette.

PROCESSOR INTERFACE

The Interface of the 179X to the CPU consists of an 8-bit Bi-directional bus, read/write controls and optional interrupt lines. By selecting the device via the CHIP SELECT Line, each of the five internal registers can be accessed.

Shown below are the registers and their addresses:

PIN 3 CS	PIN 6 A ₁	PIN 5 A ₀	PIN 4 $\overline{RE} = 0$	PIN 2 $\overline{WE} = 0$
0	0	0	STATUS REG	COMMAND REG
0	0	1	TRACK REG	TRACK REG
0	1	0	SECTOR REG	SECTOR REG
0	1	1	DATA REG	DATA REG
1	X	X	H1-Z	H1-Z

Each time a command is issued to the 179X, the Busy bit is set and the INTRQ (Interrupt Request) Line is reset. The user has the option of checking the busy bit or use the INTRQ Line to denote command completion. The Busy bit will be reset whenever the 179X is idle and awaiting a new command. The INTRQ Line, once set, can only be reset by a READ of the status register or issuing a new command. The MR (Master Reset) Line does not affect INTRQ.

The A₀, A₁, Lines used for register selections can be configured at the CPU in a variety of ways. These lines may actually tie to CPU address lines, in which case the 179X will be memory-mapped and addressed like RAM. They may also be used under Program Control by tying to a port device such as the 8255, 6820, etc. As a diagnostic tool when checking out the CPU interface, the Track and Sector registers should respond like "RAM" when the 179X is idle (Busy = INTRQ = 0).

Because of internal synchronization cycles, certain time delays must be introduced when operating under Programmed I/O. The worst case delays are:

OPERATION	NEXT OPERATION	DELAY REQ'D
WRITE TO COMMAND REG	READ STATUS REGISTER	MFM = 14 μ s* FM = 28 μ s.
WRITE TO ANY REGISTER	READ FROM A DIFFERENT REG	NO DELAY

*NOTE: Times Double when CLK = 1MHz (5 $\frac{1}{4}$ " drive)

Other CPU interface lines are CLK, MR and DDEN. The CLK line should be 2MHz (8" drive) or 1MHz (5 $\frac{1}{4}$ " drive) with a 50% duty cycle. Accuracy should be $\pm 1\%$ (crystal source) since all internal timing, including stepping rates, are based upon this clock.

The MR or Master Reset Line should be strobed a minimum of 50 microseconds upon each power-on condition. This line clears and initializes all internal registers and issues a restore command (Hex '03') on the rising edge. A quicker stepping rate can be written to the command register after a MR, in which case the remaining steps will occur at the faster programmed rate. The 179X will issue a maximum of 255 stepping pulses in an attempt to expect the TROO line to go active low. This line should be connected to the drive's TROO sensor.

The DDEN line causes selection of either single density (DDEN = 1) or double density operation. DDEN should not be switched during a read or write operation.

FLOPPY DISK INTERFACE

The Floppy Disk Interface can be divided into three sections: Motor Control, Write Signals and Read Signals. All of these lines are capable of driving one TTL load and not compatible for direct connection to the drive. Most drives require an open-collector TTL interface with high current drive capability. This must be done on all outputs from the 179X. Inputs to the 179X may be buffered or tied to the Drives outputs, providing the appropriate resistor termination networks are used. Undershoot should not exceed -0.3 volts, while integrity of V_{IH} and V_{OH} levels should be kept within spec.

MOTOR CONTROL

Motor Control is accomplished by the STEP and DIRC Lines. The STEP Line issues stepping pulses with a period defined by the rate field in all Type I commands. The DIRC Line defines the direction of steps (DIRC = 1 STEP IN/DIRC = 0 STEP OUT).

Other Control Lines include the IP or Index Pulse. This Line is tied to the drives' Index L.E.D. sensor and makes an active transition for each revolution of the diskette. The TROO Line is another L.E.D. sensor that informs the 179X that the stepper motor is at its furthest position, over Track 00. The READY Line can be used for a number of functions, such as sensing "door open", Drive motor on, etc. Most drives provide a programmable READY Signal selected by option jumpers on the drive. The 179X will look at the ready signal prior to executing READ/WRITE commands. READY is not inspected during any Type I commands. All Type I commands will execute regardless of the Logic Level on this Line.

WRITE SIGNALS

Writing of data is accomplished by the use of the WD, WG, WF, TG43, EARLY and LATE Lines. The WG or Write Gate Line is used to enable write current at the drive's R/W head. It is made active prior to writing data on the disk. The WF or WRITE FAULT Line is used to inform the 179X of a failure in drive electronics. This signal is multiplexed with the VFOE Line and must be logically separated if required. Figure 5 illustrates three methods of demultiplexing.

The TG43 or "TRACK GREATER than 43" Line is used to decrease the Write current on the inner tracks, where bit densities are the highest. If not required on the drive, TG43 may be left open.

WRITE PRECOMPENSATION

The 179X provides three signals for double density Write Precompensation use. These signals are WRITE DATA, EARLY and LATE. When using single density drives (eighth 8" or 5 1/4"), Write Precompensation is not necessary and the WRITE DATA line is generally TTL Buffered and sent directly to the drive. In this mode, EARLY and LATE are left open.

For double density use, Write Precompensation is a function of the drive. Some manufacturers recommend Precompensating the 5 1/4" drive, while others do not. With the 8" drive, Precompensation may be specified from TRACK 43 on, or in most cases, all TRACKS. If the recommended Precompensation is not specified,

check with the manufacturer for the proper configuration required.

The amount of Precompensation time also varies. A typical value will usually be specified from 100-300ns. Regardless of the parameters used, Write Precompensation must be done external to the 179X. When DDEN is tied low, EARLY or LATE will be activated at least 125ns. before and after the Write Data pulse. An Algorithm internal the 179X decides whether to raise EARLY or LATE, depending upon the previous bit pattern sent. As an example, suppose the recommended Precomp value has been specified at 150ns. The following action should be taken:

EARLY	LATE	ACTION TAKEN
0	0	delay WD by 150ns (nominal)
0	1	delay WD by 300ns (2X value)
1	0	do not delay WD

There are two methods of performing Write Precompensation:

- 1) External Delay elements
- 2) Digitally

Shown in Figure 6 is a Precomp circuit using the Western Digital 2143 clock generator as the delay element. The WD pulse from the 179X creates a strobe to the 2143, causing subsequent output pulses on the θ_1 , θ_2 and θ_3 signals. The 5K Precomp adjust sets the desired Precomp value. Depending upon the condition of EARLY and LATE, θ_1 will be used for EARLY, θ_2 for nominal (EARLY = LATE = 0), and θ_3 for LATE. The use of "one-shots" or delay line in a Write Precompensation scheme offers the user the ability to vary the Precomp value. The θ_4 output resets the 74LS175 Latch in anticipation of the next WD pulse. Figure 7 shows the WD-EARLY/LATE relationship, while Figure 8 shows the timing of this write Precomp scheme.

Another method of Precomp is to perform the function digitally. Figure 9 illustrates a relationship between the WD pulse and the CLK pin, allowing a digital Precomp scheme. Figure 10 shows such a scheme with a preset Write Precompensation value of 250ns. The synchronous counter is used to generate 2MHz and 4MHz clock signals. The 2MHz clock is sent to the CLK input of the 179X and the 4MHz is used by the 4-bit shift register. When a WD pulse is not present, the 4MHz clock is shifting "ones" through the shift register and maintaining Q_D at a zero level. When a WD pulse is present, a zero is loaded at either A, B, or C depending upon the states of LATE, EN PRECOMP and EARLY. The zero is then shifted by the 4MHz clock until it reaches the Q_D output. The number of shift operations determines whether the WRITE DATA pulse is written early, nominal or late. If both FM and MFM operations is a system requirement, the output of this circuit should be disabled and the WD pulse should be sent directly to the drive.

DATA SEPARATION

The 179X has two inputs (RAW READ & RCLK) and one output (VFOE) for use by an external data separator. The RAW READ input must present clock and data pulses to the 179X, while the RCLK input provides a "window" or strobe signal to clock each RAW READ pulse into the device. An ideal Data Separator would have the leading edge of the RAW READ pulse occur in the exact center of the RCLK strobe.

Motor Speed Variation, Bit shifts and read amplifier recovery circuits all cause the RAW READ pulses to drift away from their nominal positions. As this occurs, the RAW READ pulses will shift left or right with respect to RCLK. Eventually, a pulse will make its transition outside of its RCLK window, causing either a CRC error or a Record-not-Found error at the 179X. A Phase-Lock-Loop circuit is one method of achieving synchronization between the RCLK and RAW READ signals. As RAW READ pulses are fed to the PLL, minor adjustments of the free-running RCLK frequency can be made. If pulses are occurring too far apart, the RCLK frequency is decreased to keep synchronization. If pulses begin to occur closer together, RCLK is increased until this new higher frequency is achieved. In normal read operations, RCLK will be constantly adjusted in an attempt to match the incoming RAW READ frequency.

Another method of Data Separation is the Counter-Separator technique. The RCLK signal is again free-running at a nominal rate, until a RAW READ pulse occurs. The Separator then denotes the position of the pulse with respect to RCLK (by the counter value), and counts down to increase or decrease the current RCLK window. The next RCLK window will occur at a nominal rate and will continue to run at this frequency until another RAW READ pulse adjusts RCLK, but only the present window is adjusted.

Both PPL and Counter/Separator are acceptable methods of Data Separation. The PPL has the highest reliability because of its "tracking" capability and is recommended for 8" double density designs.

As a final note, the term "Data Separator" may be misleading, since the physical separation of clock and data bits are not actually performed. This term is used throughout the industry, and can better be described as a "Data Recovery Circuit" rather than a Data Separator.

The VFOE signal is an output from the 179X that signifies the head has been loaded and valid data pulses are appearing on the RAW READ line. It can be used to enable the Data Separator and to insure clean RCLK transitions to the 179X. Since some drives will output random pulses when the head is disengaged, VFOE can prevent an erratic RCLK signal during this time. If the Data Separator requires synchronization during a known pattern of one's or zero's, then RG (READ GATE) can be used. The RG signal will go active when the 179X is currently over a field of zeros or ones. RG is not available on the 1795/1797 devices, since this signal was replaced with the SSO (Side Select Output) Line.

Shown in Figure 11 is a 2½ IC Counter/Separator. The 74LS193 free runs at a frequency determined by the CRYCLK input. When a RAW READ pulse occurs, the counter is loaded with a starting count of '5'. When the RAW READ Line returns to a Logic 1, the counter counts down to zero and again free runs. The 74LS74 insures a 50% duty cycle to the 179X and performs a divide-by-two of the Q_0 output.

Figure 12 illustrates another Counter/Separator utilizing a PROM as the count generator. Depending upon the RAW READ phase relationship to RCLK, the PROM is addressed and its data output is used as the counter value. A 16MHz clock is required for 8" double density, while an 8MHz clock can be used for single density.

Figure 13 shows a Phase-Lock-Loop data recovery circuit. The phase detector (U2, Figure 2) compares the phase of the SHAPED DATA pulse to the phase of VFO CLK $\div 2$. If VFO CLK $\div 2$ is lagging the SHAPED DATA pulse an output pulse on #9, U2 is generated. The filter/amplifier converts this pulse into a DC signal which increases the frequency of the VCO. If, correspondingly, CLK $\div 2$ is leading the SHAPED DATA pulse, an output pulse on #5, U2 is generated. This pulse is converted into a DC signal which decreases the frequency of the VCO. These two actions cause the VCO to track the frequency of the incoming READ DATA pulses. This correction process to keep the two signals in phase is constantly occurring because of spindle speed variation and circuit parameter variations.

The operating specifications for this circuit are as follows:

Free Running Frequency	2MHz
Capture Range	$\pm 15\%$
Lock Up Time	50 microsec. "1111" or "0000" Pattern 100 Microsec "1010" Pattern

The RAW READ pulses are generated from the falling edge of the SHAPED DATA pulses. The pulses are also reshaped to meet the 179X requirements. VFO CLK $\div 2$ OR 4 is divided by 2 once again to obtain VFO CLK OUT whose frequency is that required by the 179X RCLK input. RCLK must be controlled by VFOE so VFOE is sampled on each rising edge of VFO CLK OUT. When VFOE goes active EN RCLK goes active in synchronization with VFO CLK OUT preventing any glitches on the RCLK output. When VFOE goes inactive EN RCLK goes inactive in synchronization with VFO CLK OUT, again preventing any glitches on the RCLK output.

Figure 14 illustrates a PPL data recovery circuit using the Western Digital 1691 Floppy Support device. Both data recovery and Write Precomp Logic is contained within the 1691, allowing low chip count and PLL reliability. The 74S124 supplies the free-running VCO output. The PUMP UP and PUMP DOWN signals from the 1691 are used to control the 74S124's frequency.

COMMAND USAGE

Whenever a command is successfully or unsuccessfully completed, the busy bit of the status register is reset and the INTRQ line is forced high. Command termination may be detected either way. The INTRQ can be tied to the host processor's interrupt with an appropriate service routine to terminate commands. The busy bit may be monitored with a user program and will achieve the same results through software. Performing both an INTRQ and a busy bit check is not recommended because a read of the status register to determine the condition of the busy bit will reset the INTRQ line. This can cause an INTRQ from not occurring.

RESTORE COMMAND

On some disk drives, it is possible to position the R/W head outward past Track 00 and prevent the TROO line from going low unless a STEP IN is first performed. If this condition exists in the drive used, the RESTORE command will never detect a TROO. Issuing several STEP IN pulses before a RESTORE command will remedy this situation. The RESTORE and all other Type I commands will execute even though the READY bit indicates the drive is not ready (NOT READY = 1).

READ TRACK COMMAND

The READ TRACK command can be used to manually inspect data on a hard copy printout. Gaps, address marks and all data are brought in to the data register during this command. The READ TRACK command may be used to inspect diskettes for valid formatting and data fields as well as address marks. Since the 179X does not synchronize clock and data until the Index Address Mark is detected, data previous to this ID mark will not be valid. READ GATE (RG) is not actuated during this command.

READ ADDRESS COMMAND

In systems that use either multiple drives or sides, the read address command can be used to tell the host processor which drive or side is selected. The current position of the R/W head is also denoted in the six bytes of data that are sent to the computer.

TRACK	SIDE	SECTOR	CRS LENGTH	CRC 1	CRC 2
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The READ ADDRESS command as well as all other Type II and Type III commands will not execute if the READY line is inactive (READY = 0). Instead, an interrupt will be generated and the NOT READY status bit will be set to a 1.

FORCED INTERRUPT COMMAND

The Forced Interrupt command is generally used to terminate a multiple sector command or to insure Type I status in the status register. The lower four bits of the command determine the conditional interrupt as follows:

$I_0 =$	NOT-READY TO READY TRANSITION
$I_1 =$	READY TO NOT-READY TRANSITION
$I_2 =$	EVERY INDEX PULSE
$I_3 =$	IMMEDIATE INTERRUPT

Regardless of the conditional interrupt set, any command that is currently being executed when the Forced Interrupt command is loaded will immediately be terminated and the busy bit will be reset indicating an idle condition.

Then, when the condition for interrupt is met, the INTRQ line will go high signifying that the condition specified has occurred.

The conditional interrupt is enabled when the corresponding bit positions of the command ($I_3 - I_0$) are set to a 1. If $I_3 - I_0$ are all set to zero, no interrupt will occur, but any command presently under execution will be immediately terminated upon receipt of the Force Interrupt command (HEX DO).

As usual, to clear the interrupt a read of the status register or a write to the command register is required. The exception is when using the immediate interrupt condition ($I_3 = 1$). If this command is loaded into the command register, an interrupt will be immediately generated and the current command terminated. Reading the status or writing to the command register will not automatically clear the interrupt; another forced interrupt command with $I_3 - I_0 = 0$ must be loaded into the command register in order to reset the INTRQ from this condition.

More than one condition may be set at a time. If for example, the READY TO NOT-READY condition ($I_1 = 1$) and the Every Index Pulse ($I_2 = 1$) are both set, the resultant command would be HEX "DA". The "OR" function is performed so that either a READY TO NOT-READY or the next Index Pulse will cause an interrupt condition.

DATA RECOVERY

Occasionally, the R/W head of the disk drive may get "off track", and dust or dirt may get trapped on the media. Both of these conditions will cause a RECORD NOT FOUND and/or a CRC error to occur. This "soft error" can usually be recovered by the following procedure:

1. Issue the command again
2. Unload and load the head and repeat step
3. Issue a restore, seek the track, and repeat step 1

If RNF or CRC errors are still occurring after trying these methods, a "hard error" may exist. This is usually caused by improper disk handling, exposure to high magnetic fields, etc. and generally results in destroying portions or tracks of the diskette.

FIGURE 1. DEVICE CHARACTERISTICS

DEVICE	SNGL DENSITY	DBLE DENSITY	INVERTED BUS	TRUE BUS	DOUBLE-SIDED
1791	X	X	X		
1792	X	X	X		
1793	X	X		X	
1794	X	X	X	X	
1795	X	X		X	X
1797	X	X			X

FIGURE 2. STORAGE CAPACITIES

SIZE	DENSITY	SIDES	UNFORMATTED CAPACITY (NOMINAL)		BYTE TRANSFER TIME	FORMATTED CAPACITY	
			PER TRACK	PER DISK		PER TRACK	PER DISK
5 ¹ / ₄ "	SINGLE	1	3125	109,375*	64μs	2304**	80,640
5 ¹ / ₄ "	DOUBLE	1	6250	218,750	32μs	4608***	161,280
5 ¹ / ₄ "	SINGLE	2	3125	218,750	64μs	2304	161,280
5 ¹ / ₄ "	DOUBLE	2	6250	437,500	32μs	4608	322,560
8"	SINGLE	1	5208	401,016	32μs	3328	256,256
8"	DOUBLE	1	10,416	802,032	16μs	6656	512,512
8"	SINGLE	2	5208	802,032	32μs	3328	512,512
8"	DOUBLE	2	10,416	1,604,064	16μs	6656	1,025,024

*Based on 35 Tracks/Side

**Based on 18 Sectors/Track (128 byte/sec)

***Based on 18 Sectors/Track (256 bytes/sec)

FIGURE 3. NOMINAL VS. WORSE CASE SERVICE TIME

SIZE	DENSITY	NOMINAL TRANSFER TIME	WORST-CASE 179X SERVICE TIME	
			READ	WRITE
5½"	SINGLE	64µs	55.0µs	47.0µs
5½"	DOUBLE	32µs	27.5µs	23.5µs
8"	SINGLE	32µs	27.5µs	23.5µs
8"	DOUBLE	16µs	13.5µs	11.5µs

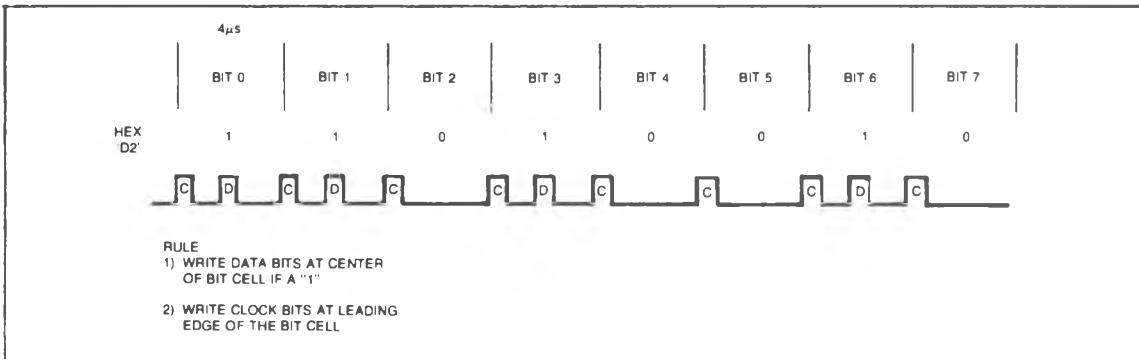
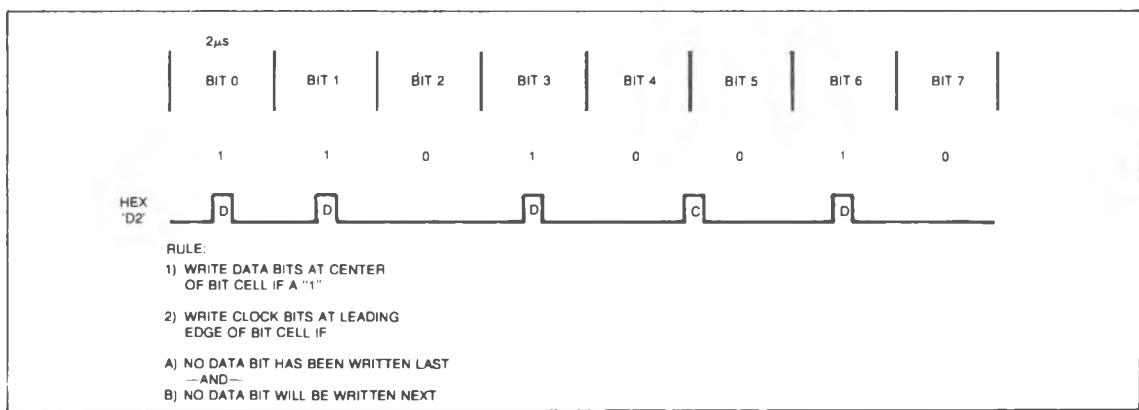
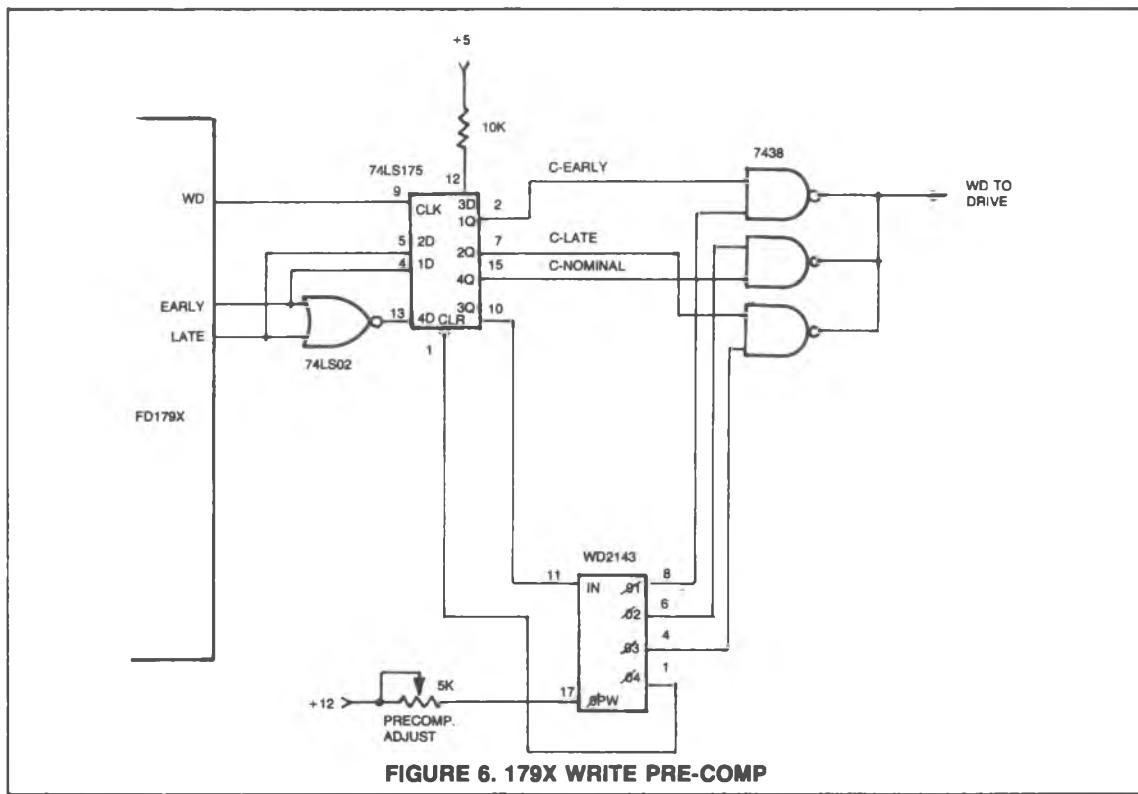
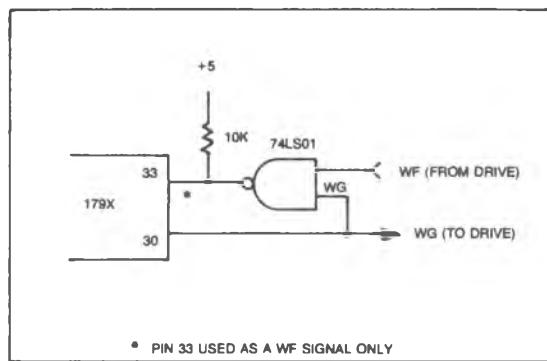
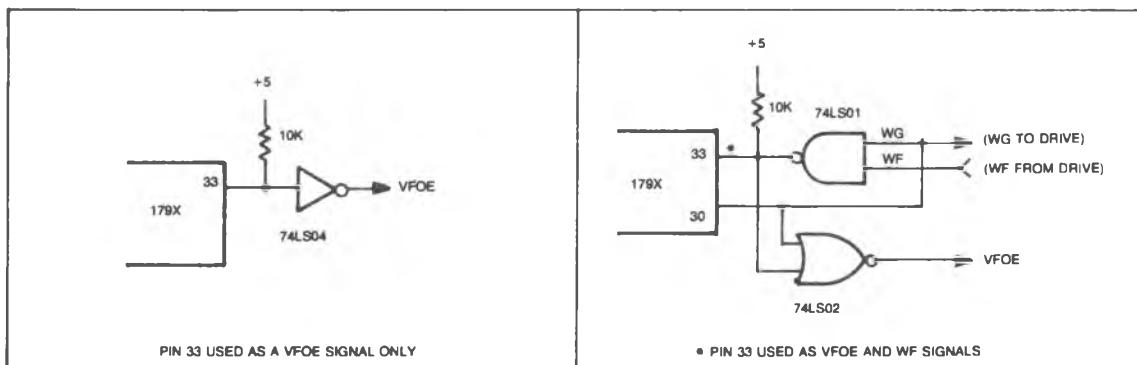
FIGURE 4A. FM RECORDING**FIGURE 4B. MFM RECORDING**

FIGURE 5. WF/VFOE DEMULTIPLEXING CIRCUITY



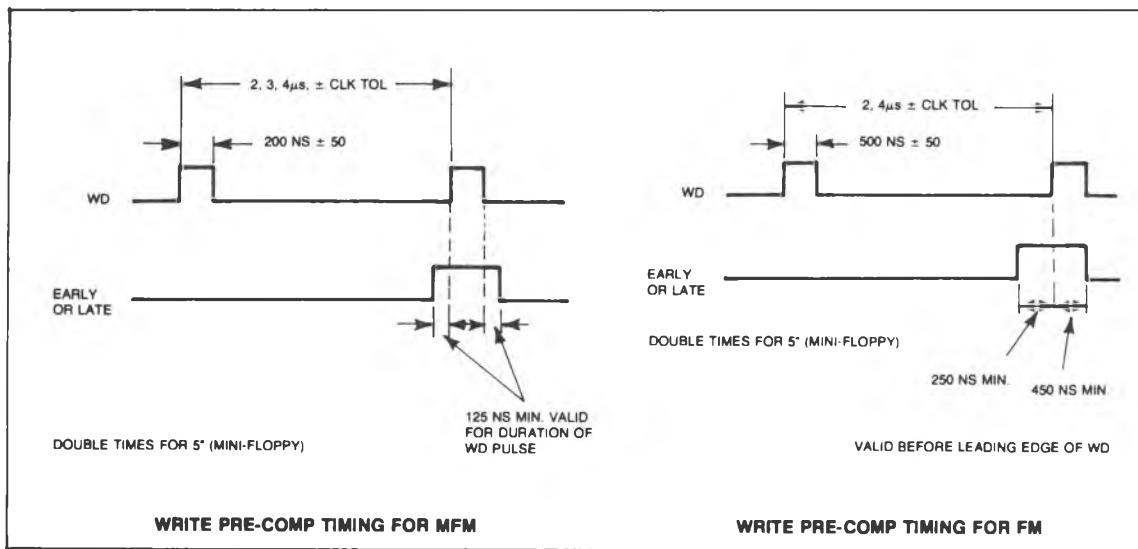


FIGURE 7. WRITE PRE-COMP TIMING

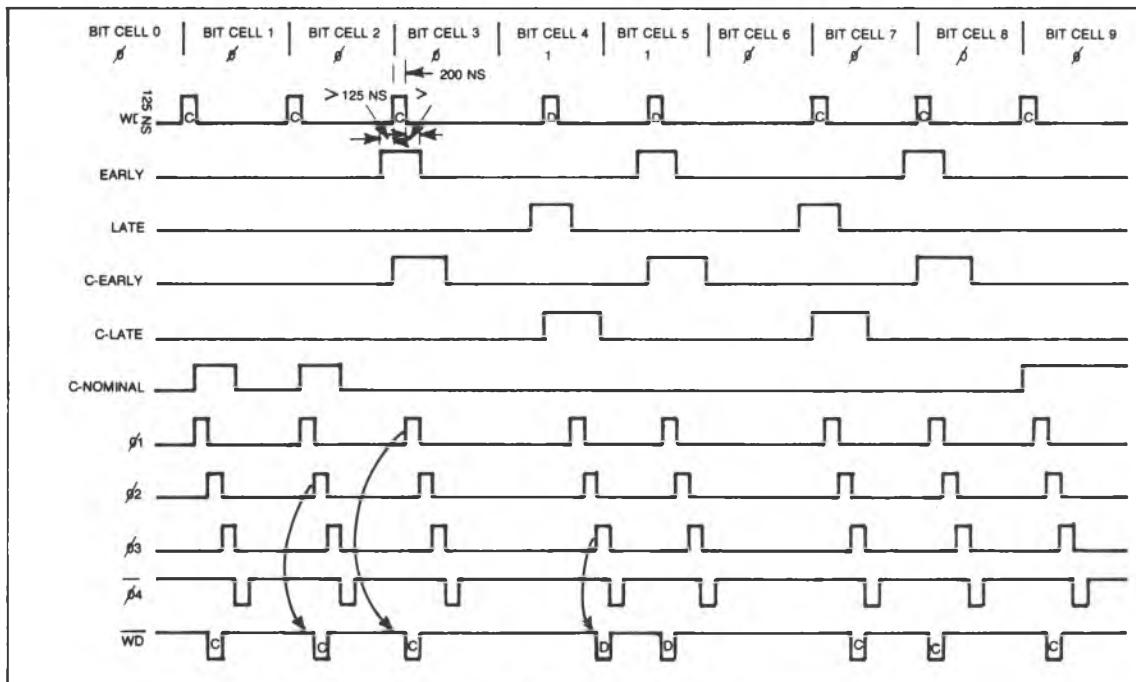


FIGURE 8. PRECOMP TIMING FOR CIRCUIT IN FIGURE 6

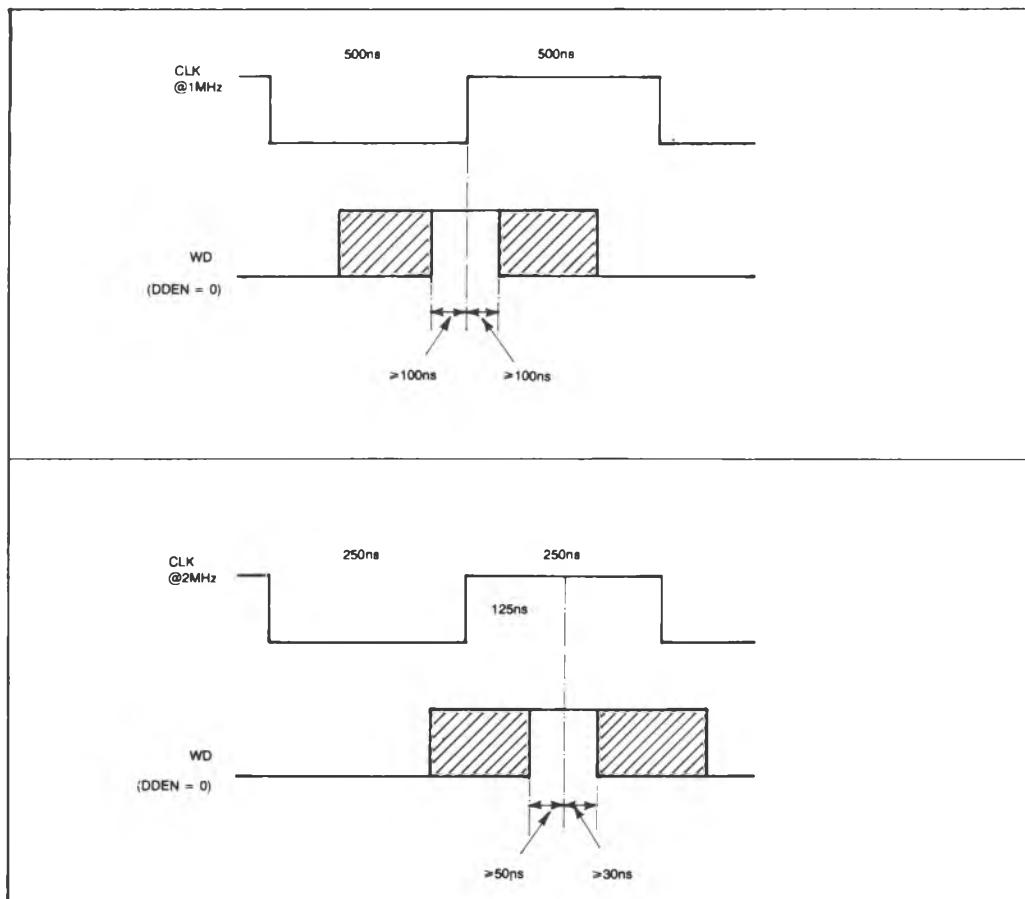
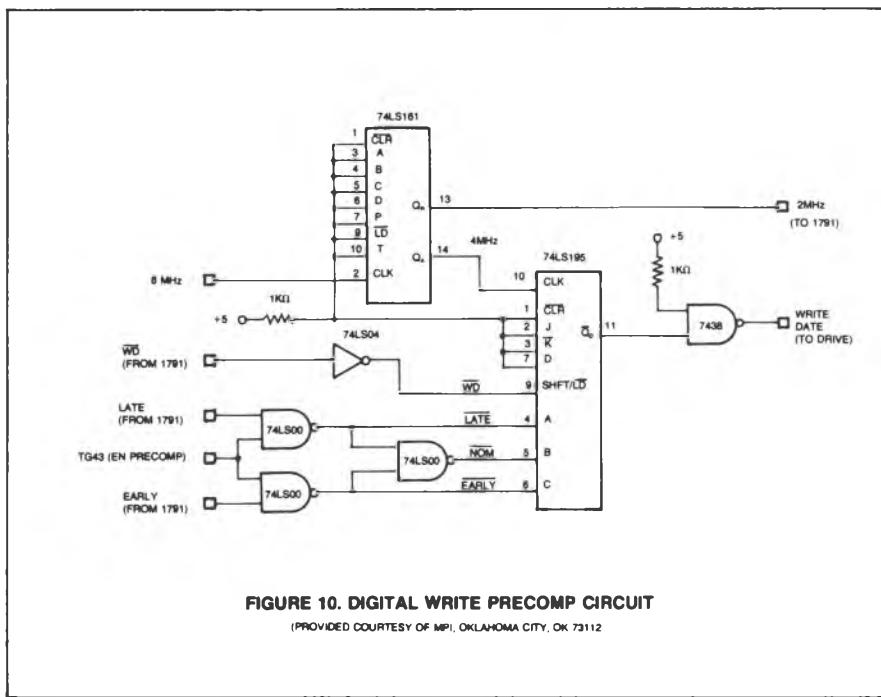


FIGURE 9. WD/CLK RELATIONSHIP FOR WRITE PRECOMP USE



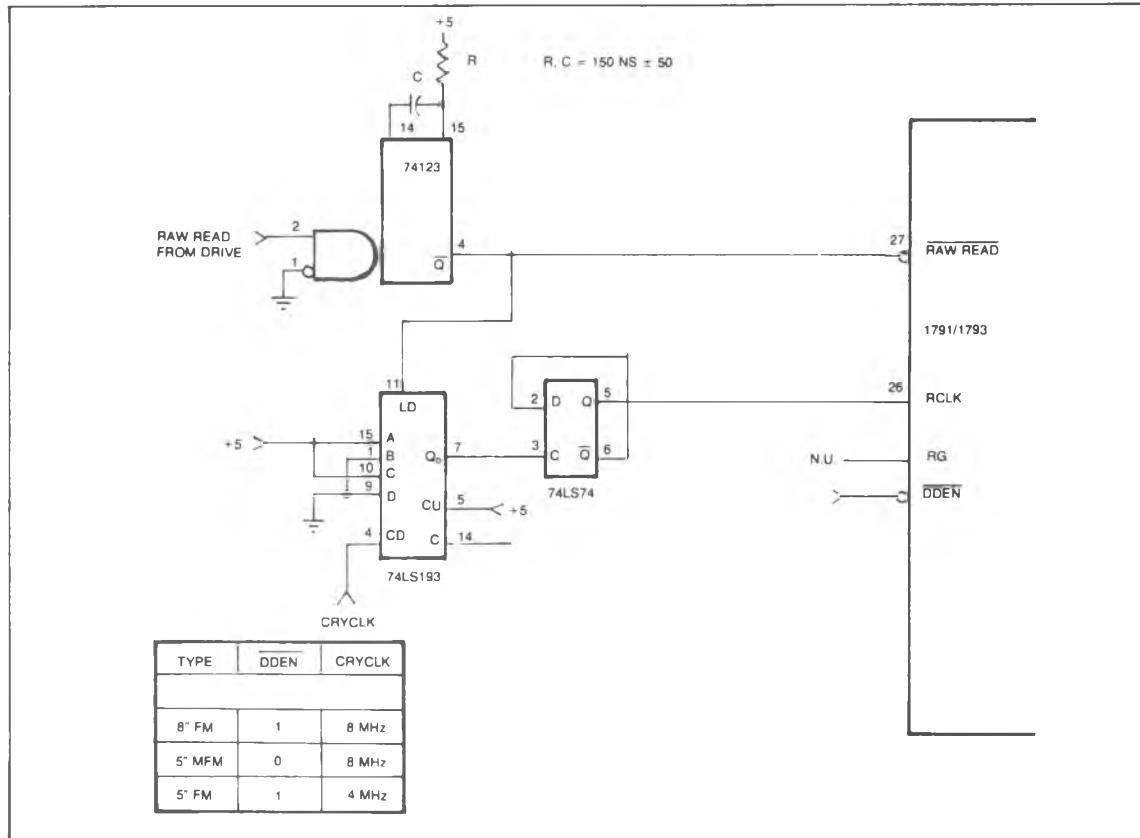
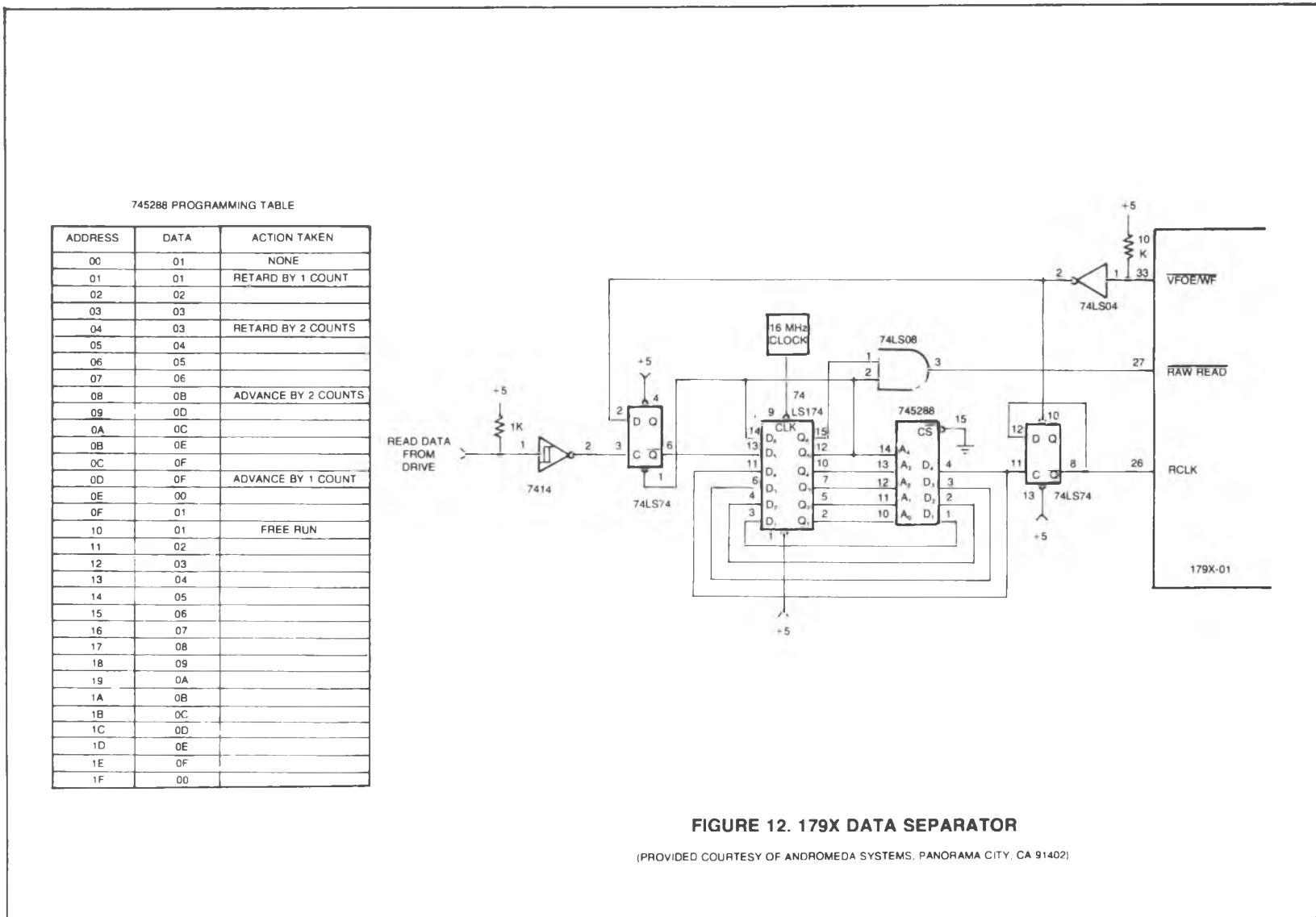
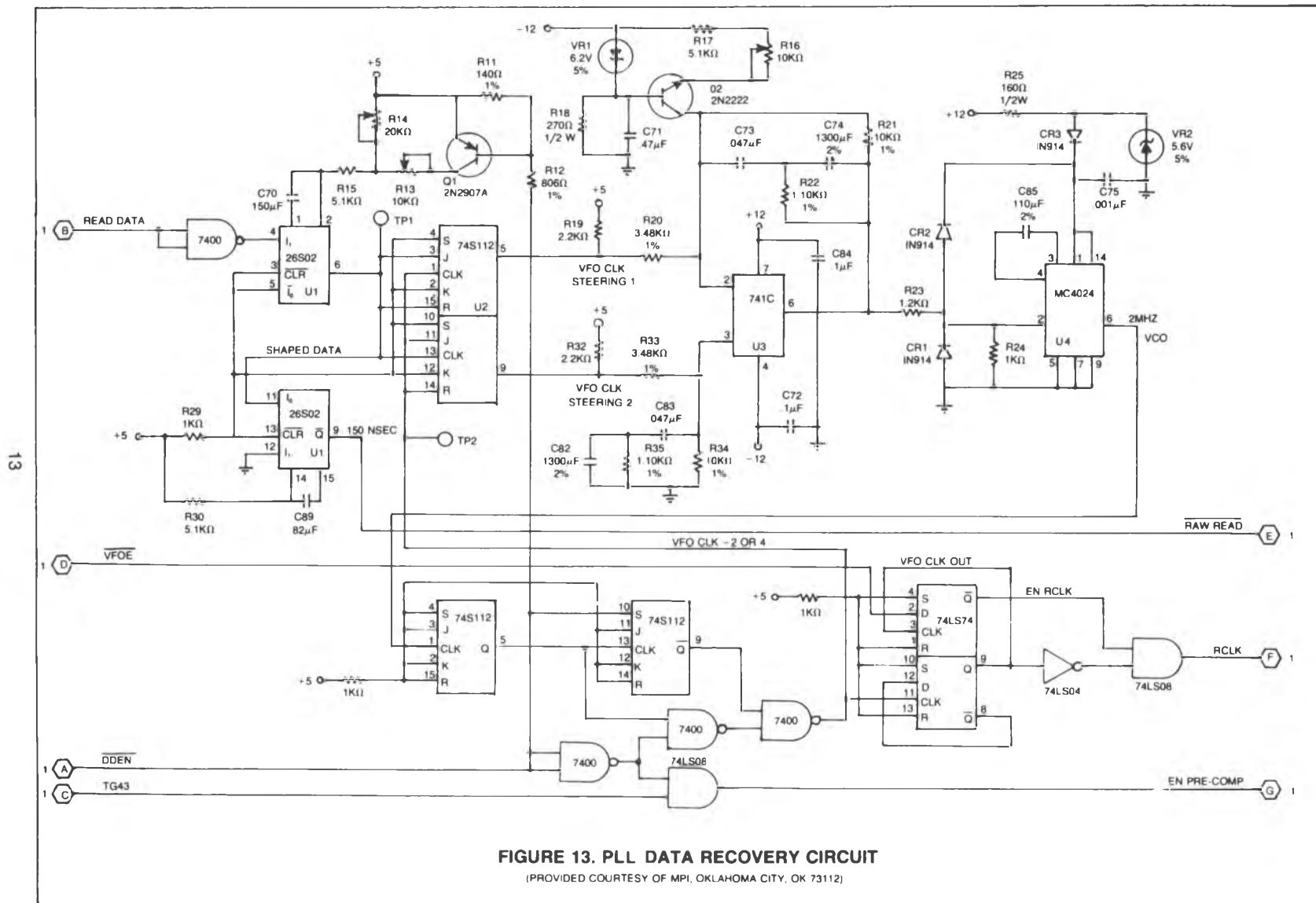
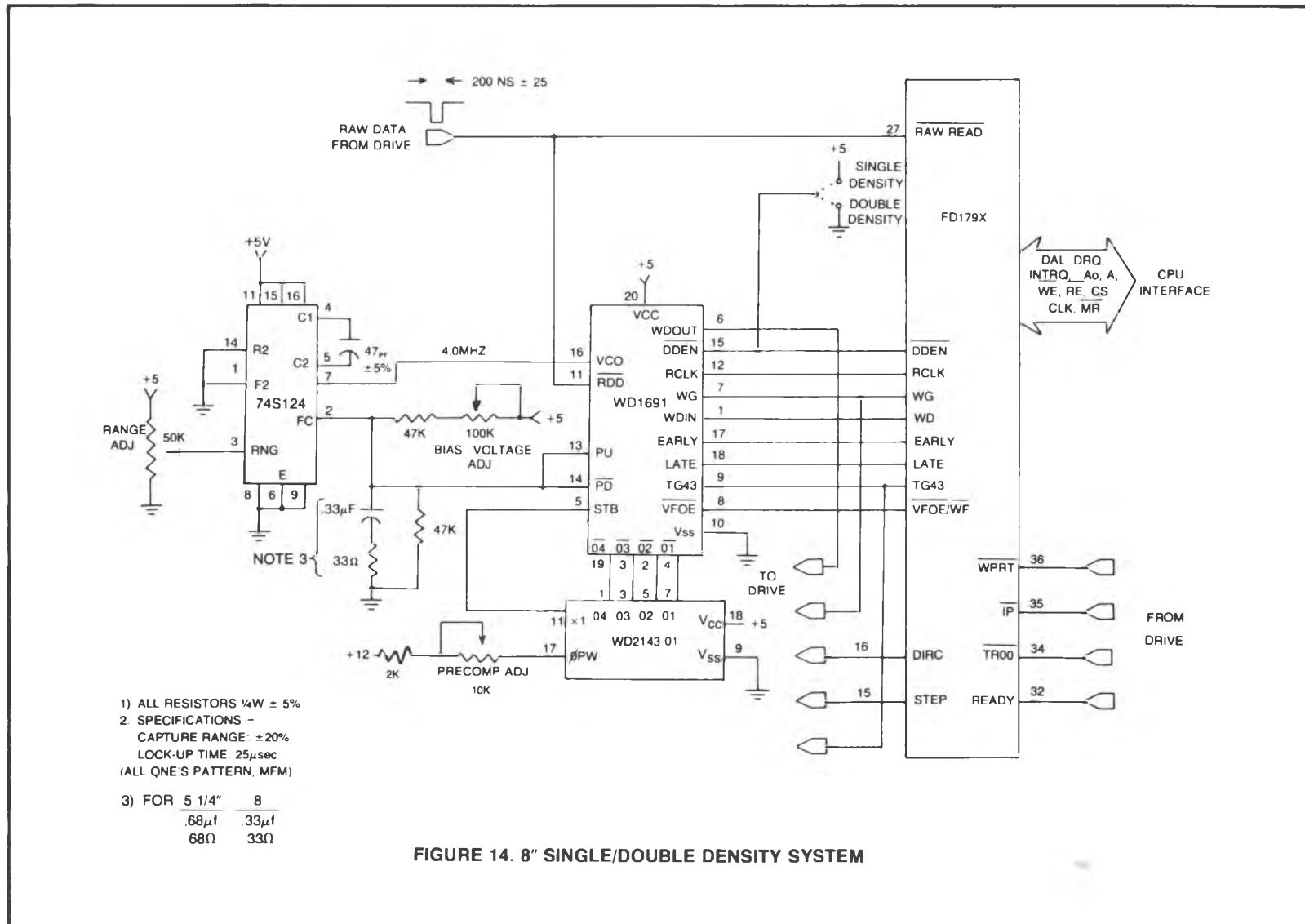


FIGURE 11. COUNTER/SEPARATOR







COMMAND SUMMARY

		BITS							
TYPE COMMAND		7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r ₁	r ₀
I	Seek	0	0	0	1	h	V	r ₁	r ₀
I	Step	0	0	1	u	h	V	r ₁	r ₀
I	Step In	0	1	0	u	h	V	r ₁	r ₀
I	Step Out	0	1	1	u	h	V	r ₁	r ₀
II	Read Sector	1	0	0	m	S	E	C	0
II	Write Sector	1	0	1	m	S	E	C	a ₀
III	Read Address	1	1	0	0	0	E	0	0
III	Read Track	1	1	1	0	0	E	0	0
III	Write Track	1	1	1	1	0	E	0	0
IV	Force Interrupt	1	1	0	1	I ₃	I ₂	I ₁	I ₀

Note: Bits shown in TRUE form.

STEPPING RATES

CLK	2 MHz	2 MHz	1 MHz	1 MHz	2 MHz	1 MHz
DDEN	0	1	0	1	X	X
R ₁ , R ₀	TEST=1	TEST=1	TEST=1	TEST=1	TEST=0	TEST=0
0 0	3 ms	3 ms	6 ms	6 ms	184μs	368μs
0 1	6 ms	6 ms	12 ms	12 ms	190μs	380μs
1 0	10 ms	10 ms	20 ms	20 ms	198μs	396μs
1 1	15 ms	15 ms	30 ms	30 ms	208μs	416μs

FLAG SUMMARY**TYPE I COMMANDS**

h = Head Load Flag (Bit 3)
h = 1, Load head at beginning
h = 0, Unload head at beginning

V = Verify flag (Bit 2)

V = 1, Verify on destination track
V = 0, No verify

r₁r₀ = Stepping motor rate (Bits 1-0)

Refer to Table 1 for rate summary

u = Update flag (Bit 4)

u = 1, Update Track register
u = 0, No update

FLAG SUMMARY**TYPE II & III COMMANDS**

m = Multiple Record flag (Bit 4)

m = 0, Single Record
m = 1, Multiple Records

a₀ = Data Address Mark (Bit 0)

a₀ = 0, FB (Data Mark)
a₀ = 1, F8 (Deleted Data Mark)

E = 15 ms Delay (2MHz)

E = 1, 15 ms delay

E = 0, no 15 ms delay

S = Side Select Flat

S = 0, Compare for Side 0

S = 1, Compare for Side 1

C = Side Compare Flag

C = 0, disable side select compare

C = 1, enable side select compare

FLAG SUMMARY**TYPE IV COMMAND**

i = Interrupt Condition flags (Bits 3-0)

I₀ = 1, Not-Ready to Ready Transition
I₁ = 1, Ready to Not-Ready Transition
I₂ = 1, Index Pulse
I₃ = 1, Immediate Interrupt

I₃-I₀ = 0, Terminate with no interrupt

This is a preliminary specification with tentative device parameters and may be subject to change after final product characterization is completed.

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Appendix C

WD1691 DATA INFORMATION

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WESTERN DIGITAL

C O R P O R A T I O N

WD1691 FLOPPY SUPPORT LOGIC (F.S.L.)

October, 1980

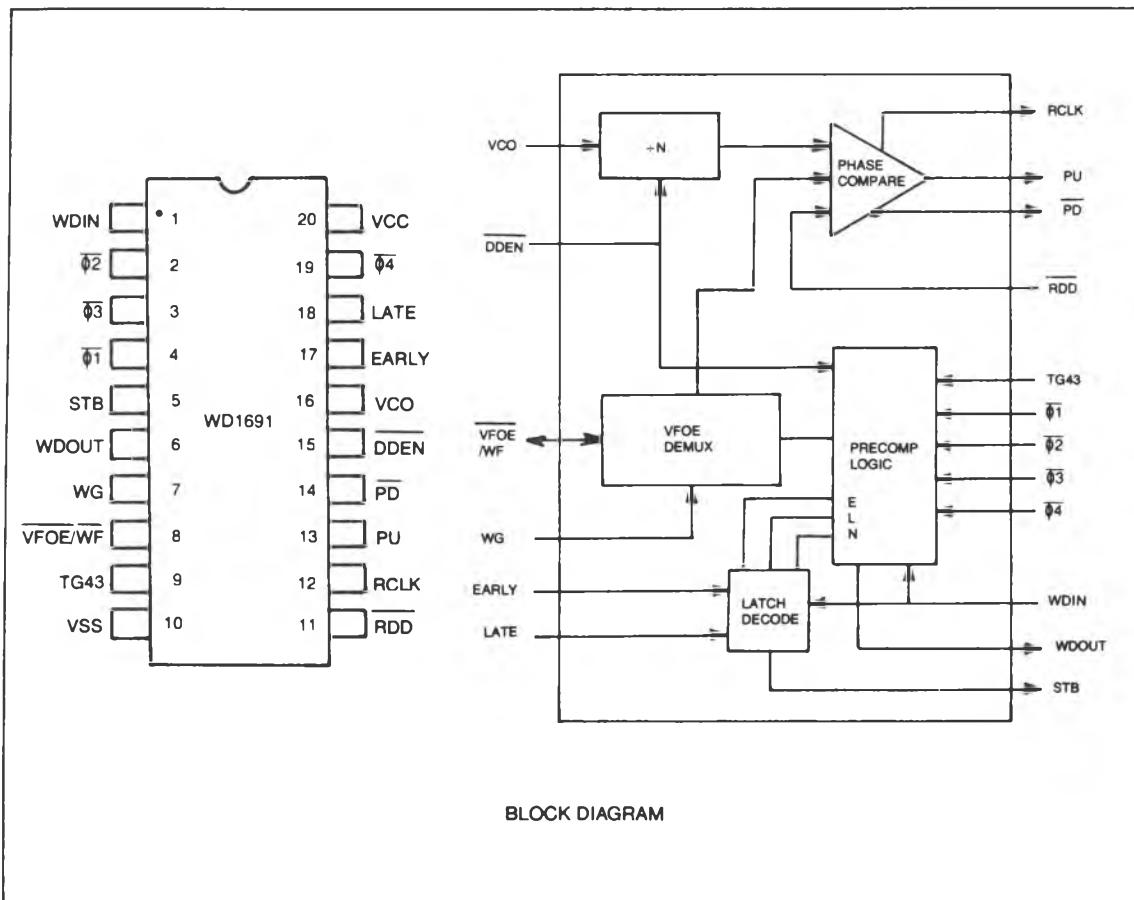
FEATURES

- Direct interface to the FD179X
- Eliminates external FDC Logic
- Data Separation/RCLK GENERATION
- Write Precompensation Signals
- VFOE/WF Demultiplexing
- Programmable Density
- 8" or 5.25" Drive Compatible
- All inputs and outputs TTL Compatible
- Single +5V Supply

GENERAL DESCRIPTION

The WD1691 F.S.L. has been designed to minimize the external logic required to interface the 179X Family of Floppy Disk Controllers to a drive. With the use of an external VCO, the WD 1691 will generate the RCLK signal for the WD179X, while providing an adjustment pulse (PUMP) to control the VCO frequency. VFOE/WF de-multiplexing is also accomplished and Write Precompensation signals have been included to interface directly with the WD2143 Clock Generator.

The WD1691 is implemented in N-MOS silicon gate technology and is available in a plastic or ceramic 20 pin dual-in-line package.



PIN	NAME	SYMBOL	FUNCTION
1	WRITE DATA INPUT	WDIN	Ties directly to the FD179X WD pin.
2, 3, 4, 19	PHASE 2, 3, 1, 4	Φ2 Φ3 Φ1 Φ4	4 Phase inputs to generate a desired Write Precompensation delay. These signals tie directly to the WD2143 Clock Generator.
5	STROBE	STB	Strobe output from the 1691. Strobe will latch at a high level on the leading edge of WDIN and reset to a low level on the leading edge of 04.
6	WRITE DATA OUTPUT	WDOUT	Serial, pre-compensated Write data stream to be sent to the disk drive's WD line.
7	WRITE GATE	WG	Ties directly to the FD179X WG pin.
8	VFO ENABLE/ WRITE FAULT	VFOE/WF	Ties directly to the FD179X VFOE/WF pin.
9	TRACK 43	TG43	Ties directly to the FD179X TG43 pin, If Write Compensation is required on TRACKS 44-76.
10	V _{ss}	V _{ss}	Ground
11	READ DATA	RDD	Composite clock and data stream input from the drive.
12	READ CLOCK	RCLK	RCLK signal generated by the WD1691, to be tied to the FD179X RCLK pin.
13	PUMP UP	PU	Tri-state output that will be forced high when the WD1691 requires an increase in VCO frequency.
14	PUMP DOWN	PD	Tri-state output that will be forced low when the WD1691 required a decrease in VCO frequency.
15	Double Density Enable	DDEN	Double Density Select input. When Inactive (High), the VCO frequency is internally divided by two.
16	Voltage Controlled Oscillator	VCO	A nominal 4.0MHz (8" drive) or 2.0MHz (5.25" drive) master clock input.
17, 18	EARLY LATE	EARLY LATE	EARLY and LATE signals from the FD179X, used to determine Write Precompensation.
20	V _{cc}	V _{cc}	+ 5V ± 10% power supply

DEVICE DESCRIPTION

The WD1691 is divided into two sections:

- 1) Data Recovery Circuit
- 2) Write precompensation Circuit

The Data Separator or Recovery Circuit has four inputs: DDEN, VCO, RDD, and VFOE/WF; and three outputs: PU, PD and RCLK. The VFOE/WF input is used in conjunction with the Write Gate signal to enable the Data recovery circuit. When Write Gate is high, a write operation is taking place, and the data recovery circuits are disabled, regardless of the state on any other inputs.

When VFOE/WF and WRITE GATE are low, the data recovery circuit is enabled. When the RDD line goes Active Low, the PU or PD signals will become active. If the RDD line has made its transition in the beginning of the RCLK window, PU will go from a HI-Z state to a Logic I, requesting an increase in VCO frequency. If the RDD line has made its transition at the end of the RCLK window, PU will remain in a HI-Z state while PD will go to a logic zero, requesting a decrease in VCO frequency. When the leading edge of RDD occurs in the center of the RCLK window, both PU and PD will remain tri-stated, indicating that no adjustment of the VCO frequency is needed. The RCLK signal is a divide-by-16 (DDEN=1) or a divide-by-8 (DDEN=0) of the VCO frequency.

WG	VFOE/WF	RDD	PU + PD
1	X	X	HI-Z
0	1	X	HI-Z
0	0	1	HI-Z
0	0	0	Enable

The Write Precompensation circuit has been designed to be used with the WD2143-01 clock generator. When the WD1691 is operated in a "single density only" mode, write precompensation as well as the WD2143-01 is not needed. In this case, Q1, Q2, Q3, Q4, and STB should be tied together, DDEN left open, and TG43 tied to ground.

In the double-density mode (DDEN=0), the signals Early and Late are used to select a phase input (Q1 – Q4) on the leading edge of WDIN. The STB line is latched high when this occurs, causing the WD2143-01 to start its pulse generation. Q2 is used as the write data pulse on nominal (Early=Late=0). Q2 is used for early, and Q3 is used for late. The leading edge of Q4 resets the STB line in anticipation of the next write data pulse. When TG43=0 or DDEN=1, Precompensation is disabled and any transitions on the WDIN line will appear on the WDout line. If write precompensation is desired on all tracks, leave TG43 open (an internal pull-up will force a Logic I) while DDEN=0.

The signals, DDEN, TG43, and RDD have internal pull-up resistors and may be left open if a logic I is desired on any of these lines.

The minimum Voh level on PU is specified at 2.4V, sourcing 200ua. During PUMP UP time, this output will "drift" from a tri-state to .4V minimum. By tying PU and PD together, a PUMP signal is created that will be forced low for a decrease in VCO frequency and forced high for an increase in VCO frequency. To speed up rise times and stabilize the output voltage, a resistor divider can be used to set the tri-state level to approximately 1.4V. This yields a worst case swing of ± 1 V; acceptable for most VCO chips with a linear voltage-to-frequency characteristic.

Both PU and PD signals are affected by the width of the RAW READ (RDD) pulse. The wider the RAW READ pulse, the longer the PU or PD signal (depending upon the phase relationship to RCLK) will remain active. If the RAW READ pulse exceeds 250ns. (VCO = 4MHz, DDEN = 0) or 500ns. (VCO = 4MHz, DDEN = 1), then both a PU and PD will occur in the same window. This is undesirable and reduces the accuracy of the external integrator or low-pass filter to convert the PUMP signals into a slow moving D.C. correction voltage.

Eventually, the PUMP signals will have corrected the VCO input to exactly the same frequency multiple as the RAW READ signal. The leading edge of the RAW READ pulse will then occur in the exact center of the RCLK window, an ideal condition for the FD179X internal recovery circuits.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias -25° to 70°C
 Voltage on any pin with respect
 to Ground (V_{SS}) -0.2 to +7V
 Power Dissipation 1W

Storage Temp.—Ceramic—65°C to +150°C
 Plastic—55°C to +125°C

NOTE: Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Electrical characteristics.

DC ELECTRICAL CHARACTERISTICS

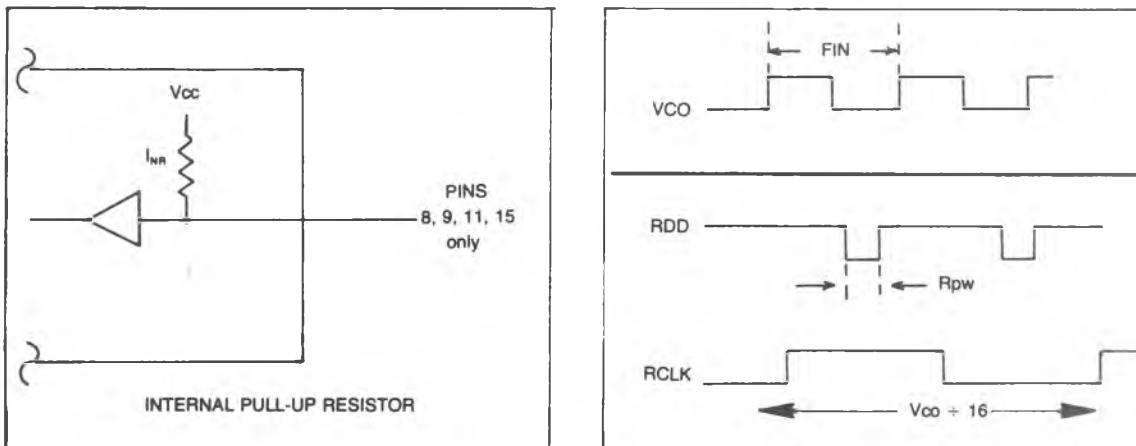
T_A = 0° to 70°C; V_{CC} = 5.0V±10%; V_{SS} = OV

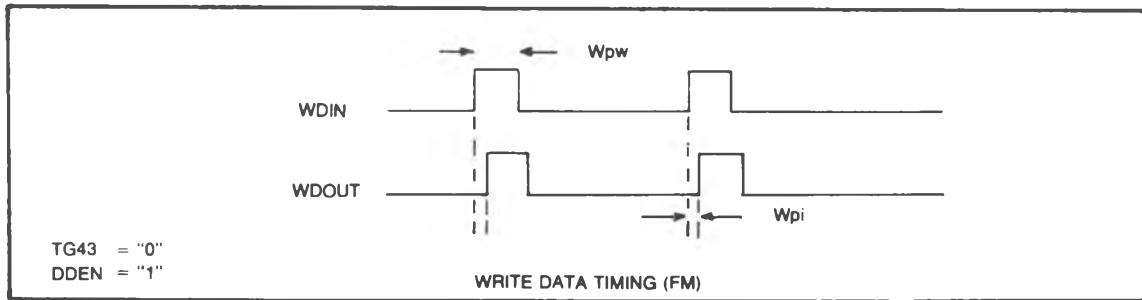
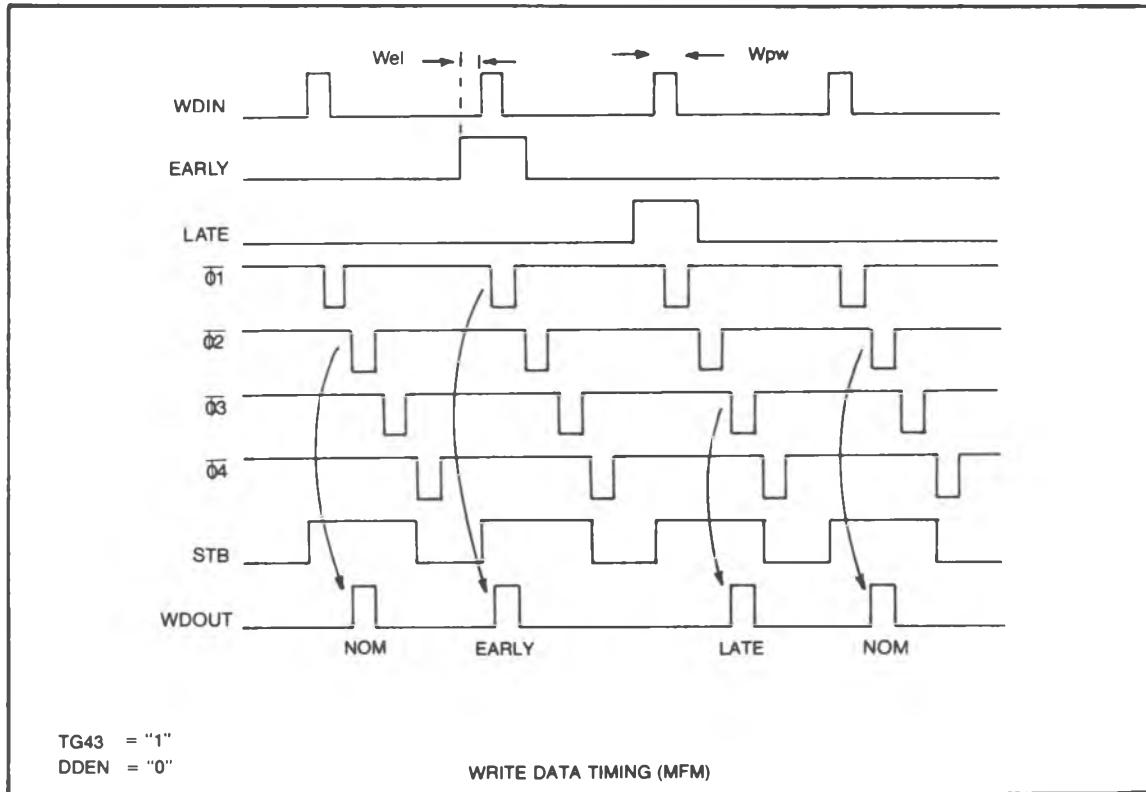
SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
V _{IL}	Input Low Voltage	-0.2		+0.8	V	
V _{IH}	Input High Voltage	2.0			V	
V _{OL}	Output Low Voltage			0.45	V	I _{OL} =3.2mA
V _{OH}	High Level Output Voltage	2.4			V	I _{OH} =-200μa
V _{CC}	Supply Voltage	4.5	5.0	5.5	V	
i _{CC}	Supply Current		40	100	MA	All outputs open

AC ELECTRICAL CHARACTERISTICS

T_A = 0° to 70°C; V_{CC} = 5V±10%; V_{SS} = OV

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
FIN	VCO Input Frequency	.5	4	6	MHz	DDEN=0
		.5	2	6	MHz	DDEN=1
R _{DW}	RDD Pulse Width	100	200		ns.	
W _{EI}	EARLY (LATE) to WDIN	100			ns.	
P _{on}	PUMP UP/DN Time	0		250	ns.	
W _{DI}	WDIN to WDOUT			80	ns.	DDEN=1
I _{NR}	Internal Pull-up Resistor	4.0	6.5	10	KΩ	





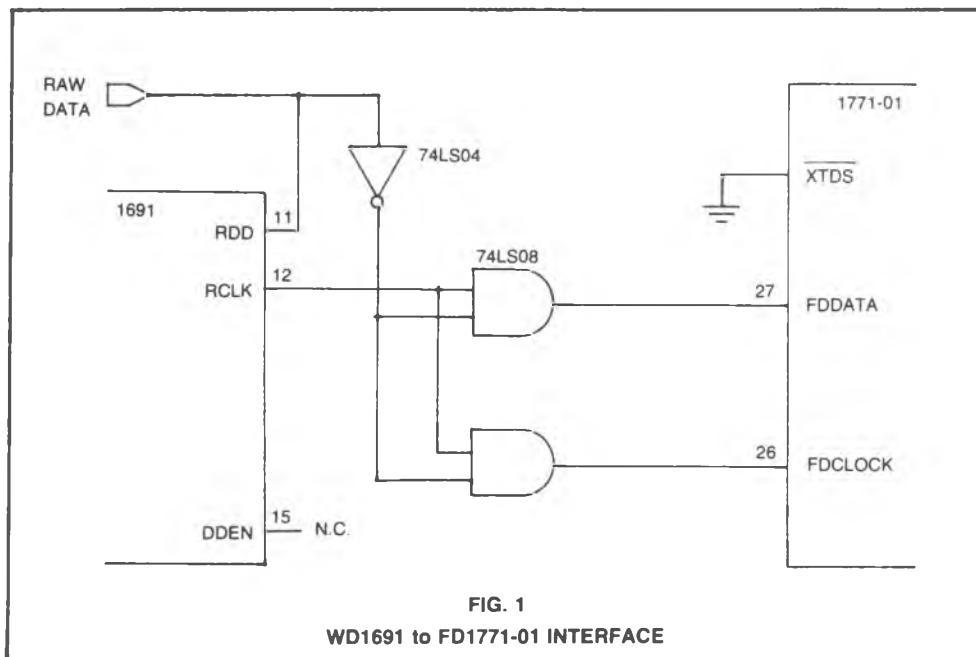
TYPICAL APPLICATIONS

Figure 1 illustrates the 1691 to FD1771-01 floppy disk controller. The RCLK signal is used to gate the RAW data pulses which are inverted by the 74LS04 inverter. Since RCLK will be high during data and low during clock a 74LS08 is used to switch the proper clock or data pulse to the FD1771.

Shown in Figure 2 is a Phase-Lock Loop data separator and the support logic for a single and double-density 8" drive. The raw data (Both clock and data bits) are fed to the WD1691 and FD179X. The WD1691 outputs its PU or PD signal, which is integrated by the .33uf capacitor and 33ohm resistor to form a control voltage for the 74S124 VCO device. The 4.0MHZ nominal output of the VCO then feeds back to the WD1691 completing the loop. The WD2143-01 is also used, providing write precompensation when in double-density, from tracks 44-77. The DDEN line can either be controlled by a toggle switch or a logic level from the host system.

To adjust write precompensation, issue a command to the FD179X so that write data pulses are present. This can be done with a 'WRITE TRACK' command and the IP line open, or a continuous 'WRITE SECTOR' operation. With a scope on pin 4 of the WD1691, adjust the precomp pot for the desired value. This will range from 100 to 300 ns typically. The pulse width set on pin 4 (01) will be the desired precomp delay from nominal.

The data separator must be adjusted with the RDD or VFOE/WF line at a Logic 1. Adjust the bias voltage potentiometer for 1.4V on pin 2 of the 74S124. Then adjust the range control to yield 4.0MHZ on pin 7 of the 74S124.



SUBSTITUTING VCO's

There are other VCO circuits available that may be substituted for the 74S124. The specifications required are:

- 1) The VCO must free run at 4.0MHz with a 1.4V control signal. The WD1691 will force this voltage 1 Volt in either direction (i.e., .4V = decrease frequency, 2.4V = increase frequency). If a $\pm 15\%$ capture range is desired, then a 1 Volt change on the VCO input should change the frequency by 15%. Capture range should be limited to about $\pm 25\%$, to prevent the VCO from breaking into oscillation and/or losing lock because of noise spikes (causing abnormally quick adjustments of the VCO frequency). Jitter in the VCO output frequency may further be reduced by increasing the integration capacitor/resistor, but this will also decrease the final capture range and lock-up time.
- 2) The sink output current of the WD1691 is 3.2ma minimum. The source output current is -200ua. Therefore, source current is the limiting factor. Insure that the input circuitry of the VCO does not require source current in excess of -200ua.

Another alternative is to use a voltage follower/level shifter circuit to match the input requirements of the VCO chosen. A more complex filter can be used to convert the PUMP UP/PUMP DOWN pulses to the varying DC voltage signal required by the VCO, achieving an optimum condition between lock-up time and high frequency rejection.

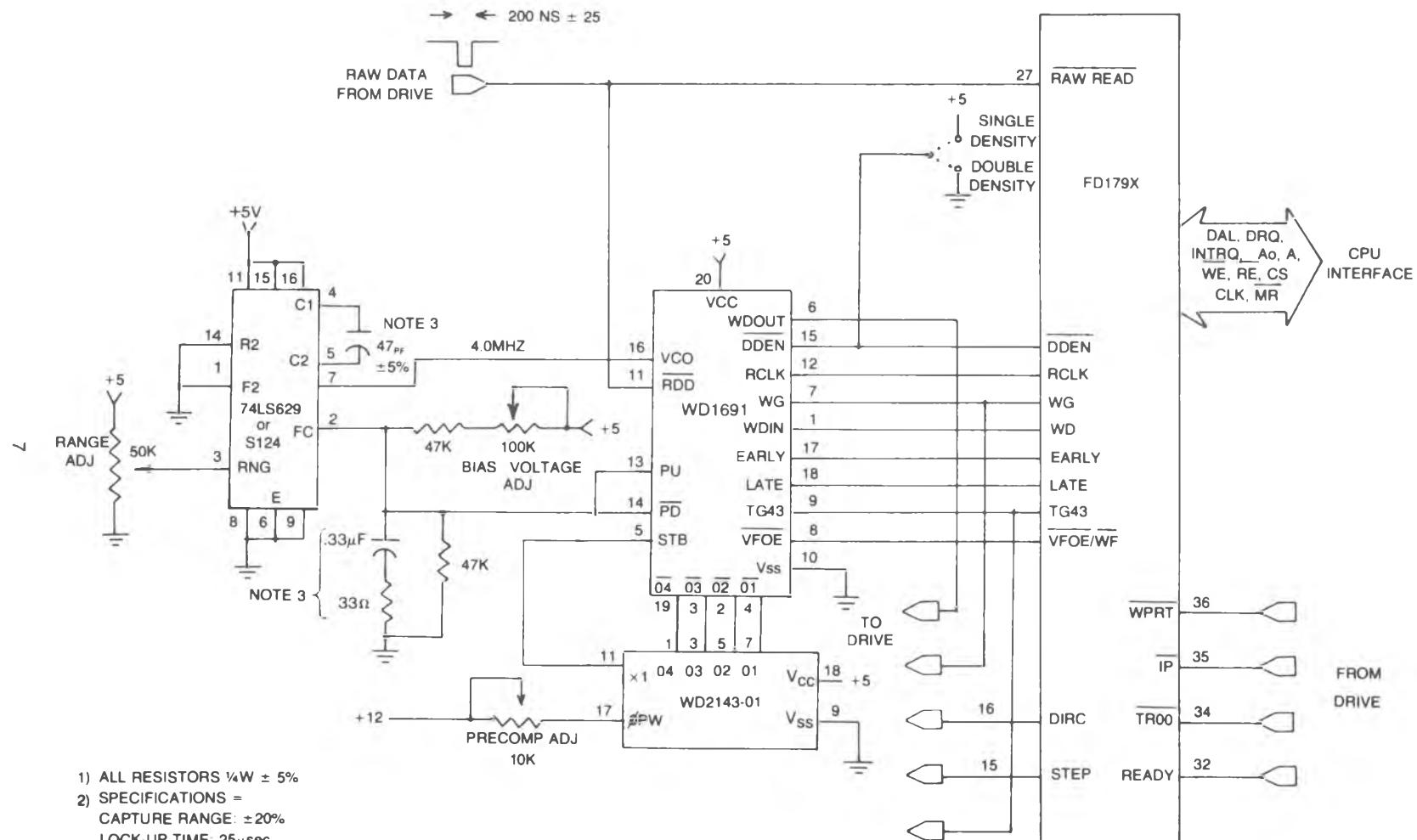
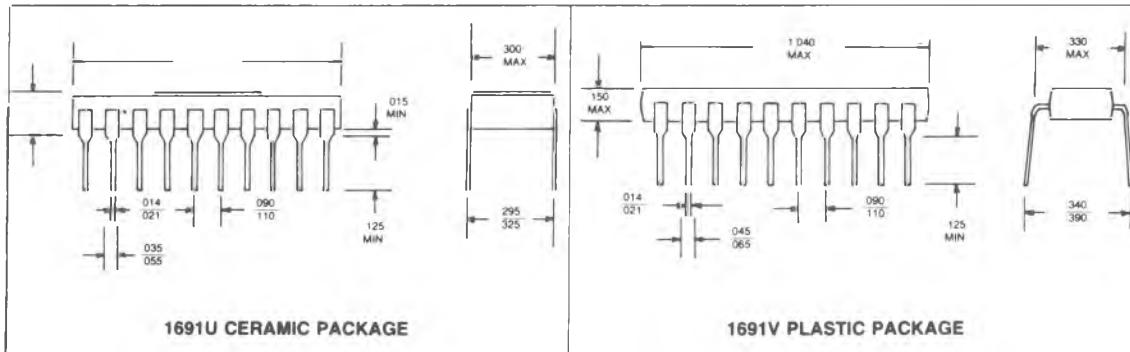


FIG. 2
8" SINGLE/DOUBLE DENSITY FLOPPY INTERFACE



This is a preliminary specification with tentative device parameters and may be subject to change after final product characterization is completed.

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Appendix D

WD2143-01 DATA INFORMATION

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WESTERN DIGITAL

C O R P O R A T I O N

WD2143-03 Four Phase Clock Generator

SEPTEMBER, 1981

FEATURES

- IMPROVED VERSION OF WD2143-01
- TRUE AND INVERTED OUTPUTS
- SINGLE 5 VOLT SUPPLY
- TTL COMPATABLE
- ON CHIP OSCILLATOR
- TTL CLOCK INPUTS
- TTL CLOCK OUTPUT
- PROGRAMMABLE PULSE WIDTHS
- PROGRAMMABLE PHASE WIDTHS
- NO EXTERNAL CAPACITOR

GENERAL DESCRIPTION

The WD2143-03 Four-Phase Clock Generator is a MOS/LSI device capable of generating four phase clocks. The output pulse widths are controlled by tying an external resistor to the proper control inputs. All pulse widths may be set to the same width by tying the ϕ_{PW} line through an external resistor. Each pulse width can also be individually programmed by tying a resistor through the appropriate ϕ_{1PW} — ϕ_{4PW} control inputs.

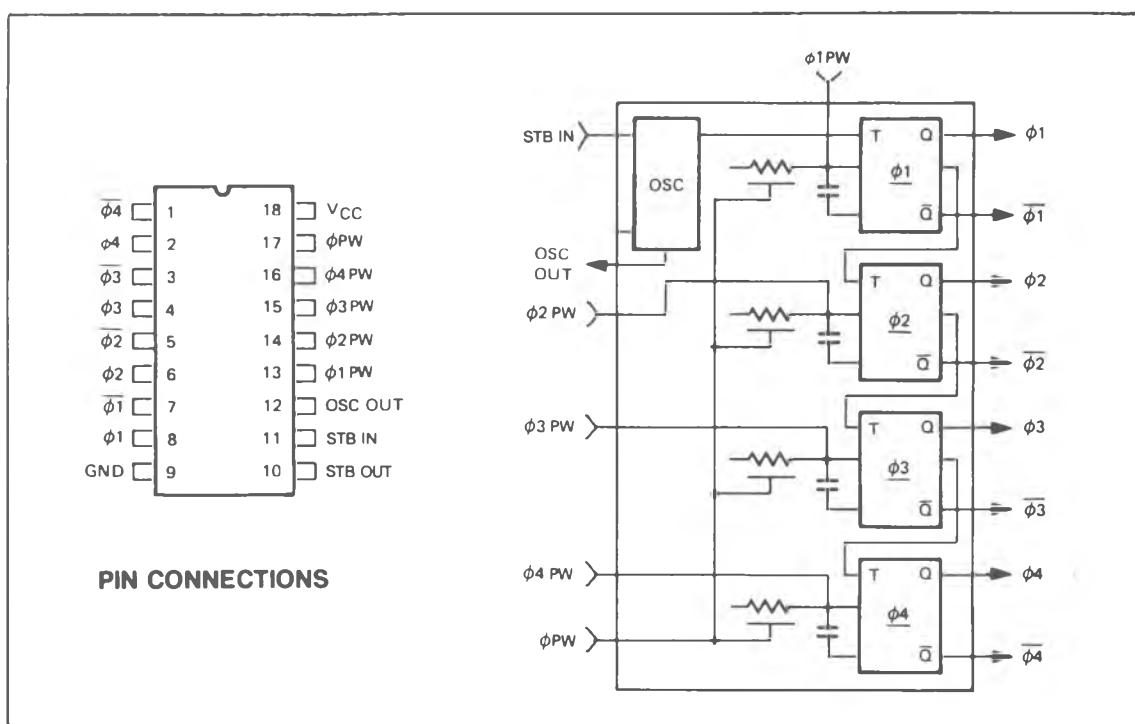


Figure 1 WD2143-03 PIN CONNECTIONS AND BLOCK DIAGRAM

DEVICE OPERATION

Each of the phase outputs can be controlled individually by tying an external resistor from ϕ_{1PW} — ϕ_{4PW} to a +5V supply. When it is desired to have ϕ_1 through ϕ_4 outputs the same width, the ϕ_{1PW} — ϕ_{4PW} inputs should be left open and an external resistor tied from the ϕ_{PW} (Pin 17) input to +12V.

STROBE IN (pin 11) is driven by a TTL square wave with STROBE OUT (pin 10) left open. Each of the four phase outputs provide both true and inverted signals, capable of driving 1 TTL load each.

PIN NUMBER	SYMBOL	DESCRIPTION
1, 3, 5, 7	$\overline{\phi_1 - \phi_4}$	Four phase clock outputs. These outputs are inverted (active low).
2, 4, 6, 8	$\phi_1 - \phi_4$	Four Phase clock outputs. These outputs are true (active high).
9	GND	Ground
10	STB OUT	This pin is left unconnected.
11	STB IN	Input signal to initiate four-phase clock outputs.
12	N.C.	No connection
13-16	$\phi_{1PW} - \phi_{4PW}$	External resistor inputs to control the individual pulse widths of each output. These pins can be left open if ϕ_{PW} is used.
17	ϕ_{PW}	External resistor input to control all phase outputs to the same pulse widths.
18	V _{cc}	+5V ± 5% power supply input

Table 1 PIN DESCRIPTIONS

TYPICAL APPLICATIONS

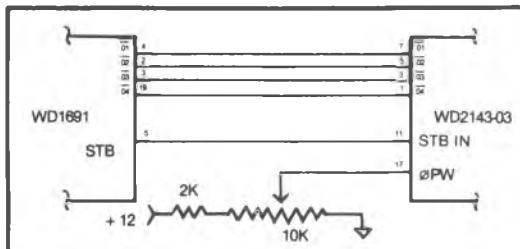
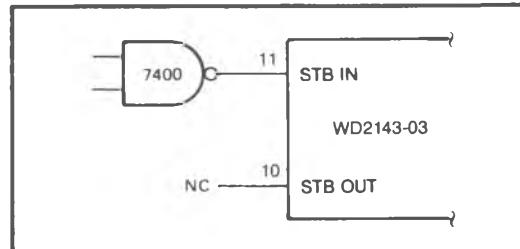
Figure 2 WRITE PRECOMP OPERATION WITH F.S.L.
WD1691

Figure 3 TTL SQUARE WAVE OPERATION

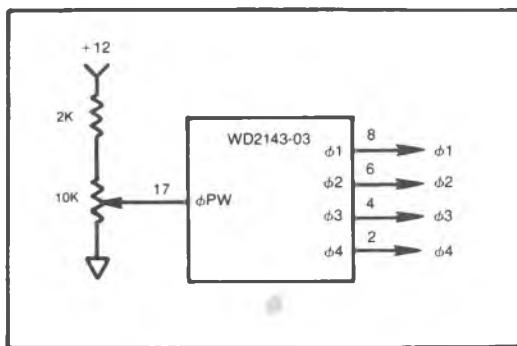


Figure 4 EQUAL PULSE WIDTH OUTPUTS

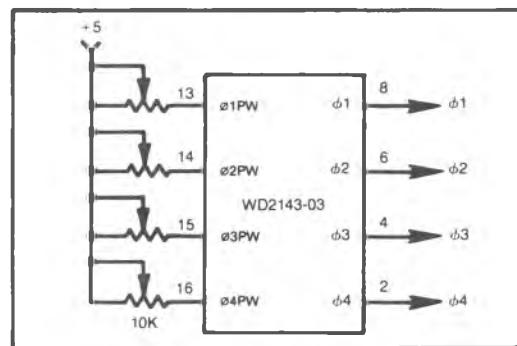


Figure 5 INDIVIDUAL PULSE WIDTH OUTPUTS

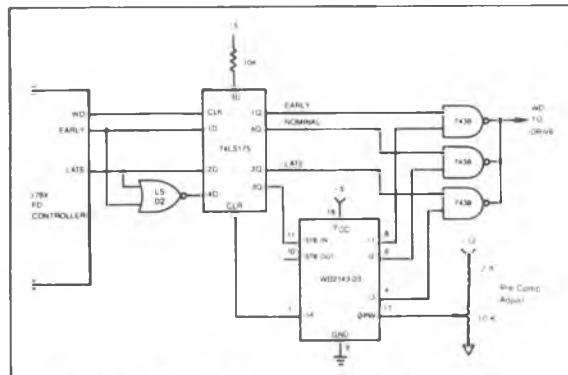


Figure 6 WRITE PRECOMP FOR FLOPPY DISK

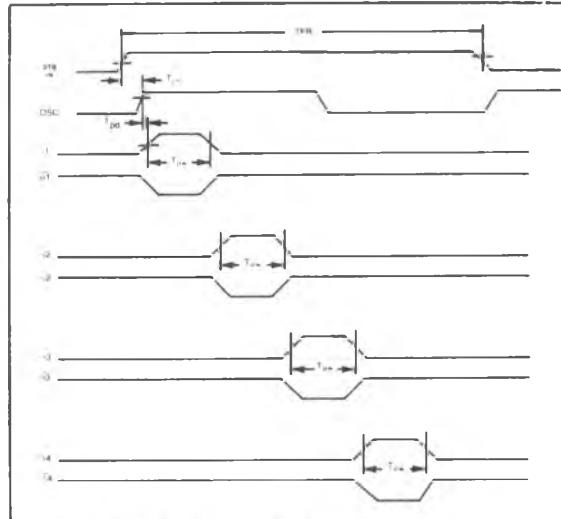


Figure 7 WD2143-03 TIMING DIAGRAM

SPECIFICATIONS**Absolute Maximum Ratings**

Operating Temperature	0° to + 70° C
Voltage on any pin with respect to Ground*	-0.5 to +7V
Power Dissipation	1 Watt
Storage Temperature	plastic -55° to +125° C ceramic -65° to +150°C

Note: Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to the DC electrical characteristics specified.

*Pin 17 = -0.5V to +12V. Increasing voltage on Pin 17 will decrease T_{pw} .

DC ELECTRICAL CHARACTERISTICS

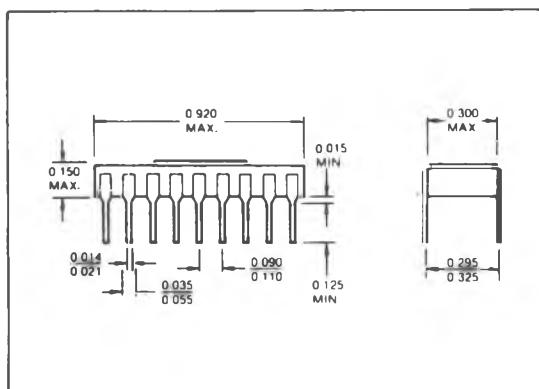
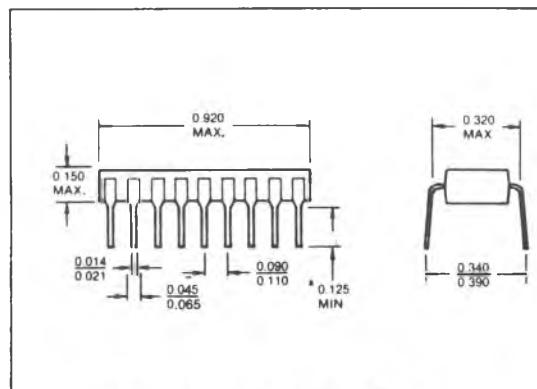
$V_{CC} = 5V \pm 5\%$, GND = OV, $T_A = 0^\circ$ to $70^\circ C$.

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	CONDITIONS
V_{OL}	TTL low level output		0.4	V	$I_{OL} = 1.6$ ma.
V_{OH}	TTL high level output	2.4		V	$I_{OH} = -100$ ua.
V_{IL}	STB in low voltage		0.8	V	
V_{IH}	STB in high voltage	2.4		V	
I_{CC}	Supply Current		80	ma	All outputs open

Table 2 DC ELECTRICAL CHARACTERISTICS

SWITCHING CHARACTERISTICS $V_{CC} = 5V \pm 5\%$, GND = 0V $T_A = 0^\circ$ to 70° C

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	CONDITIONS
T_{cd}	STB IN to OSC out (\uparrow)		70	NS	
T_{pd}	STB OUT to $\phi 1$		70	NS	
T_{pw}	Pulse Width (any output)	100	300	NS	$CL = 30\text{pf}$
T_{pr}	Rise Time (any output)		30	NS	$CL = 30\text{ pf}$
T_{pf}	Fall Time (any output)		25	NS	$CL = 30\text{ pf}$
T_{FR}	STROBE Frequency		2.5	MHz	combined $T_{pw} = 400\text{ NS}$.
T_{dpw}	Pulse Width Differential		10	%	100–300 NS.

Table 3 SWITCHING CHARACTERISTICSNOTE: T_{pw} measured at 50% V_{OH} Point; $V_{OL} = 0.8V$, $V_{OH} = 2.0V$.**WD2143L-03 CERAMIC PACKAGE****WD2143M-03 PLASTIC PACKAGE**

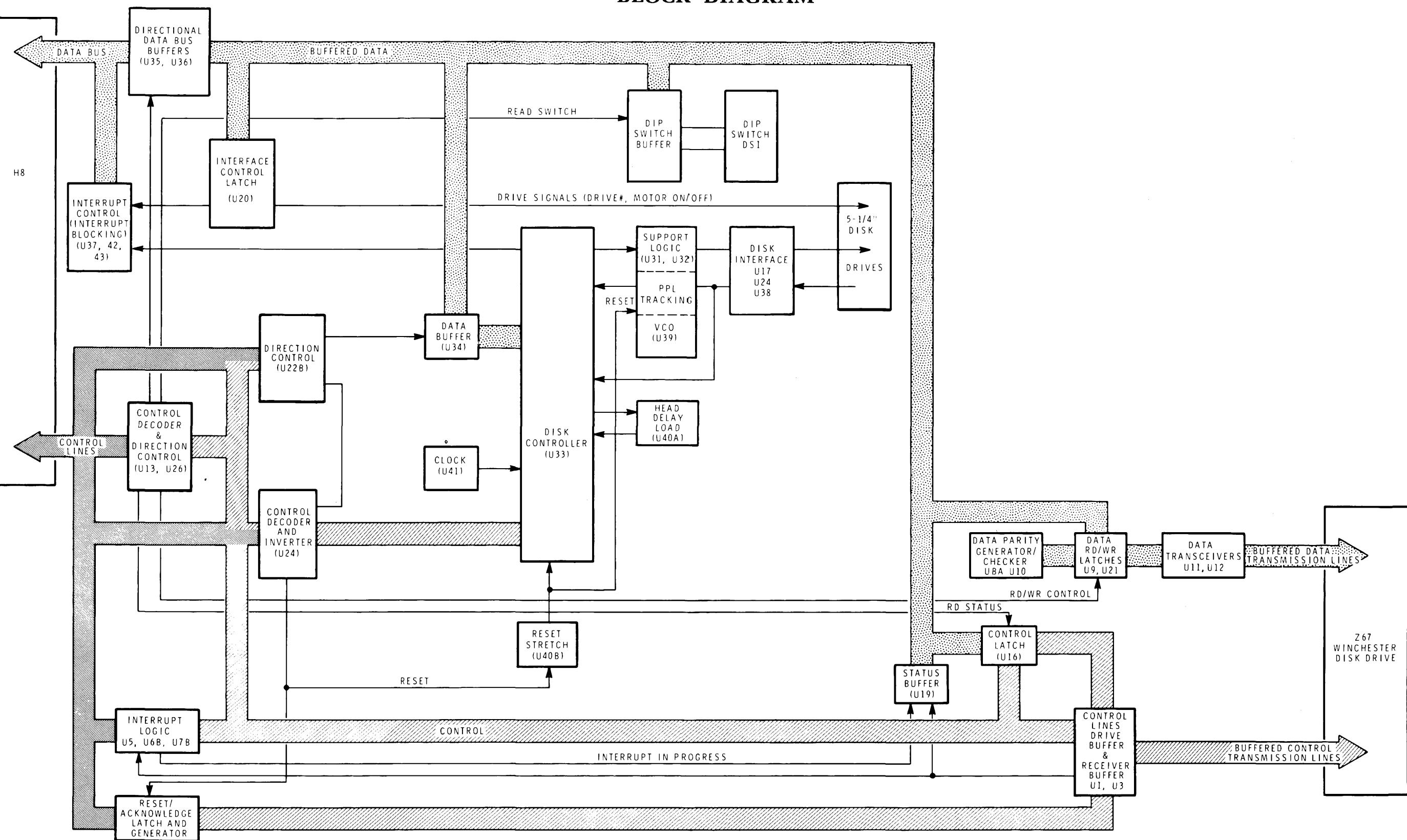
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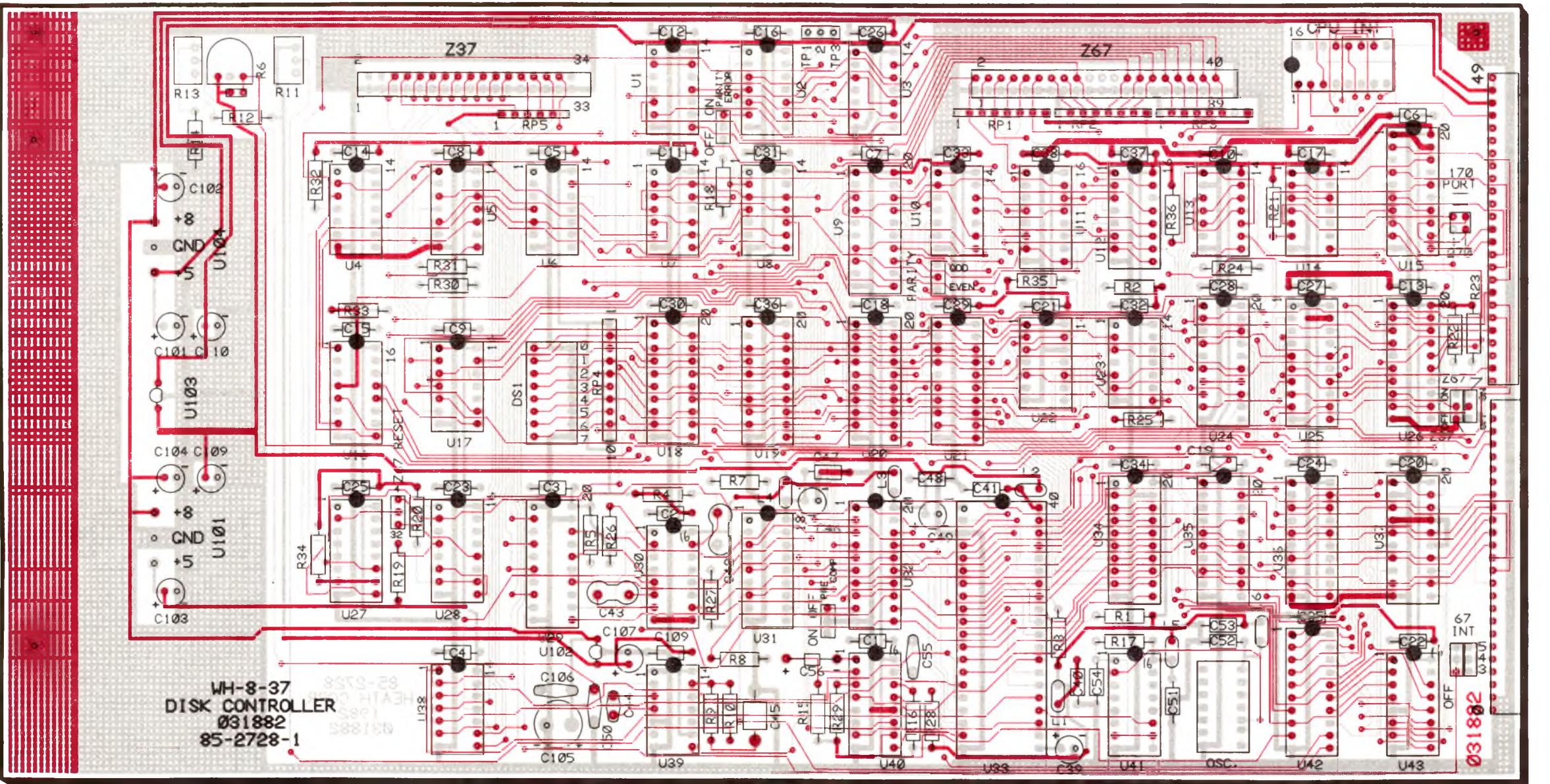
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BLOCK DIAGRAM



CIRCUIT BOARD X-RAY VIEW



YOUR HEATH FACTORY ASSEMBLED COMPUTER PRODUCT (90-DAY) LIMITED WARRANTY

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HEATH'S RESPONSIBILITY

PARTS — Replacement for factory defective parts will be supplied free for 90 days from date of purchase. Replacement parts are warranted for the remaining portion of the original warranty period. You can obtain warranty parts direct from Heath Company by writing or telephoning us at (616) 982-3571. And we will pay the shipping charges to get those parts to you . . . anywhere in the world.

SERVICE LABOR — For a period of 90 days from the date of purchase, any malfunction caused by factory defective parts or workmanship will be corrected at no charge to you. You must deliver the unit at your expense to the Heath factory, any Heathkit Electronic Center (units of Veritechnology Electronics Corporation) or any of our authorized overseas distributors.

TECHNICAL CONSULTATION — You will receive free consultation on any problem you might encounter in the use of your Heath product. Just drop us a line or give us a call. Sorry, we cannot accept collect calls.

NOT COVERED — Repair service, adjustments and calibration due to misuse, abuse or negligence are not covered by this warranty. Unauthorized modification of the product or of any furnished component will void this warranty in its entirety. This warranty does not include reimbursement for inconvenience, installation, set-up time, loss of use, or unauthorized service.

This warranty covers only Heath factory assembled computer products and is not extended to other equipment and components that a customer uses in conjunction with our products.

SUCH REPAIR AND/OR PARTS REPLACEMENT SHALL BE THE SOLE REMEDY OF THE CUSTOMER AND THERE SHALL BE NO LIABILITY ON THE PART OF HEATH FOR ANY SPECIAL, INDIRECT, INCIDENTAL OR CONSEQUENTIAL DAMAGES, INCLUDING BUT NOT LIMITED TO ANY LOSS OF BUSINESS OR PROFITS, WHETHER OR NOT FORESEEABLE.

Some states do not allow the exclusion or limitation of incidental or consequential damages, so the above limitation or exclusion may not apply to you.

OWNER'S RESPONSIBILITY

EFFECTIVE WARRANTY DATE — Warranty begins on the date of first consumer purchase. You must supply a copy of your proof of purchase when you request warranty service or parts.

OPERATING MANUAL — Read your operating instructions carefully so that you will fully understand the proper operation and function of your unit.

ACCESSORY EQUIPMENT — Performance malfunctions involving connections to (or interfacing with) other non-Heath equipment are not covered by this warranty and are the owner's responsibility.

SHIPPING UNITS — Follow the packing instructions published in your manual. Damage due to inadequate packing cannot be repaired under warranty.

If you are not satisfied with our service (warranty or otherwise) or our products, write directly to our Director of Customer Service, Heath Company, Benton Harbor MI 49022. He will make certain your problems receive immediate, personal attention.

