

8080A & 8085A

MICROPROCESSOR INSTANT REFERENCE CARD

LSD → HEX to Instruction Conversion

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0	NOP	LXI	STAX	INX	INR	DCR	MVI	RCL		DAD	LDAX	DCX	INR	DCR	MVI	RRC	
1		LXI	STAX	INX	INR	DCR	MVI	RAL		DAD	LDAX	DCX	INR	DCR	MVI	RAR	
2	RIM	LXI	SHLD	INX	INR	DCR	MVI	DAA		DAD	LHLD	DCX	INR	DCR	MVI	CMA	
3	SIM	LXI	SP	STA	INX	SP	M	DCR	MVI	STC		DAD	LDA	DCX	INR	DCR	CMD
4	MOV	B.C	MOV	MOV	MOV	B.H	MOV	B.L	MOV	MOV	MOV	MOV	C.C	MOV	MOV	MOV	
5	MOV	D.B	MOV	MOV	MOV	D.H	MOV	D.M	MOV	MOV	MOV	MOV	E.C	MOV	MOV	MOV	
6	MOV	H.B	MOV	MOV	MOV	H.C	MOV	H.D	MOV	MOV	MOV	MOV	L.C	MOV	MOV	MOV	
7	MOV	M.B	MOV	MOV	MOV	M.C	MOV	M.D	HLT	MOV	MOV	MOV	A.C	MOV	MOV	MOV	
8	ADD	B.C	ADD	ADD	ADD	E.H	ADD	L.M	ADD	ADC	ADC	ADC	D.E	ADC	ADC	ADC	
9	SUB	B.C	SUB	SUB	SUB	E.H	SUB	L.M	SUB	SBB	SBB	SBB	C.D	SBB	SBB	SBB	
A	ANA	A.C	ANA	ANA	ANA	H.A	ANA	M.A	XRA	B.C	XRA	XRA	C.D	XRA	XRA	XRA	
B	ORA	B.C	ORA	ORA	ORA	H.E	ORA	L.M	ORA	CMP	CMP	CMP	D.E	CMP	CMP	CMP	
C	RNZ	POP	B	JNZ	JMP	CNZ	PUSH	B	ADI	RST	0	RZ	RET	JZ		CZ	
D	RNC	POP	D	JNC	OUT	CNC	PUSH	D	SUI	RST	2	RC		JC	IN	CC	
E	RPO	POP	H	JPO	XTHL	CPO	PUSH	H	ANI	RST	4	RPE	PCHL	JPE	XCHG	CPE	
F	RP	POP	PSW	JP	DI	CP	PUSH	PSW	ORI	RST	6	RM	SPHL	JM	EI	CM	

ASCII Character Set

MSD	0	1	2	3	4	5	6	7
LSD	000	001	010	011	100	101	110	111
0	0000	NUL	DLE	SP	0	@	P	'
1	0001	SOH	DC1	!	1	A	Q	a
2	0010	STX	DC2	"	2	B	R	r
3	0011	ETX	DC3	#	3	C	S	s
4	0100	EOT	DC4	\$	4	D	T	t
5	0101	ENQ	NAK	%	5	E	U	u
6	0110	ACK	SYN	&	6	F	V	v
7	0111	BEL	ETB	'	7	G	W	w
8	1000	BS	CAN	(8	H	X	x
9	1001	HT	EM)	9	I	Y	y
A	1010	LF	SUB	*	:	J	Z	z
B	1011	VT	ESC	+	:	K	[{
C	1100	FF	FS	'	<	L	\	I
D	1101	CR	GS	-	=	M]	m
E	1110	SO	RS	.	>	N	!	n
F	1111	SI	US	/	?	O	-	DEL

8085A RIM & SIM bits

MSB	SID	17.5	16.5	15.5	IE	M7.5	M6.5	M5.5	
LSB	SIM	SOD	SOE	-	R7.5	MSE	M7.5	M6.5	M5.5

8080 Timing Example

Using 8224 clock chip:

XTAL = 18 mhz/9 = 2 mhz
= 500 ns = 1 state.
ADD A = 4 states = 2 us

8085 Timing Example

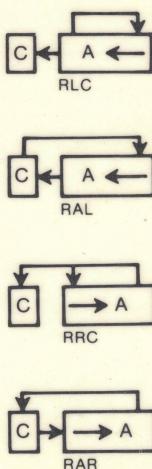
XTAL = 6 mhz/2 = 3 mhz
= 333 ns = 1 state.
ADD A = 4 states = 1.333 us

DAA (Decimal Adjust Accumulator)

The 8 bits in the acc are adjusted to form 2 BCD digits by:

- If the low 4 bits are > 9 or if the AC flag = 1, 6 is added to the acc.
- If the high 4 bits are now > 9, or if CY = 1, 6 is added to the high 4 bits.

Rotate Instructions



Status Flags

MSB	S	Z	-AC-	-P-	C	LSB
-----	---	---	------	-----	---	-----

S = sign (MSB) of result
Z = 1 = result is 0
AC = aux C from bit 3
P = 1 = parity is even
C = 1 = carry (also CY)

Flag Codes

Circled letters in Instruction Set indicate which flags are effected as follows:

- (A) All
- (B) All But C
- (C) Just C
- (D) Depends on which MPU:
8080: All, C=0, AC=OR of bits 3
8085: All, C=0, AC=1
- (E) All, C=0, AC=0
- (N) None

8085A Pins

X ₁	1	40	V _{CC}
X ₂	2	39	HOLD
RESET OUT	3	38	HLDA
SOD	4	37	CLK (OUT)
SID	5	36	RESET IN
TRAP	6	35	READY
RST 7.5	7	34	I/O/M
RST 6.5	8	33	S ₁
RST 5.5	9	32	RD
INTR	10	31	WR
INTA	11	30	ALE
AD ₀	12	29	S ₀
AD ₁	13	28	A ₁₅
AD ₂	14	27	A ₁₄
AD ₃	15	26	A ₁₃
AD ₄	16	25	A ₁₂
AD ₅	17	24	A ₁₁
AD ₆	18	23	A ₁₀
AD ₇	19	22	A ₉
V _{SS}	20	21	A ₈

8080A Pins

A ₁₀	1	40	A ₁₁
D ₄	2	39	A ₁₄
D ₅	3	38	A ₁₃
D ₆	4	37	A ₁₂
D ₇	5	36	A ₁₅
D ₃	6	35	A ₉
D ₂	7	34	A ₈
D ₁	8	33	A ₇
D ₀	9	32	A ₆
-5V	10	31	A ₅
RESET	11	30	A ₄
HOLD	12	29	A ₃
INT	13	28	A ₂
INTA	14	27	A ₁
DBIN	15	26	A ₀
WR	16	25	WAIT
SYNC	17	24	READY
+5V	18	23	
	19	22	
	20	21	

Registers

A (Acc.) (8)	Flags (8)
B (8)	C (8)
D (8)	E (8)
H (8)	L (8)
PC (Program Counter) (16)	
SP (Stack Pointer) (16)	

Note: When BC, DE, HL used as pairs, B,D,H, are high order.

8085 Interrupts

Name	Adr	Type (starting with highest priority)
TRAP	24H	Rising edge & high level till sampled
RST 7.5	3CH	Rising edge (latched)
RST 6.5	34H	
RST 5.5	2CH	High level till sampled
INTR	---	

Unsigned Comparisons

example: CMP B

A < B	JC YES
A ≤ B	JC YES ①
A = B	JZ YES
A ≠ B	JNZ YES
A ≥ B	JNC YES
A > B	JC *+6 ①

YES represents label for code to be executed if condition is true. Internally, A-B is computed to determine flags as for 'SUB B'.

① Requires both instructions.

Miscellaneous

The 2 byte addresses in code, stack, and data areas are stored low byte followed by high byte. Thus, in hex, JMP 1234H is: C3 34 12.

SP points to used byte at top of stack. Stack push decrements SP by 2. High byte of pair is pushed first.

This card is based on specifications from Intel®.

Abbreviations

aa	= a 2 byte address
v	= a 1 byte value
vv	= a 2 byte value
M	= Memory location that reg pair H&L points to
S&F	= States and Flag Codes
LOC	= Location
MSE	= Mask Set Enable
PSW	= Program Status Word (Acc & Flags)
SID	= Serial Input Data
SOD	= Serial Output Data
SOE	= Serial Output Enable
	See also: "Registers" and "Status Flags"

INSTRUCTION SET

INSTRUCTION	OCT	HEX	S&F	DESCRIPTION
ADC A	217	8F	4	Double A with carry (shift left with carry)
ADC B	210	88		Add B and carry to A
ADC C	211	89		Add C and carry to A
ADC D	212	8A		Add D and carry to A
ADC E	213	8B		Add E and carry to A
ADC H	214	8C		Add H and carry to A
ADC L	215	8D	(A)	Add L and carry to A
ADC M	216	8E	7	(A) Add LOC (H&L) and carry to A
ACI v	316	CE	7	(A) Add v and carry to A
ADD A	207	B7	4	Double A (shift A left)
ADD B	200	80		Add B to A
ADD C	201	81		Add C to A
ADD D	202	82		Add D to A
ADD E	203	83		Add E to A
ADD H	204	84		Add H to A
ADD L	205	85	(A)	Add L to A
ADD M	206	86	7	(A) Add LOC(H&L) to A
ADI v	306	C6	7	(A) Add v to A
ANA A	247	A7	4	Test A and clear carry AND B to A
ANA B	240	A0		AND C to A
ANA C	241	A1		AND D to A
ANA D	242	A2		AND E to A
ANA E	243	A3		AND H to A
ANA H	244	A4		AND L to A
ANA M	246	A6	7	(D) AND LOC(H&L) to A
ANI v	346	E6	7	(D) AND v to A
CALL aa	315	CC	17-18 (N)	Call subroutine aa
CZ aa	314	CC	11/17	If zero CALL
CNZ aa	304	C4		If not zero CALL
CP aa	364	F4		If plus CALL
CM aa	374	FC	9/18	If minus CALL
CC aa	334	DC		If carry CALL
CNC aa	324	D4		If no carry CALL
CPE aa	354	EC		If even parity CALL
CPO aa	344	E4		If odd parity CALL
CMA	057	2F	4	(N) Complement A (1's comp)
CMC	077	3F	4	(C) Complement carry
CMP A	277	BF	4	Set zero flag
CMP B	270	B8		Compare A with B
CMP C	271	B9		Compare A with C
CMP D	272	BA		Compare A with D
CMP E	273	BB		Compare A with E
CMP H	274	BC		Compare A with H
CMP L	275	BD	(A)	Compare A with L
CMP M	276	BE	7	(A) Compare A with LOC(H&L)
CPI v	376	FE	7	(A) Compare A with v
DAA	047	27	4	(A) Decimal adjust A
DAD B	011	09	10	Add B&C to H&L
DAD D	031	19		Add D&E to H&L
DAD H	051	29		Double H&L (shift H&L left)
DAD SP	071	39	(C)	Add SP to H&L
DCR A	075	3D	5-4	Decrement A
DCR B	005	05		Decrement B
DCR C	015	0D		Decrement C
DCR D	025	15		Decrement D
DCR E	035	1D		Decrement E
DCR H	045	25		Decrement H
DCR L	055	2D	(B)	Decrement L
DCR M	065	35	10	(B) Decrement LOC(H&L)
DCX B	013	0B	5-6	Decrement B&C
DCX D	033	1B		Decrement D&E
DCX H	053	2B		Decrement H&L
DCX SP	073	3B	(N)	Decrement SP
DI	363	F3	4	(N) Disable interrupts
EI	373	FB		Enable interrupts
HLT	166	76	7-5 (N)	Halt until interrupt
IN v	333	DB	10	(N) Input from device v to A
INR A	074	3C	5-4	Increment A
INR B	004	04		Increment B
INR C	014	0C		Increment C
INR D	024	14		Increment D
INR E	034	1C		Increment E
INR H	044	24		Increment H
INR L	054	2C	(B)	Increment L
INR M	064	34	10	(B) Increment LOC(H&L)
INX B	003	03	5-6	Increment B&C
INX D	023	13		Increment D&E
INX H	043	23		Increment H&L
INX SP	063	33	(N)	Increment SP
JMP aa	303	C3	10	(N) Jump to LOC aa
JZ aa	312	CA	10	If zero JMP
JNZ aa	302	C2	10 - 7/10	If not zero JMP
JP aa	362	F2		If plus JMP
JM aa	372	FA		If minus JMP
JC aa	332	DA		If carry JMP
JNC aa	322	D2		If no carry JMP
JPE aa	352	EA		If even parity JMP
JPO aa	342	E2		If odd parity JMP

INSTRUCTION	OCT	HEX	S&F	DESCRIPTION
LDA aa	072	3A	13	(N) Load A from LOC aa
LDAX B	012	0A	7	Load A from LOC(B&C)
LDAX D	032	1A	(N)	Load A from LOC(D&E)
LHLD aa	052	2A	16	(N) Load H&L from aa & next
LXI B, vv	001	01	10	Load B with vv
LXI D, vv	021	11		Load D&E with vv
LXI H, vv	041	21		Load H&L with vv
LXI SP, vv	061	31	(N)	Load SP with vv
MOV A, B	170	78	5-4	Move B to A
MOV A, C	171	79		Move C to A
MOV A, D	172	7A		Move D to A
MOV A, E	173	7B		Move E to A
MOV A, H	174	7C		Move H to A
MOV A, L	175	7D	(N)	Move L to A
MOV A, M	176	7E	7	(N) Move LOC(H&L) to A
MOV B, A	107	47	5-4	Move A to B
MOV B, C	101	41		Move C to B
MOV B, D	102	42		Move D to B
MOV B, E	103	43		Move E to B
MOV B, H	104	44		Move H to B
MOV B, L	105	45	(N)	Move L to B
MOV B, M	106	46	7	(N) Move LOC(H&L) to B
MOV C, A	117	4F	5-4	Move A to C
MOV C, B	110	48		Move B to C
MOV C, D	112	4A		Move D to C
MOV C, E	113	4B		Move E to C
MOV C, H	114	4C		Move H to C
MOV C, L	115	4D	(N)	Move L to C
MOV C, M	116	4E	7	(N) Move LOC(H&L) to C
MOV D, A	127	57	5-4	Move A to D
MOV D, B	120	50		Move B to D
MOV D, C	121	51		Move C to D
MOV D, E	123	53		Move E to D
MOV D, H	124	54		Move H to D
MOV D, L	125	55	(N)	Move L to D
MOV D, M	126	56	7	(N) Move LOC(H&L) to D
MOV E, A	137	5F	5-4	Move A to E
MOV E, B	130	58		Move B to E
MOV E, C	131	59		Move C to E
MOV E, D	132	5A		Move D to E
MOV E, H	134	5C		Move H to E
MOV E, L	135	5D	(N)	Move L to E
MOV E, M	136	5E	7	(N) Move LOC(H&L) to E
MOV H, A	147	67	5-4	Move A to H
MOV H, B	140	60		Move B to H
MOV H, C	141	61		Move C to H
MOV H, D	142	62		Move D to H
MOV H, E	143	63		Move E to H
MOV H, L	145	65	(N)	Move L to H
MOV H, M	146	66	7	(N) Move LOC(H&L) to H
MOV I, A	157	6F	5-4	Move A to I
MOV I, B	150	68		Move B to I
MOV I, C	151	69		Move C to I
MOV I, D	152	6A		Move D to I
MOV I, E	153	6B		Move E to I
MOV I, H	154	6C	(N)	Move H to I
MOV I, M	156	6E	7	(N) Move LOC(H&L) to I
MOV J, A	167	77	7	Move A to LOC(H&L)
MOV J, B	160	70		Move B to LOC(H&L)
MOV J, C	161	71		Move C to LOC(H&L)
MOV J, D	162	72		Move D to LOC(H&L)
MOV J, E	163	73		Move E to LOC(H&L)
MOV J, H	164	74		Move H to LOC(H&L)
MOV J, L	165	75	(N)	Move L to LOC(H&L)
MVI A, v	076	3E	7	Move v to A
MVI B, v	006	06		Move v to B
MVI C, v	016	0E		Move v to C
MVI D, v	026	16		Move v to D
MVI E, v	036	1E		Move v to E
MVI H, v	046	26		Move v to H
MVI L, v	056	2E	(N)	Move v to L
MVI M, v	066	36	10	(N) Move v to LOC(H&L)
NOP	000	00	4	(N) No operation
ORA A	267	B7	4	Test A and clear carry OR B to A
ORA B	260	B0		OR C to A
ORA C	261	B1		OR D to A
ORA D	262	B2		OR E to A
ORA E	263	B3		OR H to A
ORA H	264	B4		OR L to A
ORA L	265	B5	(E)	Exclusive OR L to A
ORA M	266	B6	7	(E) OR LOC(H&L) to A
ORI v	366	F6	7	(E) OR v to A
OUT v	323	D3	10	(N) Output A to device v
PCHL	351	E9	5-6	(N) Jump to LOC(H&L)
POP B	301	C1	10	Pop B&C from stack
POP D	321	D1		Pop D&E from stack
POP H	341	E1		Pop H&L from stack
POP PSW	361	F1	10	(A) Pop A and flags from stack

INSTRUCTION	OCT	HEX	S&F	DESCRIPTION
PUSH B	305	C5	11-12	Push B&C onto stack
PUSH D	325	D5		Push D&E onto stack
PUSH H	345	E5		Push H&L onto stack
PUSH PSW	365	F5	(N)	Push A and flags onto stack
RAL	027	17	4	Rotate CY & A left
RAR	037	1F		Rotate CY & A right
RLC	007	07		Rotate A left and into carry
RRC	017	0F	(C)	Rotate A right and into carry
RIM (8085)	040	20	4	(N) Read interrupt mask
RET	311	C9	10	(N) Return from subroutine
RZ	310	C8	5-11	Call subroutine at 00H
RNZ	300	C0		Call subroutine at 08H
RP	360	F0		Call subroutine at 10H
RM	370	F8		Call subroutine at 18H
RC	330	D8		Call subroutine at 20H
RNC	320	D0		Call subroutine at 28H
RPE	350	E8		Call subroutine at 30H
RPO	340	E0	(N)	Call subroutine at 38H
RST 0	307	C7	11-12	Call subroutine at 00H
RST 1	317	CF		Call subroutine at 08H
RST 2	327	D7		Call subroutine at 10H
RST 3	337	DF		Call subroutine at 18H
RST 4	347	E7		Call subroutine at 20H
RST 5	357	EF		Call subroutine at 28H
RST 6	367	F7		Call subroutine at 30H
RST 7	377	FF	(N)	Call subroutine at 38H
SBB A	237	9F	4	Subtract B & CY from A
SBB B	230	98		Subtract C & CY from A
SBB C	231	99		Subtract D & CY from A
SBB D	232	9A		Subtract E & CY from A
SBB E	233	9B		Subtract F & CY from A
SBB H	234	9C		Subtract G & CY from A
SBB L	235	9D	(A)	Subtract L & CY from A
SBB M	236	9E	7	(A) Subtract LOC (H&L) & CY from A
SBI v	336	DE	7	(A) Subtract v and CY from A
SHLD aa	042	22	16	(N) Store H&L at aa & next
SIM (8085)	060	30	4	Set interrupt mask
SPHL	371	F9	5-6	(N) Load SP from H&L
STA aa	062	32	13	(N) Store A at LOC aa
STAX B	002	02	7	Store A at LOC(B&C)
STAX D	022	12	(N)	Store A at LOC(D&E)
STC	067	37	4	(C) Set carry (to 1)
SUB A	227	97	4	Clear A
SUB B	220	90		Subtract B from A
SUB C	221	91		Subtract C from A
SUB D	222	92		Subtract D from A
SUB E	223	93		Subtract E from A
SUB H	224	94		Subtract F from A
SUB L	225	95	(A)	Subtract L from A
SUB M	226	96	7	(A) Subtract LOC(H&L) from A
SUI v	326	D6	7	(A) Subtract v from A
XCHG	353	EB	4	(N) Exchange D&E with H&L
XRA A	257	AF	4	Clear A
XRA B	250	AB		Exclusive OR B to A
XRA C	251	A9		Exclusive OR C to A
XRA D	252	AA		Exclusive OR D to A
XRA E	253	AB		Exclusive OR E to A
XRA H	254	AC		Exclusive OR H to A
XRA L	255	AD	(E)	Exclusive OR L to A
XRA M	256	AE	7	(E) to A
XRI v	356	EE	7	(E) Exclusive OR v to A
XTHL	343	E3	18-16	(N) Exchange top of stack with H&L

EXAMPLES FROM S & F COLUMN

7	7 STATES FOR 8080 & 8085
5-4	5 STATES 8080; 4 STATES 8085
10-7/10	10 STATES 8080; 7 STATES FOR FAILURE.
	10 STATES FOR SUCCESS ON 8085

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MICRO CHART
AUTHOR:
JAMES D. LEWIS