

H/Z-100 COMPUTERS

SERVICE DATA MANUAL

585-18

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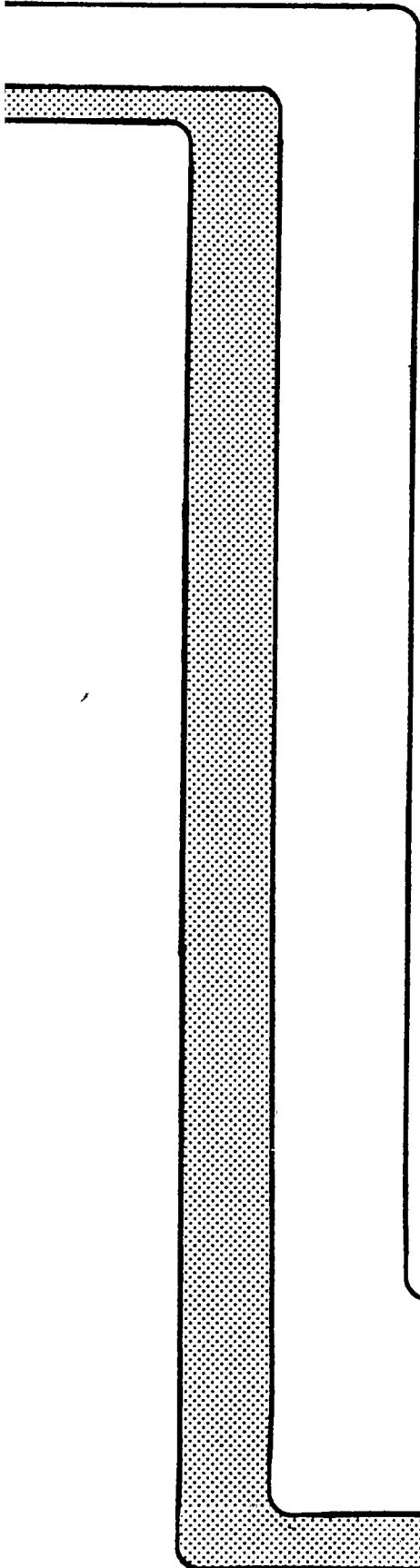


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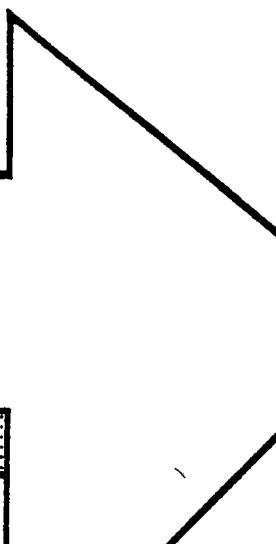
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INTRODUCTION



The H/Z-100 COMPUTER SERVICE DATA MANUAL (Blue Book) contains in-depth data about the new H/Z-100 Computers, both the All-In-One model and the Low-Profile model.

The information in this manual will help you efficiently troubleshoot and repair H/Z-100 Computers to either the module level or the component level.

There are thirteen sections in this manual. The first is a general introduction to the manual and an explanation of the model numbering system.

Section 2 introduces you to the Computer System and is presented in the familiar Blue Book format.

The following six sections, also laid out in the Blue Book format, contain detailed data on the:

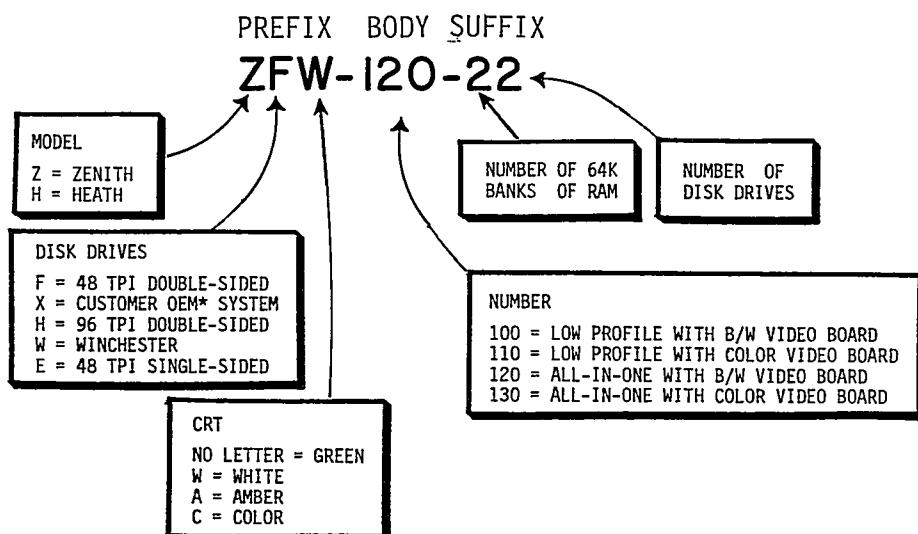
- Motherboard,
- Video Board,
- Disk Controller and Drives,
- Video Monitor,
- Keyboard, and
- Power Supply

The balance of the manual is set aside for your inclusion of material for Accessories, Service Bulletins, Data Sheets, and Diagnostics. Data on the S-100 bus has already been included in an Appendix section.

All thirteen sections are contained in an easy-to-use 3-ring binder...this will let you insert updates and new product information and will let you keep your H/Z-100 Computer Blue Book up to date.

And now for a look at the model number system...

Each model number lets you see at a glance the main features of that particular model. The illustration below shows what each portion of the model number means:



So, if the model number is ZF-120-22, it means:

Z a Zenith wired model,
 F with a 48 TPI,
 W a white CRT,
 -120 and it's an ALL-IN-ONE with a black and white video board
 -2 with two banks of 64K of RAM ($2 \times 64 = 128K$ RAM), and
 2 two disk drives!

A couple of things to remember...

Note that in the body (or number), "Color Video Board" refers to the ability of the video board to produce color--not the nature of any CRT. Also, in the suffix portion of the model number, characters are alphanumeric for OEM models (and stand for a specific OEM); for all other models, the characters are numeric.

Carefully read each section in this Blue Book. After doing so, you'll not only become an expert on the H/Z-100, you will also be able to quickly locate the exact information that you need to service the unit.

Before learning how each module works in the Computer, you should know how the H/Z-100 works as a complete system. To gain this understanding, begin by reading section 2, "System."

SERVICE MANUAL ADDENDUM

for

SM-Z-100



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INTRODUCTION

This service manual addendum provides disassembly instructions for the Winchester drive, data separator board, Z-217 Winchester controller card, and half-height drives.

Also provided is a replacement parts list, for the All-in-One model with a Winchester and a standard size drive, the All-in-One model with a Winchester and half-height drives, and the Low-Profile model with a Winchester and standard size drive.

The Z-217 Winchester controller card, data separator board, and Winchester drive provides 12 megabytes unformatted and 11 megabytes formatted of storage to the Z-100 Computer system. The Z-217 controller card resides in one of the S-100 card slots, and the data separator board is mounted on the Winchester drive. The Winchester drive is located in the front panel of the Computer.



DISASSEMBLY

CAUTION

The SHIP Utility allows you to place the heads of the Winchester system over a non-vital area of the disks. If the system is accidentally jarred during movement, damage will be limited to an area that is not used by the Computer. The floating head design of Winchester drives makes them very sensitive to physical shocks, which can damage the surface of the disks. Therefore, you should use this utility when ever you move, disassemble, or service the Winchester disk system. Refer to Page 3-1.

ALL-IN-ONE MODEL

Top Cover Removal (Refer to Figure 2-1.)

The top cover is secured to the cabinet base by two metal slide rails. To remove the top cover:

- Insert a screwdriver into the metal slides on both sides of the Computer.
- With the screwdriver, push the metal slide to the rear of the Computer about $1/4"$ to free the latches.
- When the latches are free, lift the top cover straight up.

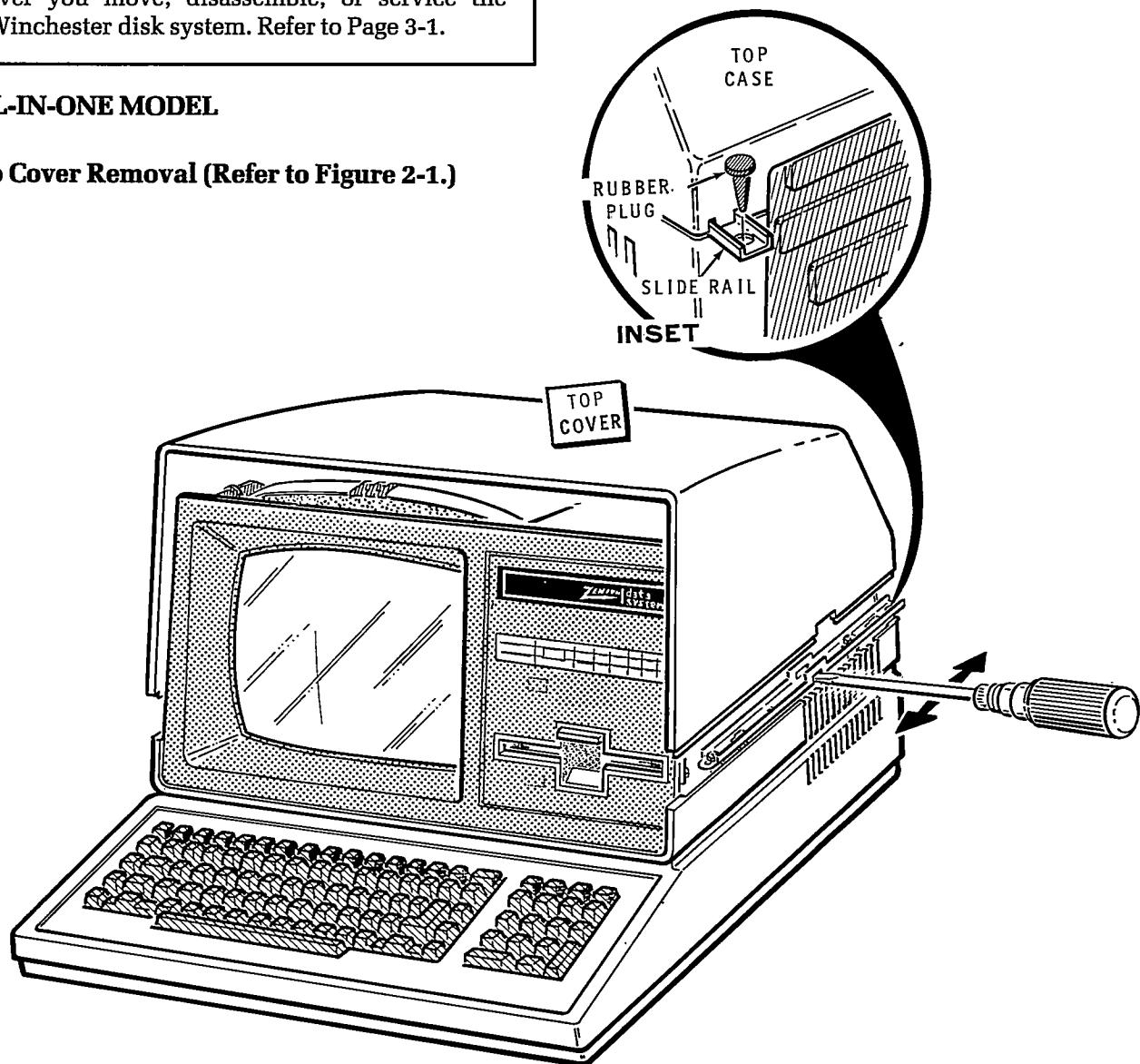


Figure 2-1
Top cover removal

CRT and Disk Drive Assembly Removal (Refer to Figure 2-2.)

BE SURE THE WINCHESTER HEADS ARE IN THE SHIP POSITION. Refer to Page 3-1.

To remove the CRT and disk drive assembly:

- Remove the top cover.
- Disconnect the floppy cable from P2 of the disk controller card.

- Disconnect cables to the Winchester drive and data separator board.
- Disconnect the power supply connector to each disk drive.
- Disconnect the connector from P1 on the video deflection board.
- Completely loosen the five screws that secure the assembly to the cabinet base (three on the right side(A), and two on the left side (B).

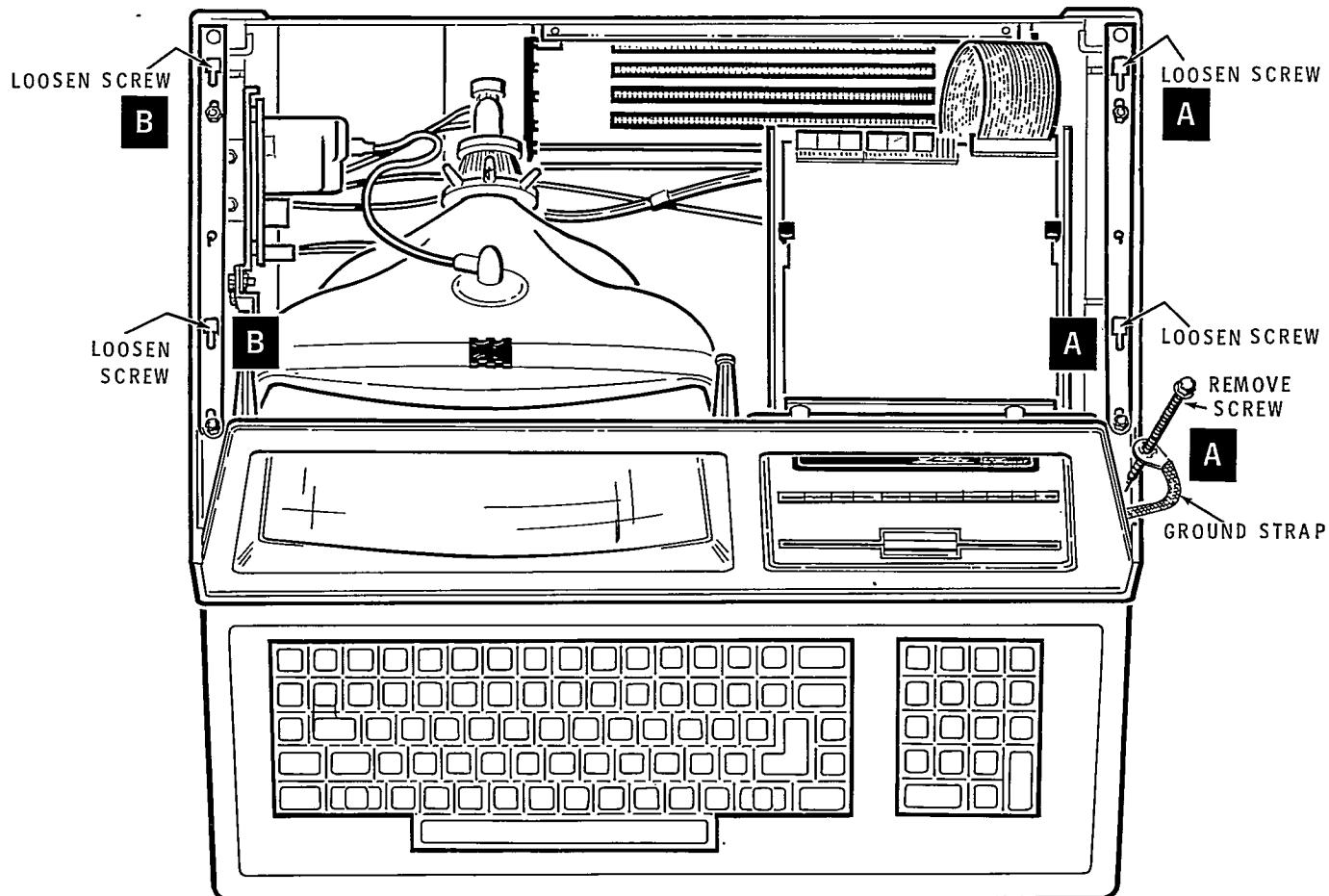


Figure 2-2
CRT and disk drive assembly removal

Winchester Drive Removal (Refer to Figure 2-3.)

BE SURE THE WINCHESTER HEADS ARE IN THE SHIP POSITION. Refer to Page 3-1.

To remove the drive:

- Remove the top cover.
- Remove the CRT and disk drive assembly.
- Disconnect cables from the Winchester drive.
- Remove the escutcheon.
- Remove the panel by removing three screws (A).
- Remove the four screws (B).
- Carefully lift out the Winchester drive.

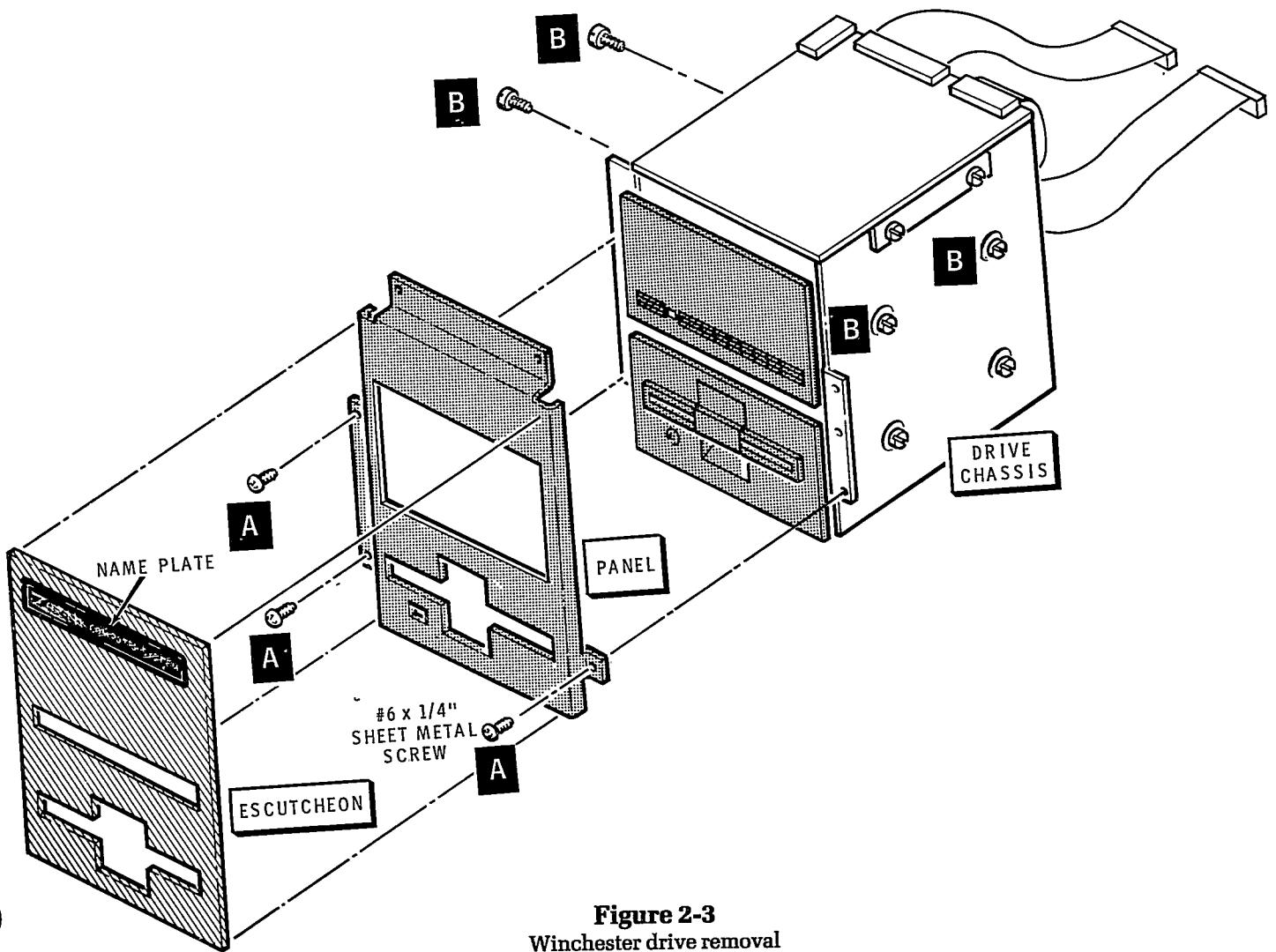


Figure 2-3
Winchester drive removal

Winchester Controller Card Removal (Refer to Figure 2-4.)

To remove the Winchester controller card:

- Remove the top cover.
- Remove cables 134-1279 and 134-1281 from the Winchester controller card.
- If necessary, remove cable 134-1264 from the floppy disk controller card.
- Remove P6, the power supply connector from the Winchester controller card.
- Lift up on the two card pullers (A) to remove the Winchester controller card.

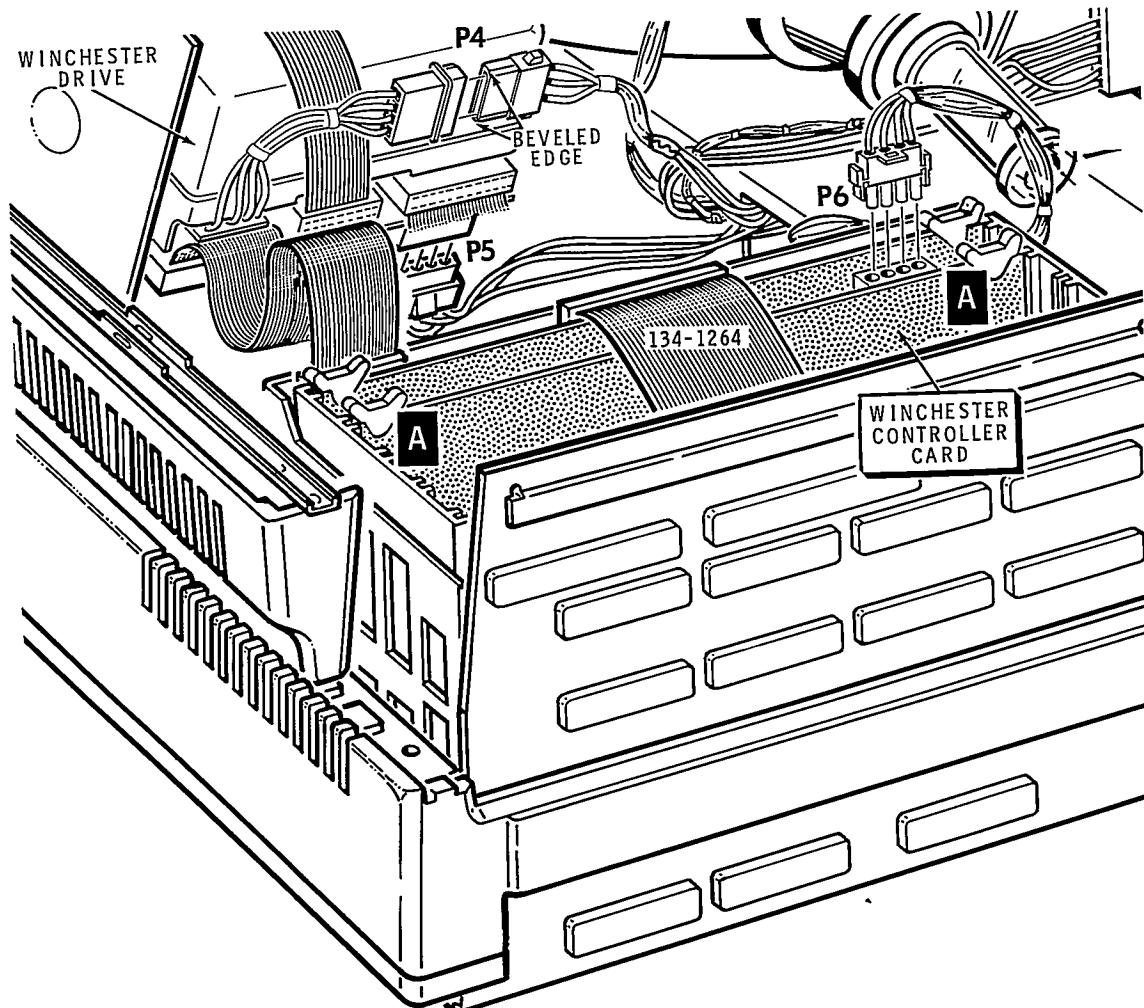


Figure 2-4
Winchester controller card removal

Data Separator Board Removal (Refer to Figure 2-5.)

BE SURE THE WINCHESTER HEADS ARE IN THE SHIP POSITION. Refer to Page 3-1.

To remove the data separator board:

- Remove the top cover.
- Remove cables 134-1280 and 134-1281 from the data separator board.
- Remove the power supply connector P3.
- Remove the four screws (A).
- Carefully lift out the data separator board.

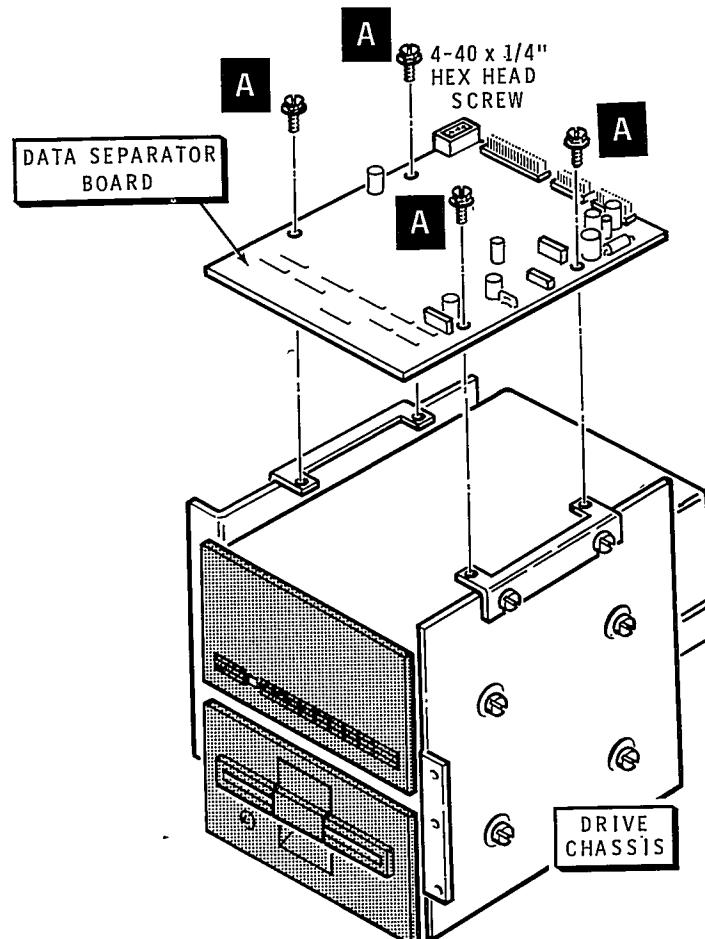


Figure 2-5
Data separator board removal

LOW-PROFILE MODEL

Top Cover Removal (Refer to Figure 2-6.)

The top cover is secured to the cabinet base by two metal slide rails. To remove the top cover:

- Pull out the two metal slide rails at the rear of the Computer about 1/4".
- When the metal rails free the latches, lift the top cover straight up.

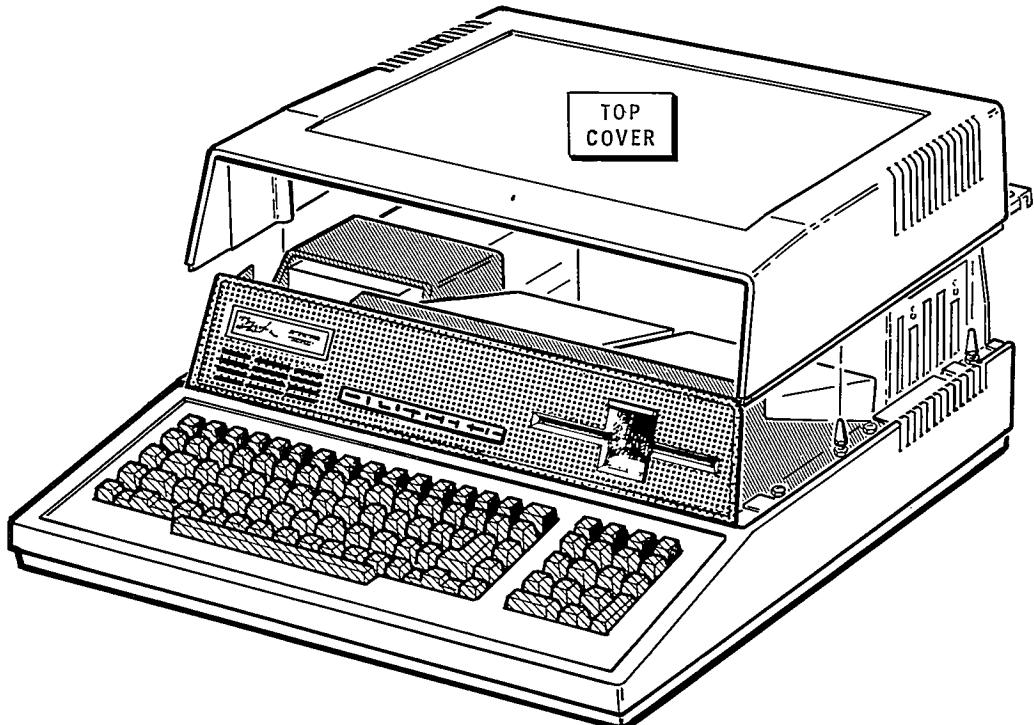


Figure 2-6
Top cover removal

Drive Assembly Removal (Refer to Figure 2-7.)

BE SURE THE WINCHESTER HEADS ARE IN THE SHIP POSITION. Refer to Page 3-1.

To remove the drive assembly:

- Remove the top cover.
- Remove the four screws (A) and the two threaded locking pins (B) that secure the drive assembly to the cabinet base.
- Disconnect the floppy cable from P2 of the disk controller card.
- Disconnect the two floppy cables going to the Winchester controller card.
- Lift the drive assembly up and to the left.
- Disconnect the power supply connector to each drive.

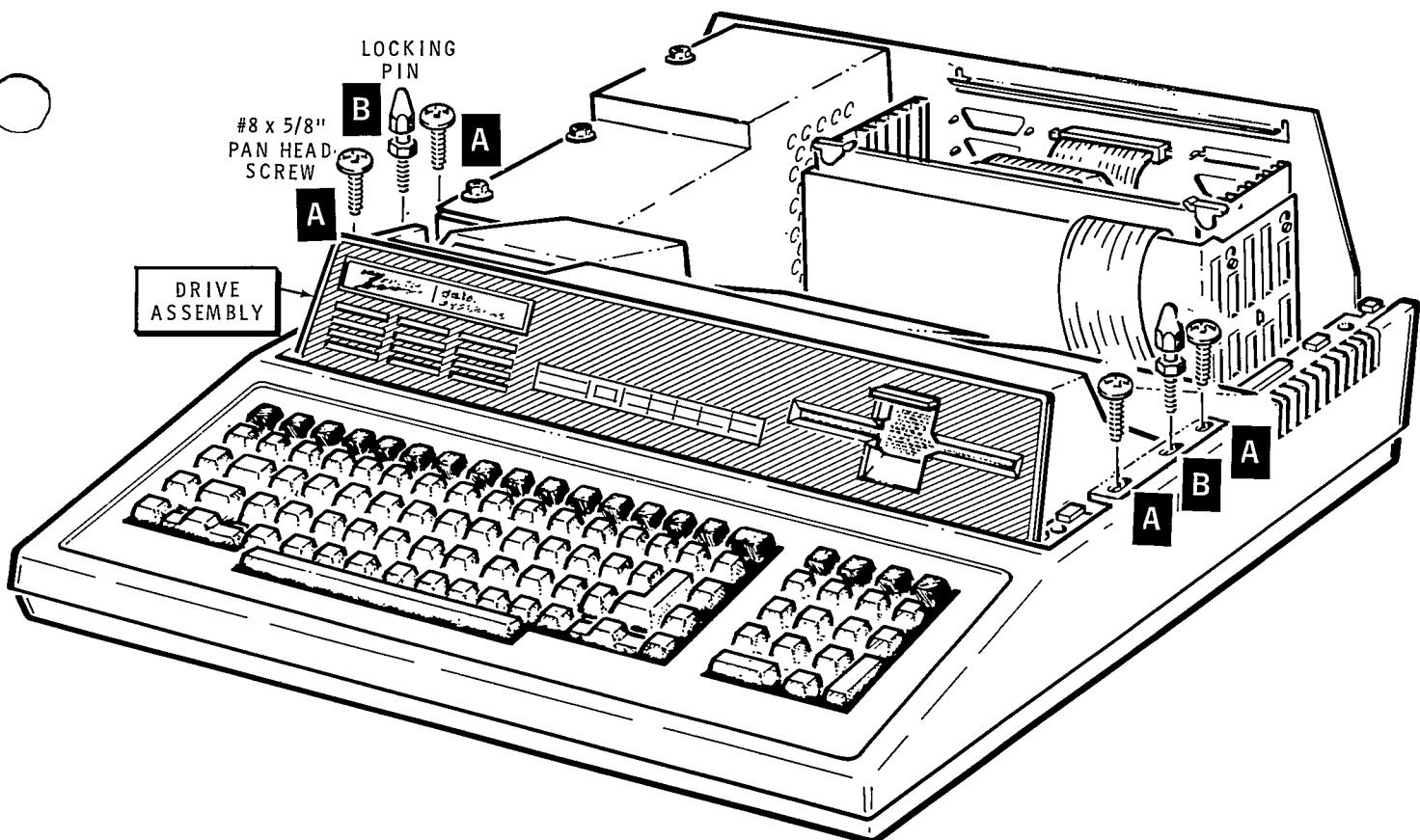


Figure 2-7
Drive assembly removal

Winchester Drive Removal (Refer to Figure 2-8.)

BE SURE THE WINCHESTER HEADS ARE IN THE SHIP POSITION. Refer to Page 3-1.

To remove the Winchester drive:

- Remove the top cover.
- Remove the drive assembly.
- Disconnect cables to the Winchester drive.
- Remove the four screws (A) from the bottom of the drive shelf.
- Remove the data separator board by removing the four screws (B).
- Carefully pull off the escutcheon from the front of the drive shelf.
- Carefully pull the Winchester Drive out from the front of the drive shelf.

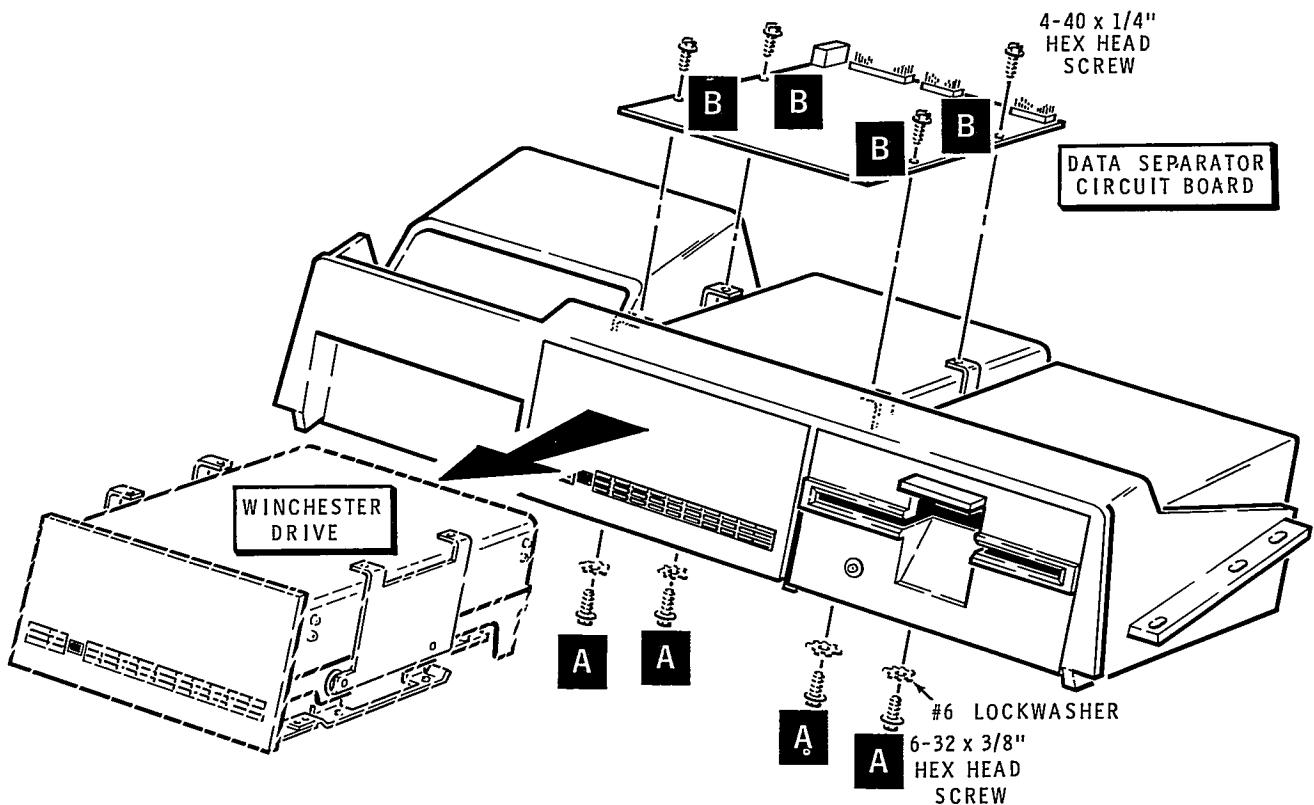


Figure 2-8
Winchester drive removal

CRT and Disk Drive Assembly Removal (Refer to Figure 2-12.)

BE SURE THE WINCHESTER HEADS ARE IN THE SHIP POSITION. Refer to Page 3-1.

To remove the CRT and disk drive assembly:

- Remove the top cover.
- Disconnect the floppy cable from P2 of the disk controller board.
- Disconnect the power supply connector from each drive.

- Disconnect the connector from P1 on the video deflection board.
- Disconnect the floppy cable from the Winchester drive to the Winchester controller card.
- Completely loosen the four screws (A), but do not remove them. Remove screw (B).
- Carefully remove the CRT and disk drive assembly.

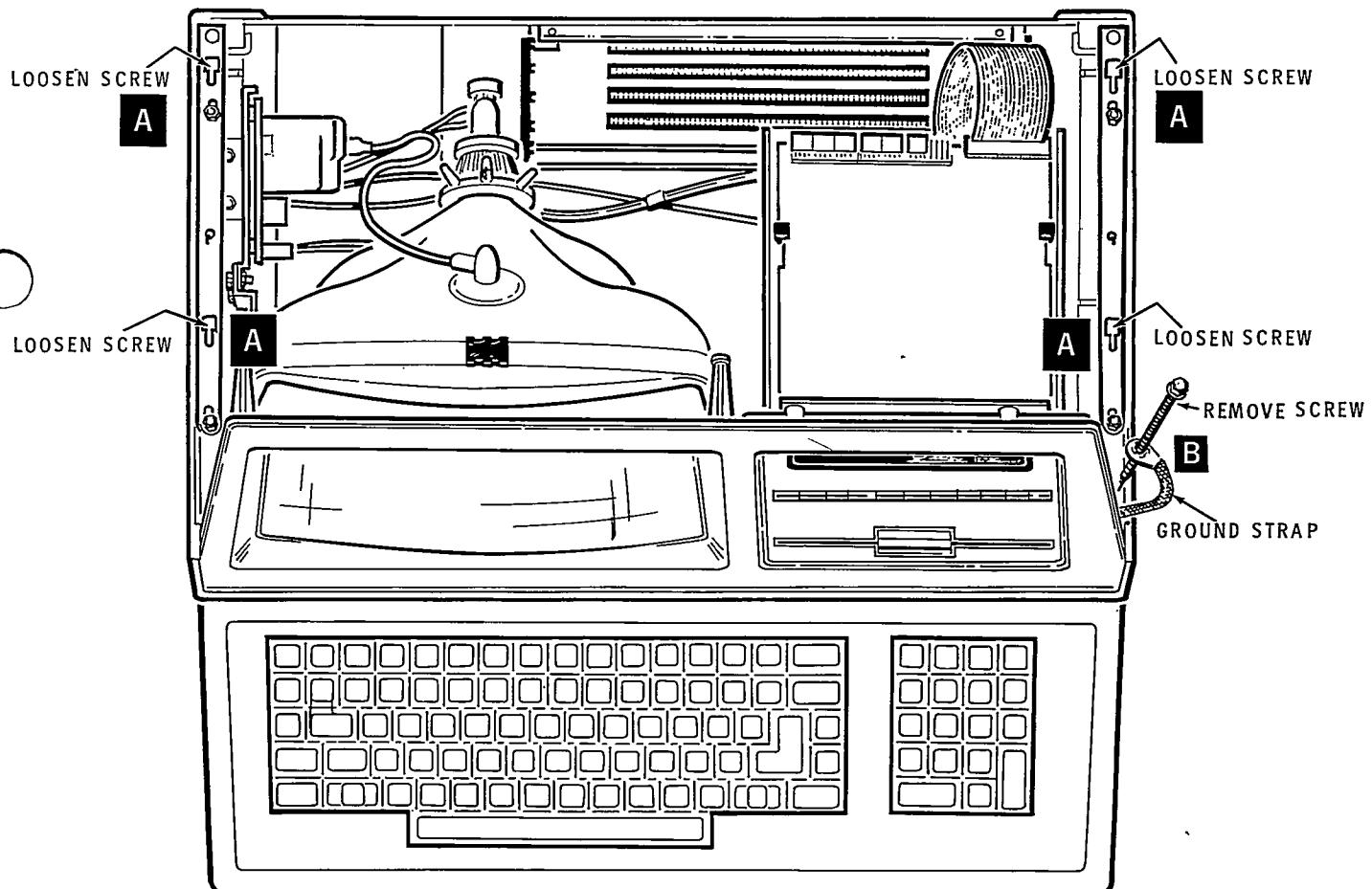


Figure 2-12
CRT and disk drive assembly

Winchester Drive Removal (Refer to Figure 2-13.)

BE SURE THE WINCHESTER HEADS ARE IN THE SHIP POSITION. Refer to Page 3-1.

To remove the Winchester drive:

- Remove the top cover.
- Remove the CRT and disk drive assembly.
- Lay the CRT and disk drive assembly face down.
- Remove the six screws (A).
- Remove the four screws (B) on the bottom of the drive assembly.
- Lift the drive assembly up and away from the center base.
- Remove cables 134-1281 and 134-1389 from the Winchester drive.
- Disconnect the power supply cable from the Winchester drive.
- Remove the four screws (E).
- Carefully pull out the Winchester drive.

Half-Height Drive Removal (Refer to Figure 2-13.)

BE SURE THE WINCHESTER HEADS ARE IN THE SHIP POSITION. Refer to Page 3-1.

To remove the half-height drive:

- Remove the top cover.
- Remove the CRT and disk drive assembly.
- Lay the CRT and disk drive assembly face down.
- Remove the six screws (A).
- Remove the four screws (B) on the bottom of the drive assembly.
- Lift the drive assembly up and away from the center base.
- Remove cables 134-1281 and 134-1379 from the data separator board.

- Remove cable 134-1144 from the half-height drive.
- Remove the four screws (C) holding the data separator board in place.
- Lift off the data separator board.
- Remove the four screws (D) holding the drive to the drive chassis.
- Carefully remove the half height drive.

Winchester Controller Card Removal (Refer to Figure 2-14, foldout from Page 2-13.)

To remove the Winchester controller card:

- Remove the top cover.
- Remove cables 134-1279 and 134-1281 from the Winchester controller card.
- If necessary, remove cable 134-1264 from the floppy disk controller card.
- Remove P6, the power supply connector from the Winchester controller card.
- Lift up on the two card pullers (A) to remove the Winchester controller card.

Data Separator Board Removal (Refer to Figure 2-15, foldout from Page 2-13.)

BE SURE THE WINCHESTER HEADS ARE IN THE SHIP POSITION. Refer to Page 3-1.

To remove the data separator board:

- Remove the top cover.
- Remove cables 134-1280 and 134-1281 from the data separator board.
- Remove the power supply cable.
- Remove the four screws (A).
- Carefully lift out the data separator board.

SHIP UTILITY

The SHIP Utility allows you to place the heads of the Winchester system over a non-vital area of the disks. Then if the system is accidentally jarred during movement, damage will be limited to an area that is not used by the Computer. The floating head design of Winchester drives makes them very sensitive to physical shocks, which can damage the surface of the disks. Therefore, you should use this utility whenever you move the Computer or disassemble the Winchester disk system.

To operate the SHIP Utility, boot your Winchester Utilities disk and type:

SHIP

and press the RETURN key. You will see a display similar to that in Figure 3-1.

SHIP version 1.00
Copyright (C) 1983, Zenith Data Systems

The SHIP utility helps you to:

- * Position the read/write heads of the Winchester disk at a safe location for subsequent transportation of the Winchester disk unit.

SHIP will prompt you to specify a cylinder address to identify where the read/write heads should be moved.

Enter shipping cylinder address in hex:

Figure 3-1
Display for SHIP

At the bottom of the display, you will see:

Enter shipping cylinder
address in hex:

You will need to enter a number that corresponds to the address (location) of the shipping position of the read/write heads.

- Enter 14F (the address in hexadecimal for a Miniscribe Mod II 2012 that corresponds to the shipping position of the heads) and press the RETURN key.
- If you do not have this model, then refer to Drive Specifications, Page 3-2, for the addresses of the shipping position for typical Winchester drives.

The system will correctly position the heads over unused disk space.

- Remove any floppy disk in the system and turn off the Computer. You may now unplug the power cord and proceed with disassembly of the system.

When you start the system running after this utility, the computer will automatically move the heads back to the correct position over the disks.

NOTE: Do not copy this utility to a regular Z-DOS disk. It will modify the operating system of the computer's memory; you will have to reboot the system if you want to perform any other functions with the Z-DOS operating system.

DRIVE SPECIFICATIONS

Some of the Winchester disk systems that can be used with the Z-217 Winchester controller card are listed in Table 3-1.

The model normally supplied in 10 megabyte Winchester configurations is the Miniscribe Mod II 2012 (indicated by the asterisk in the table).

If you have a different drive, use the corresponding figures to answer the prompts presented by the SHIP utility.

NOTE: All amounts are listed in hexadecimal.

Table 3-1
Drive specifications

Manufacturer and Model	No. of Cylinders	No. of Heads	Write Current Cylinder	Precomp Cylinder	Step code	SHIP Cylinder Address
Seagate						
ST-506	99	4	80	40	96	9A
ST-706	132	2	200	80	1	131
ST-406	132	2	200	80	1	131
ST-412	132	4	200	80	1	131
ST-419	132	6	200	80	1	131
Miniscribe						
Mod II 2012*	132	4	200	80	1	14F
Mod IV 4020	1E0	4	200	80	1	209
Mod III 3012	264	2	300	80	1	28D
IMI						
5006H	132	2	200	D6	1	148
4012H	132	4	200	D6	1	148
5018H	132	6	200	D6	1	148
Tandon						
TM 602S	99	4	80	40	96	9A
TM 6032	99	6	80	40	96	9A

This information is provided from Manufacturer's specifications and is subject to change without notice.

REPLACEMENT PARTS LIST

All-In-One, Winchester and Standard Drive Model

ZDS <u>PART NO.</u>	DESCRIPTION
------------------------	-------------

MECHANICAL PARTS

HE 200-1434	Drive chassis
HE 204-2672	Drive bracket
HE 203-2152	Escutcheon
HE 203-2130	Drive panel
HE 391-658	Nameplate
HE 206-1473	Card cage

HARDWARE

HE 250-1418	4-40 × 1/4" hex head screw
HE 250-1422	6-32 × 1/4" phillips head screw
HE 250-1428	6-32 × 1/4" phillips head screw
HE 250-1264	6-32 × 3/8" hex head screw
HE 254-6	# 6 lockwasher

ELECTRICAL PARTS

Circuit Boards

HE 181-3919	Data separator board
HE 181-3920	Winchester controller card
HE 181-3763	Floppy disk controller card

Cables

HE 134-1279	Separator/controller cable – 34 pin
HE 134-1280	Separator/drive cable – 20 pin
HE 134-1281	Drive/controller cable – 34 pin
HE 134-1264	Floppy drive/controller cable – 34 pin

Drives

HE 150-156	Winchester Drive
HE 150-142	Standard floppy disk drive

Low-Profile, Winchester and Standard Drive Model

ZDS <u>PART NO.</u>	DESCRIPTION
------------------------	-------------

MECHANICAL PARTS

HE 204-2675	Left bracket
HE 204-2676	Right bracket
HE 203-2153	Escutcheon
HE 391-653	Nameplate
HE 203-2192	Drive panel

HARDWARE

HE 250-1418	4-40 × 1/4" hex head screw
HE 250-1422	6-32 × 1/4" phillips head screw
HE 250-1428	6-32 × 1/4" phillips head screw
HE 250-1264	6-32 × 3/8" hex head screw
HE 254-6	# 6 lockwasher

ELECTRICAL PARTS

Circuit Boards

HE 181-3919	Data separator board
HE 181-3920	Winchester controller card
HE 181-3763	Floppy disk controller card

Cables

HE 134-1279	Separator/controller cable – 34 pin
HE 134-1280	Separator/drive cable – 20 pin
HE 134-1281	Drive/controller cable – 34 pin
HE 134-1264	Floppy drive/controller cable – 34 pin

Drives

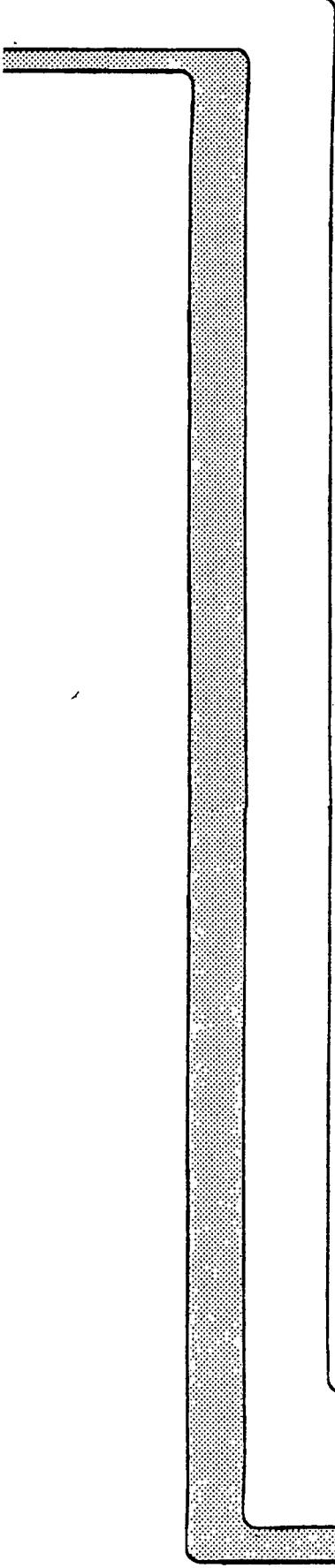
HE 150-156	Winchester drive
HE 150-142	Standard floppy disk drive

All-In-One, Winchester and Half-Height Drive Model

ZDS <u>PART NO.</u>	<u>DESCRIPTION</u>	ZDS <u>PART NO.</u>	<u>DESCRIPTION</u>
MECHANICAL PARTS			
HE 200-1434	Drive chassis		
HE 204-2672	Drive bracket		
HE 203-2189	Drive panel		
HE 391-658	Nameplate		
HE 206-1473	Card cage		
HARDWARE			
HE 250-1218	4-40 × 1/4" hex head screw	HE 150-156	Winchester drive
HE 250-1422	6-32 × 1/4" phillips head screw	HE 150-163	Floppy disk drive – Shugart
HE 250-1428	6-32 × 1/4" phillips head screw	HE 150-168	Floppy disk drive – Mitsubishi
HE 250-1264	6-32 × 3/8" hex head screw	HE 150-169	Floppy disk drive – Qume
HE 254-6	# 6 lockwasher		
ELECTRICAL PARTS			
Circuit Board			
		HE 181-3763	Floppy disk controller card
		HE 181-3919	Data separator board
		HE 181-3920	Winchester controller card
Drives			
		HE 134-1279	Separator/controller cable – 34 pin
		HE 134-1280	Separator/drive cable – 20 pin
		HE 134-1281	Drive/controller cable – 34 pin
		HE 134-1264	Floppy drive/controller cable – 34 pin
Cables			

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INTRODUCTION



The H/Z-100 is a versatile computer system. This computer is designed to be compatible with existing hardware and software products. The H/Z-100 offers an industry standard bus, a widely accepted operating system, high-resolution graphics, expandability, and high-speed computing to the prospective customer.

The computing functions of the H/Z-100 are controlled by two microprocessors; an 8088 and an 8085. The 8088 processor features 16-bit processing in an 8-bit environment. This gives the computer 16-bit speed and power, while still retaining an 8-bit bus. The 8085 processor is an 8-bit processor that is 8080 code compatible. This processor assures a large available software base. Thus, the computer buff with existing 8-bit software is supported.

The H/Z-100 computer is available in two models; the All-in-One and the Low Profile. The main difference between the two models is that the All-in-One contains a built-in video monitor, while the Low Profile does not. Both models include a mass-storage device, two processors, Dynamic RAM, and a professional keyboard.

Flexibility of the computer is assured by a 5-slot, S-100 compatible bus. The S-100 bus was designed to conform to the IEEE-696 definition of the S-100 bus. This definition was chosen since it is the widely accepted standard among computer manufacturers. This bus design provides an opportunity for the user to tailor a hardware environment to suit his needs. Additional I/O, slave processors, and special function S-100 boards from Heath Company and other sources will work within the H/Z-100.

To communicate with the outside world, the H/Z-100 motherboard contains on-board peripheral connections. These connections consist of two serial ports and a parallel port. The serial ports are configured to RS-232C standards. One is a DCE interface and the other is a DTE interface. The parallel port is configured as a Centronics compatible printer interface. Because these connections are built into the motherboard, a separate S-100 I/O card is not needed. Thus, space in the S-100 card cage is conserved.

In addition, the H/Z-100 contains many other features. These include:

- Two keyboard modes.
- Light pen input.
- Three timer outputs.
- H-19 graphic and escape code compatible.
- Wired and tested mother board.

These features, along with the stylish molded cabinet, make the H/Z-100 computer a powerful computing tool.

The information in this section of the manual enables you to service the H/Z-100 to the module level. If you require more information on an individual board, refer to the section entitled by the board name.

SPECIFICATIONS

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CPU

Processor 1 Intel 8088.
Clock 5 MHz.
Type 16-bit CPU.
Wait State Memory, Ø; I/O, 1.

Processor 2 Intel 8085.
Clock 5 MHz.
Type 8-bit CPU.
Wait State Memory, 1; I/O, 2.

On-Board Memory 64K to 192K bytes in 64K increments. Parity checked.

Memory Space 1 megabyte.
Monitor Space One 64K page.
Video RAM Space Three 64K pages.
User Memory Space 3/4 megabyte.

Interrupts

Controller Dual 8259A.
System 15-level priority vector interrupt.

VIDEO DISPLAY

CRT (All-in-One) 12" diagonal, green non-glare or optional white or amber.
Display Format 25 lines of 80 characters.
Display Size 6.5" high x 8.5" wide.
Character Size 0.2" high x .1" wide (approximate).
Character Set "Soft", dynamically redefinable.
Character Type 5 x 9 dot matrix.
Dot Resolution 640 x 225 pixels.
Colors (optional) Eight: Red, green, blue, white, black, cyan, magenta, and yellow.
Gray Scale Eight levels when a monochrome display is used and the color option is installed in the computer.

Options

Interlace Mode 640 x 500 pixels.
Pages Second page of display.
Light Pen One pixel resolution.

Outputs Red, green, blue, composite video,
composite sync and separated
horizontal and vertical sync.

BUS STRUCTURE

Type Proposed IEEE-696 (S-100).
Number of Slots Five.
Data Bus Width Eight bits.
Address Bus Width Twenty-four bits.
I/O Addressing Eight bits.

TIMER

Type Programmable.

KEYBOARD

Type 95 keys: 61-key alphanumeric
and 16-key function and control
section, plus an 18-key numeric
and cursor control section.
Modes Two: ASCII and Event Driven.
Processor FIFO buffer (17 character).
Key Click May be disabled.

DISK CONTROLLER

(May be omitted on S-100 Card)

Type	WD1797.
Drives Supported	Up to four each.
5-1/4"	Single/double-sided, 48 TPI, single/double density.
8"	Single/double-sided, single/ double density.
Data Separator	Phase-locked loop.
Precompensation	Variable independently for both 5-1/4" and 8" sizes.
Data Transfer	Programmed using wait states, interrupt or polling.

Internal Disk Drive

Size	5-1/4".
Sides	Single or double.
Tracks per Inch	48.
Capacity (formatted) ..	80K, 160K, or 320K; depending on the number of sides and density.
Track Format	4K, eight sectors of 512 bytes each.
Stepping Speed	6 milliseconds per track or faster.

External Disk Drive

Interface Type	Shugart 850 or equivalent.
Winchester Disk Drive (optional)	
Type	One internal 5" replacing one internal disk drive.

INPUT/OUTPUT

Serial I/O	Dual RS-232 ports, one DTE and one DCE.
Baud Rate	110 to 38,400.
Operation	Asynchronous RS-232 or synchronous.
Stop Bits	One, one and one half, or two.
Word Length	Five, six, seven, or eight bits.
Break Capability	Detection and generation.
Parity	Even, odd, or none.
Parallel I/O	Eight-bit output only.
Type	Centronics.

POWER SUPPLY

Input, Volts 120 VAC or 240 VAC.
Input, Hertz 50 Hz or 60 Hz.

TEMPERATURE AND HUMIDITY

Operating Temperature ... 15.6 to 32.2 degrees Celsius
(60 to 90 degrees Fahrenheit).
Storage Temperature 10 to 43 degrees Celsius
(50 to 110 degrees Fahrenheit).
Operating Humidity 8% to 80%, noncondensing.

DIMENSIONS

All-in-One 19" W x 19.5" D x 13.5" H
(47.5 x 48.75 x 33.75 cm).
Low-Profile w/o Monitor . 19" W x 19.5" D x 7.125" H
(47.5 x 48.75 x 17.8 cm).

WEIGHT

All-in-One 50 lbs (22.7 kg).
Low-Profile 40 lbs (18.2 kg).

*Heath Company and Zenith Data Systems reserves the right
to discontinue products and to change specifications at
any time without incurring obligation to incorporate new
features in products previously sold.*

OPERATION

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In this section, operation of the H/Z-100 computer is discussed. This specifically covers power-up and reset, MTR-100 commands, and H-19 emulation. Information on hardware and peripheral applications can be found in the configuration section.

POWER-UP AND RESET

When shipped to the customer, the H/Z-100 is hardware set by S101 in auto-boot mode. This means that upon power-up or reset, MTR-100 will initialize the computer and automatically start the boot routine. If a disk is not found in the default drive within 30 seconds after power-up or reset, MTR-100 will print a boot error message and enter the monitor mode. The boot routine, however, may be averted in two different ways. The first way is to reset S101 (this is covered in Configuration). The second way is to use the delete key. By pressing the delete key during the boot routine, the routine is halted and the computer enters the monitor mode.

To power-up the computer, flip the switch on the right rear corner of the computer. To reset, the CTRL and RESET keys are simultaneously pressed. During the initialization process, MTR-100 selects the active processor, initializes the hardware devices, sizes RAM, and sets the stack segment. MTR-100 then times out 30 seconds and starts the boot routine.

There are two MTR-100 commands; Boot and Version. MTR-100 features command completion where only the first letter of the command is typed in and the computer will finish typing in the rest of the command. A detailed description of each command follows. Please note that these commands will be ignored if the computer is not in the monitor mode.

BOOT

The boot command will boot from the default drive specified by bits 0-2 of the configuration dip switch S101. MTR-100 contains all the code necessary to boot an operating system from the default drive. The command is initiated by pressing the B key after the hand prompt. The computer will respond with "oot". The pressing of the RETURN key will cause MTR-100 to jump to and start the boot-up routine. Pressing the DELETE or BACKSPACE keys will cause the boot routine to abort. An aborted boot returns the computer to the monitor mode, even if auto-boot is configured.

VERSION

The version command is intended to allow non-technical users of the H/Z-100 to identify which version of MTR-100 is installed in their machine. The command is implemented by pressing the V key after the hand prompt. The computer will respond with "ersion" and MTR-100 will identify itself.

H-19 EMULATION

To keep the H/Z-100 compatible with existing software, H-19 emulation of the keyboard and character display is necessary. This is accomplished through the use of subroutines within MTR-100. All of the H-19 escape sequences except the ANSI mode are supported. It is important to note that the H-19 escape sequences are supported during software control. Since there is no OFF LINE key, the terminal cannot be programmed directly from the keyboard. For further information on the keyboard, refer to the keyboard section of this manual.

SUMMARY OF H/Z-100 ESCAPE CODES

Escape Sequence	Definition	Escape Sequence	Definition	Escape Sequence	Definition
CURSOR FUNCTIONS		Configuration (continued)		ALTERNATE KEYPAD SEQUENCE	
ESC A	Cursor up	ESC x*	Set mode(s)	ESC ?M	Enter key
ESC B	Cursor down	*	1 = Enable 25th line	ESC ?n	Period (.) key
ESC C	Cursor right		2 = No key click	ESC ?p	0 key
ESC D	Cursor left		3 = Enter hold screen mode	ESC ?q	1 key
ESC H	Cursor home		4 = Block cursor	ESC ?r	2 key
ESC I	Reverse index		5 = Cursor off	ESC ?s	3 key
ESC Y	Direct cursor addressing		6 = Keypad shifted	ESC ?t	4 key
ESC J	Save cursor position		7 = Enter alternate keypad mode	ESC ?u	5 key
ESC n	Cursor position report		8 = Auto line feed on receipt of CR	ESC ?v	6 key
ESC k	Set cursor to previously saved position		9 = Auto CR on receipt of line feed	ESC ?w	7 key
			! = Nonblinking cursor	ESC ?x	8 key
			< = Disable keyboard auto repeat	ESC ?y	9 key
			? = Enable key expansion		
			Reset mode(s)		
		ESC y*		ADDITIONAL FUNCTIONS	
ESC E	Clear display and home cursor			ESC Z	Identify as VT52/ESC /K)
ESC J	Erase to end of page			ESC #	Transmit page
ESC K	Erase to end of line			ESC]	Transmit 25th line
ESC L	Insert line			ESC ^	Transmit current line
ESC M	Delete line			ESC _	Transmit character at cursor
ESC N	Delete character			ESC \	Zenith identify terminal type
ESC O	Exit insert character mode			ESC 10	
ESC @	Enter insert character mode			ESC m*	Foreground and background colors
ESC b	Erase to beginning of display			*	
ESC 1	Erase entire line			0 = Black	
ESC o	Erase to beginning of line			1 = Blue	
				2 = Red	
				3 = Magenta	
				4 = Green	
				5 = Cyan	
				6 = Yellow	
				7 = White	
				Keyboard enable	
				Keyboard disable	
				Wrap-around at end of line	
				Discard at end of line	
CONFIGURATION		ESC z	Modify baud rate	ESC {	
ESC r*		*	A = 110	ESC }	
			B = 150	ESC]	
			C = 300	ESC v	
			D = 600	ESC w	
			E = 1200		
			F = 1800		
			G = 2000		
			H = 2400		
			I = 3600		
			J = 4800		
			K = 7200		
			L = 9600		
			M = 14400		
			N = 19200		
			O = 38400		
			P = 57600		
			Q = 72000		
			R = 96000		
			S = 115200		
			T = 153600		
			U = 230400		
			V = 384000		
			W = 576000		
			X = 720000		
			Y = 960000		
			Z = 1152000		
			Modes of operation		
			ESC F	Enter graphics mode	
			ESC G	Exit graphics mode	
			ESC >	Enter alternate keypad mode	
			ESC >	Exit alternate keypad mode	
			ESC P	Enter reverse video mode	
			ESC Q	Exit reverse video mode	
			ESC T	Enter keypad shifted mode	
			ESC U	Exit keypad shifted mode	

Octal ()
Decimal []
Hex

GRAPHIC SYMBOLS

(136) 94 6E	(137) 95 5F	(140) 96 60	(141) 97 61 a	(142) 98 62 b	(143) 99 63 c	(144) 100 64 d	
(145) 101 65 e	(146) 102 66 f	(147) 103 67 g	(150) 104 68 h	(151) 105 69 i	(152) 106 6A j	(153) 107 6B k	
(154) 108 6C l	(155) 109 6D m	(156) 110 6E n	(157) 111 6F o	(160) 112 70 p	(161) 113 71 q	(162) 114 72 r	
(163) 115 73 s	(164) 116 74 t	(165) 117 75 u	(166) 118 76 v	(167) 119 77 w	(170) 120 78 x	(171) 121 79 y	
(172) 122 7A z	(173) 123 7B {	(174) 124 7C :	(175) 125 7D }	(176) 126 7E			

CONFIGURATION

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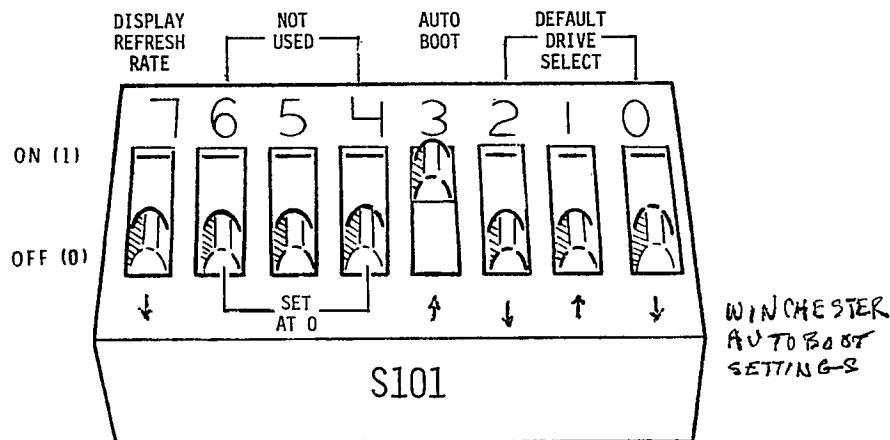
INTRODUCTION

The H/Z-100 is a versatile computer. Due to this versatility, many different configurations are possible. This section provides the basic information on how the computer may be configured.

MOTHERBOARD CONFIGURATION

S-101

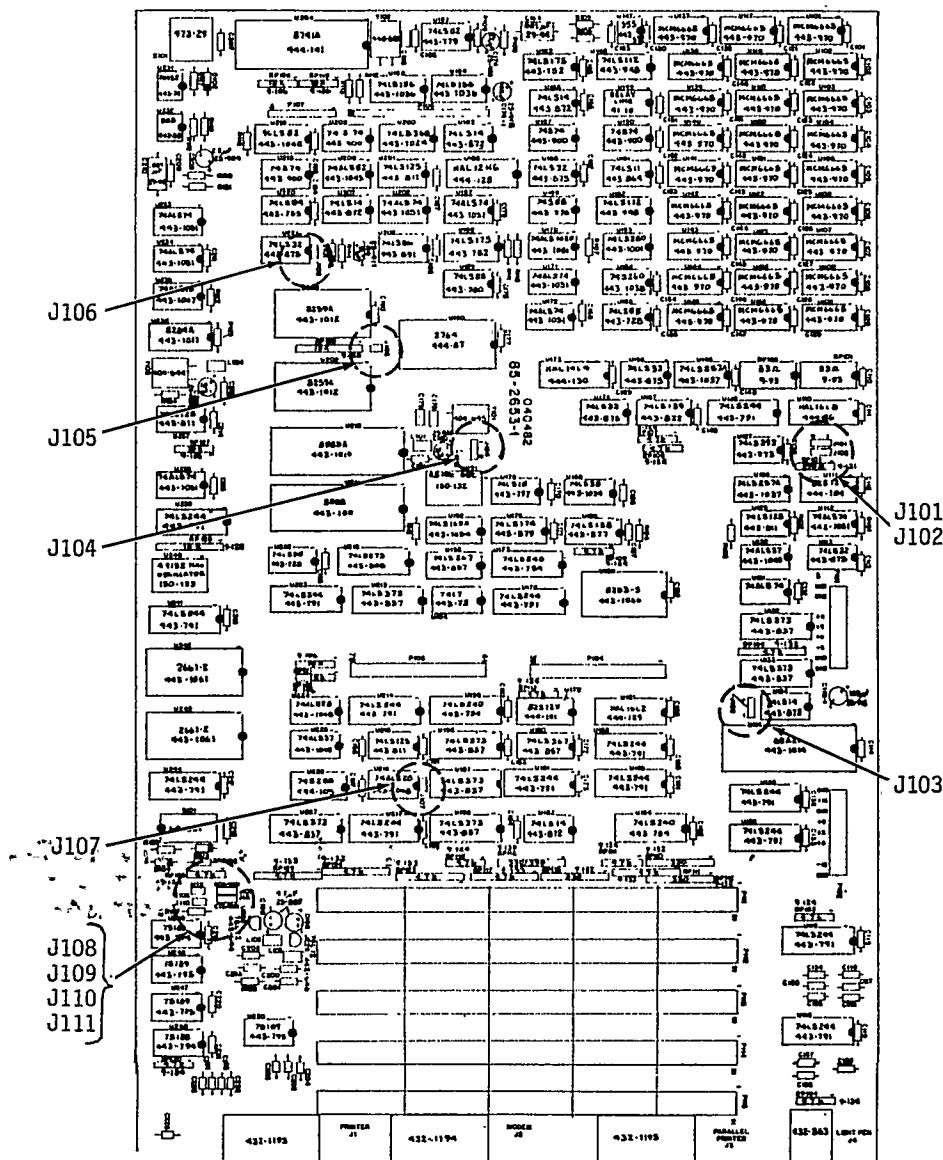
The 8-section slide switch (S101) on the motherboard determines the condition of the computer upon power-up or reset. The sections of S101 are defined as follows:



<u>Section</u>	<u>Definition</u>
0-1-2	The positions of these bits determine the default drive. 000 = 5-1/4". 100 = 8". 010 = Winchester.
3	This bit determines auto-boot. 0 = manual booting. 1 = Auto-boot.
4	Not used. Leave at 0.
5	Not used. Leave at 0.
6	Not used. Leave at 0.
7	This bit determines refresh rate of the display RAM. 0 = 60 Hz. 1 = 50 Hz.

JUMPERS J101 THROUGH J111

Refer to the pictorial below when reading through the jumper descriptions.



J101 and J102 determine the size of ROM that may be installed.

<u>ROM</u>	<u>J101</u>	<u>J102</u>
2764 (8K)	0	0
27128 (16K)	1	0
27256 (32K)	0	1

The 27128 and 27256 ROMs are not used in the H/Z-100 at this time, but may be supported in the future.

J103 determines the polarity of the light pen. The markings on the PC board are self-explanatory. The light pen is not supported at this time.

J104 is jumpered by a foil run on the motherboard to the 1 position. This connection jumpers the NMI line to ground.

J105 when jumpered, grounds the test pin of the 8088 microprocessor. J105 is not used at this time.

J106 is not used at this time. This position is normally unjumpered.

J107 is jumpered by a foil run on the motherboard. This position will be shorted regardless of a jumper.

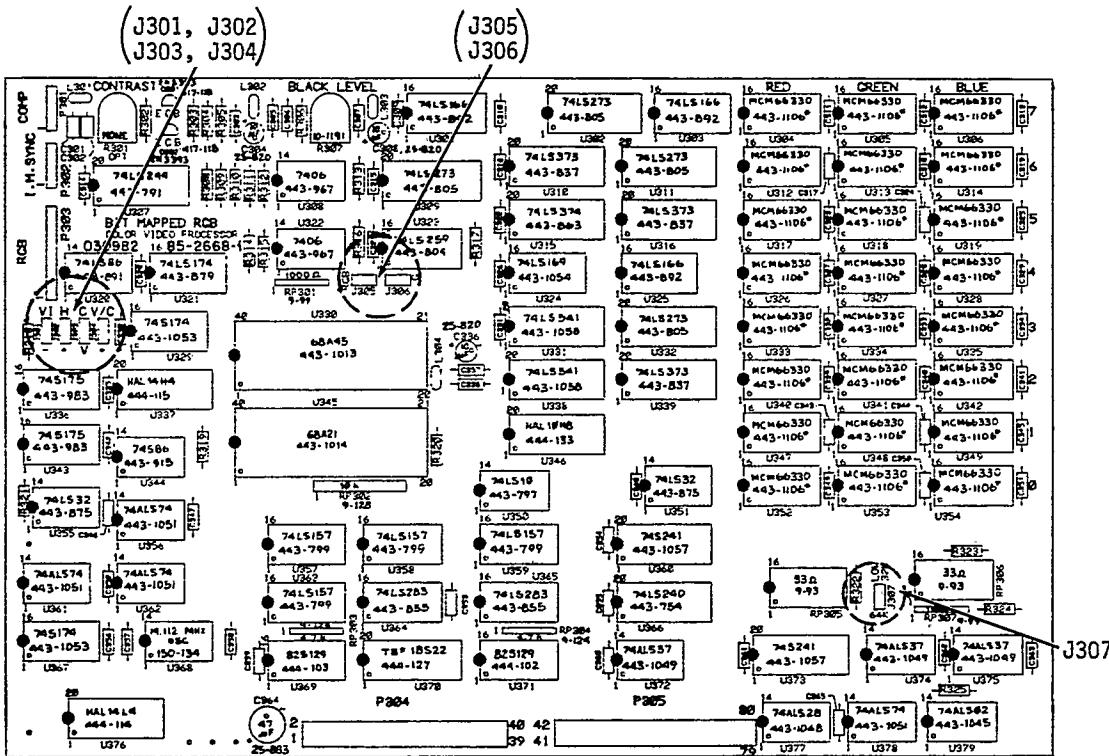
J108 determines whether or not pin 18 (TxEMP) of U242 is connected to the serial interrupt line (EPCIBINT). When using Heath peripherals, this jumper location is normally unjumpered.

J109 and J111 determine the handshaking protocol of IC U243. This port will support many different printers through the positioning of these jumpers. J109 determines whether pin 16 (DCD) of U243 is connected to the RTS line or ground. J111 determines whether pin 17 (CTS) of U243 is connected to the RTS line or ground. Using Heath peripherals, J109 connects DCD to RTS and J111 connects CTS to ground. If the H/Z-100 you are servicing is not set up in the Heath configuration, the jumpers may be connected to support another manufacturer's peripheral. Consult the peripheral manual for proper jumpering.

J110 determines whether or not pin 18 (TxEMP) of U243 is connected to the serial interrupt line (EPCIANT). The position of this jumper is determined by the peripheral used on this port. When using Heath peripherals, this jumper location is normally unjumpered.

VIDEO BOARD CONFIGURATION

Refer to the pictorial below when reading through the jumper descriptions.



J301 determines the polarity of the vertical sync as connected to the internal monitor. The markings on the PC board are self-explanatory. In the Heath mode, this jumper is set for negative vertical sync.

J302 determines the polarity of the horizontal sync. The markings on the PC board are self-explanatory. In the Heath mode, this jumper is set for negative horizontal sync.

J303 determines whether the signal at pin 9 of the RGB cable assembly is composite sync or vertical sync. When the jumper is in the CV position, the signal at pin 9 of the RGB cable assembly is composite sync. When the jumper is in the V position, the signal at pin 9 of the RGB cable assembly is vertical sync.

J304 determines the polarity of the vertical sync as connected to the RGB cable assembly. The markings on the PC board are self-explanatory. In the Heath mode, this jumper is set for negative vertical sync.

J305 and J306 determine the type of video signal that is to be available. When the jumpers are in the RGB position, the output video signal will support a color or an 8-level gray scale output. When the jumpers are in the G position, the video output will be a monochrome signal. If the video board contains only one bank of RAM, these jumpers must be set at G.

J307 determines how the individual 64K RAM banks will be addressed. When no jumper is installed, the video board will address the high 32K end of the 64K bank. When the jumper is installed in the 32K position, the video board will address the lower 32K end of the 64K bank. When the jumper is installed in the 64K position, the video board will address a 32K section within the 64K bank. NOTE: An advanced programmer may address the whole 64K bank of RAM if he alters the operation of the CRTC. This, however, is not supported at this time. To further explain the jumpering of these two jumpers, the RAM chips that may be installed in the banks must be discussed.

There may be two primary RAM chips installed on the video board; 64K or 32K chips. The 32K RAM chips are further divided in two categories; high end 32K or low end 32K chips. Because 32K RAM chips are actually 64K chips that failed in either the high or low section of the 64K memory area, the 32K and 64K chips are pin for pin compatible. To tell the difference between the two types of 32K chips, you must first identify the manufacturer.

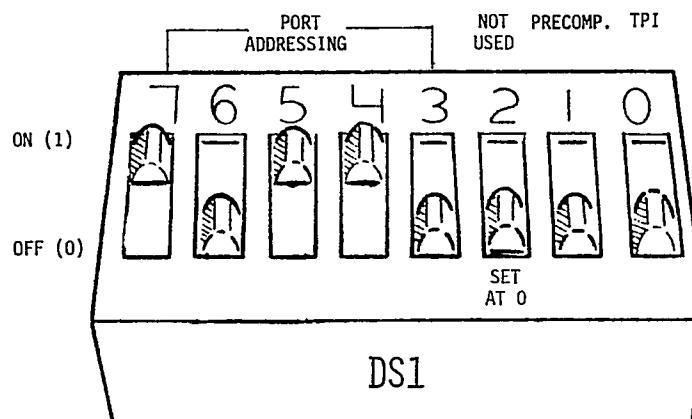
There are two approved manufacturers at this time, Motorola and Okie. Use the chart below to identify high-end or low-end chips.

Manufacturer	Generic Number	Type
Okie	MSM3732L-20AS	low end (HE 443-1106)
Okie	MSM3732H-20AS	high end (HE 443-1107)
Motorola	MCM66330	low end (HE 443-1106)
Motorola	MCM66331	high end (HE 443-1107)

Once you have the chips identified, you can set the jumper J307. Remember, you cannot mix low end and high end 32K chips on the video board. You may, however, mix manufacturers. If the majority of chips are high end chips, then all chips must be high end and J307 set accordingly. If the majority of the chips are low end chips, then all chips must be low end and J307 set accordingly. If the chips are 64K RAMs, you must set J307 to the 64K position.

DISK CONTROLLER (H/Z-207)

The 8-section slide switch (DS1) on the disk controller board determines the configuration of the board. The sections of DS1 are defined as follows:



<u>Section</u>	<u>Definition</u>
0	This bit determines the TPI of the 5-1/4" disk drive. 0 = 48 TPI. 1 = 96 TPI.
1	This bit determines whether precomp is on or off. 0 = precomp off. 1 = precomp on.
2	Not used. Leave at 0.
3-4-5-6-7	Port addressing. A port I/O map is shown below:

I/O ADDR. (Binary)	READ	WRITE	PORT DESIGNATION
SSSSS000 * --- --	X		1797 Status Register
SSSSS000		X	1797 Command Register
SSSSS001	X	X	1797 Track Register
SSSSS010	X	X	1797 Sector Register
SSSSS011	X	X	1797 Data Register
SSSSS100		X	Control Latch
SSSSS101	X		Status Port

* S = dip switch bit

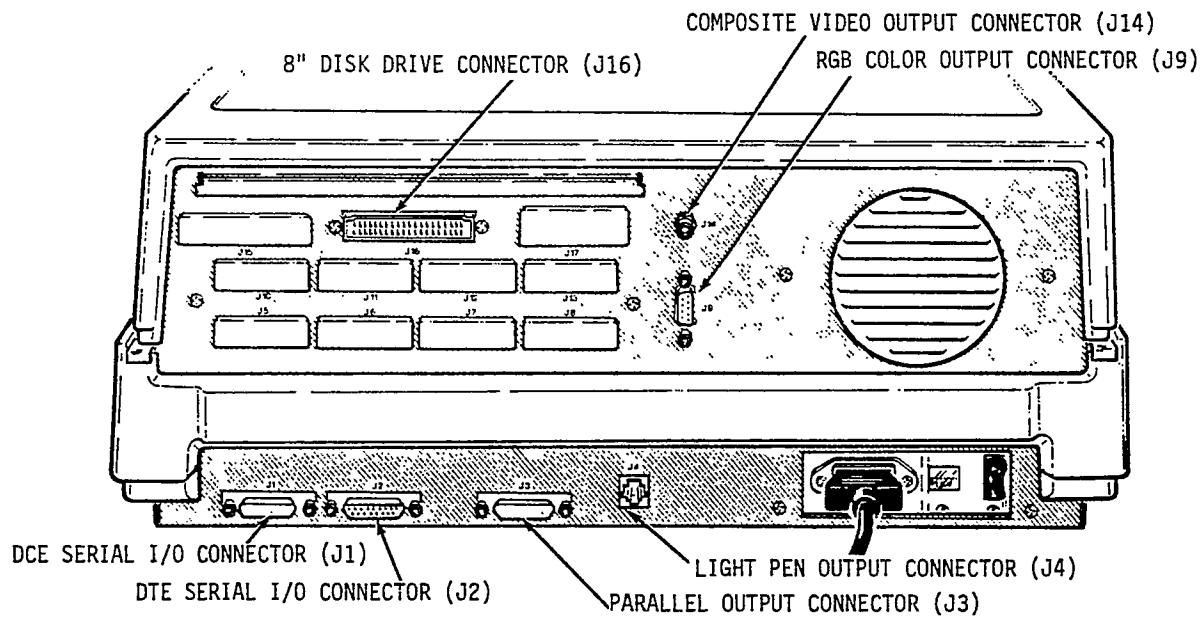
; : ;

The dip switch bits are simply defined from the binary equivalent of the switches. An example, port addressing for the H/Z-100, is shown below.

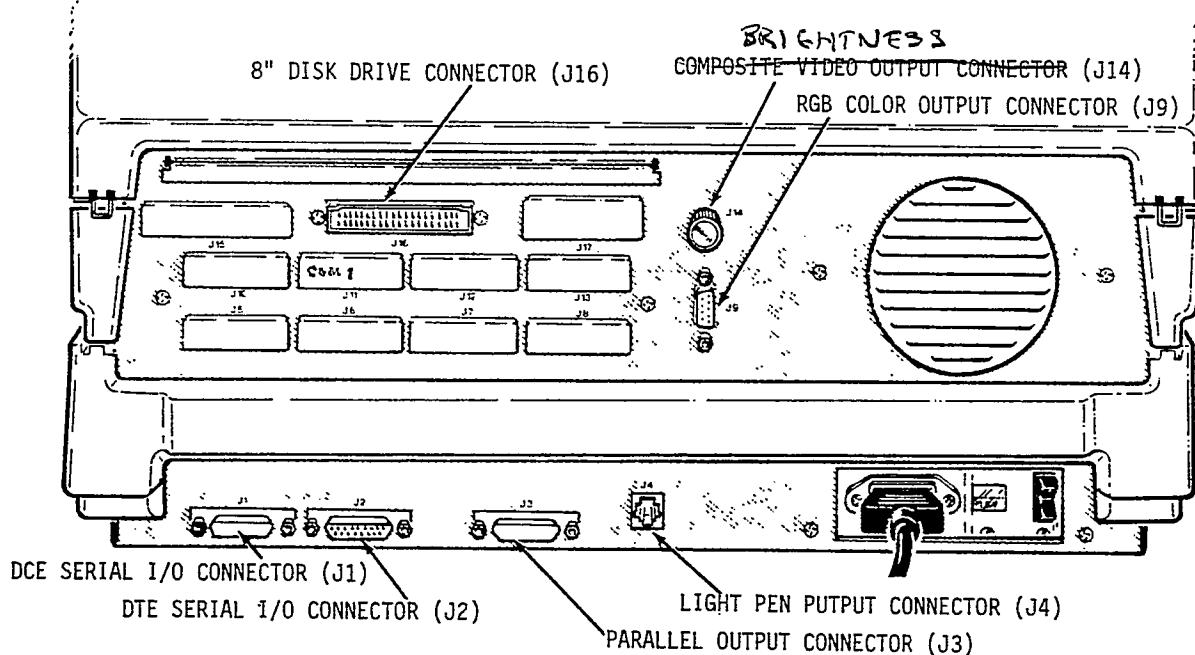
SSSSSXXX * = 10110XXX = H/Z-100 port B0 - B7.

* X = 1797 register, control latch, or status port.

OUTPUT CONNECTORS



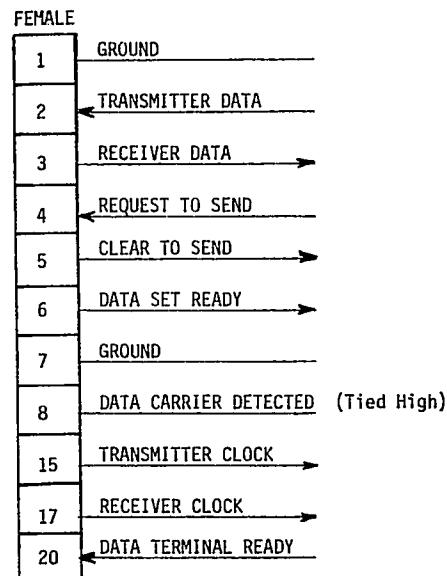
LOW PROFILE



ALL-IN-ONE

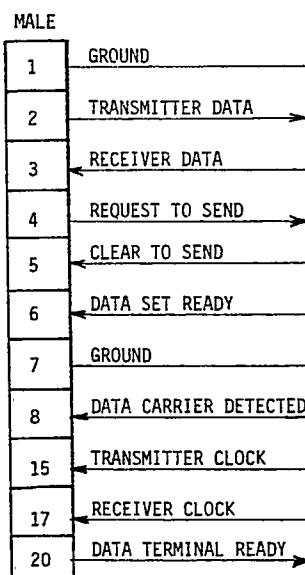
SERIAL I/O CONNECTOR (J1)

The 25-pin D connector at this location is a RS-232C DCE connector. Its location on the I/O map is port E8 (Hex). The primary use of this connector is for printer operation. For Heath supported printers, refer to "Printer Configuration" (elsewhere in this section) for recommended hardware set-up. Other peripherals and non-Heath printers may require special set up procedures. Use the pinout description and the peripheral's manual for recommended set-up.



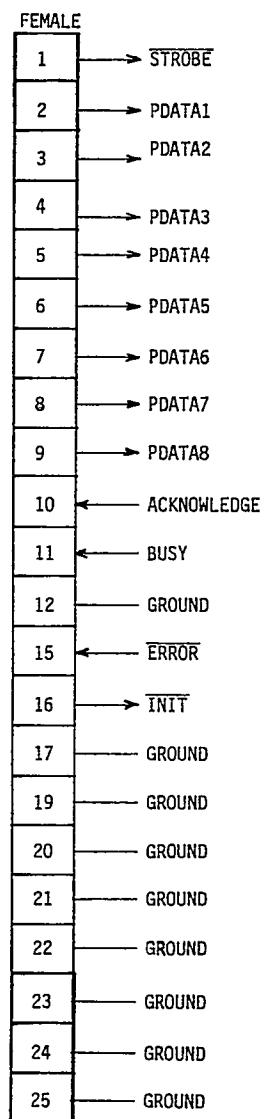
SERIAL I/O CONNECTOR (J2)

The 25-pin D connector at this location is an RS-232C DTE connector. Its location the I/O map is port EC (Hex). The primary use of this connector is for modem operation. Refer to the pictorial below for a description of the pinouts of this connector.



PARALLEL OUTPUT CONNECTOR (J3)

The 25-pin D connector at this location is a Centronics compatible printer port. Its location on the I/O map is E0 (Hex). The primary use of this connector is for parallel printer hookup. Refer to the pictorial below for a description of the pinouts of this connector.



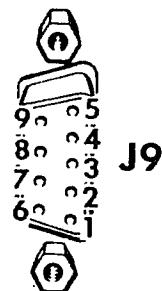
LIGHT PEN OUTPUT CONNECTOR (J4)

This connector provides the necessary signals to operate a light pen.

COLOR OUTPUT CONNECTOR (J9)

When the video board has the color option installed, this connector provides the necessary signal to drive an RGB video monitor. Refer to the pictorial below for a description of the pinouts of this connector. Also refer to the video monitor's manual for hookup instructions.

<u>Pin</u>	<u>Signal</u>
1	Ground
2	Ground
3	Red
4	Green
5	Blue
6	Not connected
7	Not connected
8	Horizontal Sync
9	Vertical or Composite Sync

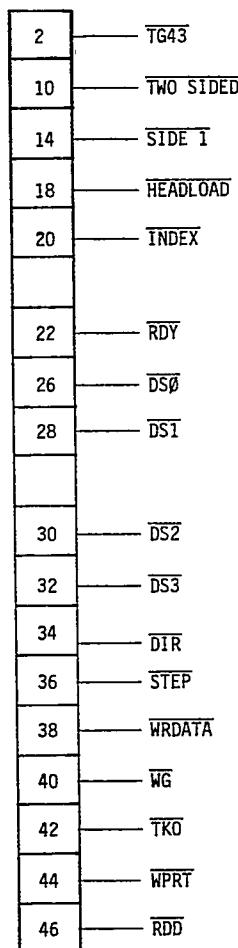


COMPOSITE VIDEO OUTPUT CONNECTOR (J14, LOW PROFILE ONLY)

This connector is located on the Low Profile model. This connector provides the necessary signals to drive a monochrome video monitor. Refer to the manual of the video monitor for instructions on hookup.

8" DISK DRIVE CONNECTOR (J16)

This 50-pin connector provides the necessary signals to drive an 8" Shugart compatible disk drive. Refer to the pictorial below for a description of the pinouts of this connector.



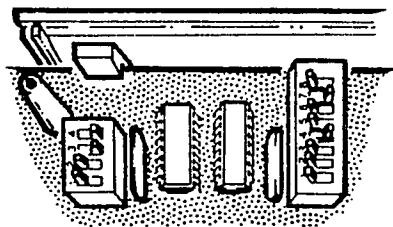
*All odd numbered pins grounded

PRINTER CONFIGURATIONS

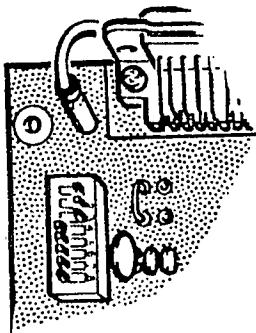
Refer to the following pictorials for information on how to set the configuration switches within the following Heath supported printers. Handshaking for each of the printers is software supported in Z-DOS using the program "CONFIGUR". For information on the Configur program, refer to the Z-DOS manual or the H/Z-100 User's Manual.

MX-80 PRINTER

The MX-80 may be connected to the H/Z-100 using either the parallel or serial modes. To use the MX-80 in the parallel mode, set the switches within the MX-80 case as follows:

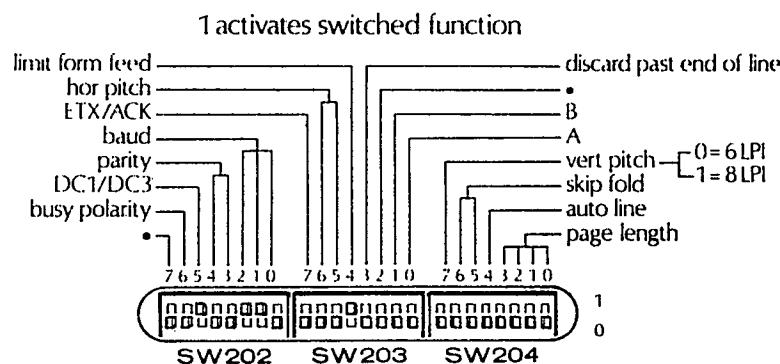


Remember, the interface cable must be attached to the parallel output connector J3 for the MX-80 to operate in the parallel mode. To use the MX-80 in the serial mode set the switch on the serial board within the MX-80 as follows:



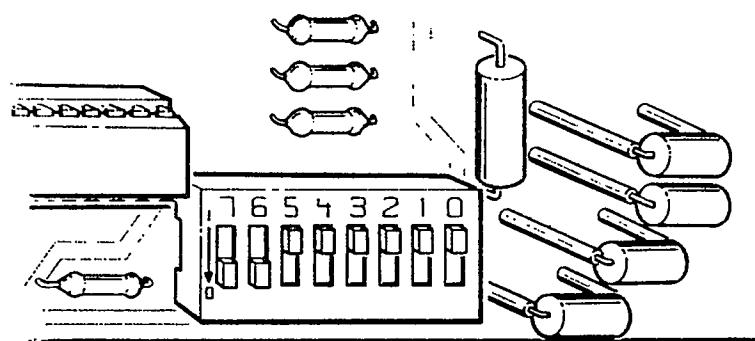
H/Z-25 PRINTER

To use the H/Z-25 with the H/Z-100, set switches SW202, SW203, and SW204 as shown below:



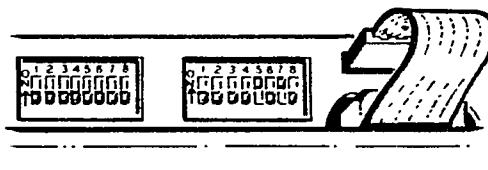
H/WH-14 PRINTER

To use an H/WH-14 with the H/Z-100, set switch SW102 as shown below:



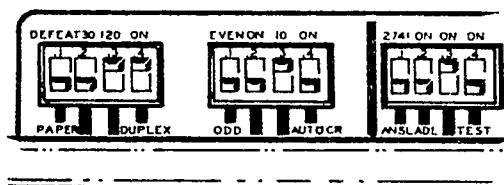
DIABLO 630 PRINTER

To use a Diablo 630 with the H/Z-100, set the internal switches as shown below:



DIABLO 1640 PRINTER

To use a Diablo 1640 with the H/Z-100, set the internal switches as shown below:



If other manufacturer's printers are being used, refer to its manual to determine proper configuration for that printer.

NEC VIDEO MONITOR CONFIGURATION

Follow the instructions below to configure the NEC Video Monitor cable for use with the H/Z-100.

- Remove the DIN-type connector from the NEC Video Monitor cable (P/N PC-8091A).
- Obtain a subminiature 9-pin male D connector (Amp P/N 205204-1) and cable clamp assembly (Amp P/N 207908-1).
- Remove 3/4" of outer insulation material from the NEC cable.
- Remove 1/4" of insulation from each end of the exposed conductors. Pre-tin each wire.
- Connect each of the wires from the NEC cable to the 9-pin connector as follows:

Quantity	NEC Cable	D Connector Pinout	Signal
1	BR/WHT	5	Blue Video
1	BR/BLK	4	Green Video
1	BR/Red	3	Red Video
3	Solid Yellow	2	Ground
2	Solid Yellow	1	Ground
1	Solid Gray	1	Ground
1	YEL/WHT	9	V Sync
1	YEL/BLK	8	H Sync

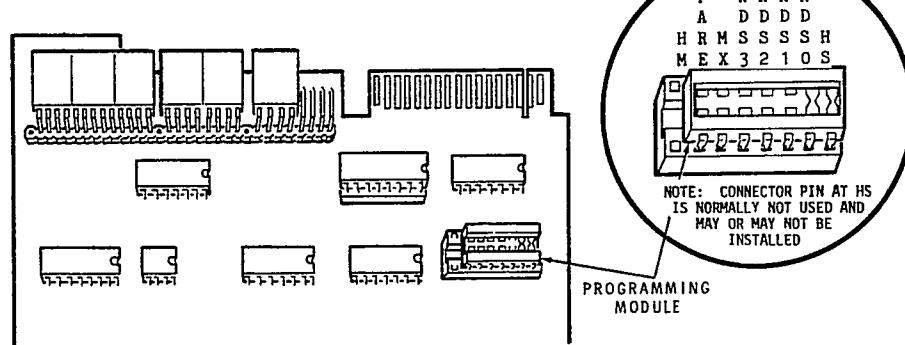
- Assemble the cable clamp assembly.

INTERNAL DISK DRIVE CONFIGURATION

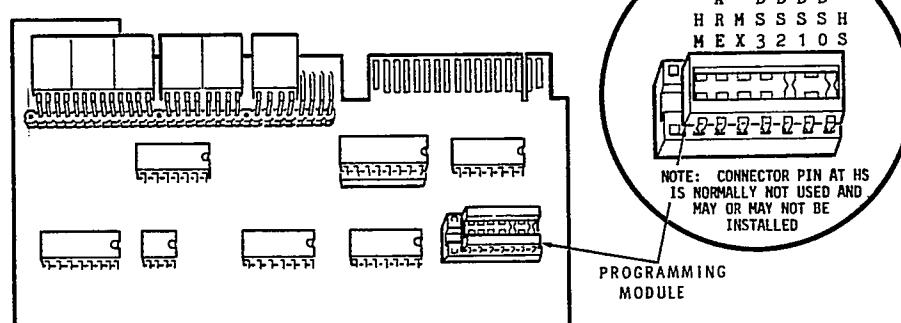
Drive programming for the internal 5-1/4", 48 TPI Tandon disk drives is shown below. On some disk drives the jumper pack shown below may be replaced with a single jumper wire at NDS0 or NDS1. This configuration is considered normal since connection across HS is not necessary. If you encounter one of these drives, do not replace the jumper wire with the jumper pack (HE 432-1068). The leads on this jumper pack are too thin and may not make proper contact in the socket. If you do not have a Tandon jumper pack, carefully insert a piece of bare wire (HE 340-8) into the proper location.

The location of the resistor pack is the same as in other Heath or Zenith Data Systems disk drive systems. That is, the resistor pack(s) are removed from all drives except the last hardware unit.

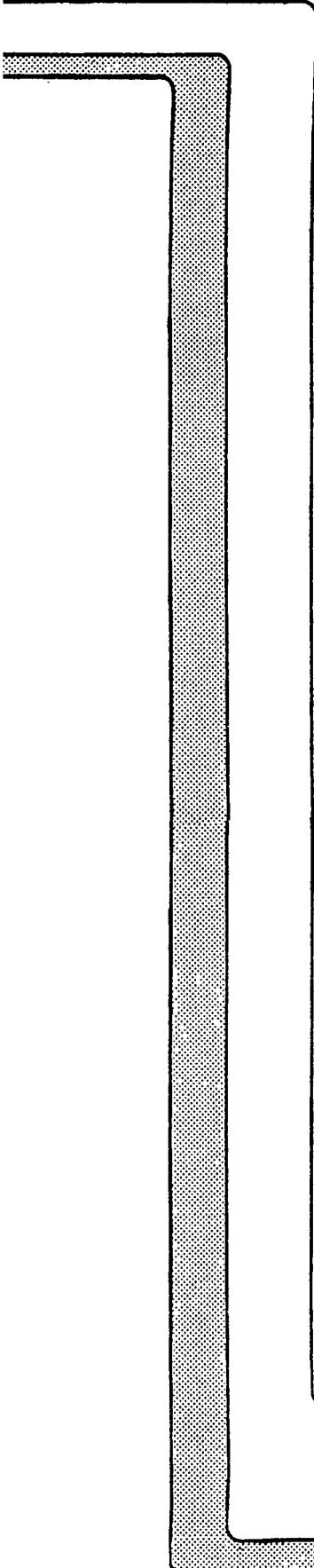
HARDWARE UNIT ZERO (DS1)



HARDWARE UNIT ONE (DS2)



TECHNICIAN NOTES:



NORMAL OPERATING CHARACTERISTICS



The following characteristics of the H/Z-100 Computer are considered normal. Become familiar with these characteristics. It can save you time by preventing any servicing of the computer for a condition that is considered normal operation.

- During the boot process, the cursor will move to a random position in the line "Read Completed". The position of the cursor may change with each boot-up.
- The internal 5-1/4" disk drives will not turn off until they time out 18 seconds after the last deselection. Even if a master reset is initiated, the drive motors will stay on until they are timed out.
- The computer is sent to the customer in the auto-boot mode. If a disk is not installed within 30 seconds after power-up, the display will show a disk error message and the computer will go into the monitor mode.

BLOCK DESCRIPTION

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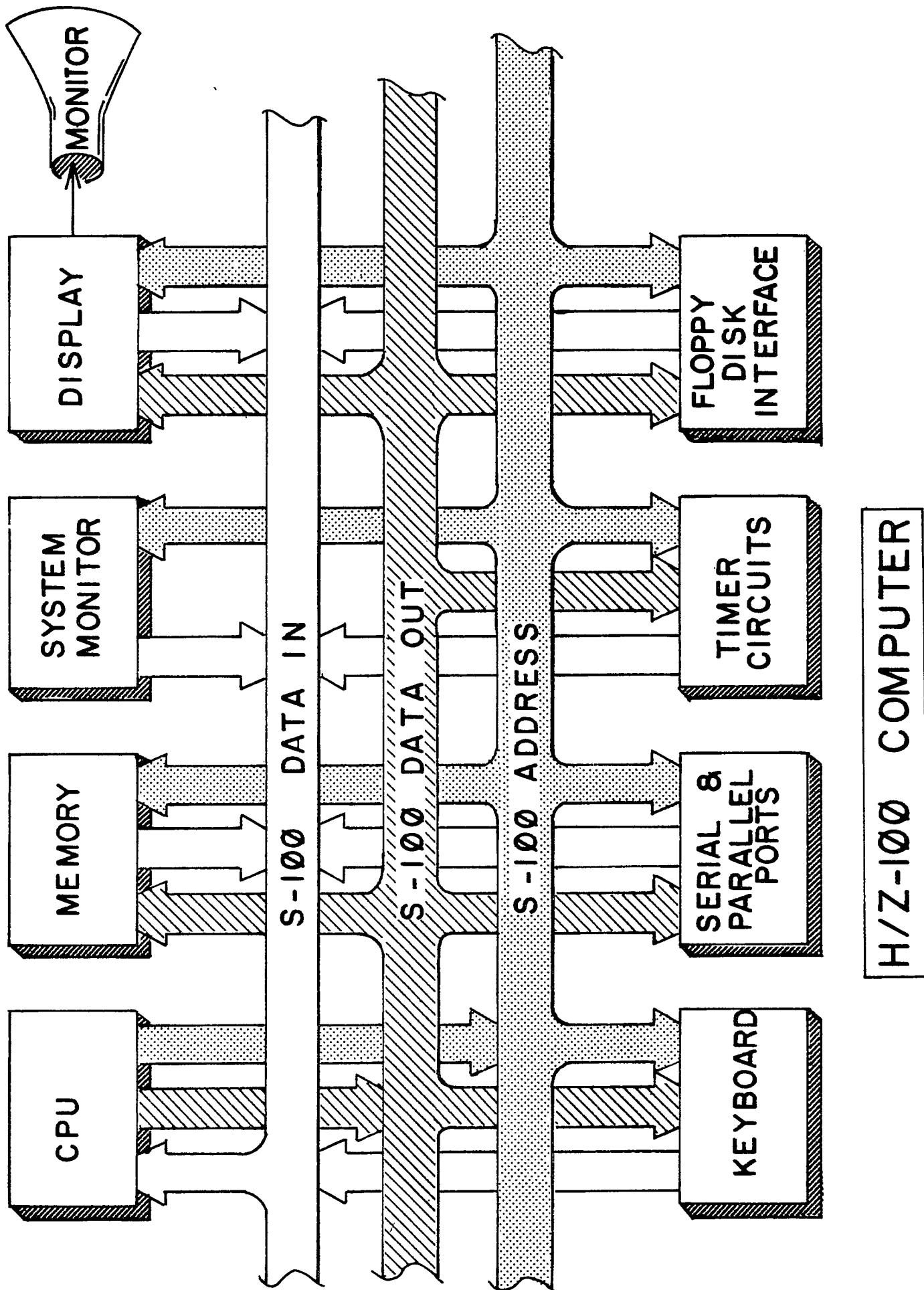
INTRODUCTION

This block diagram description will show you how the H/Z-100 operates as a system. It starts with the basic blocks and then analyzes what goes on in each block. Once you understand the operation on this level, go on to the circuit descriptions located in the appropriate section of the Blue Book.

The circuit descriptions are written on the level of the experienced microcomputer technician. If you're new to computers, we recommend that you study one of the computer courses available from Heath Company.

Even if you are an experienced computer technician, you may want to review the IC data sheets in the Data Sheets section of this book. The description explains the important features of the more complex ICs affecting circuit operation, but assumes that you know how the ICs work. This is necessary to keep the circuit description from drifting off its intended subject -- the H/Z-100.

Likewise, you should become familiar with the S-100 bus (IEEE-696). The description explains how and why certain lines are developed, but assumes that you're familiar with the bus pin-out and understand the mnemonics used. You can find a description of the S-100 bus in the Appendices section of this manual.



SYSTEM OVERVIEW

In this block diagram description, we'll cover the major circuits of the H/Z-100 Digital Computer. Though some of these block diagrams appear detailed, several buffers and gates have been left out to keep the illustrations from getting cluttered. As a result, you will see several circuits that appear to connect to the S-100 bus when they may actually be separated from the bus by an octal buffer. The block diagrams do show the buffers where the bus must be multiplexed or demultiplexed.

Basically, the H/Z-100 Digital Computer can be broken down to eight major blocks: The CPU, memory, system monitor, display, keyboard, serial & parallel ports, timer circuits, and the floppy disk interface board.

The CPU block consists of two microprocessors; an 8085 8-bit processor and an 8088 16-bit processor. The 8085 permits software compatibility with the existing body of 8080/8085 software while the 8088 provides greater computing power for new applications. Either CPU is software selectable. The 8088 CPU, however, is the active processor after power up or reset.

The memory block contains up to three 64-kilobyte banks of RAM for 192K of read/write memory. The memory circuits provide refresh to prevent data loss when the CPU isn't accessing memory. This block also has an arbitration circuit to ensure that refresh doesn't occur when the CPU is accessing RAM, and that the CPU won't access RAM while a refresh operation is taking place.

The system monitor takes control of the CPU after power up or reset. Through it, the CPU programs the I/O circuits to allow communicating with the user.

The display circuits provide a video graphics output from the computer. This can be monochrome or color. The display circuits can contain up to 192K of RAM; 64K for each primary color (red, green, blue). After reset, the system monitor programs the display circuits to print alphanumeric characters when the appropriate keyboard key is pressed. However, the display memory can be directly addressed by the CPU, permitting graphics.

The keyboard circuits are built around a dedicated micro-processor that interfaces the matrix keyboard to the CPU. Through software control, the keyboard can output either the normal ASCII character set, or a special event-driven character set for real-time applications. The keyboard circuits also contain oscillators for bell and key-click sounds.

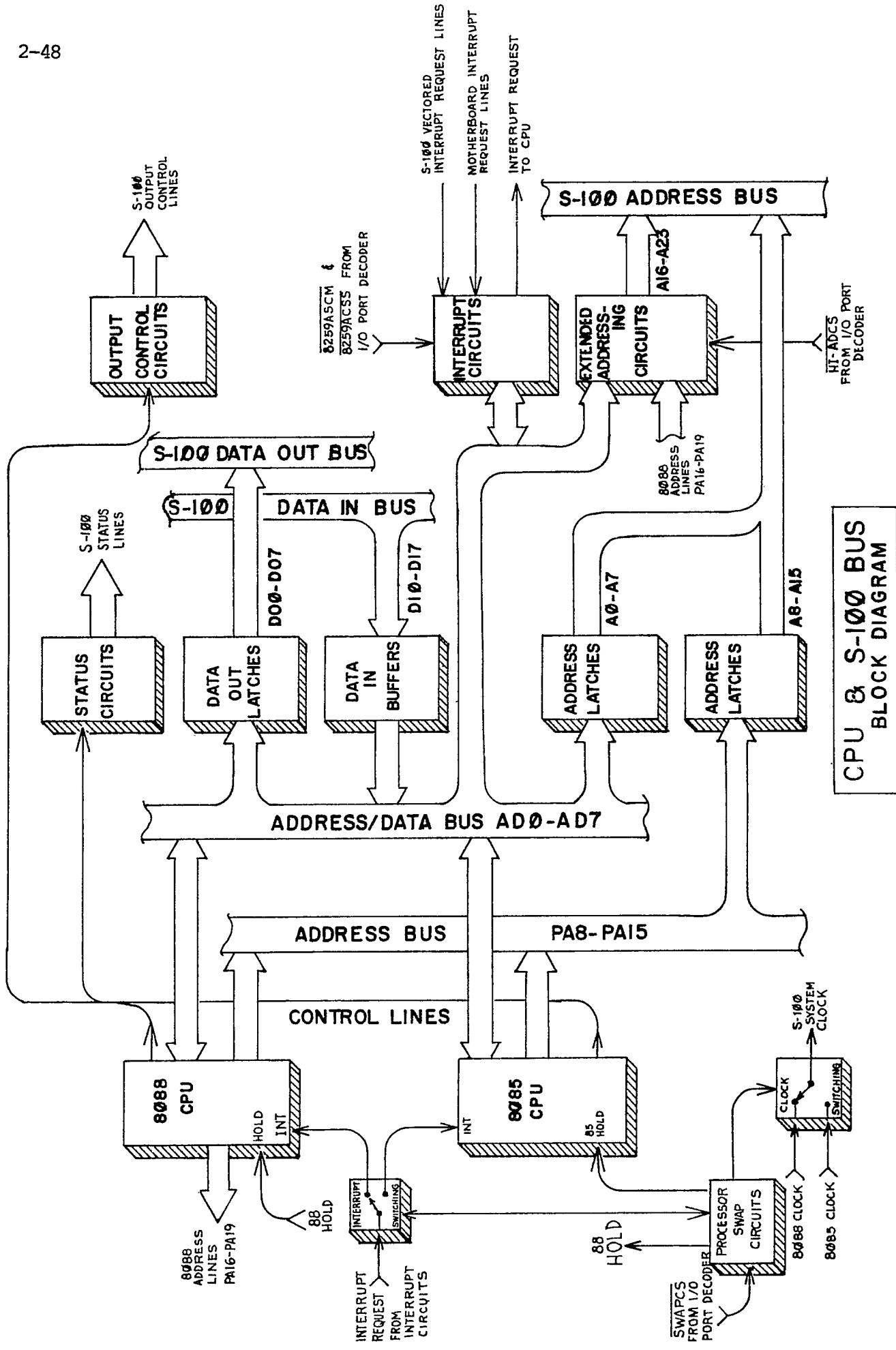
The serial and parallel ports permit the H/Z-100 to communicate with outside devices such as MODEMs, printers, and voice synthesizers.

The timer circuits contain programmable counters that the CPU can use for a real-time clock, a calendar, or for other events-related functions. This circuit has its own oscillator, so the CPU doesn't need to spend any time periodically updating the count.

The floppy disk interface permits connecting up to four 8" and four 5" floppy disk drives to the H/Z-100. This is the only circuit in this block diagram that plugs into the S-100 bus. Though the other circuits communicate through the S-100 bus, they are all located on either the motherboard or the video board. See the Disk Controller and Drives section of this Blue Book for more information on the interface board.

The block diagram also shows three of the major S-100 buses; data in, data out, and address. Both data buses are 8 bits wide; if the CPU fetches a 16-bit instruction, it transfers it a byte at a time. The address bus is 24 bits wide, allowing the CPU to directly address up to 16 megabytes of memory.

Note that the data directions are referenced to the CPU. Data from the top bus goes IN to the CPU. Data from the CPU goes OUT to memory or a port through the middle bus.



DETAILED LOOK

CPU AND S-100 BUS

READING AND WRITING DATA

The 8085 CPU is an 8-bit internal, 8-bit external processor. It is software compatible with the 8080 CPU and can directly address up to 64 kilobytes of memory. The 8088 CPU is a 16-bit internal, 8-bit external processor. It is software compatible with the 8086 CPU and can directly address up to 1 megabyte of memory. This is due to the extended-address lines, PA16-PA19.

Except for lines PA16-PA19, the 8088 address, data, and control lines function in the same manner as those of the 8085. The lower 8 bits of the address bus is multiplexed with the data bus. Whenever either CPU accesses memory, it first places the address on lines AD0-AD7 and PA8-PA15. This information is latched into the address latches shown in the lower center of the block diagram. The outputs of these latches connect to lines A0-A15 of the S-100 bus.

Next, if writing data, the CPU places the data onto lines AD0-AD7 and latches it into the data-out latch. The output of the latches connects to lines D00-D07 of the S-100 data output bus. When the data and address lines are stable, the CPU control lines activate certain lines in the status circuits and the output control circuits to write the data into the addressed memory location.

The operation is almost the same for reading from memory. In this case, however, once the address lines are stable, the status and output control lines will cause the addressed memory location to place the data byte onto the S-100 data-in bus. It is then coupled through the data-in buffers and loaded into the CPU.

EXTENDED ADDRESSING

The extended addressing circuits provide up to 16-megabyte addressing capability, in accordance with the IEEE-696 standards. It does this by latching data onto address lines A16-A23.

When the 8088 is active, the extended address lines couple the 8088 extended address lines, PA16-PA19, to A16-A19 of the S-100 bus. Thus the 8088 is able to access its normal 1-megabyte address space.

If the 8088 needs to address a location above 1 megabyte, it places the extended address values onto lines AD0-AD7 and asserts HI-ADCS from the I/O port decoder. The extended address circuits disconnect the PA16-PA19 lines and latch the value on AD0-AD7 onto A16-A23 of the S-100 bus.

When the 8085 is active, the extended addressing circuits are normally disabled; lines A16-A23 are zero so the 8085 is operating within the first 64K bank of memory.

If the 8085 needs to address a location above 64 kilobytes, it places the extended address values onto lines AD0-AD7. It then asserts HI-ADCS to latch this value onto A16-A23 of the S-100 bus.

PROCESSOR SWAP CIRCUITS

The processor swap circuits handle all the switching necessary to disable one CPU and enable the other. It is activated by asserting SWAPCS from the I/O port decoder and sending a control word from the active CPU to the swap circuits.

The swap circuits switch CPUs by asserting the proper HOLD line. For example, if switching from the 8085 to the 8088, the 85HOLD line will go high to disable the 8085, and the 88HOLD line will go low to enable the 8088.

The swap circuits also determine whether the 8088 clock or the 8085 clock is coupled to the S-100 system clock line. Although these 5-MHz clocks are crystal controlled, they aren't in phase. To ensure that a spike doesn't occur, the clock switching circuits hold the system clock line at its previously-valid logic state until the incoming signal matches it.

For example, if the system clock is logic one when the H/Z-100 swaps from the 8085 to the 8088, it will remain high until the 8088 clock is logic one. Once this occurs, the 8088 clock is allowed to pass to the S-100 system clock line.

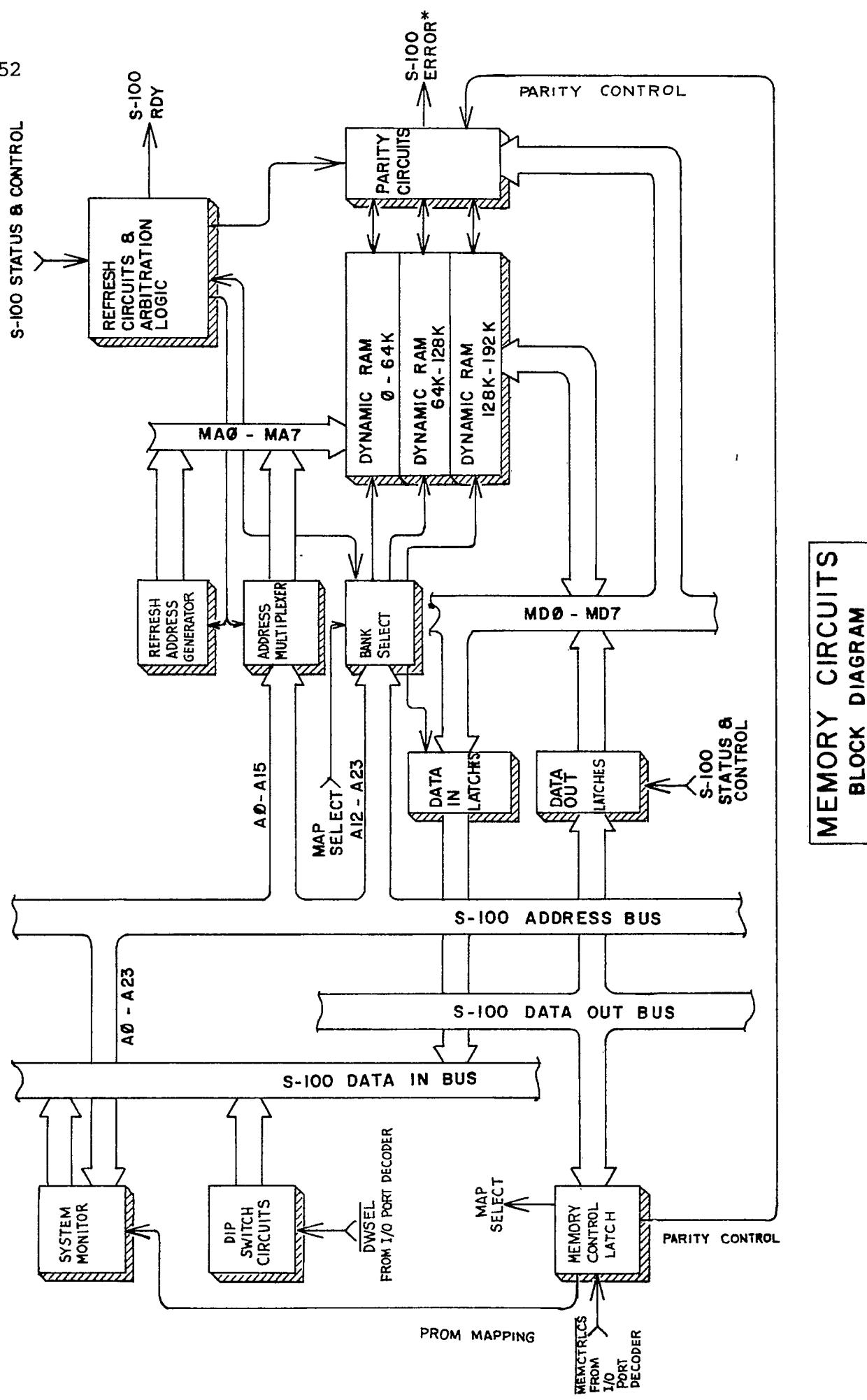
The processor swap circuits also control the interrupt switching circuits. These circuits ensure that any interrupt request is routed to the currently-selected processor. These circuits also have a masking feature that forces the 8088 to handle all interrupts.

If, for example, the 8085 is active and the mask mode is selected, the 8085 will continue to operate until an interrupt request occurs. The interrupt switching circuits cause the processor swap circuits to disable the 8085 and enable the 8088. The interrupt switching circuits then route the interrupt request to the 8088. After the interrupt is processed, it is up to the interrupt-handler program to return control to the 8085.

INTERRUPT CIRCUITS

The interrupt circuits monitor various circuits on the motherboard and notify the CPU if any of the circuits have data that requires immediate attention. These circuits include the various I/O ports, the timer, and memory parity. Also, the interrupt circuits monitor the vectored interrupt lines which are used by S-100 boards, such as the Z-207 floppy disk interface board.

The interrupt circuits are programmable through the address/data bus and the chip-select lines, 8259ACSM and 8259ACSS. Programming options include: masking out unwanted interrupts, selecting the interrupt priority, and setting up the pointer to the interrupt-handling routine.



MEMORY CIRCUITS

SYSTEM MONITOR

The system monitor is an 8K ROM that can be relocated in memory through software control. This is done by the PROM mapping signal from the memory control latch. The memory control latch is programmed by sending it a control word from the CPU and asserting the MEMCTRLCS line from the I/O port decoder.

There are four relocating options available to the system monitor:

Option 0 makes the ROM appear to be in all memory locations whenever a memory read is performed. Memory writes still take place normally. This is the option selected immediately after power-up/reset. The 8085 is in control of the H/Z-100, switches to the 8088, and then selects Option 2 for the system monitor.

Option 1 puts the ROM at the top 8K of every 64K page of memory. This is useful for the 8085, which has only a 64K natural address space.

Option 2 gates the ROM to appear in the top 8K of the 8088's natural 1 megabyte address space. This is the normal operating option when the 8088 has control of the H/Z-100.

Option 3 disables the ROM. The ROM is not accessible when this mode is selected.

When the ROM is selected, all other memory (except video RAM) is disabled. This allows other memory to share the ROM's address space using the S-100 PHANTOM line.

After reset, the monitor tests the status of the dip-switch circuits to set up the H/Z-100 default operating modes. See the Configuration section of this Manual for the various configurations.

DYNAMIC RAM

Read/write memory consists of three 64K banks of dynamic RAM. This permits a total of 192K of onboard memory.

The proper memory location is selected by the combination of the address multiplexer and the bank select circuits. The S-100 address bus couples lines A0-A15 to the address multiplexer and lines A12-A23 to the bank select.

The bank select tests to see if the address is within the 192K address range. If so, it selects one of the three 64K banks. It does this by first asserting the appropriate row address strobe (RAS), followed by asserting the column address strobe (CAS).

When RAS asserts, the address multiplexer places lines A0-A7 onto memory address lines MA0-MA7, which are then latched into the row address registers in memory. When CAS asserts, the address multiplexer places lines A8-A15 onto MA0-MA7. This, plus the row address, points to the correct location in memory.

If the CPU is reading data from memory, the memory circuits will place the addressed byte on the memory data bus, MD0-MD7. Next, the bank select circuits enable the data-in latch to couple the data to the S-100 data-in bus.

If the CPU is writing data to memory, the appropriate S-100 status and control lines enable the data out latches to couple the data to MDO-MD7. From there, the data is written into the correct memory location.

Like the system monitor, portions of the dynamic memory can be relocated to different addresses. There are four options available, these include:

Option 0 is the normal configuration. This mode provides contiguous addressing to all of the memory.

Option 1 swaps the 0-48K segment with the segment between 64K-112K. This could be used for MP/M when running the 8085 processor.

Option 2 swaps the 0-48K segment with the segment between 128K-176K. This could also be used with MP/M and the 8085.

Option 3 swaps a 56K segment located between 4K-60K with a segment located between 68K-124K. This can be used to build an advanced disk operating system for CP/M-85.

REFRESH AND ARBITRATION LOGIC

The refresh circuits keep the dynamic RAM from losing its contents when the CPU isn't accessing a specific location. When the refresh circuits have control of memory, it disables the address multiplexer and enables the refresh address generator. The refresh address generator, a binary counter, places an 8-bit refresh address onto MA0-MA7.

At the same time, the refresh circuits send a control signal to the bank select circuit that forces it to enable all three memory banks. Subsequently, the same relative memory address is refreshed in each bank. When finished, the refresh circuits disable the refresh generator, increment its address count, and restore the address multiplexer and bank select circuits to normal operation.

The arbitration circuits determine if the refresh circuits or the CPU is to have control of the dynamic memory circuits. If the CPU is accessing memory when the refresh circuits attempt to refresh the RAM, the arbitration circuits will halt the refresh operation until the CPU is done.

Likewise, if the CPU attempts to access memory during the middle of a refresh operation, the arbitration circuits will stop CPU operation until refresh is completed. It does this by placing a logic zero on the S-100 RDY line. This line couples back to the active CPU to place the CPU into a wait state. While in a wait state, all of the CPUs register and signal lines do not change states; thus maintaining the processor's last valid status.

When the refresh circuit is finished refreshing the RAM, it brings the RDY to logic one. The CPU continues where it left off.

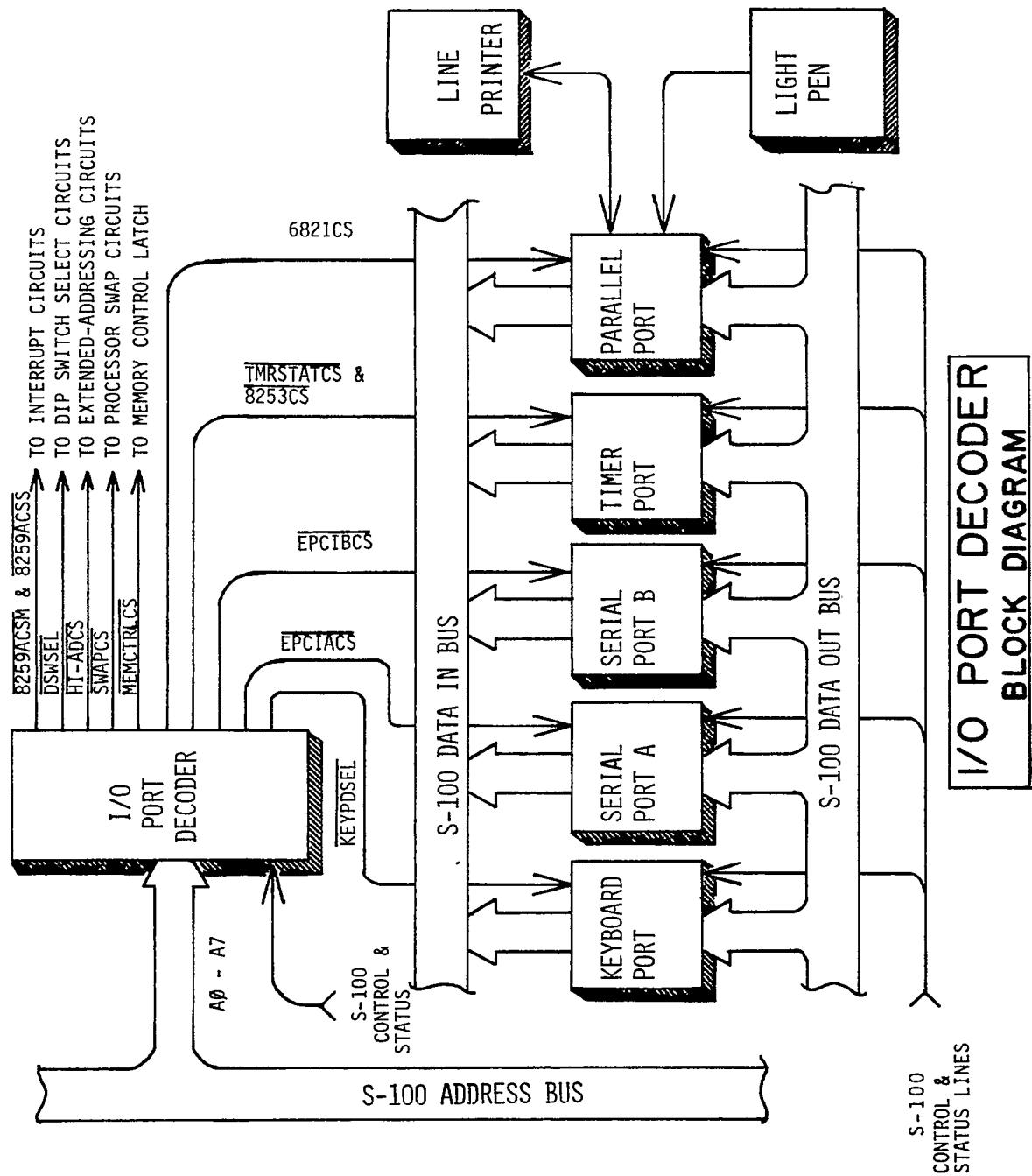
PARITY CIRCUITS

The parity circuits monitor the number of bits written into each byte of memory. If the number of bits are odd, the parity circuits adds a logic one to the count and stores it in parity RAM. Otherwise, it stores a logic zero in parity RAM. Parity RAM consists of a 64K x 1-bit RAM IC for each 64K x 8 memory bank.

When the CPU reads a memory location, the parity circuits count the number of bits in the 8-bit RAM location and adds it to the bit in the equivalent location in parity RAM. If the result is still even, everything is okay. However, if the total number of bits are odd, due to a bad memory chip for example, the parity circuits will assert the S-100 ERROR* line.

In turn, the ERROR* signal will send an interrupt request to the CPU. It is up to the user's program to process the interrupt.

The parity control line, from the memory control latch, allows you to disable the parity circuits, or to force a parity error for test purposes. In addition, a control line from the refresh circuits ensures that a parity error isn't generated during a memory write or a refresh.



I/O PORT DECODER

GENERAL

The I/O port decoder provides enable lines to the data and control ports on the H/Z-100 motherboard. Each enable line is asserted by placing an address on A0-A7 of the address bus and asserting the appropriate S-100 control and status lines. The I/O port decoder responds by asserting the correct enable line.

The following lines have been discussed previously: 8259ACSM & 8259ACSS, DSWSEL, HI-ADCS, SWAPCS, and MEMCTRLCS. Refer to the appropriate block diagram description to see how these work.

The remaining lines control data transfer ports. This is done in conjunction with control and status signal from the S-100 bus.

KEYBOARD

The keyboard port contains an 8041A UPI, a dedicated microprocessor that handles all keyboard processing. When a key is pressed, the UPI determines which key it was, and sends the appropriate ASCII code to the computer. The UPI can also send an interrupt to the computer to tell it that it has a character ready. The program must provide the software to process this interrupt.

Through program control, you can change the ASCII code to a special code that sends out one byte pattern when the key is pressed, and another byte pattern when the key is released. This permits real-time applications. Other programming options include disabling the key-click, disabling the beep, and clearing the UPI's buffer.

To program the program processor, the CPU places the programming byte onto the S-100 data out bus and asserts KEYBDSEL. The appropriate S-100 control and status lines write the programming data into the keyboard circuits.

SERIAL PORTS A AND B

Serial ports A and B provide RS-232 communications between the computer and the outside world. These ports feature programmable baud rate, synchronous or asynchronous operation, optional parity testing, and character transmission length.

Serial port A uses a DCE connector and can be used for an asynchronous device such as a printer.

Serial port B uses a DTE connector to connect to external devices. This port can be used for synchronous devices such as a MODEM.

Both ports can be polled or interrupt-driven. In a polled operation, for example, the CPU constantly checks the port's status register to see if it has received a data byte. If interrupt-driven, the CPU can be performing other tasks until the port has a character ready for transfer. When it does, the port sends an interrupt request to the CPU. If programmed to do so, the CPU finishes its current instruction and responds to the interrupt request.

TIMER PORT

The timer port contains an 8-bit counter and a 16-bit counter. These are driven by a 250-kHz crystal-controlled clock that is independent of the system clock. The timer circuits allow the CPU to perform other tasks, instead of spending time counting through a loop.

The CPU can load a starting count through the S-100 data out bus and, through software control, check the count through the S-100 data in bus. One application would be to translate the count into time-of-day or the date.

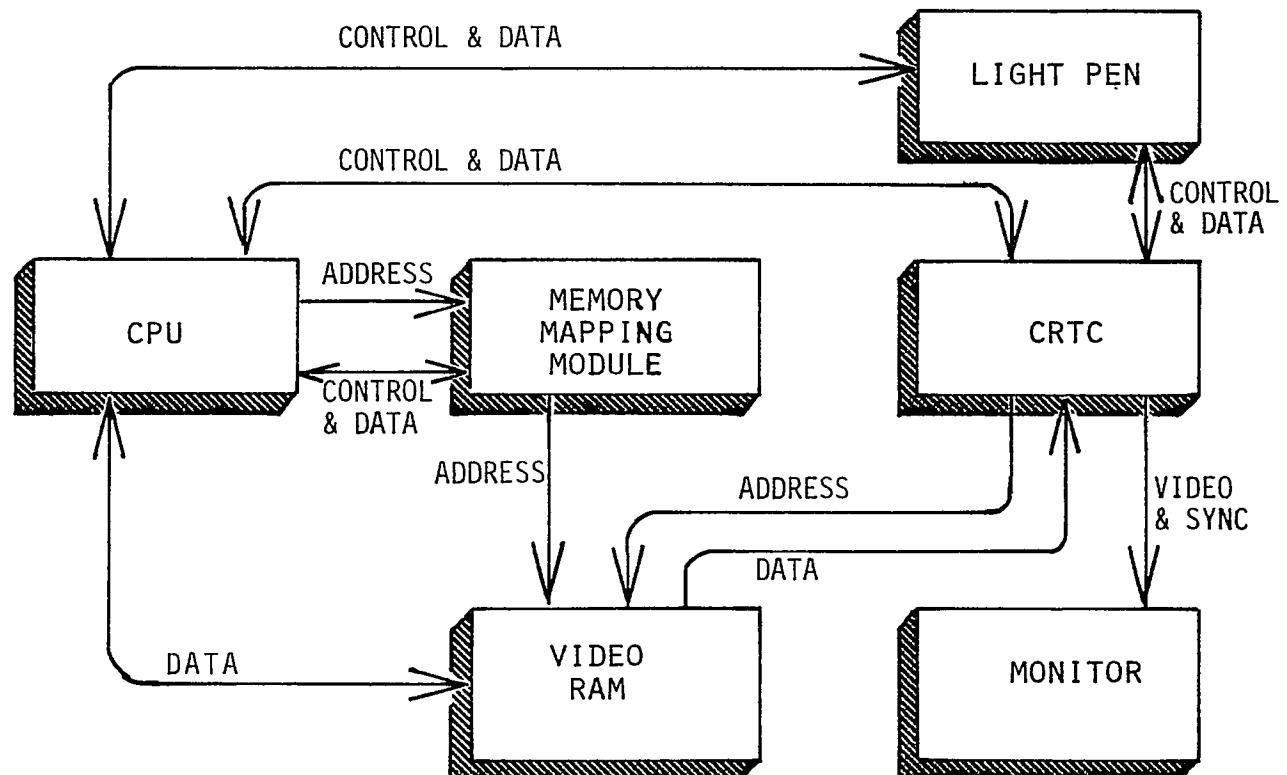
The timer will also generate an interrupt when it counts down from the preloaded number to zero. The CPU can use this for real-time applications such as displaying the total time on line, at one-second intervals, when running a MODEM program.

PARALLEL PORT

The parallel port processes two major I/O circuits: a line printer port and a light pen port. Not shown is an interrupt line from the video board.

The line printer port provides 8-bit parallel data output plus full handshaking. This port allows interfacing to some of the more popular line printers without having to buy a serial-to-parallel converter.

The light pen port permits using a light pen with the H/Z-100. When the light pen is placed near the CRT and detects a pixel, it strobes the CPU and the video board. Circuits on the video board store the location of the detected pixel. The user must supply the software to process this information (such as moving the pixel or drawing a picture).



**BASIC VIDEO CIRCUITS
BLOCK DIAGRAM**

BASIC VIDEO CIRCUITS

The CPU can access the video circuits as either a port or as a memory location. The CPU accesses the video circuits as a port to program the CRTC, and as a memory location to set up the character font or perform high-density graphics.

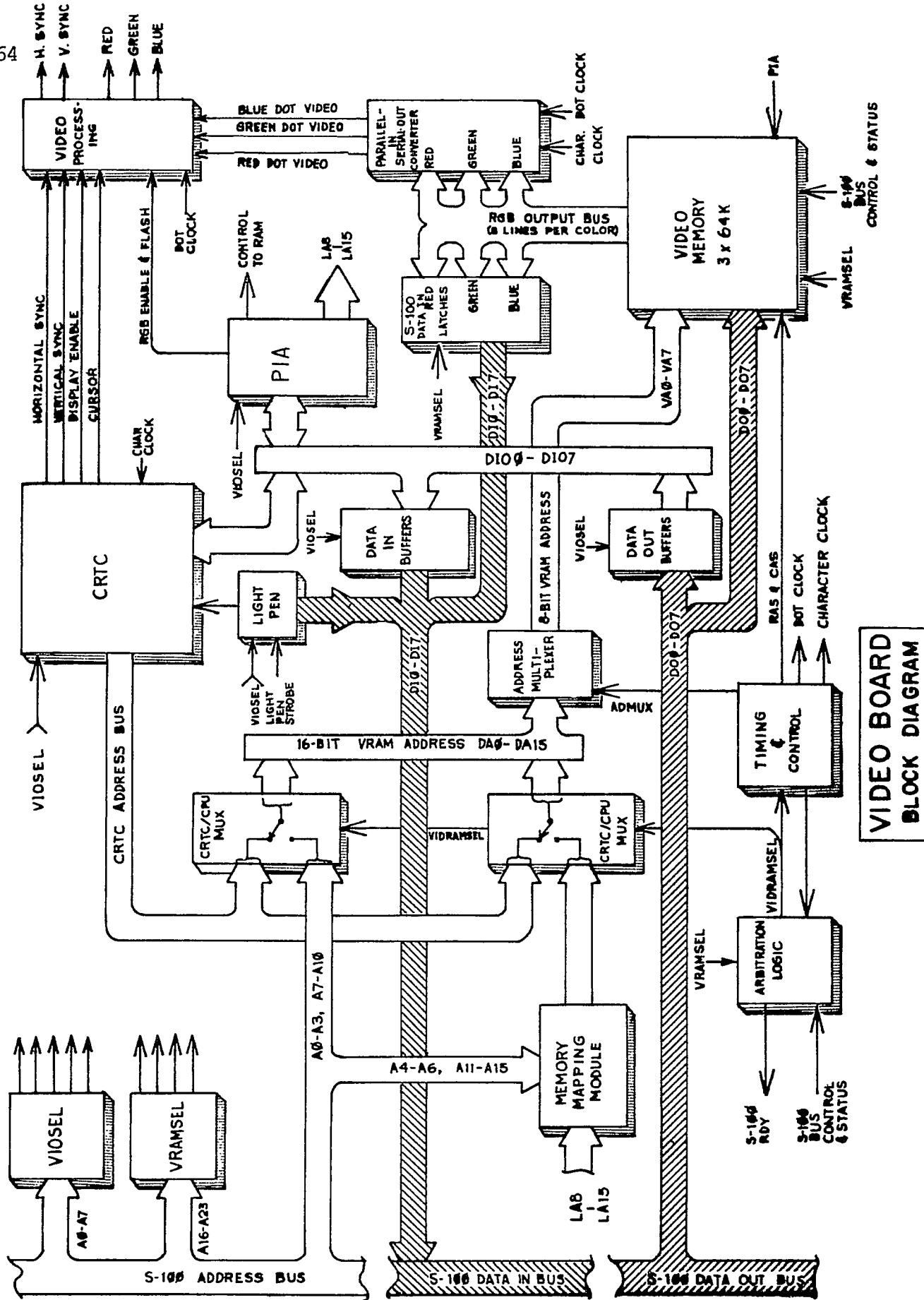
The CPU sends programming information to the CRTC along the control and data signal path. This information includes the number of characters and lines to be displayed, the scan rate, and cursor location.

Once programmed, the CRTC sequentially addresses the video RAM to fetch a character, convert it to serial, and send it to the monitor. The address counter increments, fetches the next character data, and the cycle repeats.

To write or read video memory, the CPU first programs the memory mapping module through the address and the control & data lines. The mapping module is necessary because the CRTC sees the VRAM address starting at zero and going to 64K, while the CPU sees the VRAM address starting at 744K and going to 936K. Once the mapping module is set up, the CPU can, for example, write a byte to 744K and the mapping module will send it to the same location that the CRTC sees as address 0.

The light pen circuits consist of the interface circuits discussed earlier and some counters on the video board. These registers hold the exact location of the pixel pointed to by the light pen.

Because of the complexity of the video board, we will discuss it in more detail.



VIDEO BOARD

PROGRAMMING THE CRTC

The CPU programs the CRTC by asserting the appropriate VIOSEL line. VIOSEL is a port decoder that selects the right video port by monitoring address lines A0-A7. Programming data couples through the S-100 data out bus, the data out buffers, bus D100-D107, to the CRTC.

Similarly, the CPU can read certain CRTC registers through the S-100 data in bus and the data in buffers.

CRTC OPERATION

Once programmed, the CRTC sends the video RAM address to the CRTC/CPU address multiplexers. These multiplexers are normally in the address shown; that is, they couple the CRTC address to the 16-bit VRAM address bus, DAO-DA15.

The 16-bit VRAM address bus connects the CRTC address to the address multiplexer. This circuit, under control of the ADMUX line, places the address onto the VRAM address bus, VA0-VA7, 8 bits at a time. At the same time, the timing & control block sends a RAS and CAS signal to the video memory to load each half of the 16-bit address into the row and column latches.

The video RAM is made up of three 32K x 8 banks located 64K apart. These banks can be expanded to 64K; however, this isn't supported at this time. There is one bank for each primary color; red, green, and blue. The minimum configuration for monochrome only has memory in the green bank. Otherwise, all three banks are filled.

The CRTC can only read video RAM, and it addresses all three banks at once. When the address lines are stable, the byte(s) are placed on the RGB output bus. There are 8 bus lines for each color.

The RGB buses connect to the CPU data-in latches, which are disabled, and to the parallel-to-serial converters. This circuit loads the parallel data in at the character clock rate and serially shifts it out at the dot clock rate (dot clock = 8 x character clock). The three serial dot video lines enter the video processing circuits.

At the same time the CRTC is addressing memory, it is also generating horizontal and vertical sync, blanking, and cursor information. These signals are also coupled to the video processing circuits where they are retimed to match the dot video data.

From here, these signals go through buffers to an RGB color monitor for display. Also, there are circuits to combine these pulses into a composite signal for output to a monochrome monitor.

A set of control lines also go to the video processing circuits. These are the RGB enable and flash lines. The RGB enable lines allow selectively turning off a particular color, while the flash line forces the screen to become a solid color. The exact color depends on what primary colors are enabled by the RGB enable line.

These enable lines are controlled by the PIA. In turn, the PIA is controlled by the CPU in the same manner that the CPU programs the CRTC. That is, one of the VIOSEL lines selects the PIA and the CPU reads or writes data through the DIO0-DIO7 bus.

ACCESSING THE VRAM WITH THE CPU

When the CPU reads or writes video RAM, it asserts the lines from the VRAMSEL block. This block activates the appropriate gates and enables the desired color bank in memory. VRAMSEL does this by monitoring address lines A16-A23, which ensures that the address will always be an even 64-kilobyte boundary between 744K and 936K.

The CPU first programs lines LA8-LA15 of the PIA for a specific mapping pattern. The mapping pattern is fed to the memory mapping module where it is compared to address lines A4-A6 and A11-A15. The memory mapping module connects to one of the CRTC/CPU multiplexers. Address lines A0-A3 and A7-A10 connect directly to the other multiplexer.

When the CPU attempts to read or write memory, one of the VRAMSEL lines sends a request to the arbitration logic. The CRTC has top priority, so if the CRTC is accessing memory, the arbitration logic puts the CPU into a wait state by bringing S-100 RDY low.

When the CRTC is done, the arbitration logic activates VIDRAMSEL to switch the CRTC/CPU multiplexers to the CPU position. The mapped address couples through the address multiplexer to the RAM in the same manner as described for the CRTC.

- ' If the CPU is writing data, it couples the data through D00-D07 to the memory circuits. It selects the correct bank with VRAMSEL. If reading data, the addressed byte(s) are placed on the RGB output bus and the CPU selects one of the three groups of CPU latches. The VRAM data couples to D10-D17 of the S-100 data in bus.

TIMING AND CONTROL

The ADMUX, RAS, and CAS timing was previously explained. The timing and control circuits also provide dot clock and character clock timing. The dot clock, at 14.112 MHz, is the basic timing frequency for the video board.

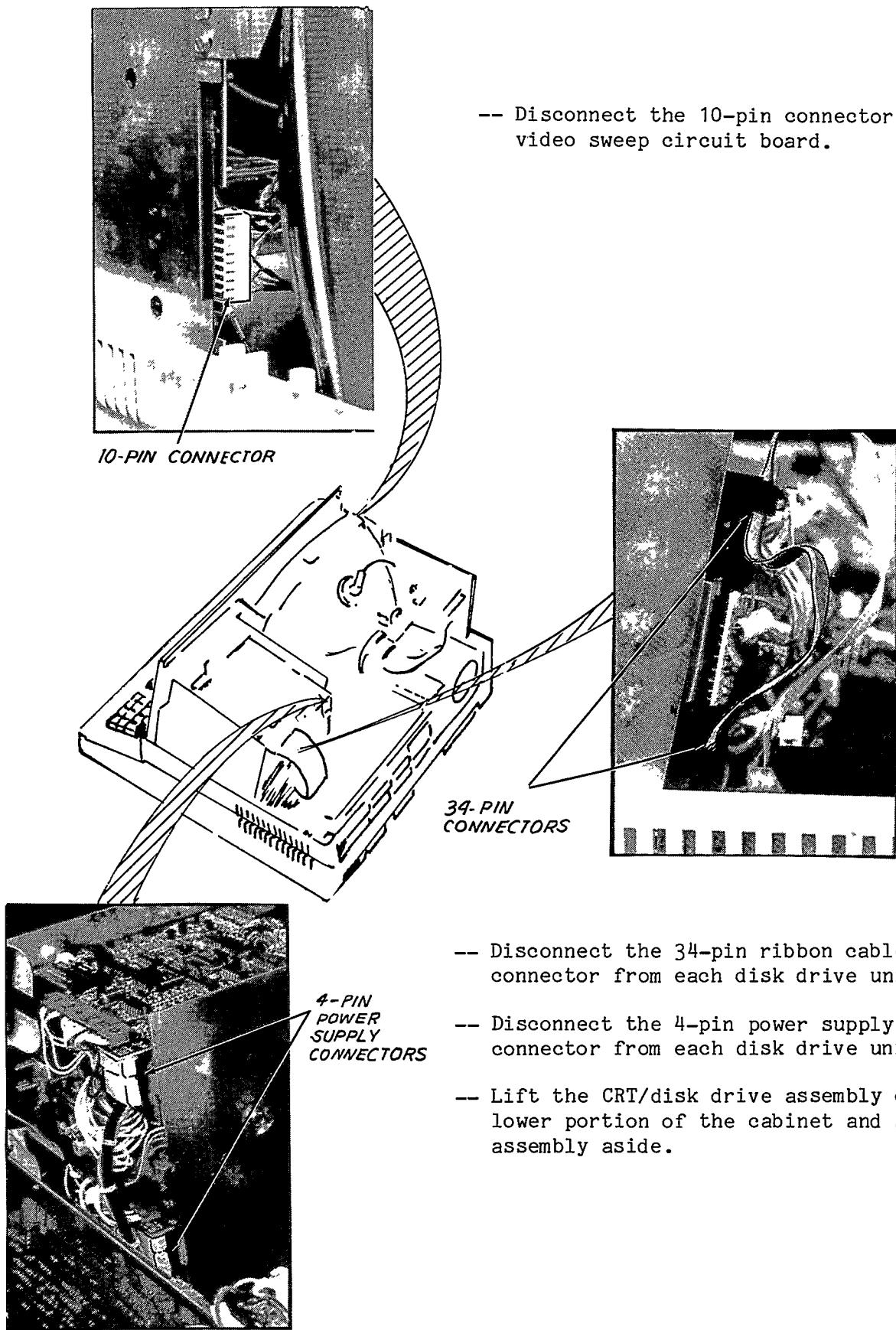
The timing circuits also provide a control signal to the arbitration logic. The video circuits are designed to let the CRTC have control of the video board for two RAS cycles, and let the CPU have control for the third cycle. The line from the timing block to the arbitration block tells the arbitration block when it can give the CPU control of the video circuits.

If the CPU isn't requesting control at this time, then nothing happens until the next RAS cycle, at which time the CRTC again has control of the board.

If the CPU is requesting control of the video board, indicated by VRAMSEL and signals on the S-100 bus control and status lines, the CPU will get control of the video board as described previously.

DISASSEMBLY

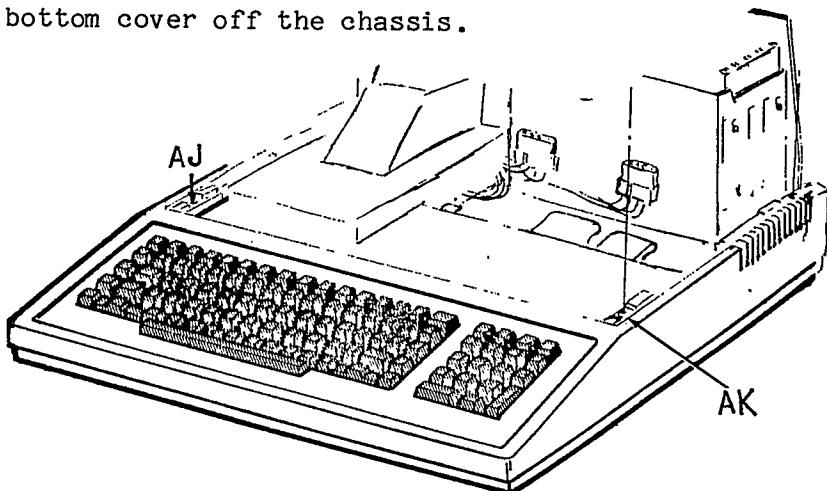
ALL-IN-ONE COMPUTER	
Cabinet Top Removal	2-71
CRT/Disk Drive Removal	2-72
Bottom Cover Removal	2-74
Keyboard Removal	2-74
Video Board Removal	2-75
Power Supply Removal	2-76
Motherboard Removal	2-77
LOW-PROFILE COMPUTER	
Cabinet Top Removal	2-78
Disk Drive Assembly/Bottom Cover Removal	2-79
Keyboard Removal	2-80
Video Board Removal	2-81
Power Supply Removal	2-82
Motherboard Removal	2-83



BOTTOM COVER REMOVAL

-- Remove the two #8 x 5/8" screws at AJ and AK.

-- Lift the bottom cover off the chassis.

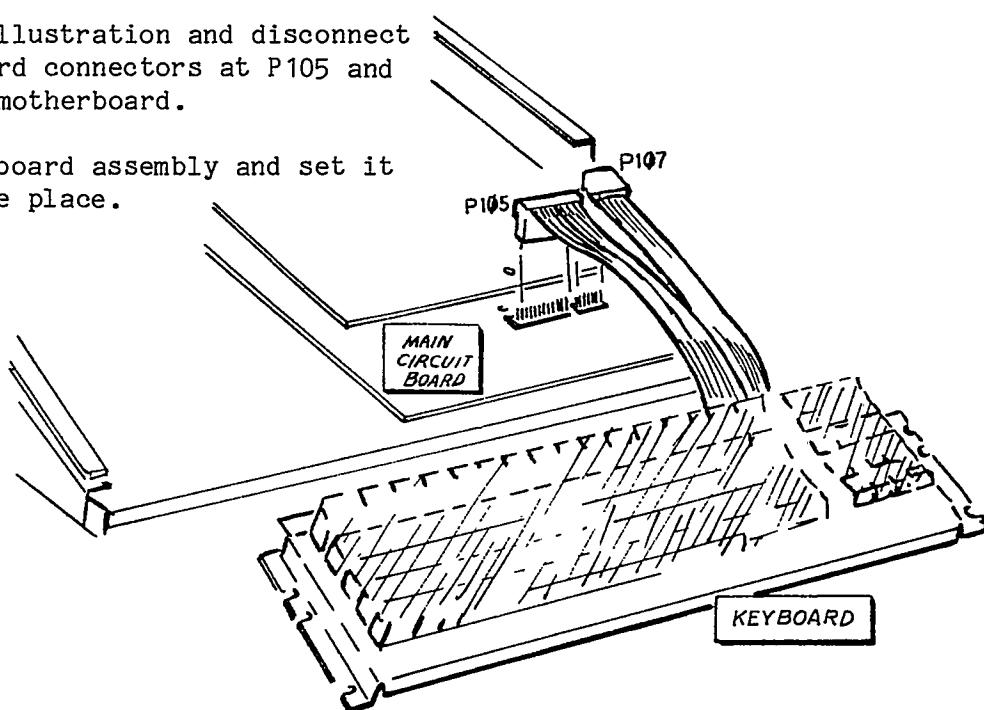


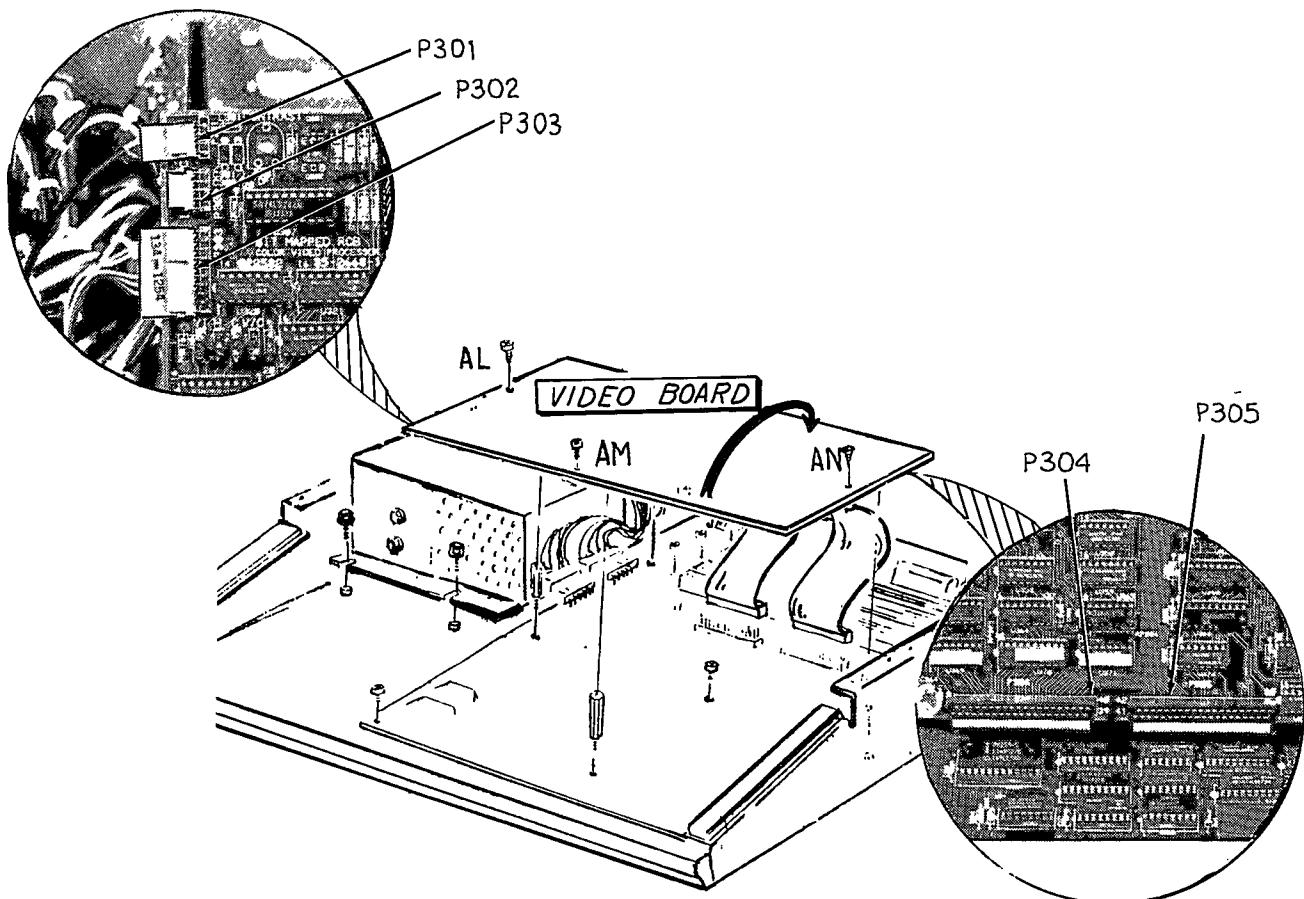
KEYBOARD REMOVAL

-- Place the keyboard in front of the chassis.

-- Refer to the illustration and disconnect the two keyboard connectors at P105 and P107 from the motherboard.

-- Remove the keyboard assembly and set it aside in a safe place.





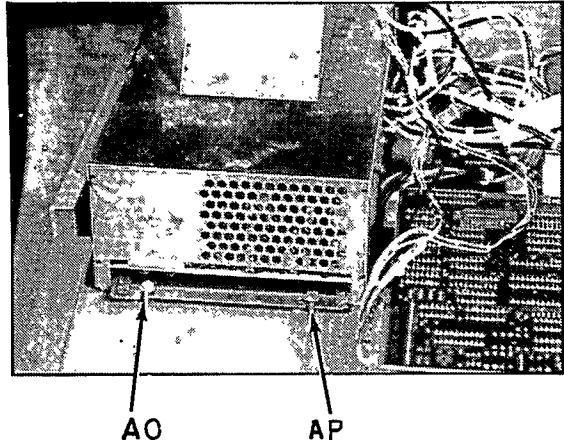
VIDEO BOARD REMOVAL

- Remove the three 4-40 x 1/4" phillips screws at AL, AM, and AN on the video board.
- Carefully lift the video board by the front edge to a vertical position.
- Disconnect the three cable connectors at P301, P302, and P303.
- Disconnect the two 40-pin cable connectors at P304 and P305 on the video board.
- Carefully lift the video board from the chassis.

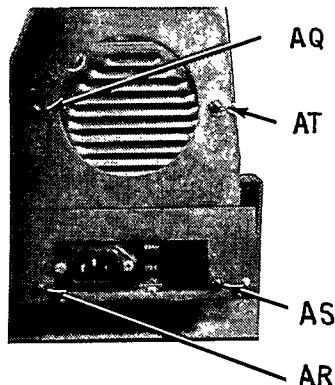
Depending on your servicing needs, the power supply and/or the motherboard may be removed from the chassis. Find the appropriate procedure and follow the instructions.

POWER SUPPLY REMOVAL

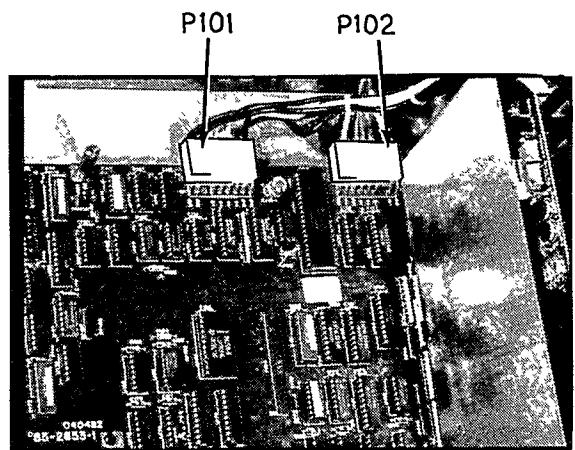
- Remove the two 6-32 x 3/8" hex-head screws from the front of the power supply at AO and AP.



- Remove the four #6 x 1/4" screws at AQ, AR, AS and AT that secure the power supply to the back panel.

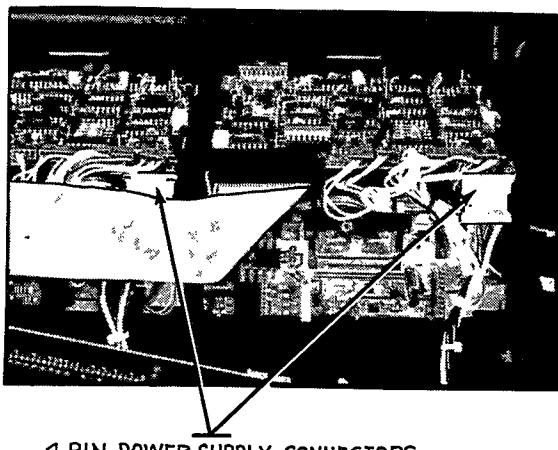
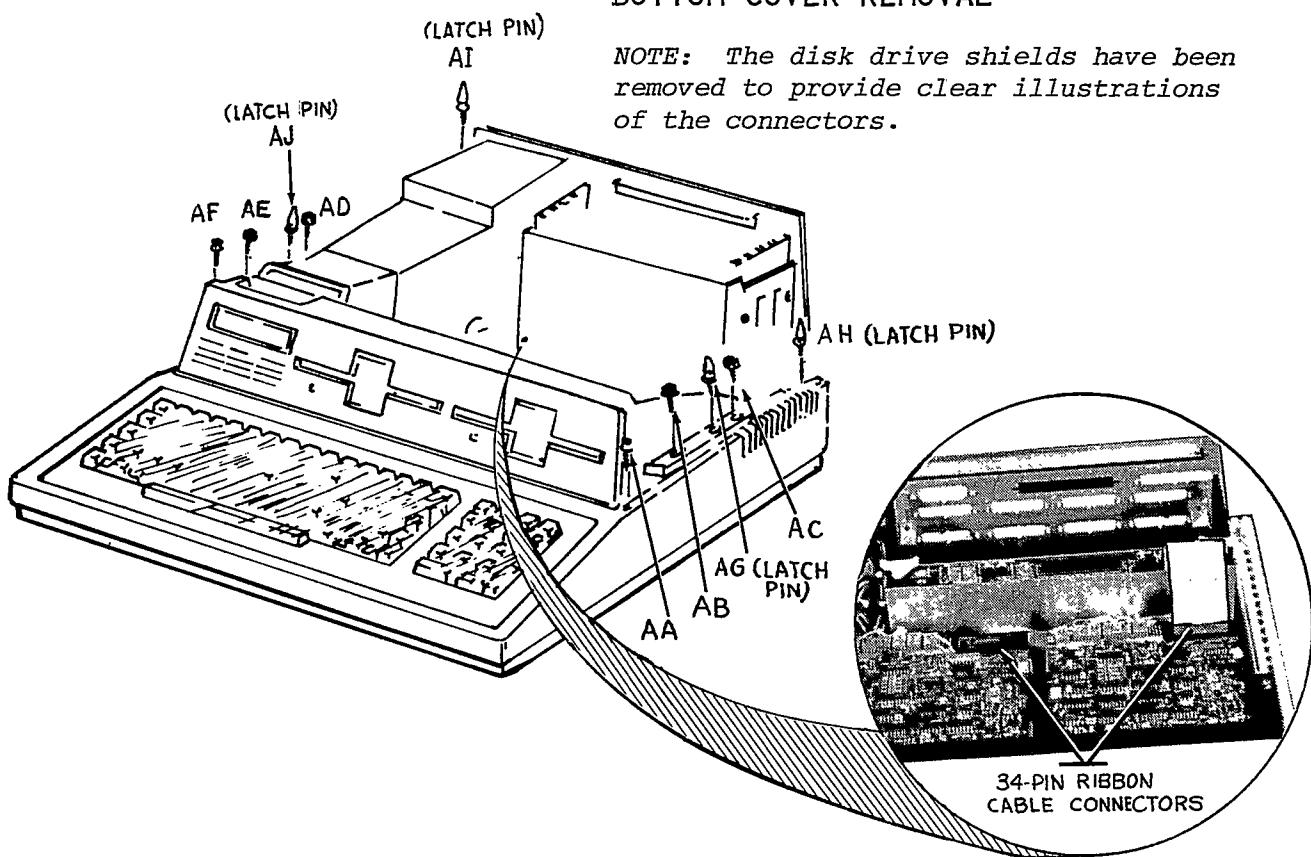


- Lift the power supply until you are able to disconnect the two power supply connectors P101 and P102 from the motherboard.
- Remove the knob on the brightness control by pulling it straight off the control shaft.
- Remove the control nut from the brightness control.
- Find the large toothed washer on the brightness control and set it aside in a safe place.
- Carefully remove the power supply from the chassis.



DISK DRIVE ASSEMBLY/ BOTTOM COVER REMOVAL

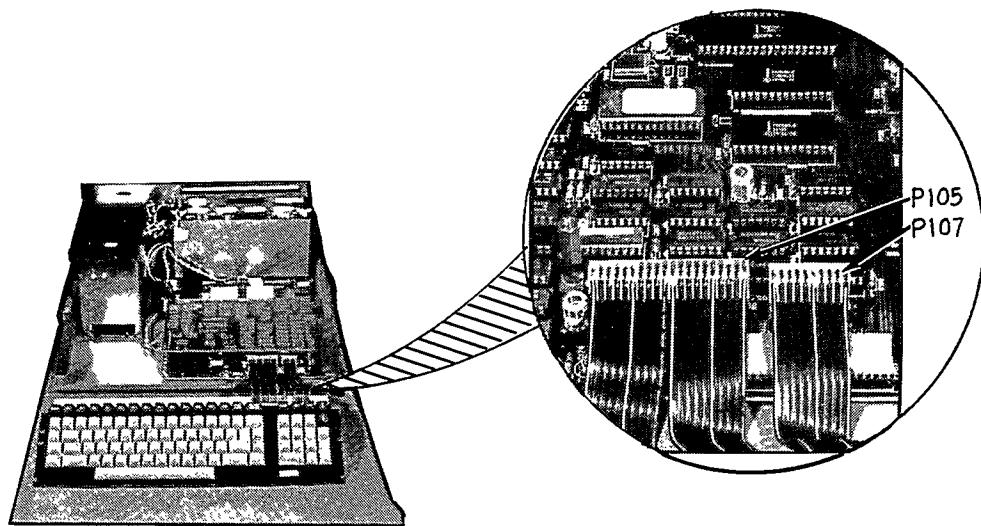
NOTE: The disk drive shields have been removed to provide clear illustrations of the connectors.



4-PIN POWER SUPPLY CONNECTORS

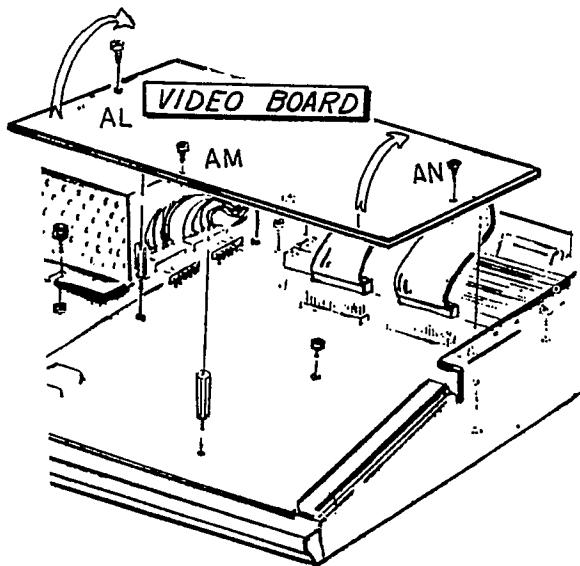
- Remove the six #8 x 3/4" screws at AA, AB, AC, AD, AE, and AF.
- Remove the four latch pins at AG, AH, AI, and AJ.
- Disconnect the 34-pin ribbon cable connectors from the disk drive units.
- Disconnect the 4-pin power supply connectors from the disk drive units.
- Lift the disk drive assembly off the lower portion of the cabinet.
- Lift the bottom cover off the chassis.

To further disassemble the disk drive assembly, refer to the Disassembly section of "Disk Controller and Drives."



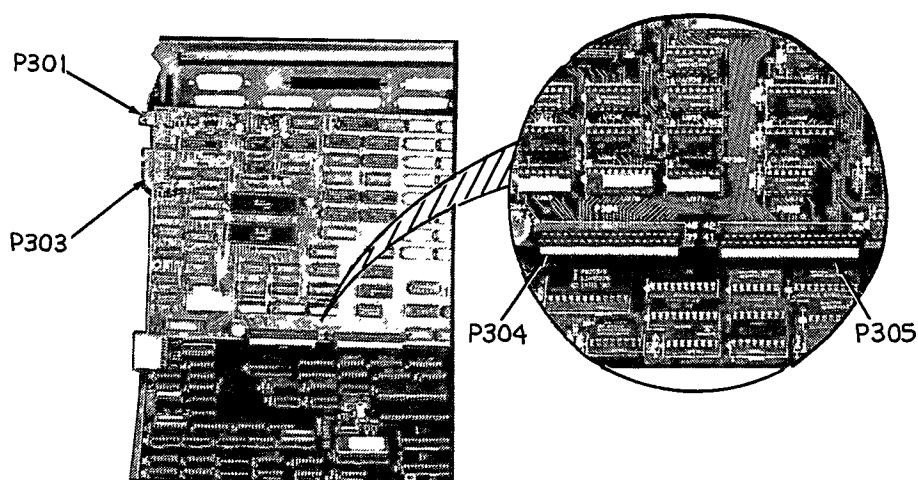
KEYBOARD REMOVAL

- Position the keyboard in front of the chassis as shown in the illustration.
- Refer to the inset, and disconnect the two keyboard connectors at P105 and P107 from the motherboard.
- Remove the keyboard assembly and set it aside in a safe place.



VIDEO BOARD REMOVAL

- Remove the three 4-40 x 1/4" phillips screws at AL, AM, and AN from the video board.

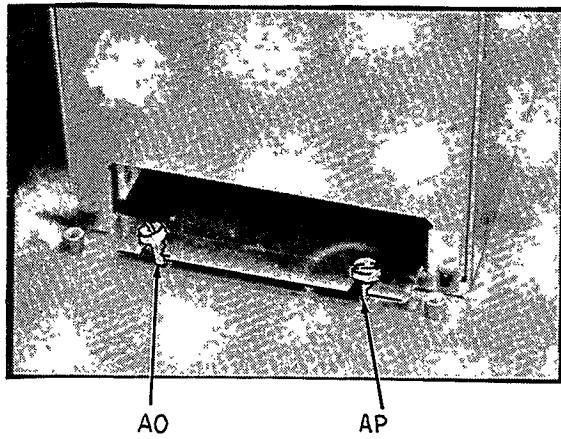


- Carefully lift the front edge of the video board so the board is in a vertical position.
- Disconnect the two cable assemblies at P301 and P303.
- Disconnect the two 40-pin cable connectors at P304 and P305 on the video board.
- Carefully lift the video board from the chassis.

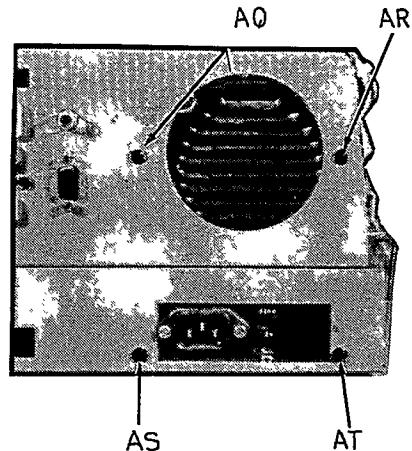
Depending on your servicing needs, the power supply and/or the motherboard may be removed from the chassis. Find the appropriate procedure and follow the instructions.

POWER SUPPLY REMOVAL

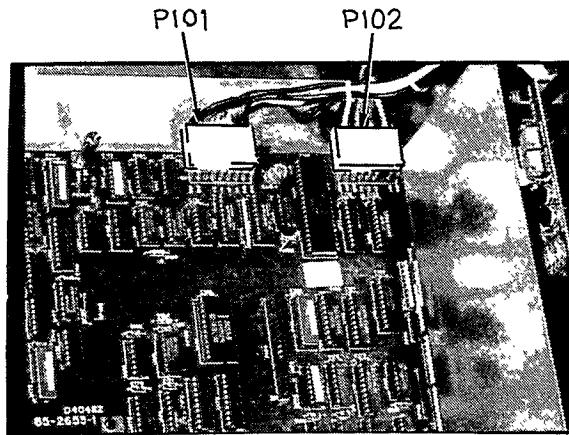
- Remove the two 6-32 x 3/8" hex-head screws at AO and AP from the front of the power supply.

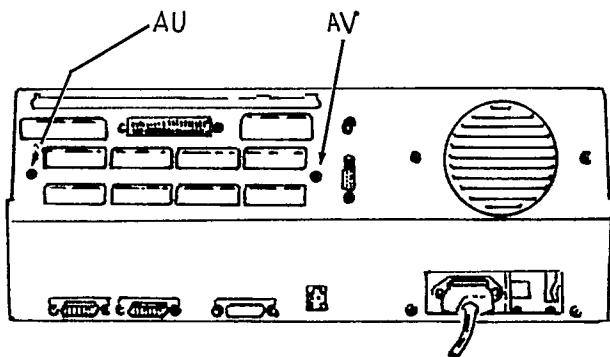


- Remove the four #6 x 1/4" screws at AQ, AR, AS, and AT that secure the power supply to the back panel.



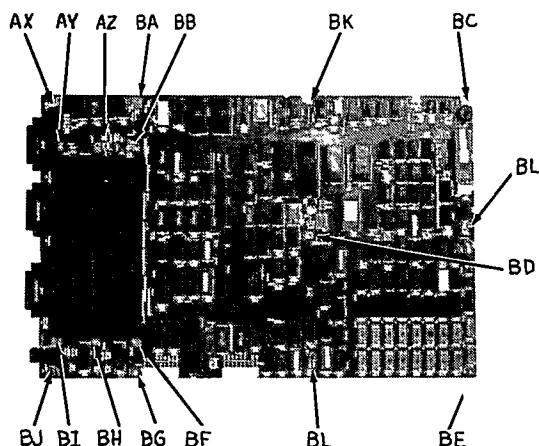
- Lift the power supply until you are able to disconnect the two power supply connectors P101 and P102 from the motherboard.
- Carefully remove the power supply from the chassis.



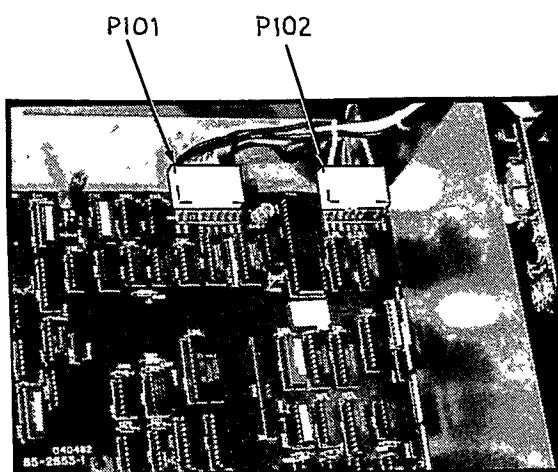


MOTHERBOARD REMOVAL

- Remove any accessory from the S-100 card cage.
- Remove the two #6 x 1/4" screws at AU and AV that secure the card cage to the back panel.



- With a phillips screwdriver, remove the thirteen 4-40 x 1/4" screws at AX through BJ from the motherboard.
- Lift the card cage from the motherboard.
- Remove the three 4-40 x 1" hex spacers at BK, BL, and BM from the motherboard.

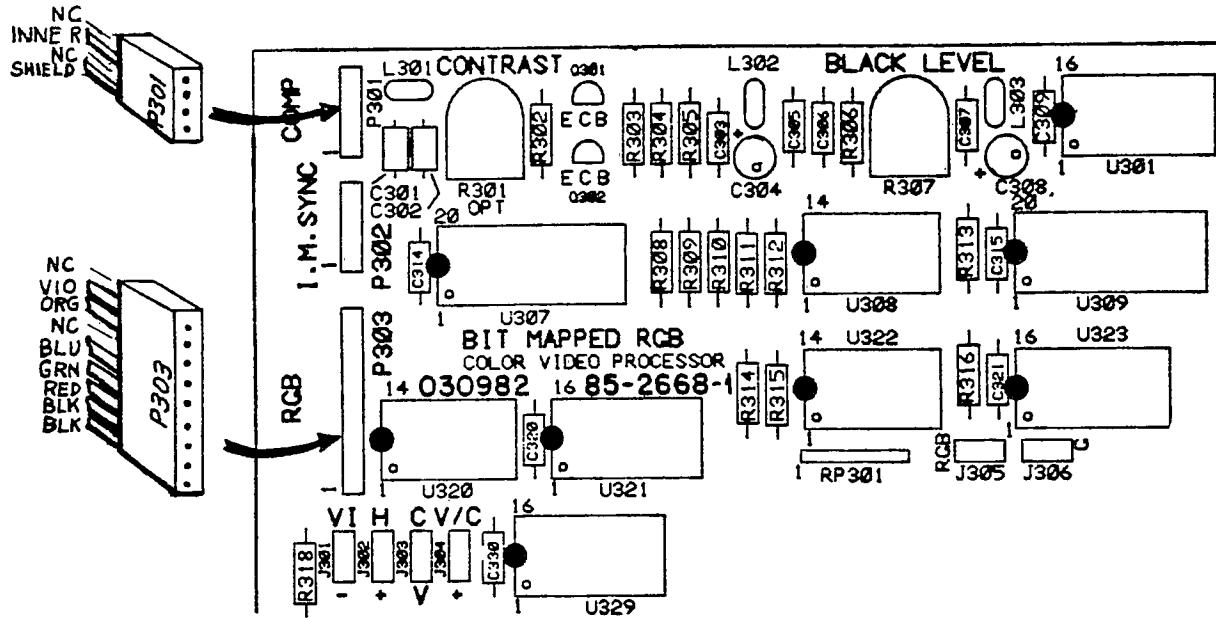


- Lift the motherboard until you are able to disconnect the two power supply connectors P101 and P102 from the motherboard.
- Carefully lift the motherboard from the chassis.

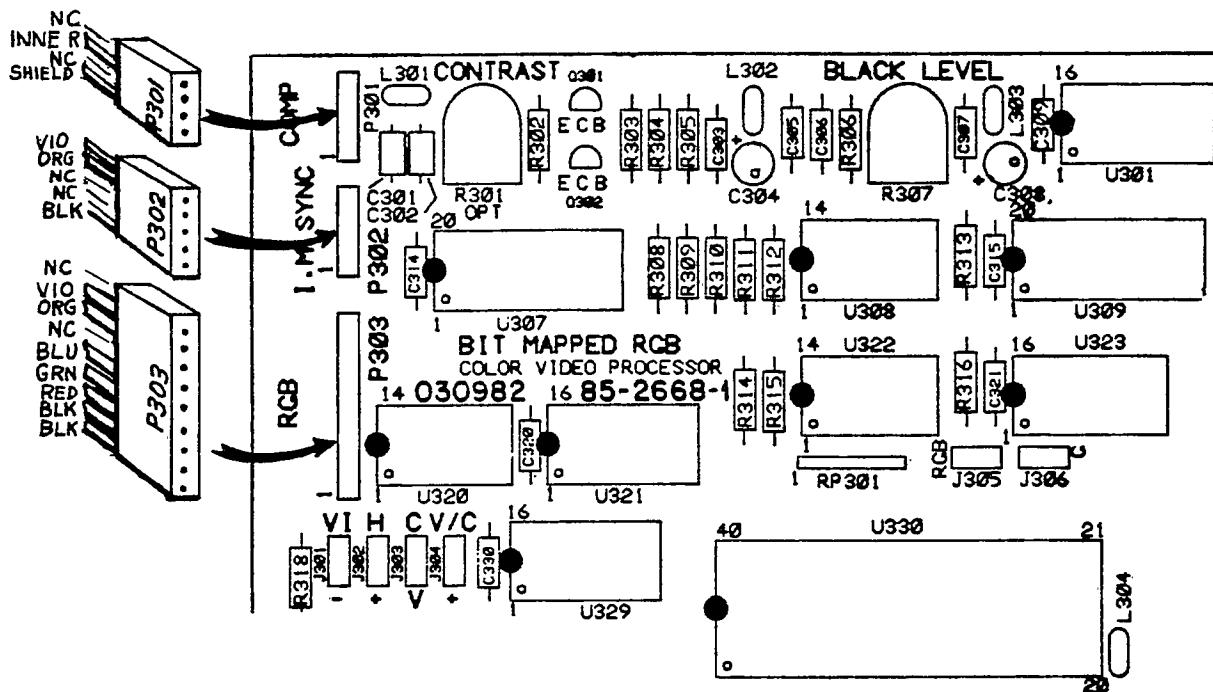
This completes the disassembly of the Low Profile Computer. Reverse the procedure to reassemble the computer. Be careful not to pinch any wires.

VISUAL CHECKS

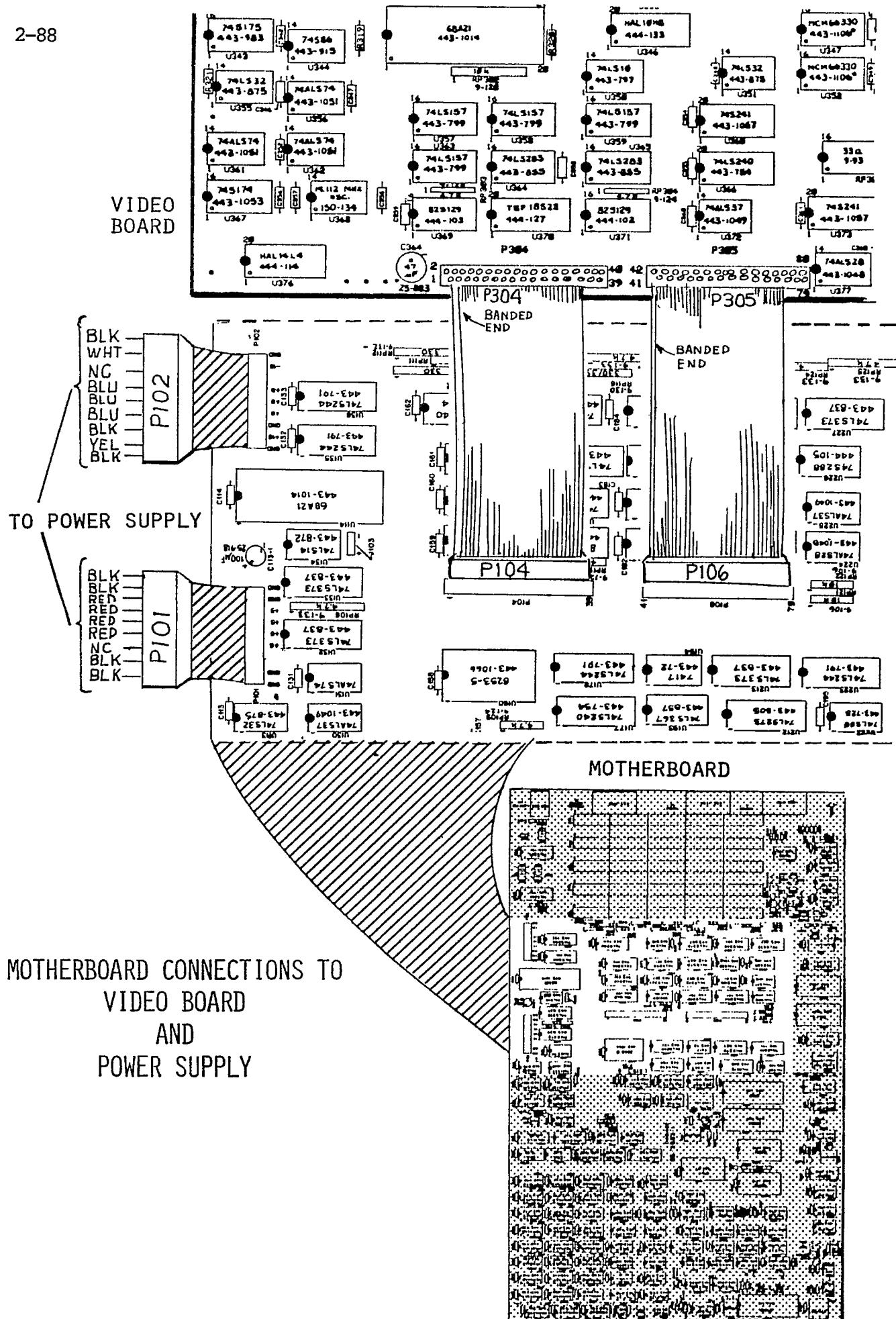
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LOW-PROFILE VIDEO BOARD CONNECTIONS

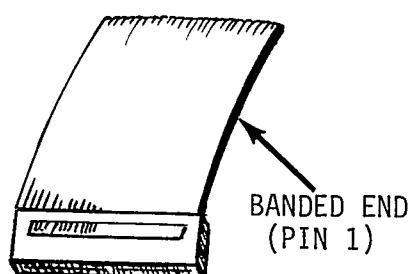


ALL-IN-ONE VIDEO BOARD CONNECTIONS

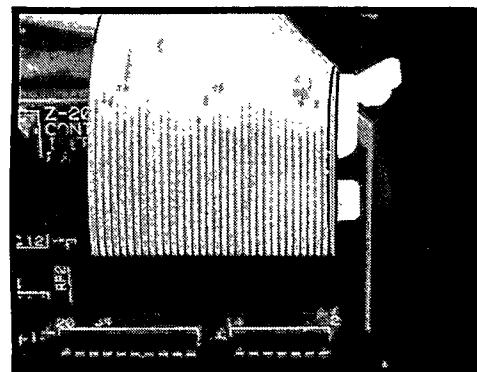


DISK CONTROLLER BOARD CABLE CONNECTIONS AND SWITCH POSITIONS

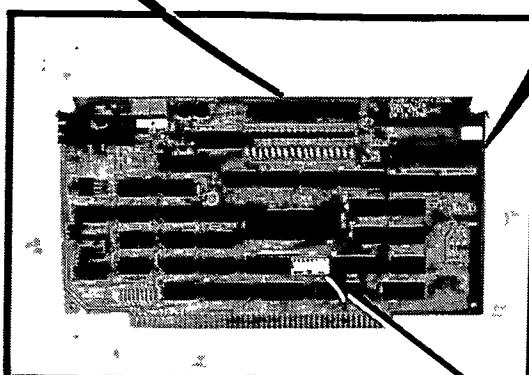
8" DRIVE CABLE



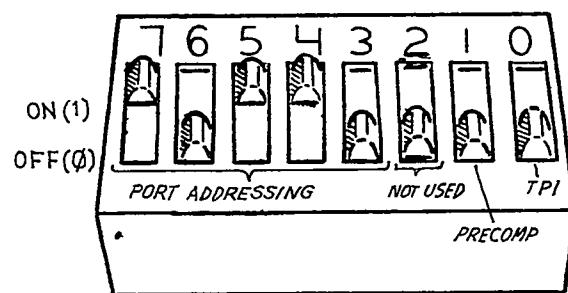
INTERNAL 5-1/4" DRIVE CABLE

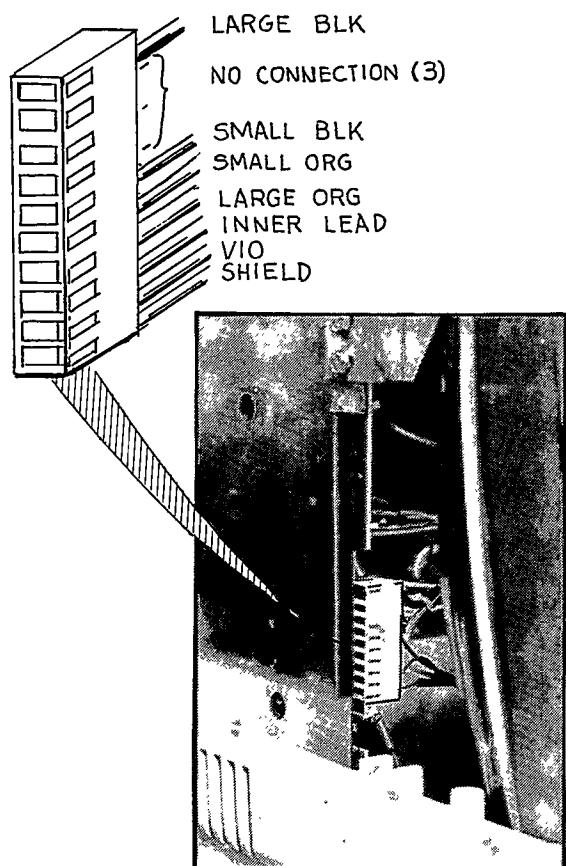


BANDED END
(PIN 1)



SWITCH SET FOR HEATH
48 TPI 5-1/4" DRIVES



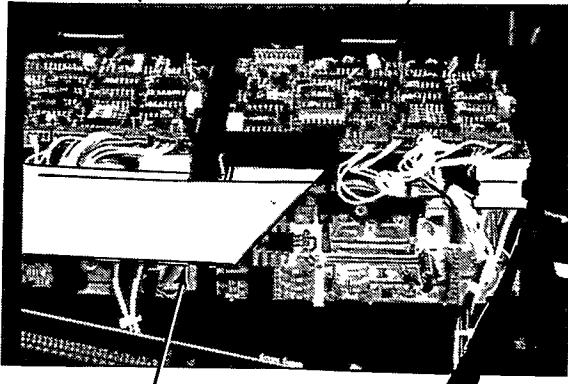


ALL-IN-ONE SWEEP BOARD
CONNECTIONS

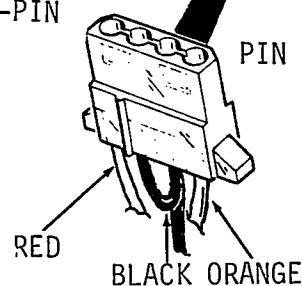
DISK CONTROLLER BOARD
5-1/4" DISK DRIVE CONNECTIONS

LOW PROFILE COMPUTER (SHOWN WITH DRIVE SHIELDS REMOVED)

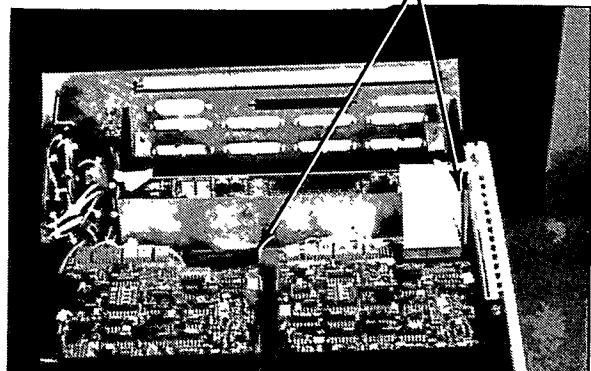
(Viewed from Rear)



BANDED END OF 34-PIN CONNECTOR PIN 1



BANDED END OF 34-PIN CONNECTOR



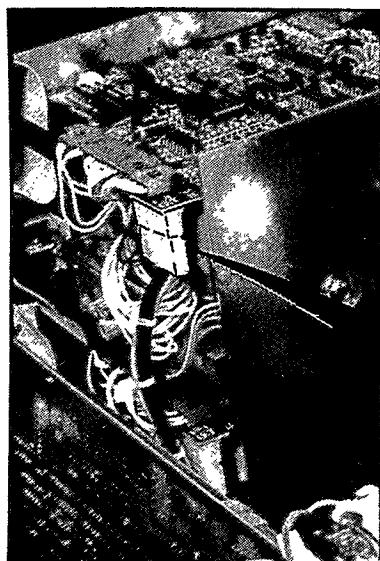
(Viewed from Top)

ALL-IN-ONE COMPUTER

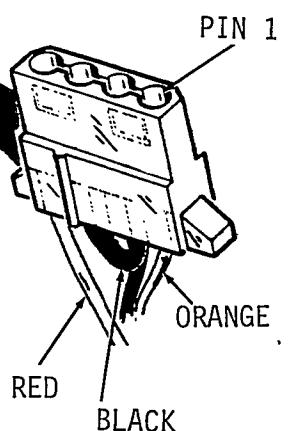
BANDED END OF 34-PIN CONNECTOR



(Viewed from Right Side)



(Viewed from Left Top)



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INTRODUCTION

GENERAL

These troubleshooting procedures provide guidelines on what modules and components to check when troubleshooting a particular problem. Due to the complexity of the H/Z-100, however, these tests will not always lead you to the exact component causing the problem.

To service to the component level, you must be familiar with the H/Z-100 circuitry. Study the Circuit Descriptions, IC Data Sheets of the more complex ICs, Operation, and Specifications sections of this Manual. But, once you understand how the computer works, you will be able to quickly repair the unit and have fewer tough-dogs to contend with.

TROUBLESHOOTING PROCEDURE

This section, System Troubleshooting, will help you narrow the problem down to a board/module level. What you do next depends on whether you're servicing to the module level or to the component level.

If you're doing module-level repair, replace the defective board and proceed to Final Checks in this section.

If you're repairing the unit to the component level, perform the procedure outlined in this section to narrow the problem down to a board or module. Once you've determined which module is defective, go to the appropriate section in this manual (such as the Motherboard or Video Board) for detailed troubleshooting information.

When you've repaired the problem, return to this section and perform the final checks.

DIAGNOSTICS

The diagnostic programs make it easier to service the H/Z-100. These routines will show which circuit is bad and, in some cases, will locate the component causing the failure. Some of the diagnostic programs will continually exercise a suspected defective circuit, allowing you to test the circuit with a logic probe or oscilloscope. See the Diagnostics section of this Manual for the available programs and operating instructions.

From time to time, new diagnostic programs will be added to this Manual. Depending on what the program is for, it will be supplied as a printed source listing, or on a disk, or in ROM.

EQUIPMENT NEEDED

To troubleshoot the H/Z-100, you need the following test equipment. The test equipment specifications should meet or exceed those listed after the underlined item. The suggested model numbers, at the end of each item, will fulfill these recommendations.

Oscilloscope DC to 20-MHz, dual trace, triggered sweep. Heath SO-3220, or equivalent. Note: This oscilloscope is suitable for most of your troubleshooting needs. However, for critical pulse measurements, use a 35-MHz, delayed-sweep oscilloscope such as the Heath SO-4235.

Logic Probe DC to 20-MHz, capable of detecting 10-nS single pulses. Indicates logic one, logic zero, and high-impedance states. Heath IT-7410, Hewlett-Packard HP-545A, or equivalent.

DVM High-impedance input. 0-1000 volts, 0-1 megohm. Heath SM-2215 DVM or equivalent.

Voltage-Variable AC Power Supply Zero to 120 Vac RMS, 3 amperes. Heath SP-5220 or equivalent.

Variable DC Power Supply Voltage adjustable to 1 volt, current-limiting adjustable to 100 mA. Heath IP-2728 or equivalent.

Low-Capacitance Oscilloscope Probe Input capacitance adjustable between 15-50 pF, 4-nS rise time. Heath PKW-105 or equivalent.

High-Voltage Probe Capable of measuring up to 40 kV in color video monitors. Heath IM-5210 or equivalent.

Video Monitor RGB wide-band color monitor. Nippon Electric Co. JC-1202DH or equivalent. If a color monitor is not available, use a wide-band (15 MHz) monochrome monitor. Zenith ZVM-121 or equivalent.

USEFUL TOOLS



Long-Nose Pliers



Diagonal Cutters



Wire Strippers



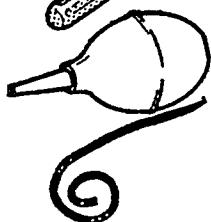
1/8" Blade Screwdriver



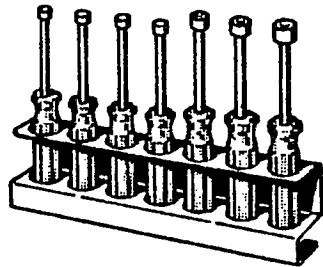
1/4" Blade Screwdriver



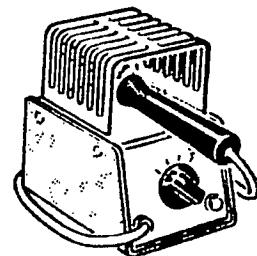
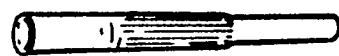
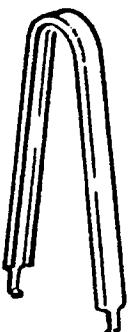
Phillips Screwdriver



Desoldering Bulb

Desoldering Braid
(#HE490-185)

Nut Drivers

Soldering Iron
(Model GH-17A)1/4" & 5/16" Open-End Wrench
(#HE490-168)Nut Starter
(#HE490-5)IC Puller
(#HE490-111)IC Puller
(#HE490-189)

INITIAL SETUP

INTRODUCTION

The H/Z-100 is easy to disassemble; even an all-in-one unit requires only about 15 minutes to remove the motherboard.

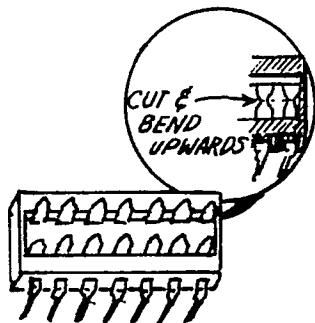
However, due to the way the unit is packaged, there are very few test points that you can reach while the unit is assembled and operating. To get around this, you should build the following extender cables.

These extender cables allow you to spread out the H/Z-100 over a 29" x 46" surface. This permits you to easily reach every IC while the unit is operating.

PARTS REQUIRED

Qty.	Description	Part No.
2	40-pin ribbon cable w/connectors	HE 134-1108
1	34-pin ribbon cable w/connectors	HE 134-1025
4	Small alligator clips for jumper wire construction	HE 260-16
20 ft.	#18 stranded wire	HE 344-155
20	Large spring connector	HE 432-753
1	10-pin adapter plug	HE 432-788
2	10-hole socket shell	HE 432-1061
1	Programming plug	HE-432-1168

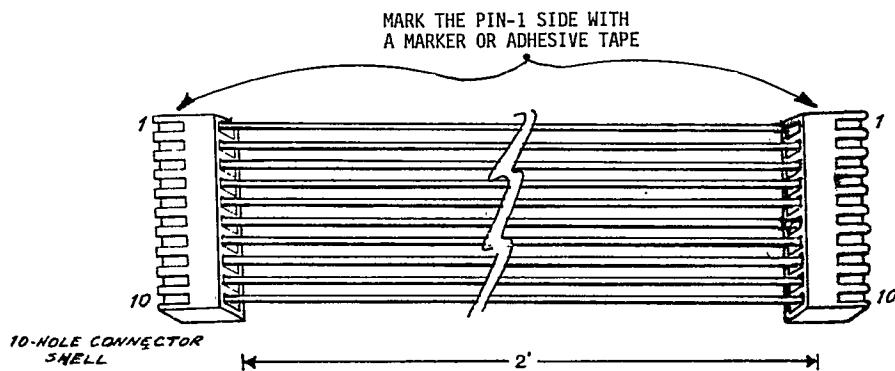
PROGRAMMING PLUG CONSTRUCTION



In some of these tests you'll be required to remove an IC and short one of the socket pins to ground or to +5 volts. If you use a resistor lead to make the socket connection, you may bend the spring connector of the socket out of place. This could cause intermittent operation when the IC is reinstalled. Since replacing an IC socket on a four-layer board is a time-consuming task, build and use the following test jig.

- Locate the programming plug and cut all jumpers along their centers.
- Bend every other lead up so you can connect an alligator clip to any one of them without shorting to another lead.

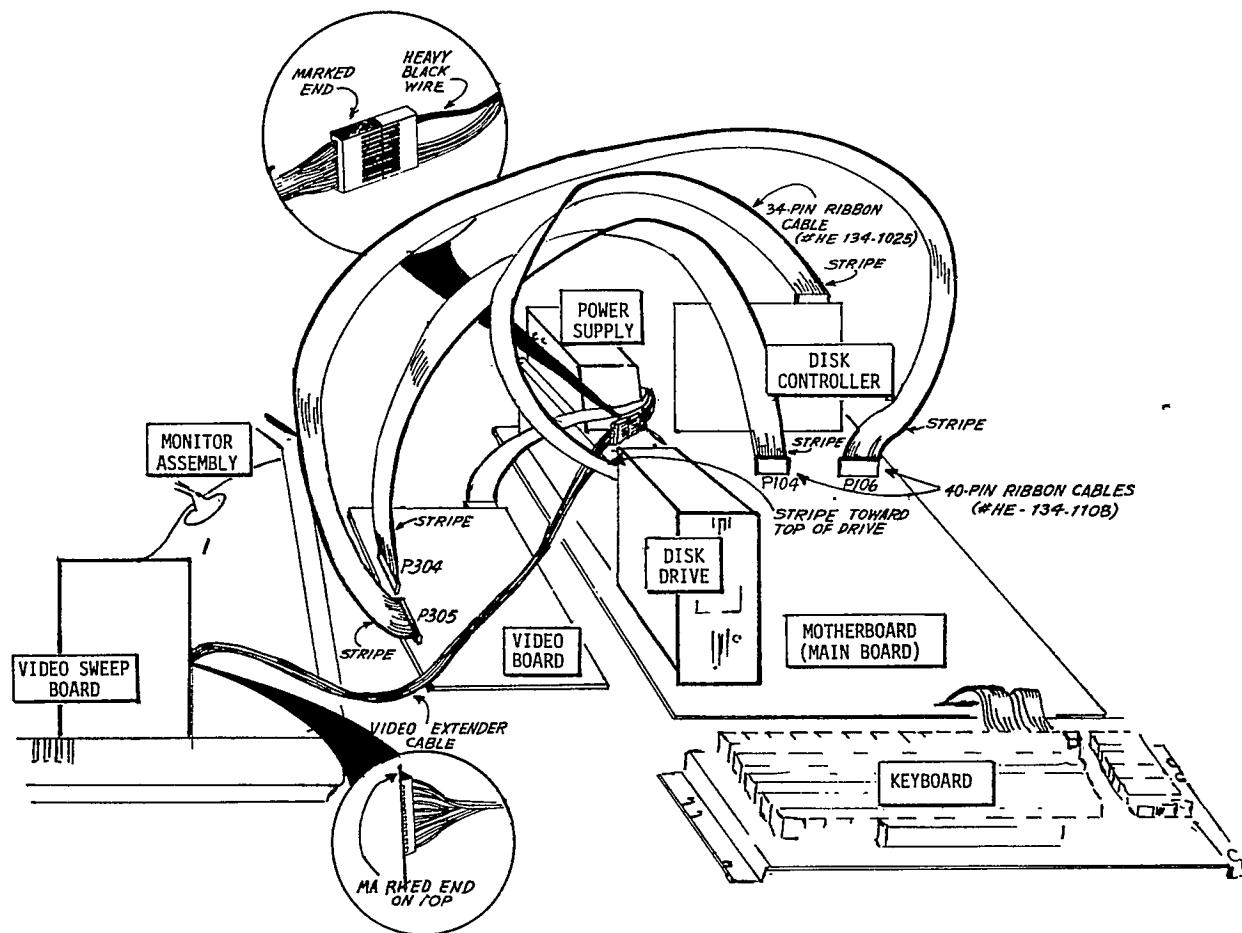
VIDEO BOARD EXTENDER CABLE CONSTRUCTION



NOTE: The video board circuits do not use all ten leads of the following extender cable. However, you should install all ten leads into the extender cable to allow for future modifications.

- Cut the stranded wire into 10 two-foot lengths and solder a spring connector to both ends of each wire.
- Position the 10-hole socket shells so that the slotted sides are facing toward you and install the wires as shown in the previous illustration.
- Refer to the illustration and mark the pin-1 side of each shell with a marker or adhesive tape.
- Locate the 10-pin adapter plug and install it into one end of the extension cable.
- Locate the two 40-pin ribbon cables and inspect the connectors. If there are any pin plugs present, remove them with a pair of long-nosed pliers.





H/Z-100 TEST SETUP

- Refer to the Disassembly section and disassemble the H/Z-100 down to the motherboard. Leave the motherboard and power supply mounted on the base.
- Remove the S-100 card cage assembly so you can reach the ICs that it covers.

If you're working on the low-profile H/Z-100, skip the next step.

- Refer to the accompanying illustration and install the video sweep board extender cable as shown. Make sure that the slots are facing the same way at the 10-pin adapter plug end.

If you're working on the all-in-one H/Z-100, skip the next step.

- Connect the unit under test to your video monitor. Use 75-ohm coaxial cable.
- Connect the disk drives to the floppy disk controller board with the 34-pin ribbon connector cable. The cable stripe should face the same direction at both the board and the drives.
- With the 40-pin ribbon cable, connect P304 on the video board to P104 on the motherboard. Make sure that the striped edge of the cable is facing the same direction on both boards (see the inset in the accompanying illustration).
- In the same manner, connect P305 to P105.
- Set up S101 for 5-1/4" drives (primary boot), and auto-boot defeated (see the Configuration section).

DISK DRIVE SETUP

Currently, the male pins needed to build an extension cable for the disk drive power supply are not available from stock. To test a disk drive, you'll have to remove it from its mounting bracket and place it closer to the main chassis. A convenient location is the open area to the left of the motherboard and in front of the power supply module.

- Position the disk drive as described and install the power cable.

The H/Z-100 is ready for servicing.

GENERAL TROUBLESHOOTING INFORMATION

REPAIRING MULTILAYER BOARDS

The H/Z-100 contains two 4-layer circuit boards: the motherboard and the bit-mapped video board. These boards contain foil runs on the two outer surfaces and a +5 volt plane and ground plane on the inside of the board.

Although a 4-layer board is more complex than a double-sided board, you can replace components on the board by being careful and using tools similar to the following:

1. Heath GH-17A 25-watt soldering iron with the temperature control set to medium.
2. #2 solder wick (G.C. Electronics catalog no. 684).
3. A desoldering bulb. Do not use a spring-action solder sucker; it could damage the foil runs.
4. Solder, long-nose pliers, diagonal pliers, and small screwdriver.

There are two problems you should watch out for when replacing a component on the motherboard or video board: (1) A sleeve connecting one layer to another may open when you remove a component. (2) A solder bridge may short together two foil runs, which are closely spaced.

Since most of the circuit board foils are solder-masked, solder bridges should not be a problem. However, be careful around IC sockets; you'll quite often find conductors running between the socket pins.

If a sleeve opens, you can repair it by using wire-wrap wire to jumper the component lead to its destination. Note, however, that this may make the circuit board incompatible with the automated board-testing equipment at the factory.

To prevent opening a sleeve, or causing other damage to the multilayer board, observe the following guidelines:

1. AXIAL-LEAD COMPONENTS (SUCH AS RESISTORS)

Removal

Completely remove the solder from the leads with solder wick.

Straighten the resistor leads so they won't pull against the sleeves when you remove the resistor.

Heat one lead with the soldering iron until the solder melts, then gently pull that lead away from the board.

In the same manner, remove the remaining lead.

Replacement

Make sure that the holes where the resistor leads are to be installed are clear. Use solder wick, if necessary, to remove excess solder.

Install the resistor, solder it, and clip off the excess lead lengths as you normally do for any circuit board.

2. VERTICALLY-MOUNTED COMPONENTS (SUCH AS ELECTROLYTIC CANS)

Removal

Remove the solder with solder wick. This may take longer than removing solder from a resistor lead. Most of the electrolytics connect to the +5 volt and ground planes of the circuit board, which act as heat-sinks.

Straighten the component leads so they won't drag against the sleeves when you remove the component.

Generally, solder wick will not completely remove all the solder between the leads and the sleeves; causing the leads to stick to the sleeves. Since, in vertically mounted components, you usually can't pull one lead out at a time, you must use a rocking technique. Here's how...

Heat one lead with the soldering iron and tilt the capacitor so that the lead starts to move out of its hole.

Then heat the other lead and tilt the component in the opposite direction so that lead starts to move out of its hole.

Continue the previous two steps until the capacitor pulls free of the circuit board.

The above is a common procedure for removing vertically mounted components from any circuit board. The only difference here is that you must be more careful.

Replacement

Use the same technique described in the section on resistor replacement. Do not apply too much solder, since you won't be able to tell if a solder blob is forming between the capacitor and circuit board.

3. IC Sockets

Removal

Pry off the plastic portion of the socket with a small screwdriver.

Remove the socket spring connectors, one at a time, using the following technique:

Position the board on its edge so that you can reach both sides of the board.

Grip the spring connector with a pair of long-nose pliers.

Heat the spring connector solder connection from the foil-side of the board.

When the solder melts, gently pull the spring connector from the board.

Replacing

Remove any excess solder from the IC socket holes. Use the desoldering bulb if the solder wick won't remove all of the solder.

Install and solder the IC socket. Apply the solder sparingly to prevent solder blobs from forming beneath the IC socket.

4. OTHER COMPONENTS

Board Connector Pins

Generally, you would remove these in the same manner as described under "IC Sockets." That is, grip one pin with the pliers, heat the solder connection, and gently pull the pin out. Repeat until all pins have been removed.

Resistor Packs

You will probably never have to replace a resistor pack. However, if the situation arises, review the following.

Like other rigid, multi-pin components, resistor packs have to be destroyed in order to be removed -- unless you have special desoldering tools. The leads of some resistor packs are accessible to diagonal pliers; allowing you to clip the pack away from the leads and then removing each lead from the board.

Other resistor packs are mounted flush to the board; preventing you from reaching the leads. In cases like this, use a slightly heavier pair of diagonal pliers and cut up the resistor pack to get to the leads.

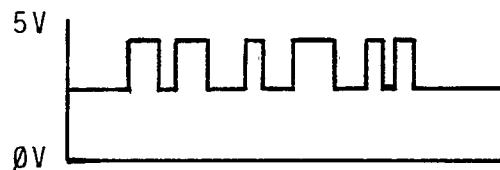
Be careful and don't apply any stress to the board.

S-100 Bus Connectors

You will not be able to efficiently replace the S-100 connectors without special desoldering tools. If you discover a bad S-100 socket that can't easily be fixed, you may be better off if you replace the entire motherboard. If this situation arises, first check with the technical consultants and your store manager or service supervisor.

CHECKING SHORTED FOIL RUNS

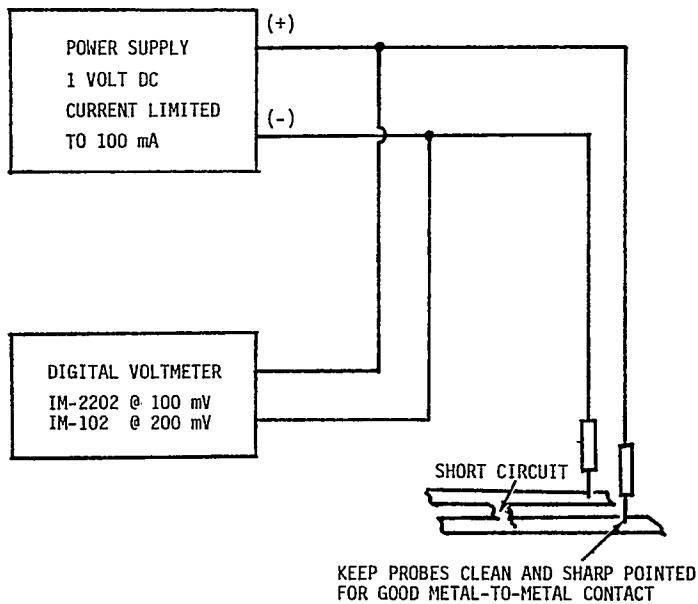
Occasionally the input or output of a TTL logic circuit can partially short inside the IC, causing a high-resistance path to the +5 volt supply. The resulting logic level on that bus line may be an undefined state of about +1.5 volts. If this line is shared by other ICs, their outputs will override this level to give a waveform similar to the one shown below:



Measuring this line with a logic probe may indicate normal operation. Although most logic probes will show pulses going from a high-impedance state to logic one, this can be easily overlooked. In this case, an oscilloscope will give a quick and definite indication of a faulty line.

A direct short, on the other hand, can cause zero ohms between a bus line and +5 volts, ground, or another bus line. If this should occur, the most likely cause is a shorted IC rather than a solder bridge, since most of the H/Z-100 boards are factory assembled and tested. Since the ICs are installed in plug-in sockets, it is perhaps quickest to place an ohmmeter across the shorted lines and start pulling ICs connected to those lines until the reading jumps up from zero ohms.

If removing the ICs doesn't correct the problem, you can use the following technique:



- Unplug all ICs and lift (if possible) all components connected to the shorted line.
- Adjust the DC power supply to 1.0 volt and set the current limiting to 100 mA.
- Set the DVM to its 200-mV range and connect it in parallel with the DC power supply.
- Connect two sharp-pointed test probes (for good metal-to-metal contact) to the two shorted lines. Test various sections of the line until you locate the area where the displayed voltage is lowest. The short circuit should be at this point.

When the short is beneath an IC socket, the voltage along the lines will drop as the pair of probes enters the socket area, and rise again as measurements are made further away from the socket on the other side.

Depending on line length, maximum voltage will be about 10 to 15 mV furthest away from the short.

NOISE PROBLEMS

The H/Z-100 contains six RF-frequency crystal oscillators and dozens of circuits generating fast rise-time pulses. These all contribute noise to the power supply lines and ground returns, even when filtered. This can cause erroneous readings if you do not properly connect your test probe. If you don't maintain an awareness of this noise, you can waste a lot of time trying to track down a symptom that doesn't exist.

When testing the H/Z-100, connect the ground return of your logic probe or oscilloscope probe as close as possible to the component that you're measuring. If there's a long distance between the point you're measuring and the ground connection, the ground run may pick up noise which could give you false readings. A good place to ground your test lead is one of the diode-shaped ceramic capacitors near the IC under test.

Another type of noise problem can occur if the power supply isn't regulating or filtering properly. In this case, for example, a surge of current, such as when a disk drive turns on, may generate a large enough spike into the line to affect some of the logic circuits. This could result in intermittent crashes, and, in this example, cause you to waste time troubleshooting the drive circuits instead of the power supply. So, when troubleshooting H/Z-100 -- or any electronic circuit for that matter -- check the power supply first.

SERVICE HINTS

DEAD UNIT

OPEN FUSE OR CIRCUIT BREAKER

Unplug the power supply from the circuit boards. Then connect the power supply to a voltage-variable AC supply and adjust the primary voltage from 0 Vac to 120 Vac. If the primary current should suddenly increase above 2 amperes, then replace the power supply module. (The average primary current is about 1.5 amperes.)

If the current is okay, then check the DC output voltages. If any of the voltages or peak-to-peak ripple is incorrect, then replace the power supply module.

If the voltages are okay, then one of the circuit boards is defective.

To find out which one, make resistance readings. If you find a shorted foil run, locate the short by using the techniques described earlier.

If you can't find an obvious short circuit, then plug in boards, one at a time, and slowly adjust the variable AC supply from 0 to 120 Vac each time. When the current rises too fast, you've found the bad board.

Inspect the suspected board for heat-damaged components and improperly installed components (see Visual Checks for the board you're inspecting). Check the on-board regulators for short circuits between their inputs and outputs.

If necessary, replace the suspected board with a known-good one.

INCORRECT VOLTAGES

Use the same procedure described under "Opens Fuse or Circuit Breaker." That is, unplug the power supply module from all the circuit boards and check the supply voltages. If any of these are incorrect, then replace the power supply.

Otherwise, a circuit board is causing the problem. For example, if it's pulling a voltage line down, you probably won't find the cause by taking ohmmeter measurements.

In this case, use the visual checks section and make sure that each component is in the right place. Make sure that none of the ICs are installed backwards. Touch each IC and make sure that none of them are hot -- indicating an internal short. (Note that the larger ICs will be warm, but not so hot that you can't keep your finger on it.)

If necessary, replace the circuit board.

DISPLAY PROBLEMS

If an all-in-one unit, check the 12-volt power supply to the video sweep board. If missing, check the power supply cables and, if necessary, replace the power supply module.

Connect your shop monitor to the appropriate video output (RGB or composite). If the display is okay on your monitor, then the customer's video sweep board or monitor is bad.

If the video sweep board or monitor is okay, then substitute a known-good bit-mapped video board. If this corrects the problem, go to the video board troubleshooting section, or replace the video board.

If the video sweep board and the bit-mapped video board test okay, then proceed to the motherboard troubleshooting section.

DEFECTIVE KEYBOARD

Is the LED on the RESET key lit? If not, then check the 5-volt supply to the motherboard. If missing, refer to the suggestions under "Dead Unit." If 5 volts is present, then check for open foil runs on the motherboard.

Substitute a known-good keyboard assembly. If this corrects the problem, then replace the keyboard. Otherwise, replace the motherboard; or, if you're troubleshooting to the component level, perform the tests in the Motherboard Troubleshooting section.

WON'T BOOT

Attempt to boot up with known-good software. If you can, then try the customer's software. Also, make sure the customer is correctly following the boot-up procedure. If the software is okay, then perform the following hardware checks.

Check the power cables to the drives. Make sure that the drives are getting both +12 volts and +5 volts.

Make sure that the 34-pin ribbon cable between the drives and controller board is installed properly.

Check the configuration section and make sure that the slide switches are correctly positioned and jumper plugs properly installed. This includes the motherboard, disk controller board, and disk drives.

Substitute a known-good disk controller board. If this corrects the problem, then replace the board or refer to "Troubleshooting" in the Disk Controller section of this Manual for more service information.

Substitute a known-good disk drive. Though it's unlikely for both drives in a dual-drive system to go bad, it can happen.

If the above modules test okay, then replace the motherboard. Or, for in-depth troubleshooting, refer to "Troubleshooting" in the Motherboard section of this Manual.

OTHER PROBLEMS

SERIAL PORT A DEFECTIVE (ASYNCHRONOUS PRINTER)

Check this port with a known-good printer (such as the H/Z-25), connecting cables, and software. If the system works properly, then the problem is likely in the customer's peripheral equipment. Otherwise, perform the following tests.

Check the +5 volt and +16 volt supplies to the motherboard. If missing, replace the power supply module.

Replace the motherboard; or, for in-depth troubleshooting, refer to "Troubleshooting" in the Motherboard section of this manual.

SERIAL PORT B DEFECTIVE (MODEM)

Check this port with a known-good MODEM (such as the Heath WH-43 {Hayes Stack Smartmodem}), connecting cables, and software. If the system works properly, then the problem is likely in the customer's peripheral equipment. Otherwise, perform the following tests.

Check the +5 volt and +16 volt supplies to the motherboard. If missing, replace the power supply module.

Replace the motherboard; or, for in-depth troubleshooting, refer to "Troubleshooting" in the Motherboard section of this manual.

PARALLEL PORT DEFECTIVE

Check this port with a known-good line printer (such as the Epson MX-80), connecting cables, and software. If the system works properly, then the problem is likely in the customer's peripheral equipment. Otherwise, perform the following tests.

Check the +5 volt power supply to the motherboard. If missing, replace the power supply module.

Replace the motherboard; or, for in-depth troubleshooting, refer to "Troubleshooting" in the Motherboard section of this manual.

FINAL CHECKS

Before returning the H/Z-100 to the customer, ensure that the computer is operating properly by performing the following final checks:

- All circuit boards, plugs, and other connectors securely installed.
- All hardware installed and tightened.
- All switches and jumper options configured for the customer's system; or configured to the customer's specifications. (Unless requested otherwise, the auto-boot feature should be enabled.)
- Unit powers up properly.
- Unit loads and runs Z-DOS, CP/M-85, and other programs properly.
- Keyboard echos all printable characters to the CRT under Z-DOS.
- Display is properly calibrated for height, width, and linearity.
- Display is uniformly focused across the CRT.
- Unit passes the system and video memory tests on the Z-DOS disk (see the Diagnostics section in this manual).
- Let the H/Z-100 operate for an hour and again test the memory for thermal problem.

If the customer has complained of a thermal or intermittent problem (or you suspect one), let the unit run overnight and again perform the diagnostics in the morning.
- Paperwork is in order.
- The customer has been notified.

TECHNICIAN NOTES:

PARTS LISTS



PARTS LIST - ALL-IN-ONE CABINET AND ASSEMBLIES

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.	CIRCUIT Comp. No.	DESCRIPTION
ASSEMBLIES			HARDWARE	#4 and #6 Hardware
CRT monitor assembly consisting of:		HE 234-202	#4 lockwasher	#4 lockwasher
1) CRT (green)	100-724-03		#4 nut (large)	#4 nut (large)
2) Yoke	A-8337		#4 nut	#4 nut
3) Video sweep p/c bd	A-10520		4-.40 x 1/4" bl	4-.40 x 1/4" bl
Disk drive 5-1/4", 48TRPI	HE 150-142		Phillips-head 4-.40 x 1/2" sc	Phillips-head 4-.40 x 1/2" sc
Keyboard	HE 64-899		4-.40 x 3/16" h	4-.40 x 3/16" h
Power supply	HE 234-201		4-.40 x 1" hex	4-.40 x 1" hex
Wired floppy control board	HE 181-3763		#6 flat washer	#6 flat washer
Wired mother board	HE 181-3630		#6 lockwasher	#6 lockwasher
Wired video board (B/W) (Color)	HE 181-3631		(internal-bo #6 lockwasher	(internal-bo #6 solder lug
	HE 181-3267		external-to #6 lockwasher	external-to #6 x 5/8" hex-
CABINET - CHASSIS			#6 x 1/4" blac head self-ta	#6 x 1/4" blac head self-ta
Bottom cover	HE 92-759		6-32 nut	6-32 nut
CRT support bracket	HE 204-2606		6-32 x 3/4" bl	6-32 x 3/4" bl
CRT support panel	HE 203-2116		head screw	head screw
Cabinet center	HE 92-762		6-32 x 1/2" sc	6-32 x 1/2" sc
Cabinet top	HE 92-761		6-32 x 1/4" ph	6-32 x 1/4" ph
Cable clamp	HE 204-2638-1		screw	screw
Chassis	HE 200-1418-1		6-32 x 3/8" he	6-32 x 3/8" he
Drive mounting plate	HE 200-1419		6-32 x 1-3/4"	6-32 x 1-3/4"
Dual drive support panel	HE 203-2129			
Dual drive front panel	HE 203-2131			
Front bezel	HE 92-763			
Latch bracket	HE 204-2632			
Nut holding plate	HE 205-8199			
Rear panel	HE 203-2139-1			
S-100 card cage	HE 206-21416			
S-100 panel guide	HE 94-631			
			OTHER HARDWARE	
CABLES			#8 x 1/2" black head screw	#8 x 1-1/2" he #8 x 3/4" hex-
34-conductor flat ribbon	HE 134-1247		#8 x 5/8" hex-	#10 flat wash
cable assembly	HE 134-1247		#10 x 1-1/2" h	Control lockwa
50-conductor flat ribbon	HE 134-1264			Latch pin
cable assembly	HE 134-1265			Small control
Composite video cable assembly	HE 134-1273			Spring
Internal video cable assembly	HE 134-1253			
RGB cable assembly	HE 134-1254			
Video interface cable assembly	HE 134-1257			

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.	CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
HARDWARE					
#4 and #6 Hardware					
#4 lockwasher	HE 254-9	100 ohm 1/4 watt, 5%	HE 6-101-1		
#4 nut (large)	HE 252-2	500 ohm control	HE 10-1192		
#4 nut (small)	HE 252-15	Braid	HE 345-1		
4-40 x 1 1/4" black		Foam tape	HE 74-41		
phillips-head screw	HE 250-1411	Insulating paper			
4-40 x 1 1/2" screw	HE 250-1413	5-1/2" x 6-1/2"	HE 75-826		
4-40 x 3/16" hex "D" spacer	HE 255-757	Knob	HE 462-952		
4-40 x 1" hex spacer	HE 255-804	Label: Class A FCC	HE 390-2331		
#6 flat washer	HE 253-60	Label: Power rating	HE 390-2038		
#6 lockwasher		Label: Serial set	HE 390-2039		
(internal-toothed)	HE 254-1	Label: Warning	HE 390-2328		
#6 lockwasher		Line cord	HE 89-60		
(external toothed)	HE 254-6	Name plate	HE 391-953		
#6 solder lug	HE 259-1	Rubber grommet	HE 73-6		
#6 x 5/8" hex-head screw	HE 250-1199	Rubber foot	HE 261-29		
#6 x 1/4" black phillips-head self-tapping screw	HE 250-1307	2-1/8" brown hole cover	HE 485-42		
6-32 nut	HE 252-3	2-3/8" brwn hole cover	HE 485-43		
6-32 x 3/4" black phillips-head screw	HE 250-1240	2-7/8" brown hole cover	HE 485-44		
6-32 x 1 1/2" screw	HE 250-1430	Manual set	HE 172-8281		
6-32 x 1/4" phillips-head screw	HE 250-1325	consisting of:			
6-32 x 3/8" hex-head screw	HE 250-1264	1) Binder	HE 701-140		
6-32 x 1-3/4" screw	HE 250-1315	2) Slip-in cover	HE 597-2802		
OTHER HARDWARE					
#8 x 1 1/2" black phillips-head screw	HE 250-1265	3) Spine cover	HE 597-2803		
#8 x 1-1/2" hex-head screw	HE 250-1405	4) Document holder	HE 597-2910		
#8 x 3/4" hex-head screw	HE 250-512	5) Diskette holder	HE 703-73		
#8 x 5/8" hex-head screw	HE 250-1138	6) Demonstration disk	HE 891-342		
#10 flat washer	HE 253-98	7) Publisher's package	HE 593-0038		
Control lockwasher	HE 250-1318	consisting of:			
Latch pin	HE 252-56	1) User's manual	HE 595-2892		
Small control nut	HE 252-39	2) Tab set	HE 597-2766		
Spring	HE 258-749	3) Fly sheet	HE 597-2907		

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PARTS LIST - LOW PROFILE CABINET AND ASSEMBLIES

2-122

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.	CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.	CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
ASSEMBLIES								
Disk drive 5-1/4", 48 TPI								
Keyboard								
HE 150-142	HE 64-899	HE 234-200	HE 234-200	#4 lockwasher	HE 254-9	HE 254-9	HE 254-9	HE 254-9
Power supply	HE 181-3763	HE 181-3763	HE 181-3763	#4 nut (large)	HE 252-15	HE 252-15	HE 252-15	HE 252-15
Wired floppy control board	HE 181-3630	HE 181-3630	HE 181-3630	#4 nut (small)	HE 250-1411	HE 250-1411	HE 250-1411	HE 250-1411
Wired mother board	HE 181-3631	HE 181-3631	HE 181-3631	4-10 x 1-1/4" black	HE 250-1411	HE 250-1411	HE 250-1411	HE 250-1411
Wired video board (B/W)	HE 181-3267	HE 181-3267	HE 181-3267	Phillips-head screw	HE 250-1411	HE 250-1411	HE 250-1411	HE 250-1411
(Color)				4-10 x 1-1/2" screw	HE 250-1413	HE 250-1413	HE 250-1413	HE 250-1413
CABINET - CHASSIS								
Bottom cover	HE 92-759	HE 92-759	HE 92-759	4-10 x 3/16" hex "D" spacer	HE 255-757	HE 255-757	HE 255-757	HE 255-757
Cabinet cover	HE 92-758	HE 92-758	HE 92-758	#4 lockwasher	HE 255-804	HE 255-804	HE 255-804	HE 255-804
Cable clamp	HE 200-1418-1	HE 200-1418-1	HE 200-1418-1	(internal-toothed)	HE 254-1	HE 254-1	HE 254-1	HE 254-1
Chassis	HE 92-760	HE 92-760	HE 92-760	#6 lockwasher	HE 254-6	HE 254-6	HE 254-6	HE 254-6
Drive shelf	HE 206-1441	HE 206-1441	HE 206-1441	(external-toothed)	HE 254-6	HE 254-6	HE 254-6	HE 254-6
Drive shield	HE 203-2125	HE 203-2125	HE 203-2125	#6 x 5/8" hex-head screw	HE 250-1199	HE 250-1199	HE 250-1199	HE 250-1199
Front panel	HE 203-2139-1	HE 203-2139-1	HE 203-2139-1	#6 x 1/4" black phillips-head self-tapping screw	HE 250-1307	HE 250-1307	HE 250-1307	HE 250-1307
Rear panel	HE 206-1416	HE 206-1416	HE 206-1416	6-32 x 1-1/4" screw	HE 252-3	HE 252-3	HE 252-3	HE 252-3
S-100 card cage	HE 94-631	HE 94-631	HE 94-631	6-32 x 1/8" philips-head screw	HE 250-1422	HE 250-1422	HE 250-1422	HE 250-1422
S-100 panel guide	HE 204-2605	HE 204-2605	HE 204-2605	6-32 x 3/8" hex-head screw	HE 250-1325	HE 250-1325	HE 250-1325	HE 250-1325
Slide bracket								
CABLES								
34-conductor flat ribbon	HE 134-1246	HE 134-1246	HE 134-1246	#8 x 3/4" hex-head screw	HE 250-512	HE 250-512	HE 250-512	HE 250-512
cable assembly				Latch pin	HE 262-56	HE 262-56	HE 262-56	HE 262-56
50-conductor flat ribbon	HE 134-1254	HE 134-1254	HE 134-1254					
cable assembly								
Composite video cable assembly	HE 134-1265	HE 134-1265	HE 134-1265					
RGB cable assembly	HE 134-1254	HE 134-1254	HE 134-1254					
Video Interface cable assembly	HE 134-1257	HE 134-1257	HE 134-1257					
MISCELLANEOUS								
34-conductor flat ribbon	HE 134-1246	HE 134-1246	HE 134-1246	Foam tape 3/4"W x 5/16" T	HE 74-41	HE 74-41	HE 74-41	HE 74-41
cable assembly				Label: Class A FCC	HE 390-2331	HE 390-2331	HE 390-2331	HE 390-2331
50-conductor flat ribbon				Label: Power rating	HE 390-2334	HE 390-2334	HE 390-2334	HE 390-2334
cable assembly				Label: Serial set	HE 390-2036	HE 390-2036	HE 390-2036	HE 390-2036
Composite video cable assembly				Label: Warning	HE 390-2325	HE 390-2325	HE 390-2325	HE 390-2325
RGB cable assembly				Line cord	HE 89-60	HE 89-60	HE 89-60	HE 89-60
Video Interface cable assembly				Name plate	HE 391-658	HE 391-658	HE 391-658	HE 391-658
				Phono socket	HE 434-107	HE 434-107	HE 434-107	HE 434-107
				Rubber foot	HE 261-27	HE 261-27	HE 261-27	HE 261-27
				Spring	HE 750-750	HE 750-750	HE 750-750	HE 750-750
				2-1/8" brown hole cover	HE 485-42	HE 485-42	HE 485-42	HE 485-42
				2-1/8" brown hole cover	HE 485-43	HE 485-43	HE 485-43	HE 485-43
				2-7/8" brown hole cover	HE 485-44	HE 485-44	HE 485-44	HE 485-44

HEATH
Part No.

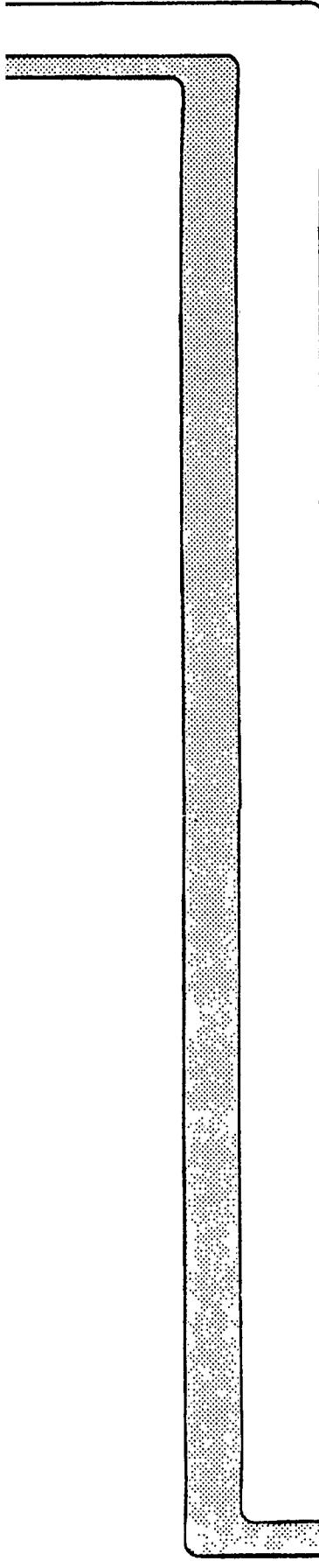
MISCELLANEOUS (CONTINUED)

DESCRIPTION	CIRCUIT Comp. No.	HEATH Part No.	DESCRIPTION	CIRCUIT Comp. No.	HEATH Part No.
Manual set consisting of:			Manual set consisting of:		
1) Binder			1) Binder		
2) Slip-in cover			2) Slip-in cover		
3) Spine cover			3) Spine cover		
4) Document holder			4) Document holder		
5) Diskette holder			5) Diskette holder		
6) Demonstration disk			6) Demonstration disk		
7) Publisher's package			7) Publisher's package		
consisting of:			consisting of:		
1) User's manual			1) User's manual		
2) Tab set			2) Tab set		
3) Fly sheet			3) Fly sheet		

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C



INTRODUCTION



The motherboard is the primary component of the H/Z-100. This is the large four-layer circuit board located on the chassis floor. This board is factory wired and tested to be 100% operational. The motherboard contains the processors, I/O, and memory facilities for the computer.

The processors for the H/Z-100 are the 8088 and the 8085. The 8088 is a 16-bit processor that operates in an 8-bit environment. This processor gives the computer its power and speed. The 8085 is an 8-bit processor that is code compatible with the popular 8080 microprocessor. The use of the 8085 microprocessor assures the user a large software base. Both processors run at a clock speed of 5 MHz. By using the advantages of both processors, the H/Z-100 is a powerful and versatile machine.

I/O communication to the outside world is located on the motherboard. It contains two serial ports, a parallel port, and a keyboard. The two serial ports are RS-232C compatible; the parallel port is a Centronics compatible printer interface. A 95-key keyboard provides user input to the computer through a dedicated microprocessor.

Also located on the motherboard are the memory facilities for the computer. This consists of on-board RAM and ROM. MTR-100, an 8K ROM, contains all the code necessary to initialize the computer and emulate H-19 functions. The standard RAM configuration for the H/Z-100 is 128K bytes. This may be expanded to 192K bytes of on-board RAM. These features make the H/Z-100 the most powerful Heath computer available.

In addition, a 5-slot, S-100 bus is located on the motherboard. It is defined by the IEE-696 definition for a S-100 bus. This allows the H/Z-100 flexibility in hardware configurations. The motherboard is configured to be the controller for the bus; however, the memory and I/O facilities may be accessed by slave processors. The only areas on the motherboard that are not accessible by slave processors are the interrupt controllers for the 8088 and the 8085, the high order address latch, and the processor swap port.

The information located in this section of the manual will aid you in troubleshooting the motherboard to the component level. Contained in this section are: Circuit Description, Visual Checks, Troubleshooting, Parts List, and X-Ray Views. If additional information on a particular IC is required, refer to the IC Data section in the back of this manual.

CIRCUIT DESCRIPTION

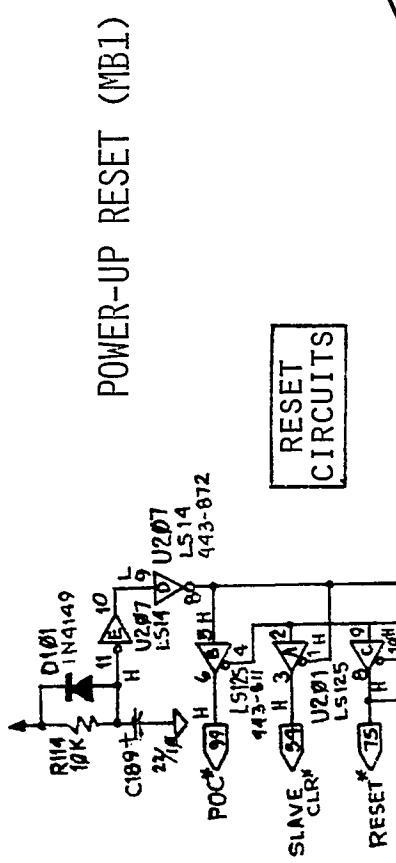
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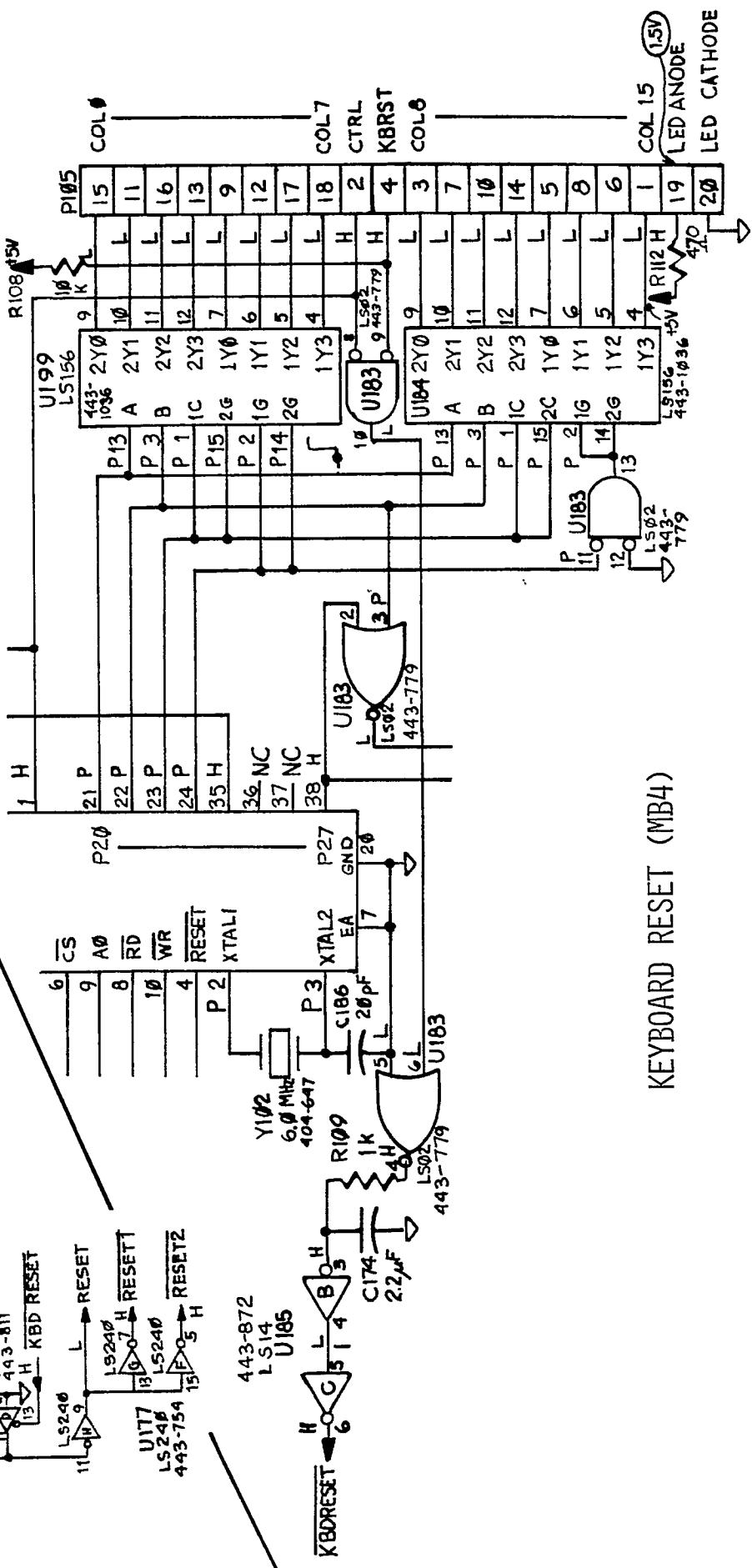
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POWER-UP RESET (MB1)



RESET CIRCUITS

POWER-UP RESET

Refer to schematic MB1.

R114 and C189 provide the power-up reset pulse for the H/Z-100. Upon turn-on, C189 charges through R114, holding U207-8 low for about 200 mS. This pulse connects to several buffers to provide the proper reset levels to the rest of the computer:

U201B buffers the reset pulse to provide the S-100 power-up clear (POC*) signal. This signal is logic zero for reset and logic one otherwise. POC* resets the video board through U215D and P106-64 on schematic MB2.

U201A buffers the reset pulse to provide the S-100 SLAVE CLR* signal. Because U207-8 controls U201A through its gate line (pin 1), SLAVE CLR* is logic zero to clear and open-collector otherwise. This signal is present only to maintain IEEE-696 (S-100) standards. Currently, it's not used in the H/Z-100.

U210C is also wired to provide a logic zero for reset and a high-impedance state otherwise. This is because several circuits may share the S-100 RESET* line. This line drives U177H and, through the S-100 bus, resets the floppy disk controller board.

U177H inverts the reset signal, which can be the power-up reset or a keyboard reset, to drive the RESET line high. This line is again inverted by U177G and U177F to provide RESET1 and RESET2; all three lines go to several places on the motherboard and video board to provide the proper reset signals.

KEYBOARD RESET

Refer to the keyboard circuits on schematic MB4.

When you press the CRTL key and the RESET key at the same time, pins 8 and 9 of U183 will go low and force U183-10 to logic one. This is inverted at U183-4 and to U185A through the filter network, R109 and C174.

U185B and U185C double inverts the signal to provide the active-low $\overline{KBDRESET}$ pulse that couples to U201-13 (see schematic MB1). The output, U201-11, is logic zero for reset and high-impedance otherwise.

From U201-11, the reset signal is processed as described under "Power-Up Reset."

8085 CPU

PIN-OUT DESCRIPTION

The 8085 CPU, U210 on schematic MB1, is the H/Z-100 8-bit processor. Because it uses the same instruction set as the Intel 8080, the H/Z-100 maintains software compatibility with previous Heath computers.

However, this IC has some hardware differences from the 8080, so we will briefly discuss the pin-out and basic timing. If you need to know more about the 8085, see the IC data sheets elsewhere in this manual.

A8-A15 (Output, Tri-State) These are multiplexed lines. During a memory access they contain the upper 8-bits of the memory address; during an I/O operation these lines contain the port address. These lines are tri-stated during Hold, Halt, and RESET.

AD0-AD7 (Input/Output, Tri-State) These are multiplexed lines. During a memory access they first contain the lower 8 bits of the memory address. This address is then stored in external latches. The CPU next places on AD0-AD7 the input or output data associated with that address. During an I/O operation these lines first contain the port address, then the data (either input or output) associated with that port.

ALE (Output) This is the address latch enable line. This line pulses high, then low, when either the memory or I/O address is on lines A0-A7. The external circuits use the negative-going transition to latch the address information. The falling edge of ALE is also used to strobe CPU status information.

S0, S1, IO/M (Output) These lines are used in conjunction with ALE to develop the S-100 machine cycle status lines at U227. See the section "Bus Status Circuits" for more detail.

RD (Output, Tri-State) The read control line goes to logic zero to indicate that the data bus is ready to transfer data from memory or I/O to the CPU. Tri-stated during Hold, Halt, and RESET.

WR (Output, Tri-State) The write control line goes to logic zero to indicate that the data bus is ready to transfer data from the CPU to memory or I/O. Data is set up on the trailing edge of the pulse. Tri-stated during Hold, Halt, and RESET.

READY (Input) If logic zero, the CPU will enter a wait state until READY is brought to logic one again. This allows using the 8085 with slow memories or peripherals.

HOLD (Input) If logic zero, the CPU will halt operation, raise the hold-acknowledge line (HLDA), and place the following lines into a high-impedance state: Address/Data, WR, RD, and IO/M. This allows other processors, such as the 8088, to gain control of the H/Z-100.

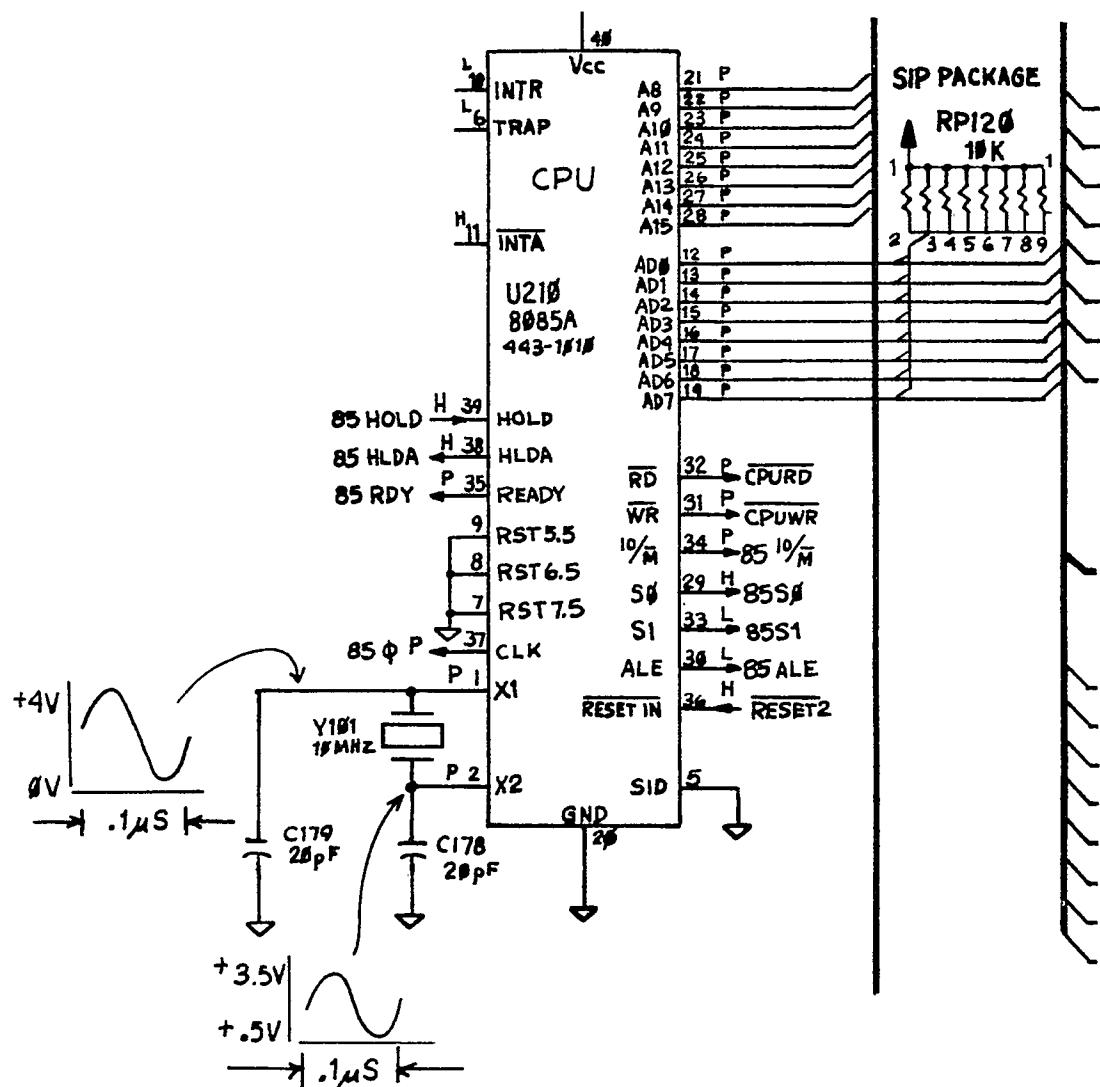
HLDA (Output) The hold acknowledge goes high to indicate that the CPU received the HOLD request and will release control of the bus in the next cycle. HLDA goes low again after the HOLD request is removed.

INTR (Input) This is the interrupt request line. If brought high, and the interrupts aren't disabled through software, the CPU will complete its current cycle and then process the interrupt. See the section "Interrupt Circuits" for more detail.

INTA (Output) The interrupt acknowledge goes low to indicate that the CPU has accepted the interrupt.

TRAP (Input) This is the nonmaskable interrupt input line. It is the highest priority interrupt and can't be disabled.

RESETIN (Input) Bringing this line low resets the computer. It sets the program counter to zero, disables interrupts, and resets the HLDA flip-flop.

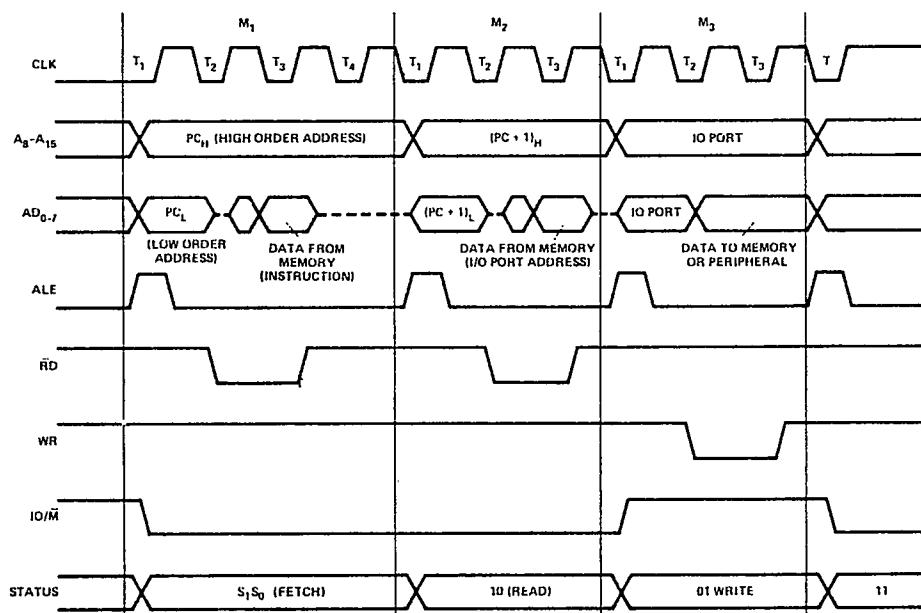


U210, 8085 CPU (MB1)

X1, X2 (Input) The clock input. The 10-MHz signal from Y101 is internally divided down to 5 MHz.

CLK (Output) The clock output. This provides 5-MHz timing to the H/Z-100 when the 8085 has control of the computer.

BASIC SYSTEM TIMING



To better understand how the H/Z-100 works, you should become familiar with the 8085 timing. The above illustration shows the waveforms that occur when the 8085 processes the OUT instruction. Though there are seven possible types of machine cycles (see the data sheets), these waveforms are typical.

During the M1 cycle, the computer fetches the op-code; in this example, the OUT instruction. The M1 cycle lasts for four clock states (T-states). During this time, A₈ through A₁₅ contain the upper 8 bits of the memory address of the instruction to be fetched.

From time T1 to T2, lines AD₀-AD₇ contain the lower 8 bits of memory address data. The ALE line goes low to strobe this information into the external address latches. The IO/M line goes low to indicate that this is a

memory-read operation. The signals on the status lines, S0 and S1, indicate that the op-code fetch cycle is taking place. The status circuitry will be covered in more detail later.

From time T2 to T3, \overline{RD} goes low and the instruction in the memory location pointed to by the address latches is placed on lines ADO-AD7, which are now acting as data lines. This data, the OUT instruction, is loaded into the computer for internal processing during time T3 to T4.

From time T3 to T4, RD goes high and ADO-AD7 goes to a high-impedance state.

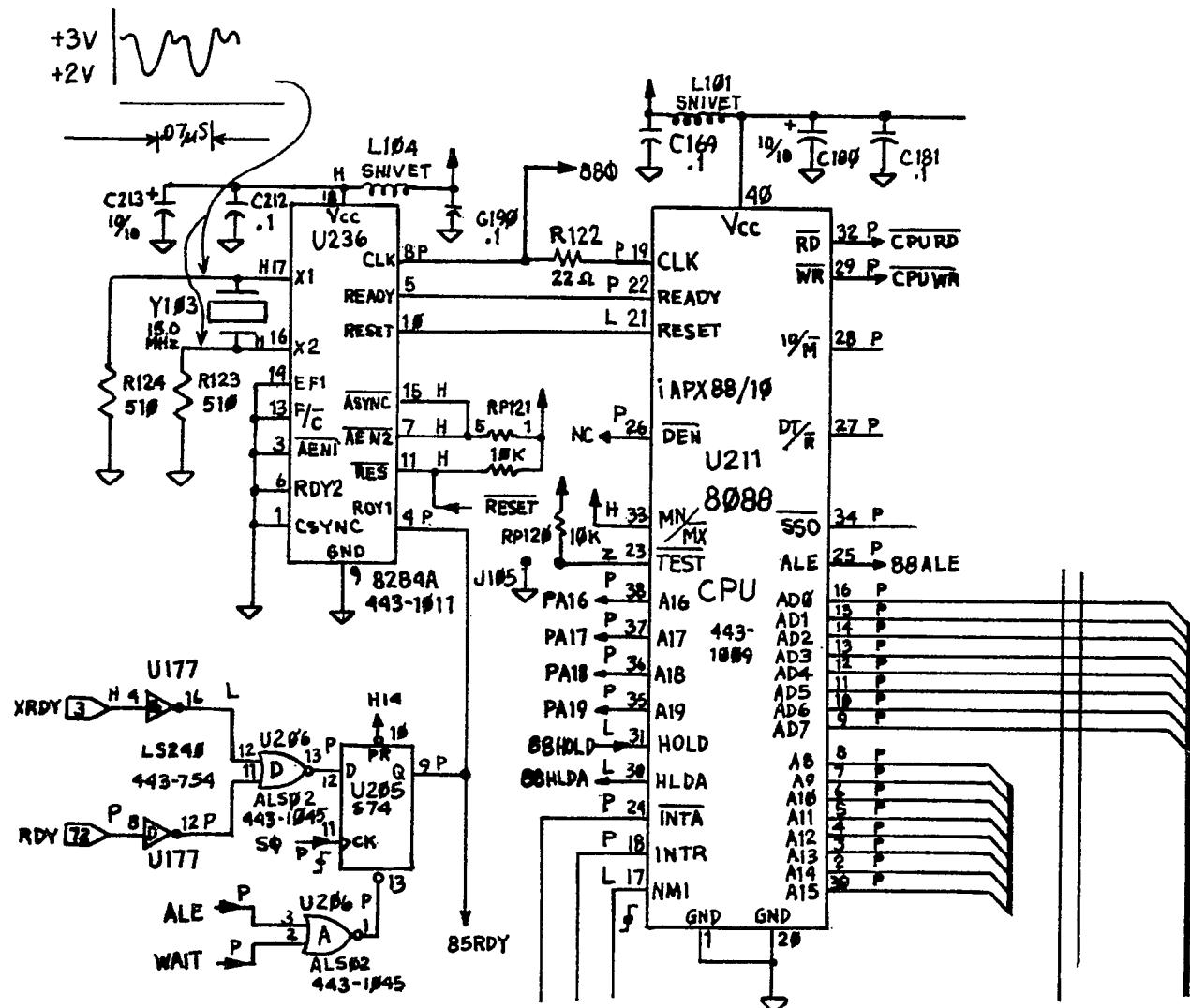
During the M2 cycle, the computer reads the data in the next memory location, which is the I/O port address the computer is to OUTput the data to. At time T1, lines A0-A15 contain the address of the memory location that holds the I/O port address. The ALE line strobes this address into the external address latches. Line $I0/\overline{M}$ is still low to indicate that the M2 cycle is a memory read cycle. This is also indicated by the logic states on status lines S1 and S0.

At time T2 to T3, \overline{RD} goes low to read the memory location pointed to by the address latches. This location contains the address of the I/O port to be accessed.

During the M3 cycle, the computer transfers the data in its accumulator to the port address specified by the M2 cycle. This time, during T1-T2, lines ADO-AD7 contain the port address fetched during the M2 cycle. Line ALE strobes this information into the external address latches. Lines AD8-AD15 also contain the port address, but aren't used in the H/Z-100. The $I0/\overline{M}$ line goes high to indicate that this cycle is an I/O cycle, rather than a memory cycle. The logic states of the status lines, S0 and S1, will indicate that this cycle is an I/O write cycle.

During time T2 to T3, the data in the accumulator of the 8085 is placed on the data bus and WR goes low to write it to the port pointed to by the address latches.

After T3, the 8085 generates another M1 cycle and fetches the next instruction in the program.



U211, 8088 CPU (MB1)

8088 CPU

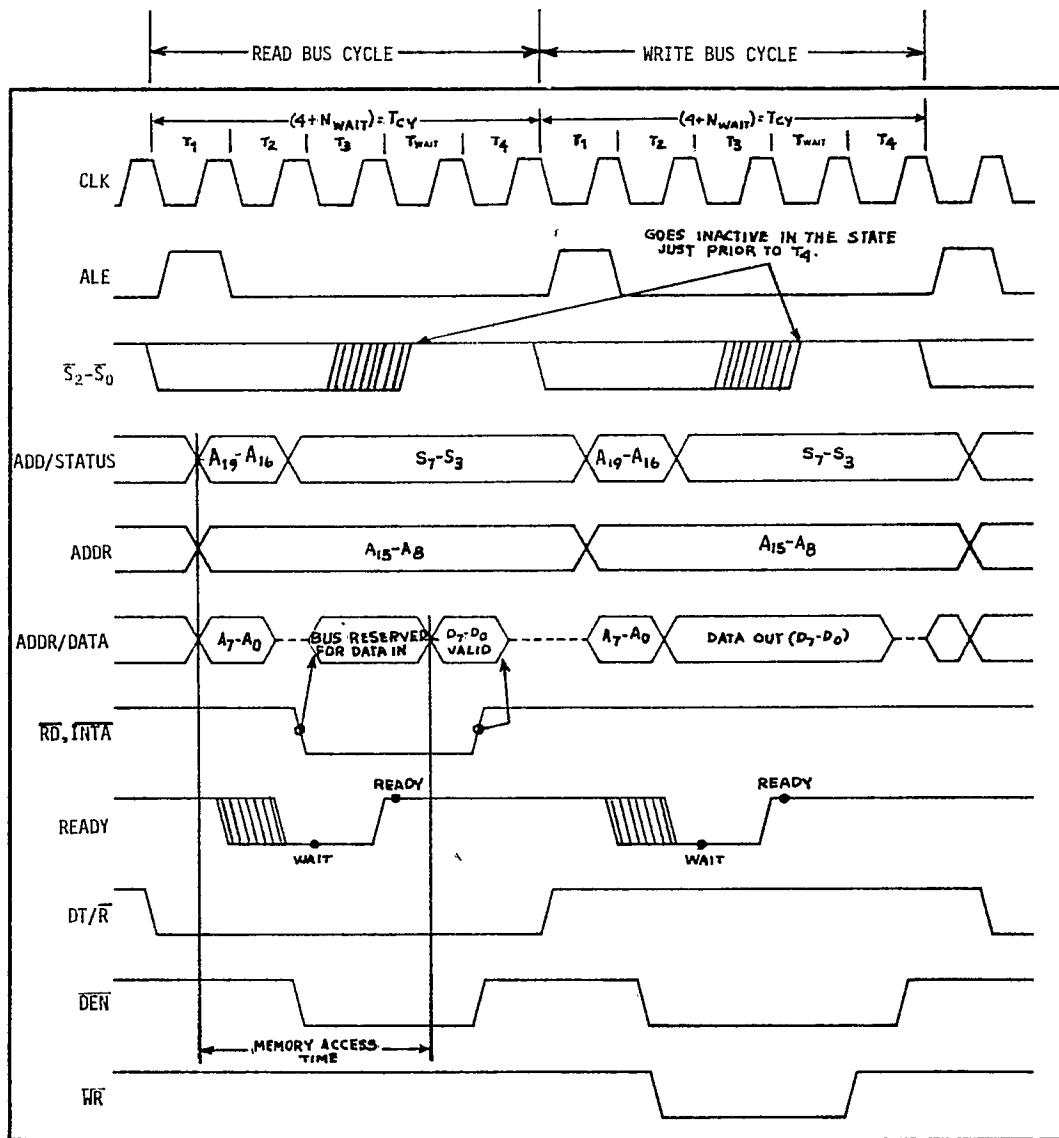
OVERVIEW

The 8088 CPU is located at U211 on schematic MB1. This IC combines the powerful resources of a 16-bit microprocessor internal architecture with the easy-to-use 8-bit bus interface. In fact, most of the functions of the bus lines are identical to the 8085 at U210, making it easy to interface both CPUs to the H/Z-100 motherboard.

The 8088 is completely software compatible with the 8086, the 16-bit bus CPU in this family. Other features are:

- Seventy basic instructions and 24 different addressing modes.
- 20-bit address bus, allowing the 8088 to directly address up to 1 megabyte of memory.
- 16-bit input/output port address range, allowing the 8088 to select up to 65536 port addresses.
- Thirteen 16-bit registers; consisting of four segment registers, four pointer and index registers, one flag register (9 bits used), and four data registers. The four data registers can also be used as eight 8-bit registers.
- Pipelined architecture to allow fetching instructions and processing previously-fetched instructions at the same time. (Understanding the instruction pipeline isn't critical for hardware troubleshooting; so it won't be discussed here. However, if you'd like to learn more about the 8088, order the "iAPX 88 Book" from Intel Corporation, Literature Department SV3-3, 3065 Bowers Avenue, Santa Clara, CA 95051. This book is also available from Heath Company Parts Department; part number 500-68.)

8088 CPU PIN FUNCTIONS



Refer to the accompanying set of waveforms and U211 on schematic MB1 as you read this.

RD, Pin 32 Read Strobe: This line goes low at time T₂ when the CPU reads from memory or an I/O port. This signal goes to a high-impedance state during hold acknowledge.

WR, Pin 29 Write Strobe: This line goes low when the CPU writes to memory or an I/O port. This signal goes to a high-impedance state during hold acknowledge.

IO/M, Pin 28 Status Line: This line goes low during a memory read or write (RD or WR asserted). It goes to logic one for an I/O read or write. It's tri-stated during hold acknowledge. (Also see the description on the S-100 bus status circuits.)

DT/R, Pin 27 Data Transmit/Receive: This line is similar to IO/M. It's used in the H/Z-100 to develop the S-100 bus status circuits. It goes low during a read operation and high for write. It is tri-stated during hold acknowledge.

SSO, Pin 34 Status Line: This line is used with DT/R and IO/M to develop the S-100 status circuit signals. The logic levels on this line depend on what type of instruction the CPU is processing. See the status circuit description elsewhere in this manual. This line is brought to a high-impedance state during hold acknowledge.

ALE, Pin 25 Address Latch Enable: This line pulses high when the CPU places the address information on the address/data bus. In the H/Z-100, this line clocks the address into external latches on the negative-going edge of ALE.

ADO-AD7, Pins 16-9 Address/Data Bus: When ALE is asserted, these lines contain the lower 8 bits of the 20-bit address. This can be a memory address or an I/O port address. From time T3 to T4, these lines contain the input or output data. Demultiplexing circuits in the H/Z-100 are used to separate the data and address information. These lines are tri-stated during hold acknowledge.

A8-A15, Pins 2-8 & 39 Address Bus: These lines carry the next 8 bits of the address. This is memory address during a memory access and I/O address during a port access. These lines hold the address during the entire bus cycle. They're tri-stated during hold acknowledge.

NMI, Pin 17 Non-maskable Interrupt: A positive-going transition on this line will interrupt the CPU. It can't be blocked with software. The CPU will complete its current instruction and then service the interrupt.

INTR, Pin 18 Interrupt Request: The CPU tests this line during the last clock cycle of each instruction to see if some device is requesting an interrupt. If pin 18 is logic one, then an interrupt request is taking place. The CPU will process the interrupt unless the interrupt is masked by software.

INTA, Pin 24 Interrupt Acknowledge: The CPU brings this line to logic zero to inform the interrupting device that it's processing the interrupt. It's used as a read strobe to get vector information from the interrupt circuits (see the interrupt circuit description for more details).

HLDA, Pin 30 Hold Acknowledge: Goes high to indicate that the CPU has acknowledged a hold request at pin 31. See the description of the processor swap port for more details.

HOLD, Pin 31 Hold Request: This line goes high when another device requests control of the H/Z-100; such as when the 8085 is the active processor. The CPU will assert the HLDA line and suspend operation. See the description of the processor swap port for more details.

A19-A16, Pins 31 & 35-38 Address/Status Bus: From time T1 to T2, these lines hold the top 4 bits of the 20-bit address bus. ALE clocks this value into external latches when it returns to zero. The CPU then places the bus cycle status information on these lines. This feature isn't used in the H/Z-100 since the status information is developed in a different manner. See the description on the status circuits. These lines are tri-stated during hold acknowledge.

TEST, Pin 23 Test Input: This input is examined by the "wait for test" software instruction. If pin 23 is low, execution continues, otherwise the processor waits in an idle state.

MN/MX, Pin 33 Minimum/Maximum: Logic one on this pin places the 8088 in the minimum mode, the mode used by the H/Z-100. When placed in the maximum mode, some of the pin functions change. Usually, the maximum mode is used for larger systems and multi-processing systems.

RESET, Pin 21 Reset: Goes high to reset the 8088. The interrupts are disabled, certain registers in the 8088 are set or cleared, and the instruction pointer (program counter) points to the memory address 16 bytes below the top end of the 1 megabyte range (FFFF0H).

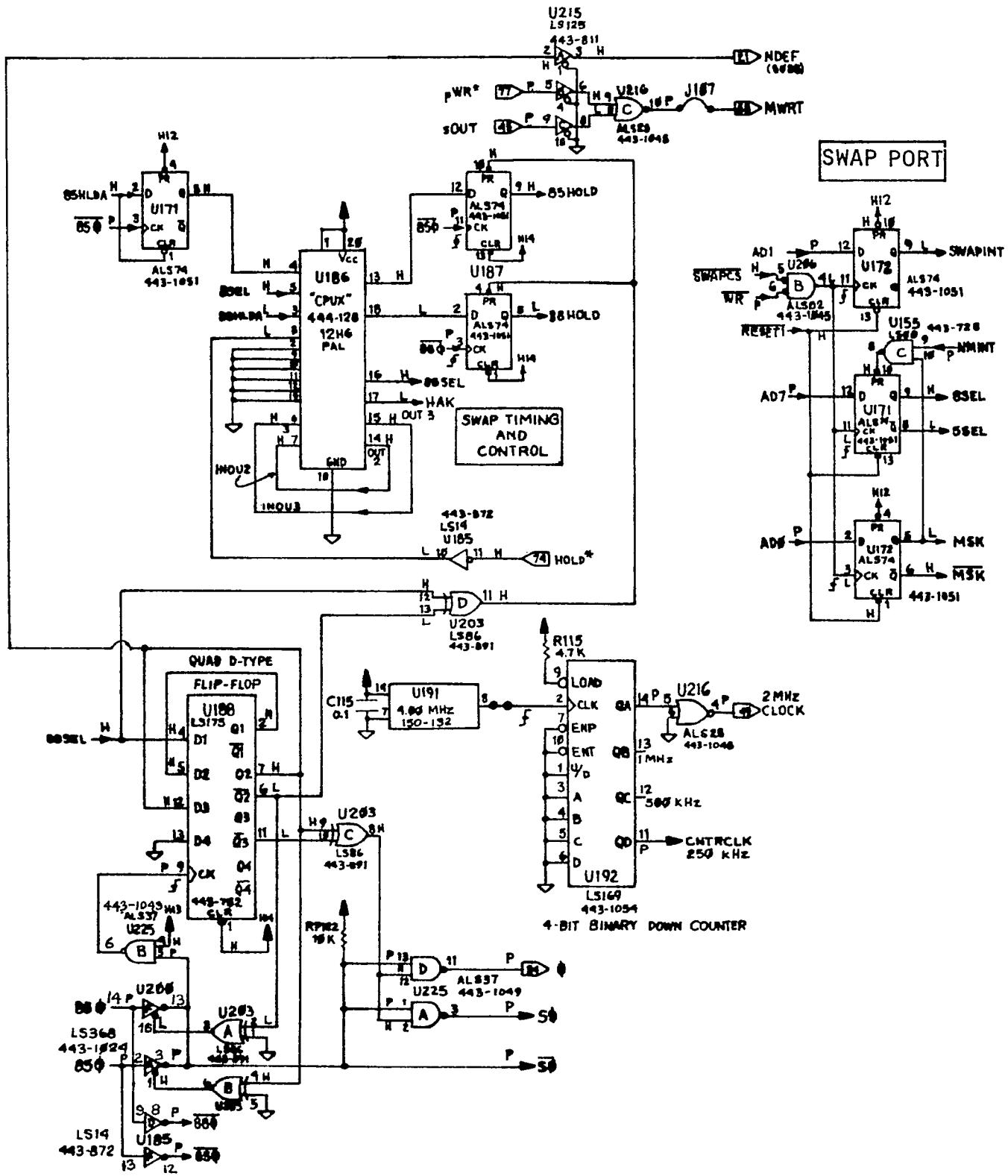
This line is asserted when the RESET line at U236-11 is pulled low. A Schmitt trigger shapes this signal and the clock circuits retimes it before applying it to the 8088.

READY, Pin 22 Ready: This is an acknowledgement signal from the addressed memory or I/O port that it is ready to transfer data. When this line is low, the CPU goes into a wait state until the addressed device brings it high. This allows using the 8088 with slow memory or I/O devices.

The READY signal is generated when U205-9 places a logic one on U236-4. U236 synchronizes this signal with the 8088 clock to ensure correct set up and hold times.

CLK, Pin 19 8088 Clock Input. Five-megahertz clock to provide timing to the 8088.

This signal comes from U236-8 which derives it from the 15-MHz crystal at Y103. Duty cycle is about 33% for optimized timing inside the 8088. When the 8088 is the active processor, this line also goes to the processor swap port as 880 to provide system timing.



PROCESSOR SWAP PORT (MB1)

PROCESSOR SWAP PORT

OVERVIEW

The processor swap port controls which CPU is to be active, handles interrupt routing, and ensures proper timing of the clock circuits during the swap. To access the swap port, the CPU writes a control byte to port OFEH. Only three bits of the byte are used: AD0 controls the interrupt mask, AD1 controls the swap interrupt line, and AD7 performs the processor swap.

PROCESSOR SWAP

Refer to schematic MB1 as you read the following.

At power up, the reset circuits clear U171-9 to logic zero. This pin, 8SEL, connects to U186-5, a 12H6 PAL. This IC responds by placing a logic zero on U187-12 and a logic one on U187-2. On the first positive transition of 85⁰, the 85HOLD line will go low, enabling the 8085 CPU. On the first positive transition of 88⁰, the 88HOLD line will go high, disabling the 8088 CPU.

The 8085, while executing the code in the monitor ROM, soon transfers control to the 8088. It does this by setting bit 7 of the processor swap port control byte to logic one. Here's how...

The CPU addresses port OFEH to assert SWAPCS (from the I/O decoder) at U206-5. It then sets AD7 to logic one at U171-12. Finally, it asserts the write line at U206-6. As a result, U171-11 goes high and latches U171-9 to logic one. The 8SEL line is now asserted.

The values at U172-12 and U172-2 are also latched to their respective outputs, but these will be covered later.

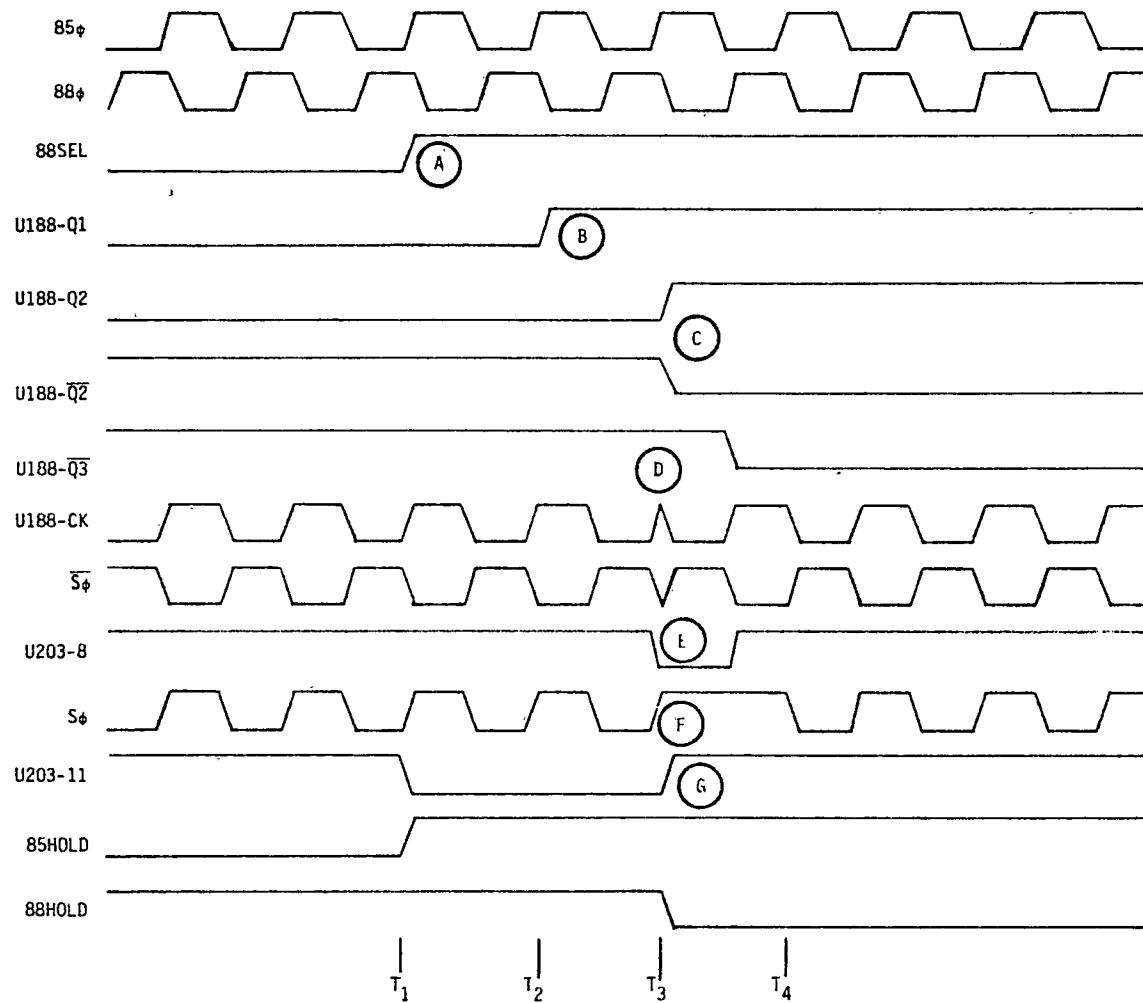
The 8SEL line, now logic one, causes U186-13 to change to logic one, U186-18 to change to logic zero, and U186-16 to change to logic one.

The HOLD* line at U185-11 asserts whenever a board on the S-100 bus takes control of the H/Z-100. This causes U186 to disable both the 8085 and the 8088 through U187. Both CPUs respond by returning their hold-acknowledge signals; the 8088 at U186-3 and the 8085 at U171-2. When this happens, U186 asserts the HAK line at pin 17. This, in turn, raises the S-100 pHLDA line to logic one at U180-9. The board that generated the HOLD* request can now take control of the H/Z-100.

SWAP TIMING

The 88SEL line also goes to U188-4, a quad D-type latch. This circuit is designed to suppress any glitches on the system clock line when the H/Z-100 switches from one CPU to the other. It also ensures that the CPU being disabled is no longer active when the other CPU is enabled.

The 8085 and the 8088 run on separate crystal-controlled clocks; the 8085 from Y101 and the 8088 from Y103. Although these clocks are stable, they aren't in phase. Switching from one clock to another can cause a glitch on the system clock line, S₀, which can upset the timing in other circuits.



SWITCHING FROM 8085 to 8088

To see how U188 and its associated circuits block this spike, refer to the waveforms on the previous page.

The two top waveforms are the respective clocks for the 8085 and 8088 CPUs. These are present at the inputs of inverters U200-2 and U200-14. Assuming that the 8085 is the active processor, then U200-1 is low and 85ϕ couples through the inverter to form $S\phi$. It also couples through U225B to clock U188.

At time T1, the 8088 is selected; the 88SEL line goes to logic one as shown at A on the waveforms illustration. The next clock pulse at U188-9 latches this logic one into U188-2, the Q1 output at B.

The next clock pulse causes the Q2 output to latch high, shown at C. This tri-states U200 through the exclusive-OR gate at U203B. At the same time, $\bar{Q}2$ goes low to couple the 88ϕ clock to the $S\phi$ line. Since, in this example, the two clocks are nearly 180-degrees out of phase, the clock immediately returns to zero, causing the spike at D in the waveforms illustration.

Up until this time, the output of U203-8, another exclusive-OR gate, has been logic one. This is because its inputs Q2 and $\bar{Q}3$ of U188 have been in opposite states. However, since Q2 went low at time T3, both inputs to U203C are the same, causing U203-8 to go to logic zero (waveform E). This forces the system clock output at U225-3 to logic one until time T4 (waveform F).

At time T⁴, the first positive-going edge of the 8088 clock causes the $\overline{Q3}$ output of U188 to go high. This opens the gate at U225A to pass the system clock, which is now the 8088 signal.

As mentioned earlier, the other function that 88SEL and U188 perform is to ensure that the CPU being disabled is completely disabled before the other CPU is activated. To see how this is done, again refer to the waveforms illustration.

Once again, assume that the H/Z-100 is switching from the 8085 to the 8088. At time T¹, the 88SEL line goes high, which is coupled to U203-11. The other input of this exclusive-OR gate is the Q2 line from U188. Since both inputs are now the same state, U203-11 goes to logic zero to preset both HOLD latches at U187.

Both CPUs respond by going into a HOLD state and sending hold-acknowledge signals to U186; the 8088 to pin 3 and the 8085 to pin 4 through U171. This asserts HAK at pin 17 which drives the S-100 pHLDA line at U180-9.

At time T³, the $\overline{Q2}$ line goes low and U203-11 returns to logic one, thus releasing the latches at U187 from their preset states. The next 88⁰ clock pulse latches the logic zero at U187-2 into U187-5, removing the 8088 from the hold state.

Also at this time, U188-7 goes high to drive U215-3 high. This last IC connects to pin 21 of the S-100 bus to form the NDEF (8088) line. This line is a "not-to-be-defined" line that can be used for any function by the computer manufacturer. For the H/Z-100, this line asserts when the 8088 is active.

INTERRUPT MASK

The interrupt mask circuits ensure that interrupt requests are sent to the currently active CPU. The mask bit, MSK, is set or cleared by setting or clearing bit 0 of the processor swap port. If set, and the 8085 is active, the 8085 gets all interrupt requests. If cleared, and the 8085 is active, the interrupt request is blocked. However, the swap port will disable the 8085 and enable the 8088. If the 8088 is active, all interrupt requests are sent to the 8088 regardless of the mask bit. Here's how it's done...

Immediately after reset, the 8085 CPU is the active processor. Control lines 5SEL at U171-8 and MSK at U172-6 are logic one. These two lines connect to U225-9 and U225-10, shown near the 8085 IC on the schematic. U220-2 inverts the resulting logic zero to enable U189A and U189D. So all interrupts are sent to the 8085; maskable through U189A, non-maskable through U189D.

The 8SEL line, which is the complement of 5SEL, disables U189B and U189C, the AND gates to the 8088. Later, when the 8085 hands control to the 8088 CPU, 8SEL will go high and 5SEL will go low.

If, while the 8085 is selected, the $\overline{\text{MSK}}$ line is set to logic zero, U220-2 disables U189A and U189D. This blocks the interrupt request from both the 8085 and the 8088. However, if an interrupt request should occur, either standard or NMI, U156-6 will go high to assert the NMINT line.

The NMINT line connects to U155-9 in the processor swap port. The other input is the MSK line which is also high. As a result, U155-8 goes low to assert the 8SEL line. The H/Z-100 swaps to the 8088 processor as described previously.

When the 8088 CPU is active, 8SEL is high to enable U189B and U189C. U189A and U189D are disabled because 5SEL is logic zero at U225-9. So, no matter what the setting of the $\overline{\text{MSK}}$ bit at U225-10, all interrupt requests will be routed to the 8088 processor.

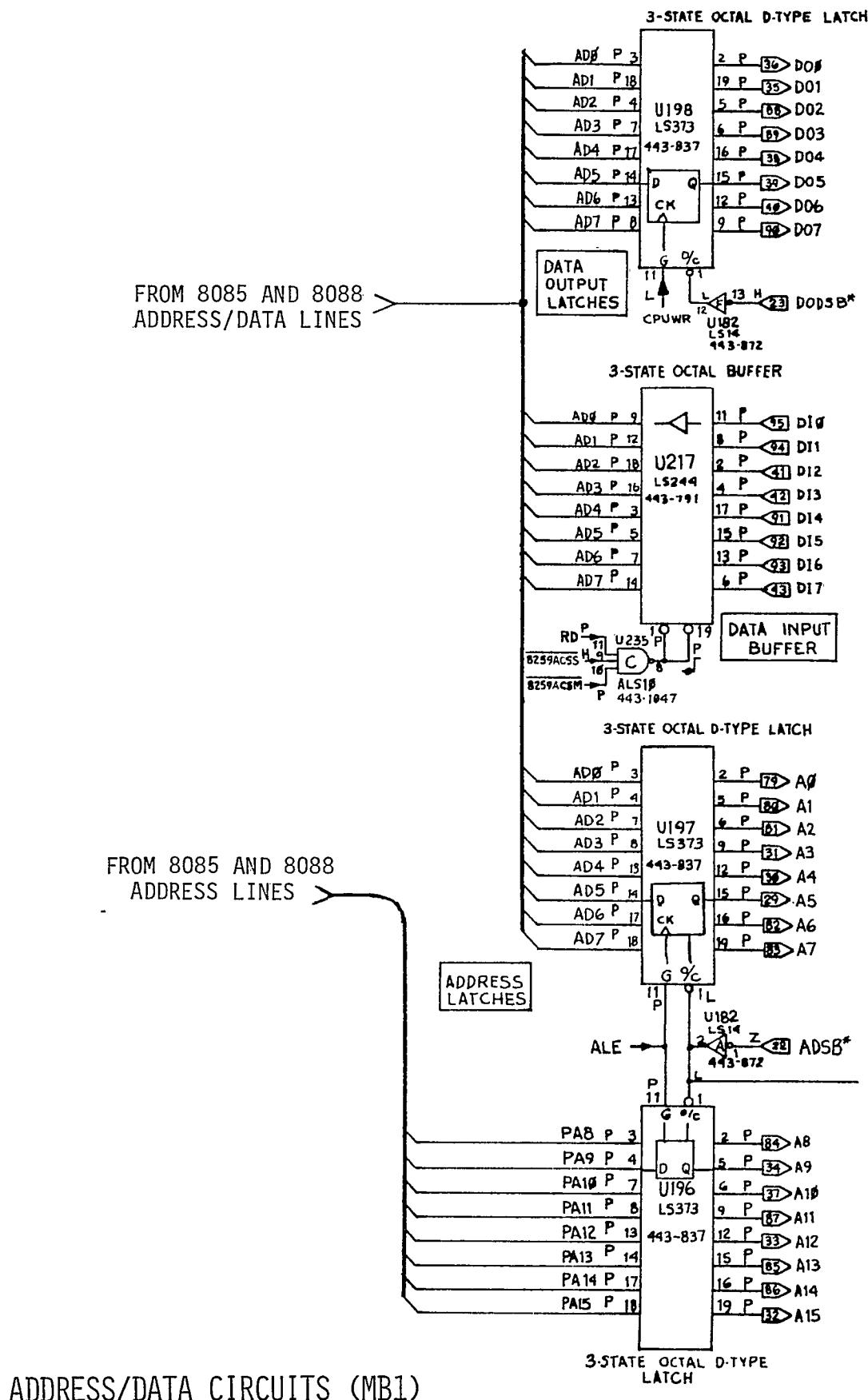
SWAP INTERRUPT

When either CPU is in the hold state, it retains the contents in its registers. So, when that CPU is again enabled, it will begin processing where it left off.

To start the disabled CPU at a different memory location than where it was when it was turned off, the active CPU can generate a swap interrupt command. The active CPU does this by selecting the proper interrupt vectors, performs an interrupt-disable upon itself (through software), and then asserts the SWAPINT line.

To generate the swap interrupt command, the computer sets bit 1 to logic one in the processor swap port. It does this by asserting SWAPCS (from the I/O decoder) at U206-5, setting AD1 to logic one at U172-12, and then asserting the WR line at U206-6. U206-4 goes high to latch U172-9 to logic one, sending the SWAPINT command to the interrupt circuits.

At the same time, the CPU also writes the correct control bits to 8SEL and MSK on the processor swap port. The H/Z-100 changes CPUs, finds that the SWAPINT line is asserted, and jumps to the correct location to process the interrupt.



ADDRESS/DATA CIRCUITS

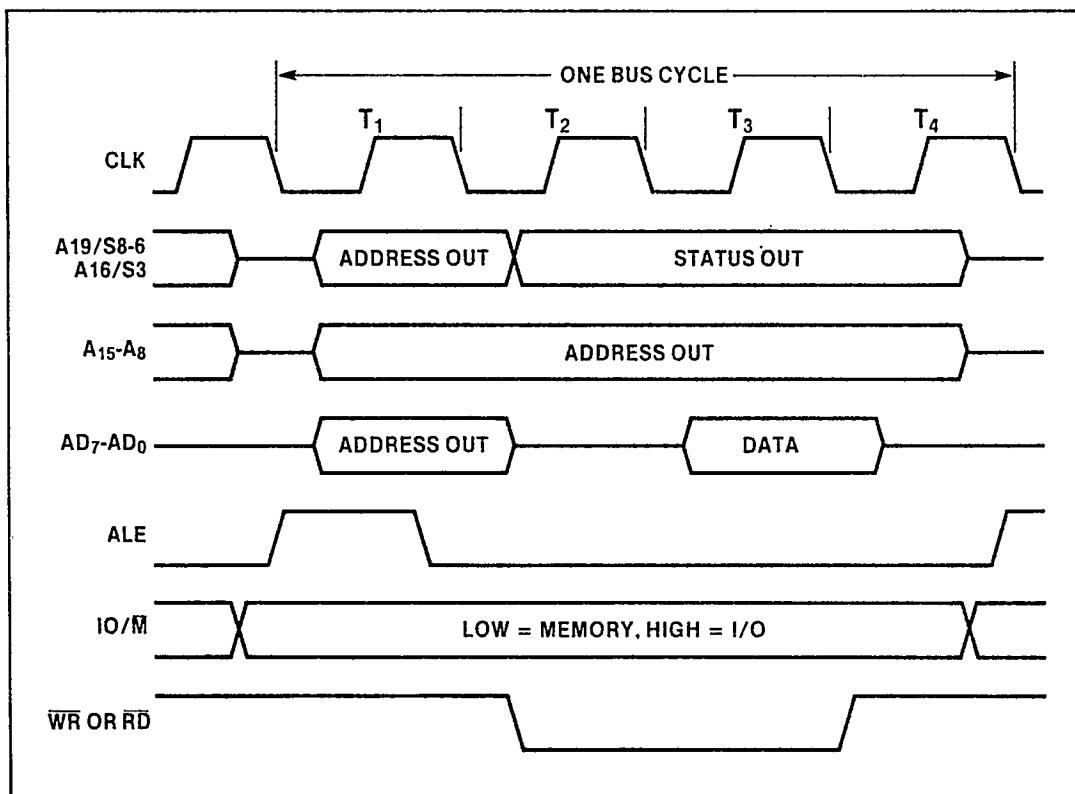
OVERVIEW

As stated in the discussions on the 8085 and the 8088, the address and data lines of these CPUs are multiplexed onto the same bus. That is, first the address is present on the bus, then the data. It's up to a control line called the address latch enable, or ALE, to separate these signals and send them to their appropriate latches.

Refer to schematic MB1 as we explain how.

Under normal operation, the CPU selection logic will enable either the 8085 CPU or the 8088 CPU. Although the address/data lines of these processors are connected in parallel, the bus of the disabled processor will be tri-stated and so will not interfere with the active CPU.

ADDRESS LATCHES



In the following description, we'll use the 8088 waveforms. Although these are slightly different than the 8085 waveforms, the description applies to both.

At the beginning of clock cycle T1, the 8088 asserts the 88ALE line at U211-25. This signal couples through the OR gate at U221-1 to pin 11 of U197 and U196, two tri-state, octal D-type latches.

A short time later, the 8088 places address data on the address lines. The lower 8 bits, AD0-AD7, go to U197 and the upper 8 bits, PA8-PA15, go to U196. These latches are transparent as long as the ALE line is high; that is, the output logic levels are the same as the input logic levels. At the end of T1, ALE goes low to latch the outputs with the address.

The line going to pin 1 of U197 and U196 provides S-100 compatibility. If an external processor or DMA device were plugged into one of the S-100 slots, and it wanted to take control of the H/Z-100, it would assert ADSB* low. This would tri-state U197 and U196, thus isolating the 8085 and 8088.

DATA LATCHES

If the CPU is writing data, either to memory or to an output port, it asserts the WR line at U211-29. This signal is inverted by U220-12 (in the center of the schematic) to form the CPUWR control signal. CPUWR connects to the data output latch at U198-11 and holds this latch transparent as long as CPUWR is high.

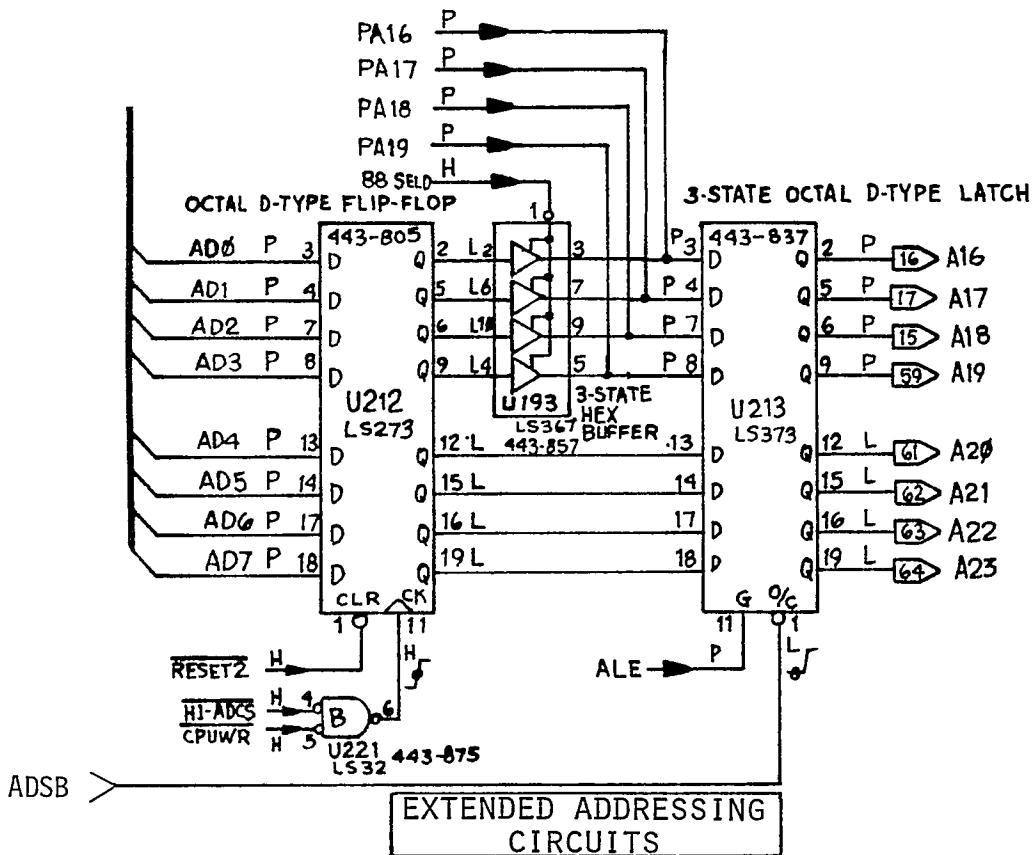
During time T3, the CPU places the data on bus lines ADO-AD7, which couple through U198 to the S-100 bus. At time T4, CPUWR goes low to latch this data onto D00-D07. From here, the data will be sent to the location pointed to by the address on the outputs of U197 and U196.

U198-1 is the inverted version of DODSB* from the S-100 bus. This signal functions in the same manner as ADSB*.

If the CPU is reading data, either from memory or an input port, its timing is the same as when it writes data. However, this time it asserts the RD line at pin 32 of the 8088. This control line is inverted by U220-4 to form RD (located near the top center of the schematic).

Control line RD connects to U235-11, a 3-input NAND gate, at the data input buffer, U217. The other two inputs to U235C, 8259ACSS and 8259ACSM are from the interrupt circuits and won't go low unless an interrupt occurs (see the interrupt circuit description for more details). During a data read, RD is high, so U235-8 is low, and the octal buffer, U217, passes the data on bus lines D10-DI7 to ADO-AD7. At time T3 the CPU assumes that the data is stable and loads it into the accumulator.

EXTENDED ADDRESSING



The extended addressing circuits, U193, U212, and U213, maintain S-100 compatibility by making it possible for the CPU to address up to 16 megabytes of memory.

When the 8088 is active, 88SEL is high to tri-state U193. The 8088 extended address lines, PA16-PA19, connect to pins 3, 4, 7, and 8 of U213. When ALE asserts at U213-11, these address values are coupled to the S-100 bus. Lines A20-A23 are logic zero because the outputs of U212 have not changed from their cleared condition. In this case, the 8088 is operating normally and can directly address its natural one-megabyte range.

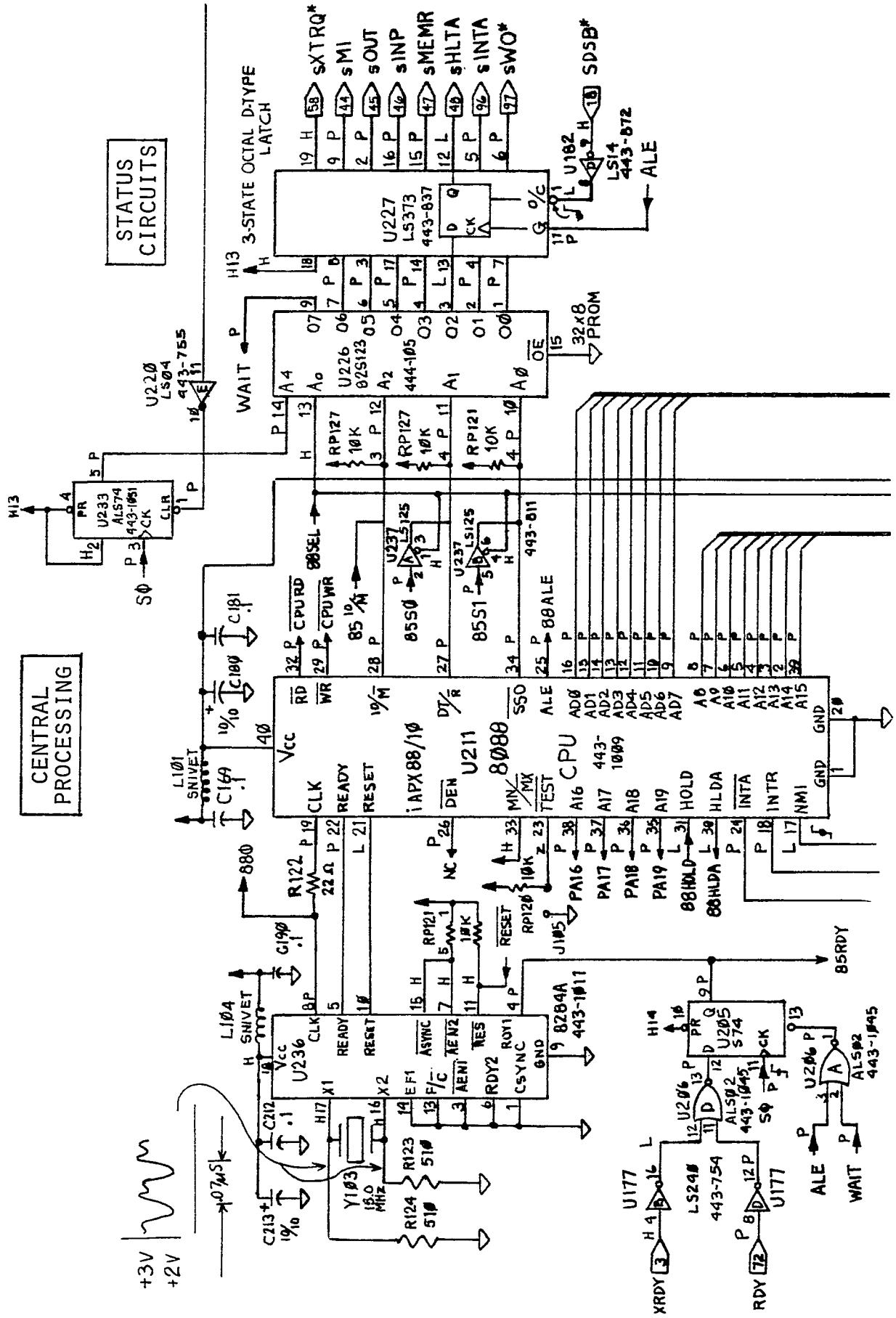
To access the address space above 1MB, the CPU asserts HI-ADCS from the I/O port decoder (U159 on MB2). Then CPUWR asserts and U221-6 goes low. Finally, the extended address is placed on lines AD4-AD7 at U212. (Lines AD0-AD5 are blocked by U193 while the 8088 is active.)

At the end of that cycle, the CPUWR line goes high and latches AD4-AD7 onto the outputs of U212.

At the beginning of the next machine cycle, when ALE again asserts, the outputs of U212 will latch into U213. For example, if U213-12 is logic one and pins 15, 16, and 19 are zero, the CPU will be in the one-megabyte to two-megabyte range.

These circuits work the same way if the 8085 is the active CPU. The only difference is that 88SEL at U193 is low so that the lower four bits of U212 couples directly to U213. This allows the 8085 to address memory between 64K and 16M. (When the 8085 is active, lines PA16-PA18 from the 8088 are tri-stated.)

Note, however, that once the CPU jumps to these higher ranges it can't return unless there is a program there to tell it to return. This is because U212 and U213 are latches and can only be changed by writing to the high-address port (or through a hard reset). One possible way around this is to preload a program in higher memory by using direct memory access.



BUS STATUS CIRCUITS (MB1)

S-100 BUS STATUS CIRCUITS AND WAIT TIMING

BUS STATUS

The IEEE-696 S-100 bus contains 8 status lines; these lines assert to indicate what machine cycle the computer is in. The H/Z-100 uses all but one of these lines. However, the unused line, sXTRQ*, is still available for use by plug-in boards.

Following the S-100 standard, the status lines are prefixed with a lowercase s. All but two of the lines, sWO* and sXTRQ*, assert on logic one. Briefly, here's what each status line does:

sXTRQ* Sixteen-bit request. This line allows 8-bit and 16-bit boards to share the same bus. Since the H/Z-100 is an 8-bit machine externally, and a 16-bit machine only inside the 8088, this line is disabled by connecting U227-18 to logic one.

However, if a true 16-bit CPU board is plugged into the S-100 bus, the H/Z-100 can be programmed to give control to this CPU, and this CPU can perform 16-bit transfers with other 16-bit boards on the bus.

It does this by asserting sXTRQ* and addressing the 16-bit board (U227-19 is tri-stated at this time by a high at U227-1). If the addressed device can process 16-bit words, it will assert another S-100 line called SIXTN*. Next, the data buses are ganged together; lines D00-D07 handle DATA0-DATA7 while lines D10-DI7 handle DATA8-DATA15. The data transfer takes place.

If the device can't process 16-bit words, such as memory and I/O on the motherboard and video board, then SIXTN* remains high. In this case, DO and DI lines operate normally and the CPU must process the data a byte at a time.

sM1 Opcode fetch. This line asserts when the H/Z-100 fetches a new instruction from program memory. It returns to logic zero at the end of the M1 machine cycle.

sOUT Write to output port. This line asserts to indicate that the CPU is going to send data to a previously-addressed output port.

sINP Read from input port. This line asserts to indicate that the CPU is going to read data from a previously-addressed input port.

sMEMR Memory read. This line asserts to indicate that the CPU is going to read data from the addressed memory location.

sHLTA Halt acknowledge. This line asserts when the CPU processes a HALT command and has stopped executing the program.

sINTA Interrupt acknowledge. This line asserts when it is processing an interrupt.

sWO* Memory write. This line asserts when the CPU is going to write data to a previously-addressed location in memory.

These lines are derived from the status lines of whichever CPU is active. In the 8088, these lines are IO/M, DT/R, and SSO. In the 8085, these lines are IO/M, S1, and S0.

When the 8088 is active, the 88SEL line at U226-13 is logic one. This causes the 32 x 8 PROM to correctly decode the bit pattern on pins 10, 11, and 12 as an 8088 status code. As you'll see later, this code is different for the 8085.

88SEL also tri-states 85S0 and 85S1 at pins 1 and 4 of U237. The line from 85IO/M is in a high-impedance state when the 8085 is disabled, so doesn't need a buffer.

U226 decodes the machine cycle status and asserts the correct line on the output, U226-1 through U226-7. When the ALE line goes low, the outputs of U226 are latched into U227.

When the 8085 is active, the 88SEL line at U226-13 is logic zero. This causes U227 to correctly decode the bit pattern on pins 10, 11, and 12 as an 8085 status code. U226 decodes this status which is subsequently latched into U227 when ALE goes low.

The following chart shows the status codes of each CPU and what S-100 status line each code affects.

8085			8088			S-100		
IO/M	S1	S0	Status	IO/M	DT/R	SSO	Status	Status
0	1	1	Opcode fetch	0	0	0	Code access	sM1
1	0	1	I/O write	1	1	0	Write I/O port	sOUT
1	1	0	I/O read	1	0	1	Read I/O port	sINP
0	1	0	Memory read	0	0	1	Memory read	sMEMR
1	0	0	HALT	1	1	1	HALT	sHLTA
1	1	1	Interrupt Ack.	1	0	0	Interrupt Ack.	sINTA
0	0	1	Memory write	0	1	0	Write memory	sWO*

WAIT TIMING

The WAIT line at U226-9 equalizes the timing characteristics between the 8085 and 8088. It does this by adding the appropriate wait states during a memory or I/O access. The number of wait states depends on the active CPU and the type of access.

	8085 Active	8088 Active
Memory Access	1 wait state	0 wait state
I/O Access	2 wait states	1 wait state

U233-5 provides the basic wait timing. When ALE asserts, U233-5 is cleared. After ALE goes low, U233-5 will go high on the next system clock pulse. If the machine cycle is a memory or I/O access, the wait line will assert according to the above chart.

The asserted wait line is inverted by U206A to clear U205-9. This logic zero couples directly to the 8085 READY input and indirectly to the 8088 READY input through U236. The active CPU will go into a wait state until the next system clock pulse at U205-11. Operation will then proceed normally.

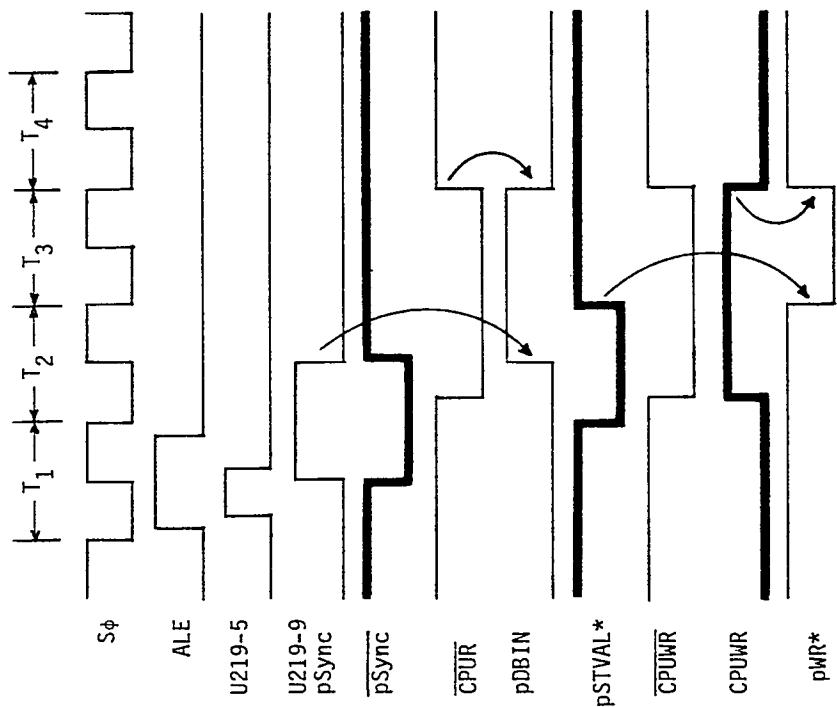
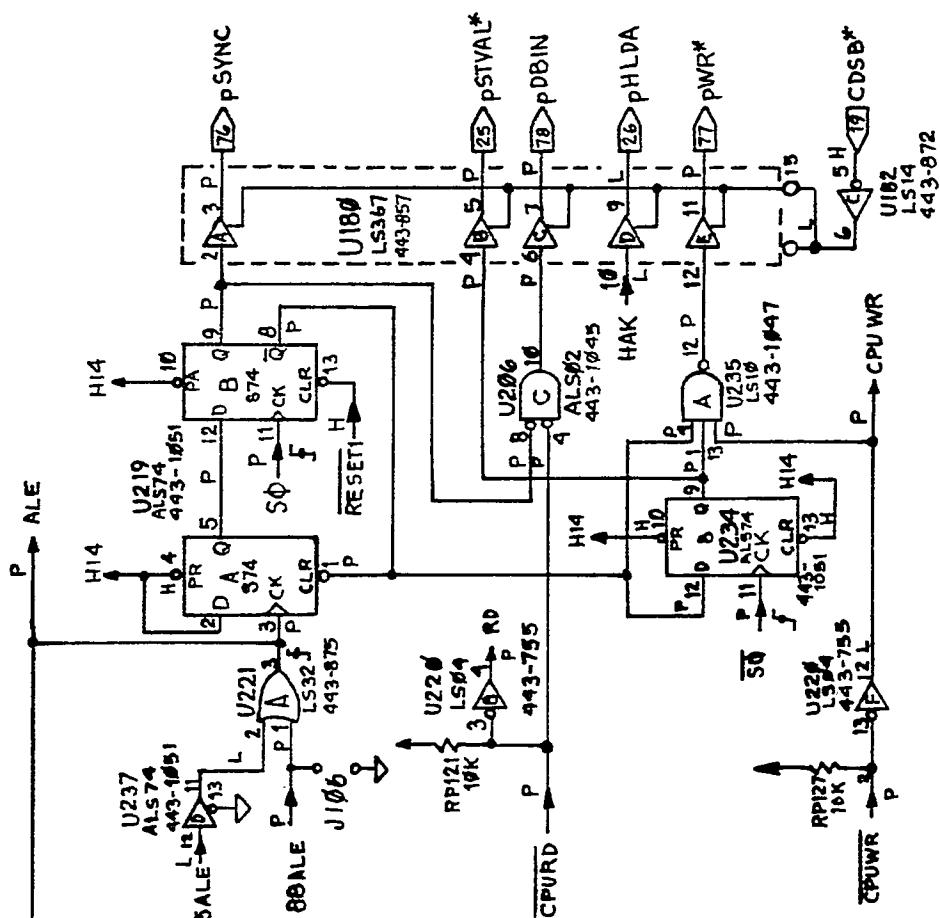
The RDY and XRDY lines are S-100 ready lines. If either line is low, the CPU will go into a wait state at the end of a machine cycle. Here's how:

The ALE line clears U205 at the beginning of each machine cycle. Both RDY and XRDY are normally logic one, which places a logic one at U205-12. Unless the wait line is asserted, the next system clock pulse will latch U205-9 to logic one; ensuring that the active CPU will not generate a wait state during that machine cycle.

If either RDY or XRDY should go low, U205-9 remains at logic zero during that bus cycle. This causes the CPU to go into a wait state at the end of the cycle. See the 8085 and 8088 specification sheets for exact timing relationships.

We'll discuss the uses of the RDY line in the H/Z-100 in the circuit descriptions on the dynamic memory, video board, and floppy disk controller board.

**BUS CONTROL
OUTPUT CIRCUITS**



BUS CONTROL OUTPUT CIRCUITS (MB1)

BUS CONTROL OUTPUT CIRCUITS

The five lines of the bus control output circuits determine the timing and movement of data during any bus cycle. The mnemonics of these lines always begin with a lowercase p. Refer to the accompanying waveforms (8088 timing) and schematic MB1 as we discuss each.

pSYNC

This line goes high to indicate the start of a new bus cycle. Basically, it's the ALE signal of the currently active CPU retimed to the rising edge of the system clock.

In the 8088, the ALE line goes high at the beginning of the bus cycle. This couples through U221A to latch a logic one on U219-5. Halfway through time T1 the system clock goes high at U219-11, causing U180-3, the pSYNC output, to go high.

At the same time that pSYNC asserts, U219-8 goes low to clear U219A at pin 1.

During time T2, the next positive-going edge of the system clock latches U219-9 to logic 0; the pSYNC line is no longer asserted and U219A is no longer held cleared.

pSTVAL*

The pSTVAL* line works in conjunction with pSYNC to indicate when the S-100 address and status lines are stable.

Inverted pSYNC couples from U219-8 to U234-12 and inverted system clock connects to U234-11. Between time T1 and T2, the inverted pSYNC is logic zero. The rising edge of $\overline{S\phi}$ latches this onto U234-9, which is buffered through U180B to form the pSTVAL* signal.

On the next rising edge of $\overline{S\phi}$, between T2 and T3, the inverted pSYNC has returned to logic one; this is coupled through U234B and U180B to the pSTVAL* line.

pDBIN

This is a generalized read strobe that gates data from memory (or an input port) to the data bus.

The pDBIN signal is derived by NORing CPURD and pSYNC at U206C. This ensures that pDBIN won't assert until after the negative-going edge of pSTVAL*.

pHLDA

This is the hold acknowledge signal; it goes high when both the 8088 and the 8085 are in a hold state. Such a situation can occur if a board plugged into the S-100 bus must take control of the bus, such as when a DMA transfer is to take place.

The device requesting control of the bus asserts the S-100 HOLD* line at U185-11 (lower right on the schematic). U186-8 detects this logic zero and will write logic ones to U187-9 and U187-5. These lines send HOLD commands to the 8085 and 8088 CPUs.

In our example, the 8085 is already in a hold state, so the 85HOLD line is already high. When the 8088 CPU detects the asserted 88HOLD line, it finishes the current instruction and indicates a hold acknowledge status by asserting 88HLDA at U186-3.

Now that both 88HLDA and 85HLDA are asserted, U186-17 goes high. This line, HAK, couples through U180D to form pHLDA.

See the description on the processor swap port for more information on U186.

pWR*

This is a generalized write strobe that writes data from the data bus into memory or an output port. It's timed with pSYNC and pSTVAL* to ensure that the address lines are stable before a write takes place.

The CPU write command is inverted through U220-12 and applied to U235-13, a three-input NAND gate. The pSTVAL* line connects to pin 1 of this gate and prevents a write from taking place until the address lines are stable. The inverted pSYNC, at U235-2, ensures that a pulse doesn't occur on the pWR* line if the CPU write command should assert before pSTVAL* goes low.

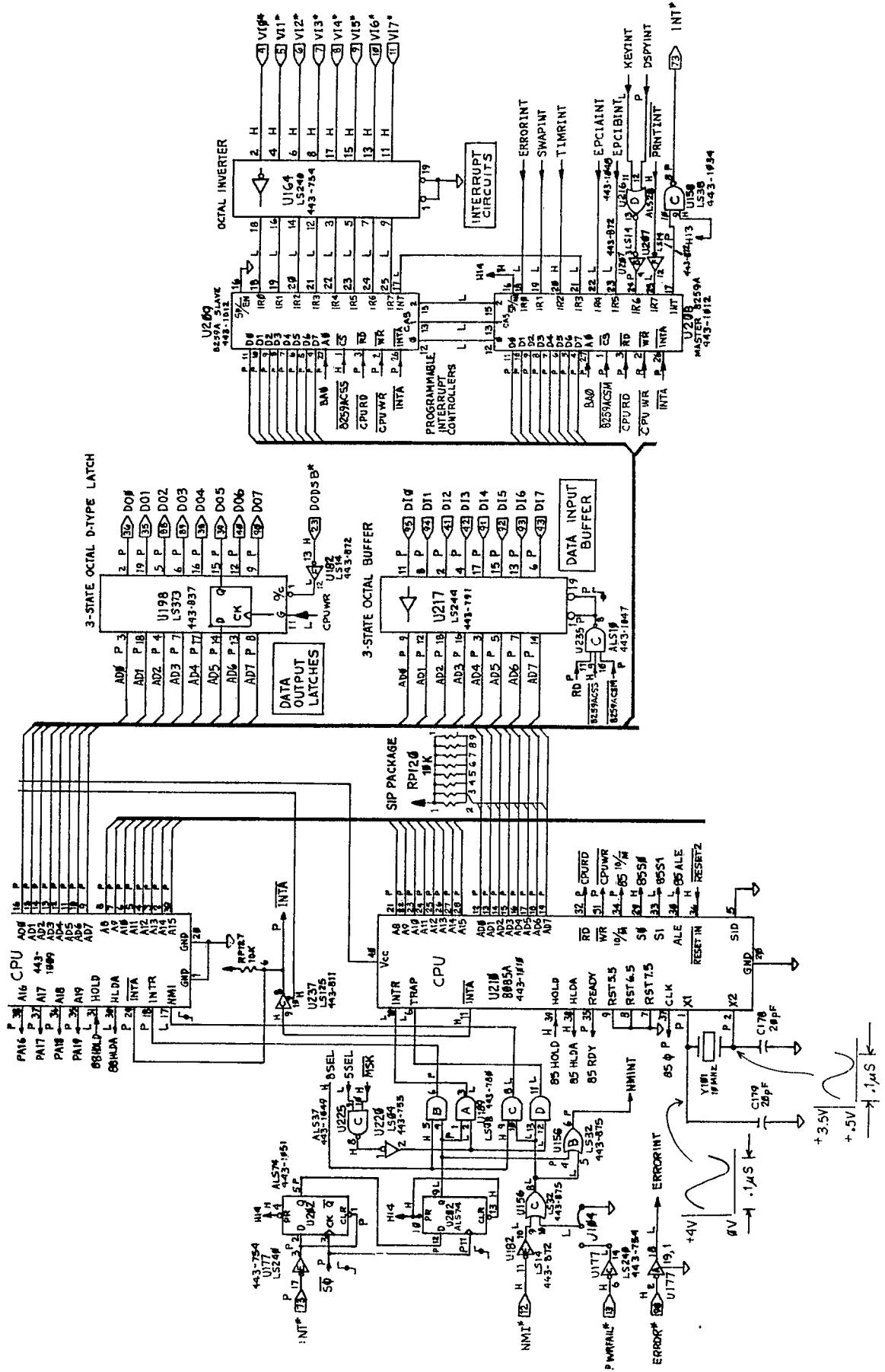
CDSB* AND MWRT

These lines are not control output lines, but are associated with them.

Asserting the CDSB* line tri-states U180 to disconnect the bus control lines. This situation can happen if another CPU board that is plugged into the S-100 bus takes control of the bus. If so, that board must supply the output control signals.

While pDBIN is a generalized write strobe for both memory and output ports, MWRT is a write strobe for memory write cycles only. In the H/Z-100, it is used in the memory refresh circuits and on the video board.

The MWRT signal is derived by NORing pWR* and sOUT (from the status circuits) at U216C. (You'll find this IC near the right side of schematic MB1.)



INTERRUPT CIRCUITS (MB1)

INTERRUPT CIRCUITS

GENERAL INFORMATION

Maskable interrupts are routed through the IC at U208, an 8259A programmable interrupt controller (PIC). This IC features an 8-level priority controller and programmable interrupt modes that, among other things, allow using this IC with either the 8085 or the 8088. Also, individual interrupt lines can be masked without affecting those above or below it. See the 8259A IC data sheets for detailed information.

Before the 8259A can be used, It must be initialized by the CPU. It does this by outputting the programming information to ports 0F2H and 0F3H for the master, and to 0FOH and 0F1H for the slave. When it accesses these ports, the I/O port decoder asserts 8259ACSM for the master PIC (U208), and 8259ACSS for the slave PIC (U209). In addition, it will assert BA0 to select the desired register inside the IC. Once the data to be written has settled on the data pins, D0-D7, the CPU asserts the CPUWR line at pin 2 to perform the write.

To read the status registers of the 8259A, the CPU performs the same steps as described above, except it will assert the CPURD line at pin 3.

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As previously mentioned, U208 is the master PIC and handles all of the motherboard and video board interrupts. In order of priority (highest first), these interrupts are:

Level	Description
0	ERRORINT: Parity error or S-100 pin 98 (ERROR*) asserted.
1	SWAPINT: Processor swap interrupt.
2	TIMRINT: Programmable timer interrupt (Out 0 or Out 2).
3	SLAVE: S-100 vectored interrupt from the 8259A slave IC at U209.
4	EPCIAINT: Serial port A interrupt.
5	EPCIBINT: Serial port B interrupt.
6	KEYINT or DSPYINT: Interrupt from the keyboard or the slave circuits.
7	PRINTINT: Interrupt line from the printer port.

MASKABLE INTERRUPT SEQUENCE

Whenever one or more of the interrupt lines goes high, U208 evaluates its priority and sends an interrupt request to the CPU through U158-8. The 8259A will also assert the INT* line if the CPU is currently processing a lower-priority interrupt.

Assume that a master interrupt has occurred; that is, one of the interrupt lines other than U208-21 has been asserted. How the CPU responds to the interrupt depends on whether the 8085 or the 8088 is active.

If the 8085 is active, the following sequence will occur:

- The CPU asserts the INTA line at U208-26.
- U208 places the 8080/8085 CALL instruction (OCDH) onto the data bus at pins 4 through 11.
- The 8085 decodes this call instruction and determines that it requires two more bytes to complete the instruction. So it sends two more INTA signals to U208.
- When U208 receives the second INTA, it sends the low byte of the vector address to the CPU. When it receives the third INTA, it sends the high byte of the vector address to the CPU. (The vector addresses must be programmed into the 8259A during the initialization process.)
- After saving the current address in stack, the CPU jumps to the address supplied by the 8259A to process the interrupt. When it finishes, the CPU returns to the location saved in stack and continues the program it was processing before interruption.

When the 8088 CPU is active, the 8259A responds somewhat differently to an interrupt acknowledge.

- The CPU asserts the INTA line at U208-26; the 8259A will not respond at this time.
- The CPU again asserts INTA on the next machine cycle.
- The 8259A places a byte on D0-D7 that represents the interrupt type. The interrupt type is an 8-bit number that depends on which interrupt line is causing the interrupt.
- The CPU multiplies the type number by four to find the correct location in the vector table. This is a reserved section in memory that stores the addresses of the interrupt service programs. See the "iAPX 88 Book" by Intel Corp. for more detail.
- The CPU saves the current address in stack and loads the addressed vector table data into the code segment register and instruction pointer. It then processes the service routine pointed to by these registers.
- When done, the CPU returns to the program that it was processing before the interrupt took place.

The slave PIC at U209 processes the S-100 vectored interrupt lines. If one of these lines is asserted, U209-17 goes high to cause a level-3 interrupt at U208-21. This, in turn, sends an interrupt request to the CPU through U158C. When the CPU responds, it asserts pin 26 of U208 and U209.

This time, the master does not place the vector information onto the data bus. Instead, it enables U209 through the cascade lines at pins 12, 13, and 15. U209 then places the vector information onto the bus.

If no interrupt request is present at the time the CPU sends its first INTA signal (i.e., the request duration was too short) the 8259A will issue a level-7 interrupt. Both the vectoring bytes and the cascade lines will look like a level-7 interrupt was requested.

NON-MASKABLE INTERRUPT SEQUENCE

The non-maskable interrupt is an interrupt request that can't be blocked by software. When the rising edge of the NMI pulse is present at the CPU, the processor must finish its current instruction and service the interrupt request.

The NMI circuits consist of U156C, U156B, and surrounding components. There are two signals that couple to these circuits, NMI* and PWRFAIL; both from the S-100 bus.

NMI* is a general S-100 bus non-maskable interrupt line. It can be used by S-100 boards to signal the CPU of a catastrophic event, such as imminent loss of power, memory error, or bus parity error.

PWRFAIL* is a dedicated line that asserts if system power failure is imminent. If asserted, the line must stay low until the POC* (power-on clear) line is activated. This line is tied to logic one through a 4.7-kilohm resistor on the S-100 bus. Both hardware and software must be provided to use PWRFAIL*. PWRFAIL* can be selected or disabled by the jumper at J104.

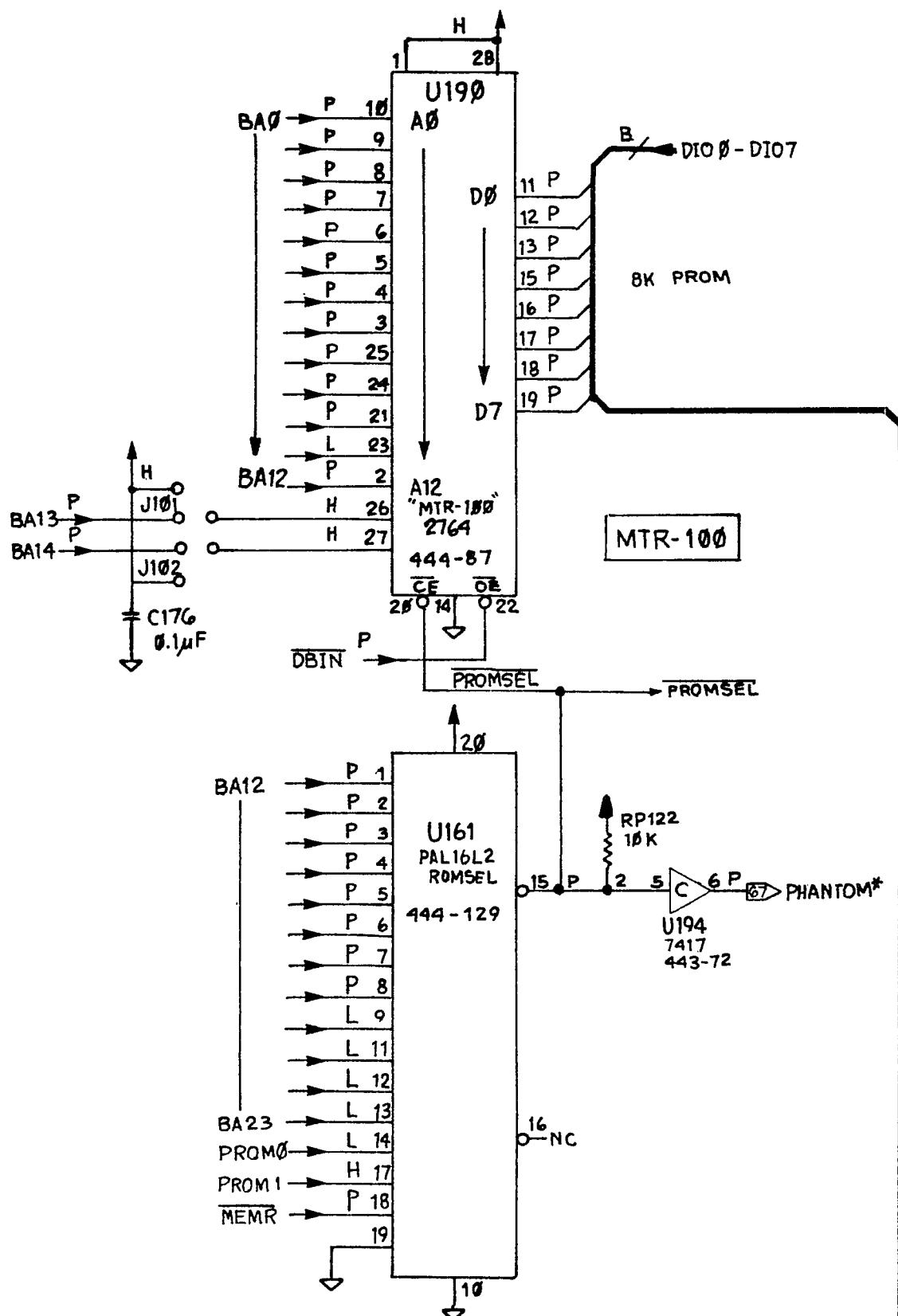
INTERRUPT ROUTING

The dual-D flip-flop at U202 retimes the maskable interrupt and applies it to U189A and U189B. If the 8085 is the active CPU, U189A couples the interrupt request to U210-10. If the 8088 is active, U189B routes the request to U211-18.

If an NMI occurs while the 8085 is active, U189D sends it to the TRAP input at U210-6; while if the 8088 is active, U189C sends the interrupt to U211-17.

If either an interrupt request or an NMI occur, U156B asserts the NMINT line. This works in conjunction with the interrupt mask bit (MSK) in the processor swap port to force the 8088 into the active state. If MSK is low, or NMINT is low, then NMINT has no affect; if MSK is high, and NMINT is high, then NMINT disables the 8085 and enables the 8088.

See the description of the processor swap port for more details.



SYSTEM MONITOR (MB2)

SYSTEM MONITOR

ADDRESSING

The monitor ROM, U190, controls the operation of the H/Z-100 after power-up reset or hard reset. It initializes the necessary I/O ports and determines which CPU will be active in the monitor mode. Though currently 8K, jumpers J101 and J102 allow expanding this ROM to 32 kilobytes.

Whenever the CPU fetches an instruction from the ROM, it asserts DBIN, pin 22, the inverted S-100 pDBIN line. This line comes from U195-16.

Accessing the monitor also asserts PROMSEL at U161-15. This IC changes the memory address that the monitor ROM responds to; effectively repositioning the ROM in memory. When PROMSEL is asserted, it enables U241 on schematic MB⁴. U241 couples the data from U290 to the CPU.

Here's what happens...

After power-up or a hard reset, the memory control latch at U176 is cleared by the reset line at pin 1. This places lines PROM0 and PROM1, U161-14 and U161-17, at logic zero.

When both PROM0 and PROM1 are zero, U161-15 asserts whenever the memory read line asserts at U161-18, no matter what the address. Effectively, the monitor appears to be in all of the address locations.

After a reset, the 8085 CPU is selected by the swap circuits and the 8088 is disabled. The program counter of the 8085 starts fetching op-codes starting at address zero in U190. The monitor causes the CPU to switch itself off and activate the 8088 (to see how this is done, see the "CPU Selection Logic" circuit description).

When the 8088 is in control, its program counter starts fetching monitor instructions from memory address FFFF0H, 16 bytes below the top end of the 1 megabyte address space. However, this is okay since the ROM still appears to be in all of address space.

The 8088 selects the next operating mode by latching PROM1 to logic one and leaving PROM0 at logic zero. U190 is now located in the top 8K of the 8088's natural 1 megabyte address space. This is the location that the ROM is normally in while the H/Z-100 is in the monitor mode.

Two other options are available: (1) If PROM0 = 1 and PROM1 = 0, then the ROM is effectively placed at the top 8K of every 64K page of memory. This is useful for the 8085 which has only a 64K natural address space. (2) If PROM0 = 1 and PROM1 = 1 then the ROM is disabled.

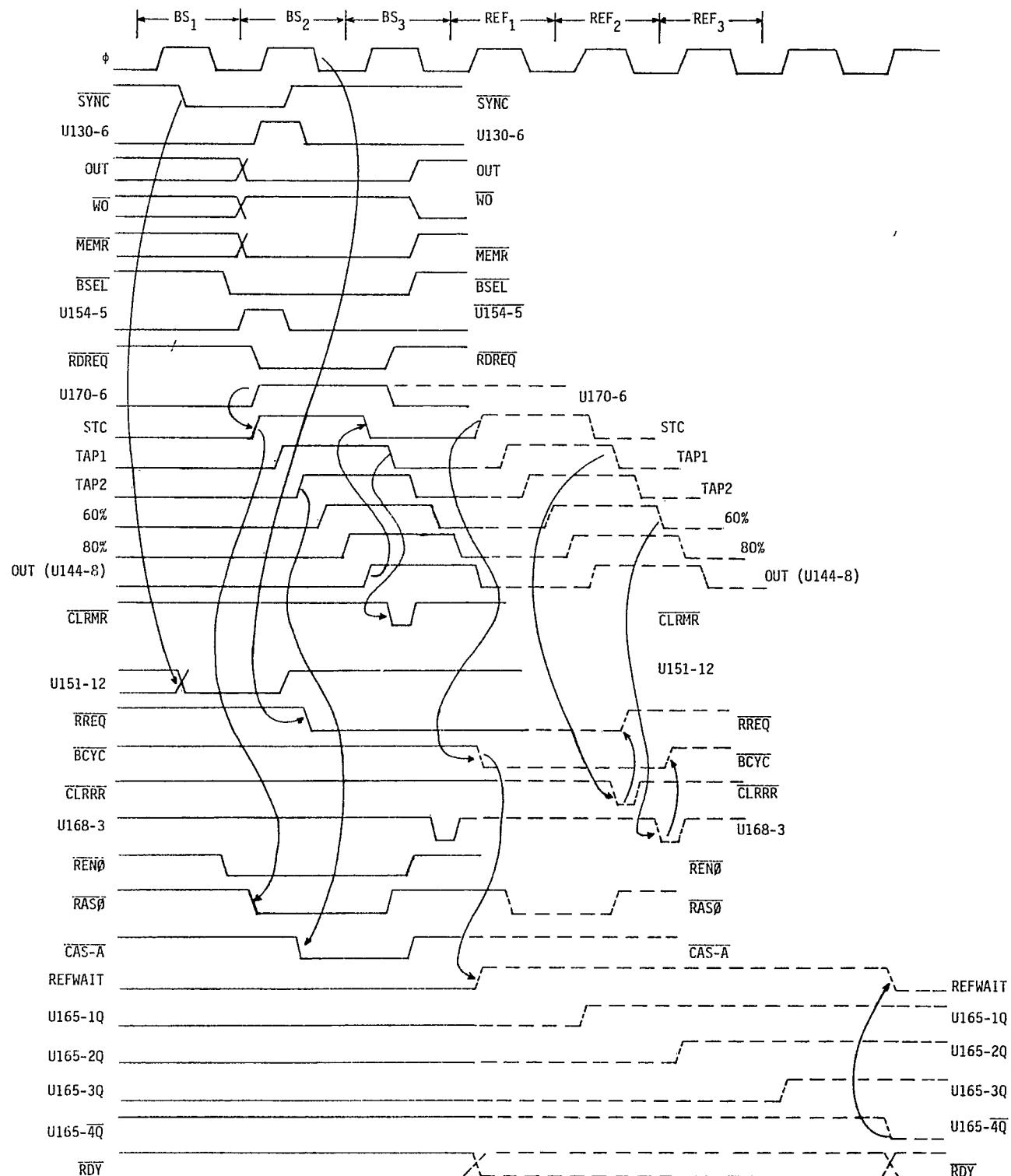
To select one of the above four options, the CPU must output a data byte to port 0FCH, the memory control latch. Data bit D2 directly affects PROM0 and D3 affects PROM1.

PHANTOM*

The PROMSEL line from U161 also connects to U194-5, an open collector buffer that connects to the PHANTOM* line on the S-100 bus. The PHANTOM* line allows overlapping blocks of memory on the S-100 bus. When properly decoded, the PHANTOM* line will disable one block of memory while enabling another.

In this case, whenever the monitor is selected by PROMSEL, the PHANTOM* line goes low and all RAM locations are disabled. Thus, when both PROM0 and PROM1 are zero at power-up, the CPU reads from ROM, but writes to RAM.

Since you can disable the monitor by raising both PROM0 and PROM1 to logic one, it's possible to have continuous read/write memory from address zero to the top end of 16 megabytes (technology permitting). However, you would have to supply your own monitor routine.



MEMORY CIRCUITS WAVEFORMS:
READ MEMORY AND REFRESH CYCLES (MB3)

DYNAMIC MEMORY

OVERVIEW

Refer to schematic MB3 as you read the following.

The dynamic memory consists of five major circuits: (1) the memory itself, which can be 64K, 128K, or 192K; (2) the address multiplexer, used to convert the 16-bit address bus to the 8-bit address bus required by the dynamic RAMs; (3) the memory map decoder, used to select the correct 64K bank of memory within 192K; (4) the refresh circuits, used to keep RAM from "forgetting" the data stored in memory; and (5) the parity circuits, which can send an error signal to the CPU if the incorrect byte is at the addressed memory location.

DYNAMIC RAM

The H/Z-100 uses 6665/TMS4164 64K x 1 bit dynamic RAMs for main memory. These ICs are upward-compatible with the 4116 16K chips and the 6633 32K memories. There is one IC per bank per bit position, so that 8 ICs make up 64 kilobytes. For the first 64K bank, U109 = MDO and U102 = MD7.

Three sets of these RAMs make up the 192K address space:

U109-U102 = 1st 64K
U125-U118 = 2nd 64K
U145-U138 = 3rd 64K

To read or write memory, the address circuits select the correct RAM location by placing the lower 8 bits of the address onto lines MA0-MA7. One of the three RAS lines, 0-2, asserts to latch this address into RAM. The upper 8 bits of the address is placed onto MA0-MA7. After waiting a short time for the lines to settle, the CAS lines assert to latch the byte at MDO-MD7 into RAM.

If reading memory, pin 3 of all the RAM chips are logic one. This places the addressed data onto pin 14 of each RAM chip. U110-12 then enables U133 to couple this data to the S-100 bus and to the CPU.

If writing memory, the CPU enables U132 at pins 1 and 11. U132 couples the data from the S-100 bus to pin 2 of each RAM chip. U110-13 asserts WE at pin 3 of each RAM chip to latch the data into the addressed memory location.

ADDRESS MULTIPLEXER

The address multiplexers consists of U146 and U128. These ICs couple the lower 8 bits of the 16-bit address bus to MA0-MA7 during RAS time. They next pass the upper 8 bits during CAS time. Multiplexing permits keeping the pin count down on the RAM ICs.

When the CPU starts to access memory, line TAP1 is logic zero. This couples the A inputs of the multiplexer to the Y outputs at MA0-MA7. These lines now hold the lower 8 bits of the 16-bit address bus. U110, in the memory map circuits, generates a $\overline{\text{RAS}}$ signal to latch this address into RAM.

Forty nanoseconds later, TAP1 goes high. This couples the B inputs of the multiplexer to MA0-MA7; these are the upper 8 bits of the address.

Forty nanoseconds after TAP1 is asserted, TAP2 at U110-5 goes high. This clocks MA0-MA7 into the CAS latches. See the description of the refresh circuits for more detail on TAP1 and TAP2.

Another line going to the multiplexers is $\overline{\text{BCYC}}$. This line is low to indicate that a bus cycle is taking place. The memory is going through a bus cycle whenever the CPU is accessing the memory. BCYC asserts pin 15 of each multiplexer IC to activate their outputs.

If a memory refresh is taking place, $\overline{\text{BCYC}}$ is high and tri-states the multiplexers. At the same time, it activates the outputs of U126, part of the refresh address generator. U126 places a refresh address on MA0-MA7. All three RAS lines assert to refresh the same location in each 64K bank.

If the CPU attempts to read or write memory during refresh, the refresh circuits place the CPU into a wait state until refresh is complete. See the refresh circuit description.

MEMORY MAP DECODER

The memory map decoder is made up of U111, U110, and U173. It performs three major functions: (1) decodes the address bus to select the correct 64K bank. (2) provides read/write control lines for the RAM and the data bus. (3) performs correct addressing and control during refresh (this will be covered in the refresh circuit description).

Here's how it does it...

U111 selects the correct 64K bank for any memory address below 192K. The address is determined by the map select lines and BA16 and BA17. We'll cover the map select lines later. For now, assume the standard configuration (MAPSEL0 = 0, MAPSEL1 = 0; contiguous RAM from 0 to 192K).

Under normal operation, BA16 and BA17 will select the banks as follows:

BA17 BA16 Condition		
0	0	0 to 64K, <u>REN0</u> asserted.
0	1	(64K+1) to 128K, <u>REN1</u> asserted.
1	0	(128K+1) to 192K, <u>REN2</u> asserted.
1	1	U111 disabled.

The last condition is necessary because BA17 will allow addressing up to 256K. Since there isn't any on-board RAM between 192K+1 and 256K, U111 must be disabled. However, this doesn't prevent filling this memory range with a 64K board on the S-100 bus.

Also, U111 is disabled if the CPU addresses a location above 256K. In this case, the DECODEN line at pin 14 goes high to place all of U111's outputs to logic one. DECODEN is controlled by U173 and will be discussed later.

BSEL, at U111-9, asserts whenever REN0, REN1, or REN2 asserts. This line is used in the refresh circuits and will be discussed later.

The three row-enable lines connect to pins 1, 2, and 3 of the PAL at U110. This IC decodes these, and other inputs, to assert RAS, CAS, WE, and MDGATE at the appropriate times.

Basically, $\overline{\text{RAS}}$ asserts under the following Boolean conditions (* = AND, + = OR):

$$\overline{\text{RASn}} = (\overline{\text{RENn}} * \overline{\text{TAP1}}) + (\overline{\text{RENn}} * \overline{\text{STC}} * \overline{\text{RREQ}}) + (\overline{\text{BCYC}} * \overline{\text{TAP1}})$$

While CAS asserts when:

$$\overline{\text{CAS-A}} = \overline{\text{CAS-B}} = \overline{\text{CAS-C}} = (\overline{\text{BCYC}} * \overline{\text{TAP2}} * \overline{\text{WO}}) + (\overline{\text{BCYC}} * \overline{\text{TAP2}} * \overline{\text{PHANTOM}})$$

The PHANTOM line permits placing other memory devices into the same address space as the dynamic RAM. When PHANTOM is asserted, the CPU can access the alternate memory device without disturbing the on-board memory. For CAS, in the read mode, the addressed memory location will be placed on the memory outputs, but will not reach the S-100 bus. This is because DIEN will be logic one on U133-1, tri-stating this buffer. During memory write, PHANTOM prevents $\overline{\text{WE}}$ from asserting, causing a dummy read cycle.

Refer to the memory circuits timing diagram as we discuss the basic timing cycle.

Assume that the CPU is addressing a location in the first 64K of memory. STC goes high during bus cycle 2; TAP1 = 0 so the logic 0 on $\overline{\text{REN0}}$ couples to U110-19, $\overline{\text{RAS0}}$. The lower 8 bits of the address is latched into RAM ICs U102-U109.

Forty nanoseconds later, TAP1 goes high. This line causes the address multiplexers to place the upper 8 bits of the address onto lines MA0-MA7.

In another 40 nS, TAP2 goes high, causing the CAS lines to assert. The 40-nS delay ensures that the address on MA0-MA7 has had time to settle. Since the 0-64K bank is the only one previously loaded by $\overline{\text{RAS0}}$, $\overline{\text{CAS-A}}$ latches the upper 8 bits of the address into U102-U109. The other two banks aren't affected by $\overline{\text{CAS-B}}$ and $\overline{\text{CAS-C}}$.

The memory location pointed to by the address is now written to or read from by the CPU.

The two remaining outputs of U110 are the write-enable line at pin 13 and the memory data gate at pin 12. Write-enable asserts whenever there's a memory write during a bus cycle at TAP1 or TAP2 time. MDGATE asserts when TAP1 or BCYC is asserted. It blocks data from the S-100 bus during a memory write or a refresh operation.

The PAL at U173 is the final IC in the memory map decoder circuits. This IC provides an enable line to U111 (DECODEN), an enable line to U133 (DIEN), and two reset lines to the refresh circuits (CLRRR and CLRMR).

DECODEN, at U173-17, is normally low for CPU accesses to any memory locations below 256K. If above 256K, one of the extended address lines (BA18-BA23) will be low and cause DECODEN to be high. This, in turn, forces all of the outputs of U111 to go high.

DIEN, at U173-14, enables the outputs of U133 during a memory read to send the addressed data to the CPU. This line goes low when DBIN = 0, MDENB = 1, and PHANTOM = 0. MDENB asserts whenever the CPU is accessing the dynamic RAM; this will be discussed later. PHANTOM and DBIN are the inverted versions of the S-100 signals, PHANTOM* and pDBIN.

CLRRR, from pin 16, is the clear refresh request. This line resets the refresh request circuits at the end of a memory refresh cycle. This line asserts when TAP1 = 0, TAP2 = 1, and BCYC = 0. See the description of the refresh circuits for more detail.

CLRMR, from pin 15, is the clear memory request line. This signal clears the memory request circuits at the end of a CPU memory read or write cycle. It asserts when TAP1 = 0, TAP2 = 1, and BCYC = 1. See the description of the refresh circuits for more detail.

REFRESH CIRCUITS

The refresh circuits consists of a refresh clock, U147 and U148; the refresh request circuit, U152; memory request, U167; timing and control, U149 and U150; control circuits to the CPU, U168 through U158, U150, and U165; and the refresh address generator, U127 and U126.

These circuits refresh the memory when the CPU isn't accessing RAM. This is necessary because it is a characteristic of dynamic RAM to lose the contents of its memory if not accessed one every 2 mS (approximately).

The refresh circuits contain arbitration logic. If the refresh circuit's generate a refresh while the CPU is accessing memory, it waits until the CPU is done before gaining control of the RAM. If the CPU attempts to access memory during a refresh operation, the refresh circuits put the CPU into a wait state until refresh is complete.

Also, the refresh circuits provide timing for RAS, CAS, BCYC, and other memory functions for both refresh and CPU operation.

Here's how it does it...

U147, a 16-uS oscillator, generates the refresh clock. The first negative-going pulse latches U148-5 to logic one; starting the refresh request. The signal at U168-11 retimes the refresh request to the system clock.

The logic one from U148-9 connects to U151-2. Two other lines to this gate must go to logic one before the refresh request can take place. The start-write (STWRT) line in the memory request circuits, and the SYNC line from the S-100 bus. If either line is low, then the CPU is about to perform a memory write, or the start of a bus cycle is taking place. As a result, U151-12 stays at logic zero and a refresh request doesn't take place.

If STWRT and SYNC are high, then S ϕ latches U152-5 to logic one, causing a refresh request.

However, the memory circuits will not acknowledge this request if the CPU is executing a memory read cycle. This is because U149 and U150 time the signal so that BCYC (bus cycle active) at U150-9 can't change to its BCYC state until memory read is completed. You'll see how shortly.

If, however, no memory read or write is taking place during the refresh request, the logic zero at U150-12 will be latched into U150-9 on the next positive-going signal from U169-3. The signal from U169-3 is generated by the delay line at U149 and will be explained in more detail later.

BCYC, now logic zero, tri-states the address multiplexers, U146 and U148, and places the refresh address generator, U127 and U126, onto MA0-MA7. To allow the refresh address generator time to stabilize, U149 delays asserting TAP1 by 40 nS.

Since BCYC is low, U110 in the memory mapping circuits recognizes that this is a refresh cycle. When TAP1 goes high, all three RAS lines assert. This refreshes the entire row, pointed to by U126, in each bank.

If the CPU attempts to access memory at this time, the logic circuits at U150 through U158 will put the CPU into a wait state. When refresh occurred, BCYC went high to latch U150-5 to logic one. REFWAIT stays asserted for 4 clock cycles and is then cleared by a low at U150-1.

If the CPU attempts to write or read memory, then MEMWR or MEMR will assert at pins 10 and 9 of U170. BSEL, at U130-12, is also asserted because the CPU has asserted \overline{REN}_0 , \overline{REN}_1 , or \overline{REN}_2 at U111. Since pins 4 and 5 of U169 are both logic one, then MDENB asserts.

With both MDENB and REFWAIT high, RDY goes low and the CPU goes into a wait state until the refresh cycle is finished; i.e., when REFWAIT goes low.

Incidentally, MDENB asserts only when the CPU is attempting to access the on-board dynamic RAM. If the CPU is accessing a memory board on the S-100 bus, it won't affect the logic shown on schematic MB4, so there's no need to put the CPU in a wait state during refresh.

To get an idea of timing relationships, refer to the memory circuits waveforms and schematic MB4 as you read the following.

Assume that a memory read to an address in the 0-64K range takes place. U154-5 goes high during BS2 because MEMR, BSEL, and SYNC are asserted. pSTVAL* asserts shortly afterward to clock U167-6, RDREQ, to logic zero. U169-2 is logic one, and because U149-8 is zero, U169-1 is 1.

This asserts STC and causes U110-19, RAS0, to assert. The lower 8 bits on MA0-MA7 are loaded into the RAM's row address latches.

STC also drives U149, a 200-nS delay line with 40-nS taps. TAP1 asserts 40 nS after STC and causes U146 and U128 to place the upper 8 bits of the 16-bit address onto MA0-MA7. Forty nanoseconds after that, TAP2 asserts and causes CAS-A to assert at U110-16. Since this is a read cycle, U110-13 is logic one, so ICs U102-U109 places the addressed data onto pin 14 of each IC--this data is sent to the CPU through U133.

After TAP2 asserts, the delay line asserts outputs 60%, 80%, and OUT at 40 nS intervals. When OUT goes high, it drives STC low through U166E and U169-1. Forty nanoseconds later, TAP1 goes low to generate a clear memory request pulse (CLRMR = TAP1*TAP2*BCYC).

CLRMR clears U167 to drive U170-6 low, as shown on the solid line on the memory circuits waveforms.

The read cycle is finished; a write cycle would operate in the same manner.

Now, assume that a refresh request occurs during the read cycle previously discussed. U148-9 in the request circuits latches high. Also, U151-13 is high since this isn't a write operation. However, SYNC at U151 is low during the first part of the bus cycle, so U151-12 is low.

When SYNC goes high, U151-12 goes high and U152-5 (RREQ) goes high on the next system clock pulse (end of BS2 on the waveforms). RREQ goes low and holds U170-6 high at the end of the read cycle. This is shown as the dashed line in the memory circuits waveforms.

The low forced on STC by OUT ripples through the delay line and forces STC high during time REF1. This clocks RREQ into U150-9, driving BCYC to logic zero. In turn, BCYC tri-states the address multiplexer and places the contents of the refresh address generator onto MA0-MA7.

When TAP1 goes high, all three RAS lines assert to refresh memory as described previously.

The RAS lines return high at the end of TAP1 time and U173 asserts the clear refresh request line (CLRRR = TAP1*TAP2*BCYC). This resets U148 and U152 in the refresh request circuits.

CLRRR also increments the refresh address generator at U127-1.

Meanwhile, as the logic one ripples through the delay line (shown in dotted lines on the waveforms), the 80% tap is ORed with the inverted 60% tap to pulse U168-3 at time REF3. This places a logic one on U150-9 to restore normal bus cycle operation.

The bottom waveforms show what takes place in the ready circuits during a refresh operation.

At the start of a refresh cycle, BCYC goes high to clock REFWAIT high. The system clock at U165-9 clocks REFWAIT through U165-1Q, -2Q, -3Q, to -4Q; clearing REFWAIT at U150-1.

The four clock periods that REFWAIT is high mark the time required for the refresh circuits to activate, refresh the memory, and return to their quiescent states.
>

As described before, if the CPU attempts to read or write the onboard memory during this time, MDENB will go high and force RDY low--generating a wait state. After REFWAIT goes low, RDY goes high; allowing a normal bus cycle to occur.

Note that the refresh circuits don't generate a refresh request every time the CPU isn't accessing memory--only once every 16 uS. The CPU is running about 80 times faster than this and can perform many instruction cycles between refreshes. Since the RAMs can go for about 2 mS before requiring refresh, there's no danger of losing memory.

PARITY CIRCUITS

The parity circuits consist of U153, U101, U117, U137, and U152.

These circuits maintain the parity status for each byte in the 192K of RAM. If a memory location should not match its parity bit, then the parity circuits will send an error signal to the CPU.

U101, U117, and U137, are 64K by 1-bit RAMs and store one bit of parity information for each address location of RAM. These RAMs are addressed by \overline{RAS} and \overline{CAS} in the same way as the other RAMs. However, data transfers take place through U153 instead of the data bus. U153 is a 9-bit odd/even parity generator/checker that processes and maintains the parity status.

During a memory write, the data written into RAM is present at pins 8-13 and 1-2 of U153. Pin 14 of each parity RAM is a high-impedance state so U153-4 is logic 1 through pullup resistor R107.

The following truth table show the levels of the odd and even outputs for the number of high inputs:

Number of Input Pins That Are High. (1, 2, 4, 8-13)	Outputs	
	Even	Odd
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

So if there is an odd number of high bits in the data byte, the logic 1 on U153-4 makes it even. U153-5 responds by going high.

If there is an even number of data bits in the data byte, U153-5 stays low, so the total bit count remains even.

U153-5 couples the one or zero through the normally-enabled gate at U151-4 to the data input pins of the parity RAMs.

The ZEROPAR line at U151-5 is normally high. This can be brought low to force all addressed parity RAM locations to zero--regardless of the byte status. It is brought low by clearing data bit D4 to zero and outputting it to port OFCH, the memory control latch. ZEROPAR is used as a quick test to see if the error-detection circuits work.

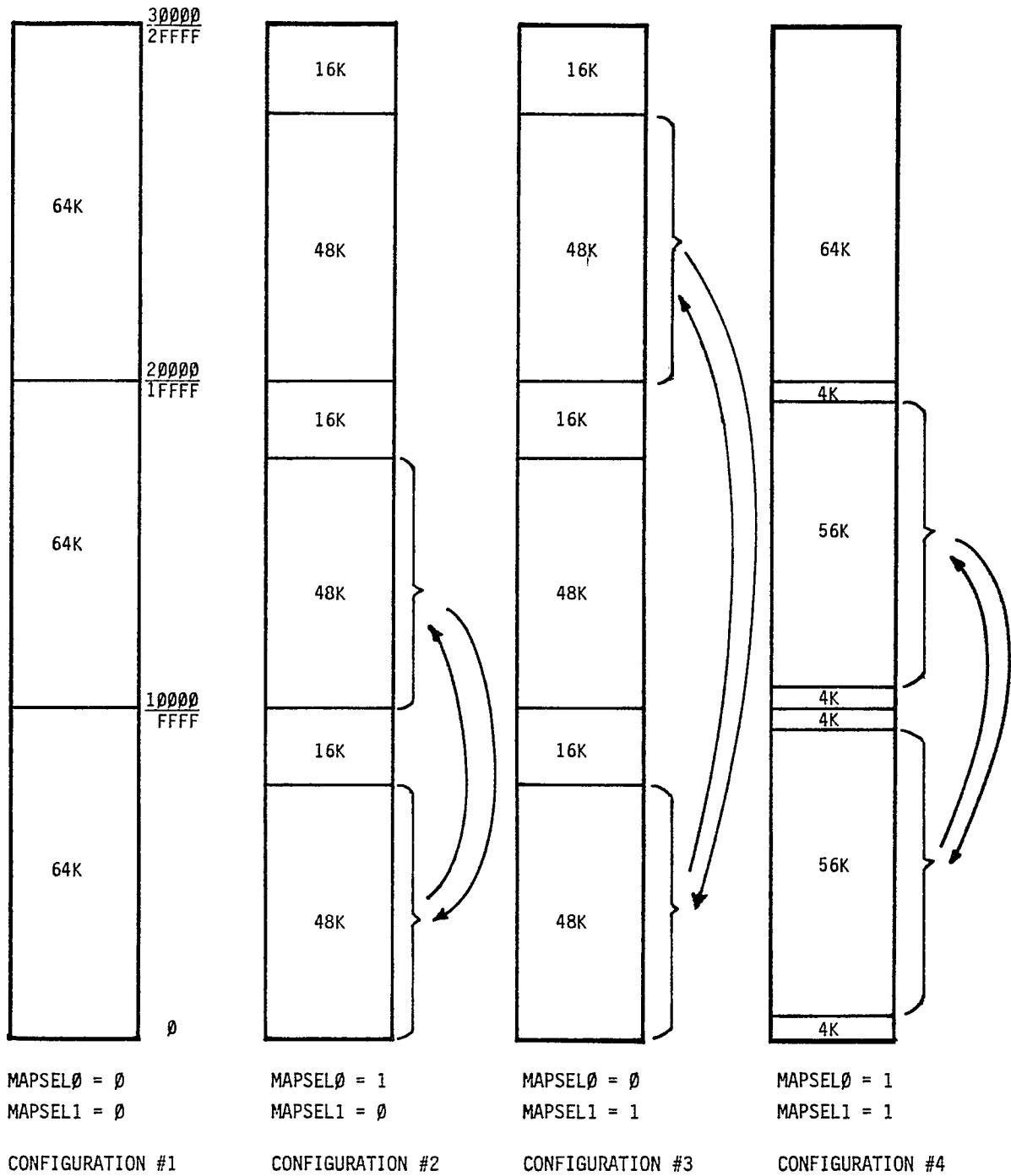
The odd-parity output goes to U152-11. During a memory write, U151-11 is low; preventing a false error signal from being generated. For the same reason, U151-9 remains low for a memory refresh.

During a memory read, data output from the addressed RAMs are present at the inputs of U153. The corresponding parity bit, from U101, U117, or U137, is placed on U153-4. If the bit pattern that was previously written into data RAM and parity RAM hasn't changed, the total number of high bits is always even.

So U153-6 remains low, the non-error condition.

If, however, the bit count totals to an odd number--due to a chip failure or soft error for example--then U153-6 goes high. When TAP2 goes low, U152-9 is latched to logic one and asserts the S-100 ERROR* line at U158-6. This will generate an error interrupt at U208-18 (schematic MB1). From here, it is up to the user's software to process the interrupt.

When KILPAR is asserted, U152 is held clear to prevent a parity error interrupt. To assert KILPAR, clear data bit D5 to zero and output it to port OFCH, the memory control latch.



MOTHERBOARD MEMORY MAP OPTIONS

MAP SELECTING

Map selecting takes place at pins 1 and 15 of U111. These two lines, MAPSEL0 and MAPSEL1, also go to U173-7 and -8; but currently are not used by this IC. Depending on the logic state of U111-1 and U111-15, plus the address on lines BA12-BA15, the memory map will appear to be in one of the four configurations shown in the illustration:

Configuration #1: MAPSEL1 = 0 MAPSEL0 = 0

This is the default configuration, memory is contiguous from 0 to 192K.

Configuration #2: MAPSEL1 = 0 MAPSEL0 = 1

In this configuration, the first 48K of bank zero appears to be swapped with the first 48K of bank 1. The two 16K areas and the rest of RAM are unchanged. This configuration may be used for MP/M while running the 8085 CPU.

Configuration #3: MAPSEL1 = 1 MAPSEL0 = 0

In this configuration, the first 48K of bank zero appears to be swapped with the first 48K of bank 2. The two 16K areas and the middle 64K of RAM are unchanged. This configuration may also be used for MP/M while running the 8085 CPU.

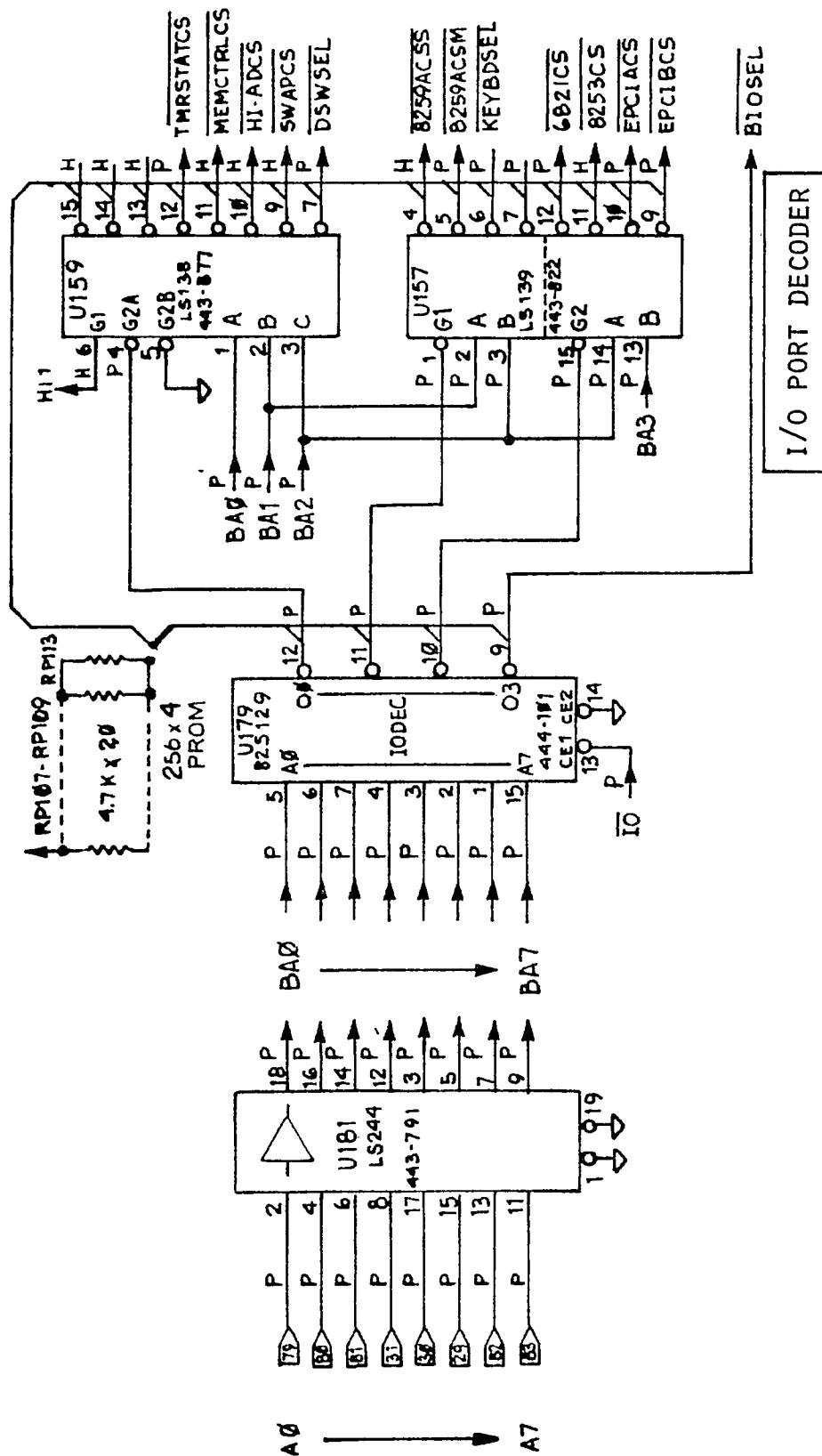
Configuration #4: MAPSEL1 = 1 MAPSEL0 = 1

In this configuration, 56K in bank 0 appears to be swapped with 56K in bank 1. Four kilobyte buffers above and below each 56K area remain unchanged, as does the top 64K bank. This configuration would permit using an extended BIOS when running CP/M-85.

Note that, in all cases, the memory only appears to be swapped from the memory's point of view. When the CPU addresses the swapped memory, the memory map decoder merely asserts a different RAS line than it normally would.

For example, assume that the H/Z-100 is operating in Configuration #4. If the CPU should write to the byte at the 6K location, U111 would assert REN1 instead of REN0. The memory at the 70K location will be written to. Bear in mind, however, that as far as the CPU (and the programmer) is concerned, the byte at 6K was written to.

Address lines BA12-BA15 allow the memory map decoder to keep some sections of memory in place--down to 4K increments.



I/O PORT DECODER (MB2)

I/O PORT DECODER

Refer to schematic MB2 as you read the following.

The heart of the I/O port decoder is U179, a 256 x 4 PROM. Depending on which motherboard/video port the CPU addresses, U179 will enable U159 or U157; respectively a 3-to-8 line decoder and a dual 2-to-4 line decoder.

To address one of these ports (0D8H through OFFH), the CPU first places the appropriate port address on the inputs of U179, A0 through A7. This address comes from the S-100 address lines, A0-A7, through octal buffer U181.

When the address lines have stabilized, the CPU enables U179 by asserting pin 13, the IO line. This signal comes from U224C-10, and goes low whenever the CPU asserts the S-100 SINP or SOUT lines. Once IO is asserted, U179 decodes the address at its inputs and selects either U159 or U157. For example, it selects U159 for a memory control latch operation by bringing U179-12 to logic zero. Pins 1, 2, and 3 of U159 then decode the lower three bits of the address bus to assert pin 11, MEMCTRLCS.

U159 also selects the following ports:

TMRSTATCS This is the timer status port; U160 on schematic MB4.

HI-ADCS This line controls the extended addressing latches shown on schematic MB1.

SWAPCS This line connects to the processor swap port shown on schematic MB1.

DWSEL This line controls the power-up reset configuration port, U239 on schematic MB2.

If U179-11 is asserted, section A of decoder U157 will be selected. It will decode address lines BA1 and BA2 to enable the interrupt ports, 8259ACSS and 8259ACSM, on schematic MB1; or the keyboard port, KEYBDSEL, on schematic MB4.

If U179-10 is asserted, section B of decoder U157 is selected. It will decode address lines BA2 and BA3 to enable one of the following ports:

6821CS The parallel port, U114, on schematic MB4.

8253CS The timer port, U160, shown on schematic MB4.

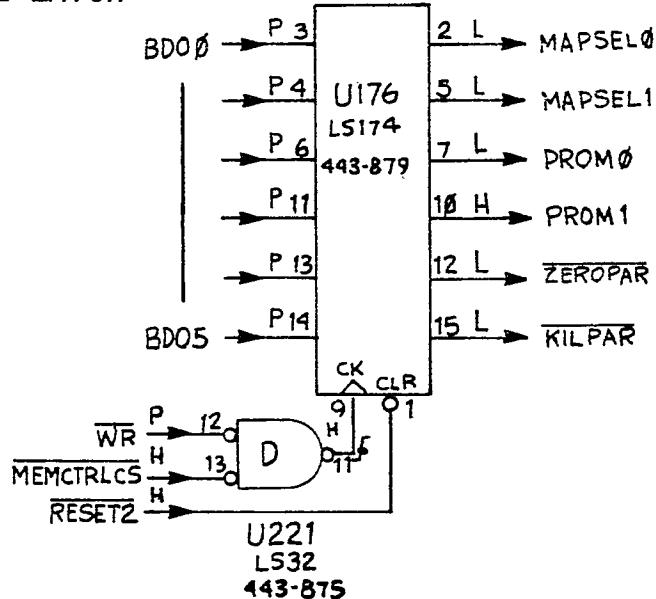
EPCIACS Serial port A on schematic MB4.

EPCIBCS Serial port B on schematic MB4.

If the keyboard, serial port A, or serial port B is selected, U179-9 will also go low. This line is further decoded by U222 (schematic MB4) to enable U241 whenever the CPU reads data from one of these ports.

See the appropriate circuit description and the block diagram description to see how each of these circuits are affected by the I/O port decoder.

MEMORY CONTROL LATCH



The memory control latch, U176, determines the addressing of RAM and ROM; it also sets the status of the parity circuits.

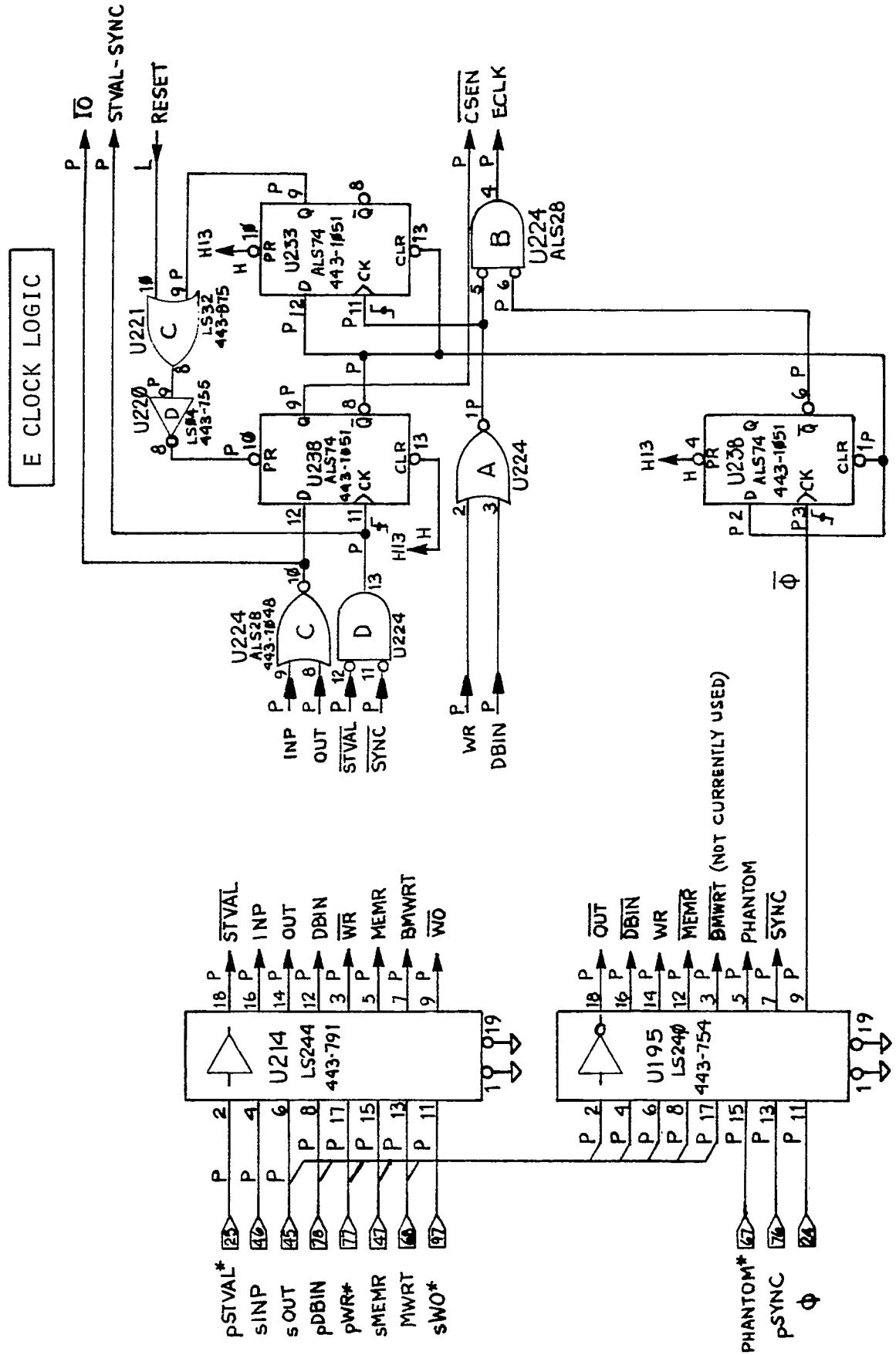
The CPU accesses this latch by writing the correct byte to port OFCH. This is done by asserting the MEMCTRLCS line at U159-11 in the I/O port decoder. This signal is then applied to U221D-13, an OR gate.

The CPU next places the data byte to the D inputs of U176, a hex D-type flip-flop, and then asserts pWR* on the S-100 bus. U214-17 couples this control signal through U214-3 to U221-12 and drives U221-11 low.

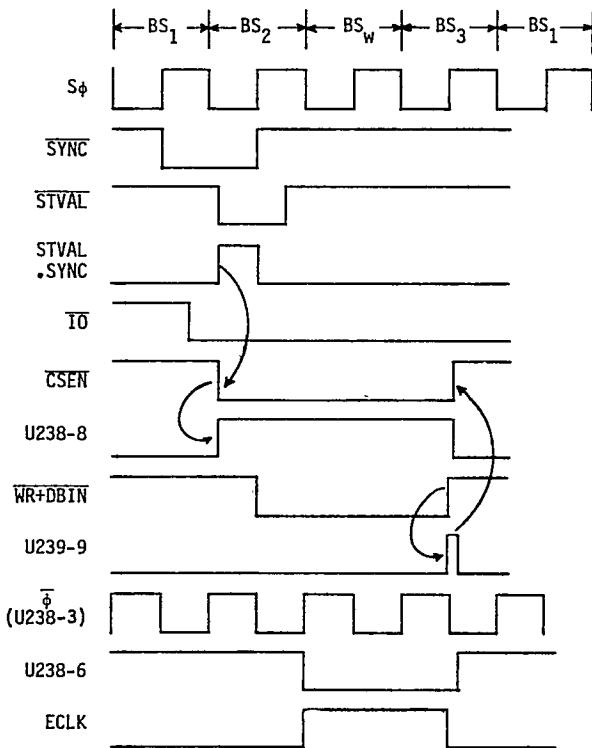
When the data byte on the D inputs of U176 has had time to stabilize, U221-11 goes high; clocking the data bus signals into U176 on the positive-going edge.

The bit pattern that was on the data bus is now latched onto the Q outputs of U176, setting the type of memory map addressing (MAPSEL0 and MAPSEL1), monitor ROM addressing (PROM0 and PROM1), and parity operation (ZEROPAR and KILPAR).

See the appropriate circuit description and the block diagram description to see how these circuits are affected.



E CLOCK LOGIC



The E clock logic, located on schematic MB2, retimes the S-100 clock and control signals to values required by some of the ICs on the video board and I/O circuits. Refer to the accompanying timing diagram as you read the following.

U224-13 forms the STVALxSYNC signal during bus cycle 2. This provides a status valid signal to the video board.

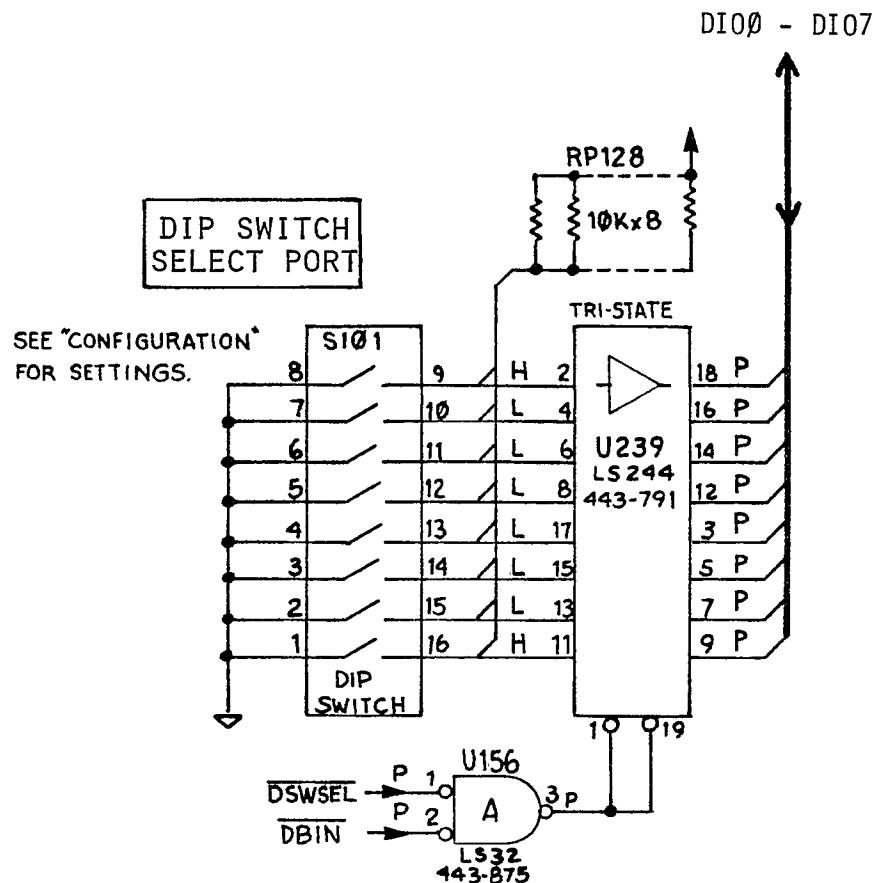
U224-10 generates \overline{IO} , a chip-select line to the I/O port decoder and to the video board.

The combination of \overline{IO} and STVALxSYNC form \overline{CSEN} at U238-9. This line provides a chip-enable signal to serial ports A and B.

At the end of the read or write pulse from U224-1, the logic one at U238-8 is latched into U233-9. This presets U238-9 and brings \overline{CSEN} back to logic one during BS3. At the same time, U238-8 goes low to clear U233-9.

During this time, the inverted system clock, ϕ , works with U238-8 and WR+DBIN to form the ELCK signal. This signal provides timing to the parallel port.

See the circuit description on each of the above mentioned circuits to see how they use the E clock signals.



DIP-SWITCH SELECT (MB2) CIRCUITS

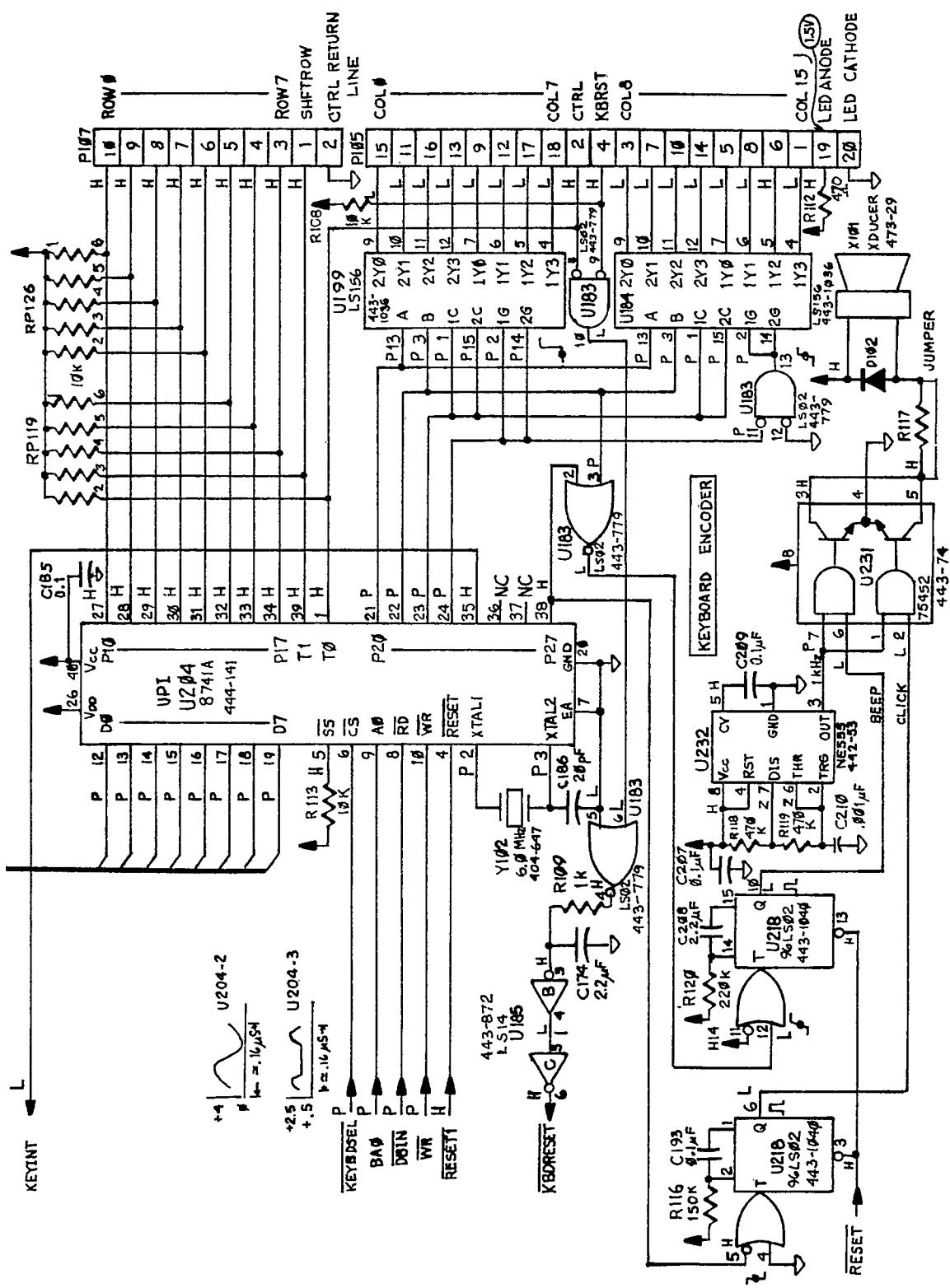
DIP-SWITCH SELECT CIRCUITS

Refer to schematic MB2.

U239, S101, and U156A make up the dip-switch select circuits. The position of these switches determine the operating mode of the H/Z-100. See the configuration section for the various options.

The H/Z-100 reads the status of S101 during power-up by addressing input port OFFH. To read the dip-switch port, the CPU asserts the DSWSEL port select line coming from the I/O port decoder at U159-7. The CPU also asserts the S-100 pDBIN line to indicate that an I/O read operation is to take place. U195 inverts the pDBIN line to produce DBIN at U156-2.

Since U156-1 and U156-2 are both low, pin 3 of this OR gate also goes low to enable U239. The outputs of U239 go from a high-impedance state to the logic level of each switch section; this in turn is coupled through U241 (schematic MB4) to the CPU for further processing.



KEYBOARD CIRCUITS (MB4)

KEYBOARD CIRCUITS

Refer to schematic MB4 as you read the following:

The keyboard circuits are designed around the 8041A/8741A universal peripheral interface (UPI) at U204. This IC is a dedicated 8-bit microprocessor with internal RAM and ROM. The RAM is 64 by 8 bits, while the ROM is 1024 by 8 bits.

Since U204 is a dedicated processor, we will only cover the pin-outs of this IC; see the the IC Data section if you're interested in what happens inside the chip.

D0-D7 Three-state, bidirectional data bus lines used to interface the UPI to the H/Z-100 data bus. The CPU uses this bus to read the code of the pressed key, read UPI status information, and to write command words to the UPI.

CS Chip-select line. When the CPU addresses the keyboard circuits at ports 0F4H & 0F5H, the I/O port decoder asserts line KEYBDSEL. This activates U204.

A0 Address input used by the H/Z-100 to indicate whether the byte transfer to D0-D7 is data (A0 = 0) or a command (A0 = 1). This signal is derived from the buffered address line zero (BA0) from U181-18 on schematic MB2.

RD Read data line. When asserted, the UPI transfers its internal data to the D0-D7 lines. The CPU can then load this data into its accumulator.

WR Write data line. The CPU places data on pins D0-D7 of the UPI. The H/Z-100 then asserts WR to load this data into U204.

RESET Input used to clear the UPI's status flip-flops and program counter to zero.

XTAL1 & XTAL2 Provides 6-MHz crystal-controlled clock to the circuits inside the UPI.

P10-P17 Bidirectional I/O lines programmed as input lines. These lines connect to ROW0-ROW7 of the H/Z-100's matrix keyboard. When a key is pressed, a pulse from one of the column lines (P20-P23) is coupled into one of the row lines. U204 notes which row is being strobed and, by checking an internal counter, when it's being strobed.

By finding when the strobe pulse occurred, the UPI can tell which column was connected to which row when the key was pressed. From this, the UPI can look up the appropriate key code in ROM and send the code to the computer.

T1 An input pin that can be directly tested by software conditional branch instructions. When a key is pressed, the UPI checks this line to see if the SHIFT key is also pressed. If so, the UPI jumps to a routine that translates the key press at ROW0-ROW7 to its appropriate shifted code--if it has one.

T0 Input pin which can be directly tested using conditional branch instructions. When a key is pressed, the UPI checks this line to see if the CONTROL key is also pressed. If so, the UPI jumps to a routine that translates the key press at ROW0-ROW7 to its appropriate control code--if it has one.

P20-P23 Bidirectional I/O lines programmed as outputs. P20 and P21 form a 4-bit counter that connects to the A and B inputs of U199 and U184, two dual 2-line-to-4-line decoders.

P22 connects to the 1C and 2C inputs of the two decoders. When P22 is low, the data at the A and B inputs will be routed to the 2Y outputs; when P22 is high, that A and B data will be routed to the 1Y outputs.

P23 connects to the 1G and 2G inputs of U199; it's also coupled to the 1G and 2G inputs of U184 after being inverted. When P23 goes low, it selects U199 and disables U184; when high, it does the opposite.

The combination of these four lines effectively turns U199 and U184 into a 4-line-to-16-line decoder. The UPI pulses these lines in such a manner that each column will pulse low once; columns 8 through 15, then columns 0 through 7. At that point, the cycle repeats.

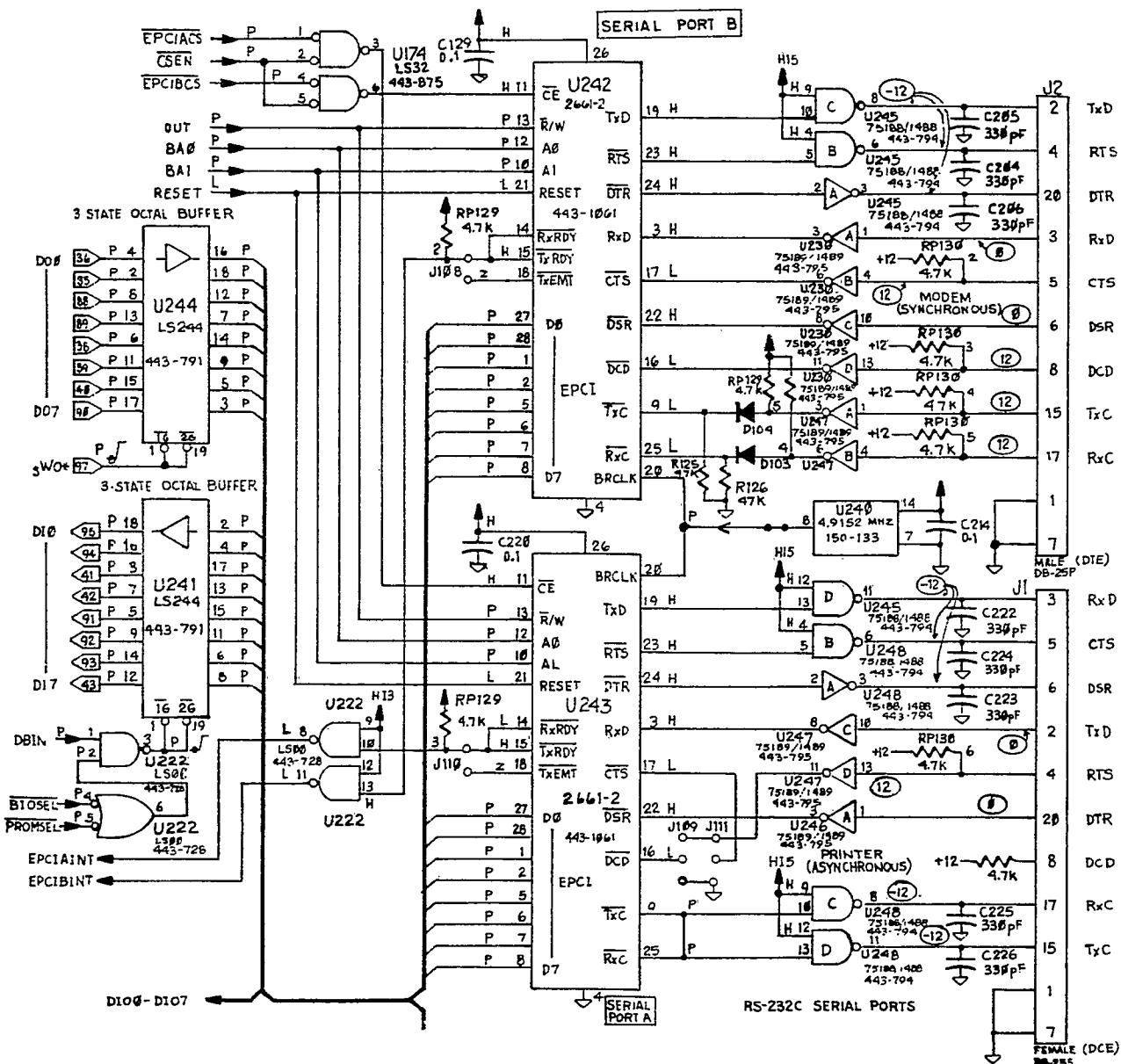
Note that U199 and U184 have open-collector outputs. When a key isn't being pressed, these lines will switch between a high-impedance state and logic zero, rather than between one and zero.

P24 Bidirectional I/O line programmed as an output. When the UPI has data to be sent to the CPU, it places the data on D0-D7 and then raises P24 to logic one. This asserts KEYINT, sending a keyboard interrupt to the CPU.

P27 Bidirectional I/O line programmed as an output. This line pulses to generate the bell and key click sounds. U183 NORs this line with P21 to generate the bell. When U183-1 goes low, it triggers the single-shot at U218. U218-10 pulses high for about 200 mS to gate U232-3, the 1-kHz oscillator, through U231 to the speaker.

To generate a key click, the negative edge of P27 directly fires the one-shot at U218-5. Pin 6 of this IC goes high for about 10 mS to gate U232 through U231 to the speaker. Note that the click line asserts whenever the bell does. However, since both circuits use the same oscillator, the click isn't heard.

See the "Keyboard" section in this manual for a complete description of the keyboard features and operating instructions.



SERIAL PORTS A AND B (MB4)

SERIAL PORTS A AND B

OVERVIEW

Refer to schematic MB4 as you read the following.

The two serial ports permit the H/Z-100 to communicate with external devices such as printers, MODEMs, plotters, and voice synthesizers. Since the serial ports are on the motherboard, the S-100 slots can be used for other purposes.

The serial ports are designed around the 2661-2 EPCI (Enhanced Programmable Communications Interface). These ICs have a large number of features, including:

- Polled or interrupt mode operation.
- Asynchronous or synchronous operation.
- 5 to 8-bit characters plus parity.
- Odd, even, or no parity.
- Baud rate from 45.5 baud to 38,400 baud.
- Full handshaking.

See the 2661-2 IC data sheets for complete specifications.

SERIAL PORT A

Serial port A consists of U243 and its surrounding circuitry. This port is a DCE port and can be used to connect to a line printer such as the H-25.

To select this port, the CPU addresses the following ports:

- OE8H Receiver holding register (read).
Transmitter holding register (write).
- OE9H Status registers (read).
SYN1/SYN2/DLE registers (write).
- OEAH Mode registers (read/write).
- OEBH Command registers (read/write).

When the CPU selects one of these ports, it asserts EPCIACS from the I/O port decoder and CSEN from the E-clock logic. These lines connect to pins 1 and 2 of U174 and assert the chip-enable line (pin 11) of U243.

Also, the CPU asserts pins 12 and 10 to select the right internal register. The OUT signal at U243-13 determines whether the selected register is written to or read from. This signal is derived from the sOUT signal at U214-14 on schematic MB2.

The CPU transmits and receives data at lines D0 through D7 on U243. If the CPU is transmitting data, it chip-enables U243, selects the correct register, raises U243-13 to logic one, places the data to be transmitted on the inputs of U244, and asserts SW0* at U244-1 and U244-19.

The data is loaded into the transmit data holding register inside the EPCI. The EPCI then asserts TxRDY at pin 15 to raise the EPCIAINT line at U222-8, interrupting the CPU. The CPU responds by not sending any more data until the transmitting holding register is empty.

The EPCI serially transmits the contents of the transmit data holding register out pin 19 and through U245, which converts the TTL to RS-232 levels. In asynchronous mode, the EPCI first sends a start bit, followed by the programmed number of data bits (5 to 8--LSB first), the parity bit (if programmed), and finally the programmed number of stop bits--1, 1-1/2, or 2.

Once the transmit data holding register is empty, the TxRDY line goes low to inform the CPU that it can send another byte.

In the receive mode, serial data enters the EPCI at pin 3 through U247C, which converts the +12-volt RS-232 levels to TTL levels. The EPCI extracts the data bits and loads it into the receive data holding register. The RxRDY line then goes low to interrupt the CPU through U222-10. When the CPU processes the interrupt, it addresses U243, places a logic zero on pin 13, and reads the data at D0-D7 through U241. U241 is selected by asserting the BIOSEL line (from the I/O port decoder) and DBIN at U222-1.

The handshake lines are standard EIA RS-232 control lines. These are clear to send (CTS), data set ready (DSR), request to send (RTS), and data terminal ready (DTR). To maintain RS-232 standards, they are swapped with their complementary lines at the DCE connector.

Jumpers J109 and J111 allow connecting the DCE RTS line to either CTS or to DCD on the EPCI. If connected to the clear-to-send line, pin 17, the RTS line controls the transmitter. If connected to the data carrier detect line at pin 16, then RTS controls the receiver.

Depending upon the peripheral, these lines may or may not be used; see the peripheral's technical manual for this information.

The crystal-controlled oscillator, U240, provides a 4.9152-MHz clock to U243-20. The EPCI uses this clock to generate the baud rate frequencies.

Pins 9 and 25 of U243 provide clock to the peripheral device, if it requires it. This timing can be either 1X or 16X the baud rate. Pins 9 and 25 are connected together since TxC is tri-stated during receive and RxC is tri-stated during transmit.

SERIAL PORT B

Serial port B consists of U242 and its surrounding circuitry. This port is a DTE port and can be used to connect to devices such as a MODEM or to another computer.

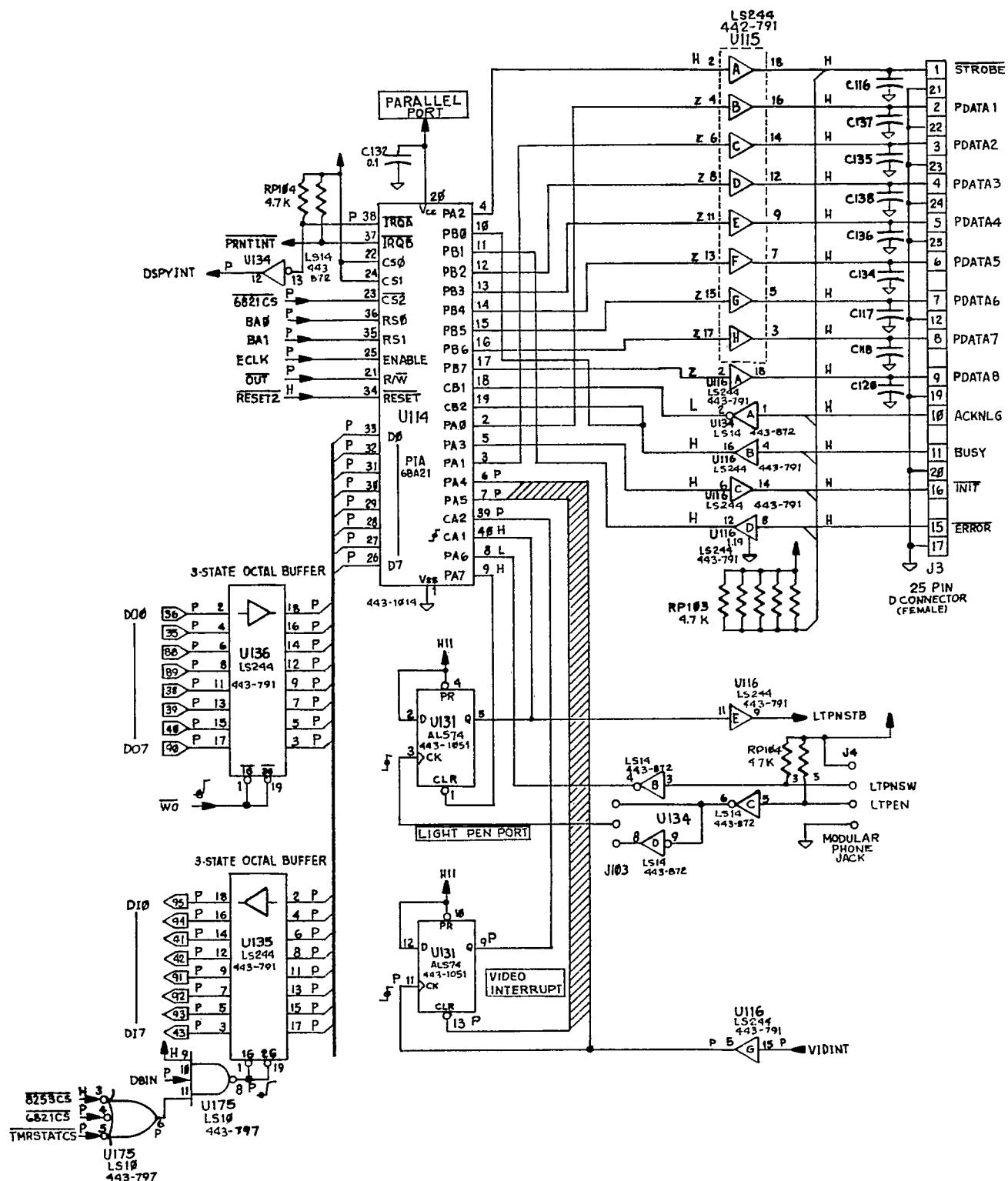
To select this IC, the CPU addresses the following ports:

- OECH Receiver holding register (read).
Transmitter holding register (write).
- OEDH Status registers (read).
SYN1/SYN2/DLE registers (write).
- OEEH Mode registers (read/write).
- OEFH Command registers (read/write).

The differences between this port and serial port A are minor. To chip-select this IC, the CPU asserts EPCIBCS instead of EPCIACS; the EPCI interrupts the computer through EPCIBINT instead of EPCIAINT; and pins 9 and 25 are clock inputs instead of outputs. This last feature is taken care of when the CPU initially programs the EPCI. The frequency can be 1X, 16X, or 64X the serial baud rate.

In the asynchronous mode, pins 9 and 25 act as outputs. Under these conditions, D103 and D104 isolate these pins from U247A and U247B.

Regulators U228 and U229 convert the +16-volt power supplies to the +12 volts required for RS-232 operation.



PARALLEL PORT (MB4)

PARALLEL PORT

OVERVIEW

Refer to schematic MB4 as you read the following circuit description.

The parallel port is designed around a 68A21 peripheral interface adapter (PIA) at U114. This IC performs three functions: (1) it operates as a printer port, (2) it serves as a port for a light pen, and (3) it couples the video board vertical retrace signal to the CPU.

The CPU accesses U114 for programming or data transfer through U135 and U136. At the same time it will chip-select U114 by asserting the $\overline{6821CS}$ control line from the I/O port decoder. The CPU also asserts address lines BA0 and BA1 (pins 36 and 35) to select the correct internal register.

The enable line, ECLK, comes from the E-clock logic circuits on schematic MB2 and provides timing to U114. All other signals to the PIA are referenced to either the rising or falling edges of this line.

The CPU asserts the \overline{OUT} line, U114-21, when the computer needs to write to the PIA. In all other cases, the PIA is in the read mode. Actual data transfer between the CPU and PIA takes place when the CPU asserts \overline{WO} at U136-1 for a write, or DBIN at U175-10 for a read.

The other connections to U114 will be covered in the following sections. For a complete description of the internal operation of the PIA, see the IC data sheets.

PRINTER PORT

The printer port is a parallel output port with handshaking capabilities. It allows connecting the H/Z-100 to some of the more popular printers without having to add a serial interface to the printer.

The parallel data leaves U114 at PB0 through PB7, couples through U115 to J3 where it becomes PDATA1 through PDATA8. J3 couples this data to the printer. When this data is sent, the STROBE line goes low to inform the printer that a new byte is present at its input.

The ACKNLG line asserts when the printer has processed the received byte and is ready to receive another character. This signal is inverted by U134A and sent to U114-18, CB1. This input can be programmed to detect either a negative-going or positive-going signal; allowing ACKNLG to assert on logic one or a logic zero.

CB1 detects the voltage transition and asserts the printer interrupt line at U114-37. When the H/Z-100 processes the interrupt, it will address U114's control register to determine which circuit caused the interrupt. When the CPU detects that the ACKNLG caused it, it will transmit the next byte to the printer.

The BUSY line asserts if the printer cannot accept a data byte at the time STROBE occurs. This can happen if the print head is moving (such as during a carriage return), or if the printer is in the off-line mode.

The BUSY signal is buffered by U116B and couples to CB2 and PA0 on U114. Input CB2 generates an interrupt in the same manner as CB1 in the ACKNLG circuits. The CPU responds to the interrupt, finds that a printer BUSY signal has occurred, and stops printing until the BUSY line goes to its inactive state.

To see when the BUSY line goes to the inactive state, the CPU monitors the logic level of PB0. This simplifies programming since, otherwise, CB2 must be reprogrammed to respond to the opposite-polarity signal transition.

The CPU uses the INIT line to initialize some printers. It does this by sending a short pulse (typically 50 nS) to the printer.

The ERROR line asserts if a printer failure occurs, such as when the ribbon needs changing, or when the printer runs out of paper. The CPU stops sending characters until the error is fixed.

LIGHT PEN PORT

The light pen circuits consist of U134B, C, and D, U116E, U131, and part of the PIA at U114.

By itself, the CPU will not respond to a signal from the light pen circuits. It must have a user-supplied program to set up interrupts, handle timing, and take care of bit locations pointed to by the light pen. As a result, this discussion will only be general.

When the CPU lights a dot on the CRT within the range of the light pen, the light pen sends a pulse to U134-5. Jumper J103 allows triggering from either the leading or trailing edge of this pulse.

This pulse will latch a logic one into U131-5 which couples through U116E to the light pen strobe input in the CRTC, U330, on the video board. The CRTC saves the address of the byte being accessed. See the video board circuit description for more details.

The output of U131 also couples to U114-40, the PIA. The rising edge of the signal at pin 40 causes IRQA at U114-38 to go low, which is inverted by U134-12 to cause a display interrupt at the CPU.

When the CPU acknowledges the interrupt, it must assert the 6821CS line (from the I/O decoder port) at U175-4. Line 6821CS also chip-selects U114 at pin 23 while BA0/BA1 addresses the PIA control register to see if the light pen circuits generated the interrupt. The OUT line at pin 21 and the DBIN line at U175-10 go to logic one to transfer the PIA data to the CPU.

If the interrupt was caused by light pen activity, the CPU processes it according to its program. Before finishing, the CPU clears U131-5 by pulsing a logic zero to U131-1.

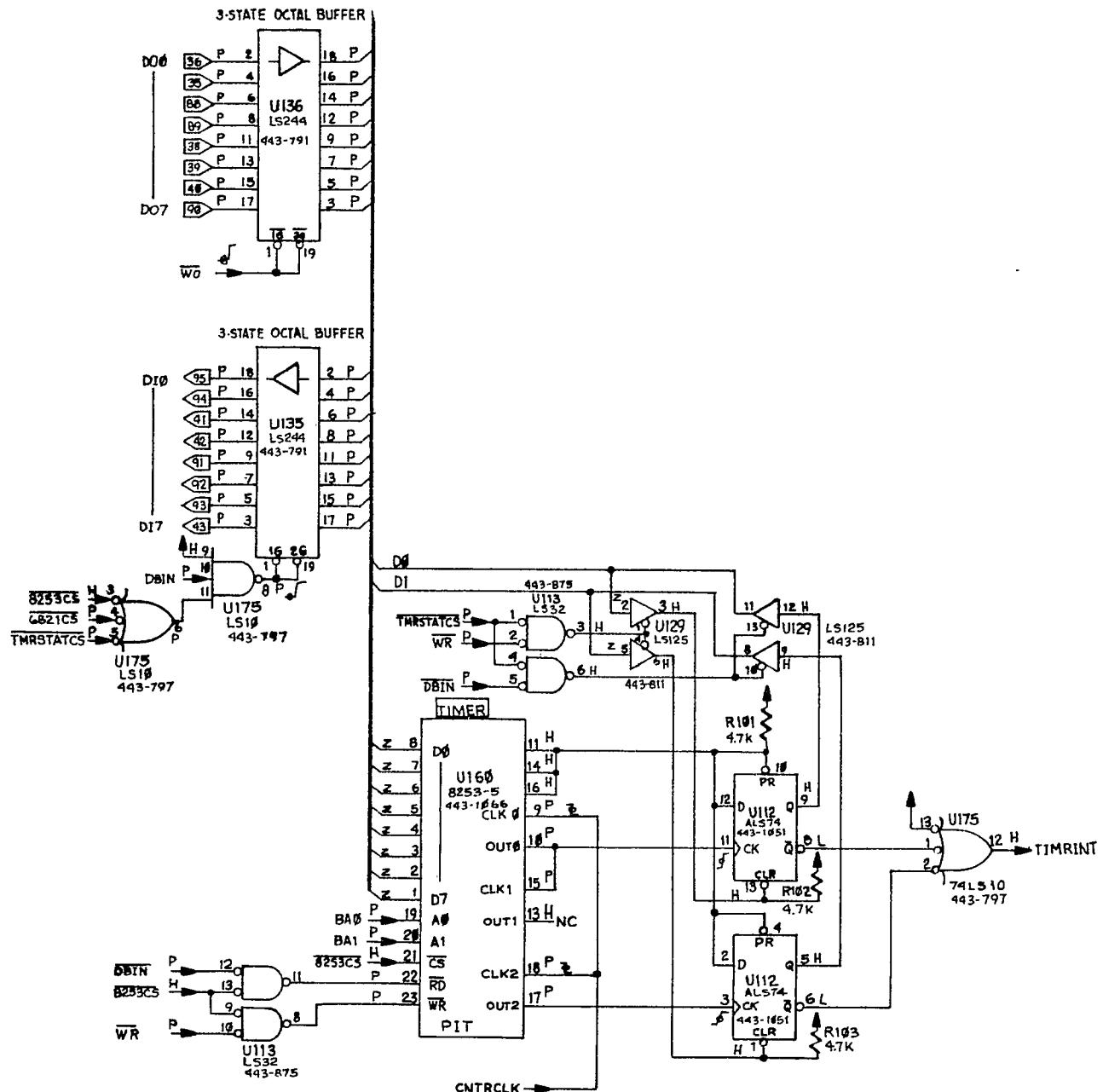
U134B, the light pen switch inverter, allows the CPU to monitor the status of a SPST switch connected to LTPNSW at J4. It does this by continually polling PA6 at U114-8. This allows you, for example, to move a dot around the CRT face with the light pen. As before, the H/Z-100 must be programmed to use this feature.

VIDEO INTERRUPT PORT

The video interrupt port consists of U116G, U131, and U114. The signal at U116-15, VIDINT, is the vertical sync pulse, VSYNC1D, buffered through U366-9 on the video board. The CPU times itself from this pulse so that it can update the display during vertical retrace; thus preventing interference on the display. See the video board circuit description for more details.

When a vertical sync pulse occurs, the positive-going edge from U116-5 latches a logic one into U131-9. This couples to U114-39 and causes the PIA to generate a display interrupt at U114-38.

When the CPU responds, it checks the PIA control register to determine which line caused the interrupt. Once it finds that VIDINT caused it, the CPU clears U131 by pulsing U114-7 low and then updates the display circuits as necessary.



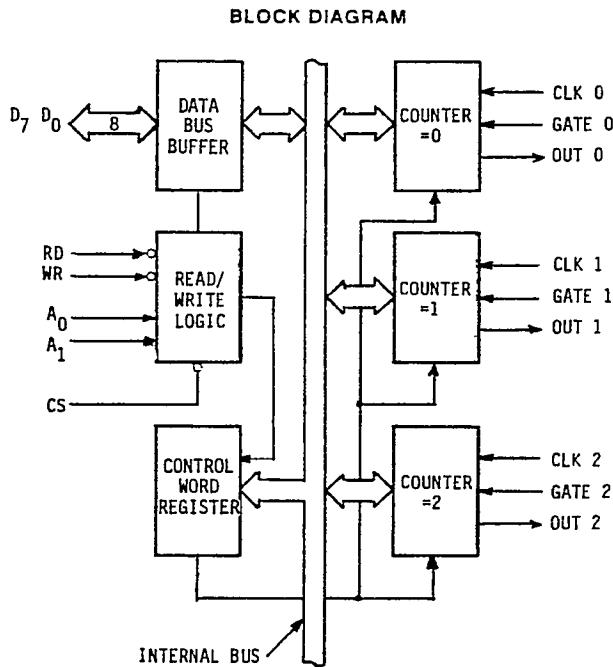
TIMER CIRCUITS (MB4)

TIMER

8253-5 BASICS

PIN NAMES

D ₇ D ₀	DATA BUS (8 BIT)
CLK N	COUNTER CLOCK INPUTS
GATE N	COUNTER GATE INPUTS
OUT N	COUNTER OUTPUTS
RD	READ COUNTER
WR	WRITE COMMAND OR DATA
CS	CHIP SELECT
A ₀ A ₁	COUNTER SELECT
V _{cc}	+5 VOLTS
GND	GROUND



The H/Z-100 timer circuit is designed around the 8253-5 programmable interval timer IC at U160.

Referring to the above block diagram, you'll see that the 8253-5 consists of three counters, a data bus buffer, read/write logic, and a control word register.

The counters are sixteen-bit down-counters with separate clock inputs, gate inputs, and outputs. The clock input causes its associated counter to decrement on the negative-going edge of the clock pulse. The gate input disables its associated counter when brought to logic zero. The output line will assert when the counter reaches zero; whether it asserts high or low depends on how its associated counter is programmed.

The read/write logic allows the CPU to communicate with the 8253-5. It communicates through the data bus buffer when CS and either RD or WR are asserted. Address lines A0 and A1 connect the data bus buffer to one of the counters or to the control word register.

If connected to one of the three counters, the CPU can load a starting count into the counter, or read the current count as the counter is down-counting. This data can be either 8 bits or 16 bits.

The CPU writes to the control word register to load it with an 8-bit programming byte. This byte selects the counter to be programmed, determines whether the counter is going to count an 8-bit or 16-bit word, and if it's going to count in binary or BCD. In addition, the control byte sets the operating mode of the counter.

The 8253-5 timer has 6 programmable operating modes. Briefly, these are:

Interrupt on Terminal Count—The output goes to logic one when the counter reaches zero (terminal count).

Programmable One-Shot—Not used in the H/Z-100 since the gate lines are tied to logic one.

Rate Generator—Divide-by-N counter. The output goes low for one clock period, returns high and counts down the number stored in the counter. When the counter reaches zero, the output pulses low again and the count starts over.

Square Wave Generator—The output remains high for one-half the count in the down-counter, then goes low for the remaining count.

Software Triggered Strobe—After the mode is set, the output will be high. When the count is loaded, the counter will begin counting. On terminal count, the output will go low for one clock period.

Hardware Triggered Strobe—Not used in the H/Z-100 because the gate lines are tied to logic one.

See the IC data sheet on the 8235-5 for detailed programming information.

TIMER OPERATION IN THE H/Z-100

Refer to schematic MB4 to see how the 8235-5 timer functions at U160.

The CPU selects the timer whenever it reads or writes port OE4 through OE7. These ports select counters 0 through 2 and the control word register, respectively. Line 8253CS, from the I/O port decoder, chip-selects U160-21 while BA0 and BA1 select the internal counter or register.

The 8253CS line also enables the two OR gates connected to pins 22 and 23 of U160. If the CPU is reading the data in U160, it asserts the DBIN line at U113-12; if it is writing to U160, it asserts WR at U113-10.

The output of counter #0, U160-10, couples to the input of counter #1 at U160-15. The counter #1 output isn't connected, but the CPU can still use this counter. When the output of counter #0 goes low, U160-10 decrements the count in counter #1 and also clocks the interrupt status latch (U112-11) to cause an interrupt. The CPU, if programmed to respond to this interrupt, will address U160 at pins 19 through 21, send a read command to pin 22, and then read the counter #1 data at pins 1 through 8.

The output of counter #2, U160-17, only connects to U112-3, the other interrupt status latch. Since both latches operate the same way, we will only discuss the operation of the latch for counter #2.

Assume that counter #2 of U160 is programmed to operate as a software-triggered strobe and that both status latches have previously been cleared. When counter #2 counts down to zero, U160-17 goes low for one clock period, then high again. This positive-going transition latches a logic one into U112-5. At the same time, U112-6 goes low to generate a timer interrupt at U175-12.

The CPU responds by asserting the TMRSTATCS line from the I/O port decoder and the data bus input line, DBIN. U113-6 goes low to enable U129 at pins 13 and 10. In turn, these two inverters couple the status of pins 9 and 5 of U112 to D0 and D1 of the data bus. The CPU notes that U112-5 has toggled so it processes the interrupt caused by U160-17.

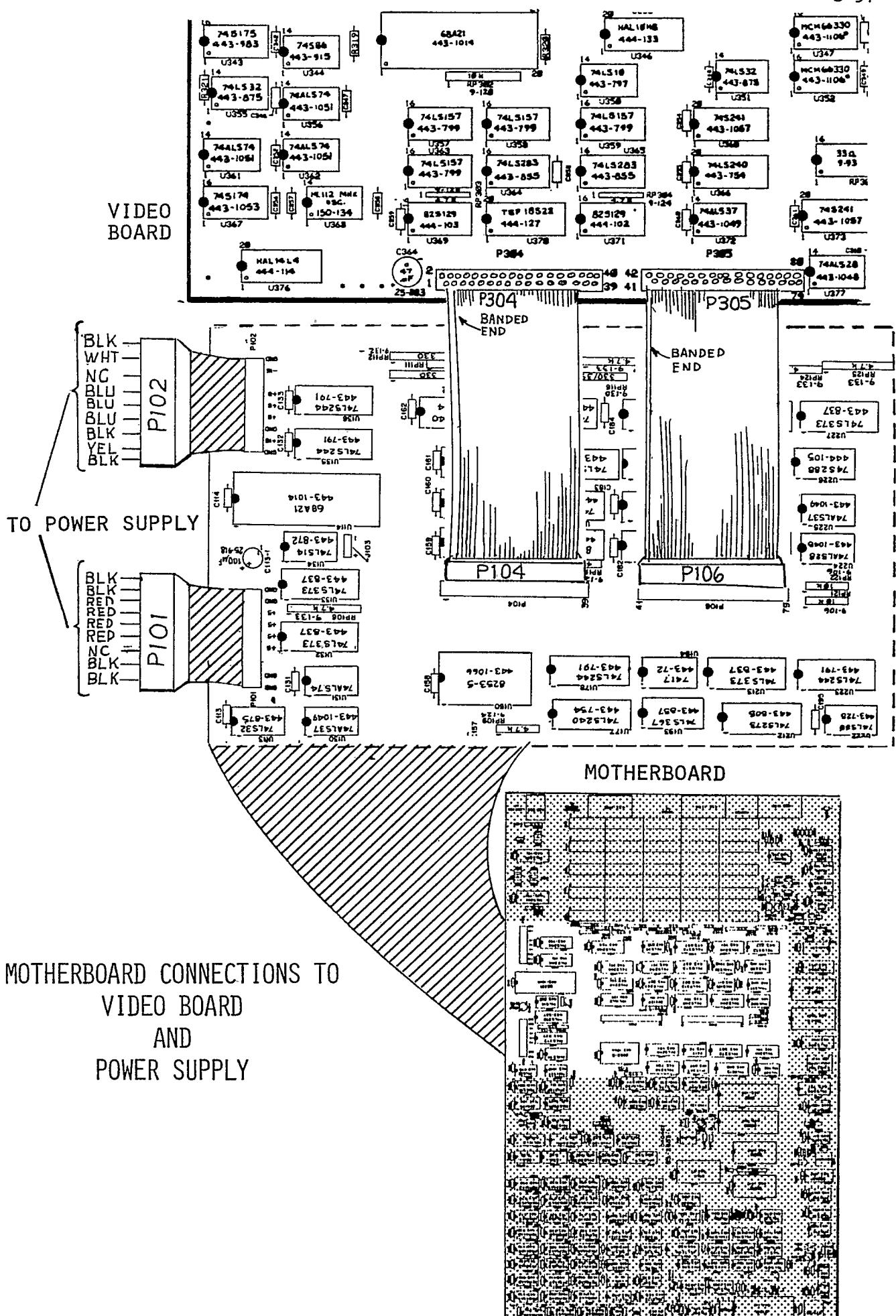
To clear the latch, the CPU again asserts TMRSTATCS, places a logic zero on data line D1, and asserts the write control line, WR. U129 couples D1 to U112-1 which forces pin 6 to one and pin 5 to zero.

The counter #0 circuits operate in the same manner.

VISUAL CHECKS

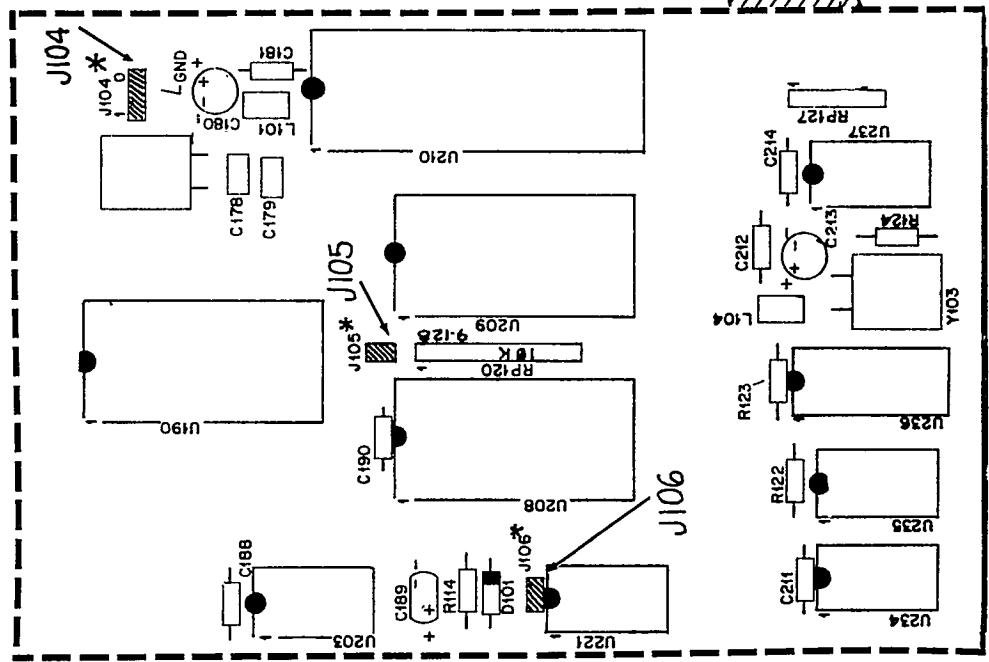
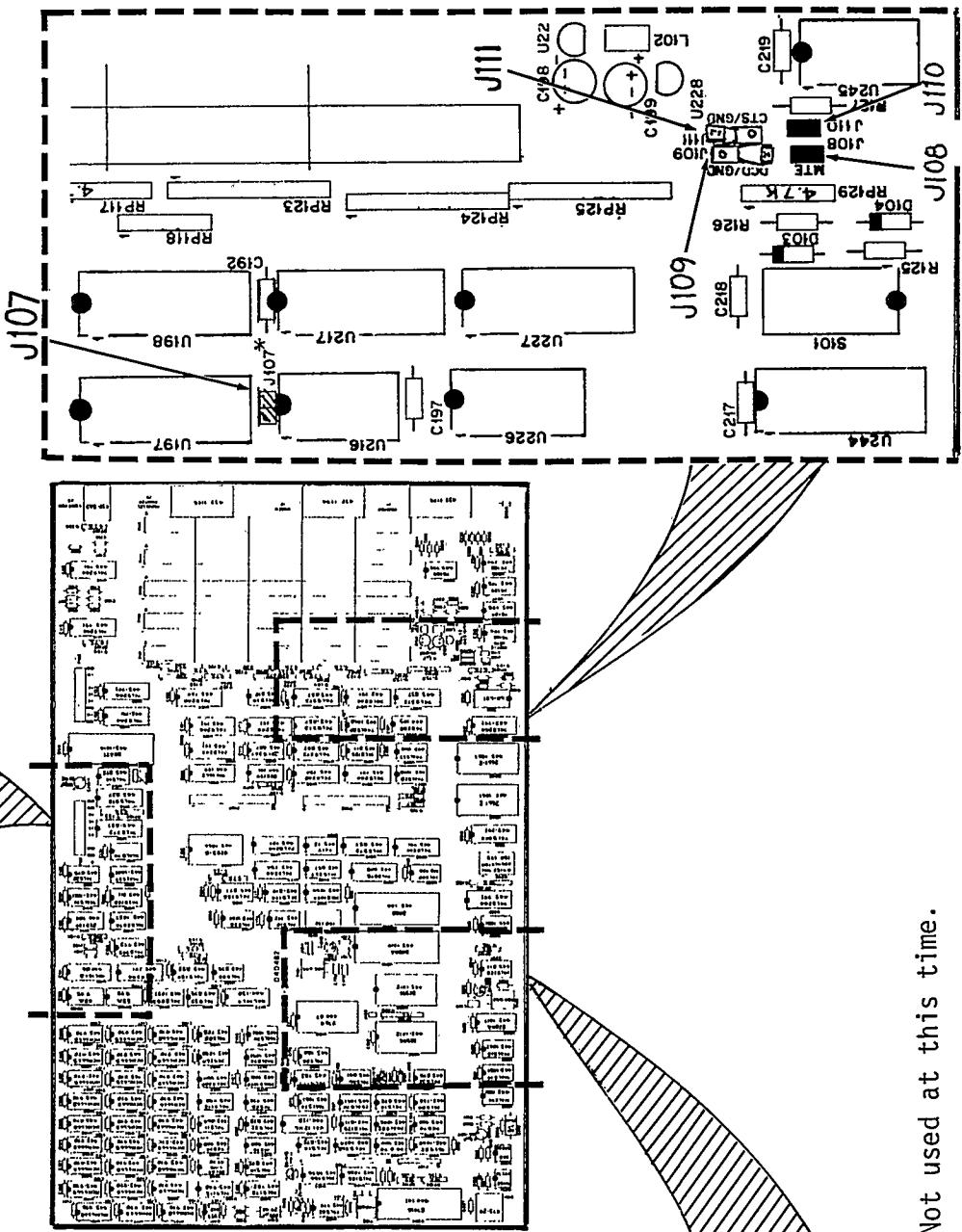
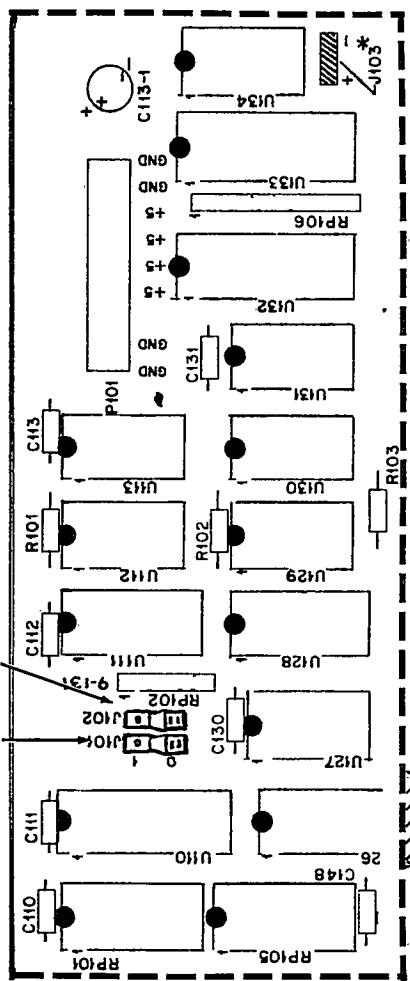
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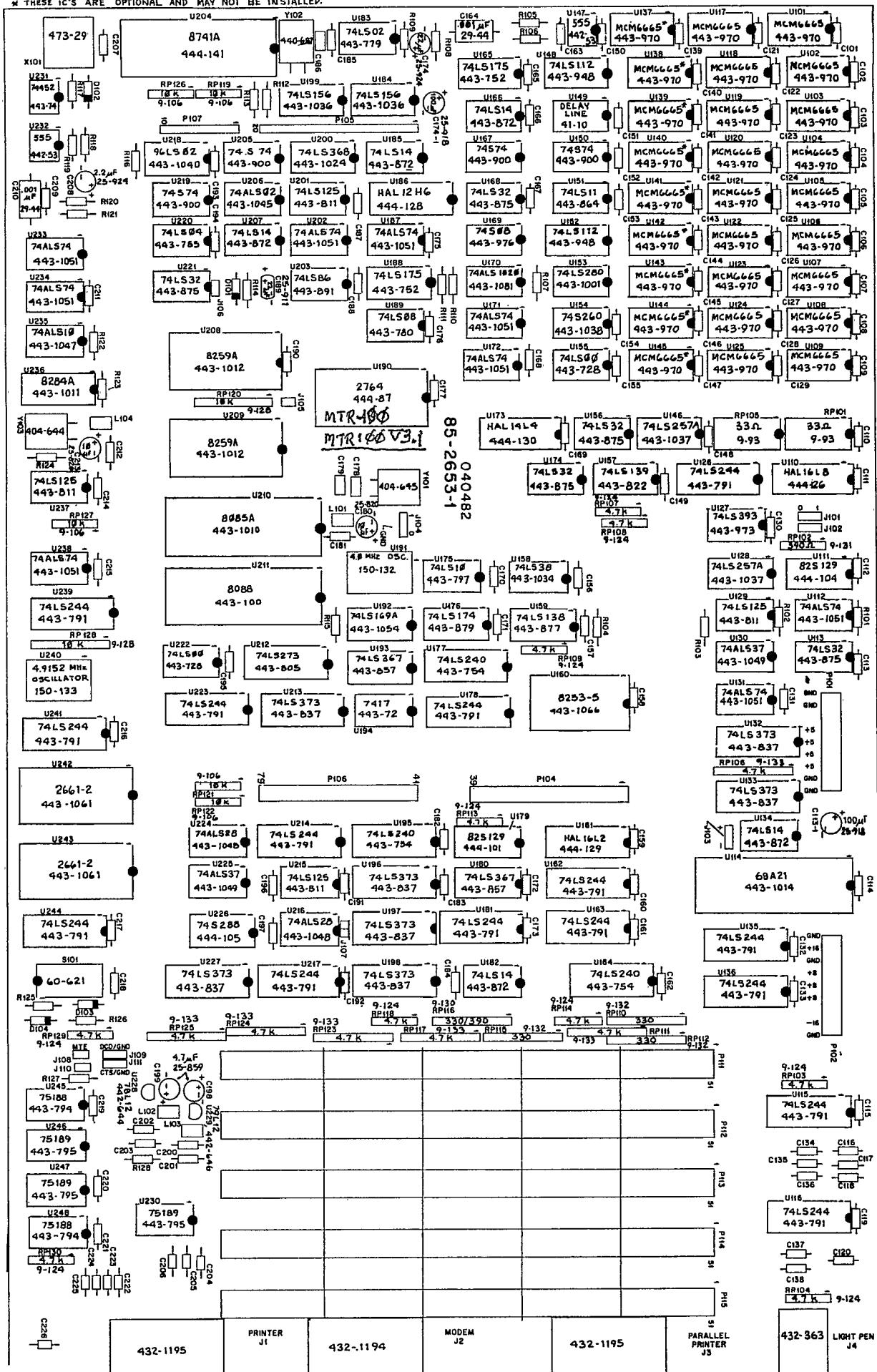




MOTHERBOARD JUMPER LOCATIONS AND CONFIGURATIONS

NOTE: Refer to "Configuration" for further explanation.





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MOTHERBOARD (HE-181-3630-1)
COMPONENT LOCATIONS AND VALUES

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INTRODUCTION

The following procedure will help you repair the motherboard to the point where you can boot a diagnostic disk. Diagnostic programs will allow more thorough and faster testing of the H/Z-100.

Currently, there aren't many diagnostic programs available. For this reason, we've included some checkout procedures that will help you test circuits that aren't critical to the boot-up operation. Though these tests aren't comprehensive, they'll help you narrow the problem down to two or three components.

As diagnostic programs become available, we will publish them for inclusion in the Diagnostics section of this manual. Also, if you develop any troubleshooting techniques or diagnostic programs that you'd like to share, send it to:

Heath Company
Service Publications and Training
Dept. 741
Benton Harbor, Mi. 49022

We will evaluate your submission, and when approved, publish it for inclusion in the Service Bulletins or Diagnostics sections of this manual. Be sure to include a complete description of the troubleshooting technique, symptoms caused by the failed component, and any special equipment needed to repair the problem. If submitting a diagnostic program, we will need a copy of the source listing; preferably on disk.

SERVICE GUIDE

As you become more experienced troubleshooting the H/Z-100, you'll be able to skip this section and go directly to the group of circuits causing the problem. Until then, use the following guide to locate the most likely circuits to test for a particular symptom.

Detailed checkout procedures for the major circuits on the video board follow the service guide. If this is your first time troubleshooting the H/Z-100, read the introduction to the checkout procedure before proceeding with those tests.

Finally, bear in mind that these test procedures are for isolating problems on the video board. All the other modules in the H/Z-100 must be known to be operating properly. Otherwise, you won't get the correct results.

1. Video circuits won't initialize. No power-up/reset beep heard.

Perform the following tests in the order listed:

Reset Circuits Tests
Processor Swap Tests
General CPU Tests
Interrupt Circuits Tests

2. Video circuits won't initialize. Power-up/reset beep heard.

Check U178 and U223 (schematic MB2).

Perform the following tests in the order listed:

E-Clock Logic Tests
Interrupt Circuits Tests
I/O Port Decoder Tests

3. System powers up properly, but characters on CRT are missing or distorted.

Check the system monitor, U190 (schematic MB2).

Perform the following tests:

Interrupt Circuits Tests
I/O Port Decoder Tests

4. Keyboard doesn't operate properly.

Perform the following tests:

Keyboard Circuit Tests
I/O Port Decoder Tests

5. Z-DOS will not complete the boot-up procedure; display locks up.

Perform the following test:

Timer Circuits Test

6. When booting Z-DOS, the CRT displays a parity error message.

Check parity circuits: U158, U152, U153, U151, U101, U117, and U137 (schematic MB3).

Perform the following tests:

Memory Circuits Tests #1
Memory Circuits Tests #2
I/O Port Decoder Tests

7. Intermittent problem when running a Z-DOS program.

Perform the system memory test described in the Diagnostics section (MEMTEST, option S).

8. Parallel printer port doesn't work.

Check Diagnostics section for in-depth testing.

Perform the following test:

Parallel Port Tests

9. Serial printer port doesn't work.

Check Diagnostics section for in-depth testing.

Perform the following test:

Serial Port A Tests

10. MODEM port doesn't work.

Check Diagnostics section for in-depth testing.

Perform the following test:

Serial Port B Tests

INTRODUCTION TO CHECKOUT PROCEDURES

In the following tests, you need only test the ICs in the left column indicated by an asterisk (*). If you don't get the suggested logic state, then check each IC listed immediately to the right. The logic states for these ICs are listed in the left column below the ICs with the asterisks.

Continue tracing backwards using this procedure until you test an IC that matches the suggested logic state. The previous IC that you tested is likely the bad IC.

Before you replace the suspected IC, check the other lines leading up to it. You must do this because this checkout procedure gives only the most likely causes to the problem. It doesn't cover such things as open ground foils, foil runs shorted together, open resistors, or missing power supplies.

To help you locate the IC on a schematic, the schematic number is shown in parenthesis to the right of the IC under test.

Unless instructed otherwise, perform these tests with the H/Z-100 configured for 5-1/4" drives (primary) and with auto-boot defeated. See the Configuration section. Also, unless noted otherwise, all logic states are those present after a power-up reset or CTRL/RESET.

BUS CONTROL OUTPUT TESTS

CHECK	IF NOT OKAY, CHECK
*U180-3 = P (MB1)	U180-2, U180-1, U180-15
*U180-5 = P (MB1)	U180-4, U180-1, U180-15
*U180-7 = P (MB1)	U180-6, U180-1, U180-15
*U180-9 = L (MB1)	U180-10, U180-1, U180-15
*U180-11 = P (MB1)	U180-12, U180-1, U180-15

Go to BUS CONTROL OUTPUT RESET TESTS.

U180-1 = L (MB1)	U182-6
U180-2 = P (MB1)	U219-9
U180-4 = P (MB1)	U234-9
U180-6 = P (MB1)	U206-10
U180-10 = L (MB1)	See PROCESSOR SWAP TESTS.
U180-12 = P (MB1)	U235-12
U180-15 = L (MB1)	U182-6
U182-5 = H (MB1)	Check S-100 bus, pin 19.
U182-6 = L (MB1)	U182-5
U206-8 = P (MB1)	U219-9
U206-9 = P (MB1)	See GENERAL CPU TESTS.
U206-10 = P (MB1)	U206-8, U206-9
U219-1 = P (MB1)	U219-3, U219-8
U219-3 = P (MB1)	U221-3
U219-5 = P (MB1)	U219-3, U219-1
U219-8 = P (MB1)	U219-11, U219-12, U219-13. NOTE: If you're "stuck in a loop" on this test, see the BUS CONTROL OUTPUT RESET TESTS.
U219-9 = P (MB1)	U219-11, U219-12, U219-13
U219-11 = P (MB1)	See CLOCK CIRCUITS TESTS.
U219-12 = P (MB1)	U219-5
U219-13 = H (MB1)	See RESET CIRCUITS TESTS.
U220-12 = P (MB1)	See GENERAL CPU TESTS.

U221-1 = P (MB1)	See GENERAL CPU TESTS.
U221-2 = L (MB1)	U237-11
U221-3 = P (MB1)	U221-1, U221-2
U234-9 = P (MB1)	U234-11, U234-12
U234-11 = P (MB1)	See CLOCK CIRCUITS TESTS.
U234-12 = P (MB1)	U219-8
U235-1 = P (MB1)	U234-9
U235-2 = P (MB1)	U219-8
U235-12 = P (MB1)	U235-1, U235-2, U235-13
U235-13 = P (MB1)	U220-12
U237-11 = L (MB1)	U237-12
U237-12 = L (MB1)	See GENERAL CPU TESTS.

BUS CONTROL OUTPUT RESET TESTS

Press and release the CTRL/RESET keys as you make the following measurements.

CHECK	IF NOT OKAY, CHECK
-------	--------------------

*U180-3 = L (MB1)	U180-2
*U180-5 = H (MB1)	U180-4
*U180-7 = L (MB1)	U180-6
*U180-9 = L (MB1)	U180-10
*U180-11 = H (MB1)	U180-12

End of tests.

U180-2 = L (MB1)	U219-9
U180-4 = H (MB1)	U234-9
U180-6 = L (MB1)	U206-10
U180-10 = L (MB1)	See PROCESSOR SWAP TESTS.
U180-12 = H (MB1)	U235-12
U206-9 = H (MB1)	See GENERAL CPU TESTS.
U206-10 = L (MB1)	U206-9
U219-8 = H (MB1)	U219-13
U219-9 = L (MB1)	U219-13
U219-13 = L (MB1)	See RESET CIRCUITS TESTS.
U220-12 = L (MB1)	See GENERAL CPU TESTS.
U234-9 = H (MB1)	U234-11, U234-12
U234-11 = P (MB1)	See CLOCK CIRCUITS TESTS.
U234-12 = P (MB1)	U219-8
U235-12 = H (MB1)	U235-13
U235-13 = L (MB1)	U220-12

CLOCK CIRCUITS TESTS

CHECK	IF NOT OKAY, CHECK
*U192-11 = P (MB1)	U192-2
*U216-4 = P (MB1)	U216-5
*U225-3 = P (MB1)	U225-1, U225-2
*U225-11 = P (MB1)	U225-12, U225-13

End of tests.

U188-2 = H (MB1)	U188-4
U188-4 = H (MB1)	See PROCESSOR SWAP TESTS
U188-5 = H (MB1)	U188-2
U188-6 = L (MB1)	U188-7
U188-7 = H (MB1)	U188-9, U188-5
U188-9 = P (MB1)	U225-6
U188-11 = L (MB1)	U188-9, U188-12
U188-12 = H (MB1)	U188-7
U191-8 = P (MB1)	U191 or C115 is defective.
U192-2 = P (MB1)	U191-8
U192-14 = P (MB1)	U192-2
U200-1 = H (MB1)	U203-6
U200-2 = P (MB1)	U210 (8085 CPU) is defective.
U200-13 = Pulse 180 degrees out of phase with U200-14 (use dual-trace oscillo- scope).	If not 180 degrees out of phase, check U200-15 and U200-1. If missing, then U236 is defective.
U200-15 = L (MB1)	U203-3
U203-2 = L (MB1)	U188-6
U203-3 = L (MB1)	U203-2
U203-4 = H (MB1)	U188-7
U203-6 = H (MB1)	U203-4
U203-8 = H (MB1)	U203-9, U203-10
U203-9 = H (MB1)	U188-7
U203-10 = L (MB1)	U188-11

U216-5	= P	(MB1)	U192-14
U225-1	= P	(MB1)	U200-13
U225-2	= H	(MB1)	U203-8
U225-5	= P	(MB1)	U200-13
U225-6	= P	(MB1)	U225-5
U225-12	= H	(MB1)	U203-8
U225-13	= P	(MB1)	U200-13, U200-2

E-CLOCK LOGIC TESTS

<u>CHECK</u>	<u>IF NOT OKAY, CHECK</u>
*U224-4 = P (MB2)	U224-5, U224-6
*U224-10 = P (MB2)	U224-8, U224-9
*U224-13 = P (MB2)	U224-11, U224-12
*U238-9 = P (MB2)	U238-10, U238-11, U238-12

Go to E CLOCK LOGIC RESET TESTS

U195-6 = P (MB2)	See BUS CONTROL OUTPUT CIRCUIT TESTS.
U195-7 = P (MB2)	U195-13
U195-9 = P (MB2)	U195-11
U195-11 = P (MB2)	See CLOCK CIRCUITS TESTS.
U195-13 = P (MB2)	See BUS CONTROL OUTPUT CIRCUITS TESTS.
U195-14 = P (MB2)	U195-6
U214-4 = P (MB2)	See STATUS CIRCUITS TESTS.
U214-6 = P (MB2)	See STATUS CIRCUITS TESTS.
U214-8 = P (MB2)	See BUS CONTROL OUTPUT CIRCUITS TESTS.
U214-12 = P (MB2)	U214-8
U214-14 = P (MB2)	U214-6 See BUS CONTROL OUTPUT CIRCUITS TESTS.
U214-16 = P (MB2)	U214-4
U214-18 = P (MB2)	U214-2
U220-8 = P (MB2)	U220-9
U220-9 = P (MB2)	U221-8
U221-8 = P (MB2)	U221-10, U221-9
U221-9 = P (MB2)	U233-9
U221-10 = L (MB2)	See RESET CIRCUITS TESTS.

U224-1 = P (MB2)	U224-2, U224-3
U224-2 = P (MB2)	U195-14
U224-3 = P (MB2)	U214-12
U224-5 = P (MB2)	U224-1
U224-6 = P (MB2)	U238-6
U224-8 = P (MB2)	U214-14
U224-9 = P (MB2)	U214-16
U224-10 = P (MB2)	U224-8, U224-9
U224-11 = P (MB2)	U195-7
U224-12 = P (MB2)	U214-18
U224-13 = P (MB2)	U224-11, U224-12
 U233-9 = P (MB2)	Check the foil runs to U233, pins 11, 12, and 13 against the schematic. If these are okay, then replace U233.
 U238-1 = P (MB2)	U238-8
U238-2 = P (MB2)	U238-8
U238-3 = P (MB2)	U195-9
U238-6 = P (MB2)	U238-1, U238-2, U238-3
U238-8 = P (MB2)	U238-10, U238-11, U238-12
U238-10 = P (MB2)	U220-8
U238-11 = P (MB2)	U224-13
U238-12 = P (MB2)	U224-10

E-CLOCK LOGIC RESET TESTS

Press and release the CTRL/RESET keys as you make the following measurements.

<u>CHECK</u>	<u>IF NOT OKAY, CHECK</u>
*U224-4 = L (MB2)	U224-6
*U233-9 = L (MB2)	U233-13
*U238-9 = H (MB2)	U238-10

End of tests.

U220-8 = L (MB2)	U220-9
U220-9 = H (MB2)	U221-8
U221-8 = H (MB2)	U221-10
U221-10 = H (MB2)	See RESET CIRCUITS TESTS.
U224-6 = H (MB2)	U238-6
U233-13 = L (MB2)	U238-8
U238-1 = L (MB2)	U238-8
U238-6 = H (MB2)	U238-1
U238-8 = L (MB2)	U238-10
U238-10 = L (MB2)	U220-8

GENERAL CPU TESTS

In the following tests, the CPU will not be able to initialize the video board. This results in a high-pitched whine from the monitor fly-back transformer and an incorrect raster on the CRT. To avoid this distraction, disconnect the video cable (and power cable for the all-in-one model) between the video board and monitor (or video sweep board for the all-in-one).

Now perform the following steps.

-- Unplug U187 (schematic MB1).

This puts both processors into a hold state.

-- Unplug U217 (schematic MB1).

This isolates the CPUs from the monitor ROM.

-- Plug the programming plug described under Systems Troubleshooting into the socket at U187.

-- Turn on the H/Z-100 and press and release the CTRL/RESET keys once.

-- Refer to schematic MB1 and check for a logic one on each line of the address/data bus, ADO-AD7.

If any line is low, check for a short circuit on the bus. This includes internal shorts on U211, U210, U198, U197, U209, U208 and U212.

If the lines are pulsing, then one of the CPUs isn't in a hold state. Check U211-30 and U210-38. If either pin is logic zero, replace the appropriate IC. Also check for leakage to ground on U211-31 and U210-39.

-- Check the logic states of the ICs in the following chart. If any are incorrect, check the suggested ICs in the right column. Otherwise go on to the next test.

CHECK IF NOT OKAY, CHECK

*U211-19 = P (MB1) U236 or Y103 defective.
 *U211-22 = P (MB1) U336-5
 *U211-29 = P (MB1) U211 defective.
 *U211-32 = P (MB1) U211 defective.

Go on to the next test. .

U177-4 = H	(MB1)	Short on pin 3 of S-100 bus.
U177-12 = P	(MB1)	U177-13
U177-13 = P	(MB1)	Short on pin 72 of S-100 bus, or U194-12 defective (MB2).
U177-16 = L	(MB1)	U177-4
U205-9 = P	(MB1)	U205-11, U205-12, U205-13
U205-11 = P	(MB1)	Restore U187 and U217 and perform the CLOCK CIRCUITS TEST.
U205-12 = P	(MB1)	U206-13
U205-13 = H	(MB1)	U206-1
U206-1 = H	(MB1)	U206-2, U206-3
U206-2 = L	(MB1)	U226-9
U206-3 = L	(MB1)	U221, U237, U210, or U211 defective.
U206-11 = P	(MB1)	U177-12
U206-12 = L	(MB1)	U177-16
U220-10 = H	(MB1)	U220-11
U220-11 = L	(MB1)	U221, U237, U210, or U211 defective.
U226-9 = L	(MB1)	U226-10, U226-11, U226-12, U226-13, U226-14
U226-10 = H	(MB1)	U210, U211, or U237 defective.
U226-11 = H	(MB1)	U210, U211, or U237 defective.
U226-12 = H	(MB1)	U210 or U211 defective.
U226-13 = H	(MB1)	Restore U187 and U217 and perform the PROCESSOR SWAP TESTS.
U226-14 = H	(MB1)	U233-5
U233-1 = H	(MB1)	U220-10
U233-3 = P	(MB1)	Restore U187 and U217 and perform the CLOCK CIRCUITS TESTS.
U233-5 = H	(MB1)	U233-1, U233-3
U236-4 = P	(MB1)	U205-9
U236-5 = P	(MB1)	U236-4

-- Check for the following logic states on the 8085 CPU,
U210. If any are incorrect, replace U210.

Pin 29 = H
Pin 30 = L
Pins 31-34 = H
Pin 39 = P

-- Connect a jumper wire from U187-9 to ground.

This will activate the 8085 CPU.

-- Reset the computer once to ensure that the circuits
are in a known state.

-- Check for pulses on pins 12-19 and pins 21-28 of U210.

If incorrect, replace U210. Also check for shorted
or open circuits on the address/data bus.

-- Check for the following logic states on U210. If any
are incorrect, replace U210.

Pin 29 = H
Pins 30-33 = P
Pin 34 = L
Pin 38 = L
Pin 39 = L

-- Remove the jumper wire from U187-9.

-- Connect the jumper wire from ground to U187-5.

This will activate the 8088 CPU.

-- Reset the computer once to ensure that the circuits
are in a known state.

-- Check for pulses on pins 2-16 and 36-39 on U211.

If any are incorrect, replace U211. Also check the
appropriate bus line for short circuits.

-- Check for the following logic states on U211. If any are incorrect, replace U211.

Pin 25 = P
Pin 27 = P
Pin 28 = L
Pin 29 = P
Pins 30-31 = L
Pin 32 = P
Pin 34 = P

-- Check for the following logic states. If incorrect, check U213, U193, and U212 (MB1).

U213-2 = P
U213-5 = P
U213-6 = P
U213-9 = P
U213-12 = L
U213-15 = L
U213-16 = L
U213-19 = L

-- Check the output pins (2, 5, 6, 9, 12, 15, 16, and 19) of U197 and U196 for pulses (MB1).

If any of these lines aren't pulsing, replace the appropriate IC.

-- Check for pulses on the following pins of the socket of U217 (MB1): 2, 4, 6, 8, 11, 13, 15, 17.

If any pulses are missing, check U244 and U241 on schematic MB4. Also check the following components on schematic MB2.

U239
U161 (ROMSEL)
U190 (MTR-100)

Pins 11-19, 20, and 22 of U190 should pulse. If not, then check the above three ICs and U195-16 (MB2).

-- Restore U187 and U217 to their sockets.

Tests complete.

INTERRUPT TESTS

CHECK	IF NOT OKAY, CHECK
*U208-18 = L (MB1)	U177-18
*U208-19 = L (MB1)	U172-9
*U208-20 = H (MB1)	See TIMER CIRCUITS TEST.
*U208-21 = L (MB1)	U209-17
*U208-22 = L (MB1)	U222-8
*U208-23 = L (MB1)	U222-11
*U208-24 = P (MB1)	U207-4
*U208-25 = L (MB1)	U207-12
*U210-6 = L (MB1)	U189-11
*U210-10 = L (MB1)	U189-3
*U211-17 = L (MB1)	U189-8
*U211-18 = P (MB1)	U189-6

End of tests.

J104 = Ground (MB1)	J104 is a foil run to ground; no connector pins are installed here. If U156-5 = H, then J104 is open or connected to U177-14.
U114-38 = P (MB4)	See PARALLEL PORT TESTS.
U134-12 = P (MB4)	U134-13
U134-13 = P (MB4)	U114-38
U151-8 = P (MB3)	See MEMORY CIRCUITS TEST.
U152-9 = L (MB3)	U152-11, U152-13, U152-14
U152-11 = P (MB3)	U153 or U151 is defective. Also check parity RAM.
U152-13 = L (MB3)	U151-8
U152-14 = L (MB3)	See MEMORY CONTROL LATCH TEST.
U155-8 = H (MB1)	U155-9, U155-10
U155-9 = P (MB1)	U156-6
U155-10 = L (MB1)	U172-5

U156-4 = P (MB1)	U202-9
U156-5 = L (MB1)	U156-8
U156-6 = P (MB1)	U156-4, U156-5
U156-8 = L (MB1)	U156-9, U156-10
U156-9 = L (MB1)	U182-10
U156-10 = L (MB1)	J104, U177-14
U158-4 = L (MB3)	U152-9
U158-5 = L (MB3)	U152-9
U158-6 = H (MB3)	U158-4, U158-5
U158-8 = P (MB1)	U158-10
U158-10 = P (MB1)	U208-17
U164-2 = H (MB1)	Pin 4 of S-100 bus shorted to ground.
U164-3 = L (MB1)	U164-17
U164-4 = H (MB1)	Pin 5 of S-100 bus shorted to ground.
U164-5 = L (MB1)	U164-15
U164-6 = H (MB1)	Pin 6 of S-100 bus shorted to ground.
U164-7 = L (MB1)	U164-13
U164-8 = H (MB1)	Pin 7 of S-100 bus shorted to ground.
U164-9 = L (MB1)	U164-11
U164-11 = H (MB1)	Pin 11 of S-100 bus shorted to ground.
U164-12 = L (MB1)	U164-8
U164-13 = H (MB1)	Pin 10 of S-100 bus shorted to ground.
U164-14 = L (MB1)	U164-6
U164-15 = H (MB1)	Pin 9 of S-100 bus shorted to ground.
U164-16 = L (MB1)	U164-4
U164-17 = H (MB1)	Pin 8 of S-100 bus shorted to ground.
U164-18 = L (MB1)	U164-2
U171-8 = L (MB1)	U171-10, U171-11, U171-12, U171-13
U171-9 = H (MB1)	U171-8
U171-10 = H (MB1)	U155-8
U171-11 = L (MB1)	U206-4
U171-12 = P (MB1)	See GENERAL CPU TESTS.
U171-13 = H (MB1)	See the RESET CIRCUITS TESTS.

U172-1 = H (MB1)	See the RESET CIRCUITS TESTS.
U172-2 = P (MB1)	See GENERAL CPU TESTS.
U172-3 = L (MB1)	U206-4
U172-5 = L (MB1)	U172-1, U172-2, U172-3
U172-6 = H (MB1)	U172-5
U172-9 = L (MB1)	U172-11, U172-12, U172-13
U172-11 = L (MB1)	U206-4
U172-12 = P (MB1)	See GENERAL CPU TESTS.
U172-13 = H (MB1)	See RESET CIRCUITS TESTS.
U177-2 = H (MB1)	U158-6 or short circuit on pin 98 of S-100 bus.
U177-3 = P (MB1)	U177-17
U177-6 = H (MB1)	Short circuit on pin 13 of S-100 bus.
U177-14 = L (MB1)	U177-6
U177-17 = P (MB1)	U158-8 or short circuit on S-100 bus, pin 73.
U177-18 = L (MB1)	U177-2
U182-10 = L (MB1)	U182-11
U182-11 = H (MB1)	Pin 12 of S-100 bus shorted to ground.
U189-1 = P (MB1)	U202-9
U189-2 = L (MB1)	U220-2
U189-3 = L (MB1)	U189-1, U189-2
U189-4 = P (MB1)	U202-9
U189-5 = H (MB1)	U171-9
U189-6 = P (MB1)	U189-4, U189-5
U189-8 = L (MB1)	U189-9, U189-10
U189-9 = H (MB1)	U171-9
U189-10 = L (MB1)	U156-8
U189-11 = L (MB1)	U189-12, U189-13
U189-12 = L (MB1)	U220-2
U189-13 = L (MB1)	U156-8
U202-1 = P (MB1)	U177-3
U202-2 = P (MB1)	U177-3
U202-3 = P (MB1)	See CLOCK CIRCUITS TEST.
U202-5 = P (MB1)	U202-1, U202-2, U202-3
U202-9 = P (MB1)	U202-12, U202-11
U202-11 = P (MB1)	See CLOCK CIRCUITS TESTS.
U202-12 = P (MB1)	U202-5

U206-4 = L (MB1)	U206-5, U206-6
U206-5 = H (MB1)	See I/O PORT DECODER TESTS.
U206-6 = P (MB1)	See the BUS CONTROL OUTPUT TESTS.
U207-3 = P (MB1)	U216-13
U207-4 = P (MB1)	U207-3
U207-12 = L (MB1)	U207-13
U207-13 = H (MB1)	See PARALLEL PORT TESTS.
U208-17 = P (MB1)	U208-18, U208-19, U208-20, U208-21, U208-22, U208-23, U208-24, U208-25
U208-18 = L (MB1)	U177-18
U208-19 = L (MB1)	U172-9
U208-20 = H (MB1)	See TIMER CIRCUITS TEST.
U208-21 = L (MB1)	U209-17
U208-22 = L (MB1)	U222-8
U208-23 = L (MB1)	U222-11
U208-24 = P (MB1)	U207-4
U208-25 = L (MB1)	U207-12
U209-17 = L (MB1)	U209-18, U209-19, U209-20, U209-21, U209-22, U209-23, U209-24, U209-25
U209-18 = L (MB1)	U164-18
U209-19 = L (MB1)	U164-16
U209-20 = L (MB1)	U164-14
U209-21 = L (MB1)	U164-12
U209-22 = L (MB1)	U164-3
U209-23 = L (MB1)	U164-5
U209-24 = L (MB1)	U164-7
U209-25 = L (MB1)	U164-9
U216-11 = L (MB1)	See KEYBOARD TESTS.
U216-12 = P (MB1)	U134-12
U216-13 = P (MB1)	U216-11, U216-12
U220-1 = H (MB1)	U225-9, U225-10
U220-2 = L (MB1)	U220-1
U222-8 = L (MB4)	U222-10
U222-10 = H (MB4)	See SERIAL PORT A TESTS.
U222-11 = L (MB4)	U222-13
U222-13 = H (MB4)	See SERIAL PORT B TESTS.
U225-9 = L (MB1)	U171-8
U225-10 = H (MB1)	U172-6

KEYBOARD CIRCUIT TESTS

The 2-line-to-4-line decoders, U199 and U184, have open-collector outputs. These outputs are left floating; that is, they're not tied to logic one through pull-up resistors. So, although the outputs are continually switching on and off, you won't see a pulse unless a key is pressed.

Note, however, that some logic probes will show pulses on the decoder outputs when no key is pressed. This is due to the probe sensitivity and system noise. If your logic probe shows pulses where there should be none, check with an oscilloscope.

-- Turn on the H/Z-100.

-- Check for pulses at pins 21 through 24 of U204.

If these pulses aren't present, then check the logic levels of pins 2 through 10 against the schematic. If these are incorrect, then check the I/O port decoder, the status circuits, the bus control output circuits, and the reset circuits.

Also check the crystal at Y102.

-- Turn off the H/Z-100.

-- Locate U185 (near P105 on the right-front side of the motherboard) and lift pin 11.

-- Turn on the H/Z-100.

-- Connect a jumper wire between U185-11 and ground.

This places both CPUs into the HOLD state to prevent the monitor from sounding the bell when you perform the following tests.

-- Press the SPACE BAR once.

You should hear a key click from the audio transducer, X101. If not, then check U231, U232, U218, and U204. If U204-38 pulses when you press the SPACE BAR, then skip the following steps and perform the tests under "Keyboard Test Chart."

-- Simultaneously press the left SHIFT and RESET keys.

The display, if connected, will go blank. This is normal.

-- Press the SPACE BAR 18 times.

You should hear a key click for the first 17 presses; the 18th should be silent. This indicates the internal type-ahead buffer of U204 is working properly.

-- Reset the computer.

-- Press and hold the SPACE BAR down.

The keyclick should occur 17 times and then go silent. This verifies U204's auto-repeat function.

-- Reset the computer.

KEYBOARD TEST CHART

Measure the following pins on P105 as you press the indicated key. Unless noted otherwise, the pin should pulse as you hold the key down. Note that the line under test will latch to a logic one after 17 key clicks, so you must periodically reset the computer.

Refer to the keyboard schematic in the Keyboard section of this manual to check the keys not listed in the following chart.

P105 No.	Key	Possible Cause
1	FAST REPEAT	U204-39, U183, U184, RP119
2	CTRL (UP = H)	RP119, U204-1
	CTRL (DOWN = L)	Ground return (P107-2)
3	BREAK	U204-34, U183, U184, RP119
4	RESET (UP = H)	R108
	RESET (DOWN = L)	Ground return (P107-2)
5	L. SHIFT (UP = L)	U204-39, U183, U184, RP119
	L. SHIFT (DOWN = H)	
6	CAPS LOCK (UP = L)	U204-39, U183, U184, RP119
	CAPS LOCK (DOWN = H)	
7	TAB	U204-33, U183, U184, RP119
8	R. SHIFT (UP = L)	U204-39, U183, U184, RP119
	R. SHIFT (DOWN = H)	
9	F2	U204-32, U199, RP119
10	4/\$	U204-31, U183, U184, RP126
11	T	U204-30, U199, RP126
12	F9	U204-29, U199, RP126
13	P	U204-29, U199, RP126
14	[U204-28, U183, U184, RP126
15	K	U204-27, U199, RP126
16	M	U204-28, U199, RP126
17	HOME	U204-34, U199, RP119
18	ENTER	U204-27, U199, RP126
19	+1.5 volts	R112, LED in RESET key
20	GROUND	R112, LED in RESET key

-- Turn off the computer.

-- Restore U185-11 to its original condition.

If you're still having keyboard problems, then check the monitor ROM, I/O port decoder, and bus lines between the CPU and U204.

I/O PORT DECODER TESTS

CHECK	IF NOT OKAY, CHECK
*U157-4 = H (MB2)	U157-1, U157-2, U157-3
*U157-5 = P (MB2)	U157-1, U157-2, U157-3
*U157-6 = P (MB2)	U157-1, U157-2, U157-3
*U157-9 = P (MB2)	U157-15, U157-4, U157-13
*U157-10 = P (MB2)	U157-15, U157-4, U157-13
*U157-11 = H (MB2)	U157-15, U157-4, U157-13
*U157-12 = P (MB2)	U157-15, U157-14, U157-13
*U159-7 = P (MB2)	U159-4, U159-1, U159-2, U159-3
*U159-9 = H (MB2)	U159-4, U159-1, U159-2, U159-3
*U159-10 = H (MB2)	U159-4, U159-1, U159-2, U159-3
*U159-11 = H (MB2)	U159-4, U159-1, U159-2, U159-3
*U159-12 = P (MB2)	U159-3
*U159-12 = P (MB2)	U159-4, U159-1, U159-2,
*U179-4 = P (MB2)	U179-13 and INPUT CHECKS

End of test.

INPUT CHECKS (MB2)	U179-1, U179-2, U179-2,
INPUT CHECKS (MB2)	U179-3, U179-4, U179-5,
INPUT CHECKS (MB2)	U179-6, U179-7, U179-15
U157-1 = P (MB2)	U179-11
U157-2 = P (MB2)	U181-16
U157-3 = P (MB2)	U181-14
U157-13 = P (MB2)	U181-12
U157-14 = P (MB2)	U181-14
U157-15 = P (MB2)	U179-10
U159-1 = P (MB2)	U181-18
U159-2 = P (MB2)	U181-16
U159-3 = P (MB2)	U181-14
U159-4 = P (MB2)	U179-12

U179-1 = P (MB2)	U181-7
U179-2 = P (MB2)	U181-5
U179-3 = P (MB2)	U181-3
U179-4 = P (MB2)	U181-12
U179-5 = P (MB2)	U181-18
U179-6 = P (MB2)	U181-16
U179-7 = P (MB2)	U181-14
U179-10 = P (MB2)	U179-13 and INPUT CHECKS
U179-11 = P (MB2)	U179-13 and INPUT CHECKS
U179-12 = P (MB2)	U179-13 and INPUT CHECKS
U179-13 = P (MB2)	See E-CLOCK LOGIC TESTS.
U179-15 = P (MB2)	U181-9
U181-2 = P (MB2)	See GENERAL CPU TESTS.
U181-3 = P (MB2)	U181-17
U181-4 = P (MB2)	See GENERAL CPU TESTS.
U181-5 = P (MB2)	U181-15
U181-6 = P (MB2)	See GENERAL CPU TESTS.
U181-7 = P (MB2)	U181-13
U181-8 = P (MB2)	See GENERAL CPU TESTS.
U181-9 = P (MB2)	U181-11
U181-11 = P (MB2)	See GENERAL CPU TESTS.
U181-12 = P (MB2)	U181-8
U181-13 = P (MB2)	See GENERAL CPU TESTS.
U181-14 = P (MB2)	U181-6
U181-15 = P (MB2)	See GENERAL CPU TESTS.
U181-16 = P (MB2)	U181-4
U181-17 = P (MB2)	See GENERAL CPU TESTS.
U181-18 = P (MB2)	U181-2

I/O PORT DECODER RESET TESTS

Press and release the CTRL/RESET keys as you make the following measurements. A logic state in parenthesis indicates that the line under test pulses one or more times when you release the CTRL/RESET keys.

CHECK	IF NOT OKAY, CHECK
*U157-4 = (H) (MB2)	See GENERAL CPU TESTS.
*U157-11 = (H) (MB2)	See GENERAL CPU TESTS.
*U159-9 = (H) (MB2)	See GENERAL CPU TESTS.
*U159-11 = (H) (MB2)	See GENERAL CPU TESTS.

MEMORY CONTROL LATCH TESTS

CHECK	IF NOT OKAY, CHECK
*U176-1 = H (MB2)	See RESET CIRCUITS TESTS.
*U176-9 = H (MB2)	U221-11

Perform the suggestions under "MEMCTL NOTES."

U214-3 = H (MB2)	U214-17
U214-17 = H (MB2)	See the BUS CONTROL OUTPUT CIRCUIT TESTS.
U221-11 = H (MB2)	U221-12, U221-13
U221-12 = H (MB2)	U214-3
U221-13 = H (MB2)	See the I/O PORT DECODER TESTS.

MEMCTL NOTES:

1. Check the data outputs and inputs of the memory control latch (U176 on MB2). Trace these back to U178 outputs and inputs. If U178's inputs are bad, check the S-100 bus and see GENERAL CPU TESTS.
2. Hold the CTRL/RESET keys down and take the following measurements. Pulses enclosed in parenthesis indicate that the line under test pulses at least once when you release the reset keys.

CHECK	IF NOT OKAY, CHECK
*U176-1 = L (MB2)	See RESET CIRCUITS TESTS.
*U176-9 = (H) (MB2)	U221-11

End of test.

U214-3 = (H) (MB2)	U214-17
U214-17 = (H) (MB2)	See the BUS CONTROL OUTPUT CIRCUITS TESTS.
U221-11 = (L) (MB2)	U221-12, U221-13
U221-12 = (H) (MB2)	U214-3
U221-13 = (H) (MB2)	See the I/O PORT DECODER TESTS.

MEMORY CIRCUIT TESTS

TEST #1

1. Lift pin 2 of U169.
2. Temporarily jumper U169-2 to U170-6 as you apply power to the H/Z-100. This ensures that the display is properly initialized.
3. Connect U169-2 to ground.
4. Perform the following checks. If you are instructed to go to another test (other than MEMORY CIRCUITS TEST #2), restore U169 to its normal condition.

CHECK	IF NOT OKAY, CHECK
*U110-14 = H (MB3)	U110-5
*U110-15 = H (MB3)	U110-5
*U110-16 = H (MB3)	U110-5
*U110-18 = H (MB3)	U110-4, U110-6
*U110-19 = H (MB3)	U110-4, U110-6
 *U169-1 = H (MB3)	U166-10
 *U170-4 = P (MB3)	U167-6
*U170-5 = P (MB3)	U130-3
*U170-6 = H (MB3)	U170-1

Go to MEMORY CIRCUITS TEST #2.

U110-4 = L (MB3)	U149 Defective
U110-5 = L (MB3)	U149 Defective
U110-6 = L (MB3)	U149 Defective
 U111-1 = L (MB3)	See MEMORY CONTROL LATCH TESTS.
U111-2 = P (MB3)	U163-16
U111-3 = P (MB3)	U163-18
U111-4 = P (MB3)	U162-9
U111-5 = P (MB3)	U162-3
U111-6 = P (MB3)	U162-5
U111-7 = P (MB3)	U162-7
U111-9 = P (MB3)	U111-1, U111-2, U111-3, U111-4, U111-5, U111-6, U111-7, U111-14, U111-15
U111-14 = P (MB3)	U173-14
U111-15 = L (MB3)	See MEMORY CONTROL LATCH TESTS.

U130-1	= P	(MB3)	U167-9
U130-2	= P	(MB3)	U214-7
U130-3	= P	(MB3)	U130-1, U130-2
U130-4	= P	(MB3)	See BUS CONTROL OUTPUT TESTS.
U130-6	= P	(MB3)	U130-4
U147-3	= P	(MB3)	U147 defective.
U148-1	= P	(MB3)	U147-3
U148-5	= H	(MB3)	U148-1, U148-15
U148-9	= H	(MB3)	U148-11, U148-13, U148-14
U148-11	= H	(MB3)	U148-5
U148-13	= P	(MB3)	U168-11
U148-14	= H	(MB3)	U173-16
U148-15	= H	(MB3)	U173-16
U151-1	= P	(MB3)	U195-7
U151-2	= H	(MB3)	U148-9
U151-12	= P	(MB3)	U151-1, U151-2, U151-13
U151-13	= P	(MB3)	U167-8
U152-1	= P	(MB3)	U168-11
U152-3	= P	(MB3)	U151-12
U152-6	= L	(MB3)	U152-1, U152-3, U152-15
U152-15	= H	(MB3)	U173-16
U154-3	= P	(MB3)	U195-12
U154-4	= P	(MB3)	U214-14
U154-6	= P	(MB3)	U154-4, U154-8, U154-10, U154-11
U154-8	= P	(MB3)	U214-9
U154-10	= P	(MB3)	U154-3, U154-12, U154-13, U111-9
U154-11	= P	(MB3)	U195-7
U154-12	= P	(MB3)	U195-7
U154-13	= P	(MB3)	U111-9
U162-3	= P	(MB2)	U162-17
U162-5	= P	(MB2)	U162-15
U162-7	= P	(MB2)	U162-13
U162-9	= P	(MB2)	U162-11
U162-11	= P	(MB2)	See GENERAL CPU TESTS.
U162-13	= P	(MB2)	See GENERAL CPU TESTS.
U162-15	= P	(MB2)	See GENERAL CPU TESTS.
U162-17	= P	(MB2)	See GENERAL CPU TESTS.

U163-2	= P	(MB2)	See GENERAL CPU TESTS.
U163-3	= L	(MB2)	U163-17
U163-4	= P	(MB2)	See GENERAL CPU TESTS.
U163-5	= L	(MB2)	U163-15
U163-6	= P	(MB2)	See GENERAL CPU TESTS.
U163-7	= L	(MB2)	U163-13
U163-8	= P	(MB2)	See GENERAL CPU TESTS.
U163-9	= L	(MB2)	U163-11
U163-11	= L	(MB2)	See GENERAL CPU TESTS.
U163-12	= P	(MB2)	U163-8
U163-13	= L	(MB2)	See GENERAL CPU TESTS.
U163-14	= P	(MB2)	U163-6
U163-15	= L	(MB2)	See GENERAL CPU TESTS.
U163-16	= P	(MB2)	U163-4
U163-17	= L	(MB2)	See GENERAL CPU TESTS.
U163-18	= P	(MB2)	U163-2
U166-10	= H	(MB3)	U166-11
U166-11	= L	(MB3)	U169-3
U167-1	= H	(MB3)	U173-15
U167-2	= P	(MB3)	U154-10
U167-3	= P	(MB3)	U130-6
U167-6	= P	(MB3)	U167-1, U167-2, U167-3
U167-8	= P	(MB3)	U167-11, U167-12, U167-13
U167-9	= P	(MB3)	U167-11, U167-12, U167-13
U167-11	= P	(MB3)	U130-6
U167-12	= P	(MB3)	U154-6
U167-13	= H	(MB3)	U173-15
U168-11	= P	(MB3)	U168-12
U168-12	= P	(MB3)	See CLOCK CIRCUITS TESTS.
U169-3	= L	(MB3)	If U169-3 = H, then replace U169. Otherwise, replace U149. Also check for open or shorted solder runs to U149.

U170-1 = L (MB3)	U152-6
U173-1 = P (MB3)	U163-14
U173-2 = P (MB3)	U163-12
U173-3 = L (MB3)	U163-3
U173-4 = L (MB3)	U163-5
U173-5 = L (MB3)	U163-7
U173-6 = L (MB3)	U163-9
U173-14 = P (MB3)	U173-1, U173-2, U173-3, U173-4, U173-5, U173-6
U173-15 = H (MB3)	U173-18
U173-16 = H (MB3)	U173-18
U173-18 = L (MB3)	U149 defective or open foil run.
U195-7 = P (MB2)	U195-13
U195-8 = P (MB2)	See STATUS CIRCUITS TESTS.
U195-12 = P (MB2)	U195-8
U195-13 = P (MB2)	See BUS CONTROL OUTPUT TESTS.
U214-6 = P (MB2)	See STATUS CIRCUITS TESTS.
U214-7 = P (MB2)	U214-13
U214-9 = P (MB2)	U214-11
U214-11 = P (MB2)	See STATUS CIRCUITS TESTS.
U214-13 = P (MB2)	See BUS CONTROL OUTPUT TESTS.
U214-14 = P (MB2)	U214-6

TEST #2

Remove the jumper wire between U169-2 and ground so that U169-2 is floating.

CHECK	IF NOT OKAY, CHECK
*U110-13 = P (MB3)	U110-4, U110-5, U110-7, U110-9
*U110-14 = P (MB3)	U110-5, U110-7, U110-9, U110-11
*U110-15 = P (MB3)	U110-5, U110-7, U110-9, U110-11
*U110-16 = P (MB3)	U110-5, U110-7, U110-9, U110-11
*U110-17 = P (MB3)	U110-1, U110-4, U110-6, U110-8
*U110-18 = P (MB3)	U110-2, U110-4, U110-6, U110-8
*U110-19 = P (MB3)	U110-3, U110-4, U110-6, U110-8
*U127-8 = P (MB3)	U127-1
*U133-1 = P (MB3)	U173-14
*U133-11 = P (MB3)	U110-12
*U150-1 = P (MB3)	U165-14
*U158-3 = P (MB3)	U158-1, U158-2
*U169-1 = P (MB3)	U169-1 & -3 should be the same logic states. If not, then replace U169. U166-10 & -11 should be opposite logic states. If not, then replace U166. U169-3 and U166-11 should be the same logic states. If not, then replace U149.

Restore U169 to its original condition. End of test.

U110-1 = P (MB3)	U111-10
U110-2 = P (MB3)	U111-11
U110-3 = P (MB3)	U111-12
U110-4 = P (MB3)	U149-12 defective.
U110-5 = P (MB3)	U149-4 defective.

U110-6 = P (MB3)	U169-3 defective.
U110-7 = P (MB3)	U150-9
U110-8 = P (MB3)	U152-5
U110-9 = P (MB3)	U214-9
U110-11 = P (MB3)	U194-6
U110-12 = P (MB3)	U110-4, U110-7
U111-10 = P (MB3)	U111 defective.
U111-11 = P (MB3)	U111 defective.
U111-12 = P (MB3)	U111 defective.
U127-1 = P (MB3)	U173-16
U148-5 = P (MB3)	U148-15
U148-9 = P (MB3)	U148-11, U148-13, U148-14
U148-11 = P (MB3)	U148-5
U148-13 = P (MB3)	U168-11
U148-14 = P (MB3)	U173-16
U148-15 = P (MB3)	U173-16
U150-3 = P (MB3)	U150-8
U150-5 = P (MB3)	U150-3
U150-8 = P (MB3)	U150-10, U150-11, U150-12
U150-9 = P (MB3)	U150-10, U150-11, U150-12
U150-10 = P (MB3)	U168-3
U150-11 = P (MB3)	Open foil run between U169-3 and U150-11.
U150-12 = P (MB3)	U152-6
U151-1 = P (MB3)	U195-7
U151-2 = P (MB3)	U148-9
U151-12 = P (MB3)	U151-1, U151-2, U151-13
U151-13 = P (MB3)	U167-8
U152-1 = P (MB3)	U168-11
U152-3 = P (MB3)	U151-12
U152-5 = P (MB3)	U152-1, U152-3, U152-15
U152-6 = P (MB3)	U152-1, U152-3, U152-15
U152-15 = P (MB3)	U173-16
U158-1 = P (MB3)	U150-5
U158-2 = P (MB3)	U169-6
U165-9 = P (MB3)	U168-11
U165-12 = P (MB3)	U150-5
U165-14 = P (MB3)	U165-9, U165-12
U166-12 = P (MB3)	U166-13
U166-13 = P (MB3)	U149 defective.

U167-8 = P (MB3)	U167-13
U167-13 = P (MB3)	U173-15
U168-1 = P (MB3)	U149 defective.
U168-2 = P (MB3)	U166-12
U168-3 = P (MB3)	U168-1, U168-2
U168-8 = P (MB3)	U168-9, U168-10
U168-9 = P (MB3)	U214-9
U168-10 = P (MB3)	U214-14
U168-11 = P (MB3)	U168-12
U168-12 = P (MB3)	See CLOCK CIRCUITS TESTS.
U169-4 = P (MB3)	U169-11
U169-5 = P (MB3)	U170-8
U169-6 = P (MB3)	U169-4, U169-5
U169-11 = P (MB3)	U169-12, U169-13
U169-12 = P (MB3)	U111-9 defective.
U169-13 = P (MB3)	U111-9 defective.
U170-8 = P (MB3)	U170-9, U170-10
U170-9 = P (MB3)	U214-5
U170-10 = P (MB3)	U168-8
U173-9 = P (MB3)	U149-12 defective.
U173-11 = P (MB3)	U195-16
U173-12 = P (MB3)	U169-6
U173-13 = P (MB3)	U194-6
U173-14 = P (MB3)	U173-11, U173-12, U173-13
U173-15 = P (MB3)	U173-9, U173-18, U173-19
U173-16 = P (MB3)	U173-9, U173-18, U173-19
U173-18 = P (MB3)	U149-4 defective.
U173-19 = P (MB3)	U150-9 defective.
U194-6 = P (MB2)	See GENERAL CPU TESTS.
U195-4 = P (MB2)	See BUS CONTROL OUTPUT TESTS.
U195-7 = P (MB2)	U195-13
U195-13 = P (MB2)	See BUS CONTROL OUTPUT TESTS.
U195-16 = P (MB2)	U195-4
U214-5 = P (MB2)	U214-15
U214-6 = P (MB2)	See STATUS CIRCUITS TESTS.
U214-9 = P (MB2)	U214-11
U214-11 = P (MB2)	See STATUS CIRCUITS TESTS.
U214-14 = P (MB2)	U214-6
U214-15 = P (MB2)	See STATUS CIRCUITS TESTS.

PARALLEL PORT TESTS

CHECK	IF NOT OKAY, CHECK
*U114-10 = H (MB4)	U116-16
*U114-11 = H (MB4)	U116-12
*U114-18 = L (MB4)	U134-2
*U114-19 = H (MB4)	U116-16
*U115-3 = H (MB4)	U115-17
*U115-5 = H (MB4)	U115-15
*U115-6 = H (MB4)	U115-4
*U115-7 = H (MB4)	U115-13
*U115-9 = H (MB4)	U115-11
*U115-12 = H (MB4)	U115-8
*U115-14 = H (MB4)	U115-6
*U115-18 = H (MB4)	U115-2
*U116-14 = H (MB4)	U116-6
*U116-18 = H (MB4)	U116-2
*U134-12 = P (MB4)	U134-13

End of test.

INPUT CHECKS (MB4)	U114-23, U114-36, U114-35,
INPUT CHECKS (MB4)	U114-25, U114-21, U114-34,
INPUT CHECKS (MB4)	U114-26 through U114-33.
U114-2 = Z (MB4)	See INPUT CHECKS.
U114-3 = Z (MB4)	See INPUT CHECKS.
U114-4 = H (MB4)	See INPUT CHECKS.
U114-5 = H (MB4)	See INPUT CHECKS.
U114-6 = P (MB4)	U116-5
U114-7 = P (MB4)	See INPUT CHECKS.
U114-12 = Z (MB4)	See INPUT CHECKS.
U114-13 = Z (MB4)	See INPUT CHECKS.
U114-14 = Z (MB4)	See INPUT CHECKS.
U114-15 = Z (MB4)	See INPUT CHECKS.
U114-16 = Z (MB4)	See INPUT CHECKS.
U114-17 = Z (MB4)	See INPUT CHECKS.
U114-21 = P (MB4)	U195-18
U114-23 = P (MB4)	See I/O PORT DECODER TESTS.
U114-25 = P (MB4)	See E-CLOCK LOGIC TESTS.

U114-26 through

U114-33 = P (MB4)

U136-1, U136-19, U135-1,
 U135-19 (NOTE: If these lines
 are okay, then check for
 shorts or opens on the bus;
 try replacing U136 and U135.)

See RESET CIRCUITS TESTS.

U114-34 = H (MB4)
 U114-35 = P (MB4)
 U114-36 = P (MB4)
 U114-38 = P (MB4)
 U114-39 = P (MB4)

U181-16
 U181-18
 U114-6, U114-39, INPUT CHECKS.
 U131-9

U115-2 = H (MB4)
 U115-4 = Z (MB4)
 U115-6 = Z (MB4)
 U115-8 = Z (MB4)
 U115-11 = Z (MB4)
 U115-13 = Z (MB4)
 U115-15 = Z (MB4)
 U115-17 = Z (MB4)

U114-4
 U114-2
 U114-3
 U114-12
 U114-13
 U114-14
 U114-15
 U114-16

U116-2 = Z (MB4)
 U116-4 = H (MB4)
 U116-5 = P (MB4)
 U116-6 = H (MB4)
 U116-8 = H (MB4)
 U116-12 = H (MB4)
 U116-15 = P (MB4)
 U116-16 = H (MB4)

U114-17
 RP103 or shorted foil run.
 U116-15
 U114-5
 RP103 or shorted foil run.
 U116-8
 See GENERAL CPU TESTS and
 VIDEO BOARD TROUBLESHOOTING.
 U116-4

U131-9 = P (MB4)
 U131-11 = P (MB4)
 U131-13 = P (MB4)

U131-11, U131-13
 U116-5
 U114-7

U134-1 = H (MB4)
 U134-2 = L (MB4)
 U134-13 = P (MB4)

RP103 or shorted foil run.
 U134-1
 U114-38

U135-1 = P (MB4)
 U135-19 = P (MB4)

U175-8
 U175-8

U136-1 = P (MB4)
 U136-19 = P (MB4)

U214-9
 U214-9

U175-3 = H (MB4)	See I/O PORT DECODER TESTS.
U175-4 = P (MB4)	See I/O PORT DECODER TESTS.
U175-5 = P (MB4)	See I/O PORT DECODER TESTS.
U175-6 = P (MB4)	U175-3, U175-4, U175-5
U175-8 = P (MB4)	U175-10, U175-11
U175-10 = P (MB4)	U214-12
U175-11 = P (MB4)	U175-6
U181-2 = P (MB2)	See GENERAL CPU TESTS.
U181-4 = P (MB2)	See GENERAL CPU TESTS.
U181-16 = P (MB2)	U181-4
U181-18 = P (MB2)	U181-2
U195-2 = P (MB2)	See STATUS CIRCUITS TESTS.
U195-18 = P (MB2)	U195-2
U214-8 = P (MB2)	See BUS CONTROL OUTPUT CIRCUITS TESTS.
U214-9 = P (MB2)	U214-11
U214-11 = P (MB2)	See STATUS CIRCUITS TESTS.
U214-12 = P (MB2)	U214-8

PROCESSOR SWAP TESTS

SWAP TEST #1

1. Lift pin 5 of U186 (MB1).
2. Jumper U186-5 to ground.
3. Apply power and perform the following steps:

CHECK	IF NOT OKAY, CHECK
*S100-21 = L (MB1)	U215-3
*U180-9 = L (MB1)	U180-10
*U186-3 = H (MB1)	U211-30
*U186-4 = L (MB1)	U171-5

Go to Swap Test #2

U171-1 = L (MB1)	U210-38
U171-5 = L (MB1)	U171-1
U180-10 = L (MB1)	U186-17
U186-3 = H (MB1)	U211-30
U186-4 = L (MB1)	U171-5
U186-16 = L (MB1)	U186-3
U186-17 = L (MB1)	U186-4
U186-18 = H (MB1)	U186 is defective.
U187-2 = H (MB1)	U186-18
U187-3 = P (MB1)	Restore U186-5 and go to CLOCK CIRCUITS TESTS.
U187-5 = H (MB1)	U187-2, U187-3
U187-9 = L (MB1)	U187-10, U187-11, U187-12
U187-10 = H (MB1)	U203-11
U187-11 = P (MB1)	Restore U186-5 and go to CLOCK CIRCUITS TESTS.
U187-12 = L (MB1)	U186-3
U203-11 = H (MB1)	U203-12, U203-13
U203-12 = L (MB1)	U186-16
U203-13 = H (MB1)	Restore U186-5 and go to CLOCK CIRCUITS TESTS.

U210-38 = L	(MB1)	U210-39
U210-39 = L	(MB1)	U187-9
U211-30 = H	(MB1)	U211-31
U211-31 = H	(MB1)	U187-5
U215-2 = L	(MB1)	Restore U186-5 and go to CLOCK CIRCUITS TESTS.
U215-3 = L	(MB1)	U215-2

SWAP TEST #2

1. Lift pins 4 and 5 of U186.
2. Jumper U186-4 and U186-5 to 5 volts.
3. Apply power and perform the following tests:

CHECK	IF NOT OKAY, CHECK
*S100-21 = H (MB1)	U215-3
*U171-5 = H (MB1)	U171-3, U171-2, U171-1
*U180-9 = L (MB1)	U180-10

)

Go to Swap Test #3.

U171-1 = H (MB1)	U210-38
U171-2 = H (MB1)	U210-38
U171-3 = P (MB1)	Restore U186-4 and U186-5 and go to CLOCK CIRCUITS TESTS.
U180-10 = L (MB1)	U186-17
U186-3 = L (MB1)	U211-30
U186-13 = H (MB1)	U186-3
U186-16 = H (MB1)	U186-3
U186-17 = L (MB1)	U186-3
U186-18 = L (MB1)	U186 is defective.

U187-2 = L (MB1)	U186-18
U187-3 = P (MB1)	Restore U186-4 and U186-5 and go to CLOCK CIRCUITS TESTS.
U187-4 = H (MB1)	U203-11
U187-5 = L (MB1)	U187-2, U187-3, U187-4
U187-9 = H (MB1)	U187-11, U187-12
U187-11 = P (MB1)	Restore U186-4 and U186-5 and go to CLOCK CIRCUITS TESTS.
U187-12 = H (MB1)	U186-13
U203-11 = H (MB1)	U203-13, U203-12
U203-12 = H (MB1)	U186-16
U203-13 = L (MB1)	Restore U186-4 and U186-5 and go to CLOCK CIRCUITS TESTS.
U210-38 = H (MB1)	U210-39
U210-39 = H (MB1)	U187-9
U211-30 = L (MB1)	U211-31
U211-31 = L (MB1)	U187-5
U215-2 = H (MB1)	Restore U186-4 and U186-5 and go to CLOCK CIRCUITS TESTS.
U215-3 = L (MB1)	U215-2

SWAP TEST #3

1. Restore pin 4 of U186; leave pin 5 lifted.
2. Jumper U186-5 to ground.
3. Turn on the H/Z-100.
4. Connect a jumper wire from ground to pin 74 of the S-100 bus (HOLD*).
5. Perform the following tests:

CHECK	IF NOT OKAY, CHECK
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*U180-9 = H (MB1)	U180-10
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Go to Swap Test #4.

U180-10 = H (MB1)	U186-17
U186-13 = H (MB1)	U186 is defective. [†]
U186-16 = H (MB1)	U186 is defective. [†]
U186-17 = H (MB1)	U186-13, U186-18

[†]NOTE: Before replacing U186, check the continuity between pins 6 and 15, and between pins 7 and 14. Also check for ground at pins 2, 8, 9, 10, 11, 12, and 19.

SWAP TEST #4

1. Remove the jumper between ground and pin 5.
2. Connect the jumper from pin 5 to +5 volts.

CHECK	IF NOT OKAY, CHECK
*U180-9 = H (MB1)	U180-10

End of tests.

U180-10 = H (MB1)	U180-17
U186-13 = H (MB1)	U186 is defective. [†]
U186-17 = H (MB1)	U186-13, U186-18
U186-18 = H (MB1)	U186 is defective. [†]

[†]NOTE: Before replacing U186, check the continuity between pins 6 and 15, and between pins 7 and 14. Also check for ground at pins 2, 8, 9, 10, 11, 12, and 19.

RESET CIRCUITS TESTS

CHECK	IF NOT OKAY, CHECK
*U177-5 = H (MB1)	U177-15
*U177-7 = H (MB1)	U177-13
*U177-11 = L (MB1)	U201-8, U201-13
*U201-3 = H (MB1)	U201-1, U201-2
*U201-6 = H (MB1)	U201-4, U201-5

Perform the RESET ACTIVE TESTS.

U177-9 = L (MB1)	U177-11
U177-11 = H (MB1)	U201-8, U201-13
U177-13 = L (MB1)	U177-9
U177-15 = L (MB1)	U177-9
U183-4 = H (MB4)	U183-6
U183-6 = L (MB4)	U183-10
U183-8 = H (MB4)	See KEYBOARD TESTS.
U183-9 = H (MB4)	See KEYBOARD TESTS.
U183-10 = L (MB4)	U183-8, U183-9
U185-3 = H (MB1)	U183-4
U185-4 = L (MB4)	U185-3
U185-5 = L (MB4)	U185-4
U185-6 = H (MB4)	U185-5
U201-1 = H (MB1)	U207-8
U201-2 = L (MB1)	Open circuit between U201-2 and ground.
U201-4 = L (MB1)	Open circuit between U201-4 and ground.
U201-5 = H (MB1)	U207-8
U201-8 = H (MB1)	U201-9, U201-10
U201-9 = L (MB1)	Open circuit between U201-9 and ground.
U201-10 = H (MB1)	U207-8
U201-13 = H (MB1)	U185-6
U207-8 = H (MB1)	U207-9
U207-9 = L (MB1)	U207-10
U207-10 = L (MB1)	U207-11
U207-11 = H (MB1)	R114, D101, or C189 defective.

RESET ACTIVE TESTS

Press and hold the CTRL/RESET keys as you make the following tests:

CHECK	IF NOT OKAY, CHECK
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*U177-5 = L (MB1)	U177-15
*U177-7 = L (MB1)	U177-13

End of tests.

U177-9 = H (MB1)	U177-11
U177-11 = L (MB1)	U201-11
U177-13 = H (MB1)	U177-9
U177-15 = H (MB1)	U177-9

U183-4 = L (MB4)	U183-6
U183-6 = H (MB4)	U183-10
U183-8 = L (MB4)	See KEYBOARD TESTS.
U183-9 = L (MB4)	See KEYBOARD TESTS.
U183-10 = H (MB4)	U183-8, U183-9

U185-3 = L (MB4)	U183-4
U185-4 = H (MB4)	U185-3
U185-5 = H (MB4)	U185-4
U185-6 = L (MB4)	U185-5

U201-11 = L (MB1)	U201-12, U201-13
U201-12 = L (MB1)	Open circuit between U201-12 and ground.
U201-13 = L (MB1)	U185-6

SERIAL PORT A TESTS

CHECK		IF NOT OKAY, CHECK
*U243-3 = H	(MB4)	U243 or U247 is defective.
*U243-14 = H	(MB4)	Perform INPUT CHECKS.
*U243-15 = H	(MB4)	Perform INPUT CHECKS.
*U243-16 = L	(MB4)	Shorting plugs at J109 and J111 incorrectly positioned or U247 defective.
*U243-17 = L	(MB4)	Shorting plugs at J109 and J111 incorrectly positioned or U247 defective.
*U243-18 = Z	(MB4)	Perform INPUT CHECKS.
*U243-20 = P	(MB4)	U240-8
*U243-22 = H	(MB4)	U243 or U246 is defective.
*U245-11 = -12V	(MB4)	U245-13, U228-3, U229-1
*U248-3 = -12V	(MB4)	U248-2
*U248-6 = -12V	(MB4)	U248-5, U228-3, U229-1
*U248-8 = P	(MB4)	U248-10
*U248-11 = P	(MB4)	U248-13

Perform SERIAL PORT A RESET CHECK.

INPUT CHECKS	(MB4)	U243-10, U243-21, U243-27,
INPUT CHECKS	(MB4)	U243-11, U243-13, U243-12,
INPUT CHECKS	(MB4)	U243-28, U243-1, U243-2,
INPUT CHECKS	(MB4)	U243-5, U243-6, U243-7, U243-8
U174-1 = P	(MB4)	See I/O PORT DECODER TESTS.
U174-2 = P	(MB4)	See E-CLOCK LOGIC TESTS.
U174-3 = H	(MB4)	U174-1, U174-2
U181-2 = P	(MB2)	See GENERAL CPU TESTS.
U181-4 = P	(MB2)	See GENERAL CPU TESTS.
U181-16 = P	(MB2)	U181-4
U181-18 = P	(MB2)	U181-2
U214-6 = P	(MB2)	See STATUS CIRCUITS TESTS.
U214-14 = P	(MB2)	U214-6
U228-1 = +16V	(MB4)	Check POWER SUPPLY MODULE.
U228-3 = +12V	(MB4)	U228-1
U229-1 = -12V	(MB4)	U229-2
U229-2 = -16V	(MB4)	Check POWER SUPPLY MODULE.

U240-8 = P	(MB4)	U240 OR C214 is bad.
U243-1 = P	(MB4)	See GENERAL CPU TESTS.
U243-2 = P	(MB4)	See GENERAL CPU TESTS.
U243-5 = P	(MB4)	See GENERAL CPU TESTS.
U243-6 = P	(MB4)	See GENERAL CPU TESTS.
U243-7 = P	(MB4)	See GENERAL CPU TESTS.
U243-8 = P	(MB4)	See GENERAL CPU TESTS.
U243-9 = P	(MB4)	Perform INPUT CHECKS.
U243-10 = P	(MB4)	U181-16
U243-11 = H	(MB4)	U174-3
U243-12 = P	(MB4)	U181-18
U243-13 = P	(MB4)	U214-14
U243-19 = H	(MB4)	Perform INPUT CHECKS.
U243-21 = L	(MB4)	See RESET CIRCUITS TESTS.
U243-23 = H	(MB4)	Perform INPUT CHECKS.
U243-24 = H	(MB4)	Perform INPUT CHECKS.
U243-25 = P	(MB4)	Perform INPUT CHECKS.
U243-27 = P	(MB4)	See GENERAL CPU TESTS.
U243-28 = P	(MB4)	See GENERAL CPU TESTS.
U245-13 = H	(MB4)	U243-19
U248-2 = H	(MB4)	U243-24
U248-5 = H	(MB4)	U243-23
U248-10 = P	(MB4)	U243-9, U243-25
U248-13 = P	(MB4)	U243-9, U243-25

SERIAL PORT A RESET TEST

Press and release the CTRL/RESET keys as you make the following measurements. A logic state in parenthesis indicates that the line under test pulses one or more times when you release the CTRL/reset keys.

CHECK		IF NOT OKAY, CHECK
*U243-9 = Z	(MB4)	U243-21
*U243-13 = (L)	(MB4)	U214-14

End of test.

U214-6 = (L)	(MB2)	See STATUS CIRCUITS TESTS.
U214-14 = (L)	(MB2)	U214-6
U243-21 = H	(MB4)	See RESET CIRCUITS TESTS.

SERIAL PORT B TESTS

CHECKS	IF NOT OKAY, CHECK
*U242-3 = H (MB4)	U242 or U230 is defective.
*U242-9 = L (MB4)	U242, D104, or U247 is defective.
*U242-14 = H (MB4)	Perform INPUT CHECKS.
*U242-15 = H (MB4)	Perform INPUT CHECKS.
*U242-16 = L (MB4)	U242 or U230 is defective.
*U242-17 = L (MB4)	U242 or U230 is defective.
*U242-18 = Z (MB4)	Perform INPUT CHECKS.
*U242-20 = P (MB4)	U240-8
*U242-22 = H (MB4)	U242 or U230 is defective.
*U242-25 = L (MB4)	U242, D103, or U247 is defective.
*U245-3 = -12V (MB4)	U245-2, U228-3, U229-1
*U245-6 = -12V (MB4)	U245-5, U228-3, U229-1
*U245-8 = -12V (MB4)	U245-10, U228-3, U229-1

Go to SERIAL PORT B RESET CHECK.

INPUT CHECKS (MB4)	U242-11, U242-13, U242-12,
INPUT CHECKS (MB4)	U242-10, U242-21, U242-27,
INPUT CHECKS (MB4)	U242-28, U242-1, U242-2,
INPUT CHECKS (MB4)	U242-5, U242-6, U242-7,
INPUT CHECKS (MB4)	U242-8
INPUT CHECKS (MB4)	(If these are okay, then replace U242.)
U174-4 = P (MB4)	See I/O PORT DECODER TESTS.
U174-5 = P (MB4)	See E-CLOCK LOGIC TESTS.
U174-6 = H (MB4)	U174-4, U174-5
U181-2 = P (MB2)	See GENERAL CPU TESTS.
U181-4 = P (MB2)	See GENERAL CPU TESTS.
U181-16 = P (MB2)	U181-4
U181-18 = P (MB2)	U181-2
U214-6 = P (MB2)	See STATUS CIRCUITS TESTS.
U214-14 = P (MB2)	U214-6
U228-1 = +16V (MB4)	Check Power Supply Module.
U228-3 = +12V (MB4)	U228-1

U229-1 = -12V (MB4)	U229-2
U229-2 = -16V (MB4)	Check Power Supply Module.
U240-8 = P (MB4)	U240 or C214 is defective.
U242-1 = P (MB4)	See GENERAL CPU TESTS.
U242-2 = P (MB4)	See GENERAL CPU TESTS.
U242-5 = P (MB4)	See GENERAL CPU TESTS.
U242-6 = P (MB4)	See GENERAL CPU TESTS.
U242-7 = P (MB4)	See GENERAL CPU TESTS.
U242-8 = P (MB4)	See GENERAL CPU TESTS.
U242-10 = P (MB4)	U181-16
U242-11 = H (MB4)	U174-6
U242-12 = P (MB4)	U181-18
U242-13 = P (MB4)	U214-14
U242-19 = H (MB4)	Perform INPUT CHECKS.
U242-21 = L (MB4)	See RESET CIRCUITS TESTS.
U242-23 = H (MB4)	Perform INPUT CHECKS.
U242-24 = H (MB4)	Perform INPUT CHECKS.
U242-27 = P (MB4)	See GENERAL CPU TESTS.
U242-28 = P (MB4)	See GENERAL CPU TESTS.
U245-2 = H (MB4)	U242-24
U245-5 = H (MB4)	U242-23
U245-10 = H (MB4)	U242-19

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SERIAL PORT B RESET TEST

Press and release the CTRL/RESET keys as you make the following measurements. A logic state in parenthesis indicates that the line under test pulses one or more times when you release the CTRL/RESET keys.

CHECK	IF NOT OKAY, CHECK
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*U242-13 = (L) (MB4)	U214-14
*U242-21 = H (MB4)	See RESET CIRCUITS TESTS.

End of test.

U214-6 = (L) (MB2)	See STATUS CIRCUITS TESTS.
U214-14 = (L) (MB2)	U214-6

STATUS CIRCUITS TESTS

CHECK	IF NOT OKAY, CHECK
*U226-9 = P (MB1)	See INPUT CHECKS
*U227-2 = P (MB1)	U227-1, U227-3, U227-11
*U227-5 = P (MB1)	U227-1, U227-4, U227-11
*U227-6 = P (MB1)	U227-1, U227-7, U227-11
*U227-9 = P (MB1)	U227-1, U227-8, U227-11
*U227-12 = L (MB1)	U227-1, U227-11, U227-13
*U227-15 = P (MB1)	U227-1, U227-11, U227-14
*U227-16 = P (MB1)	U227-1, U227-11, U227-17
*U227-19 = H (MB1)	U227-18

Tests complete.

INPUT CHECKS	U226-14, U226-13, U226-12,
INPUT CHECKS	U226-11, U226-10
U182-8 = L (MB1)	U182-9
U182-9 = H (MB1)	Problem on Pin 18 of S-100 BUS.
U220-10 = P (MB1)	U220-11
U220-11 = P (MB1)	U221-3
U221-1 = P (MB1)	See GENERAL CPU TESTS.
U221-2 = L (MB1)	U237-11
U221-3 = P (MB1)	U221-1, U221-2
U226-1 = P (MB1)	See INPUT CHECKS.
U226-2 = P (MB1)	See INPUT CHECKS.
U226-3 = L (MB1)	See INPUT CHECKS.
U226-4 = P (MB1)	See INPUT CHECKS.
U226-5 = P (MB1)	See INPUT CHECKS.
U226-6 = P (MB1)	See INPUT CHECKS.
U226-7 = P (MB1)	See INPUT CHECKS.
U226-10 = P (MB1)	See GENERAL CPU TESTS.
U226-11 = P (MB1)	See GENERAL CPU TESTS.
U226-12 = P (MB1)	See GENERAL CPU TESTS.
U226-13 = H (MB1)	See PROCESSOR SWAP TESTS.
U226-14 = P (MB1)	U233-5

U227-1 = L	(MB1)	U182-8
U227-3 = P	(MB1)	U226-6
U227-4 = P	(MB1)	U226-1
U227-8 = P	(MB1)	U226-7
U227-11 = P	(MB1)	U221-3
U227-13 = L	(MB1)	U226-3
U227-14 = P	(MB1)	U226-4
U227-17 = P	(MBA)	U226-5
U227-18 = H	(MB1)	R121 open or shorted foil to U227-18.
U233-1 = P	(MB1)	U220-10
U233-3 = P	(MB1)	See CLOCK CIRCUITS TESTS.
U233-5 = P	(MB1)	U233-1, U233-3
U237-11 = L	(MB1)	U237-12
U233-12 = L	(MB1)	See GENERAL CPU TESTS.

TIMER CIRCUITS TESTS

CHECK	IF NOT OKAY, CHECK
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*U160-10 = P	(MB4)	U160-9
*U160-17 = P	(MB4)	U160-18
*U175-12 = H	(MB4)	U175-1, U175-2

End of test.

U112-1 = H	(MB4)	U129-6
U112-8 = L	(MB4)	U112-13
U112-13 = H	(MB4)	U129-3
U113-1 = P	(MB4)	See I/O PORT DECODER TESTS.
U113-2 = P	(MB4)	U214-3
U113-3 = H	(MB4)	U113-1, U113-2
U113-4 = P	(MB4)	See I/O PORT DECODER TESTS.
U113-5 = P	(MB4)	U195-16
U113-6 = H	(MB4)	U113-4, U113-5

U129-1 = H	(MB4)	U113-3
U129-2 = P	(MB4)	U129-3. Also check U135, U136, and perform GENERAL CPU TESTS.
U129-3 = H	(MB4)	U129-1, U129-2
U129-4 = H	(MB4)	U113-3
U129-5 = P	(MB4)	U129-10. Also check U135, U136, and perform GENERAL CPU TESTS.
U129-6 = H	(MB4)	U129-4, U129-5
U129-10 = P	(MB4)	U113-6
U129-13 = H	(MB4)	U113-6
U160-9 = P	(MB4)	U192-11
U160-18 = P	(MB4)	U192-11
U175-1 = L	(MB4)	U112-8
U175-2 = L	(MB4)	U112-1
U192-2 = P	(MB1)	U191 or C115 is defective.
U192-11 = P	(MB1)	U192-2
U195-4 = P	(MB2)	See BUS CONTROL OUTPUT TESTS.
U195-16 = P	(MB2)	U195-4
U214-3 = P	(MB2)	U214-17
U214-17 = P	(MB2)	See BUS CONTROL OUTPUT TESTS.

H/Z-100 S-100 CONNECTOR PIN LOCATIONS

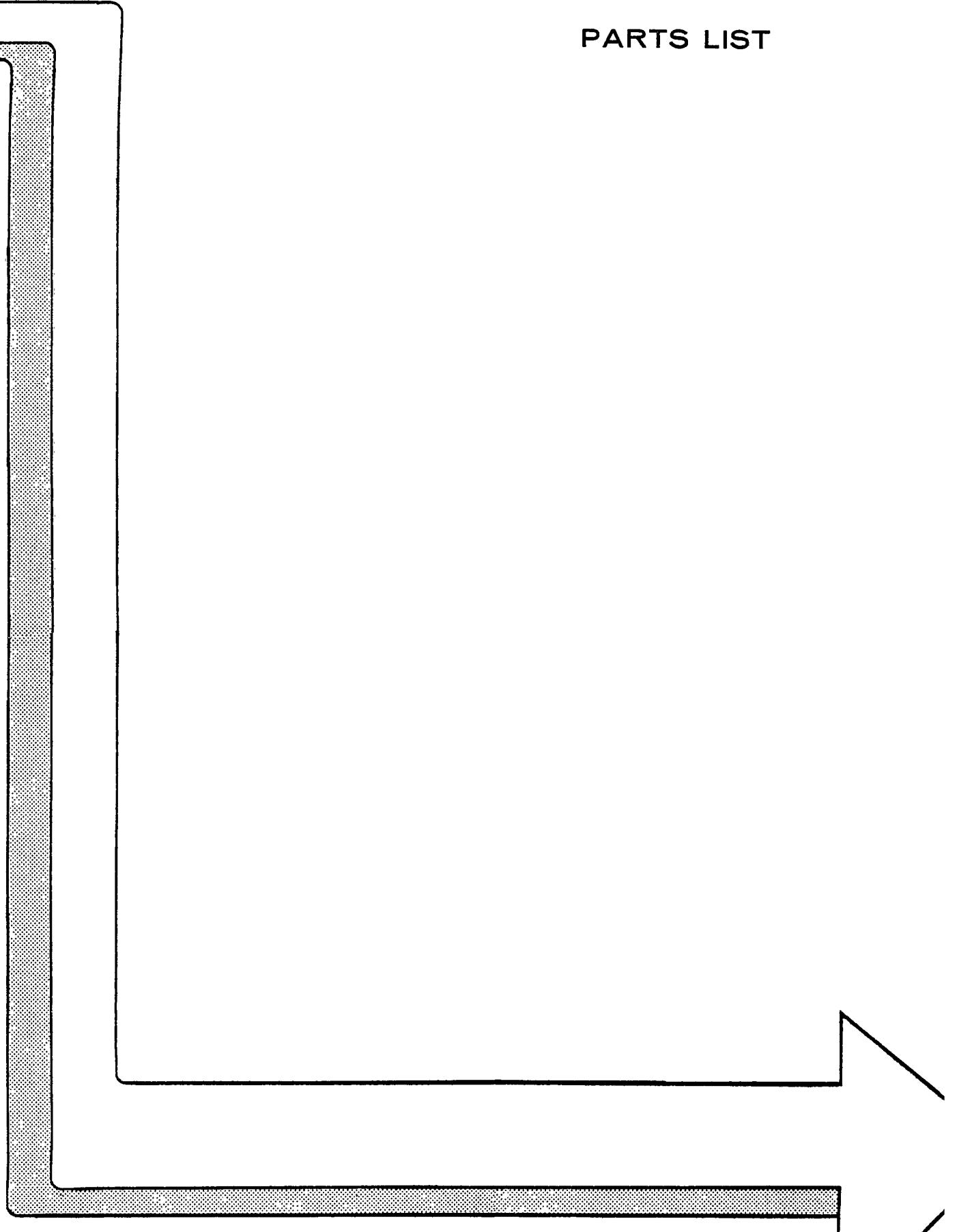
NOTES:

- PULSES TAKEN WITH LOGIC PROBE HP545A OR IT-7410.
- LOGIC STATES IN "RESET RELEASED" COLUMNS SHOULD BE PRESENT AFTER YOU PRESS AND RELEASE THE CTRL/RESET KEYS.
- LOGIC STATES IN "RESET PRESSED" COLUMNS SHOULD BE PRESENT WHEN YOU PRESS AND HOLD THE CTRL/RESET KEYS.
- LOGIC DEFINITIONS:
 - H = LOGIC ONE
 - L = LOGIC ZERO
 - P = PULSE
 - Z = HIGH IMPEDANCE STATE
 - H/L = MAY BE EITHER HIGH OR LOW--DEPENDS ON STATUS OF LATCH WHEN RESET IS PRESSED.
- LINES MARKED "330 Ω" and "4.7 kΩ" CONNECT TO PULL-UP RESISTOR PACKS.
- LINES MARKED "330/390 Ω" CONNECT TO TERMINATING RESISTOR PACKS.

◀ FRONT OF H/Z-100 COMPUTER

			RESET RELEASED	RESET PRESSED		RESET RELEASED	
		+8 VOLTS	-		1	51	
		+16 VOLTS	-		2	52	
XRDY	H	H	4.7 kΩ		3	53	L
VIO*	H	H	330 Ω		4	54	330 Ω
VII*	H	H	330 Ω		5	55	330 Ω
VI2*	H	H	330 Ω		6	56	330 Ω
VI3*	H	H	330 Ω		7	57	330 Ω
VI4*	H	H	330 Ω		8	58	4.7 kΩ
VI5*	H	H	330 Ω		9	59	4.7 kΩ
VI6*	H	H	330 Ω		10	60	330 Ω
VI7*	H	H	330 Ω		11	61	4.7 kΩ
NMI*	H	H	330 Ω		12	62	4.7 kΩ
PWRFAIL*	H	H	4.7 kΩ		13	63	4.7 kΩ
DMA3*	H	H	330 Ω		14	64	4.7 kΩ
A18	P	H/L	4.7 kΩ		15	65	Z
A16	P	H/L	4.7 kΩ		16	66	Z
A17	P	H/L	4.7 kΩ		17	67	330 Ω
SDSB*	H	H	330 Ω		18	68	330/390 Ω
CDSB*	H	H	330 Ω		19	69	Z
GND	L	L	-		20	70	L
NDEF (8088)	H	L	-		21	71	Z
ADSB*	H	H	330 Ω		22	72	330 Ω
DODSB*	H	H	330 Ω		23	73	330 Ω
Φ	P	P	330/390 Ω		24	74	330 Ω
pSTVAL	P	H	330/390 Ω		25	75	330 Ω
pHLDA	L	L	330/390 Ω		26	76	330/390 Ω
RFU	Z	Z	-		27	77	330/390 Ω
RFU	Z	Z	-		28	78	0 P
A5	P	H/L	4.7 kΩ		29	79	4.7 kΩ
A4	P	H/L	4.7 kΩ		30	80	4.7 kΩ
A3	P	H/L	4.7 kΩ		31	81	4.7 kΩ
A15	P	H/L	4.7 kΩ		32	82	4.7 kΩ
A12	P	H/L	4.7 kΩ		33	83	4.7 kΩ
A9	P	H/L	4.7 kΩ		34	84	4.7 kΩ
D01	P	H/L	4.7 kΩ		35	85	4.7 kΩ
D00	P	H/L	4.7 kΩ		36	86	4.7 kΩ
A10	P	H/L	4.7 kΩ		37	87	4.7 kΩ
D04	P	H/L	4.7 kΩ		38	88	4.7 kΩ
D05	P	H/L	4.7 kΩ		39	89	4.7 kΩ
D06	P	H/L	4.7 kΩ		40	90	4.7 kΩ
DI2	P	H	4.7 kΩ		41	91	4.7 kΩ
DI3	P	H	4.7 kΩ		42	92	4.7 kΩ
DI7	P	H	4.7 kΩ		43	93	4.7 kΩ
SM1	P	H/L	4.7 kΩ		44	94	4.7 kΩ
sOUT	P	L	4.7 kΩ		45	95	4.7 kΩ
sINP	P	H/L	4.7 kΩ		46	96	4.7 kΩ
sMEMR	P	H	4.7 kΩ		47	97	4.7 kΩ
sHLTA	L	L	4.7 kΩ		48	98	330 Ω
CLOCK	P	P	330/390 Ω		49	99	4.7 kΩ
GND	L	L	-		50	100	L

PARTS LIST



PARTS LISTS

CIRCUIT Comp. No.	DESCRIPTION Part No.	HEATH Part No.	CIRCUIT Comp. No.	DESCRIPTION Part No.	HEATH Part No.
MOTHER BOARD PART LIST (Assembled HE 181-3630-1)					
CAPACITORS			CAPACITORS (CONTINUED)		
C101 .1 uF ceramic	HE 21-762	HE 21-762	C180 10 uF electrolytic	HE 25-820	
C102 .1 uF ceramic	HE 21-762	HE 21-762	C181 .1 uF ceramic	HE 21-762	
C103 .1 uF ceramic	HE 21-762	HE 21-762	C182 .1 uF ceramic	HE 21-762	
C104 .1 uF ceramic	HE 21-762	HE 21-762	C183 .1 uF ceramic	HE 21-762	
C105 .1 uF ceramic	HE 21-762	HE 21-762	C184 .1 uF ceramic	HE 21-762	
C106 .1 uF ceramic	HE 21-762	HE 21-762	C185 .1 uF ceramic	HE 21-762	
C107 .1 uF ceramic	HE 21-762	HE 21-762	C186 .20 pF ceramic	HE 21-718	
C108 .1 uF ceramic	HE 21-762	HE 21-762	C187 .1 uF ceramic	HE 21-762	
C109 .1 uF ceramic	HE 21-762	HE 21-762	C188 .1 uF ceramic	HE 21-762	
C110 .1 uF ceramic	HE 21-762	HE 21-762	C189 100 uF electrolytic	HE 25-918	
C111 .1 uF ceramic	HE 21-762	HE 21-762	C190 .1 uF ceramic	HE 21-762	
C112 .1 uF ceramic	HE 21-762	HE 21-762	C191 .1 uF ceramic	HE 21-762	
C113 .1 uF ceramic	HE 21-762	HE 21-762	C192 .1 uF ceramic	HE 21-762	
C113-1 100 uF electrolytic	HE 25-918	HE 21-762	C193 .1 uF ceramic	HE 21-762	
C114 .1 uF ceramic	HE 21-762	HE 21-762	C194 .1 uF ceramic	HE 21-762	
C115 .1 uF ceramic	HE 21-762	HE 21-762	C195 .1 uF ceramic	HE 21-762	
C116 470 pF ceramic	HE 21-773	HE 21-773	C196 .1 uF ceramic	HE 21-762	
C117 470 pF ceramic	HE 21-773	HE 21-773	C197 .1 uF ceramic	HE 21-762	
C118 470 pF ceramic	HE 21-773	HE 21-773	C198 .47 uF electrolytic	HE 25-859	
C119 .1 uF ceramic	HE 21-762	HE 21-762	C199 .47 uF electrolytic	HE 25-859	
C120 470 pF ceramic	HE 21-773	HE 21-773	C200 .01 uF ceramic	HE 21-769	
C121 .1 uF ceramic	HE 21-762	HE 21-762	C201 .01 uF ceramic	HE 21-762	
C122 .1 uF ceramic	HE 21-762	HE 21-762	C202 .01 uF ceramic	HE 21-769	
C123 .1 uF ceramic	HE 21-762	HE 21-762	C203 .1 uF ceramic	HE 21-762	
C124 .1 uF ceramic	HE 21-762	HE 21-762	C204 .330 pF ceramic	HE 21-763	
C125 .1 uF ceramic	HE 21-762	HE 21-762	C205 .330 pF ceramic	HE 21-763	
C126 .1 uF ceramic	HE 21-762	HE 21-762	C206 .330 pF ceramic	HE 21-763	
C127 .1 uF ceramic	HE 21-762	HE 21-762	C207 .1 uF ceramic	HE 21-762	
C128 .1 uF ceramic	HE 21-762	HE 21-762	C208 .2.2 uF electrolytic	HE 25-924	
C129 .1 uF ceramic	HE 21-762	HE 21-762	C209 .1 uF ceramic	HE 21-762	
C130 .1 uF ceramic	HE 21-762	HE 21-762	C210 .001 uF polystyrene	HE 29-44	
C131 .1 uF ceramic	HE 21-762	HE 21-762	C211 .1 uF ceramic	HE 21-762	
C132 .1 uF ceramic	HE 21-762	HE 21-762	C212 .1 uF ceramic	HE 21-762	
C133 .1 uF ceramic	HE 21-762	HE 21-762	C213 10 uF electrolytic	HE 25-820	
C134 470 pF ceramic	HE 21-773	HE 21-773	C214 .1 uF ceramic	HE 21-762	
C135 470 pF ceramic	HE 21-773	HE 21-773	C215 .1 uF ceramic	HE 21-762	
C136 470 pF ceramic	HE 21-773	HE 21-773	C216 .1 uF ceramic	HE 21-762	
C137 470 pF ceramic	HE 21-773	HE 21-773	C217 .1 uF ceramic	HE 21-762	
C138 470 pF ceramic	HE 21-773	HE 21-773	C218 .1 uF ceramic	HE 21-762	
C139 .1 uF ceramic	HE 21-762	HE 21-762	C219 .1 uF ceramic	HE 21-762	

CAPACITORS (CONTINUED)					
C140 .1 uF ceramic	HE 21-762	HE 21-762	C180 10 uF electrolytic	HE 25-820	
C141 .1 uF ceramic	HE 21-762	HE 21-762	C181 .1 uF ceramic	HE 21-762	
C142 .1 uF ceramic	HE 21-762	HE 21-762	C182 .1 uF ceramic	HE 21-762	
C143 .1 uF ceramic	HE 21-762	HE 21-762	C183 .1 uF ceramic	HE 21-762	
C144 .1 uF ceramic	HE 21-762	HE 21-762	C184 .1 uF ceramic	HE 21-762	
C145 .1 uF ceramic	HE 21-762	HE 21-762	C185 .1 uF ceramic	HE 21-762	
C146 .1 uF ceramic	HE 21-762	HE 21-762	C186 .20 pF ceramic	HE 21-718	
C147 .1 uF ceramic	HE 21-762	HE 21-762	C187 .1 uF ceramic	HE 21-762	
C148 .1 uF ceramic	HE 21-762	HE 21-762	C188 .1 uF ceramic	HE 21-762	
C149 .1 uF ceramic	HE 21-762	HE 21-762	C189 100 uF electrolytic	HE 25-918	
C150 .1 uF ceramic	HE 21-762	HE 21-762	C190 .1 uF ceramic	HE 21-762	
C151 .1 uF ceramic	HE 21-762	HE 21-762	C191 .1 uF ceramic	HE 21-762	
C152 .1 uF ceramic	HE 21-762	HE 21-762	C192 .1 uF ceramic	HE 21-762	
C153 .1 uF ceramic	HE 21-762	HE 21-762	C193 .1 uF ceramic	HE 21-762	
C154 .1 uF ceramic	HE 21-762	HE 21-762	C194 .1 uF ceramic	HE 21-762	
C155 .1 uF ceramic	HE 21-762	HE 21-762	C195 .1 uF ceramic	HE 21-762	
C156 .1 uF ceramic	HE 21-762	HE 21-762	C196 .1 uF ceramic	HE 21-762	
C157 .1 uF ceramic	HE 21-762	HE 21-762	C197 .1 uF ceramic	HE 21-762	
C158 .1 uF ceramic	HE 21-762	HE 21-762	C198 .47 uF electrolytic	HE 25-859	
C159 .1 uF ceramic	HE 21-762	HE 21-762	C199 .47 uF electrolytic	HE 25-859	
C160 .1 uF ceramic	HE 21-762	HE 21-762	C200 .01 uF ceramic	HE 21-769	
C161 .1 uF ceramic	HE 21-762	HE 21-762	C201 .01 uF ceramic	HE 21-762	
C162 .1 uF ceramic	HE 21-762	HE 21-762	C202 .01 uF ceramic	HE 21-769	
C163 .1 uF ceramic	HE 21-762	HE 21-762	C203 .1 uF ceramic	HE 21-762	
C164 .001 uF polystyrene	HE 29-44	HE 29-44	C204 .330 pF ceramic	HE 21-763	
C165 .1 uF ceramic	HE 21-762	HE 21-762	C205 .330 pF ceramic	HE 21-763	
C166 .1 uF ceramic	HE 21-762	HE 21-762	C206 .330 pF ceramic	HE 21-763	
C167 .1 uF ceramic	HE 21-762	HE 21-762	C207 .1 uF ceramic	HE 21-762	
C168 .1 uF ceramic	HE 21-762	HE 21-762	C208 .2.2 uF electrolytic	HE 25-924	
C169 .1 uF ceramic	HE 21-762	HE 21-762	C209 .1 uF ceramic	HE 21-762	
C170 .1 uF ceramic	HE 21-762	HE 21-762	C210 .001 uF polystyrene	HE 29-44	
C171 .1 uF ceramic	HE 21-762	HE 21-762	C211 .1 uF ceramic	HE 21-762	
C172 .1 uF ceramic	HE 21-762	HE 21-762	C212 .1 uF ceramic	HE 21-762	
C173 .1 uF ceramic	HE 21-762	HE 21-762	C213 10 uF electrolytic	HE 25-820	
C174 .2.2 uF electrolytic	HE 25-924	HE 25-924	C214 .1 uF ceramic	HE 21-762	
C174-1 100 uF electrolytic	HE 25-918	HE 25-918	C215 .1 uF ceramic	HE 21-762	
C175 .1 uF ceramic	HE 21-762	HE 21-762	C216 .1 uF ceramic	HE 21-762	
C176 .1 uF ceramic	HE 21-773	HE 21-773	C217 .1 uF ceramic	HE 21-762	
C177 .1 uF ceramic	HE 21-773	HE 21-773	C218 .1 uF ceramic	HE 21-762	
C178 none	HE 21-773	HE 21-773	C219 .1 uF ceramic	HE 21-762	
C179 none	HE 21-762	HE 21-762	C220 .1 uF ceramic	HE 21-762	
C221 .1 uF ceramic	HE 21-762	HE 21-762	C222 .330 pF ceramic	HE 21-762	
C223 .330 pF ceramic	HE 21-763	HE 21-763	C224 .330 pF ceramic	HE 21-763	
C225 .330 pF ceramic	HE 21-763	HE 21-763	C226 .330 pF ceramic	HE 21-763	

PARTS LIST

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CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
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CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
----------------------	-------------	-------------------

INDUCTORS

L101	35 uH	HE 235-229
L102	35 uH	HE 235-229
L103	35 uH	HE 235-229
L104	35 uH	HE 235-229

RESISTORS (CONTINUED)

COMP.	DESCRIPTION	HEATH Part No.	CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
INTEGRATED CIRCUITS (CONTINUED)					
R101	4700 ohm	HE 4-472-12	RP110	330 ohm	U123 MCM6665
R102	4700 ohm	HE 4-472-12	RP111	4.7 kilohm	U124 MCH6665
R103	4700 ohm	HE 4-472-12	RP112	330 ohm	U125 MCM6665
R104	1000 ohm	HE 6-102-12	RP113	4.7 kilohm	U126 74LS244
R105	6650 ohm	HE 6-6651-12	RP114	4.7 kilohm	U127 74LS393
R106	6810 ohm	HE 6-6611-12	RP115	330 ohm	U128 74LS257A
R107	10 kilohm	HE 6-103-12	RP116	330/390 ohm	U129 74LS125
R108	10 kilohm	HE 6-103-12	RP117	4.7 kilohm	HE 4-43-971
R109	1000 ohm	HE 6-102-12	RP118	4.7 kilohm	HE 4-43-973
R110	1000 ohm	HE 6-102-12	RP119	10 kilohm	HE 4-43-974
R111	1000 ohm	HE 6-102-12	RP120	10 kilohm	HE 4-43-975
R112	470 ohm	HE 6-471-12	RP121	10 kilohm	HE 4-43-976
R113	10 kilohm	HE 6-103-12	RP122	10 kilohm	HE 4-43-977
R114	10 kilohm	HE 6-103-12	RP123	4.7 kilohm	HE 4-43-978
R115	4700 ohm	HE 6-472-12	RP124	4.7 kilohm	HE 4-43-979
R116	150 kilohm	HE 6-154-12	RP125	4.7 kilohm	HE 4-43-970
R117	1000 ohm	HE 6-102-12	RP126	10 kilohm	HE 4-43-971
R118	470 kilohm	HE 6-474-12	RP127	10 kilohm	HE 4-43-972
R119	470 kilohm	HE 6-474-12	RP128	10 kilohm	HE 4-43-973
R120	220 kilohm	HE 6-224-12	RP129	4.7 kilohm	HE 4-43-974
R121	1000 ohm	HE 6-102-12	RP130	4.7 kilohm	HE 4-43-975
R122	22 ohm	HE 6-220-12	INTEGRATED CIRCUITS		
R123	510 ohm	HE 6-511-12	U101	MCM6665	U140 MCM6665
R124	510 ohm	HE 6-511-12	U102	MCH6665	U141 MCH6665
R125	10 kilohm	HE 6-103-12	U103	MCH6665	U142 MCH6665
R126	10 kilohm	HE 6-103-12	U104	MCH6665	U143 MCH6665
R127	1000 ohm	HE 6-102-12	U105	MCH6665	U144 MCH6665
R128	4700 ohm	HE 6-472-12	U106	MCH6665	U145 MCH6665
RESISTOR PACKS			U107	74LS244	U146 74LS244
RP101	33 ohm	HE 9-93	U108	74LS244	U147 555 timer
RP102	390 ohm	HE 9-131	U109	74LS244	U148 74LS112
RP103	4.7 kilohm	HE 9-124	U110	74LS244	U149 200 ns Delay Line
RP104	4.7 kilohm	HE 9-124	U111	82S129 PROM	HE 4-43-1037
RP105	33 ohm	HE 9-93	U112	74ALS74	HE 4-43-1038
RP106	4.7 kilohm	HE 9-133	U113	74LS32	HE 4-43-1039
RP107	4.7 kilohm	HE 9-124	U114	74LS32	HE 4-43-1040
RP108	4.7 kilohm	HE 9-124	U115	74LS38	HE 4-43-1041
RP109	4.7 kilohm	HE 9-124	U116	74LS138	HE 4-43-1042
HEATH Part No.			U117	74LS138	HE 4-43-1043
HEATH Part No.			U118	74LS32	HE 4-43-1044
HEATH Part No.			U119	74LS32	HE 4-43-1045
HEATH Part No.			U120	MCH6665	U160 HAL16L8
HEATH Part No.			U121	MCH6665	U161 MCH6665
HEATH Part No.			U122	MCH6665	U162 MCH6665
HEATH Part No.			U123	8253-5	U163 HAL16L2
HEATH Part No.			U124	8253-5	U164 74LS244
HEATH Part No.			U125	8253-5	U165 74LS244
HEATH Part No.			U126	8253-5	U166 74LS244
HEATH Part No.			U127	8253-5	U167 74LS244
HEATH Part No.			U128	8253-5	U168 74LS244
HEATH Part No.			U129	8253-5	U169 74LS244

HE 4-43-976

HE 4-43-977

HE 4-43-978

HE 4-43-979

HE 4-43-980

HE 4-43-981

HE 4-43-982

HE 4-43-983

HE 4-43-984

HE 4-43-985

HE 4-43-986

HE 4-43-987

HE 4-43-988

HE 4-43-989

HE 4-43-990

HE 4-43-991

HE 4-43-992

HE 4-43-993

HE 4-43-994

HE 4-43-995

HE 4-43-996

HE 4-43-997

HE 4-43-998

HE 4-43-999

HE 4-43-1000

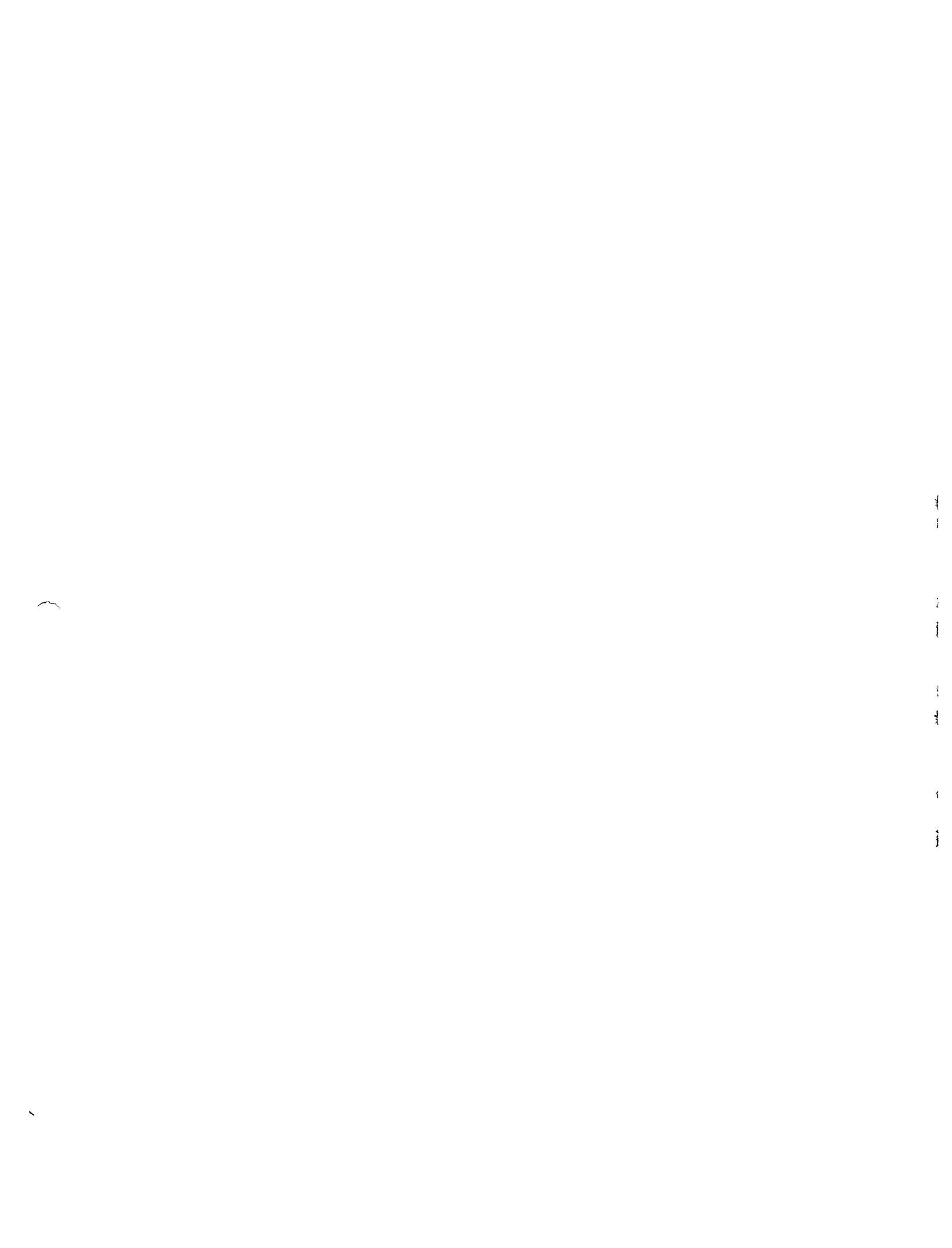
INTEGRATED CIRCUITS (CONTINUED)

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
CRYSTALS		
Y101	10,000 MHz crystal	HE 404-645
Y102	6,000 MHz crystal	HE 404-647
Y103	15,000 MHz crystal	HE 404-644
CONNECTORS - SOCKETS		
	8-pin IC socket	HE 434-230
	14-pin IC socket	HE 434-298
	16-pin IC socket	HE 434-299
	18-pin IC socket	HE 434-310
	20-pin IC socket	HE 434-311
	24-pin IC socket	HE 431-307
	28-pin IC socket	HE 431-310
	40-pin IC socket	HE 431-253
	2-pin connector	HE 432-1171
	3-pin connector	HE 432-1102
	4-pin right-angle connector	HE 431-363
	9-pin right-angle molex connector	HE 432-1202
	10-pin connector	HE 432-903
	20-pin connector	HE 432-1227
	25-pin F right-angle "D" connector	HE 432-1195
	25-pin M right-angle "D" connector	HE 432-1194
	40-pin connector	HE 432-1062
	Jumper	HE 432-1041
	S-100 board edge connector	HE 432-1193
HARDWARE		
	#4 lockwasher	HE 251-9
	#4 nut	HE 252-15
	4-40 x 5/16" hex "D" spacer	HE 255-757
	4-40 x 5/16" black phillips-head screw	HE 250-169
MISCELLANEOUS		
D101	PC board	HE 85-2653
D102	Wire, bare	HE 340-8
D103	Wire, blue wirewrap	HE 344-189
D104	IN5817 diode	HE 57-507
SW101	1N4149 diode	HE 56-56
X101	1N4149 diode	HE 56-56
	1N4149 diode	HE 60-621
	8-section slide switch	HE 473-29
	Audio transducer	HE 473-29

CIRCUIT BOARD X-RAY VIEWS

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MOTHERBOARD, Jumper and Foil Cuts	3-168





MOTHERBOARD CUTS AND JUMPERS

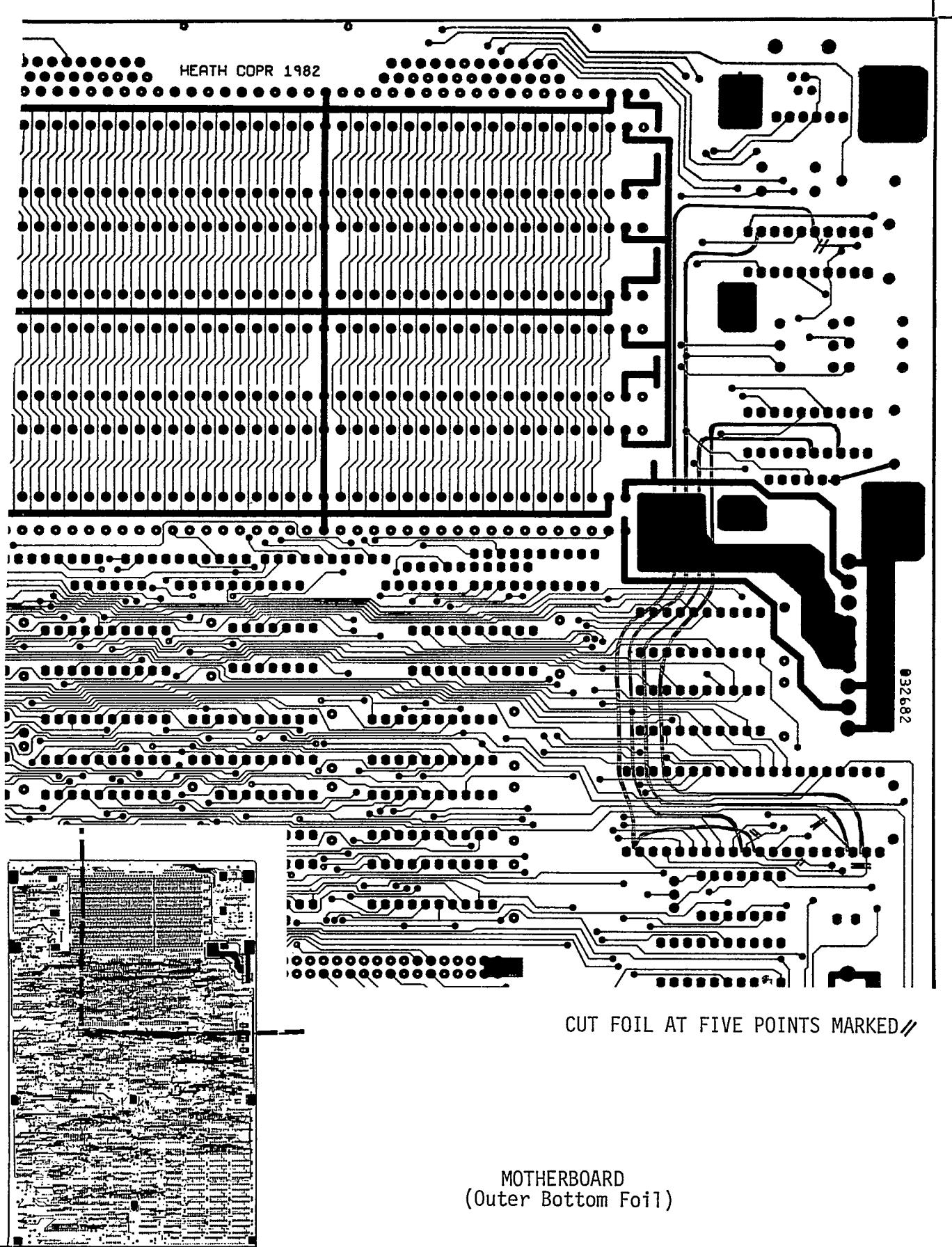
The pictorial on the facing page shows a section of the foil side of the motherboard. The red slashes (//) are cuts in existing foil runs. The lines in red are jumper wires. The schematics in this manual reflect these changes. Use this pictorial in conjunction with the other X-Ray Views. A summary of the cuts and jumpers follows:

Cuts: (all cuts on foil side of PCB)

1. Trace from U114 pin 2.
2. Trace from U114 pin 3.
3. Trace from U114 pin 10.
4. Trace from U114 pin 11.
5. Trace from U116 pin 16.

Jumpers:

1. Jumper from U116 pin 16 to U114 pin 19.
2. Jumper from U114 pin 19 to U114 pin 10.
3. Jumper from U114 pin 11 to U116 pin 12.
4. Jumper from U114 pin 2 to U115 pin 4.
5. Jumper from U114 pin 3 to U115 pin 6.
6. Jumper from RP103 pin 1 to +5V end of C115.





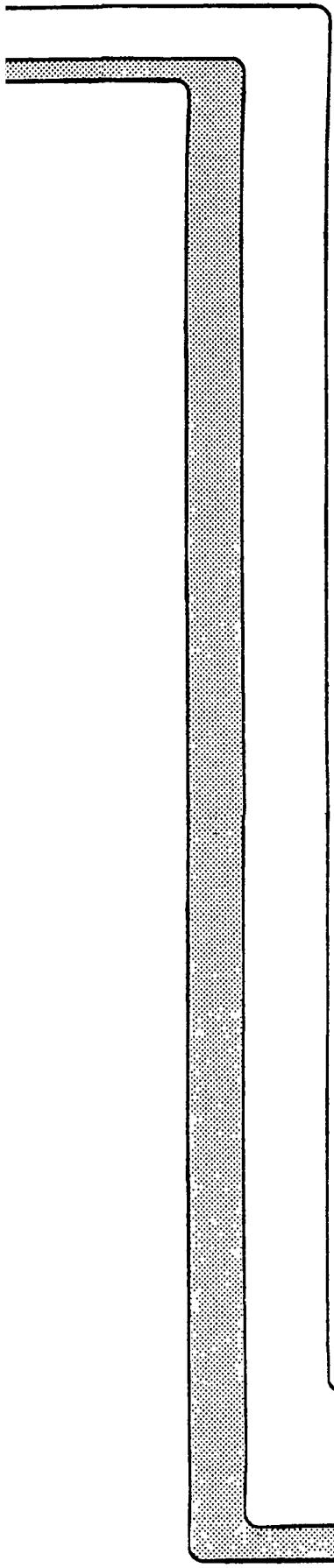
VIDEO BOARD

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5



INTRODUCTION



The color video board functions as a interface between the CPU and the video monitor. The video board receives data from the CPU and translates it into a meaningful display on a video monitor. The H/Z-100 video board features eight color capability, high-resolution graphics and S-100 bus signal compatibility.

The video board uses three banks of memory called memory planes. Each plane may contain up to 64K of RAM. A minimally configured video board will have one plane of memory and support a monochrome display. When the color option is installed, the video board contains three planes of memory. This enables the video board to produce an 8-color or an 8-level gray scale display. The type of display produced depends on the type of monitor used. When a color monitor is used, the 8 pixel colors may be mixed to produce more colors. When a monochrome display is used, pixel mixing produces more shades of gray.

To produce high-resolution graphics, the video board supports a resolution of 640 x 225 pixels. This can be visualized as 25 lines of 80 characters. A character is defined within an 8 x 9 pixel matrix. This matrix enables the H/Z-100 to display, in addition to high-resolution graphics, full width/height alphanumeric characters as currently defined by the H-19. By using this definition of character width and height, the H/Z-100 can use existing software that requires full width/height characters.

Although it is not an S-100 card, the video board is signal compatible with the S-100 bus. This allows the user to access the video board through slave processors located in the S-100 card cage. This compatibility gives the video board an added amount of flexibility.

In this section of the H/Z-100 Service Data Manual, the information supplied will familiarize you with the video board and will help you to efficiently troubleshoot it.

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OVERVIEW

The video board uses a bit-mapped technique to generate a 640 x 250 pixel display. A pixel equals one bit in each character location. A character is 8 pixels wide and 10 pixels high. In normal operation, there are 80 characters across the screen and 25 rows of characters.

There are three colors available to the H/Z-100. Each color -- red, green, and blue -- requires a 32K x 8 bank of memory. These memory banks are located 64K apart near the top end of the 1 megabyte address space: Blue starts at C0000H, red starts at D0000H, and green starts at E0000H. Sixty-four kilobyte RAM can be used at these locations; however, the system software only supports 32K. A minimum system, for monochrome, uses the green memory bank.

Unless programmed otherwise, the H/Z-100 emulates the H-19 Video Terminal. This includes most escape sequences. In addition, if you want to write high-density graphics routines, you can by directly addressing the above memory location.

The video board uses many of the S-100 lines; however, it also uses some special control lines to provide more efficient operation. For this reason, it uses non-S-100 connectors at P304 and P305.

VIDEO PROCESSING CIRCUITS

CATHODE-RAY TUBE CONTROLLER

The CRTC, U330 on schematic VB1, fetches the characters to be displayed and provides horizontal and vertical timing. It also keeps track of the affected character if the light-pen circuits are used.

Briefly, here's what each line does. See the 6845 IC data sheet for more information.

POC Power-on clear, from the S-100 bus, sets all registers to their initial conditions on power-up or reset.

6845CS Chip-selects the CRTC for accessing the internal registers.

ECLK Latches the data into or out from the registers on its trailing edge.

BA0 Helps select a specific register inside the CRTC.

OUT When low, writes data into the selected register. Otherwise, reads data from it.

DIO0-DI07 Data bus used by the CPU to access the CRTC registers.

CLK Provides character-clock timing to the CRTC.

HSYNC Horizontal sync pulse.

VSYNC Vertical sync pulse.

CURSOR Provides an indication where the next character will be printed.

DISEN Disables the display during horizontal and vertical retrace.

MA0-MA11 Memory address lines. Point to the current character line, and the character in that line.

RA0-RA3 Row address lines. Points to the current scan line in the current character line.

WRITING TO A CRTC REGISTER

To select a specific CRTC register (R0-R17), the CPU must first program the address register (AR). For example, to write to R12, the CPU outputs 0CH to port ODCH. This places the number 12 into AR. The CPU then outputs the data it wants to write to port ODDH, which is loaded into register 12. Here's how it happens.

The CPU outputs the number 12 (0CH) to port ODCH. This is coupled through U338 to the data lines of the CRTC. At this time, 6845CS at VIOSEL (U369) asserts the chip-select line at pin 25 of the CRTC. Since the port address is ODCH, line BA0 = 0; thus accessing the AR.

When ECLK goes low, the data (0CH) on the bus lines is loaded into the address register. AR now points to register 12.

The CPU now outputs the byte it wants to write into port ODDH; line 6845CS is again asserted. Since the port address is ODDH, line BA0 = 1, telling the CRTC to route the data to the register pointed to by AR. When ECLK goes low, this data is loaded into register 12.

READING DATA FROM THE CRTC

The procedure is the same as writing data, except that U331 is selected instead of U338. This is done by DBIN from the S-100 bus and by 4521CS from U366-14.

HOW THE CRTC ADDRESSES RAM

As mentioned before, the CRTC is normally programmed to emulate the H19 video terminal. That is, the display will contain 25 lines, 80 characters per line, and 10 scan lines (rows) per character line.

MA0-MA11 points to the character location within a character line and also points to the current character line. It does this by incrementing its base address by ten after every ten scan lines. RA0-RA3 counts the number of scan lines. After one scan line is complete (MA0-MA11 counts to 79), RA0-RA3 resets to 0 and MA0-MA11 resets to its base address. The count begins again. This procedure continues until 10 scan lines are processed. RA0-RA3 again returns to zero, but MA0-MA11 increments its base address by ten to point to the next character line.

For each address, a byte is read from video RAM (VRAM) and shifted serially out to the video amplifier with the horizontal and vertical sync pulses. The scan rate is such that each address row appears beneath the previous one so that the serial dots form characters on the screen. Once the last character row is processed, both RA0-RA3 and MA0-MA11 reset to zero, vertical retrace takes place, and the process repeats.

Incidentally, at vertical retrace a sync pulse is sent through U366 (lower left on the schematic) to interrupt the CPU. This permits the CPU to access the CRTC registers (for example, to scroll the display) without interfering with the display.

The address lines reach memory by passing through a set of multiplexers. RA0-RA3 connects to multiplexer U357 while MA0-MA11 connects to U363, U358, and U359. These ICs allow coupling the CRTC address lines to VRAM, or the CPU address lines to VRAM.

0	16	32	1264
1	17	33	1265
2	18	34	1266
3	19	35	1267
4	20	36	1268
5	21	37	1269
6	22	38	1270
7	23	39	1271
8	24	40	1272
9	25	41	1273
1280	1296	2544
1281	1297	2545
1282	1298	2546
1289	1305	2553
2560	3824
30720	30736	31984
30729	30745	31993

Relative Memory Location for Each Scanned Character
(80 characters per line; 10 scan lines per character
line, 25 character lines)

When line VIDRAMSEL is low, the multiplexers pass the CRTC address bus to the VRAM address bus. RA0-RA11 is the lower 4 bits, DAO-DA3; and MA0-MA11 are bits DA4-DA15. This causes the address line to increment by 16 for every scanned character. See the table on the previous page. This shows the on-screen character location and its relative address (decimal).

Lines DAO-DA15 connect to address multiplexer U360 and U373. This circuit splits the address for RAS and CAS timing. RAS timing occurs when ADMUX is high, coupling the following lines to the outputs:

VA7	VA6	VA5	VA4	VA3	VA2	VA1	VA0
---	---	---	---	---	---	---	---
DA9	DA8	DA7	DA6	DA5	DA4	DA1	DA2

CAS timing occurs when ADMUX goes low, causing:

VA7	VA6	VA5	VA4	VA3	VA2	VA1	VA0
---	---	---	---	---	---	---	---
DA15	DA14	DA13	DA12	DA11	DA10	DA9	DA3

The address lines at VA0 and VA1 are arranged so they can get refreshed during a normal CRTC scan. This results in a reduction of components in the video circuits.

Jumper J307 permits using 64K RAMs or 32K RAMs. To use 64K RAMs, connect the jumper from DA15 to U373-11. To use 32K RAMs located in the upper half of the 64K address space, remove the jumper. To use 32K RAMs in the lower half of the 64K address space, connect the jumper from U373-11 to ground. Note that if the computer uses 32K RAMs, they all must be located in either the upper 32K of each 64K bank or all in the lower 32K--they can't be mixed. See the H/Z-100 Memory Map located further on in this description.

CONVERTING THE RAM DATA TO VIDEO

There are two sets of data lines at the video memory. One is an 8-bit bus, BD0-BD7, used by the CPU to write to RAM (from U178 on schematic MB2); and three 8-bit output buses, one for each color.

The output buses go to the CPU through U339, U310, and U316. Only one of these ICs will be selected to place the data on BDI0-BDI7. This, in turn couples through U323 on MB2 to the CPU. This will be covered in more detail later.

The three output buses also couple to the video processing circuits through U332, U302, and U311. Here's how the data is processed.

When the CRTC has control of RAM (which is most of the time, since it has priority), the VRAM is in the read mode. This is due to a logic zero on VDRAMSEL (U337-4) and CLRSCRN (U366-3). When the addressed data settles, VIDSTRB from U376-17 asserts to latch the RGB data into U332, U302, and U311. (Note: If this is a minimum system--green only--U332 and U311 outputs will remain a steady state.)

Next, the load shift register line from U320-6 goes low to latch the RGB data into the parallel-to-serial converters, U325, U301, and U303. This line pulses at the character clock rate.

The dot clock, at pin 6 of these ICs, then shifts the data out through pin 13. This takes place at 8 times the character clock rate, or 14.112 MHz. While the video information is being shifted out, VIDSTRB is loading the next byte into the D latches. When the last dot is shifted out of the parallel-in/serial-out converter, the bytes in the D latches are loaded in and the cycle repeats.

The three serial dot lines connect to RIN, GIN, and BIN of U337, the VIDATTR PAL. Other inputs to U337 include the FLASH line and three enable lines at pins 1, 2, and 3.

When asserted, the enable lines from the PIA (U345) gate their respective dot video color to the outputs at pins 14, 15, and 16.

When the FLASH line--also from the PIA--is asserted, the output lines selected by the enable lines will go high, saturating that color onto the screen and masking any video data on that line.

For example, if ENBL-G were the only asserted enable line, then dot video would only be present on GOUT. Asserting the FLASH line would cause GOUT to go to logic one, causing the screen to appear solid green.

Two other lines enter U337; the display enable and the cursor signal. The display enable (DISEN) goes low to blank the video data during horizontal and vertical retrace. It comes from pin 18 of the CRTC and is delayed by two character clocks through the hex D flip-flop. This delay is used to match the timing of DISEN to the video signal delayed by the parallel-in/serial-out converters. If DISEN wasn't delayed, retrace blanking will occur 2 clock cycles early, blanking the last 2 character positions.

The cursor signal enters pin 6 to generate a cursor at ROUT, GOUT, and BOUT. It comes from pin 19 of the CRTC and goes through the hex D flip-flop to be delayed by two character clocks. This two-character delay places the cursor to the right of the last displayed character.

The horizontal and vertical sync pulses also come from the CRTC and are clocked through the D flip-flop. These signals, however, bypass U337 and connect to U329, another hex D flip-flop. The RGB lines enter this flip-flop at pins 11, 13, and 14. All five signals are clocked out by the dot clock entering at pin 9. The purpose of this flip-flop is to correct for any propagation delays in the various signal paths.

VIDEO OUTPUT

COLOR OUTPUT

The 3 RGB lines from U329 connect to U307 on schematic VB3. This buffer provides red, green, and blue video pulses to P303. Logic 1 equals color on; 0 is black level.

The horizontal and vertical sync pulses connect to U320, pins 12 and 9. These signals then pass through the drivers at U322 to P303. P303 connects through a mating cable to an RGB color monitor. Jumpers J302 and J304 allow selecting the polarity of the sync signals, while J303 allows sending composite sync to U320-9 by connecting it to U355-11.

MONOCHROME OUTPUT

RDOTA, GDOTA, and BDOTA also connect to U323, a 3-to-8-line demultiplexer. J306 and J305 connect one color to each input at pins 1, 2, and 3. If this is a minimum system (green only), then pins 1 and 2 are jumpered to pin 3.

U323 decodes the three inputs to assert only one output at Q0-Q7. This signal connects to U309, which is clocked through by the dot clock. The mnemonics on the output lines indicate the color represented by the combination of the three inputs. These outputs couple through the inverters to the resistive weighting network.

This network converts the associated line to a specific voltage level before applying it to the emitter followers at Q302 and Q301. This network forms a monochrome gray scale by controlling the current through the emitter followers.

For example, if RDOTA, GDOTA, and BDOTA were all asserted, U309-19 would go high, driving U308-8 low. This gives the highest emitter resistance, causing the most positive voltage at the output and giving maximum brightness.

If none of the RGB lines were asserted, then U309-2 would go high to place U322-6 at logic zero. This lowers Q301's emitter voltage to the black level.

Composite sync from U355-11 provides horizontal and vertical sync pulses at the blacker-than-black level.

The composite video output of P301 connects to the video input of the internal or external monochrome monitor.

CPU-VIDEO COMMUNICATIONS

OVERVIEW

The CPU can communicate with the video board through several I/O ports, or by read/writing the video RAM. It uses the I/O ports to access the CRTC, the PIA, and the light pen circuits. It can read/write the video RAM to set up the character font or draw high-density graphics.

VIDEO I/O CIRCUITS

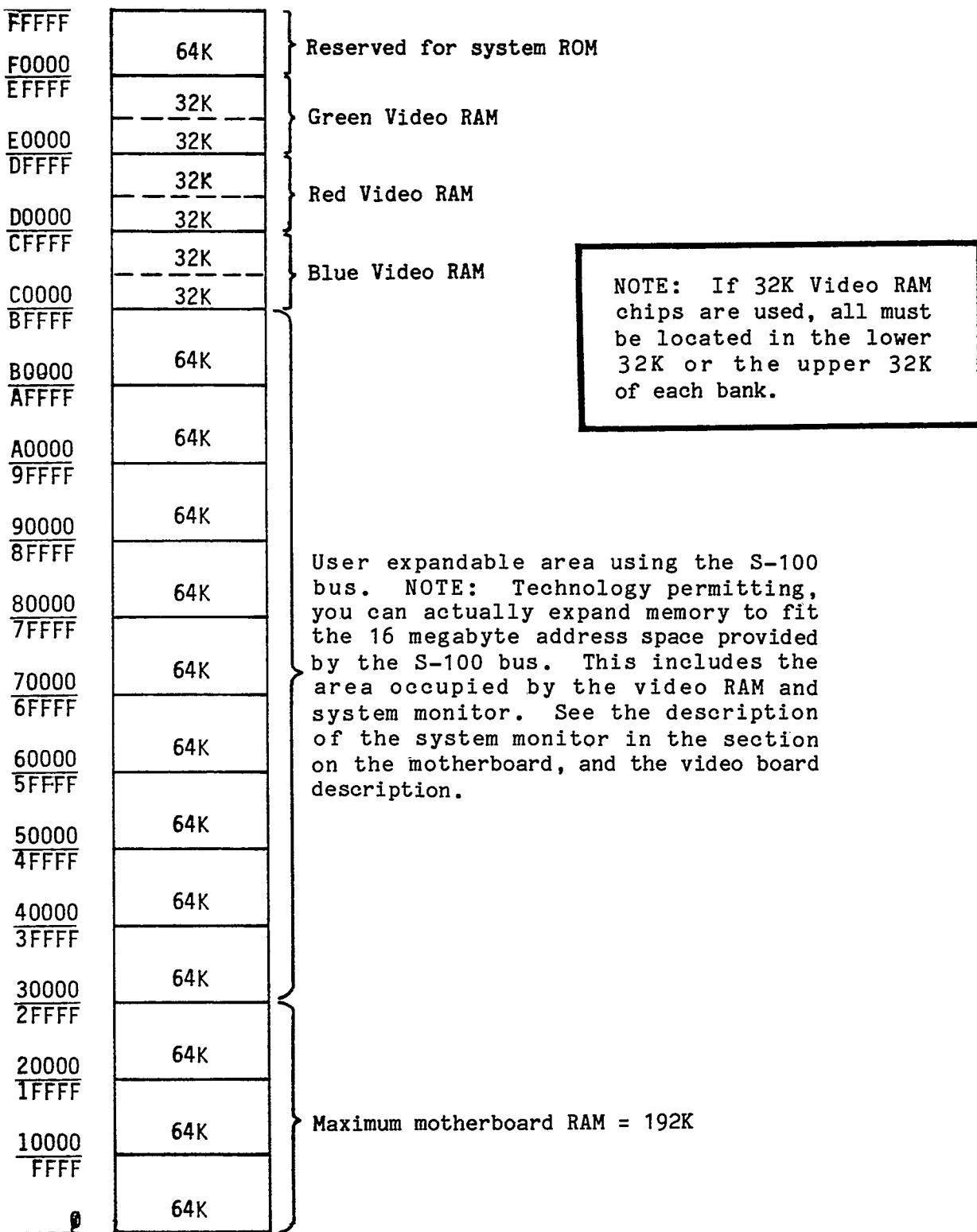
Video I/O addresses are decoded by VIOSEL, U369, a 256 x 4 PROM. This IC (on schematic VB1) is selected by the appropriate address on BA0-BA7 and the \overline{IO} line from the E-clock logic on schematic MB2. The outputs are:

6845CS Selects the CRTC programming as described earlier.

CRTI0CS (A) Chip-selects the PIA at U345, and (B) provides one input to the OR gate, U372/U366. The other input to this OR gate is 6845CS; the output is 4521CS. This line chip-selects U331 when the CPU is reading data from the CRTC or from the PIA.

LPNCS Chip-selects the light-pen counter circuits at U315 if the CPU is processing a light-pen interrupt request. See the discussion on the light-pen circuits.

VIDBSEL Asserts when pins 12, 13, or 10 asserts. This line goes to U372-13 and is NANDed with DBIN at U366-13. The result is RDBFRENBL at P304-57; this enables the read buffer, U223 on schematic MB2, when one of the VIOSEL lines is asserted.



H/Z-100 MEMORY MAP

Another video I/O circuit is the PIA at U345 (near the center of schematic VB1). This is used for address decoding, controlling the display, and performing some VRAM operations.

The CPU selects the PIA at ECLK time (pin 25) by asserting CRTIOCS at pin 23. BA0 and BA1 select the register to be accessed while OUT determines if data is to be read from or written to that register. For this PIA, all I/O lines are programmed to be outputs. Here's what they do:

ENBL-R, -G, -B, & FLASH Enables the selected video line without affecting RAM. FLASH causes the selected line to appear as a solid color. See "Converting the RAM Data to Video" for more information.

WRT-R, WRT-G, WRT-B Selects the red, green, or blue banks when the CPU writes to VRAM. These lines are necessary because there's only one 8-bit data bus from the CPU; so red, green, and blue data must be written at separate times.

CRTRAM ENBL Chip-selects VRAMSEL, U371-4, which selects the red, green, or blue banks when the CRT reads the VRAM.

LA8-LA15 Goes to the memory mapping module to decode the selected video memory location.

CLRSCRN Goes to the video memory circuits to provide a quick means to clear the screen.

MEMORY SELECT CIRCUITS

The memory select circuits are centered around U371, VRAMSEL, a 256 x 4 PROM. This IC is used when the CPU wants to access the red, green, or blue memory banks. VRAMSEL is selected by asserting CRTRAM ENABLE at the PIA. Also, MEMR or WO is gated through U377 (near VRAMSEL) for further chip-selecting. The OUT line at U377-2 ensures that U371 won't activate on an OUT port operation.

The outputs assert depending on what location in the video memory map is selected:

```
RSEL = OD0000H-ODFFFFH  
GSEL = OE0000H-OEFFFFH  
BSEL = OC0000H-OCFFFFH
```

Each line has a 64-kilobyte range; currently, Heath Company supports only 32K.

CRTRAMSEL asserts whenever pin 11, 10, or 9 asserts. This connects to U372-12 in the lower left corner of the schematic. It is combined with VIDBDSEL and DBIN to assert RDBFR ENBL. This line enables U223 (on schematic MB2) during a memory read operation.

CRTRAMSEL is double-inverted at U366-5 to form CRTRAMSEL1 at P305-61. This line asserts PHANTOM* at U194-4 on MB2. If an S-100 memory card is occupying the same memory space as VRAM, PHANTOM* prevents the CPU from writing to the S-100 memory when it's accessing video RAM. This permits installing read/write memory in the same address space as VRAM without them interfering with each other.

CRTRAMSEL also goes to U372-3, VIDRAMRDY, through an inverter. If the CRTC is busy processing a video signal, it won't let the CPU access the RAM circuits. U372-2 is also high, causing VIDRAMRDY to go low. This drives RDY low at U194-12 on schematic MB2, putting the CPU into a wait state. The CPU will hold CRTRAMSEL asserted until the CRTC gives the CPU control of the video circuits.

Finally, CRTRAMSEL goes to U379-11, part of the CPU/video arbitration circuits. These circuits synchronize the video circuits to the CPU circuits and determine when the CPU can access the video RAM. See the previous paragraph and the description of the control and timing circuits.

READ DATA BUFFERS

The CPU reads the addressed data through either U339, U310, or U316. When the CPU reads VRAM, the memory places data on the inputs of these latches. To read a particular bank, the CPU asserts RSEL, GSEL, or BSEL. For example, to read the data in the green video memory bank, the CPU addresses the desired video memory section (to be explained shortly) and asserts GSEL at U371-10 (upper left on schematic VB1). This signal connects to U351-9 (right center on schematic VB1). When DBIN from the S-100 bus asserts, U351-8 goes low to couple the data in U310's latches to the BDI bus. In turn, this data couples through U223 (on schematic MB2) to S-100 lines DIO-DI7 before coupling to the CPU.

MEMORY MAPPING MODULE

The memory mapping module consists of U370, U364, and U365. It translates the CPU address range into the address range used by the CRTC. The CRTC sees the VRAM in the range of 0-64K, while the CPU sees the memory in the range of 768K to 960K.

To convert the CRT address range to 0-64K, the CPU latches a bit pattern into LA8-LA15. The CPU then requests access of the video RAM by asserting VIDRAMSEL, the desired color bank (RSEL, BSEL, GSEL), and the appropriate address lines on the inputs of U370.

U370 decodes the address and feeds it to the adders at U364 and U365. These ICs add the decoded address to LA8-LA15 and places the result onto the B inputs of U358 and U359. The rest of the CPU address is present on the B inputs of U357 and U363.

When the CRTC is finished accessing the display, it brings VIDRAMSEL low at U377-4 (lower left corner of schematic). This couples the B inputs of the multiplexer ICs onto address lines DAO-DA15. The correct VRAM location can now be read or written.

VIDEO RAM

OVERVIEW

Schematic VB2 shows a close-up of the video RAM.

The video RAMs are 32K x 1-bit dynamic RAMs; 64K RAMs can also be used, but aren't currently supported. The RAMs are arranged into three banks, 64K apart; one bank for each of the primary colors. In a minimum system, only the green bank will contain memory. The CPU can read/write RAM, while the CRTC can only read.

CPU WRITE

The CPU writes to RAM through U346; it places data onto the bus and asserts WE of each chip through U374-11. This comes from BMWRT and VIDRAMSEL at U355-5 and U351-4.

The RAS portion of the address is present on VA0-VA7.

The correct color bank(s) is selected by asserting WRT-R, WRT-G, and WRT-B at pins 2, 4, and 10 of U350. This gates the RAS line through U375-11, U375-8, and U374-8 for the selected bank.

Next, the CAS address is placed on VA0-VA7 and the CAS line asserts U375-3, U375-6, and U374-6. Only the bank(s) previously selected by RAS will be affected.

Data present at the inputs of U346 are coupled into the appropriate memory location(s) in the video RAM.

CPU READ

When the CPU reads from RAM, it asserts R-SEL, G-SEL, or B-SEL to select the appropriate color bank. The RAS and CAS lines operate as before. The addressed data is placed on the DOUT lines of the selected banks and read by the CPU as explained previously.

CRTC READ

The CRTC reads all three banks at the same time; the enable lines at U337 (schematic VB1) select which banks are to be displayed as explained previously. When the CRTC has control, VIDRAMSEL is low and couples to pins 13, 5, and 11 of U350. This forces pins 12, 6, and 8 of U350 to logic 1.

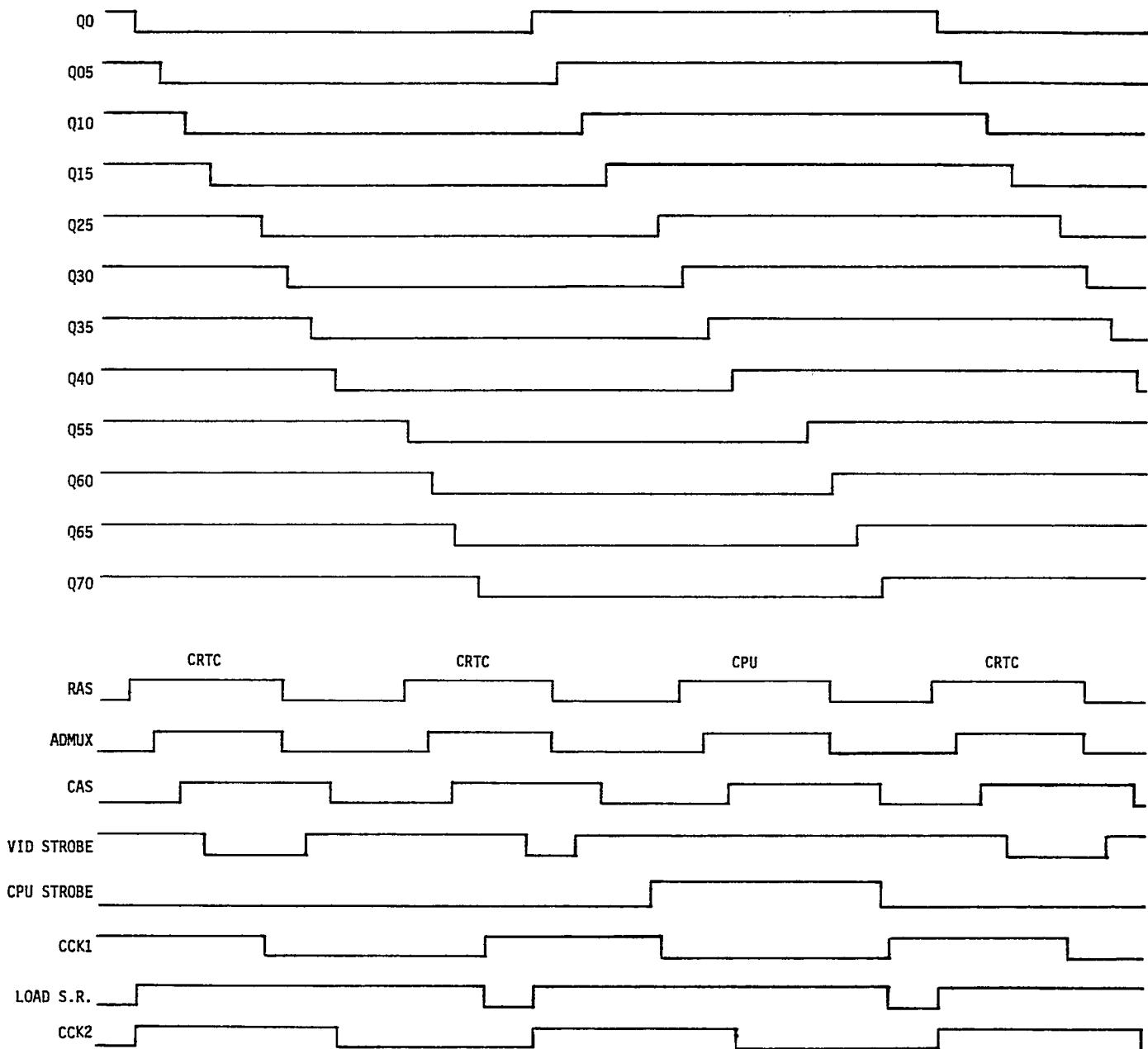
When RAS occurs, the address on VAO-VA7 is latched into all three banks. Next, CAS asserts and also addresses all three banks. The data from each bank is placed onto the appropriate bus and sent to the parallel/serial conversion circuits.

CLEAR SCREEN FUNCTION

The clear screen function allows the CPU to quickly clear the screen. Instead of directly writing to memory, which is time-consuming, the CPU uses the fast scanning feature of the CRTC. Here's how.

The CPU asserts the CLRSCRN line at the PIA; it also clears or sets the SET line. These lines connect to the PAL at U346; CLRSCRN disconnects the PAL from the data on its input, while SET places all ones or zeros on the output lines, depending on the logic level at pin 11. (If logic one, the screen will be painted white instead of blanked.)

CLRSCRN also connects to U355-4 and U351-5 to force the WE line low on all RAMs. During this time, the CRTC has control of the bus. Since the CRTC scans all memory locations, each bank will be filled with ones or zeros, depending on the level on SET. The CRT is quickly blanked or flashes white.



VIDEO BOARD TIMING

TIMING AND VIDEO ARBITRATION

TIMING

Refer to schematic VB1 and the accompanying waveforms as you read the following.

The 14.112 MHz crystal-controlled oscillator at U368 provides the basic timing for the video circuits. This signal couples through U344-11 to provide dot clock and couples through U344-6 for inverted dot clock. This method was used instead of series-connected inverters to ensure that the two clock signals are exactly 180-degrees out of phase.

DOTCLK drives U336 and U343; these ICs are wired as a ring counter to derive Q0-Q70 shown in the adjacent waveforms. U367, driven by DOTCLK, uses some of these outputs to generate the odd-numbered waveforms from Q05 to Q65. These signals connect to the VIDRAM PAL at U376.

U376 uses the Q signals to generate VIDSTRB, ADMUX, RAS, and CAS. VIDSTRB clocks addressed data into the latches prior to parallel-to-serial conversion as described previously. ADMUX multiplexes the 16-bit address bus onto an 8-bit address bus in time with RAS and CAS. ADMUX is low during RAS and high during CAS.

The CRTC has control of the video circuits for 2/3 of any timing cycle. This ensures fast display refresh while the remaining 1/3 allows the CPU to rapidly update the display memory.

The CRTC's portion of the cycle begins on the negative transition of Q0. This is indicated by the two RAS waveforms marked "CRTC" on the Video Board Timing waveforms. Video arbitration circuits (to be explained presently) ensure that the CRTC always has control during these two RAS cycles.

The third RAS cycle of the video timing cycle is reserved for the CPU. If the CPU doesn't attempt to read or write memory, RAS will not assert during the time marked "CPU." If the CPU does attempt to read or write memory, RAS will assert and the memory access can take place. Note that during CPU RAS time, VIDSTRB (U376-17) doesn't pulse. This prevents the addressed memory location from being latched into U322, U302, and U311; keeping unwanted noise off the display.

If the CPU attempts to access video memory during the CRTC portion of the cycle, the arbitration circuits places a logic zero on P305-62. This logic zero couples to the CPUs READY line which puts the CPU into a wait state. The CPU ceases activity until the "CPU" RAS cycle begins. At this time, P305-62 goes high to activate the CPU.

Obviously, the CPU processing time will slow down if it performs a lot of reading and writing to video RAM. However, the video arbitration circuits do not slow down the CPU for non-video operations (such as I/O and system memory accesses). As long as the CPU isn't accessing the video circuits, P305-62 remains high and the CPU operates at full speed.

Now for a closer look at the video arbitration circuits.

VIDEO ARBITRATION

The video arbitration circuits determine if the CPU is requesting access to the video RAM. If the CRTC is not using the RAM, it gives control to the CPU. However, the CRTC always has priority.

As mentioned previously, the CPU requests control of the VRAM by asserting RSEL, GSEL, or BSEL at U371. This asserts CRTRAMSEL which couples through U372-3 to put the CPU into a wait state after the CPU finishes the 2nd processor cycle.

CRTRAMSEL also goes to U379-11 to set up the bus arbitration circuits for a read/write request from the CPU. If the operation is a CPU write, then U379-3 goes high. If the operation is a CPU read, then MEMR is clocked into U378-5 when STVAL*SYNC asserts. In turn, U378-5 couples the logic one to U379-2.

At this time, U361-8 is latched to logic one which is coupled to U372-2. U372-1 is also logic one due to the asserted CRTRAMSEL line at U366-4. U372-3 holds the CPU in a wait state as described previously. Because of this, pins 11 and 12 of U379 remain at logic zero. The resulting logic 1 at U379-13 is the CPU request signal which couples to pin 2 of U361.

When the CRTC has completed processing the video circuits, Q15 at U361-3 goes high. This latches U361-6 to logic zero and, because U361-9 is also zero, drives the VIDRAMSEL line at U377-4 to logic one. VIDRAMSEL connects to the control inputs of the CPU/CRTC address multiplexers to couple the CPU address lines to the video memory circuits.

If the CPU is writing memory, data from the S-100 bus is present on lines BD00-BD07. BMWRT writes this data into memory. If the CPU is reading memory, the addressed memory location places the data onto U339, U310, or U316; depending on the RGB select lines going into memory.

When line Q65 goes high, the logic one at U361-5 is latched into U361-9. This latches the data on the inputs of U339, U310, and U316 onto their outputs; if memory read. The status of the gate at the input of each octal latch will determine which latch will be coupled to the bus.

At the same time, U361-8 goes low to bring VIDRAMRDY high. The CPU leaves the wait state and finishes processing the instruction. CRTRAMSEL goes high to drive U379-13 low. Since VIDRAMSEL is also low, U355-3 goes to logic zero to clear U361.

The CRTC again has control of the video board.

LIGHT PEN CIRCUITS

The light pen strobe enters U362-12 (at top center of schematic VB1) from U116-9 on schematic MB4 (see the parallel port description for more detail). The DOTCLK signal toggles LTPNSTB through U362-9 to U356-5. Next, the clock signal at U356-11 latches the LTPNSTB signal onto U356-9. This positive-going signal latches the refresh address into the CRTC's light pen register. The refresh address points to the first line of characters to be displayed after vertical retrace. See the CRTC IC data sheets.

Also, the output of U356-5, PENSTBD, goes to U315-11 (lower right corner of the schematic). U315 is an octal latch that is loaded by the CRTC row address lines, RAO-RA3, and the 4-bit down-counter, U324.

At the time of PENSTBD, RAO-RA3 point to the row that was active when the light pen strobe occurred; U324 points to the dot position.

As explained in the parallel port description, when LTPNSTB asserts, the parallel port (on schematic MB2) sends an interrupt to the CPU. From here, it's up to the user's program to process the interrupt.

If the CPU is programmed to respond to a light-pen interrupt, it will read the data stored in the CRTC light-pen register and the data stored in U315 to find the exact pixel location. The CPU reads the CRTC as described earlier; it reads U315 by asserting LTPNCS from the VIOSEL PROM and DBIN from the S-100 bus. From here, the CPU can compute the video memory location and access the bit in that memory location to be processed.

VISUAL CHECKS

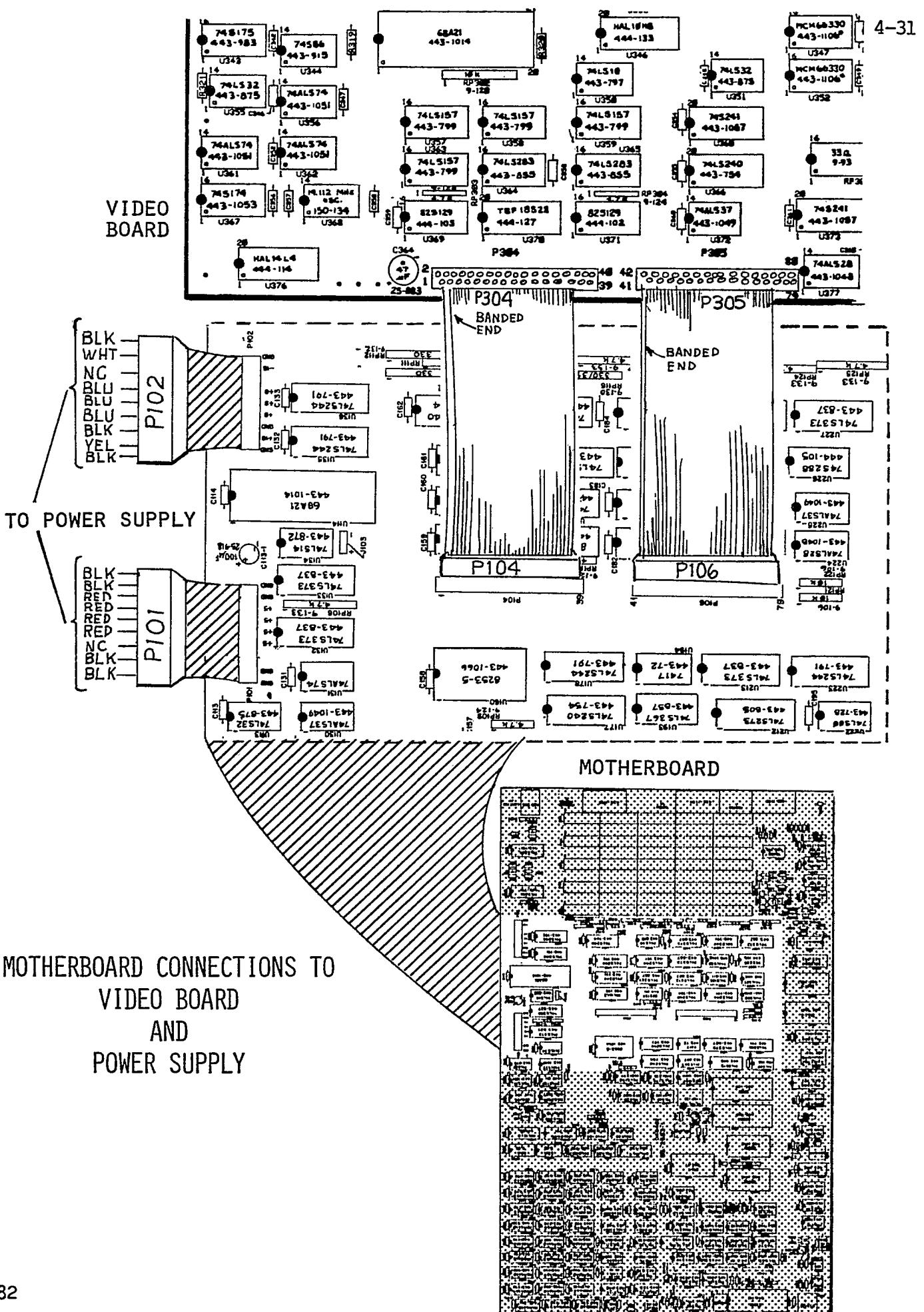
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BLACK AND WHITE VIDEO BOARD (#181-3631) JUMPER LOCATIONS AND POSITIONS	4-34
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VIDEO BOARD COMPONENT LOCATIONS AND VALUES	4-36

3

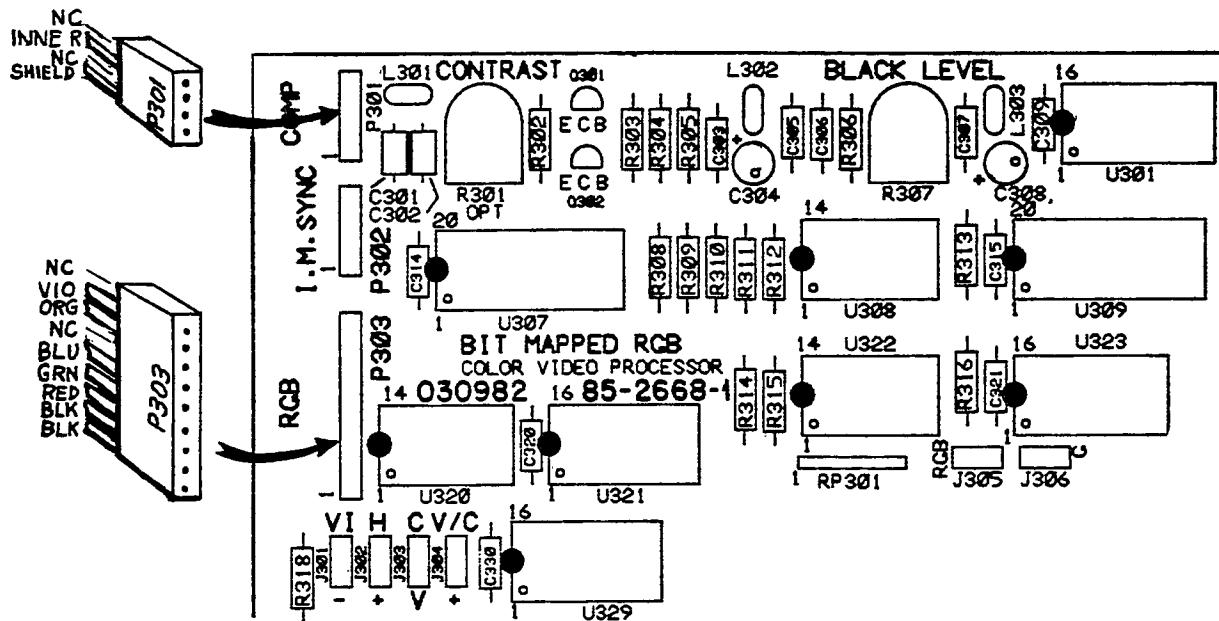
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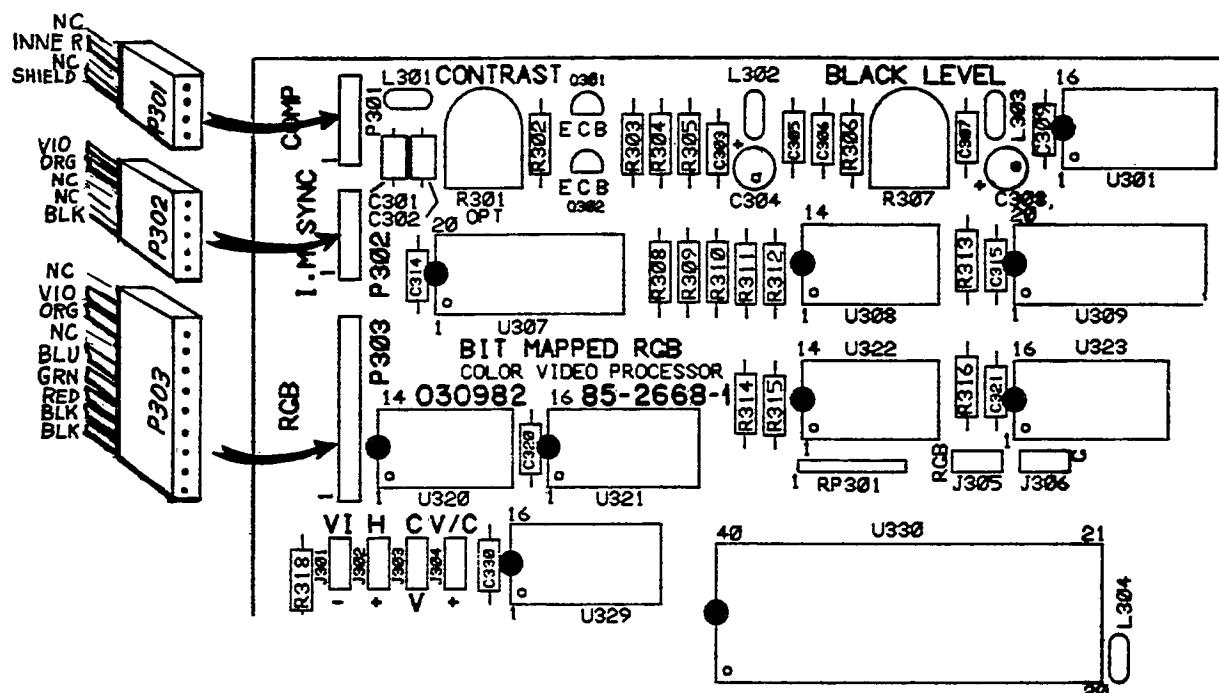
4



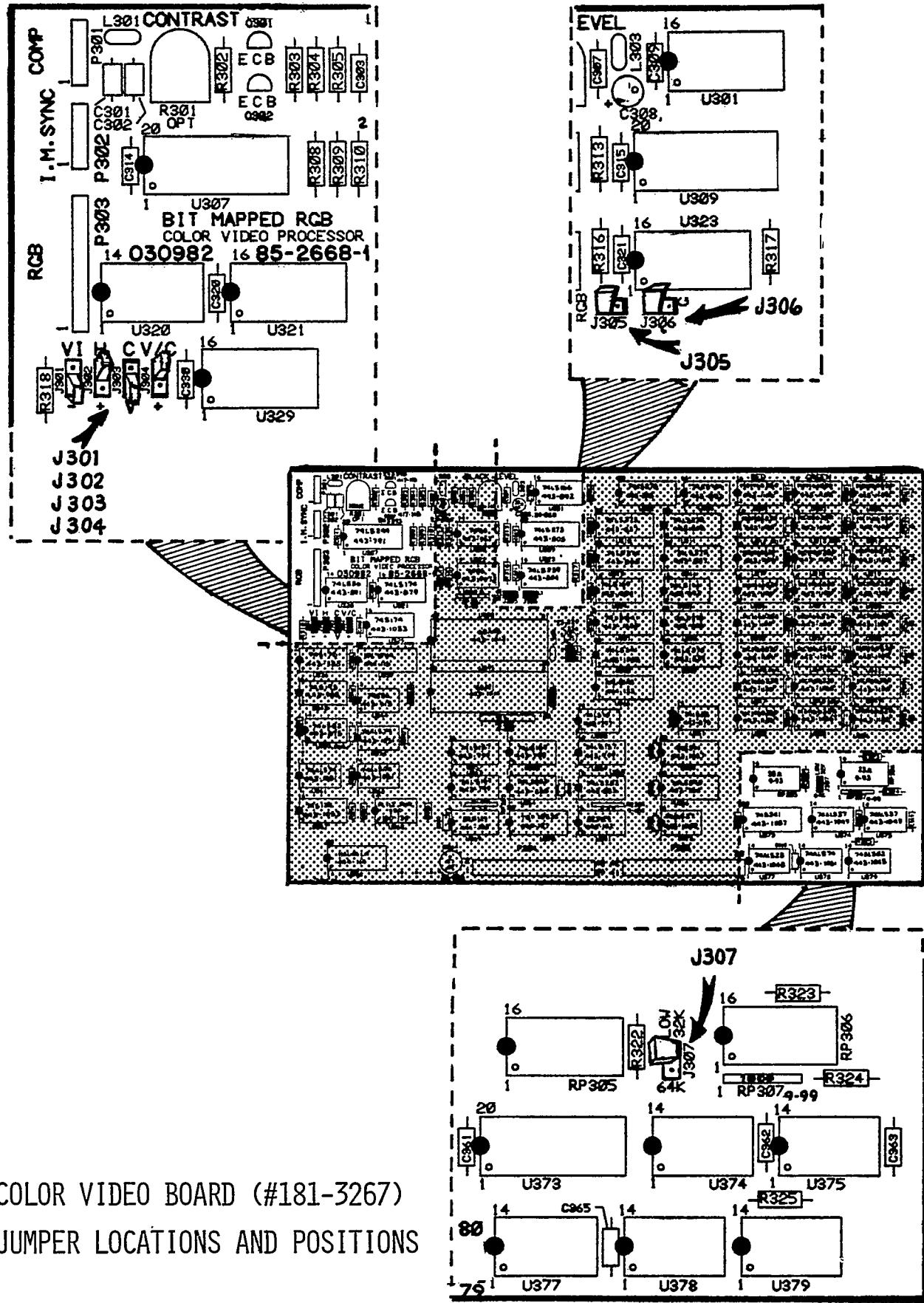
VIDEO BOARD CONNECTIONS

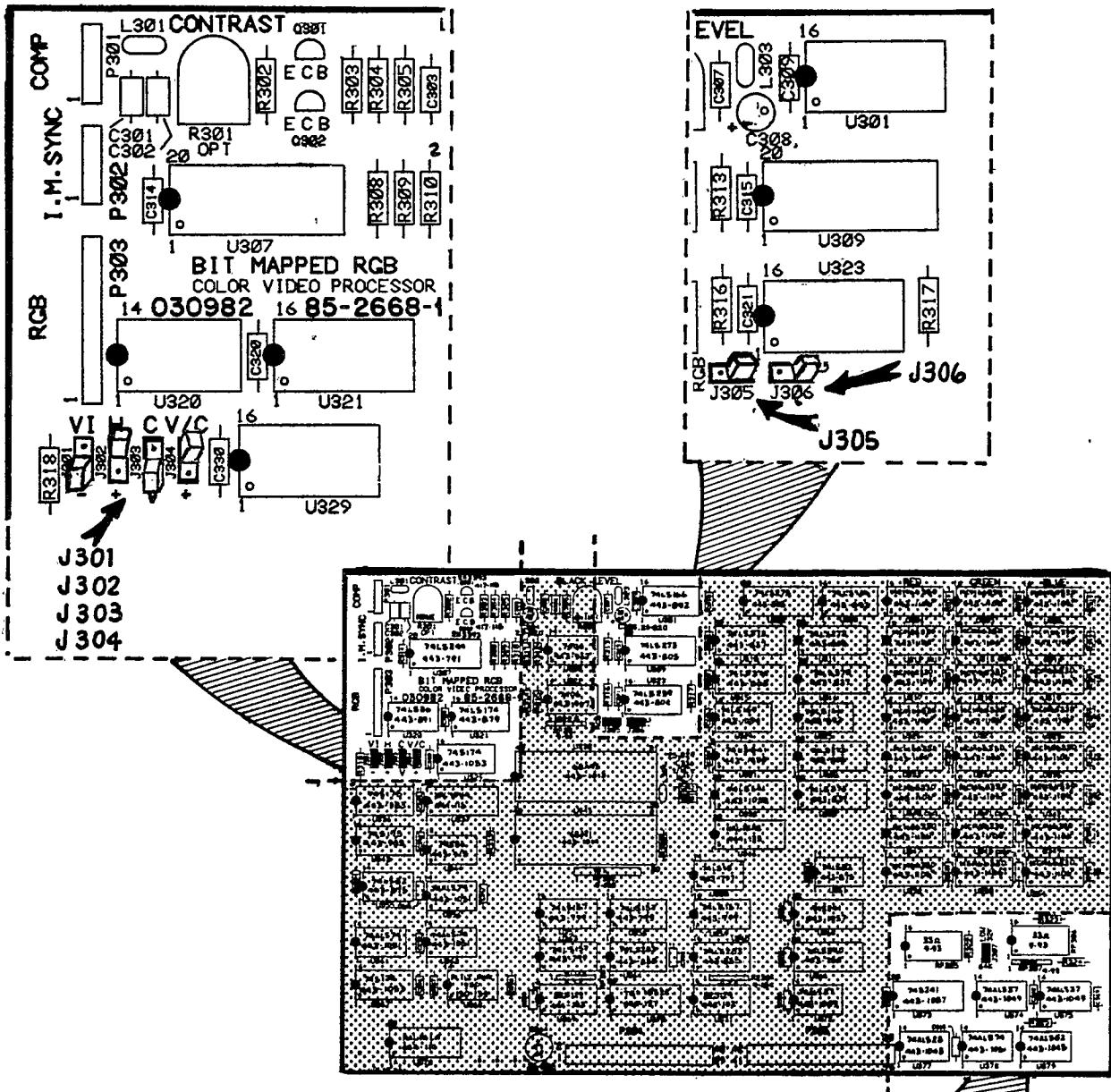


LOW-PROFILE VIDEO BOARD CONNECTIONS

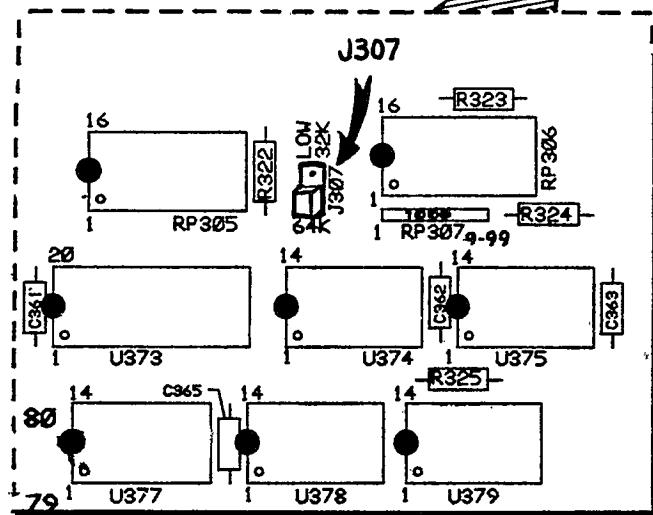


ALL-IN-ONE VIDEO BOARD CONNECTIONS

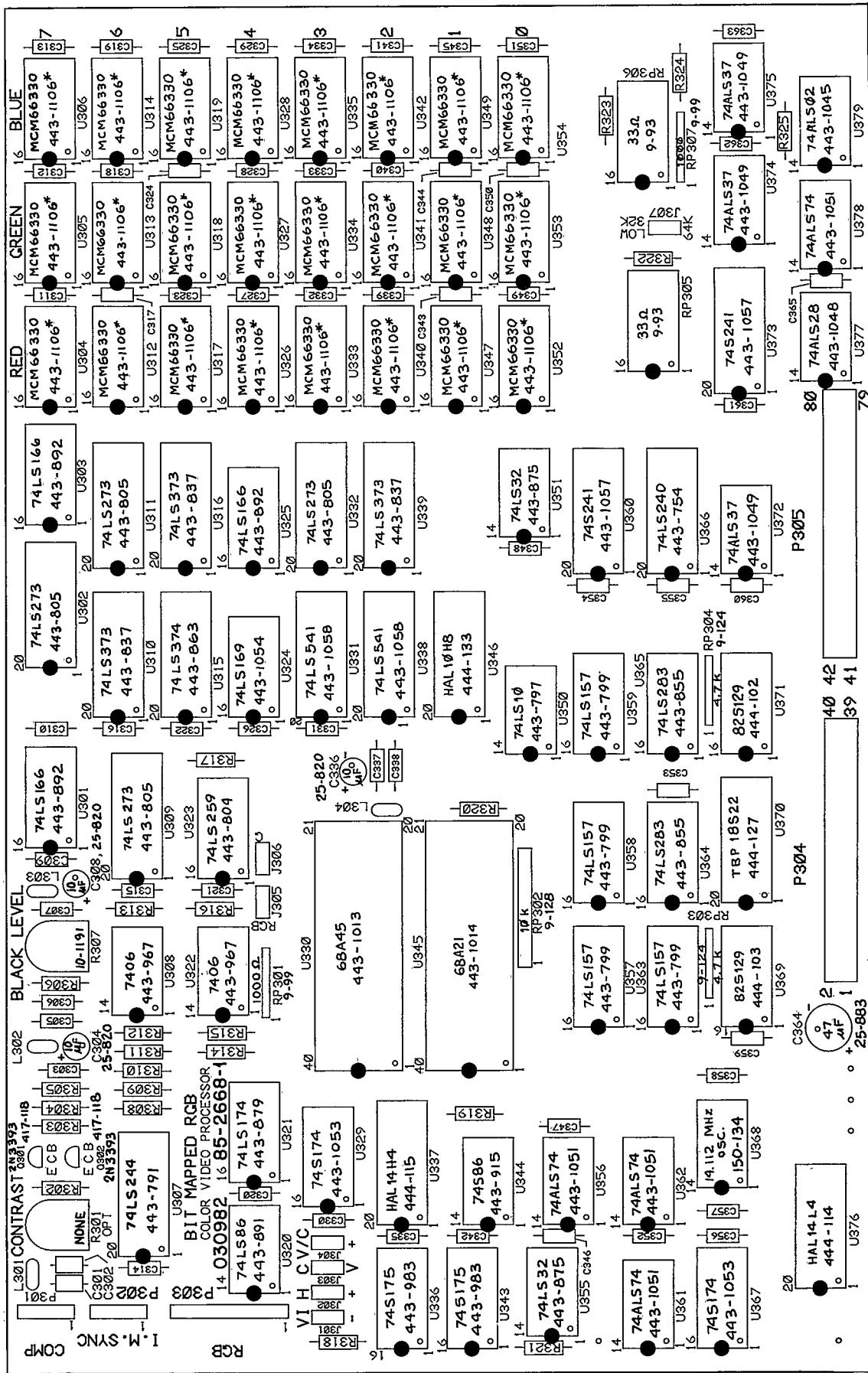




**BLACK AND WHITE VIDEO BOARD
(#181-3631)
JUMPER LOCATIONS AND POSITIONS**



CIRCUIT COMPONENT LOCATIONS AND VALUES



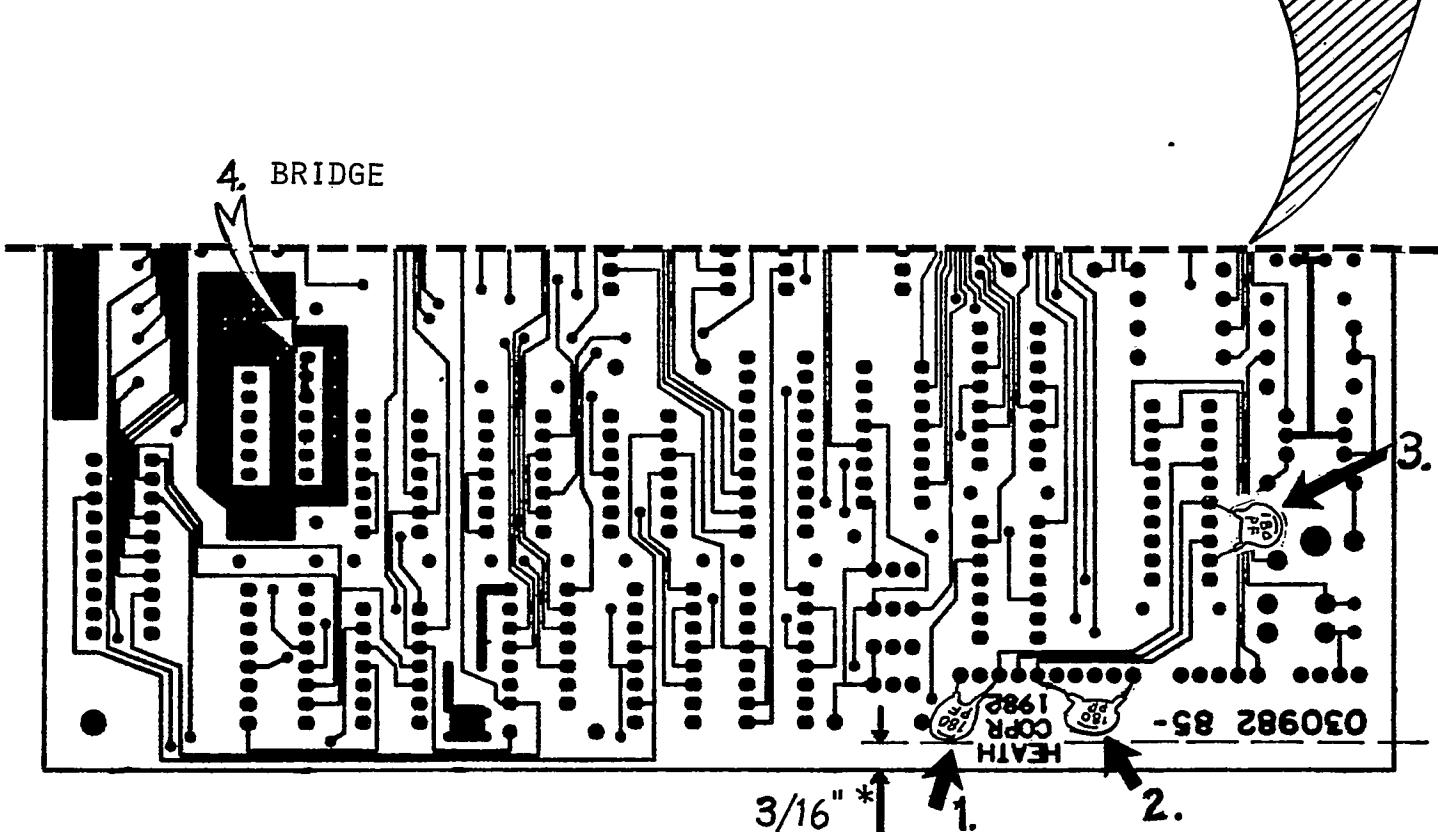
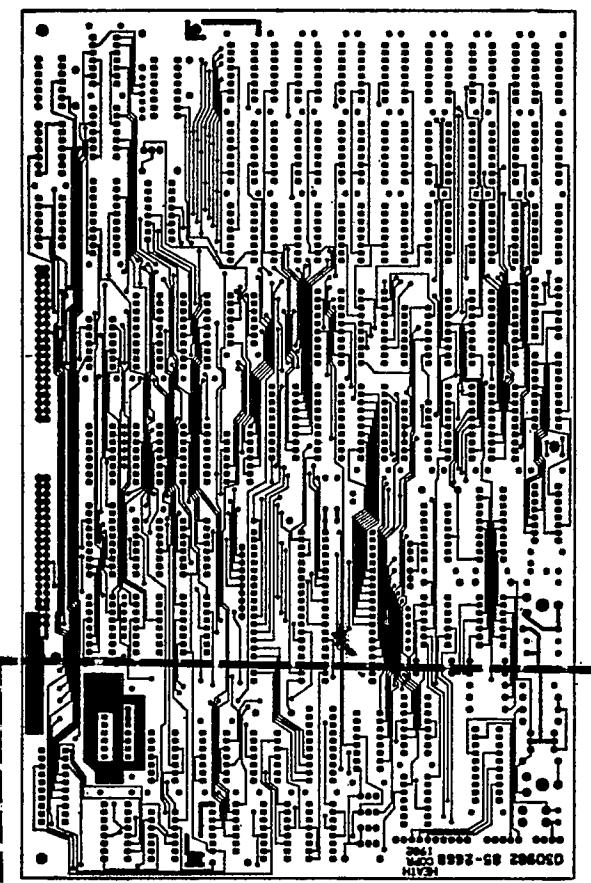
***NOTE:** The ICs in these locations may be MCIM6655 (HE 443-970). Refer to "Configuration" for further information.

COLOR VIDEO BOARD
BLACK AND WHITE: HE 181-3631
COLOR: HE 181-3267

**VIDEO BOARD
COMPONENT LOCATION AND VALUES,
FOIL SIDE OF BOARD**

1. 180 pF capacitor (HE 21-746),
Installed between P303-1 and P303-3.
2. 180 pF capacitor (HE 21-746),
Installed between P303-5 and P303-10.
3. 180 pF capacitor (HE 21-746),
Installed between U307-16 and U307-19.
4. U368-9 bridged with U368-10.

*Note: 3/16" minimum clearance from edge
of board required for capacitor installation
at 1 and 2.



TROUBLESHOOTING

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INTRODUCTION

The following procedure will help you repair the video board to the point where you can get a display on the screen. Though these tests aren't as fast or thorough as a diagnostics program, they'll help you narrow the problem down to two or three components. Once you get the display working, run the video memory test described in the Diagnostics section of this manual.

As diagnostic programs become available, we will publish them for inclusion in the Diagnostics section of this manual. Also, if you develop any troubleshooting techniques or diagnostic programs that you'd like to share, send it to:

Heath Company
Service Publications and Training
Dept. 741
Benton Harbor, Mi. 49022

We will evaluate your submission and, when approved, publish it for inclusion in the Service Bulletins or Diagnostics sections of this manual. Be sure to include a complete description of the troubleshooting technique, symptoms caused by the failed component, and any special equipment needed to repair the problem. If submitting a diagnostic program, we will need a copy of the source listing; preferably on disk.

SERVICE GUIDE

As you become more experienced troubleshooting the H/Z-100, you'll be able to skip this section and go directly to the group of circuits causing the problem. Until then, use the following guide to locate the most likely circuits to test for a particular symptom.

Detailed checkout procedures for the major circuits on the video board follow the service guide. If this is your first time troubleshooting the H/Z-100, read the introduction to the checkout procedure before proceeding with those tests.

Finally, bear in mind that these test procedures are for isolating problems on the video board. All the other modules in the H/Z-100 must be known to be operating properly. Otherwise, you won't get the correct results.

1. No display, or no horizontal or vertical sync.

Perform the Video Signal and Sync Tests.

Check the video monitor or video sweep board for proper operation.

2. Video circuits won't initialize. High-pitched squeal heard from monitor and torn raster seen on the CRT.

The CRTC isn't being programmed properly by the CPU on the motherboard. Check for secure connections on P304 and P305.

Perform the checks under Video I/O Tests.

3. Characters on the CRT are distorted.

Nonlinear sweep in the video monitor.

Perform the video memory tests in the Diagnostics section of this manual.

TECHNICIAN NOTES:

CHECKOUT PROCEDURES

In the following tests, you need only test the ICs in the left column indicated by an asterisk (*). If you don't get the suggested logic state, then check each IC listed immediately to the right. The logic states for these ICs are listed in the left column below the ICs with the asterisks.

Continue tracing backwards using this procedure until you test an IC that matches the suggested logic state. The previous IC that you tested is likely the bad IC.

Before you replace the suspected IC, check the other lines leading up to it. You must do this because this checkout procedure gives only the most likely causes of the problem. It doesn't cover such things as open ground foils, foil runs shorted together, open resistors, or missing power supplies.

To help you locate the IC on a schematic, the schematic number is shown in parenthesis to the right of the IC under test.

Unless instructed otherwise, perform these tests with the H/Z-100 configured for 5-1/4" drives (primary) and with auto-boot defeated. See the Configuration section. Also, unless noted otherwise, all logic states are those present after a hard reset.

VIDEO SIGNAL AND SYNC TESTS

CHECK	IF NOT OKAY, CHECK
*U307-7 = P (VB3)	U307-13
*U307-9 = P (VB3)	U307-11
*U307-14 = P (VB3)	U307-6
*U307-16 = P (VB3)	U307-4
*U307-18 = P (VB3)	U307-2
*U322-2 = P (VB3)	U322-1
*U322-12 = P (VB3)	U322-13
*U355-11 = P (VB3)	U355-12, U355-13

End of test.

J301	(VB3)	See Configuration Section.
J302	(VB3)	See Configuration Section.
J303	(VB3)	See Configuration Section.
J304	(VB3)	See Configuration Section.
U301-6 = P (VB1)		See VIDEO TIMING and CONTROL TESTS.
U301-13 = P (VB1)		U301-6, U301-15, U302-11
U301-15 = P (VB1)		U320-6
U302-11 = P (VB1)		See VIDEO TIMING and CONTROL TESTS.
U303-6 = P (VB1)		See VIDEO TIMING and CONTROL TESTS.
U303-13 = P (VB1)		U303-6, U303-15, U311-11
U303-15 = P (VB1)		U320-6
U307-2 = P (VB3)		U329-15
U307-4 = P (VB3)		U329-12
U307-6 = P (VB3)		U329-10
U307-11 = P (VB3)		U329-2
U307-13 = P (VB3)		U320-3
U311-11 = P (VB1)		See VIDEO TIMING and CONTROL TESTS.
U320-1 = P (VB3)		U329-5
U320-3 = P (VB3)		U320-1, J301
U320-4 = P (VB1)		See VIDEO TIMING and CONTROL TESTS.
U320-5 = P (VB1)		See VIDEO TIMING and CONTROL TESTS.
U320-6 = P (VB1)		U320-5, U320-4
U320-8 = P (VB3)		U320-9, J304
U320-9 = P (VB3)		J303, U329-5
U320-11 = P (VB3)		U320-12, J302
U320-12 = P (VB3)		U329-2

U321-2 = P	(VB1)	U321-3, U321-9
U321-3 = P	(VB1)	U330-39
U321-4 = P	(VB1)	U330-40
U321-5 = P	(VB1)	U321-4, U321-9
U321-6 = P	(VB1)	U330-19
U321-7 = P	(VB1)	U321-6
U321-9 = P	(VB1)	U344-8
U321-10 = P	(VB1)	U321-11, U321-9
U321-11 = P	(VB1)	U321-7
U321-12 = P	(VB1)	U321-13
U321-13 = P	(VB1)	U330-13
U321-14 = P	(VB1)	U321-12
U321-15 = P	(VB1)	U321-14, U321-9
U322-1 = P	(VB3)	U320-8
U322-13 = P	(VB3)	U320-11
U325-6 = P	(VB1)	See VIDEO TIMING and CONTROL TESTS.
U325-13 = P	(VB1)	U325-6, U325-15, U332-11
U325-15 = P	(VB1)	U320-6
U329-2 = P	(VB1)	U329-3, U329-9
U329-3 = P	(VB1)	U321-2
U329-4 = P	(VB1)	U321-5
U329-5 = P	(VB1)	U392-4, U329-9
U329-9 = P	(VB1)	See VIDEO TIMING and CONTROL TESTS.
U329-10 = P	(VB1)	U329-11, U329-9
U329-11 = P	(VB1)	U337-14
U329-12 = P	(VB1)	U329-13, U329-9
U329-13 = P	(VB1)	U337-15
U329-14 = P	(VB1)	U337-16
U329-15 = P	(VB1)	U329-14, U329-9
U330-13 = P	(VB1)	U330-21, VIDEO I/O TESTS. If the unit passes these tests, then replace U330, U338, and U331.
U330-19 = P	(VB1)	U330-21, VIDEO I/O TESTS.
U330-21 = P	(VB1)	U344-3
U330-39 = P	(VB1)	U331-21, VIDEO I/O TESTS. If the unit passes these tests, then replace U330, U338, and U331.
U330-40 = P	(VB1)	U330-21, VIDEO I/O TESTS. If the unit passes these tests, then replace U330, U338, and U331.

U332-11 = P (VB1)	See VIDEO TIMING and CONTROL TESTS.
U337-1 = L (VB1)	U345-2
U337-2 = L (VB1)	U345-3
U337-3 = L (VB1)	U345-4
U337-4 = H (VB1)	U345-5
U337-5 = P (VB1)	U321-15
U337-6 = P (VB1)	U321-10
U337-7 = H/P (VB1)	If the unit is a monochrome H/Z-100, then U337-7=H; replace U337. Otherwise, if the unit is color, U337-7=P. If not, check U325-13.
U337-8 = P (VB1)	U301-13
U337-9 = H/P (VB1)	If the unit is a monochrome H/Z-100, then U337-9=H; replace U337. Otherwise, if the unit is color, then U337-9=P. If not, check U303-13.
U337-14 = P (VB1)	U337-1, U337-5, U337-6, U337-7, U337-4
U337-15 = P (VB1)	U337-2, U337-5, U337-6, U337-8, U337-4
U337-16 = P (VB1)	U337-3, U337-5, U337-6, U337-9, U337-4
U344-1 = P (VB1)	See VIDEO TIMING and CONTROL TESTS.
U344-2 = P (VB1)	See VIDEO TIMING and CONTROL TESTS.
U344-3 = P (VB1)	U344-1, U344-2
U344-8 = P (VB1)	U344-9, U344-10
U344-9 = P (VB1)	See VIDEO TIMING and CONTROL TESTS.
U344-10 = P (VB1)	See VIDEO TIMING and CONTROL TESTS.
U345-2 = L (VB1)	Perform the VIDEO I/O TESTS. If the unit passes these tests, then replace U345, U338, and U331.
U345-3 = L (VB1)	Perform the VIDEO I/O TESTS. If the unit passes these tests, then replace U345, U338, and U331.
U345-4 = L (VB1)	Perform the VIDEO I/O TESTS. If the unit passes these tests, then replace U345, U338, and U331.
U345-5 = H (VB1)	Perform the VIDEO I/O TESTS. If the unit passes these tests, then replace U345, U338, and U331.
U355-12 = P (VB3)	U329-2
U355-13 = P (VB3)	U329-5

VIDEO TIMING AND CONTROL TESTS

TEST #1

- Check for dot clock pulses at U344-11, U344-6, and U368-11. If missing, replace U344 or U368 (VB1).
- Check for pulses at pins 1 through 9 and 11 through 13 of U376. If any of these are missing, check U336, U343, and U367. Check the reset and dot clock lines to these ICs (VB1).
- Perform the following test.

CHECK	IF NOT OKAY, CHECK
*U377-4 = L (VB1)	U377-6

Go to Test #2.

U355-2 = L (VB1)	U355-13
U355-3 = L (VB1)	U355-2, or open on U355-1
U355-11 = H (VB1)	U371 or U377 defective.
U355-13 = L (VB1)	U355-11
U361-1 = L (VB1)	U355-3
U361-6 = H (VB1)	U361-1
U377-6 = H (VB1)	U361-6

=====

TEST #2

-- Press the CTRL/RESET keys. You should get the following logic states. Those shown in parenthesis will pulse one or more times when you release reset.

CHECK	IF NOT OKAY, CHECK
-------	--------------------

*U377-4 = (L) (VB1)	U377-5, U377-6
---------------------	----------------

Go to Test #3.

U355-2 = (L) (VB1)	U379-13
U355-3 = (L) (VB1)	U355-2
U361-1 = (L) (VB1)	U355-3
U361-2 = (L) (VB1)	U379-13
U361-3 = P (VB1)	Open foil run to U367-5.
U361-5 = (L) (VB1)	U361-2, U361-3, U361-1
U361-6 = (H) (VB1)	U361-2, U361-3, U361-1
U361-9 = (L) (VB1)	U361-12, U361-11, U361-13
U361-11 = P (VB1)	Open foil run to U367-15.
U361-13 = (L) (VB1)	U355-3
U361-12 = (L) (VB1)	U361-5
U377-5 = (L) (VB1)	U361-9
U377-6 = (H) (VB1)	U361-6
U378-1 = H (VB1)	U378 defective.
U378-2 = H (VB1)	Open foil run to P305-69.
U378-3 = L (VB1)	Open foil run to P305-70.
U378-5 = L (VB1)	U378-2, U378-3, U378-1
U379-1 = H (VB1)	U379-2, U379-3
U379-2 = L (VB1)	U378-5
U379-3 = (L) (VB1)	Open foil run to P305-71.
U379-13 = (L) (VB1)	U379-12, U379-11
U379-11 = (H) (VB1)	U371 or U377 defective.
U379-12 = H (VB1)	U379-1

TEST #3

- Check for logic zero at U346-1 (VB2). If missing, check U366-3 and U345-39 on VB1. If U345 appears defective, perform the VIDEO I/O TESTS before replacing the IC.
 - Check for logic one at U346-11 (VB2). If missing, trace it back to U345-19 (VB1). If U345 appears defective, perform the VIDEO I/O TESTS before replacing the IC.
 - Check for pulses on pins 12 through 19 on U346 (VB2). If any are missing, check the appropriate input pin (2 through 9) and trace back to P304 and P305. Otherwise replace U346.
- Perform the following tests.

CHECK	IF NOT OKAY, CHECK
*U353-3 = H (VB2)	U374-11
*U353-4 = P (VB2)	U375-8
*U353-15 = P (VB2)	U375-6

End of test. If testing a color unit, go to Test #4.

U345-7 = L (VB1)	See VIDEO I/O TESTS.
U345-39 = H (VB1)	See VIDEO I/O TESTS.
U350-3 = H (VB2)	U371 or U377 defective.
U350-4 = L (VB2)	U345-7
U350-5 = L (VB2)	Open foil run to U377-4.
U350-6 = H (VB2)	U350-3, U350-4, U350-5
U351-4 = L (VB2)	Open foil run to U377-4.
U351-5 = L (VB2)	U366-3
U351-6 = L (VB2)	U351-4, U351-5
U366-3 = L (VB1)	U366-17
U366-17 = H (VB1)	U345-39
U374-11 = H (VB2)	U374-13
U374-13 = L (VB2)	U351-6

U375-5 = P	(VB2)	U376-15
U375-6 = P	(VB2)	U375-5
U375-8 = P	(VB2)	U375-9, U375-10
U375-9 = H	(VB2)	U350-6
U375-10 = P	(VB2)	U376-14
		U376 defective.
U376-14 = P	(VB1)	U376 is defective.
U376-15 = P	(VB1)	

TEST #4

-- For color units, perform the following.

<u>CHECK</u>	<u>IF NOT OKAY, CHECK</u>
*U352-4 = P (VB2)	U375-11
*U352-15 = P (VB2)	U375-3
*U354-4 = P (VB2)	U374-8
*U354-10 = P (VB2)	U374-6

End of test.

U345-6 = L (VB1)	See VIDEO I/O TESTS.
U345-8 = L (VB1)	See VIDEO I/O TESTS.
U350-1 = H (VB2)	U371 or U377 is defective.
U350-2 = L (VB2)	U345-6
U350-8 = H (VB2)	U350-9, U350-10, U350-11
U350-9 = H (VB2)	U371 or U377 is defective.
U350-10 = L (VB2)	U345-8
U350-11 = L (VB2)	Open foil run to U377-4.
U350-12 = H (VB2)	U350-1, U350-2, U350-13
U350-13 = L (VB2)	Open foil run to U377-4.
U374-5 = P (VB2)	U376-15
U374-6 = P (VB2)	U374-5
U374-8 = P (VB2)	U374-9, U374-10
U374-9 = H (VB2)	U350-8
U374-10 = P (VB2)	U376-14
U375-2 = P (VB1)	U376-15
U375-3 = P (VB2)	U375-2
U375-11 = P (VB2)	U375-12, U375-13
U375-12 = H (VB2)	U350-12
U375-13 = P (VB2)	U376-14
U376-14 = P (VB1)	U376 is defective.
U376-15 = P (VB1)	U376 is defective.

VIDEO I/O TESTS

Press and release the CTRL/RESET keys as you make the following tests. A logic state in parenthesis indicates the line under test will pulse one or more times upon release of RESET.

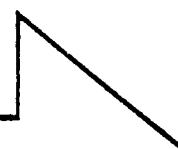
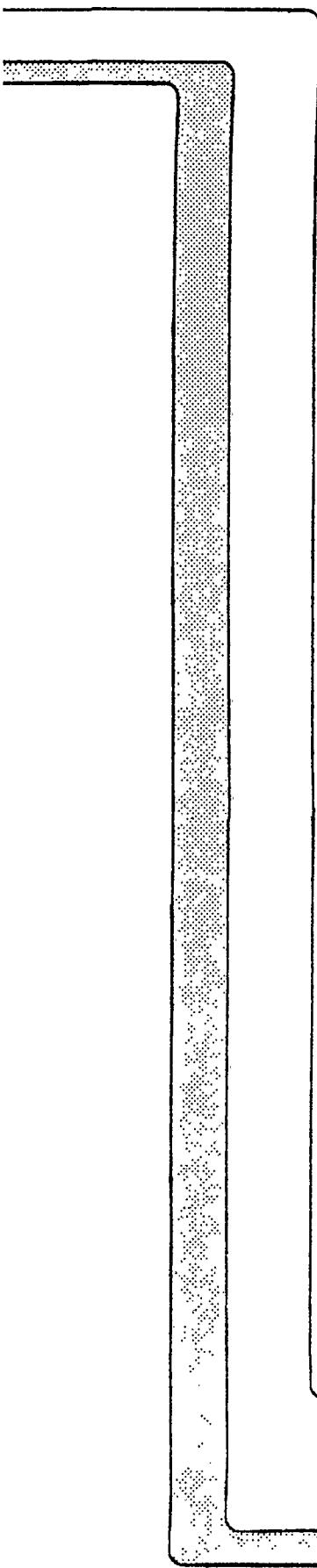
CHECK	IF NOT OKAY, CHECK
*U330-25 = (H) (VB1)	U369-12
*U331-13 = (H) (VB1)	U366-14
*U345-23 = (H) (VB1)	U369-11
*U372-13 = (H) (VB1)	U369-9

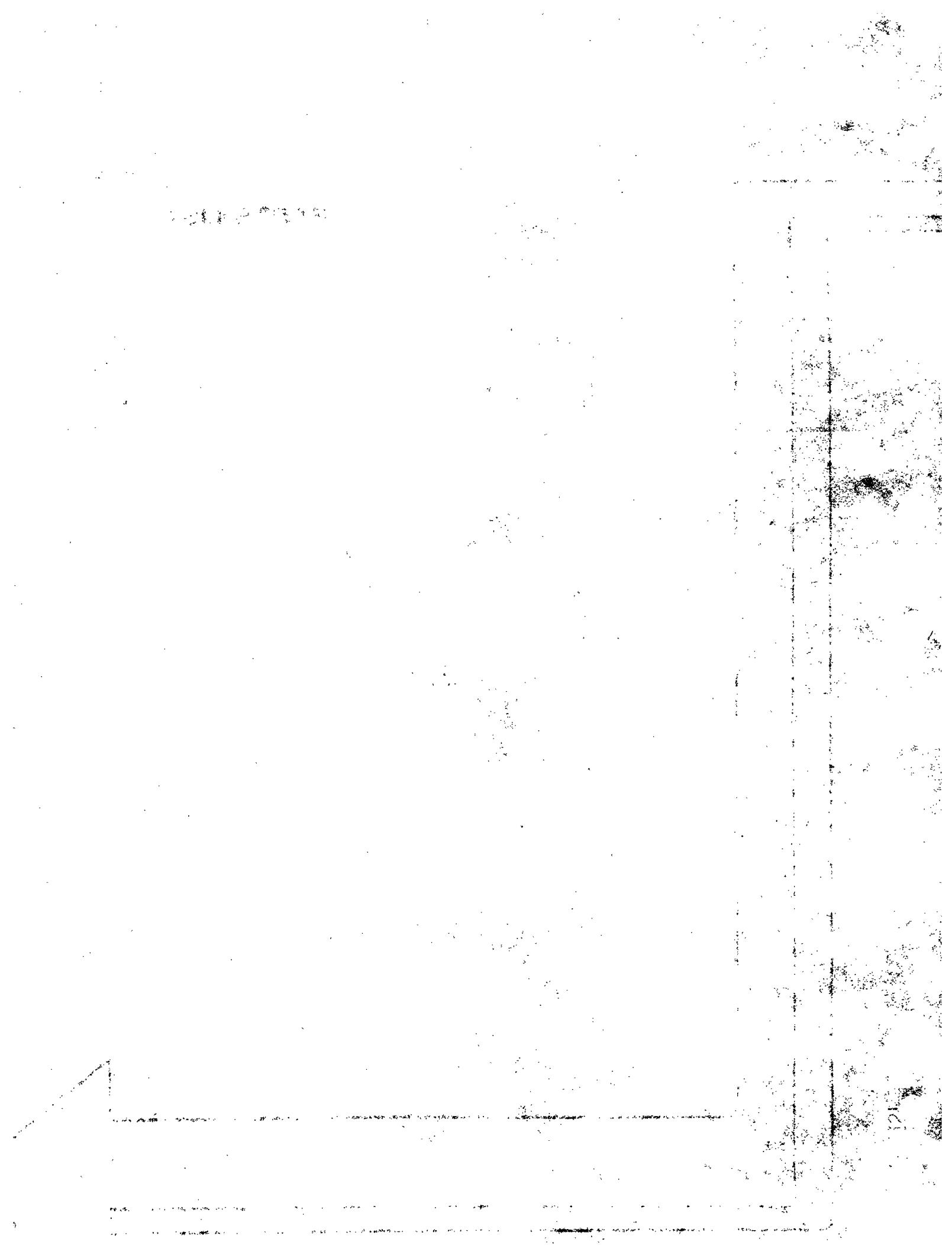
End of test.

U336-6 = (L) (VB1)	U372-6
U336-14 = (H) (VB1)	U366-6
U369-9 = (H) (VB1)	Check continuity on pins 1-7, 14, and 15 of U369.
U369-11 = (H) (VB1)	Check continuity on pins 1-7, 14, and 15 of U369
U369-12 = (H) (VB1)	Check continuity on pins 1-7, 14, and 15 of U369.
U372-6 = (L) (VB1)	U372-9, U372-10
U372-9 = (H) (VB1)	U369-12
U372-10 = (H) (VB1)	U369-11

TROUBLESHOOTING NOTES:

PARTS LIST





CIRCUIT Comp. No.	DESCRIPTION (HE 181-3267)	HEATH Part No.	DESCRIPTION (HE 181-3267)
VIDEO BOARD PART LIST			
33001	180 pF ceramic	HE 21-746	1 uF ceramic
33002	180 pF ceramic	HE 21-746	.1 uF ceramic
33003	.1 uF ceramic	HE 21-762	.1 uF ceramic
33004	10 uF electrolytic	HE 25-820	.1 uF ceramic
33005	.1 uF ceramic	HE 21-762	.1 uF ceramic
33006	.1 uF ceramic	HE 21-762	.1 uF ceramic
33007	.1 uF ceramic	HE 21-762	.1 uF ceramic
33008	10 uF electrolytic	HE 25-820	.1 uF ceramic
33009	.1 uF ceramic	HE 21-762	.1 uF ceramic
33110	.1 uF ceramic	HE 21-762	.1 uF ceramic
33111	.1 uF ceramic	HE 21-762	.1 uF ceramic
33112	.1 uF ceramic	HE 21-762	.1 uF ceramic
33113	.1 uF ceramic	HE 21-762	.1 uF ceramic
33114	.1 uF ceramic	HE 21-762	.1 uF ceramic
33115	.1 uF ceramic	HE 21-762	.1 uF ceramic
33116	.1 uF ceramic	HE 21-762	.1 uF ceramic
33117	.1 uF ceramic	HE 21-762	.1 uF ceramic
33118	.1 uF ceramic	HE 21-762	.1 uF ceramic
33119	.1 uF ceramic	HE 21-762	.1 uF ceramic
3320	.1 uF ceramic	HE 21-762	.1 uF ceramic
3321	.1 uF ceramic	HE 21-762	.1 uF ceramic
3322	.1 uF ceramic	HE 21-762	.1 uF ceramic
3323	.1 uF ceramic	HE 21-762	.1 uF ceramic
3324	.1 uF ceramic	HE 21-762	.1 uF ceramic
3325	.1 uF ceramic	HE 21-762	.1 uF electro
3326	.1 uF ceramic	HE 21-762	.47 uF
3327	.1 uF ceramic	HE 21-762	.1 uF ceramic
3328	.1 uF ceramic	HE 21-762	The following capacitor
3329	.1 uF ceramic	HE 21-762	and are located on the
3330	.1 uF ceramic	HE 21-762	location see Visual Che
3331	.1 uF ceramic	HE 21-762	180 pF ceram
3332	.1 uF ceramic	HE 21-762	180 pF ceram
3333	.1 uF ceramic	HE 21-762	180 pF ceram
3334	.1 uF ceramic	HE 21-762	
3335	.1 uF ceramic	HE 21-762	
3336	10 uF electrolytic	HE 25-820	
3337	.1 uF ceramic	HE 21-762	
3338	.1 uF ceramic	HE 21-762	
3339	.1 uF ceramic	HE 21-762	
INDUCTORS			
L301		1.22 uH	
L302		35 uH	
L303		35 uH	
L304		35 uH	

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
RESISTORS		
R301	none	
R302	jumper	
R303	1000 ohm	1/4 watt, 5%
R304	47 ohm	1/4 watt, 5%
R305	1000 ohm	1/4 watt, 5%
R306	27 ohm	1/4 watt, 5%
R307	100 ohm control	HE 6-102-1
R308	620 ohm	1/4 watt, 5%
R309	220 ohm	1/4 watt, 5%
R310	110 ohm	1/4 watt, 5%
R311	33 ohm	1/4 watt, 5%
R312	47 ohm	1/4 watt, 5%
R313	27 ohm	1/4 watt, 5%
R314	39 ohm	1/4 watt, 5%
R315	62 ohm	1/4 watt, 5%
R316	27 ohm	1/4 watt, 5%
R317	1000 ohm	1/4 watt, 5%
R318	1000 ohm	1/4 watt, 5%
R319	10 kilohm	1/4 watt, 5%
R320	10 kilohm	1/4 watt, 5%
R321	1000 ohm	1/4 watt, 5%
R322	4700 ohm	1/4 watt, 5%
R323	1000 ohm	1/4 watt, 5%
R324,	1000 ohm	1/4 watt, 5%
R325	1000 ohm	1/4 watt, 5%
RESISTOR PACKS		
RP301	1000 ohm	HE 9-99
RP302	10 kilohm	HE 9-128
RP303	4.7 kilohm	HE 9-124
RP304	4.7 kilohm	HE 9-124
RP305	33 ohm	HE 9-93
RP306	33 ohm	HE 9-93
RP307	1000 ohm	HE 9-99

PARTS LIST

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CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.	CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
INTEGRATED CIRCUITS					
U301	74LS166	HE 413-892	U342	MCM66330 (optional)	HE 413-1106*
U302	74LS273	HE 413-805	U343	74S175	HE 413-983
U303	74LS166	HE 413-882	U344	74S86	HE 413-915
U304	MCM66330 (optional)	HE 413-1106*	U345	68A21	HE 413-1014
U305	MCM66330 (optional)	HE 413-1106*	U346	HAL10H8	HE 414-133
U306	MCM66330 (optional)	HE 413-1106*	U347	MCM66330 (optional)	HE 413-1106*
U307	74LS244	HE 413-791	U348	MCM66330 (optional)	HE 413-1106*
U308	7406	HE 413-967	U349	MCM66330 (optional)	HE 413-1106*
U309	74LS273	HE 413-805	U350	74LS10	HE 413-797
U310	74LS373	HE 413-837	U351	74LS32	HE 413-975
U311	74LS273	HE 413-805	U352	MCM66330 (optional)	HE 413-1106*
U312	MCM66330 (optional)	HE 413-1106*	U353	MCM66330 (optional)	HE 413-1106*
U313	MCM66330 (optional)	HE 413-1106*	U354	MCM66330 (optional)	HE 413-1106*
U314	MCM66330 (optional)	HE 413-1106*	U355	74ALS74	HE 413-975
U315	74LS374	HE 413-863	U356	74ALS74	HE 413-1051
U316	74LS373	HE 413-837	U357	74LS157	HE 413-799
U317	MCM66330 (optional)	HE 413-1106*	U358	74LS157	HE 413-799
U318	MCM66330 (optional)	HE 413-1106*	U359	74LS157	HE 413-799
U319	MCM66330 (optional)	HE 413-1106*	U360	74ALS241	HE 413-1057
U320	74LS86	HE 413-891	U361	74ALS74	HE 413-1051
U321	74LS174	HE 413-879	U362	74ALS74	HE 413-1051
U322	7406	HE 413-967	U363	74ALS157	HE 413-799
U323	74LS259	HE 413-804	U364	74LS253	HE 413-855
U324	74LS169	HE 413-1054	U365	74LS283	HE 413-855
U325	74LS166	HE 413-892	U366	74LS210	HE 413-754
U326	MCM66330 (optional)	HE 413-1106*	U367	74S174	HE 413-1053
U327	MCM66330 (optional)	HE 413-1106*	U368	14.112 MHz oscillator	HE 150-134
U328	MCM66330 (optional)	HE 413-1106*	U369	82S129 PROM	HE 414-103
U329	74LS174	HE 413-1053	U370	TBP18S22 PROM	HE 414-127
U330	68A45	HE 413-1013	U371	82S129 PROM	HE 414-102
U331	74LS273	HE 413-1058	U372	74ALS37	HE 413-1049
U332	MCM66330 (optional)	HE 413-805	U373	74ALS37	HE 413-1057
U333	MCM66330 (optional)	HE 413-1106*	U374	74ALS37	HE 413-1049
U334	MCM66330 (optional)	HE 413-1106*	U375	74ALS37	HE 413-1049
U335	MCM66330 (optional)	HE 413-1106*	U376	74ALS28	HE 414-114
U336	74S175	HE 413-983	U377	74ALS28	HE 413-1048
U337	HAL14H4	HE 414-115	U378	74ALS74	HE 413-1051
U338	74LS541	HE 413-1058	U379	74ALS02	HE 413-1045
U339	74LS373	HE 413-837			
U340	MCM66330 (optional)	HE 413-1106*			
U341	MCM66330 (optional)	HE 413-1106*			

* MCM66330 ICs will be installed on the color versions of the video board while MCM6665 (413-970) ICs will be installed on the B/W versions. A further explanation of this is given in Configuration.

BACKUP Source File Limit

There is a limit to the number of files that you can back up during a BACKUP operation. If you exceed this limit, the BACKUP operation will be aborted and the following error message will be displayed:

You have specified too many files for BACKUP sources.

Enter more than one BACKUP command to specify these files,
or enter a single BACKUP command specifying fewer files as BACKUP sources.

A:

If this error message appears, follow the instructions in the message.

This error condition can occur if you specify more than 1300 files in a BACKUP command. Specifying this many files is unlikely, but possible if you are backing up the files from several disks and/or partitions during the same BACKUP operation.

MAKE Drive Specification

The MAKE utility supplied with this version of Z-DOS copies files under the assumption that the source drive is the default drive (the drive that is named in the system prompt). With earlier MAKE versions, drive A was always assumed to be the source drive.

The MAKE utility supplied with this version of Z-DOS also prompts you to specify the name of the drive that you wish to be the destination drive if you do not specify the destination drive in the MAKE command line. With earlier MAKE versions, drive B was assumed to be the destination drive if you did not specify the destination drive in the MAKE command line.

Therefore, before you begin a MAKE operation, you must log in the drive that you wish to be the source drive during the operation so that this intended source drive becomes the default drive.

Furthermore, you must always specify a destination drive. This drive must be a valid drive within your hardware environment. However, you should not specify the same drive as the source drive for this operation (the default drive). You can specify the default drive either by including this drive name in the MAKE command line or by responding to the following prompt:

Drive name for destination diskette (A-F): _:

This prompt will appear only if you did not specify an acceptable drive name in the MAKE command line. You only need to enter the drive letter — no colon or RETURN. If you enter a letter for a drive that does not exist or the letter for the source (default) drive, you will hear a beep and have another opportunity to enter an acceptable drive letter.

When it appears, this prompt follows the

Do you wish to continue? (Y/N) <Y>

prompt and precedes the

Are the destination diskettes single sided? (Y/N) <N>

prompt.

NOTE: The

Are the destination diskettes single sided? (Y/N) <N>

prompt will be displayed during all MAKE operations. If your destination diskette is a Winchester disk partition, respond by pressing **N** or **n** or **RETURN**. If your destination diskette is 8-inch, determine whether this diskette is single-sided or double-sided and respond to the prompt accordingly.