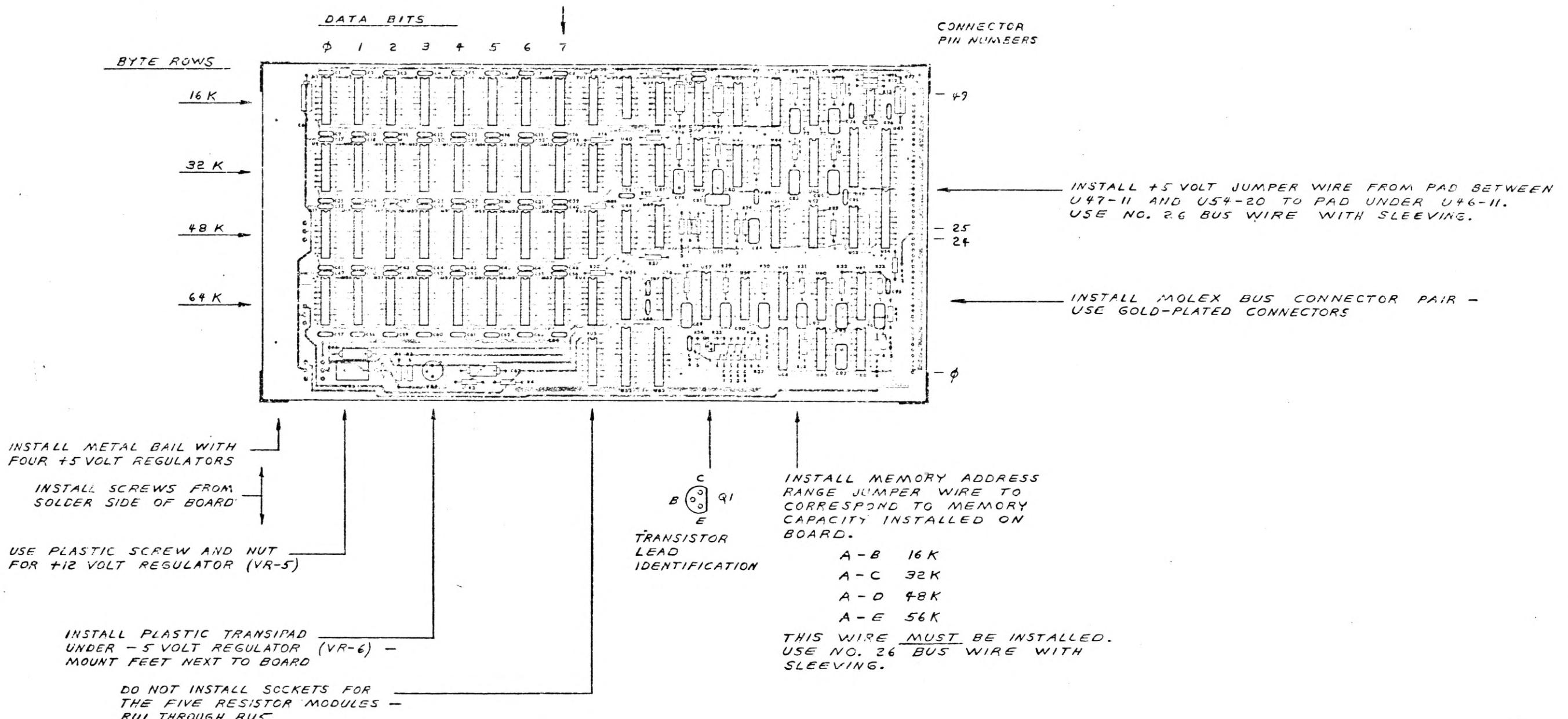


- POPULATE MEMORY STARTING WITH TOP (16K) ROW OF EIGHT MEMORY CHIPS.
- ADD MEMORY CHIPS ONE ROW AT A TIME IN A CONTIGUOUS MANNER TO EXTEND MEMORY CAPACITY. EACH ROW IS AN ADDITIONAL 16 K BYTES. BE SURE TO CHANGE ADDRESSING JUMPER (BELOW) ACCORDINGLY.



CAUTION:

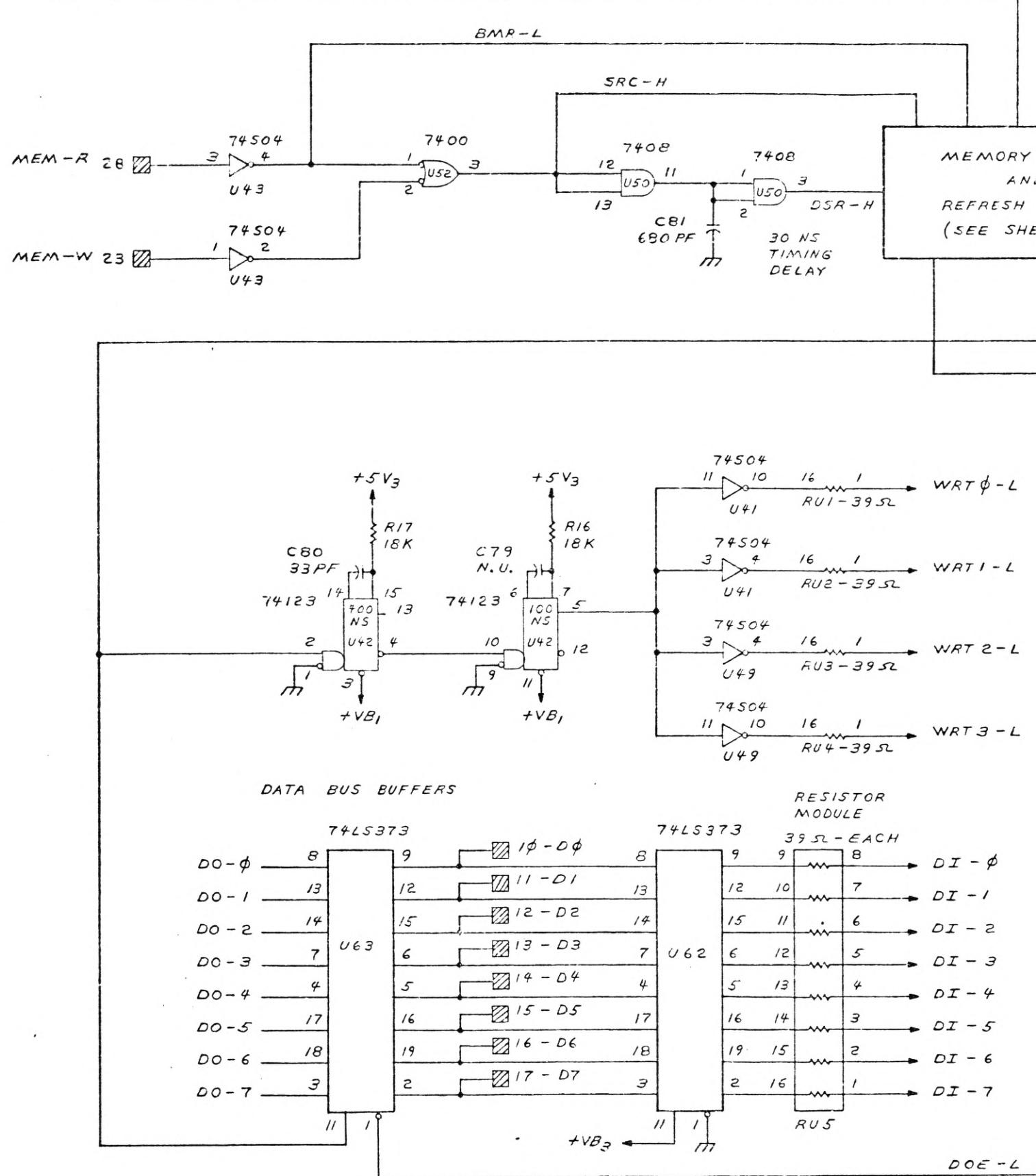
THE MEMORY CHIPS ARE MOS DEVICES AND ARE SUSCEPTABLE TO DAMAGE BY STATIC ELECTRICITY WHILE BEING HANDLED BEFORE INSTALLATION.

CONTRACT NO.	TRIONYX ELECTRONICS	
DRAWN	DWG TITLE	M-H8
CHECK		
ENGR		
PROJ. ENGR		
PROD. DESIGN	SIZE	COL. IDENT NO. DWG NO.
OTHER APPROVALS	D	TE-A-100100
	SCALE:	SHEET 1 OF 1

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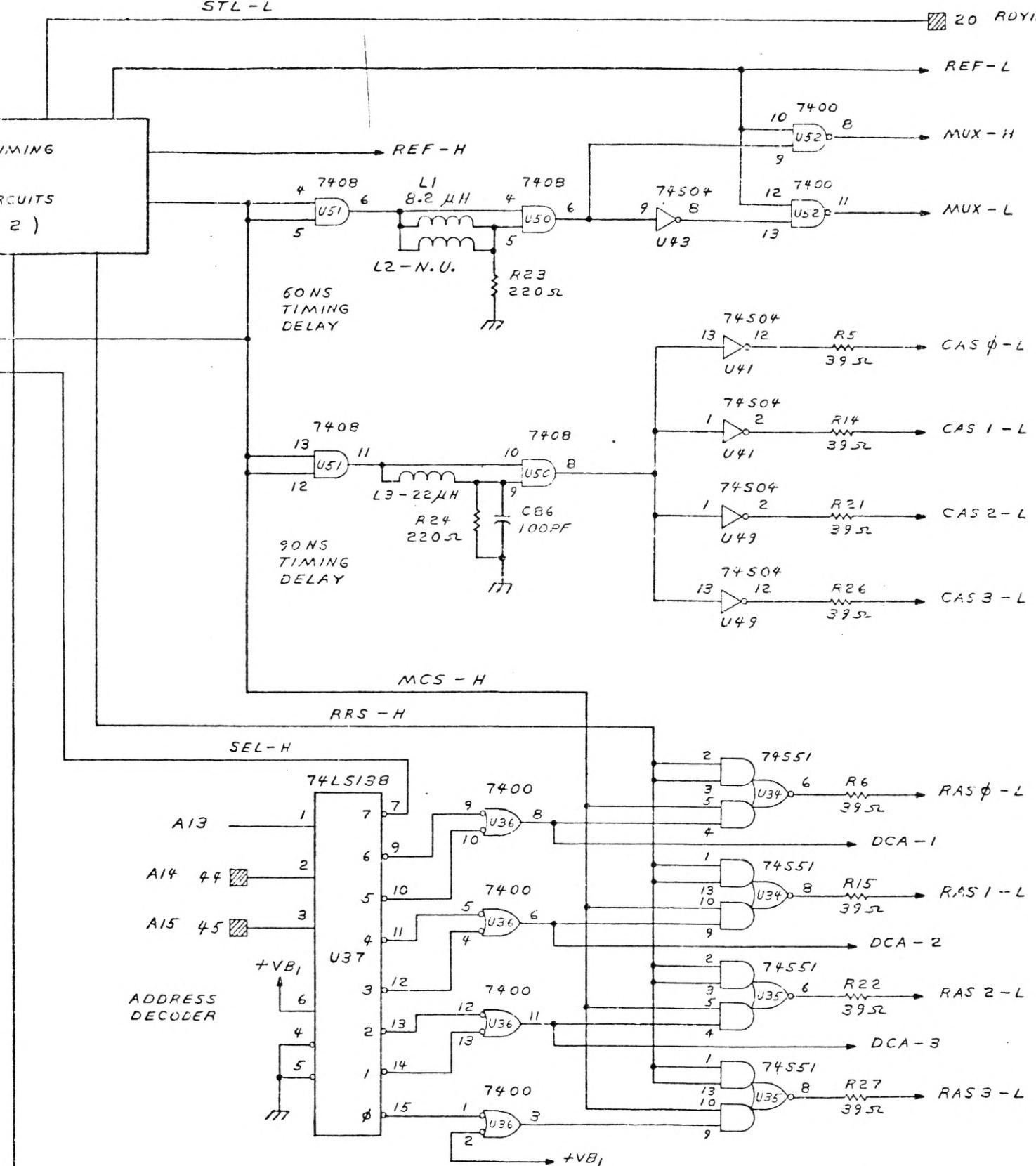
REV. NO.		DESCRIPTION		DATE	APPROVED
ZONE	LTR				

INI-L



MEMORY CONTROL CIRCUITS

STL-L

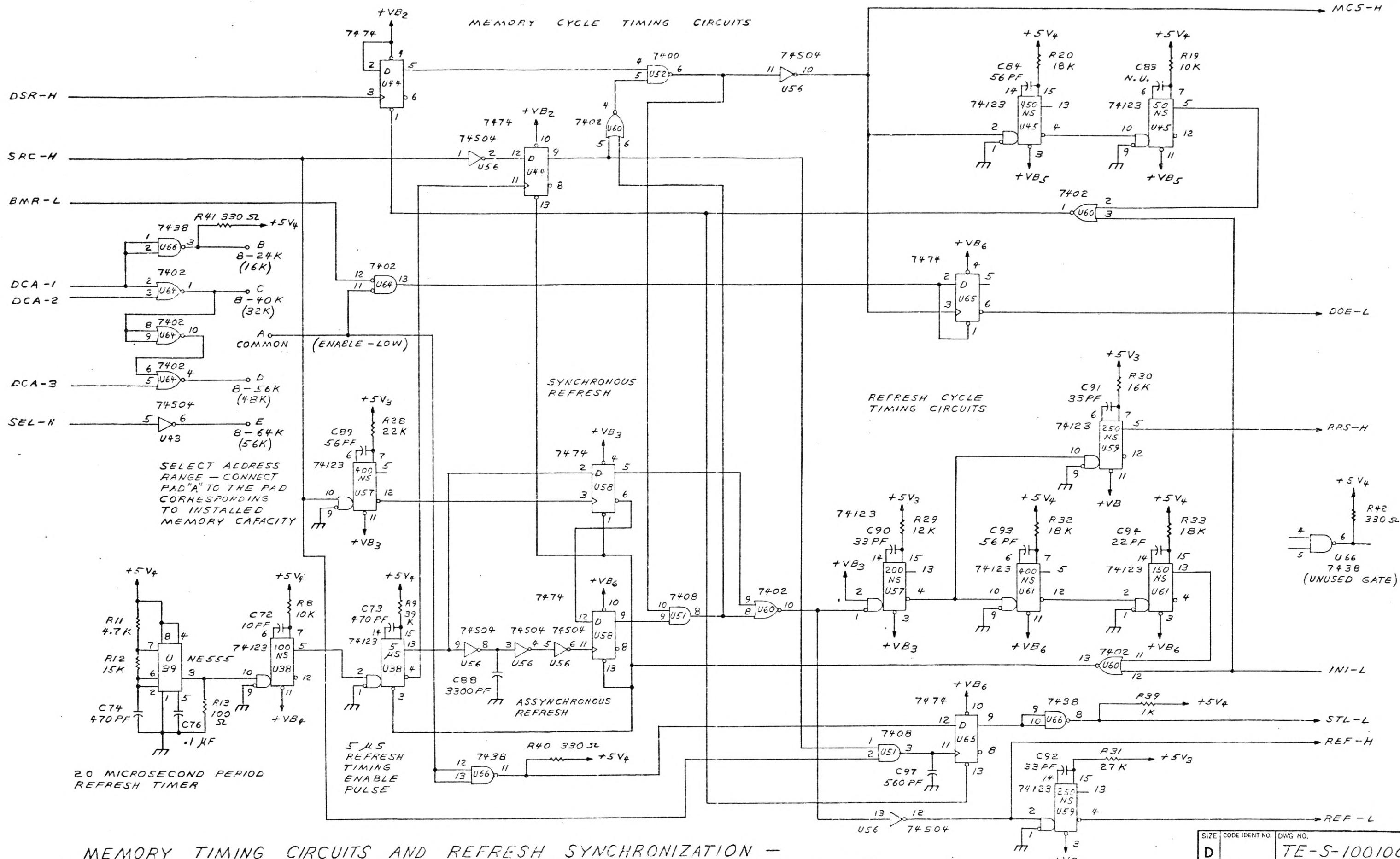


TRIONYX ELECTRONICS

▀ HB BUS CONNECTION
N.U. - NOT USED

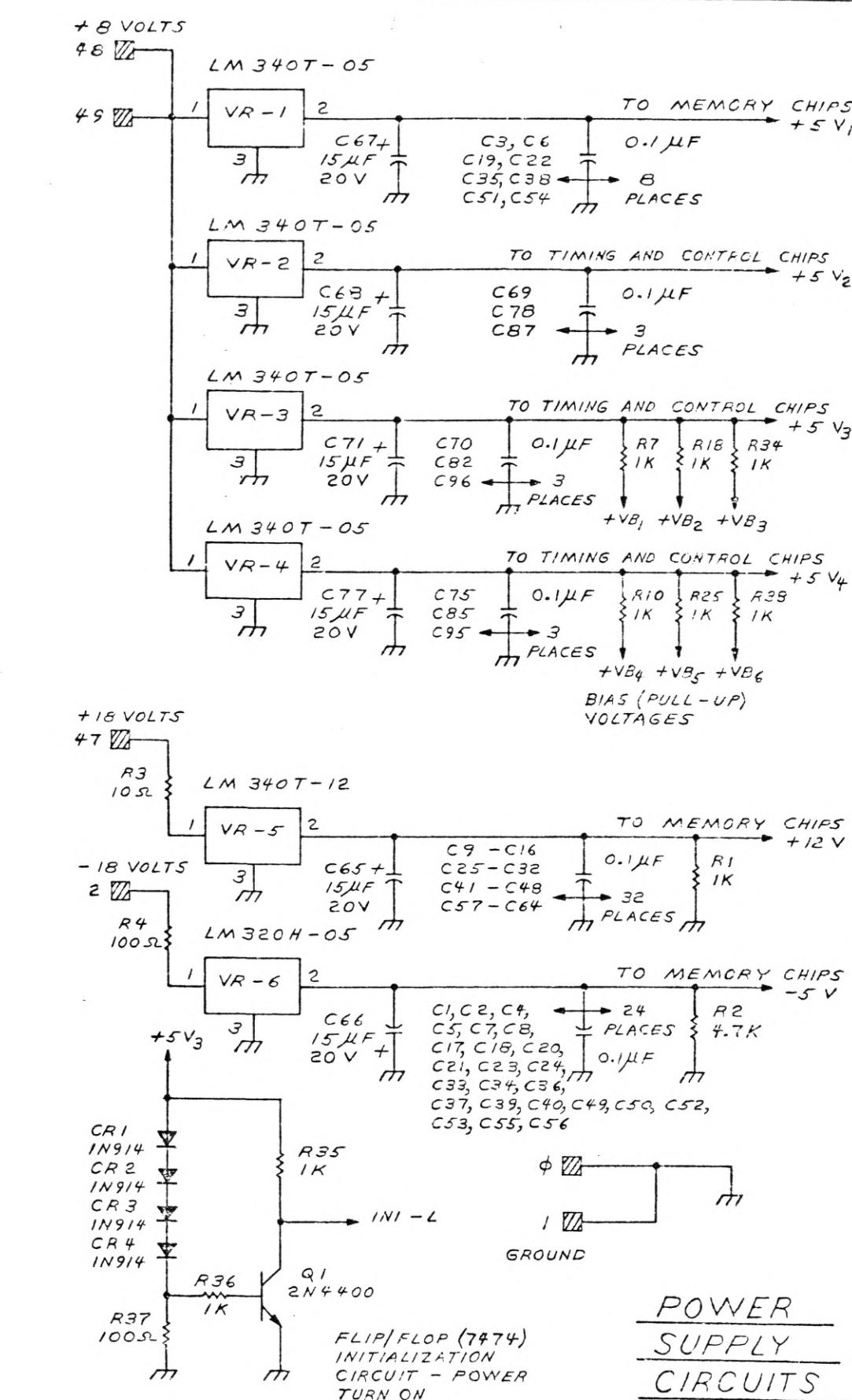
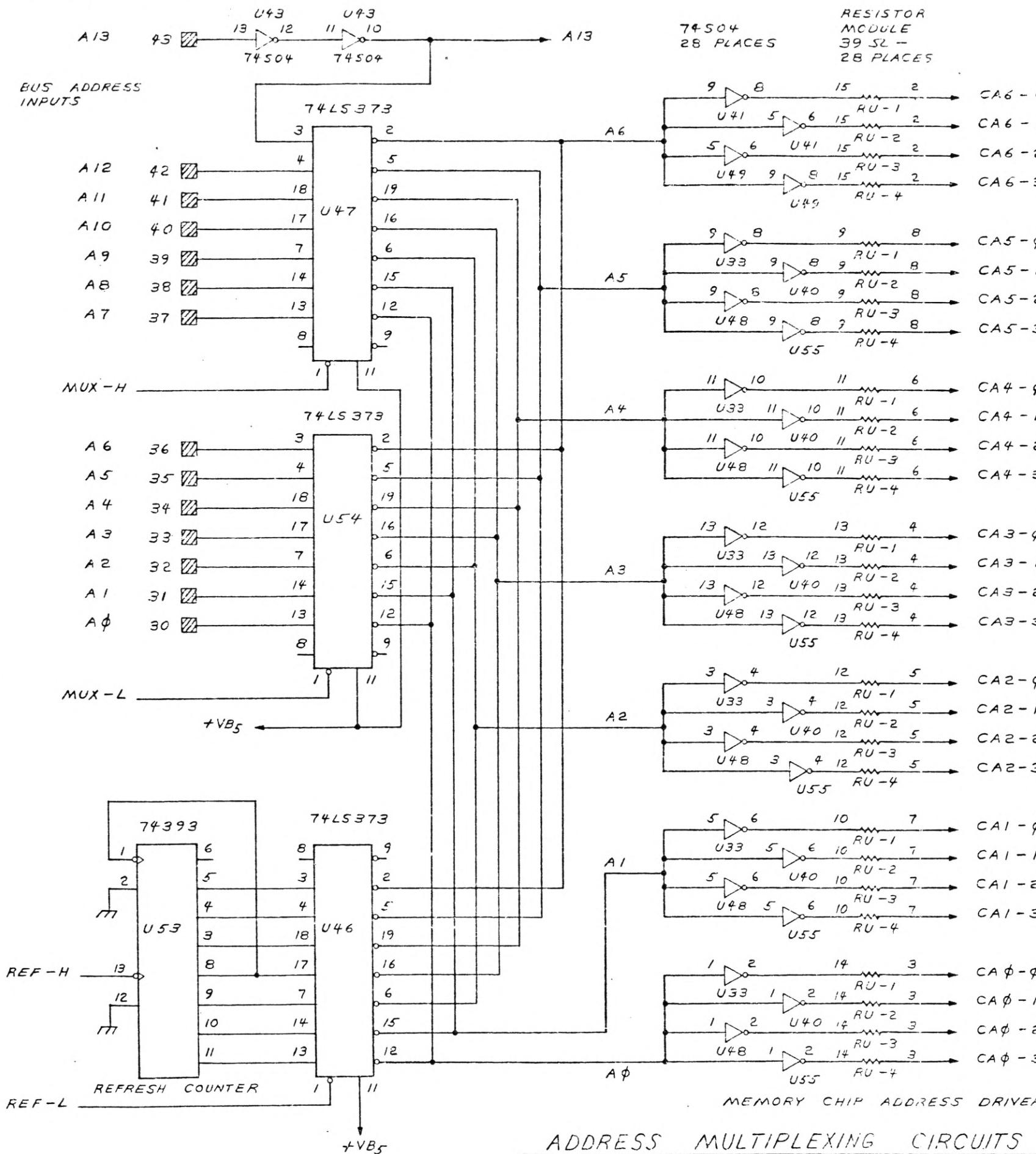
SIZE	CODE IDENT NO.	DWG NO.
D		TE-S-100100
SCALE:		SHEET 1 OF 4

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
/				



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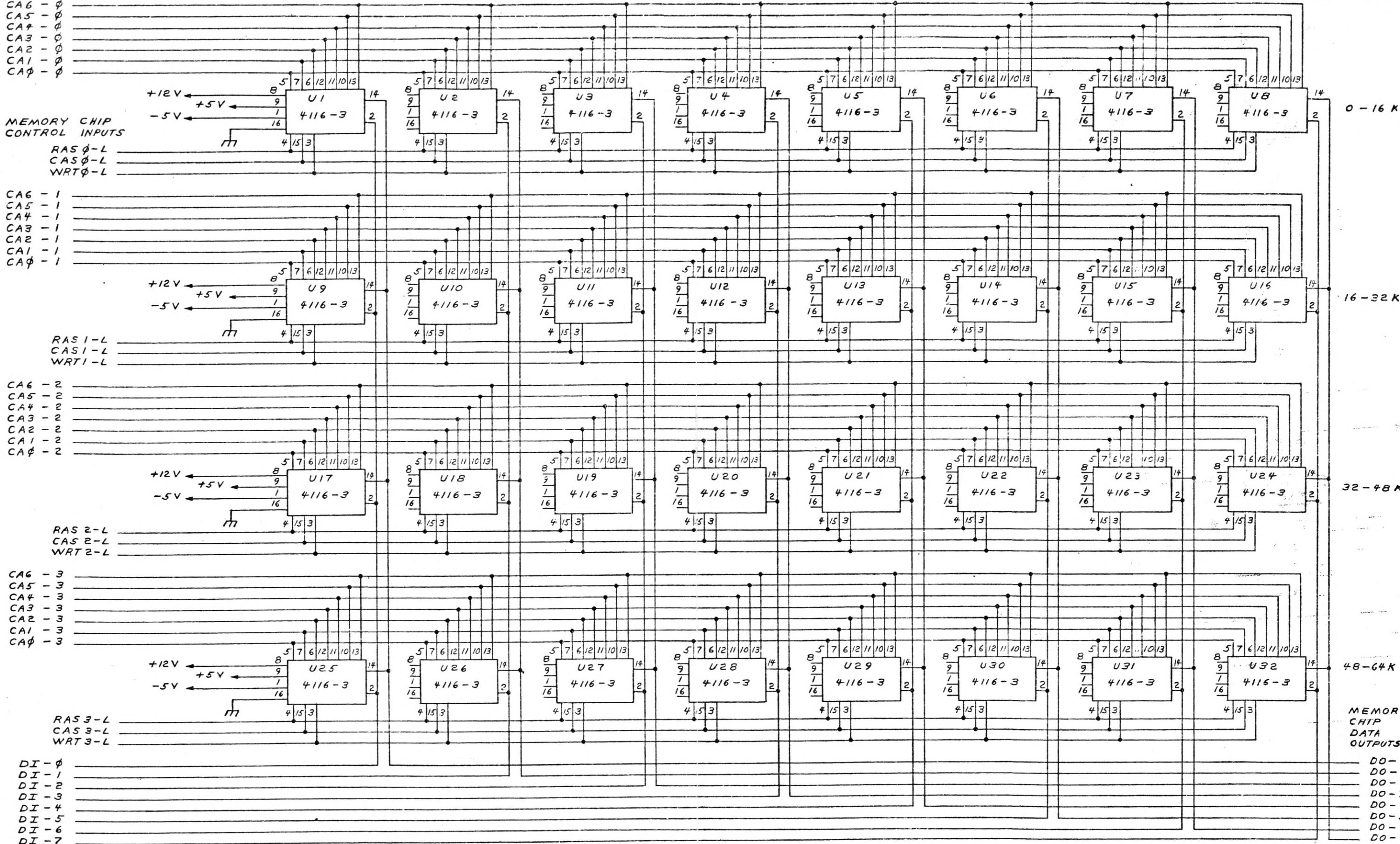
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
/				



POWER SUPPLY CIRCUITS

SIZE D	CODE IDENT NO.	DWG NO. TE-S-100100
SCALE:		SHEET 3 OF 4

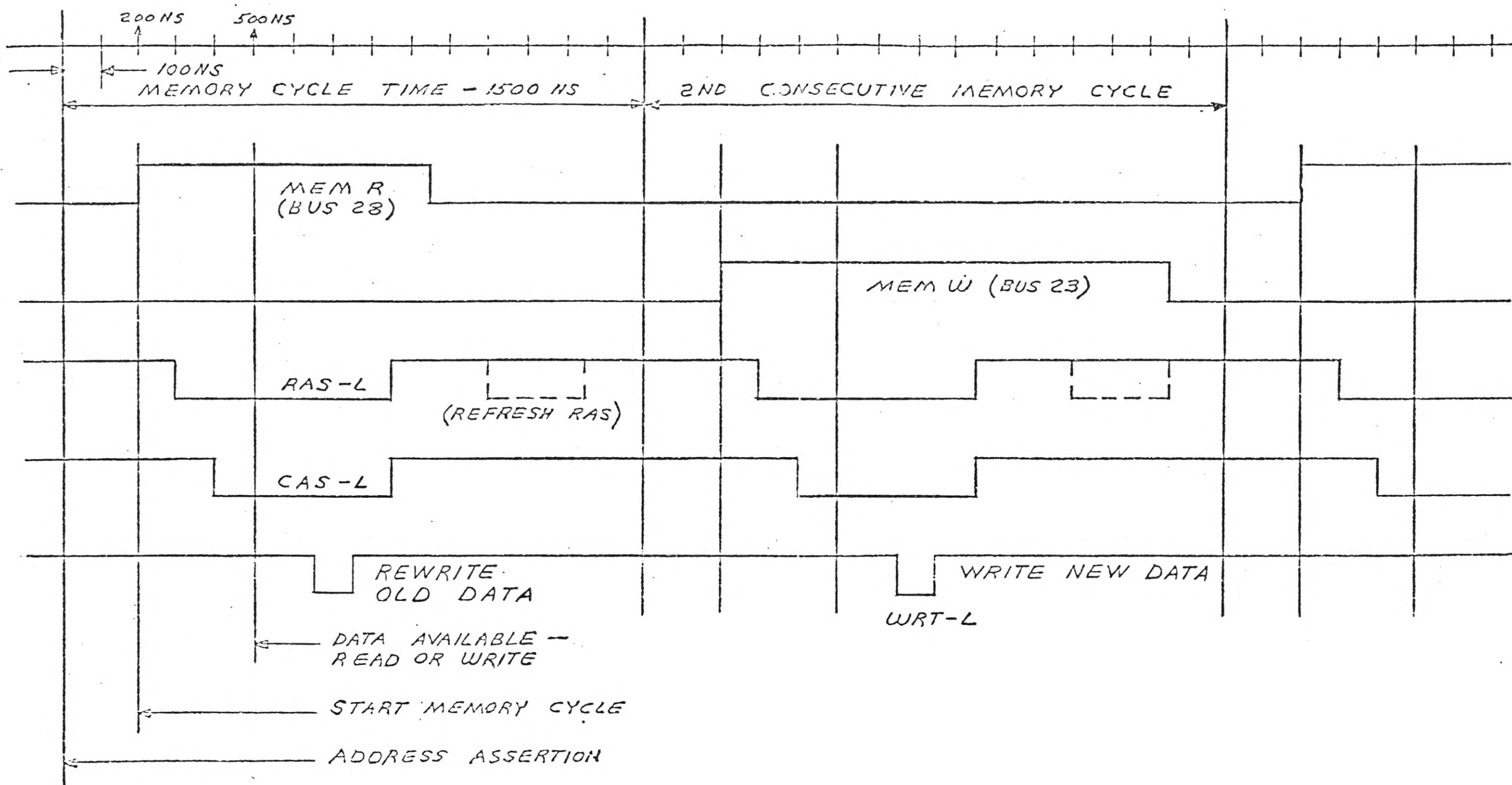
MEMORY CHIP ADDRESS INPUTS



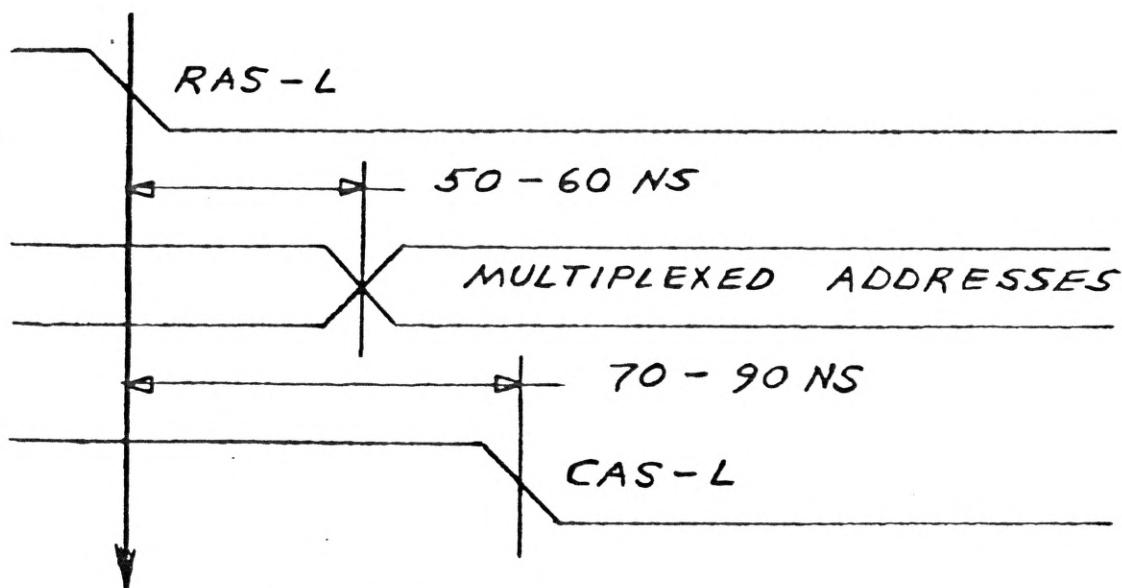
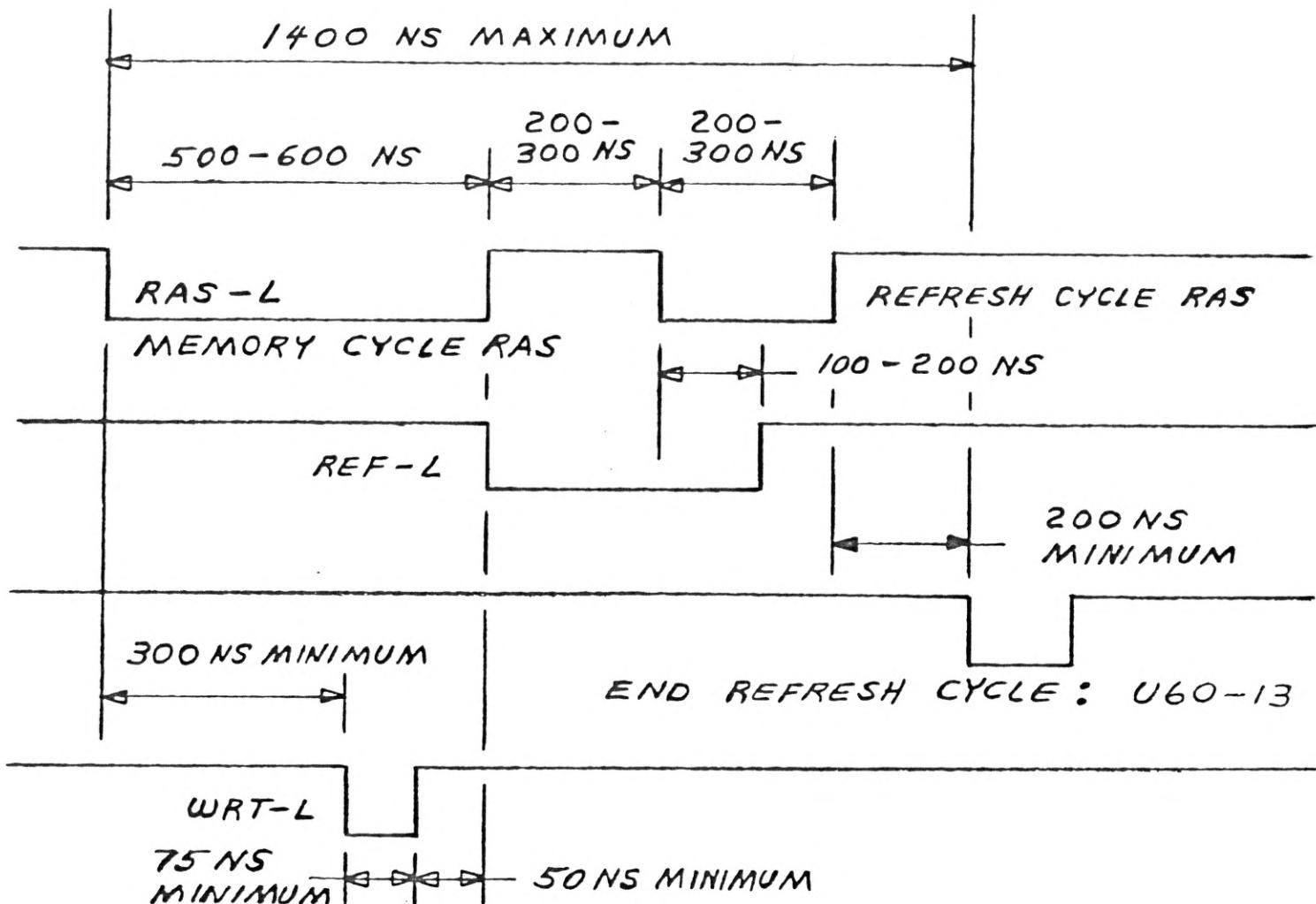
MEMORY CHIP DATA INPUTS

MEMORY DATA STORAGE DEVICE ARRAY (64 K x 8 BITS)

SIZE	CODE IDENT NO.	DWG NO.
D	TE-S-100100	
SCALE:	SHEET 4 OF 4	



MEMORY INTERFACE TIMING RELATIONSHIPS



MEASUREMENTS MADE ON MEMORY CHIP CONTACTS

MEMORY INTERNAL TIMING SPEC.