From Circuit Analysis to State-Space Representation

Organizing KVL/KCL Equations into Matrix Form

What Are "Level 1" and "Level 2"?

Level 1 (Circuit Analysis): Apply Kirchhoff's laws (KVL/KCL) to each component. Results in individual differential equations like "diL1/dt = Vin/L1" or "dvC1/dt = (-iL5)/C1".

Level 2 (State-Space Form): Organize these equations into a structured matrix format: $\dot{x} = A \cdot x + B \cdot u$. This enables systematic analysis using linear algebra tools (eigenvalues, transfer functions, controllability).

Baseline: Standard SEPIC Converter (4th-Order)

A basic SEPIC has 2 inductors (L_1, L_2) and 2 capacitors (C_1, C_out) → 4 state variables

$x = [iL1, vC1, iL2, vout]^T$

$\dot{x} = A \cdot x + B \cdot V_{in}$ (separate A_1, A_2 for switch ON/OFF states)

Why this project needs 9th-order: Two-phase interleaved + bridgeless topology
→ 4 input inductors (L1-L4), 2 output inductors (L5-L6), 3 capacitors (C1, C3, C0) = 9 states

How an Equation Becomes a Matrix Row: Example for dvC1/dt (Topology 11)

Step 1 - Circuit Analysis (Level 1): Apply KCL at C1 node for Topology 11.

Since **C1 and L5 are in series**, we have: **iC1 = iL5**
From capacitor equation: iC1 = C1·(dvC1/dt), therefore: **iL5 = C1·(dvC1/dt)**
Solving for dvC1/dt: **dvC1/dt = iL5/C1**

But in Topology 11, iL5 < 0 (reverse current). To show charging, we write: **dvC1/dt = (-iL5)/C1**

Step 2 - Matrix Form (Level 2): Express as linear combination of all state variables:

$dvC1/dt = 0 \cdot iL1 + 0 \cdot iL2 + 0 \cdot iL3 + 0 \cdot iL4 + (-1/C1) \cdot iL5 + 0 \cdot iL6 + 0 \cdot vC1 + 0 \cdot vC3 + 0 \cdot vC0$

→ **Row 7 of A_{11}:** [0, 0, 0, 0, **-1/C1**, 0, 0, 0, 0]

The coefficient of each state variable becomes a matrix element. This systematic process converts 9 KVL/KCL equations into a 9×9 matrix where each row corresponds to one state variable's derivative.

Our 9th-Order System (4 Topologies)

$x = [iL1, iL2, iL3, iL4, iL5, iL6, vC1, vC3, vC0]^T$

For each topology $k \in \{11, 10, 01, 00\}$:

$\dot{x} = A_k \cdot x + B_k \cdot V_{in} + f_{CPL}(vC0)$

- $\mathbf{A_k}$ = 9×9 system matrix (varies by switch states)
- $\mathbf{B_k}$ = 9×1 input matrix (V_{in} coupling paths)
- $\mathbf{f_{CPL}}$ = $[0, 0, 0, 0, 0, 0, 0, 0, -P/(C0 \cdot vC0)]^T$ (CPL load)

Topology-Specific Matrices

For complete details of all 4 topology matrices (A_{11}, A_{10}, A_{01}, A_{00}), see **Slides 3-7**.
Each topology has its own 9×9 state matrix reflecting different switch configurations and current paths.

Why This Matters: State-space form enables powerful analysis tools: • **Eigenvalue analysis** for stability assessment • **Transfer functions** for controller design (Slides 13-14) • **Averaging across topologies** to capture interleaved operation (Slide 12)