Introducing the Interleaved Bridgeless SEPIC PFC Converter

Understanding Our Advanced Topology

What Makes This Converter Special?

Our converter combines three advanced features to achieve high-efficiency power factor correction:

- **Bridgeless:** Eliminates the input diode bridge rectifier, reducing conduction losses by ~1-2% efficiency gain
- **Interleaved:** Two phases operate with shifted timing, reducing input/output current ripple by ~50%
- **PFC (Power Factor Correction):** Shapes input current to follow input voltage, achieving PF > 0.99 and THD < 5%

Circuit Architecture

Key Components:

- **6 Inductors:** L1, L2 (Phase 2 input), L3, L4 (unused in positive half-cycle), L5, L6 (output inductors)
- **3 Capacitors:** C1 (Phase 1 coupling), C3 (Phase 2 coupling), C0 (output)
- **2 Switches:** S1 (Phase 1), S2 (Phase 2) - actively controlled at ~50 kHz
- **2 Output Diodes:** D7, D8 - passively conduct based on voltage polarities

Standard SEPIC (4th-Order)

- 2 inductors (L_1, L_2)
- 2 capacitors (C_1, C_out)
- 1 switch (S)
- 2 states (ON/OFF)
- Simple to analyze

Our Converter (9th-Order)

- 6 inductors (L1-L6)
- 3 capacitors (C1, C3, C0)
- 2 switches (S1, S2)
- 4 topologies (11, 10, 01, 00)
- Complex but high-performance

Why the Complexity? The increased component count enables: (1) Bidirectional power flow capability, (2) Reduced electromagnetic interference (EMI), (3) Higher efficiency under varying loads, and (4) Better thermal management through distributed heat generation. The trade-off is increased modeling and control complexity, which this presentation addresses systematically.