Topology 00: Both Switches OFF

Maximum Power Transfer Mode - Both Phases Delivering Simultaneously

Circuit Behavior (ASCII Diagram)

```
Phase 1 (S1 OFF - TRANSFER):
Vin(+) → L2 → C1 → L5 → D8 → C0 (output)
         ↓     ↓    ↓    ↓    ↓
           discharge path  - energy transfers to output

Phase 2 (S2 OFF - TRANSFER):
Vin(+) → L1 → C3 → L6 → D7 → C0 (output)
         ↓     ↓    ↓    ↓    ↓
           discharge path  - energy transfers to output

Output: BOTH D7 and D8 conduct → Maximum power delivery
          All 4 active inductors (L1, L2, L5, L6) contribute
```

State Matrix A_{00} (9×9) - CORRECTED

```
A00 = [
  0,      0,      0,      0,      0,      0,       0,      -1/L1,   -1/L1;   % diL1/dt = (Vin-vC3-vC0)/L1
  0,      0,      0,      0,      0,      0,      -1/L2,    0,      -1/L2;   % diL2/dt = (Vin-vC1-vC0)/L2
  0,      0,      0,      0,      0,      0,       0,       0,       0;      % diL3/dt = 0
  0,      0,      0,      0,      0,      0,       0,       0,       0;      % diL4/dt = 0
  0,      0,      0,      0,      0,      0,       0,       0,       1/L5;   % diL5/dt = vC0/L5 (parallel)
  0,      0,      0,      0,      0,      0,       0,       0,       1/L6;   % diL6/dt = vC0/L6 (parallel)
  0,    1/C1,     0,      0,      0,      0,       0,       0,       0;       % dvC1/dt = iL2/C1
 1/C3,    0,      0,      0,      0,      0,       0,       0,       0;       % dvC3/dt = iL1/C3
 1/C0,   1/C0,    0,      0,     1/C0,   1/C0,     0,       0,       0;       % dvC0/dt = (iL1+iL2+iL5+iL6-P/vC0)/C0
];
```

Input Matrix B_{00} and CPL Term

```
B00 = [1/L1; 1/L2; 0; 0; 0; 0; 0; 0; 0]; f_CPL = [0; 0; 0; 0; 0; 0; 0; 0; -P/(C0·vC0)] (nonlinear CPL load term)
```

Key Correction: Row 7 shows **iC1 = iL2**, Row 8 shows **iC3 = iL1**. Row 9 shows **ALL FOUR inductors contribute** to output: dvC0/dt = (iL1 + iL2 + iL5 + iL6 - P/vC0)/C0.

Physical Meaning: This is the highest power transfer mode. Both phases simultaneously deliver energy to the output. All four active inductors (L1, L2, L5, L6) contribute current to C0. This topology occurs when both duty cycles are low enough that switches don't overlap.