

Topology 01: S1 OFF, S2 ON

Phase 1 Transferring, Phase 2 Storing (Symmetric to Topology 10)

Circuit Behavior (ASCII Diagram)

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Phase 1 (S1 OFF - TRANSFER):
Vin(+) → L2 → C1 → L5 → D8 → C0 (output)
      ↓   ↓   ↓   ↓   ↓
      discharge path - energy transfers to output

Phase 2 (S2 ON - STORAGE):
Vin(+) → L1 → C3 ← L6 ← S2 ← GND
      ↓   ↑   ↑
      charges | reverse current continues

Output: D8 conducts → Phase 1 delivers power (L2 + L5)
        D7 reverse biased → Phase 2 isolated
```

State Matrix A_{o1} (9×9) - CORRECTED

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A01 = [
0, 0, 0, 0, 0, 0, 0, 0, 0; % diL1/dt = Vin/L1 (direct path)
0, 0, 0, 0, 0, 0, -1/L2, 0, -1/L2; % diL2/dt = (Vin-vC1-vC0)/L2
0, 0, 0, 0, 0, 0, 0, 0, 0; % diL3/dt = 0
0, 0, 0, 0, 0, 0, 0, 0, 0; % diL4/dt = 0
0, 0, 0, 0, 0, 0, 0, 0, 1/L5; % diL5/dt = vC0/L5 (parallel)
0, 0, 0, 0, 0, 0, 0, -1/L6, 0; % diL6/dt = -vC3/L6
0, 1/C1, 0, 0, 0, 0, 0, 0, 0; % dvC1/dt = iL2/C1
0, 0, 0, 0, 0, -1/C3, 0, 0, 0; % dvC3/dt = (-iL6)/C3
0, 1/C0, 0, 0, 1/C0, 0, 0, 0, 0; % dvC0/dt = (iL2+iL5-P/vC0)/C0
];
```

Input Matrix B_{o1} and CPL Term

```
B01 = [1/L1; 1/L2; 0; 0; 0; 0; 0; 0; 0]; f_CPL = [0; 0; 0; 0; 0; 0; 0; 0; -P/(C0-vC0)] (nonlinear CPL load term)
```

Key Correction: Row 7 shows $iC1 = iL2$ (capacitor receives current from L2 as it discharges). Row 9 shows **both L2 and L5 contribute** to output current: $dvC0/dt = (iL2 + iL5 - P/vC0)/C0$.

Physical Meaning: Symmetric to Topology 10. Phase 2 continues storing (L1, C3, L6 same as Topology 11). Phase 1 transfers energy: L2 discharges through C1→L5→D8 to output. Both L2 and L5 currents contribute to charging C0 while supplying the CPL load.