Topology 10: S1 ON, S2 OFF

Phase 1 Storing, Phase 2 Transferring

Circuit Behavior (ASCII Diagram)

```
Phase 1 (S1 ON - STORAGE):
Vin(+) → L2 → C1 ← L5 ← S1 ← GND
         ↓     ↑    ↑
         charges  | reverse current continues

Phase 2 (S2 OFF - TRANSFER):
Vin(+) → L1 → C3 → L6 → D7 → C0 (output)
         ↓     ↓    ↓    ↓    ↓
           discharge path  - energy transfers to output

Output: D7 conducts → Phase 2 delivers power (L1 + L6)
          D8 reverse biased → Phase 1 isolated
```

State Matrix A_{10} (9×9) - CORRECTED

```
A10 = [
  0,      0,      0,      0,      0,      0,      0,     -1/L1,   -1/L1;   % diL1/dt = (Vin-vC3-vC0)/L1
  0,      0,      0,      0,      0,      0,      0,      0,       0;      % diL2/dt = Vin/L2 (direct path)
  0,      0,      0,      0,      0,      0,      0,      0,       0;      % diL3/dt = 0
  0,      0,      0,      0,      0,      0,      0,      0,       0;      % diL4/dt = 0
  0,      0,      0,      0,      0,      0,     -1/L5,   0,       0;      % diL5/dt = -vC1/L5
  0,      0,      0,      0,      0,      0,      0,      0,       1/L6;   % diL6/dt = vC0/L6 (parallel)
  0,      0,      0,      0,     -1/C1,   0,      0,      0,       0;      % dvC1/dt = (-iL5)/C1
 1/C3,    0,      0,      0,      0,      0,      0,      0,       0;      % dvC3/dt = iL1/C3
 1/C0,    0,      0,      0,      0,     1/C0,    0,      0,       0;      % dvC0/dt = (iL1+iL6-P/vC0)/C0
];
```

Input Matrix B_{10} and CPL Term

```
B10 = [1/L1; 1/L2; 0; 0; 0; 0; 0; 0; 0]; f_CPL = [0; 0; 0; 0; 0; 0; 0; 0; -P/(C0·vC0)] (nonlinear CPL load term)
```

Key Correction: Row 8 shows **iC3 = iL1** (capacitor receives current from L1 as it discharges). Row 9 shows **both L1 and L6 contribute** to output current: dvC0/dt = (iL1 + iL6 - P/vC0)/C0.

Physical Meaning: Phase 1 continues storing (L2, C1, L5 same as Topology 11). Phase 2 transfers energy: L1 discharges through C3→L6→D7 to output. Both L1 and L6 currents contribute to charging C0 while supplying the CPL load.