Model Verification Status

Ensuring Mathematical and Physical Correctness

Circuit Topology Verification

- ✅ All 36 equations derived from first principles (KVL/KCL)
- ✅ Component connections match Vinukumar's paper schematic
- ✅ Diode conduction states verified for each topology
- ✅ Current paths traced and confirmed

Mathematical Consistency

- ✅ Dimensional analysis passed (all equations dimensionally correct)
- ✅ Energy conservation verified (power in ≈ power out at steady state)
- ✅ Matrix dimensions consistent (9×9, 9×1, 9×2)
- ✅ Duty cycle weights sum to 1 for all cases

Physical Plausibility

- ✅ Operating point currents and voltages within realistic ranges
- ✅ L3, L4 correctly inactive during positive half-cycle
- ✅ L5, L6 reverse charging behavior explained and validated
- ✅ CPL effect correctly modeled with negative incremental resistance

Code-Model Correspondence

- ✅ Symbolic matrices in slides correctly aligned with formal derivation and MATLAB implementation
- ✅ Numeric substitution produces convergent solutions
- ✅ Transfer functions have expected pole locations
- ✅ Controller gains yield stable closed-loop response

Pending Validation

- ⏳ Hardware prototype construction (in progress)
- ⏳ Experimental verification of equations
- ⏳ Closed-loop control implementation
- ⏳ Efficiency and THD measurements