System Overview

Converter Topology: 9th-order interleaved bridgeless SEPIC (Single-Ended Primary-Inductor Converter) with Power Factor Correction (PFC) capability

System Order: 9th-order system comprising 6 inductors and 3 capacitors

State Vector Definition

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x = [iL1, iL2, iL3, iL4, iL5, iL6, vC1, vC3, vC0]^T
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Where:

- iL1, iL2: Phase 2 and Phase 1 input inductors (positive cycle)
- iL3, iL4: Phase 1 and Phase 2 input inductors (negative cycle inactive for $V_{in} > 0$)
- iL5, iL6: Phase 1 and Phase 2 output inductors
- vC1, vC3: Phase 1 and Phase 2 coupling capacitors
- vC0: Output (bus) capacitor voltage

Four Switching Topologies

Topology 11 (S1 ON, S2 ON)

Both phases store energy from AC source. Output bus isolated.

Topology 01 (S1 OFF, S2 ON)

Phase 2 stores energy. Phase 1 transfers to output.

Topology 10 (S1 ON, S2 OFF)

Phase 1 stores energy. Phase 2 transfers to output.

Topology 00 (S1 OFF, S2 OFF)

Both phases transfer energy to output simultaneously.

Note: This analysis focuses on the positive half-cycle (V_{in} > 0). Each topology has 9 differential equations, resulting in a complete set of 36 equations (4 topologies × 9 states).