Topology 11: Both Switches ON

Maximum Energy Storage Mode - No Power Transfer to Output

Circuit Behavior (ASCII Diagram)

```
Phase 1 (S1 closed):
Vin(+) → L2 → C1 ← L5 ← S1 ← GND
         ↓      ↑    ↑
         charges  | reverse current builds

Phase 2 (S2 closed):
Vin(+) → L1 → C3 ← L6 ← S2 ← GND
         ↓      ↑    ↑
         charges  | reverse current builds

Output: D7, D8 reverse biased → C0 supplies load alone
```

State Matrix A_{11} (9×9) - CORRECTED

```
A11 = [
  0,      0,      0,      0,      0,      0,       0,       0,       0;      % diL1/dt = Vin/L1 (no state deps)
  0,      0,      0,      0,      0,      0,       0,       0,       0;      % diL2/dt = Vin/L2 (no state deps)
  0,      0,      0,      0,      0,      0,       0,       0,       0;      % diL3/dt = 0
  0,      0,      0,      0,      0,      0,       0,       0,       0;      % diL4/dt = 0
  0,      0,      0,      0,      0,      0,       0,       0,       0;      % diL5/dt = -vC1/L5
  0,      0,      0,      0,      0,      0,       0,       0,       0;      % diL6/dt = -vC3/L6
  0,      0,      0,      0,   -1/C1,     0,       0,       0,       0;      % dvC1/dt = (-iL5)/C1
  0,      0,      0,      0,      0,   -1/C3,      0,       0,       0;      % dvC3/dt = (-iL6)/C3
  0,      0,      0,      0,      0,      0,       0,       0,       0;      % dvC0/dt linear part (CPL separate)
];
```

Input Matrix B_{11} and CPL Term

```
B11 = [1/L1; 1/L2; 0; 0; 0; 0; 0; 0; 0]; f_CPL = [0; 0; 0; 0; 0; 0; 0; 0; -P/(C0·vC0)] (nonlinear CPL load term)
```

Key Correction: Rows 7-8 show **iC1 = iL5** and **iC3 = iL6** (series connection). Since iL5, iL6 < 0 (reverse current), the negative sign makes dvC1/dt, dvC3/dt positive, indicating capacitor charging.

Physical Meaning: L2, L1 charge directly from Vin (no capacitor voltage in path). L5, L6 build reverse momentum through C1, C3. This stored energy will be released forward when switches open. Output capacitor C0 discharges to CPL load only - no power delivery from converter.