

# Cell Library Databook

by Team S5

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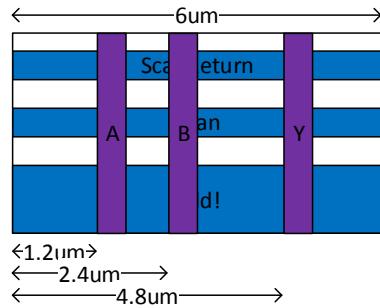
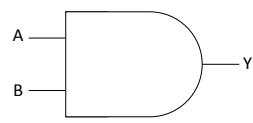
# 1 AND2

**Designer:** Constantijn Schepens

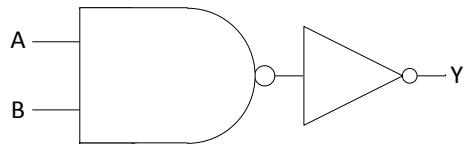
**Cell Description:** A two input AND gate

## Dimensions

### Symbol



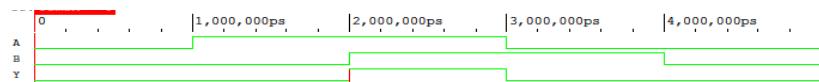
### Gate Level Diagram



### AC Characteristics

Signal	Average Delay (ps)
a propagation	121.7
b propagation	124.0

### System Verilog Simulation

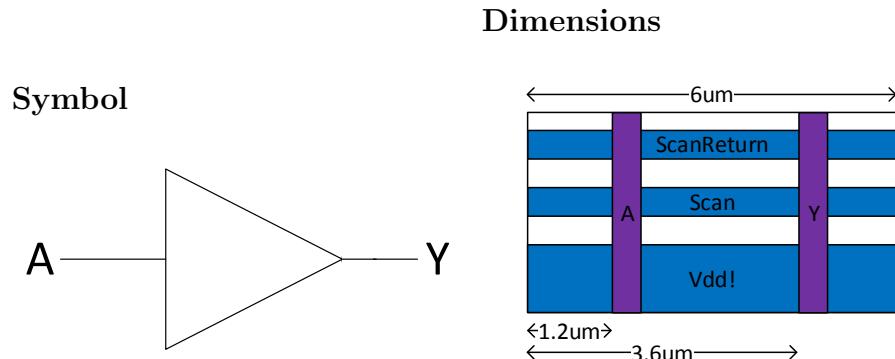


## 2 BUFFER

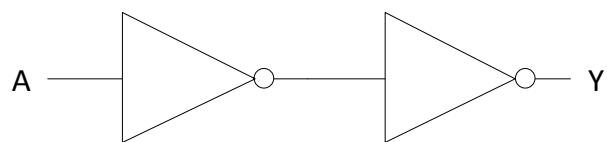
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Designer: Ashley Robinson

Cell Description: A non-inverting buffer



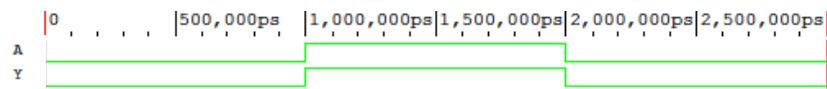
**Gate Level Diagram**



### AC Characteristics

Signal	Average Delay (ps)
a propagation	134.2

### System Verilog Simulation



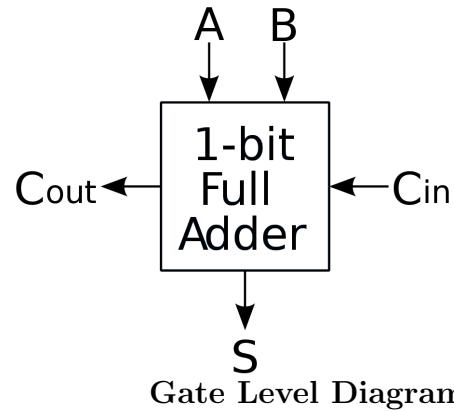
### 3 FULLADDER

---

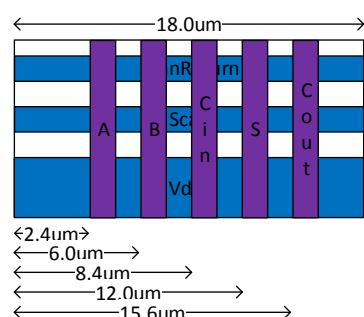
**Designer:** Martin Wearn

**Cell Description:** Adds two bit values and the previous bits crie carry out, to produce a sum and carry

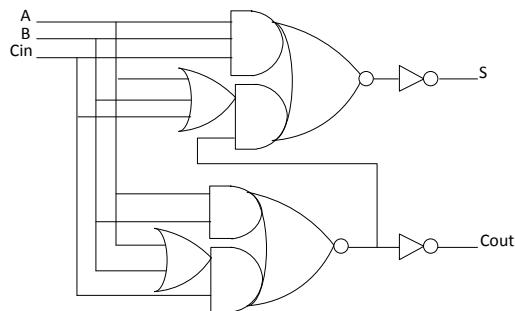
Symbol



Dimensions



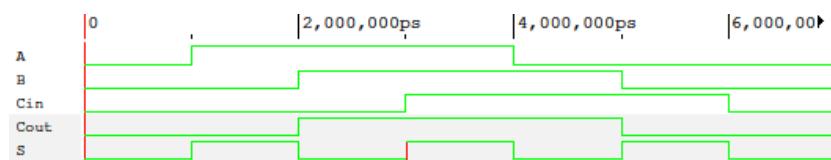
Gate Level Diagram



AC Characteristics

System Verilog Simulation

Signal	Average Delay (ps)
average a to s prop delay	294.9
average a to cout prop delay	285.0
average b to s prop delay	262.3
average b to cout prop delay	294.0
average cin to s prop delay	252.7
average cin to cout prop delay	274.6



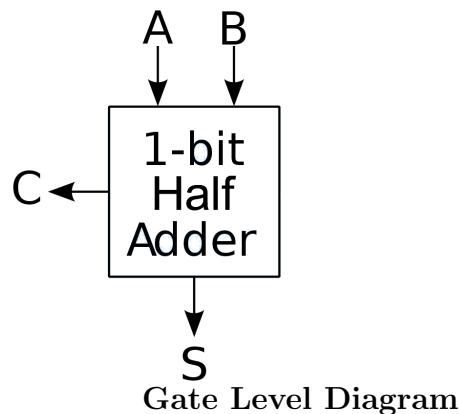
## 4 HALFADDER

---

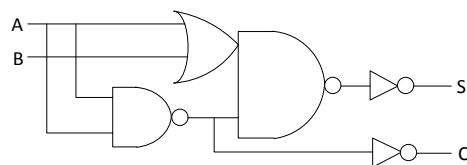
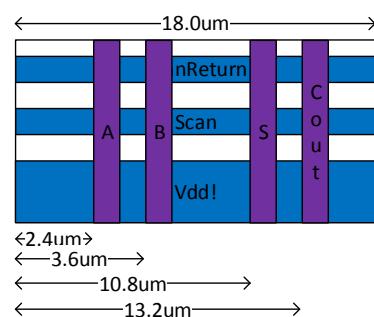
**Designer:** Martin Wearn

**Cell Description:** Adds two bits to produce a sum and carry

Symbol



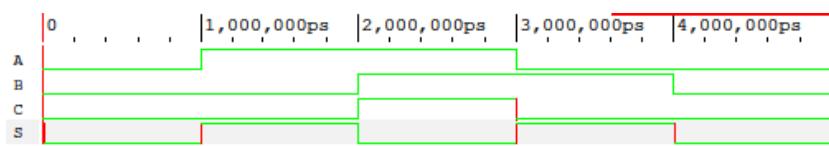
Dimensions



AC Characteristics

Signal	Average Delay (ps)
average a to s prop	251.7
average a to c prop	167.0
average b to s prop	240.9
average b to c prop	166.1

System Verilog Simulation



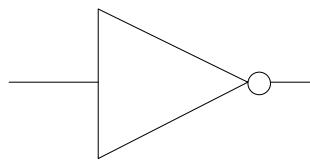
## 5 INV

---

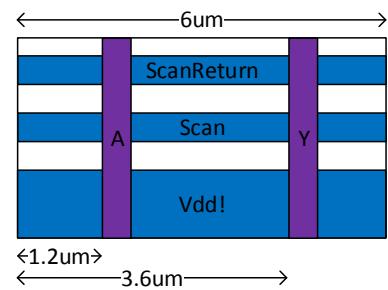
**Designer:** Henry Lovett

**Cell Description:** A basic inverter gate

**Symbol**



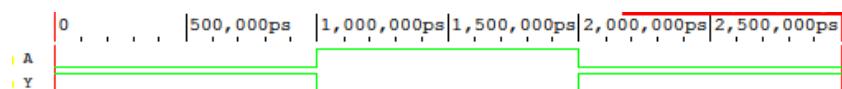
**Dimensions**



### AC Characteristics

Signal	Average Delay (ps)
a rise delay	107.3
a fall delay	81.7

### System Verilog Simulation



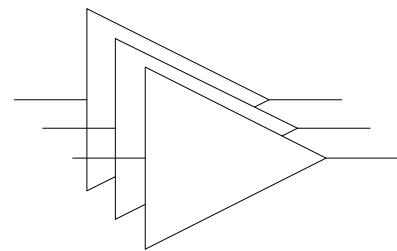
## 6 LEFTBUF

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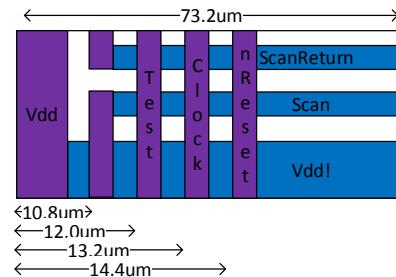
**Designer:** Henry Lovett

**Cell Description:** A start of row buffer cell.

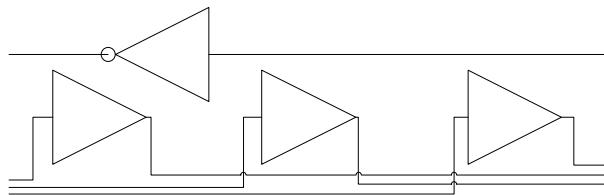
**Symbol**



**Dimensions**



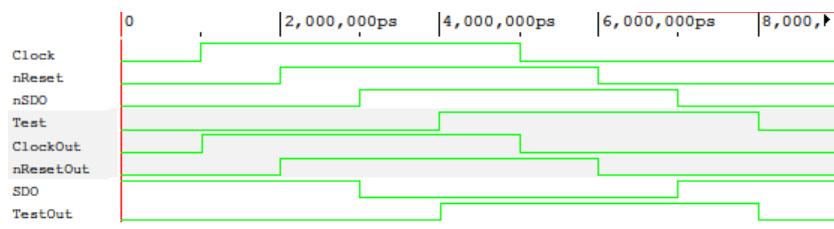
**Gate Level Diagram**



**AC Characteristics**

Signal	Average Delay (ps)
clock rise prop delay	287.5
clock fall prop delay	271.3
test rise prop delay	282.5
test fall prop delay	272.6
nreset rise prop delay	290.5
nreset fall prop delay	273.2
sdo rise prop delay	124.7
sdo fall prop delay	157.7

**System Verilog Simulation**

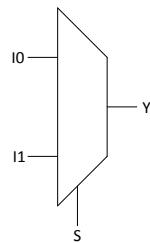


## 7 MUX2

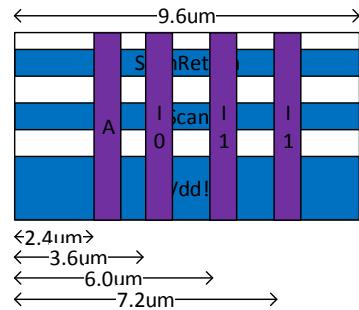
**Designer:** Constantijn Schepens

**Cell Description:** A two input Multiplexor

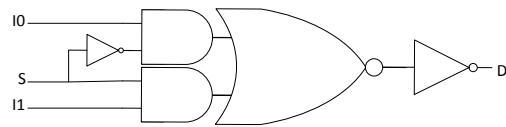
**Symbol**



**Dimensions**



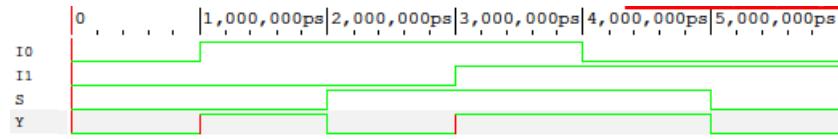
**Gate Level Diagram**



**AC Characteristics**

Signal	Average Delay (ps)
i0 propagation	182.5
i1 propagation	213.0
s pass i0 propagation	214.0
s pass i1 propagation	224.7

**System Verilog Simulation**

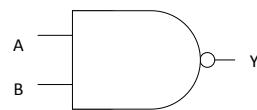


## 8 NAND2

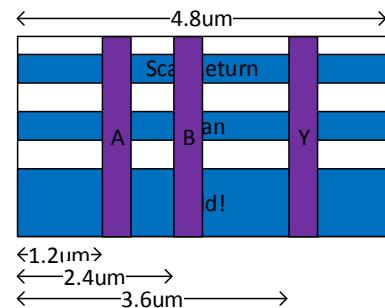
**Designer:** Constantijn Schepens

**Cell Description:** A two input NAND gate

Symbol



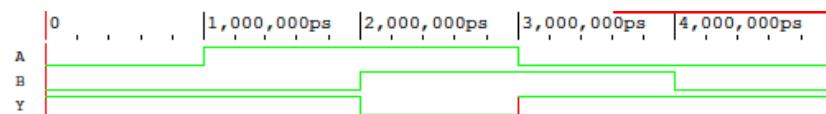
Dimensions



AC Characteristics

Signal	Average Delay (ps)
a propagation	117.0
b propagation	117.6

System Verilog Simulation



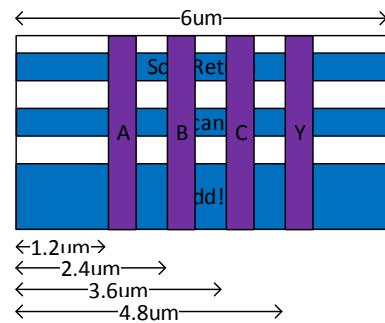
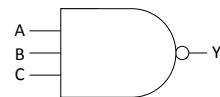
## 9 NAND3

**Designer:** Constantijn Schepens

**Cell Description:** A three input NAND gate

### Dimensions

#### Symbol



### AC Characteristics

Signal	Average Delay (ps)
a propagation	142.8
b propagation	142.3
c propagation	137.5

### System Verilog Simulation



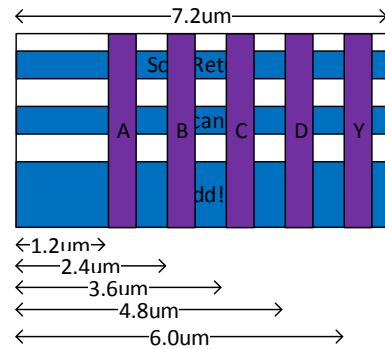
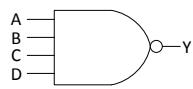
## 10 NAND4

**Designer:** Constantijn Schepens

**Cell Description:** A four input NAND gate

### Dimensions

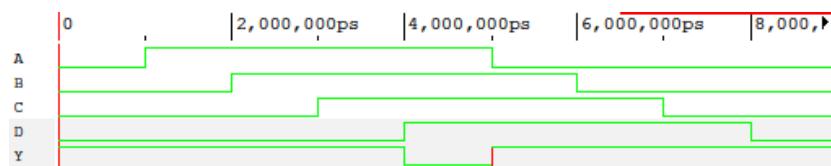
#### Symbol



### AC Characteristics

Signal	Average Delay (ps)
a propagation	171.0
b propagation	167.9
c propagation	165.1
d propagation	159.6

### System Verilog Simulation



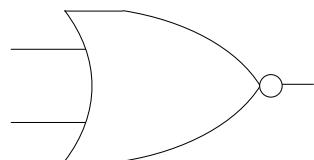
## 11 NOR2

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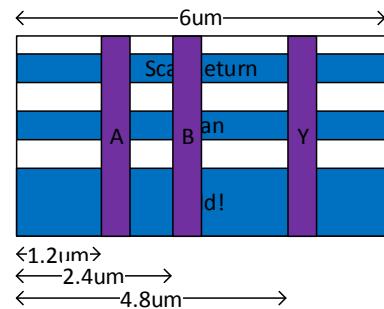
**Designer:** Henry Lovett

**Cell Description:** A two input NOR gate

**Symbol**



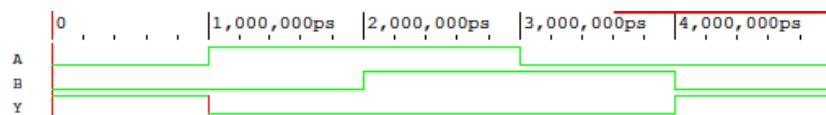
**Dimensions**



### AC Characteristics

Signal	Average Delay (ps)
a rise prop delay	91.8
a fall prop delay	196.4
b rise prop delay	87.6
b fall prop delay	192.9

### System Verilog Simulation

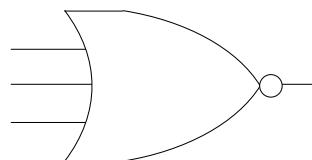


## 12 NOR3

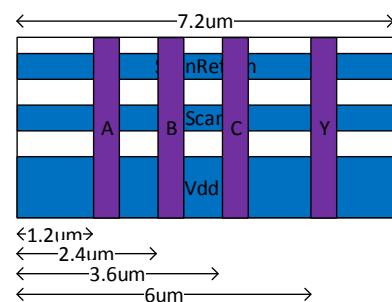
**Designer:** Henry Lovett

**Cell Description:** A three input NOR gate

**Symbol**



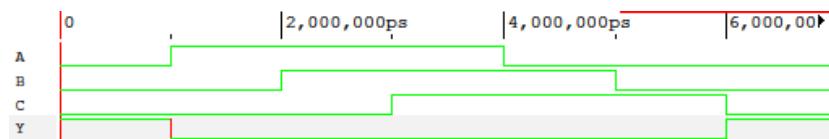
**Dimensions**



### AC Characteristics

Signal	Average Delay (ps)
a rise prop delay	100.4
a fall prop delay	305.7
b rise prop delay	89.8
b fall prop delay	281.0
c rise prop delay	95.4
c fall prop delay	300.7

### System Verilog Simulation



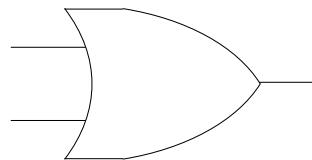
## 13 OR2

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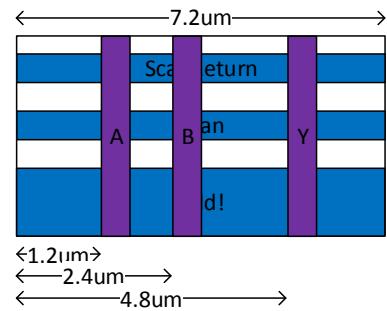
**Designer:** Henry Lovett

**Cell Description:** A two input OR gate

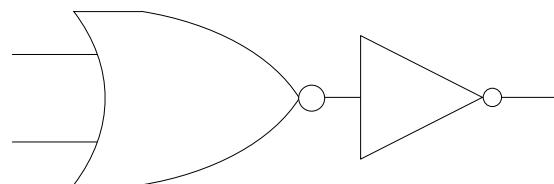
**Symbol**



**Dimensions**



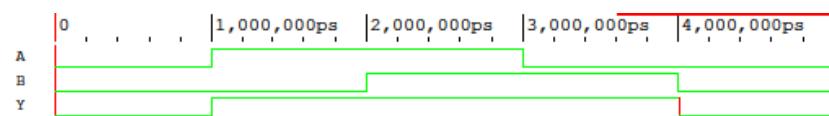
**Gate Level Diagram**



**AC Characteristics**

Signal	Average Delay (ps)
a fall delay	174.0
a rise delay	140.9
b fall delay	176.3
b rise delay	150.5

**System Verilog Simulation**



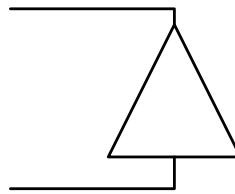
## 14 rightend

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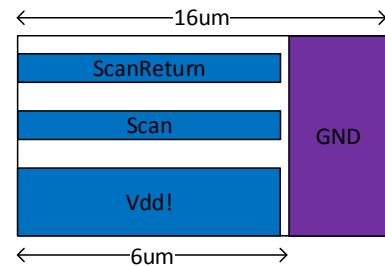
**Designer:** Henry Lovett

**Cell Description:** An end of row buffer cell.

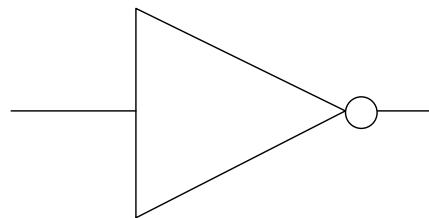
### Symbol



### Dimensions



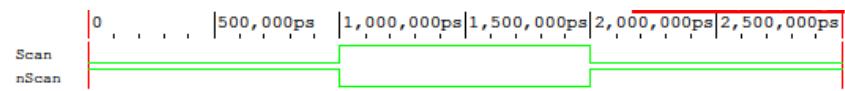
### Gate Level Diagram



### AC Characteristics

Signal	Average Delay (ps)
scan fall delay	56.4
scan rise delay	78.2

## System Verilog Simulation

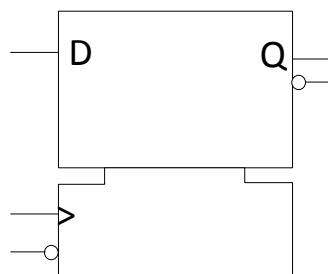


## 15 SCANDTYPE

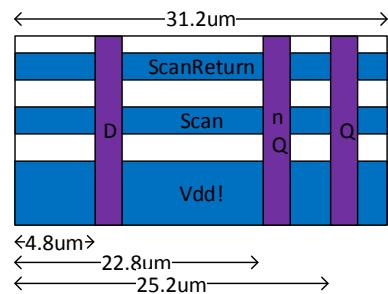
**Designer:** Constantijn Schepens

**Cell Description:** A scannable D-Type cell

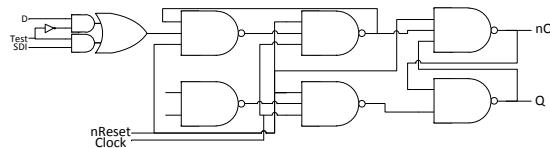
Symbol



Dimensions



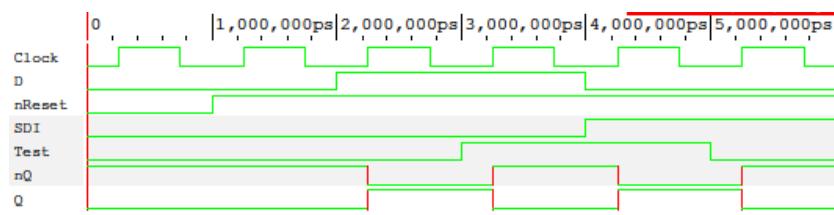
Gate Level Diagram



AC Characteristics

Signal	Average Delay (ps)
clock to q rise	336.9
clock to q fall	509.6
clock to nq rise	302.0
clock to nq fall	590.0
nreset to q fall	385.4
nreset to nq rise	177.7

System Verilog Simulation

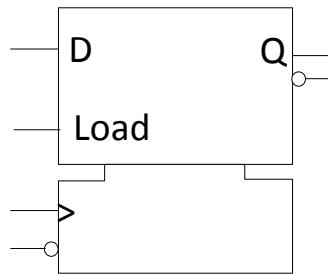


## 16 SCANREG

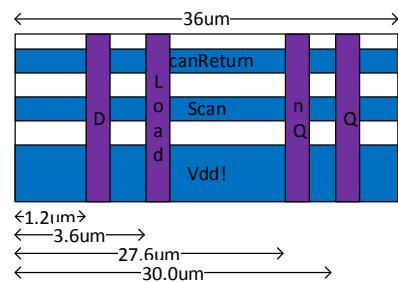
**Designer:** Constantijn Schepens

**Cell Description:** A scannable register cell

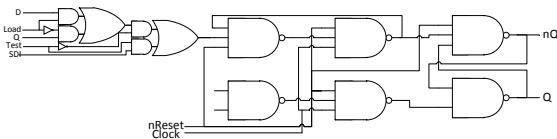
**Symbol**



**Dimensions**



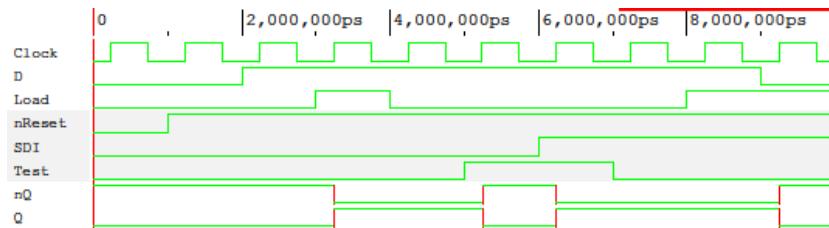
**Gate Level Diagram**



**AC Characteristics**

Signal	Average Delay (ps)
clock to q rise	357.2
clock to q fall	542.1
clock to nq rise	301.5
clock to nq fall	617.0
nreset to q fall	412.5
nreset to nq rise	178.3

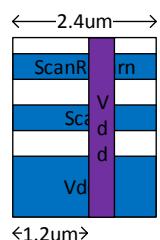
**System Verilog Simulation**



## 17 Tie High

**Designer:** Martin Wearn  
**Cell Description:** A tie to Vdd cell.

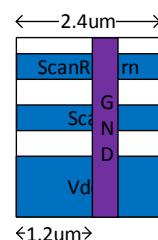
### Dimensions



## 18 Tie Low

**Designer:** Martin Wearn  
**Cell Description:** A tie to GND cell.

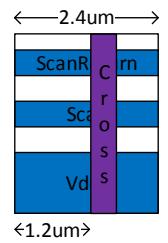
### Dimensions



## 19 Rowcrosser

**Designer:** Martin Wearn  
**Cell Description:** A row crossing cell.

## Dimensions

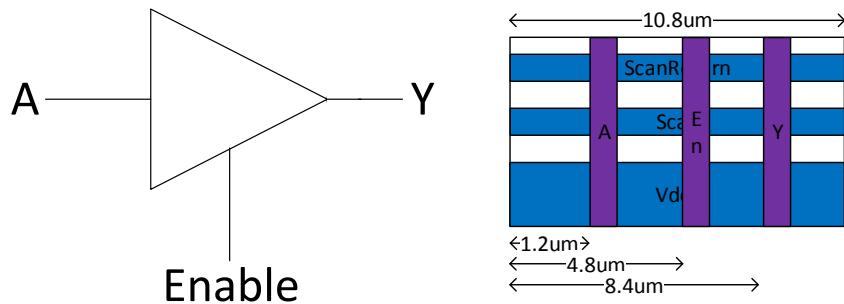


## 20 TRISBUF

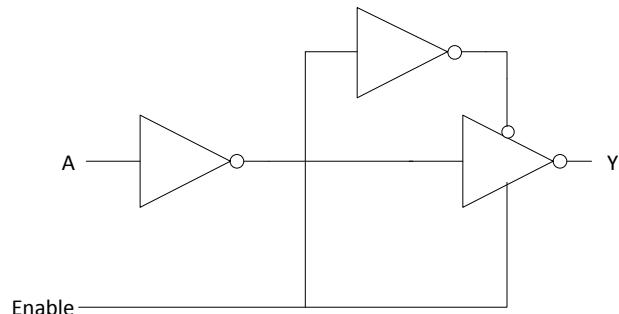
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**Designer:** Ashley Robinson  
**Cell Description:** A tristate buffer

**Symbol** **Dimensions**



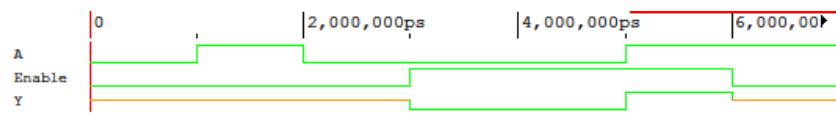
**Gate Level Diagram**



**AC Characteristics**

Signal	Average Delay (ps)
a propagation	211.8

**System Verilog Simulation**



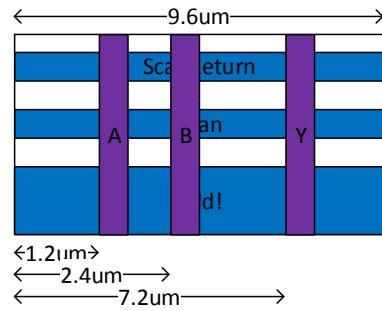
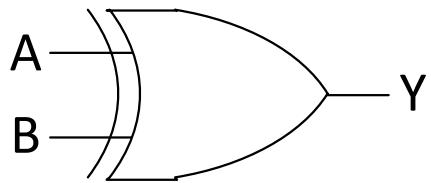
## 21 XOR2

Designer: Ashley Robinson

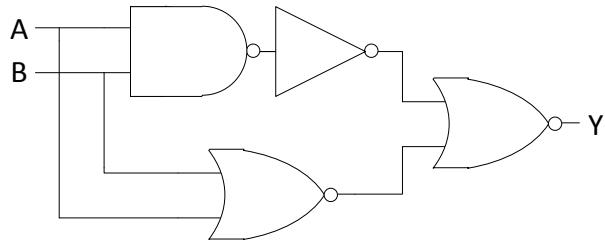
Cell Description: A two input xor gate

Dimensions

Symbol



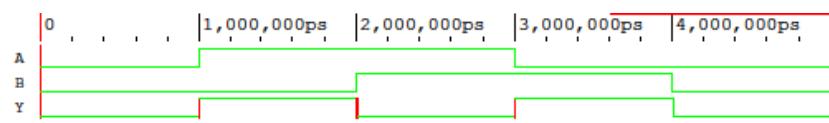
Gate Level Diagram



AC Characteristics

Signal	Average Delay (ps)
a propagation	273.4
b propagation	193.0

System Verilog Simulation



## A Appendix A

### A.1 Team Management

#### A.1.1 Justification of the Division of Labour

The four major cells were divided between the team as recommended in the specification. It was decided to also attempt the optional cells for teams of four. An extra person in a team of five would be in charge of designing the halfadder and xor2. The halfadder was assigned to the team member designing the fulladder as their expertise was greater for designing adder cells. The xor2 cell was assigned to the team member designing the rdtype as this cell was assumed less time consuming than the two other sets of major cells. The remaining cells were grouped and divided among the teams as shown in Table 1.

Cell Groupings	Reasoning
and2, and2, nand3, nand4	Nands and Ands are similar in design.
buffer, trisbuf	Buffers are similar in design.
inverter, nor2, nor3, or2	Nors and Ors similar in design. Inverter is a simple cell assigned to distribute load.
rowcrosswer, tiehigh, tielow	Low complexity cells assigned to team member tasked with designing both adders.

Table 1: Cell design groupings and reasoning

#### A.1.2 Version Control

The Git revision control system was used throughout the project to facilitate collaborative working. GitHub is a web-based hosting service for git. This was used to share files, allocate work and track bugs.

#### A.1.3 Process automation

The team produced a number of scripts to improve productivity by automating processes such extraction from magic, design simulation and consistency checking. Using Latex allowed the databook compilation to also be automated as separate files for each cell were stored in the hierarchy of folders. This way each designer could add their own files to the data book independently.

## A.2 Division of Labour

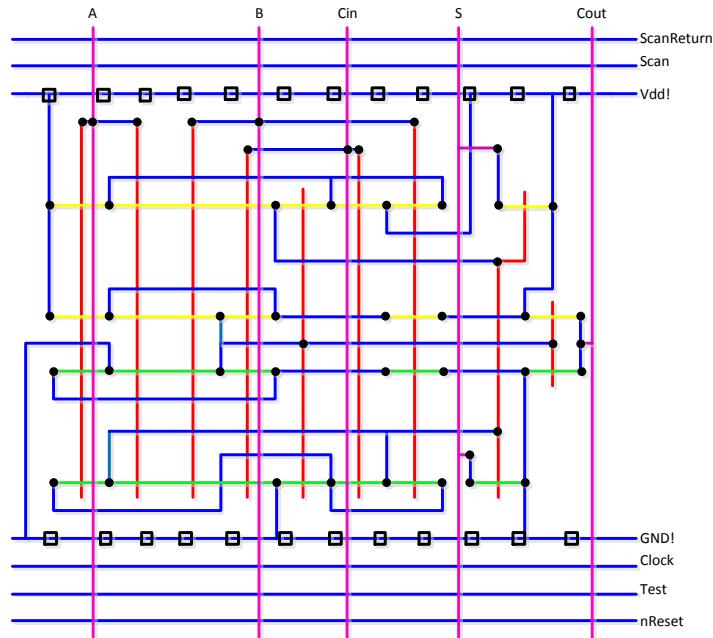
## B Design Detail

## B.1 FULLADDER

**Designer:** Martin Wearn

**Cell Description:** Adds two bit values and the previous bitslice carry out, to produce a sum and carry

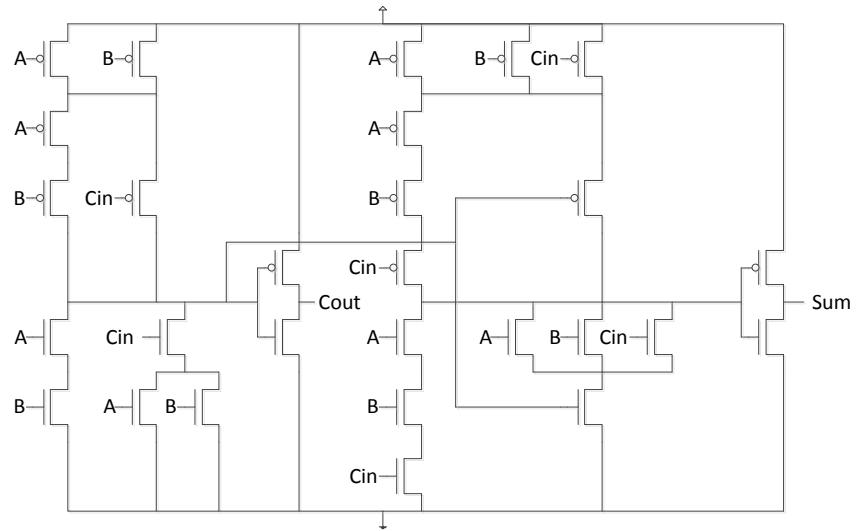
Stick Diagram



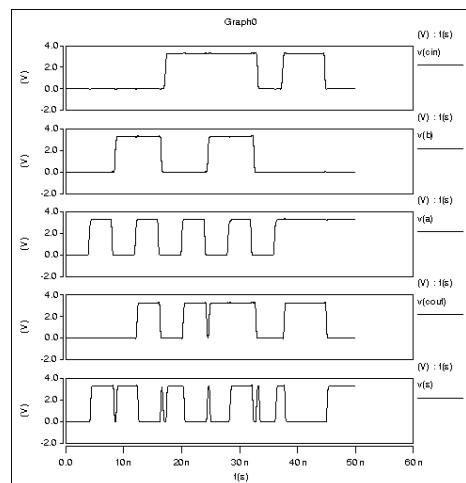
AC Characteristics

Signal	Average Delay (ps)
average a to s prop delay	294.9
average a to cout prop delay	285.0
average b to s prop delay	262.3
average b to cout prop delay	294.0
average cin to s prop delay	252.7
average cin to cout prop delay	274.6

## Transistor Level Circuit Diagram



## HSpice Simulation

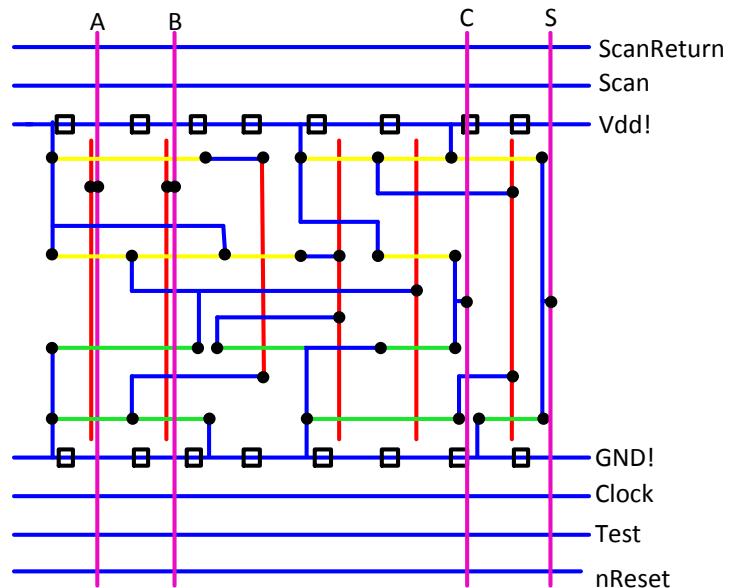


## B.2 HALFADDER

**Designer:** Martin Wearn

**Cell Description:** Adds two bits to produce a sum and carry

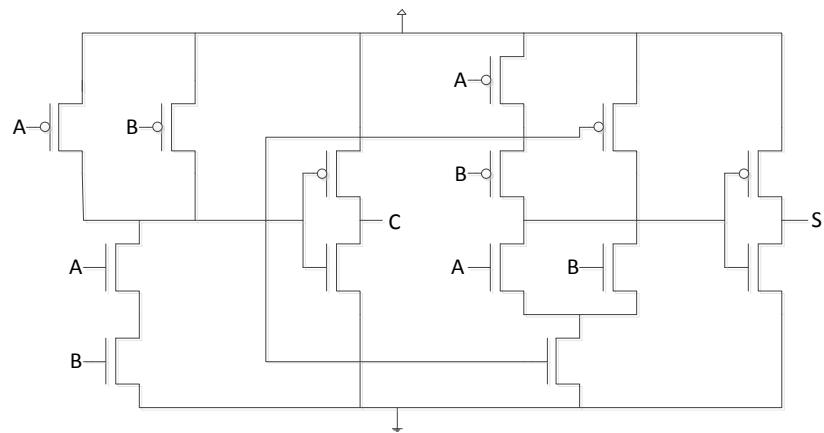
Stick Diagram



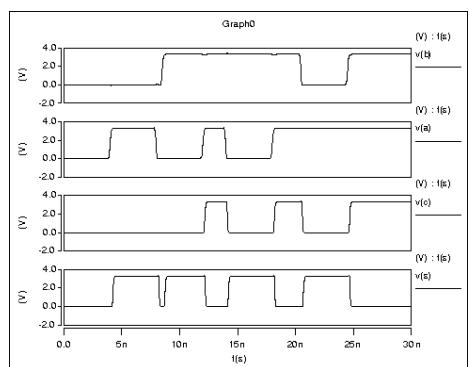
AC Characteristics

Signal	Average Delay (ps)
average a to s prop	251.7
average a to c prop	167.0
average b to s prop	240.9
average b to c prop	166.1

### Transistor Level Circuit Diagram



### HSpice Simulation



### B.3 LEFTBUF

**Designer:** Henry Lovett

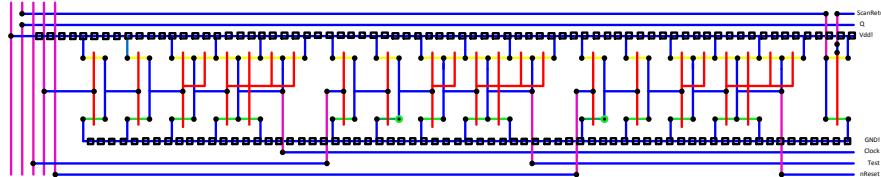
**Cell Description:** A start of row buffer cell.

This cell is to be placed at the beginning of each row of cells. The purpose of this cell is to buffer the *Clock*, *nReset* and *Test* signals to attempt to eliminate skew of the signals. They also cater for the scan path in the circuit by routing and buffering the signal.

This cell contains 3 large buffers, each made up of 4 stages. The gain of the stages are gradually increased, relative to the first. The transistors were folded to reduce the vertical height of the cell. The total, and folded sizes of the transistors are seen in the table below.

Stage	1	2	3	4
Gain	1	2.7	7.3	20
$W_n$ unfolded ( $\mu m$ )	1.0	2.7	7.3	20
$W_p$ unfolded ( $\mu m$ )	2.9	7.85	21.2	58
$W_n$ folded ( $\mu m$ )	$1 \times 1.0$	$1 \times 2.7$	$1 \times 7.3$	$2 \times 10.0$
$W_p$ folded ( $\mu m$ )	$1 \times 2.9$	$1 \times 7.85$	$2 \times 10.6$	$4 \times 14.5$

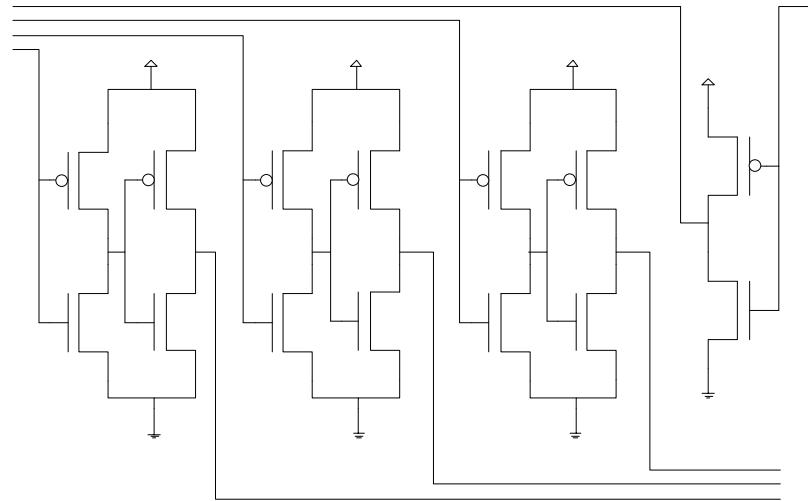
#### Stick Diagram



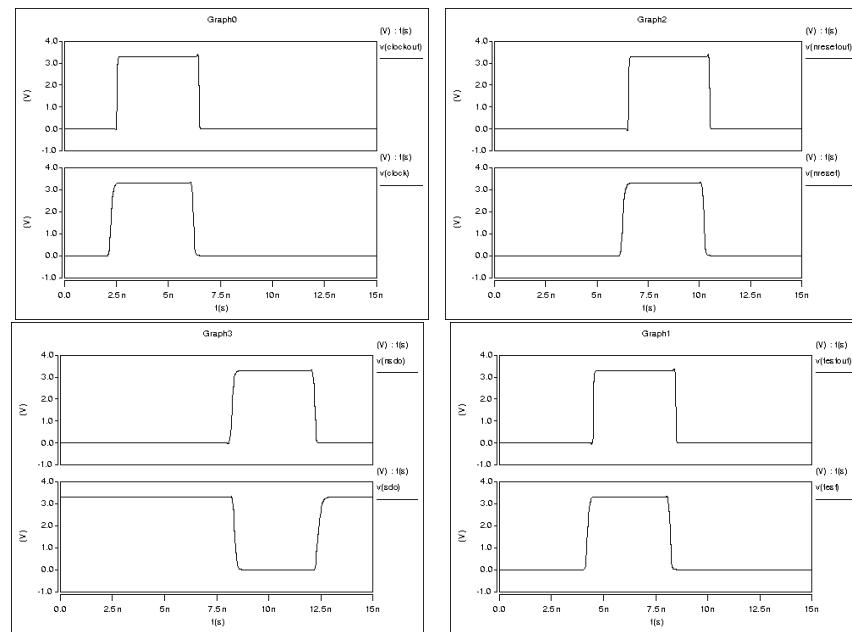
#### AC Characteristics

Signal	Average Delay (ps)
clock rise prop delay	287.5
clock fall prop delay	271.3
test rise prop delay	282.5
test fall prop delay	272.6
nreset rise prop delay	290.5
nreset fall prop delay	273.2
sdo rise prop delay	124.7
sdo fall prop delay	157.7

## Transistor Level Circuit Diagram



## HSpice Simulation



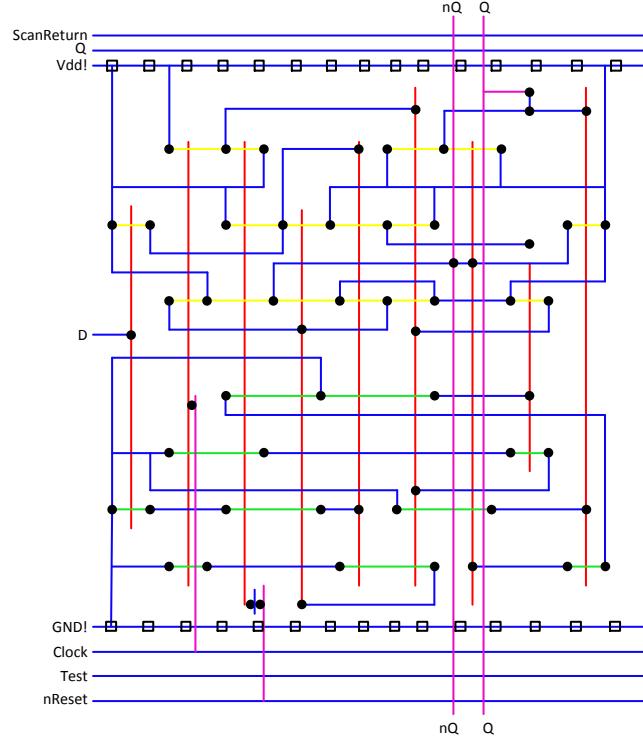
## B.4 RDTYPE

**Designer:** Ashley Robinson

**Cell Description:** Raw Dtype

This gate matrix design was optimised by arranging polysilicon columns to allow as many transistors to fit on a row as possible. Three rows of PMOS transistors and four rows of NMOS transistors make up cell. Routing power rails up both sides of the matrix allowed the design to be further compressed. The D input on the middle left was intentionally not surrounded leaving only metal1 to reroute when it came to dimension matching.

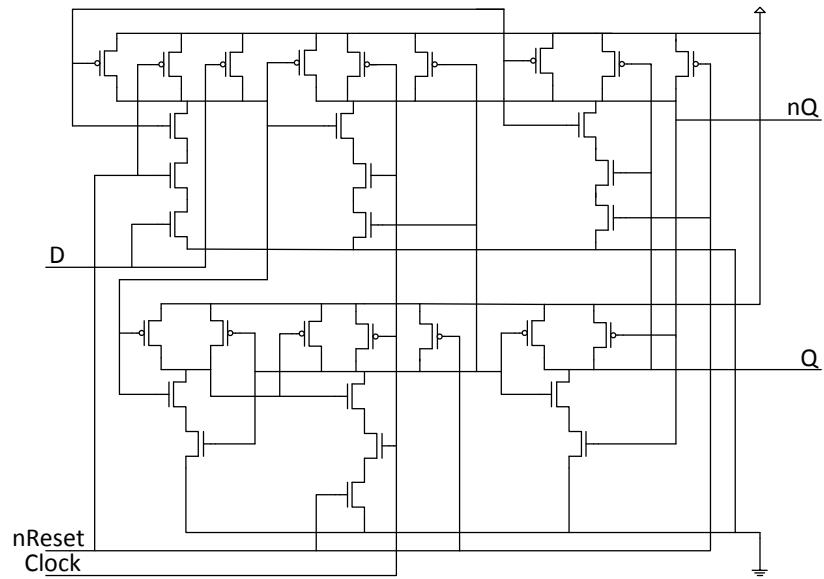
### Stick Diagram



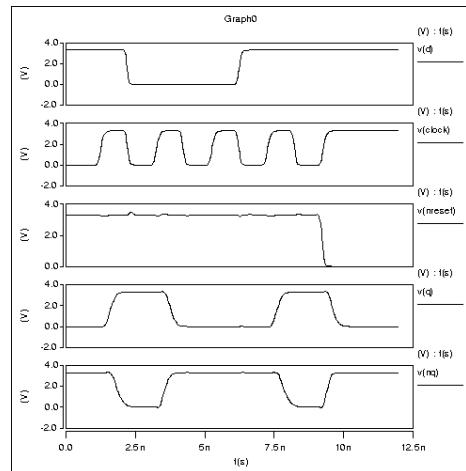
### AC Characteristics

Signal TO BE	Average Delay (ps) DONE
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### Transistor Level Circuit Diagram



### HSpice Simulation



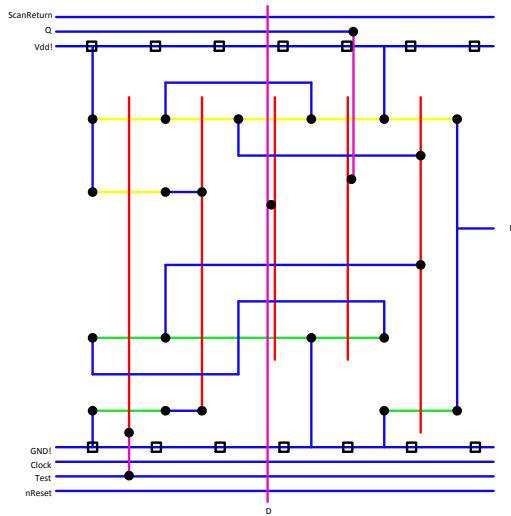
## B.5 SMUX2

**Designer:** Constantijn Schepens

**Cell Description:** A 2 input scannable multiplexer, intended to be connected to a raw D-type to create a scannable D-type.

A single Euler path was used when laying out this cell, before taking into account inverters. The Euler path (T-nT-D-S) was designed such that the output was all the way on the right side such that it could connect directly to the D input of the raw D-type. Once this was done the required internal inverters were added in by creating a gate matrix design.

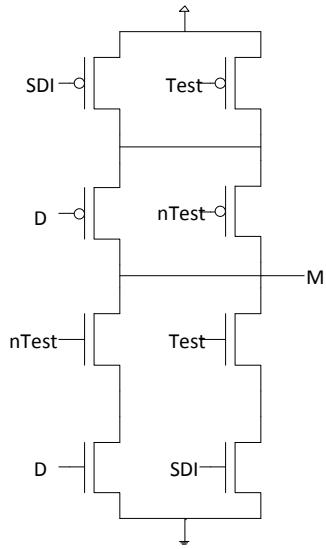
### Stick Diagram



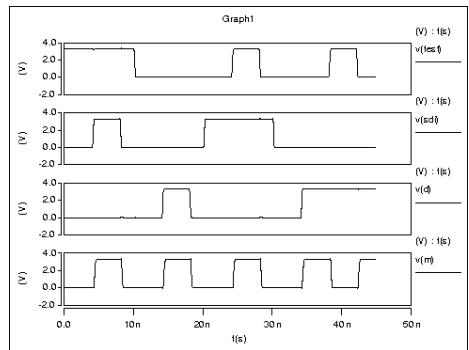
### AC Characteristics

Signal	Average Delay (ps)
sdi propagation	212.5
d propagation	182.1
test pass sdi propagation	223.5
test pass d propagation	213.8

## Transistor Level Circuit Diagram



## HSpice Simulation



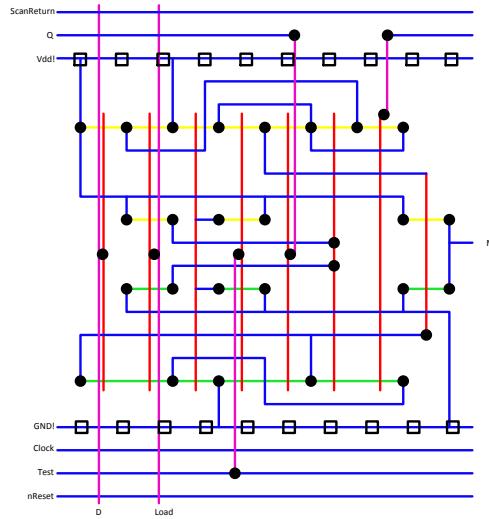
## B.6 SMUX3

**Designer:** Constantijn Schepens

**Cell Description:** A 3 input scannable multiplexer, intended to be connected to a raw D-type to create a scannable register.

A similar approach was taken for the layout of this cell as for the smux2. Initially inverters were excluded and a single Euler path (D-Load-nTest-Test-SDI-nLoad-Q) was found that both kept M and Q as close to the right side as possible (to connect to the raw D-type) and kept the Test/Load nearest to their inverted partners for easy wiring. For the internal inverter placement multiple layouts were trialed to find the most efficient one, that also allowed all the internal wiring to be done with metal 1 exclusively(to reduce the number of vias).

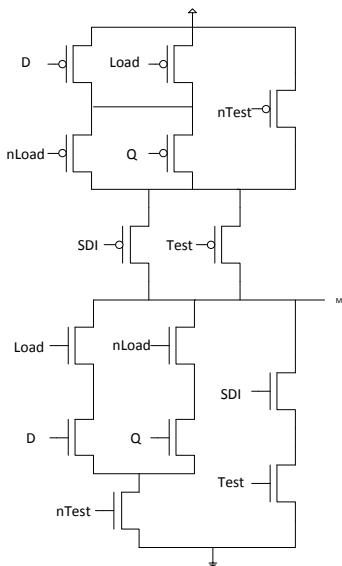
### Stick Diagram



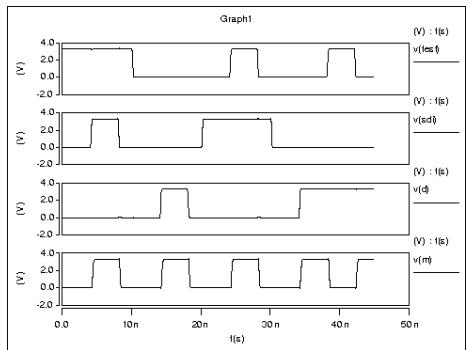
Signal	Average Delay (ps)
sdi propagation	227.0
d propagation	289.4
q propagation	259.1
test pass sdi propagation	242.9
test pass d propagation	287.0
test pass q propagation	278.9
load pass d propagation	296.1
load pass q propagation	303.6

## AC Characteristics

### Transistor Level Circuit Diagram



## HSpice Simulation



## B.7 XOR2

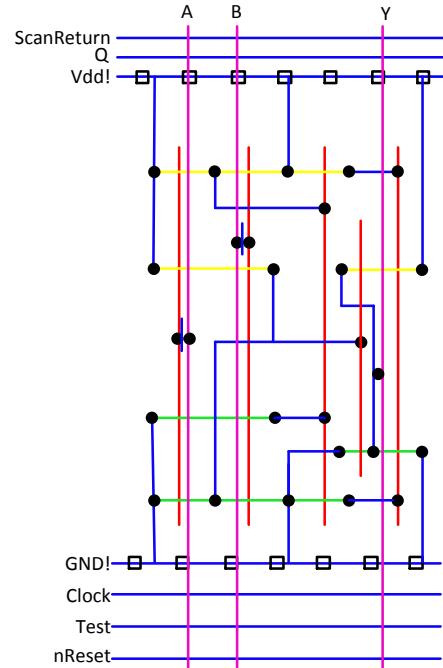
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**Designer:** Ashley Robinson

**Cell Description:** A 2 input XOR gate.

Compound gate routed using an Euler path.

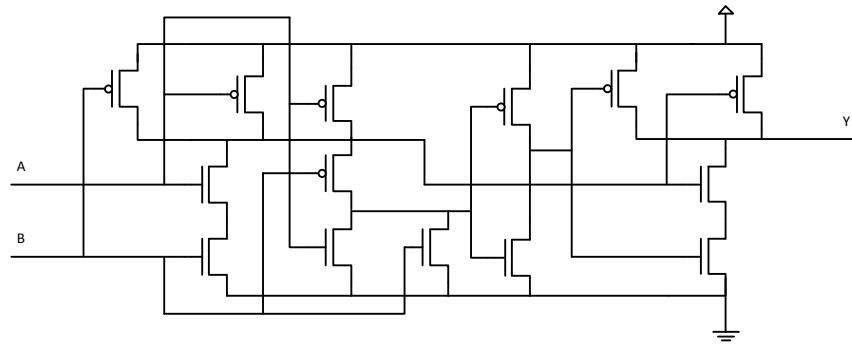
**Stick Diagram**



**AC Characteristics**

Signal	Average Delay (ps)
a propagation	273.4
b propagation	193.0

### Transistor Level Circuit Diagram



### HSpice Simulation

