Cell Library Databook

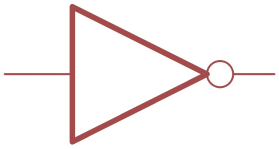
by Team S5
H. Lovett (hl13g10)
A. J. Robinson (ajr2g10)
C. Schepens (cs7g10)
M. Wearn (mw20g10)

December 3, 2013

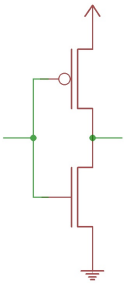
And2

Designer: Constantijn Schepens
Cell Description: A two input AND gate

Symbol



Circuit Diagram

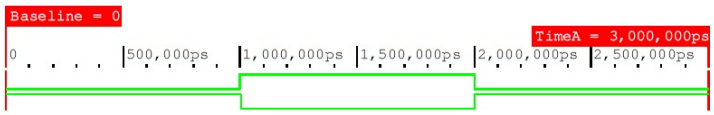


Dimensions

AC Characteristics

Signal	Delay (s)
TO BE	DONE

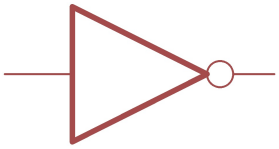
System Verilog Simulation



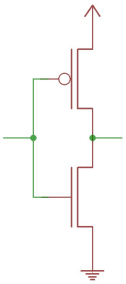
buffer

Designer: Ashley Robinson
Cell Description: A non-inverting buffer

Symbol



Circuit Diagram

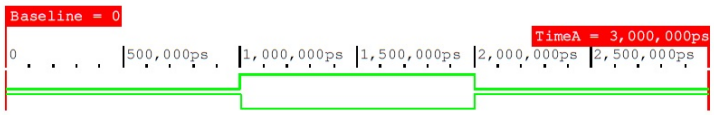


Dimensions

AC Characteristics

Signal	Delay (s)
TO BE	DONE

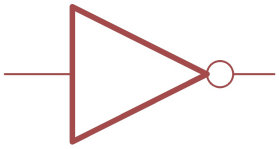
System Verilog Simulation



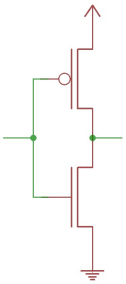
fulladder

Designer: Martin Wearn
Cell Description: A Full Adder

Symbol



Circuit Diagram

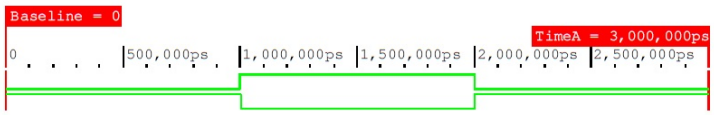


Dimensions

AC Characteristics

Signal	Delay (s)
TO BE	DONE

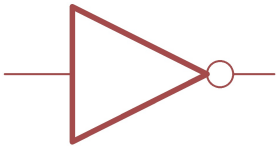
System Verilog Simulation



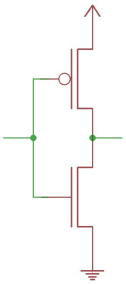
halfadder

Designer: Martin Wearn
Cell Description: A Half Adder

Symbol



Circuit Diagram

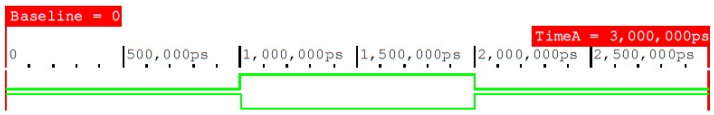


Dimensions

AC Characteristics

Signal	Delay (s)
TO BE	DONE

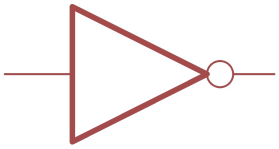
System Verilog Simulation



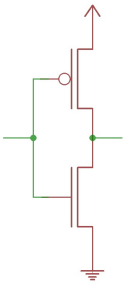
Inverter

Designer: Henry Lovett
Cell Description: A basic inverter gate

Symbol



Circuit Diagram

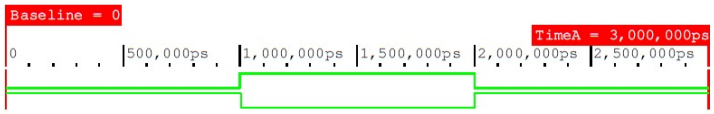


Dimensions

AC Characteristics

Signal	Delay (s)
a rise delay	1.306e-10
a fall delay	9.373e-11

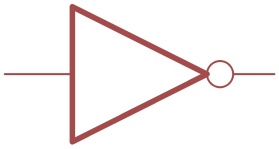
System Verilog Simulation



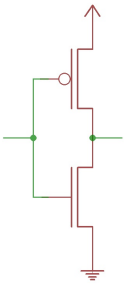
leftbuf

Designer: Henry Lovett
Cell Description: A start of row buffer cell.

Symbol



Circuit Diagram

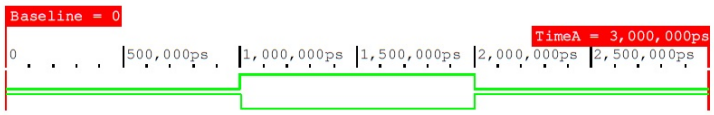


Dimensions

AC Characteristics

Signal	Delay (s)
TO BE	DONE

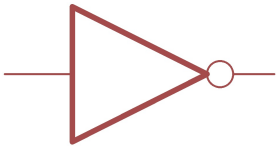
System Verilog Simulation



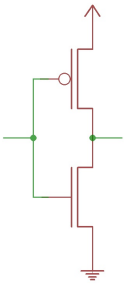
mux2

Designer: Constantijn Schepens
Cell Description: A two input Multiplexor

Symbol



Circuit Diagram

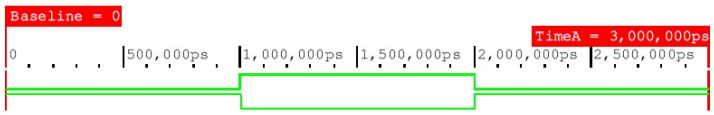


Dimensions

AC Characteristics

Signal	Delay (s)
TO BE	DONE

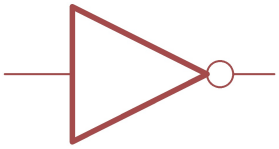
System Verilog Simulation



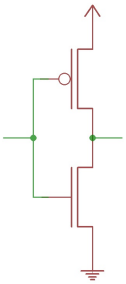
nand2

Designer: Constantijn Schepens
Cell Description: A two input NAND gate

Symbol



Circuit Diagram

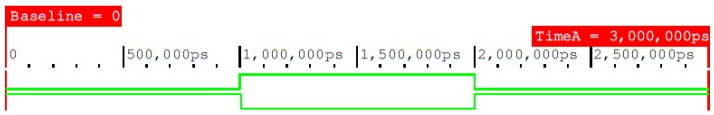


Dimensions

AC Characteristics

Signal	Delay (s)
TO BE	DONE

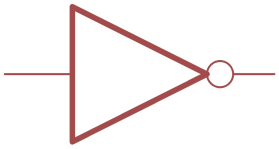
System Verilog Simulation



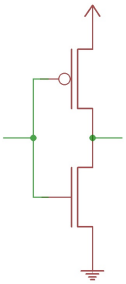
nand3

Designer: Constantijn Schepens
Cell Description: A two input NAND gate

Symbol



Circuit Diagram

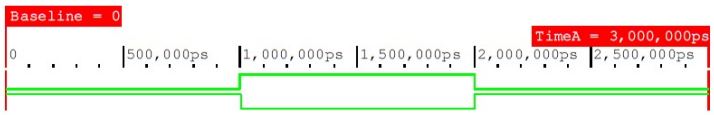


Dimensions

AC Characteristics

Signal	Delay (s)
TO BE	DONE

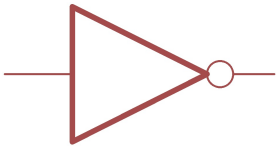
System Verilog Simulation



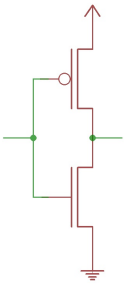
nand4

Designer: Constantijn Schepens
Cell Description: A two input NAND gate

Symbol



Circuit Diagram

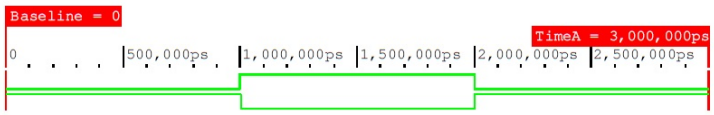


Dimensions

AC Characteristics

Signal	Delay (s)
TO BE	DONE

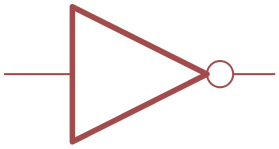
System Verilog Simulation



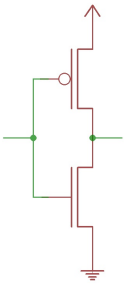
nor2

Designer: Henry Lovett
Cell Description: A two input NOR gate

Symbol



Circuit Diagram

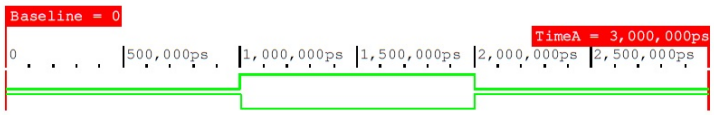


Dimensions

AC Characteristics

Signal	Delay (s)
TO BE	DONE

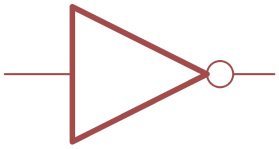
System Verilog Simulation



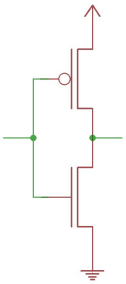
nor3

Designer: Henry Lovett
Cell Description: A three input NOR gate

Symbol



Circuit Diagram

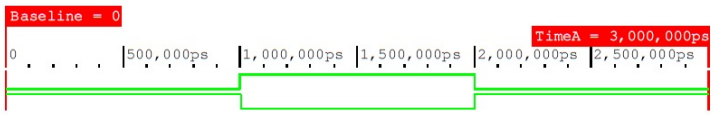


Dimensions

AC Characteristics

Signal	Delay (s)
TO BE	DONE

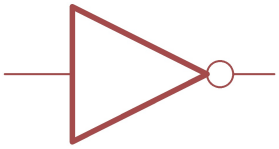
System Verilog Simulation



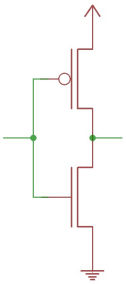
or2

Designer: Henry Lovett
Cell Description: A two input OR gate

Symbol



Circuit Diagram

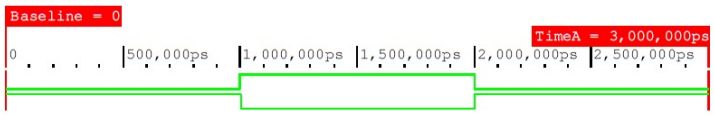


Dimensions

AC Characteristics

Signal	Delay (s)
TO BE	DONE

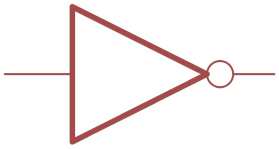
System Verilog Simulation



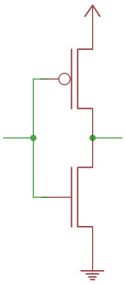
rightend

Designer: Henry Lovett
Cell Description: An end of row buffer cell.

Symbol



Circuit Diagram

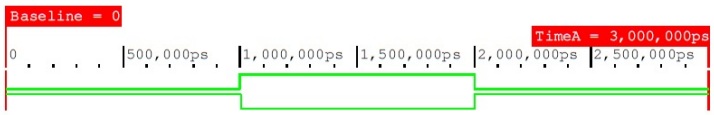


Dimensions

AC Characteristics

Signal	Delay (s)
TO BE	DONE

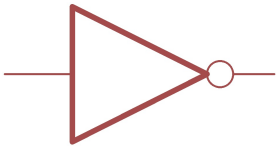
System Verilog Simulation



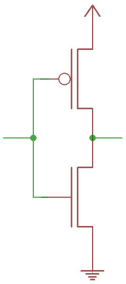
rowcrosser

Designer: Martin Wearn
Cell Description: A rowcrossing cell

Symbol



Circuit Diagram



Dimensions

AC Characteristics

Signal	Delay (s)
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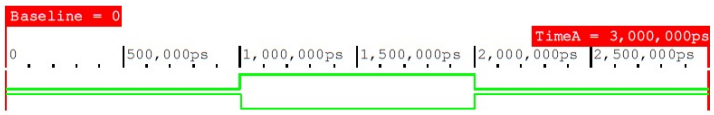
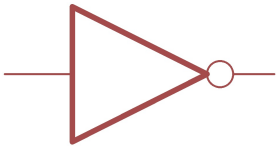
System Verilog Simulation



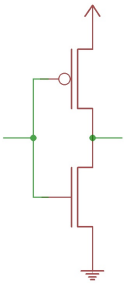
scandtype

Designer: Constantijn Schepens
Cell Description: A Raw DType cell

Symbol



Circuit Diagram

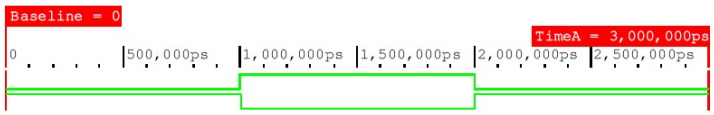


Dimensions

AC Characteristics

Signal	Delay (s)
TO BE	DONE

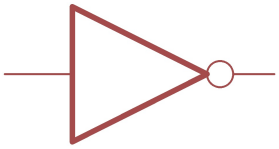
System Verilog Simulation



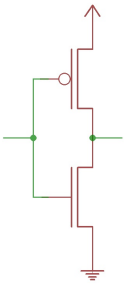
scanreg

Designer: Constantijn Schepens
Cell Description: A Raw DType cell

Symbol



Circuit Diagram



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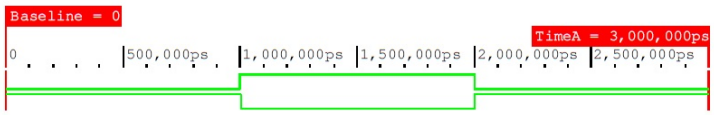
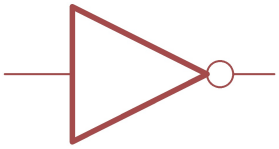


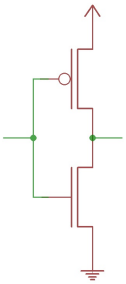
tiehigh

Designer: Martin Wearn
Cell Description: A tie to Vdd cell

Symbol



Circuit Diagram

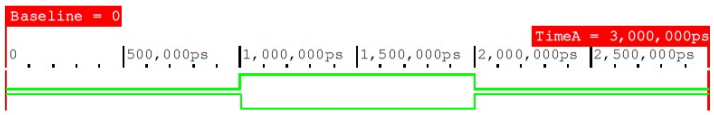


Dimensions

AC Characteristics

Signal	Delay (s)
TO BE	DONE

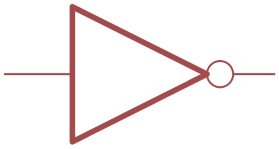
System Verilog Simulation



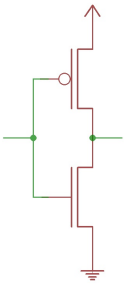
tielow

Designer: Martin Wearn
Cell Description: A tie to GND cell

Symbol



Circuit Diagram

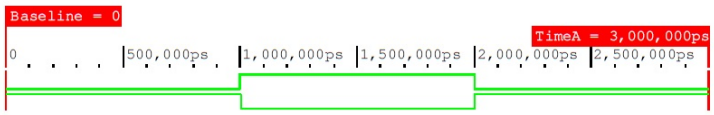


Dimensions

AC Characteristics

Signal	Delay (s)
TO BE	DONE

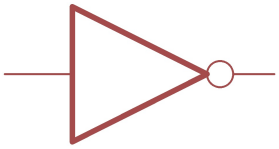
System Verilog Simulation



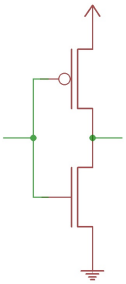
trisbuf

Designer: Ashley Robinson
Cell Description: A tristate buffer

Symbol



Circuit Diagram

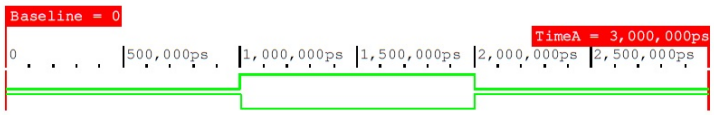


Dimensions

AC Characteristics

Signal	Delay (s)
TO BE	DONE

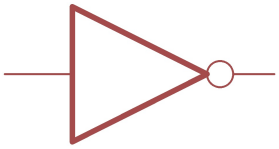
System Verilog Simulation



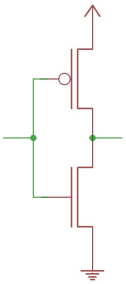
xor2

Designer: Ashley Robinson
Cell Description: A two input xor gate

Symbol



Circuit Diagram



Dimensions

AC Characteristics

Signal	Delay (s)
TO BE	DONE

System Verilog Simulation