Cell Library Databook

by Team S5
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M. Wearn (mw20g10)

December 9, 2013

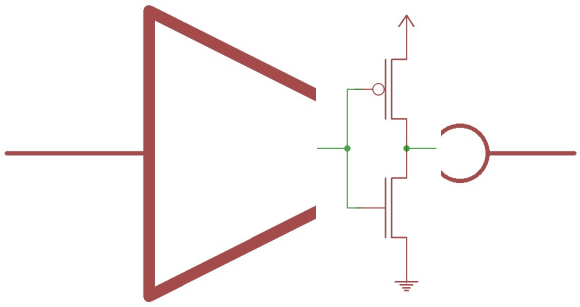
Contents

1 And2

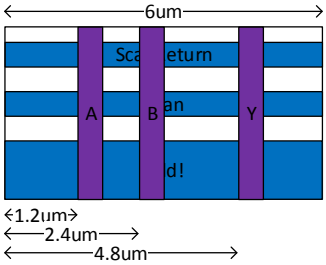
Designer: Constantijn Schepens
Cell Description: A two input AND gate

Symbol

Circuit Diagram



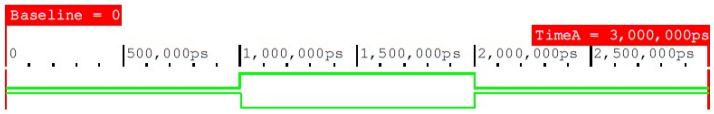
Dimensions



AC Characteristics

Signal	Delay (ps)
a fall propagation delay	171.4
a rise propagation delay	72.1
b fall propagation delay	179.7
b rise propagation delay	68.3

System Verilog Simulation



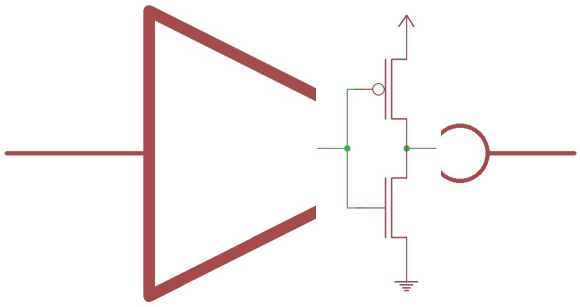
2 buffer

Designer: Ashley Robinson
Cell Description: A non-inverting buffer

Symbol

Circuit Diagram

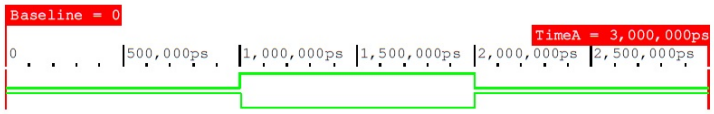
Dimensions



AC Characteristics

Signal	Delay (ps)
prop delay rise	138.5
prop delay fall	129.9
average prop	134.2

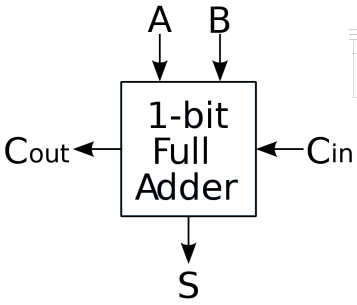
System Verilog Simulation



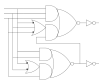
3 fulladder

Designer: Martin Wearn
Cell Description: Adds two bit values and the previous bitsclie carry out, to produce a sum and carry

Symbol



Circuit Diagram



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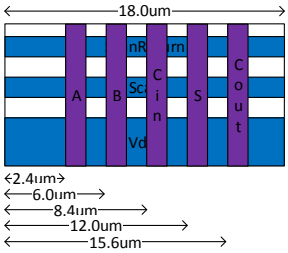
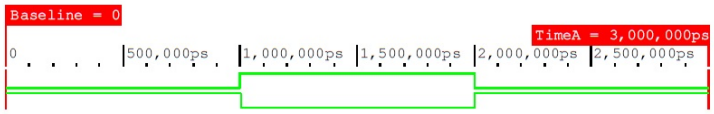


AC Characteristics

Signal	Delay (ps)
prop delay as 1	255.7
prop delay bs 1	222.7
prop delay cins 1	208.3
prop delay as 0	334.2
prop delay bs 0	301.9
prop delay cins 0	297.1
prop delay acout 1	262.0
prop delay bcout 1	228.7
prop delay cincout 1	263.5
prop delay acout 0	308.0
prop delay bcout 0	359.3
prop delay cincout 0	285.7

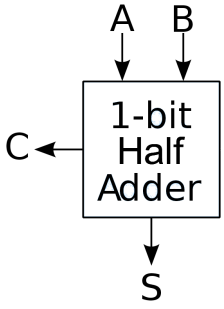
System Verilog Simulation



4 halfadder

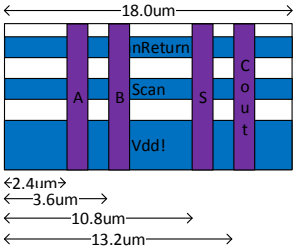
Designer: Martin Wearn
Cell Description: Adds two bits to produce a sum and carry

Symbol



Circuit Diagram

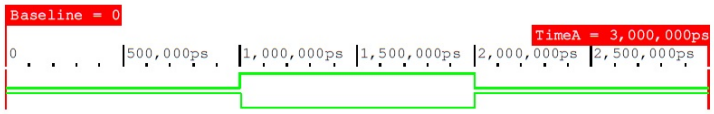
Dimensions



AC Characteristics

Signal	Delay (ps)
prop delay as 1	255.8
prop delay bs 1	244.0
prop delay as 0	247.6
prop delay bs 0	237.8
prop delay ac 1	176.7
prop delay bc 1	184.8
prop delay ac 0	157.4
prop delay bc 0	147.3

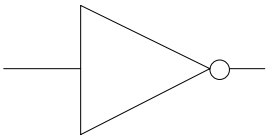
System Verilog Simulation



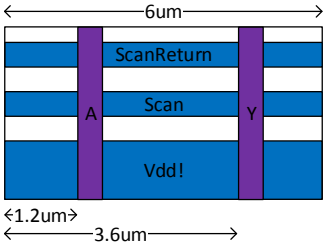
5 Inverter

Designer: Henry Lovett
Cell Description: A basic inverter gate

Symbol



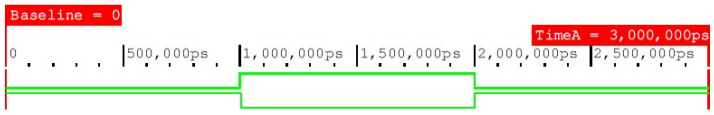
Dimensions



AC Characteristics

Signal	Delay (ps)
a rise delay	107.3
a fall delay	81.7

System Verilog Simulation

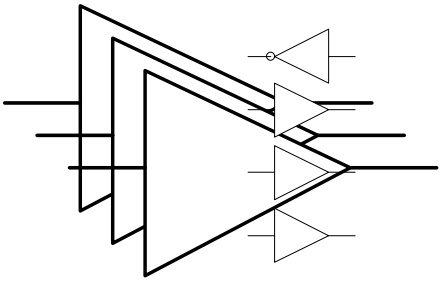


6 leftbuf

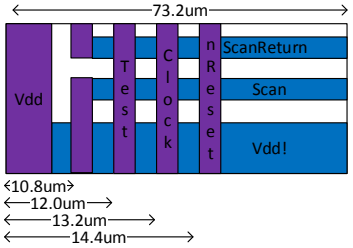
Designer: Henry Lovett
Cell Description: A start of row buffer cell.

Symbol

Circuit Diagram



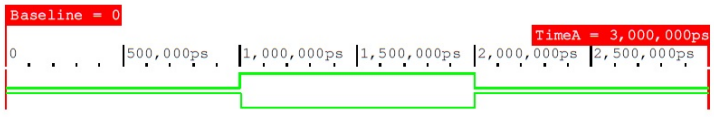
Dimensions



AC Characteristics

Signal	Delay (ps)
clock rise prop delay	287.5
clock fall prop delay	271.3
test rise prop delay	282.5
test fall prop delay	272.6
nreset rise prop delay	290.5
nreset fall prop delay	273.2
sdo rise prop delay	124.7
sdo fall prop delay	157.7

System Verilog Simulation



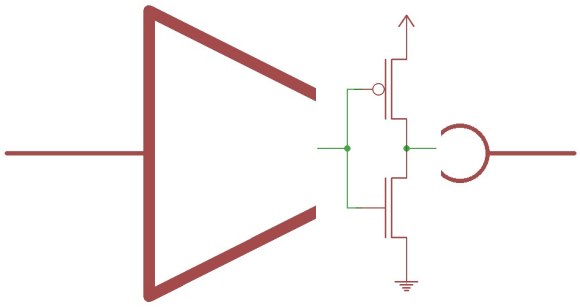
7 mux2

Designer: Constantijn Schepens
Cell Description: A two input Multiplexor

Symbol

Circuit Diagram

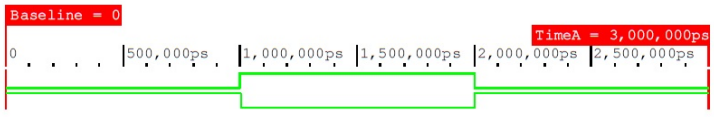
Dimensions



AC Characteristics

Signal	Delay (ps)
i1 rise propagation delay	217.3
i1 fall propagation delay	208.7
i0 rise propagation delay	180.5
i0 fall propagation delay	184.4
s pass i1 rise propagation delay	201.6
s pass i0 fall propagation delay	192.1
s pass i1 fall propagation delay	247.9
s pass i0 rise propagation delay	236.0

System Verilog Simulation

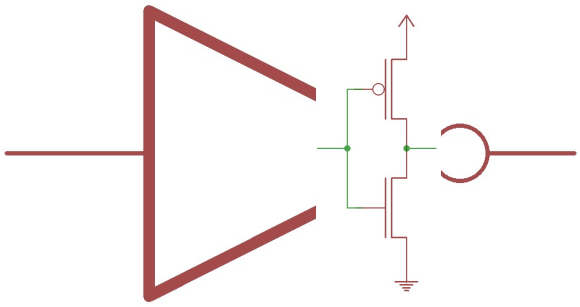


8 nand2

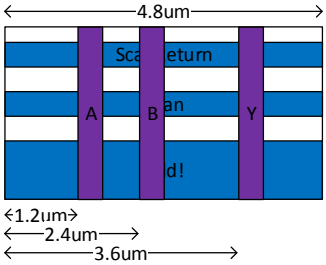
Designer: Constantijn Schepens
Cell Description: A two input NAND gate

Symbol

Circuit Diagram



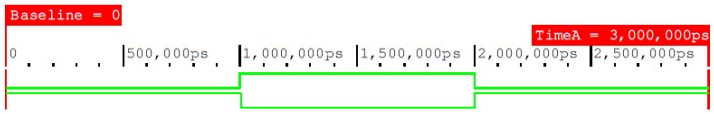
Dimensions



AC Characteristics

Signal	Delay (ps)
a rise propagation delay	118.6
a fall propagation delay	115.5
b rise propagation delay	112.8
b fall propagation delay	122.5

System Verilog Simulation

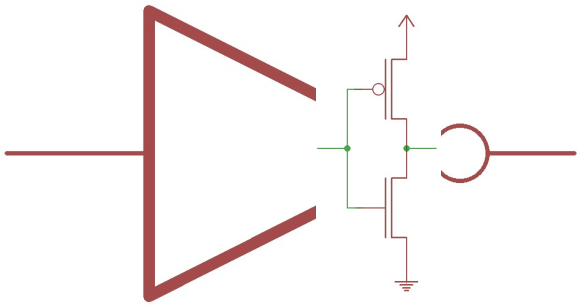


9 nand3

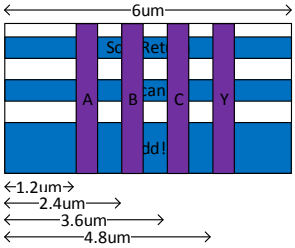
Designer: Constantijn Schepens
Cell Description: A two input NAND gate

Symbol

Circuit Diagram



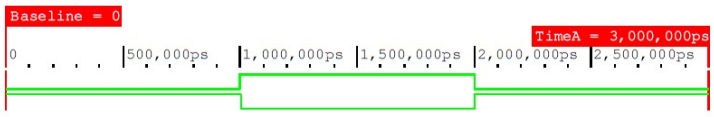
Dimensions



AC Characteristics

Signal	Delay (ps)
a rise propagation delay	128.0
a fall propagation delay	157.6
b rise propagation delay	124.9
b fall propagation delay	159.7
c rise propagation delay	116.7
c fall propagation delay	158.4

System Verilog Simulation



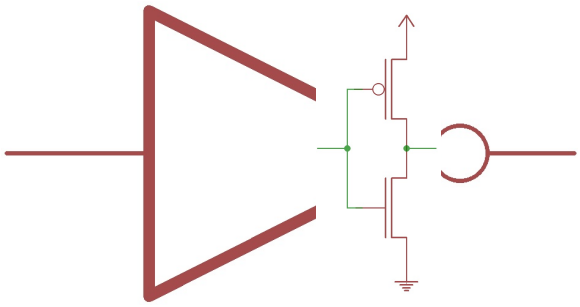
10 nand4

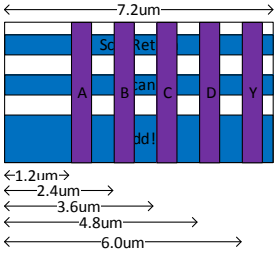
Designer: Constantijn Schepens
Cell Description: A two input NAND gate

Symbol

Circuit Diagram

Dimensions

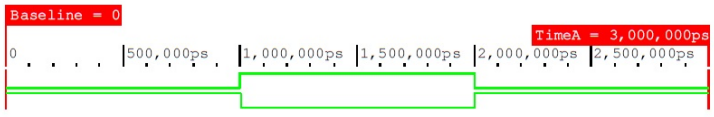




AC Characteristics

Signal	Delay (ps)
a rise propagation delay	137.5
a fall propagation delay	204.6
b rise propagation delay	132.7
b fall propagation delay	203.0
c rise propagation delay	127.7
c fall propagation delay	202.6
d rise propagation delay	121.2
d fall propagation delay	198.0

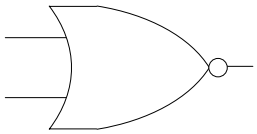
System Verilog Simulation



11 nor2

Designer: Henry Lovett
Cell Description: A two input NOR gate

Symbol



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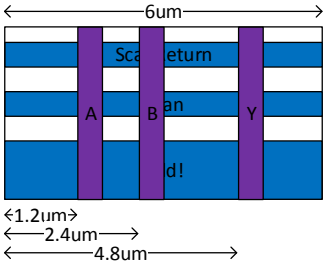
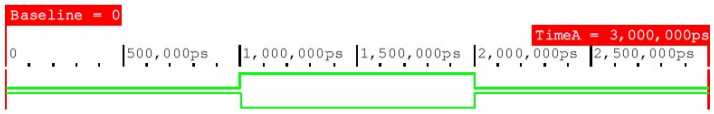


AC Characteristics

Signal	Delay (ps)
a rise prop delay	91.8
a fall prop delay	196.4
b rise prop delay	87.6
b fall prop delay	192.9

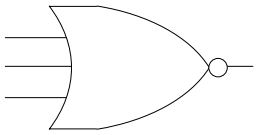
System Verilog Simulation



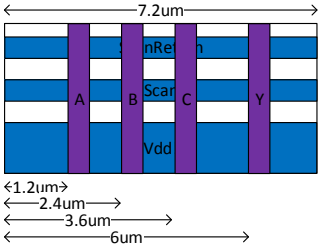
12 nor3

Designer: Henry Lovett
Cell Description: A three input NOR gate

Symbol



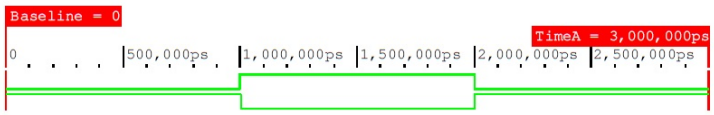
Dimensions



AC Characteristics

Signal	Delay (ps)
TO BE	DONE

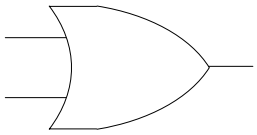
System Verilog Simulation



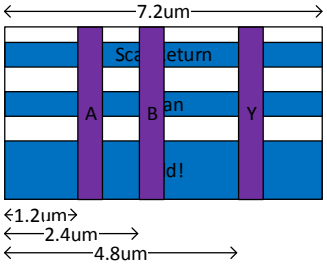
13 or2

Designer: Henry Lovett
Cell Description: A two input OR gate

Symbol



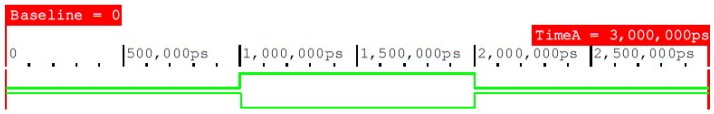
Dimensions



AC Characteristics

Signal	Delay (ps)
a fall delay	174.0
a rise delay	140.9
b fall delay	176.3
b rise delay	150.5

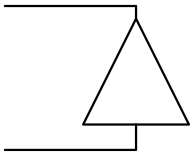
System Verilog Simulation



14 rightend

Designer: Henry Lovett
Cell Description: An end of row buffer cell.

Symbol



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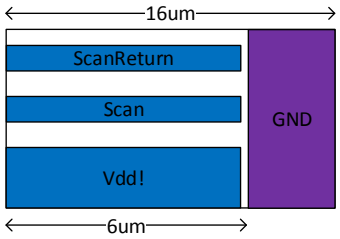
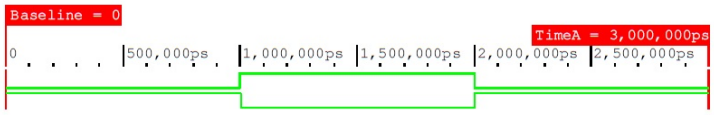


AC Characteristics

Signal	Delay (ps)
scan fall delay	56.4
scan rise delay	78.2

System Verilog Simulation



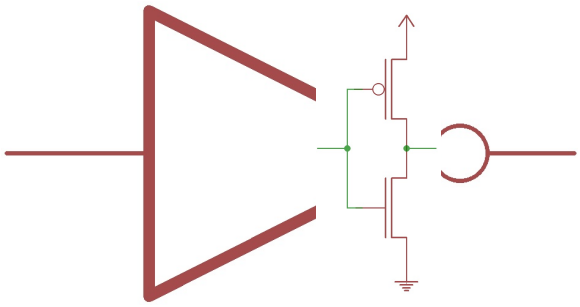
15 scandtype

Designer: Constantijn Schepens
Cell Description: A Raw DType cell

Symbol

Circuit Diagram

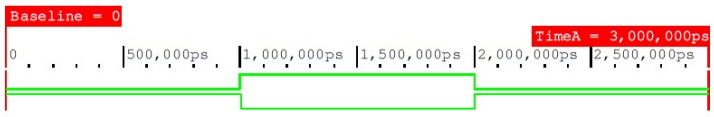
Dimensions



AC Characteristics

Signal	Delay (ps)
clock to q rise	336.9
clock to q fall	509.6
clock to nq rise	302.0
clock to nq fall	590.0
nreset to q fall	385.4
nreset to nq rise	177.7

System Verilog Simulation



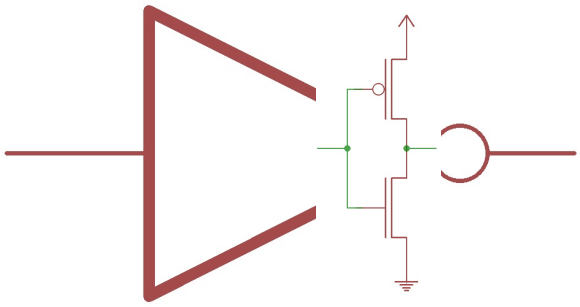
16 scanreg

Designer: Constantijn Schepens
Cell Description: A Raw DType cell

Symbol

Circuit Diagram

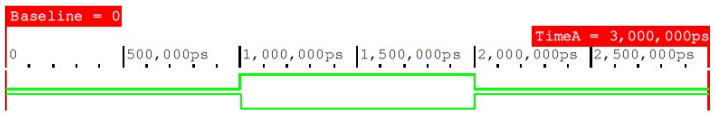
Dimensions



AC Characteristics

Signal	Delay (ps)
clock to q rise	357.2
clock to q fall	542.1
clock to nq rise	301.5
clock to nq fall	617.0
nreset to q fall	412.5
nreset to nq rise	178.3

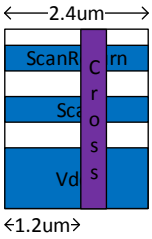
System Verilog Simulation



17 Rowcrosser

Designer: Martin Wearn
Cell Description: A row crossing cell.

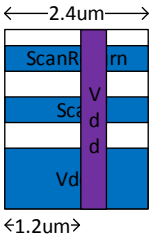
Dimensions



18 Tie High

Designer: Martin Wearn
Cell Description: A tie to Vdd cell.

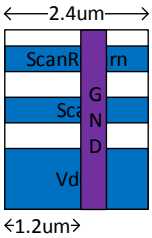
Dimensions



19 Tie Low

Designer: Martin Wearn
Cell Description: A tie low cell.

Dimensions



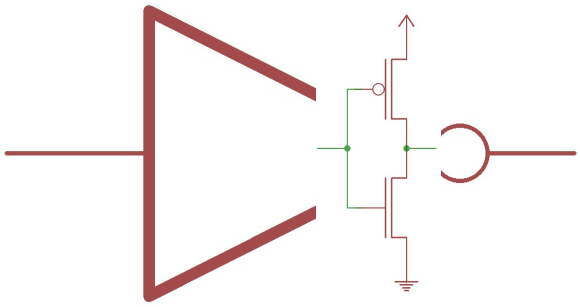
20 trisbuf

Designer: Ashley Robinson
Cell Description: A tristate buffer

Symbol

Circuit Diagram

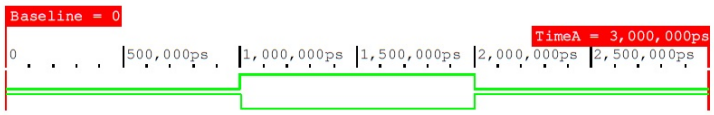
Dimensions



AC Characteristics

Signal	Delay (ps)
TO BE	DONE

System Verilog Simulation



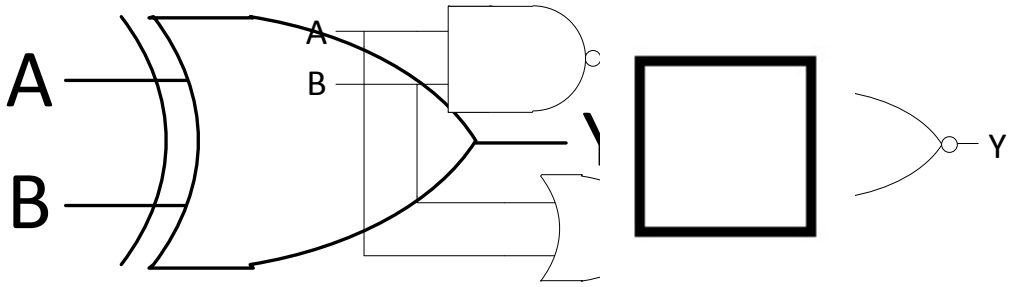
21 xor2

Designer: Ashley Robinson
Cell Description: A two input xor gate

Symbol

Circuit Diagram

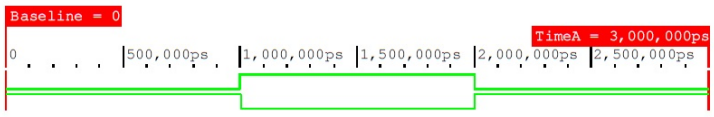
Dimensions



AC Characteristics

Signal	Delay (ps)
prop delay a 1	305.0
prop delay a 2	241.7
prop delay b 1	184.3
prop delay b 2	201.7
average prop a	273.4
average prop b	193.0

System Verilog Simulation



A Appendix A

A.1 Team Management

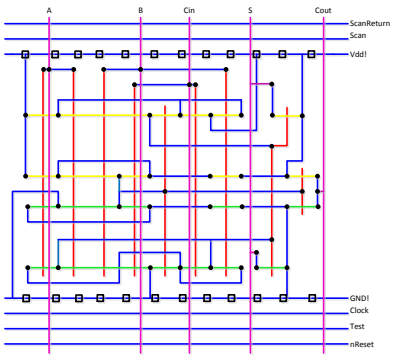
A.2 Division of Labour

B Design Detail

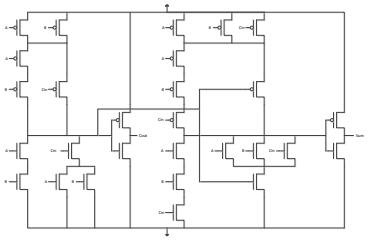
B.1 fulladder

Designer: Martin Wearn
Cell Description: Adds two bit values and the previous bitslice carry out, to produce a sum and carry

Stick Diagram



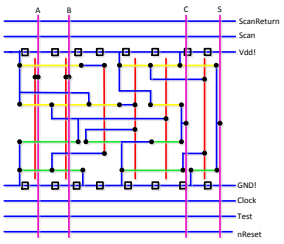
Transistor Level Circuit Diagram



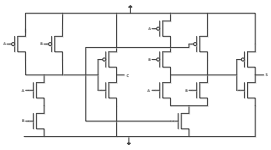
B.2 halfadder

Designer: Martin Wearn
Cell Description: Adds two bits to produce a sum and carry

Stick Diagram



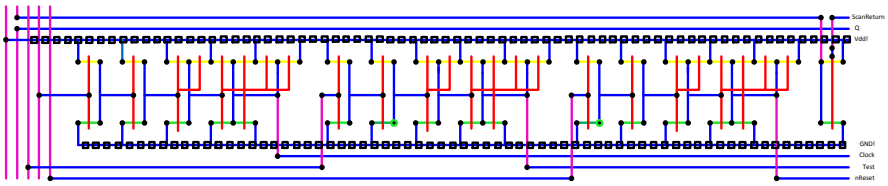
Transistor Level Circuit Diagram



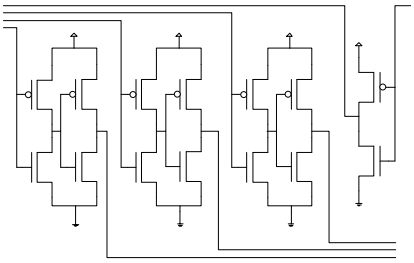
B.3 leftbuf

Designer: Henry Lovett
Cell Description: A start of row buffer cell.

Stick Diagram



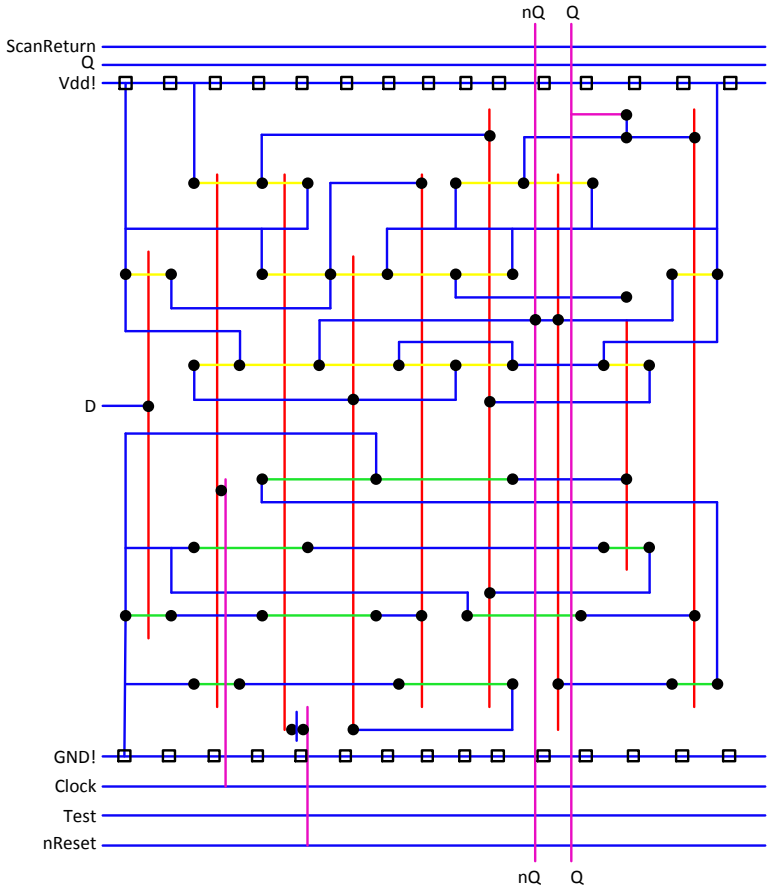
Transistor Level Circuit Diagram



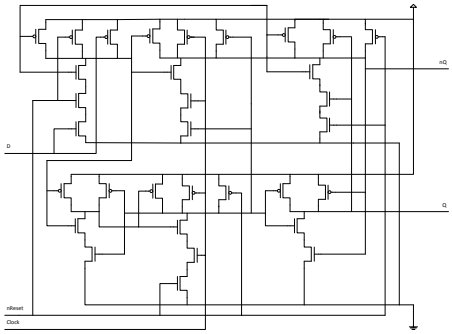
B.4 rdtype

Designer: Ashley Robinson
Cell Description: Raw Dtype

Stick Diagram



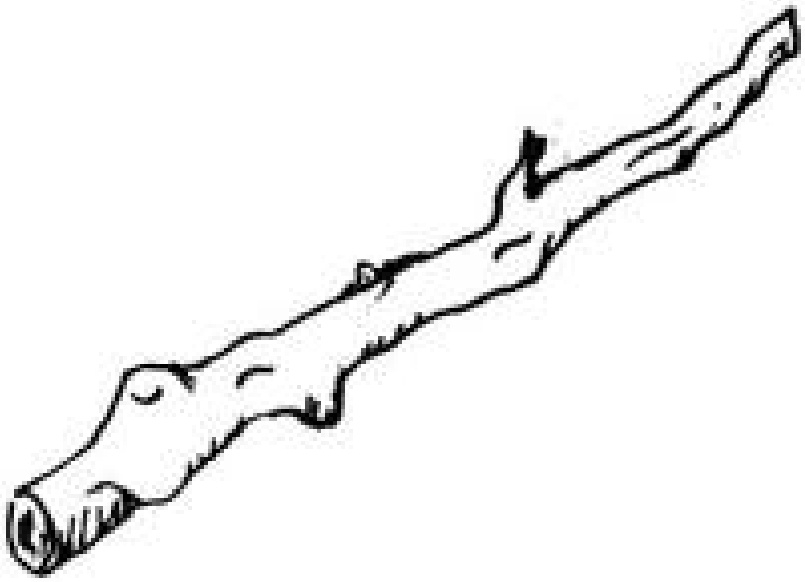
Transistor Level Circuit Diagram



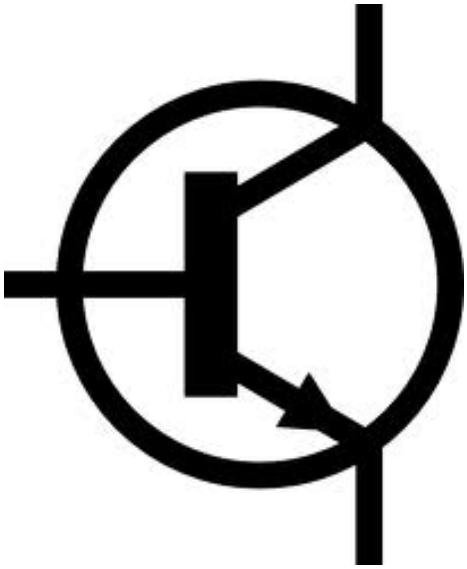
B.5 smux2

Designer: Schep
Cell Description: A start of row buffer cell.

Stick Diagram



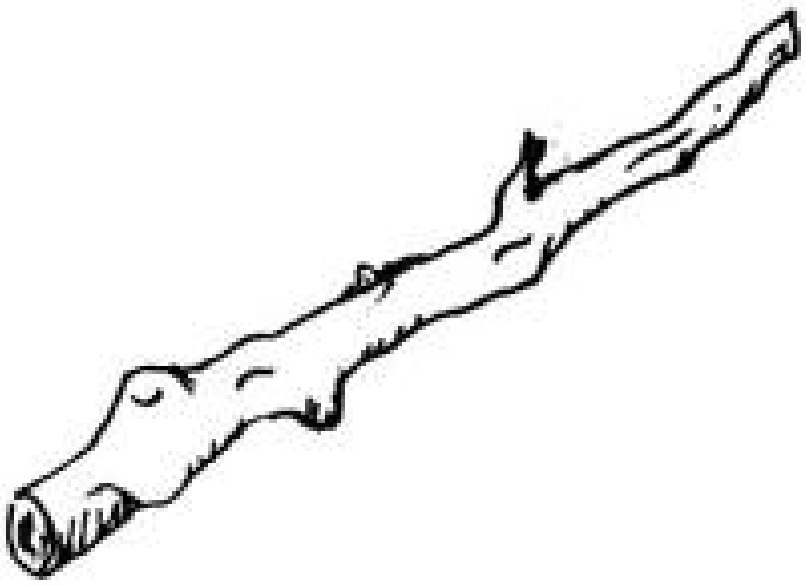
Transistor Level Circuit Diagram



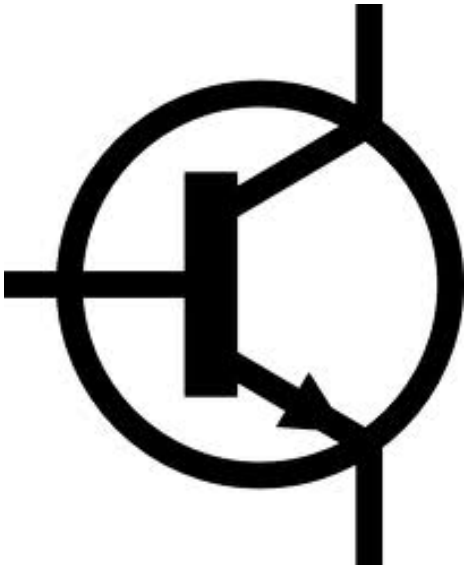
B.6 smux3

Designer: Schep
Cell Description: A scan multiplexor.

Stick Diagram



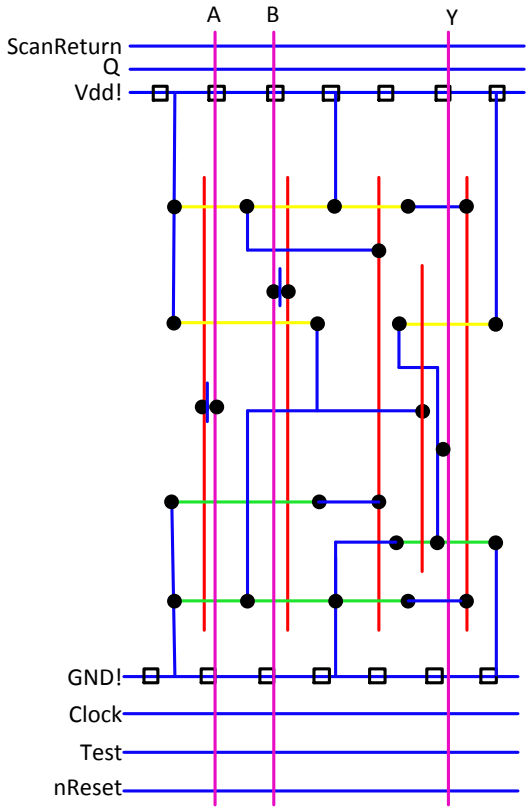
Transistor Level Circuit Diagram



B.7 xor2

Designer: Ashley Robinson
Cell Description: A 2 input XOR gate.

Stick Diagram



Transistor Level Circuit Diagram