## Cell Library Databook

by Team S5

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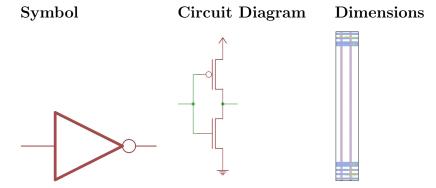
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## Inverter

**Designer:** Henry Lovett

Cell Description: A basic inverter gate



**AC** Characteristics

Signal	Delay (s)
a rise delay	1.306e-10
a fall delay	9.373e-11

## System Verilog Simulation

