Cell Library Databook

by Team S5
H. Lovett (hl13g10)
A. J. Robinson (ajr2g10)
C. Schepens (cs7g10)
M. Wearn (mw20g10)

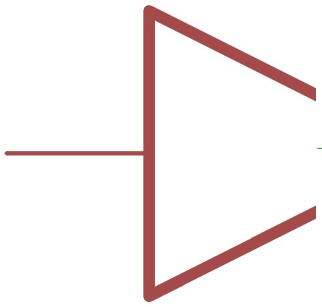
December 9, 2013

Contents

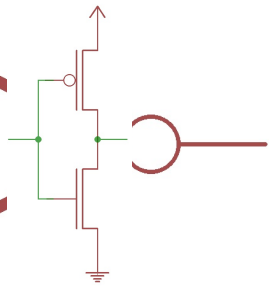
1 And2

Designer: Constantijn Schepens
Cell Description: A two input AND gate

Symbol



Circuit Diagram

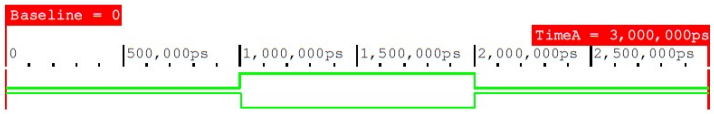


Dimensions

AC Characteristics

Signal	Delay (ps)
TO BE	DONE

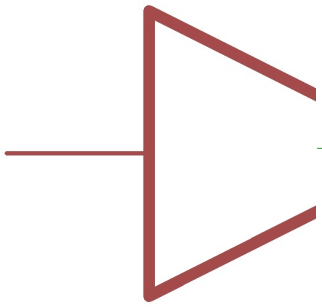
System Verilog Simulation



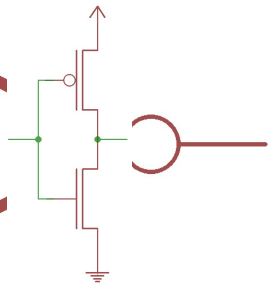
2 buffer

Designer: Ashley Robinson
Cell Description: A non-inverting buffer

Symbol



Circuit Diagram

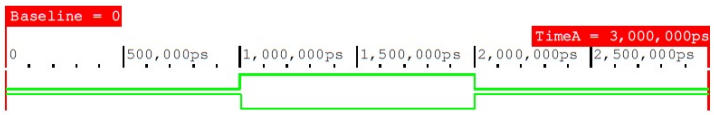


Dimensions

AC Characteristics

Signal	Delay (ps)
A to Y	134.2

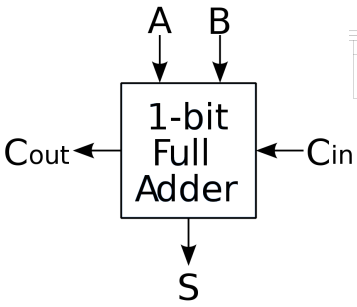
System Verilog Simulation



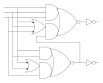
3 fulladder

Designer: Martin Wearn
Cell Description: Adds two bit values and the previous bitsclie carry out, to produce a sum and carry

Symbol



Circuit Diagram



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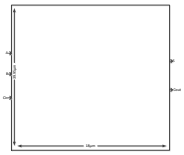
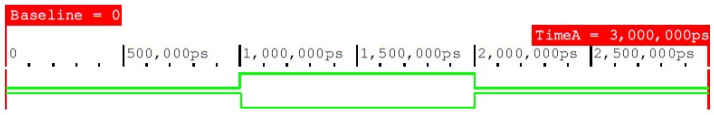


AC Characteristics

A to S/Cout prop delay (tPA) 331.7ps B to S/Cout prop delay (tPB) 358.3ps Cin to S/Cout prop delay (tP

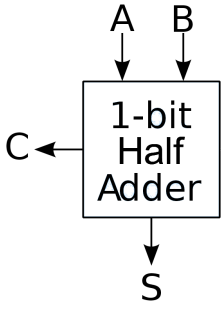
System Verilog Simulation



4 halfadder

Designer: Martin Wearn
Cell Description: Adds two bits to produce a sum and carry

Symbol



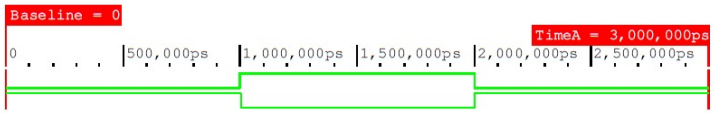
Circuit Diagram

Dimensions

AC Characteristics

Signal	Delay (ps)
A to S/Cout prop delay (tPA)	256.2ps
B to S/Cout prop delay (tPB)	242.8ps

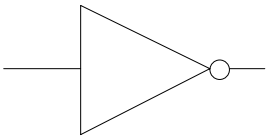
System Verilog Simulation



5 Inverter

Designer: Henry Lovett
Cell Description: A basic inverter gate

Symbol



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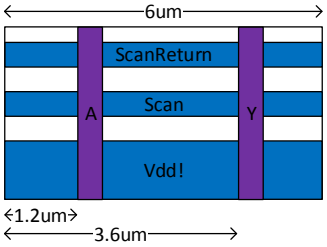
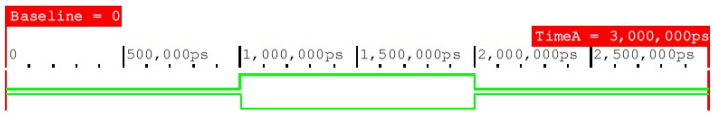


AC Characteristics

Signal	Delay (ps)
TO BE	DONE

System Verilog Simulation

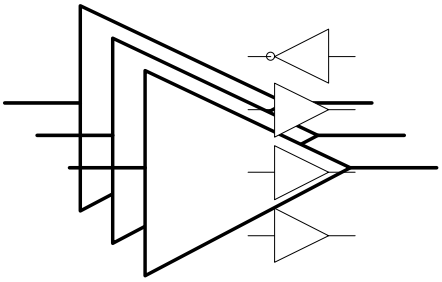


6 leftbuf

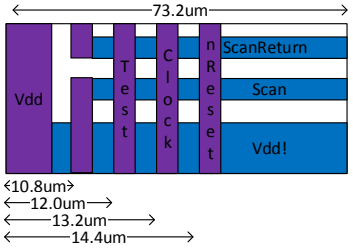
Designer: Henry Lovett
Cell Description: A start of row buffer cell.

Symbol

Circuit Diagram



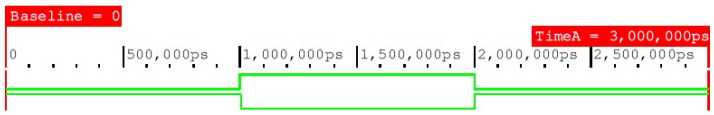
Dimensions



AC Characteristics

Signal	Delay (ps)
TO BE	DONE

System Verilog Simulation



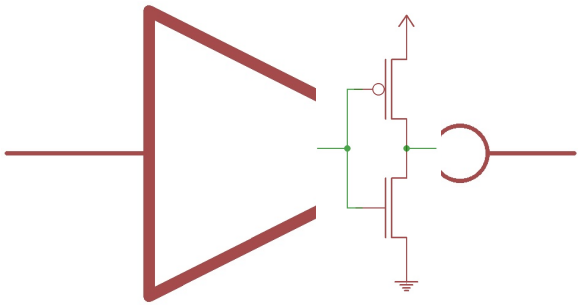
7 mux2

Designer: Constantijn Schepens
Cell Description: A two input Multiplexor

Symbol

Circuit Diagram

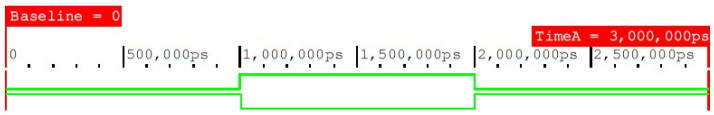
Dimensions



AC Characteristics

Signal	Delay (ps)
TO BE	DONE

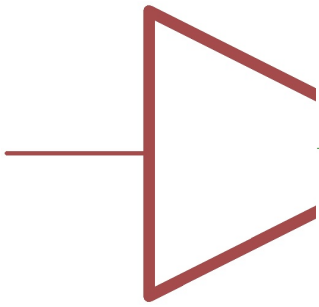
System Verilog Simulation



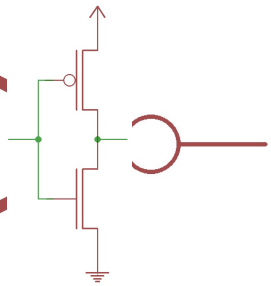
8 nand2

Designer: Constantijn Schepens
Cell Description: A two input NAND gate

Symbol



Circuit Diagram

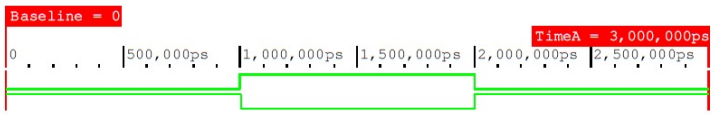


Dimensions

AC Characteristics

Signal	Delay (ps)
TO BE	DONE

System Verilog Simulation



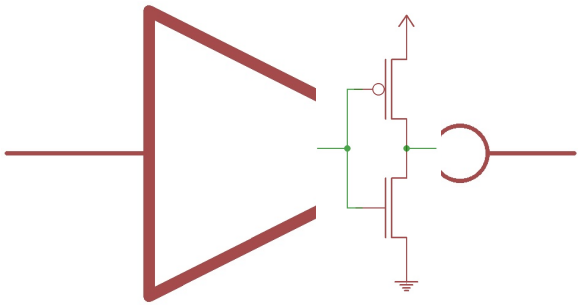
9 nand3

Designer: Constantijn Schepens
Cell Description: A two input NAND gate

Symbol

Circuit Diagram

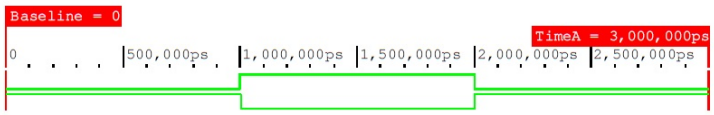
Dimensions



AC Characteristics

Signal	Delay (ps)
TO BE	DONE

System Verilog Simulation



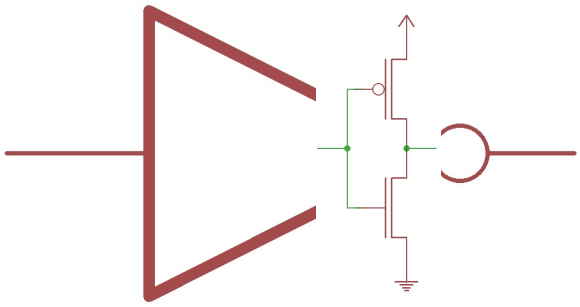
10 nand4

Designer: Constantijn Schepens
Cell Description: A two input NAND gate

Symbol

Circuit Diagram

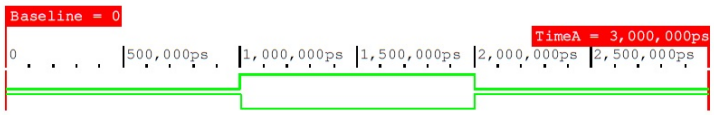
Dimensions



AC Characteristics

Signal	Delay (ps)
TO BE	DONE

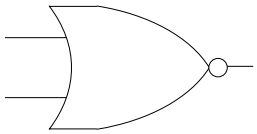
System Verilog Simulation



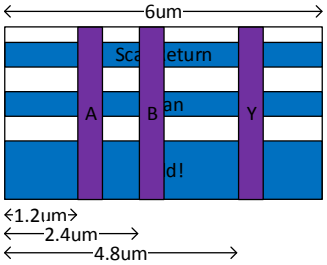
11 nor2

Designer: Henry Lovett
Cell Description: A two input NOR gate

Symbol



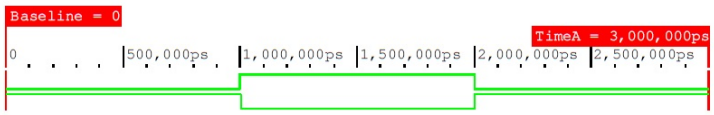
Dimensions



AC Characteristics

Signal	Delay (ps)
TO BE	DONE

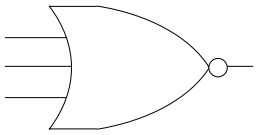
System Verilog Simulation



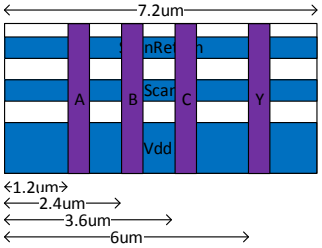
12 nor3

Designer: Henry Lovett
Cell Description: A three input NOR gate

Symbol



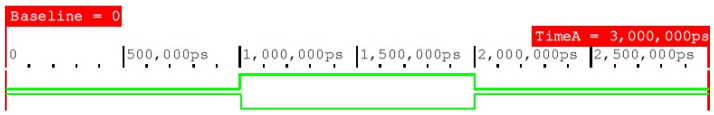
Dimensions



AC Characteristics

Signal	Delay (ps)
TO BE	DONE

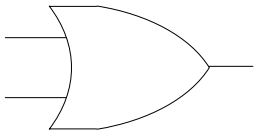
System Verilog Simulation



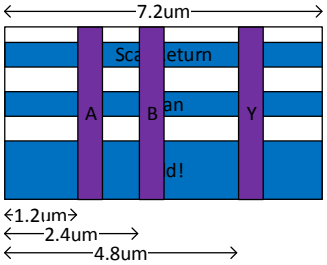
13 or2

Designer: Henry Lovett
Cell Description: A two input OR gate

Symbol



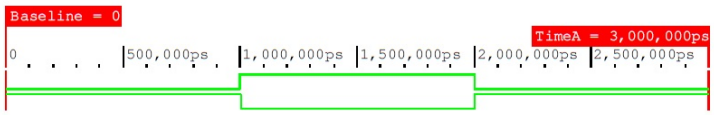
Dimensions



AC Characteristics

Signal	Delay (ps)
TO BE	DONE

System Verilog Simulation



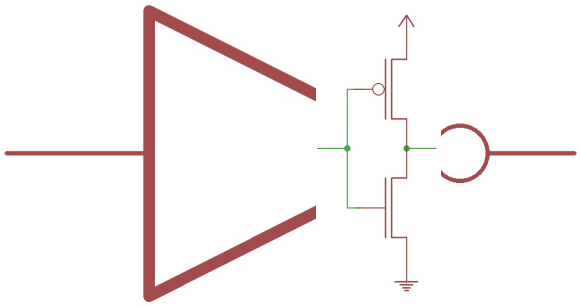
14 rightend

Designer: Henry Lovett
Cell Description: An end of row buffer cell.

Symbol

Circuit Diagram

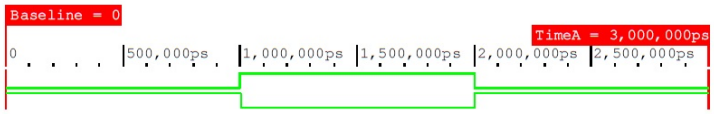
Dimensions



AC Characteristics

Signal	Delay (ps)
TO BE	DONE

System Verilog Simulation



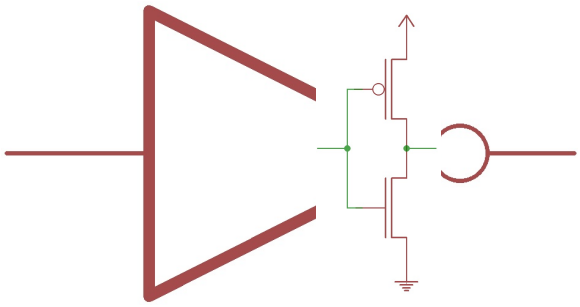
15 rowcrosser

Designer: Martin Wearn
Cell Description: A rowcrossing cell

16 scandtype

Designer: Constantijn Schepens
Cell Description: A Raw DType cell

Symbol



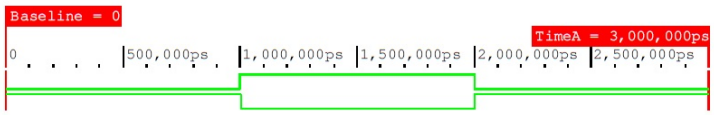
Circuit Diagram

Dimensions

AC Characteristics

Signal	Delay (ps)
TO BE	DONE

System Verilog Simulation



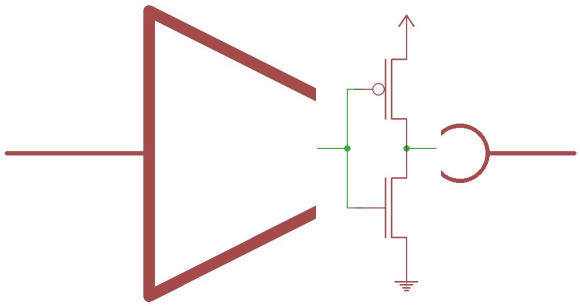
17 scanreg

Designer: Constantijn Schepens
Cell Description: A Raw DType cell

Symbol

Circuit Diagram

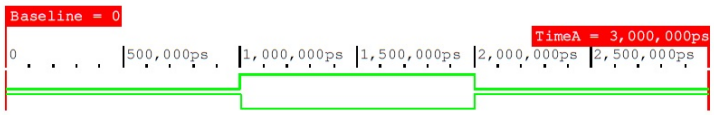
Dimensions



AC Characteristics

Signal	Delay (ps)
TO BE	DONE

System Verilog Simulation



18 tiehigh

Designer: Martin Wearn
Cell Description: A tie to Vdd cell

19 tielow

Designer: Martin Wearn
Cell Description: A tie to GND cell

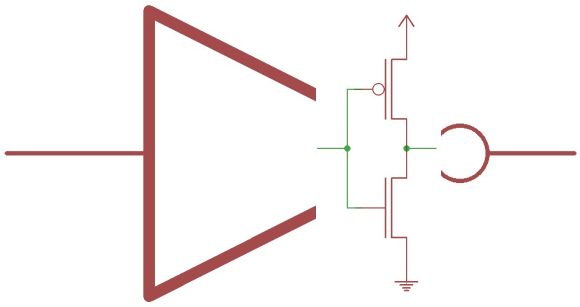
20 trisbuf

Designer: Ashley Robinson
Cell Description: A tristate buffer

Symbol

Circuit Diagram

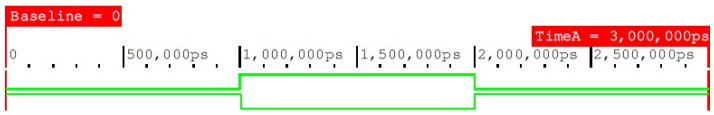
Dimensions



AC Characteristics

Signal	Delay (ps)
TO BE	DONE

System Verilog Simulation



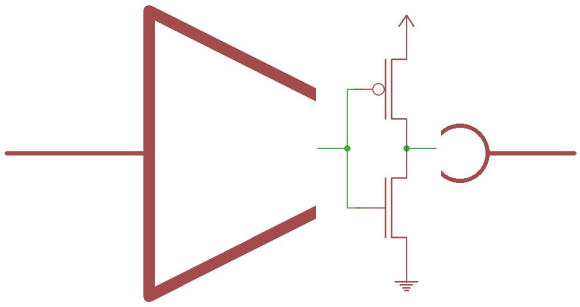
21 xor2

Designer: Ashley Robinson
Cell Description: A two input xor gate

Symbol

Circuit Diagram

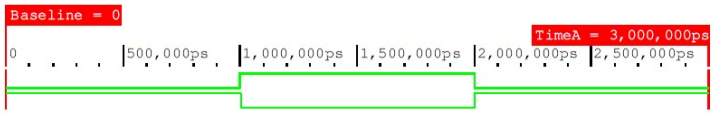
Dimensions



AC Characteristics

Signal	Delay (ps)
A to Y	273.4
B to Y	193

System Verilog Simulation



A Appendix A

A.1 Team Management

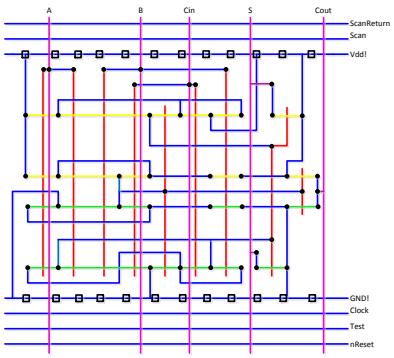
A.2 Division of Labour

B Design Detail

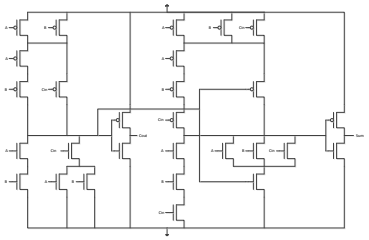
B.1 fulladder

Designer: Martin Wearn
Cell Description: Adds two bit values and the previous bitslice carry out, to produce a sum and carry

Stick Diagram



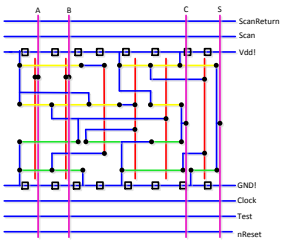
Transistor Level Circuit Diagram



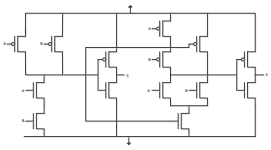
B.2 halfadder

Designer: Martin Wearn
Cell Description: Adds two bits to produce a sum and carry

Stick Diagram



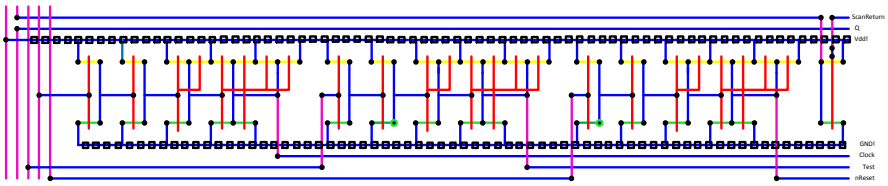
Transistor Level Circuit Diagram



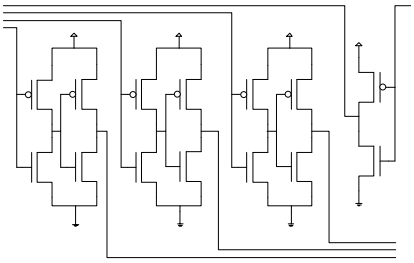
B.3 leftbuf

Designer: Henry Lovett
Cell Description: A start of row buffer cell.

Stick Diagram



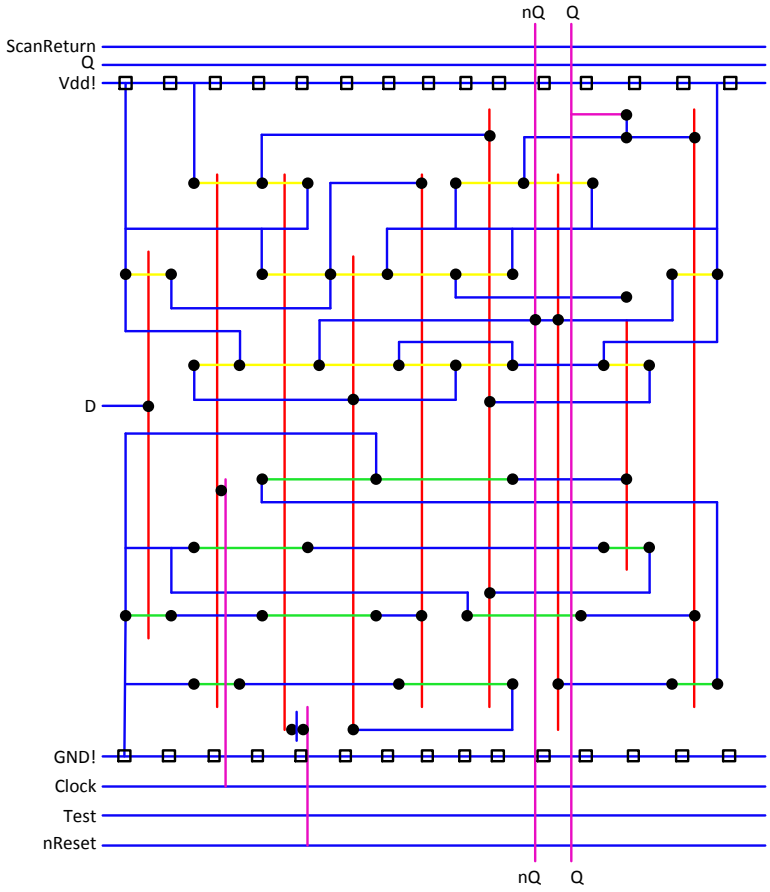
Transistor Level Circuit Diagram



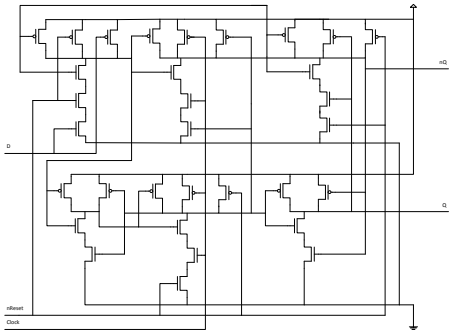
B.4 rdtype

Designer: Ashley Robinson
Cell Description: Raw Dtype

Stick Diagram



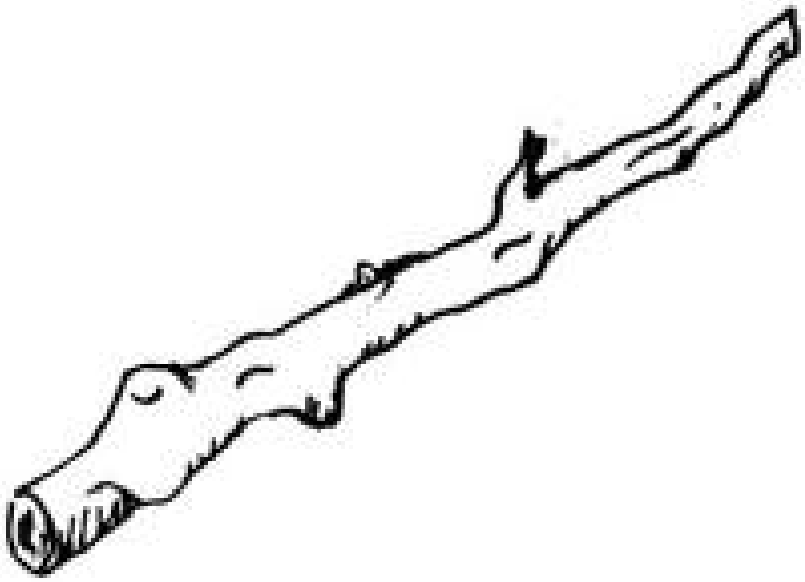
Transistor Level Circuit Diagram



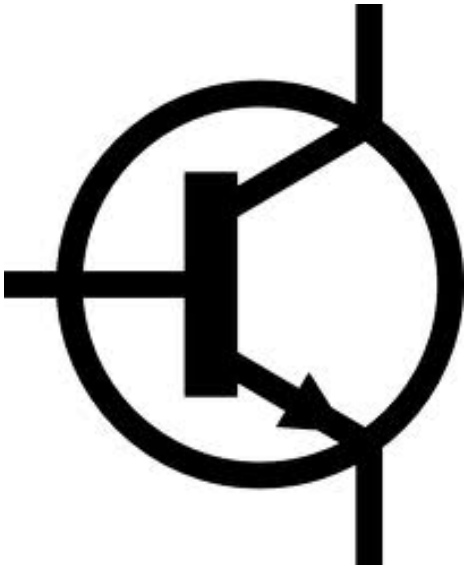
B.5 smux2

Designer: Schep
Cell Description: A start of row buffer cell.

Stick Diagram



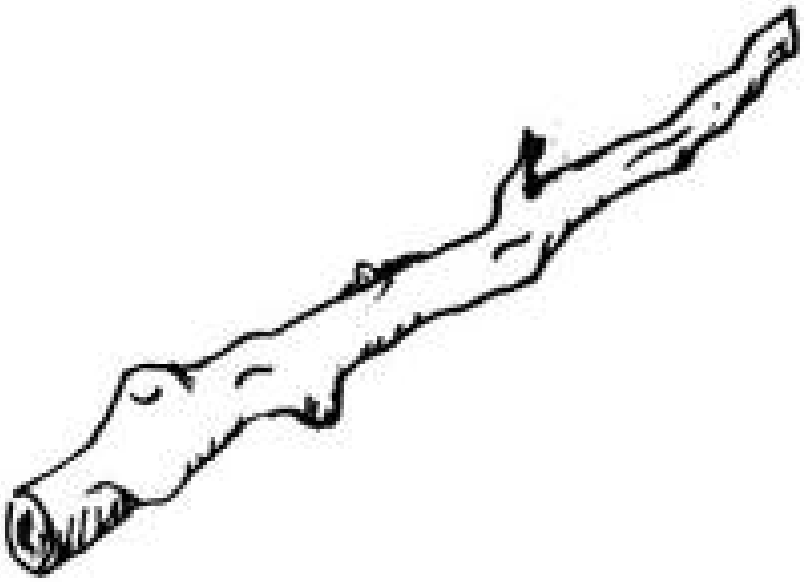
Transistor Level Circuit Diagram



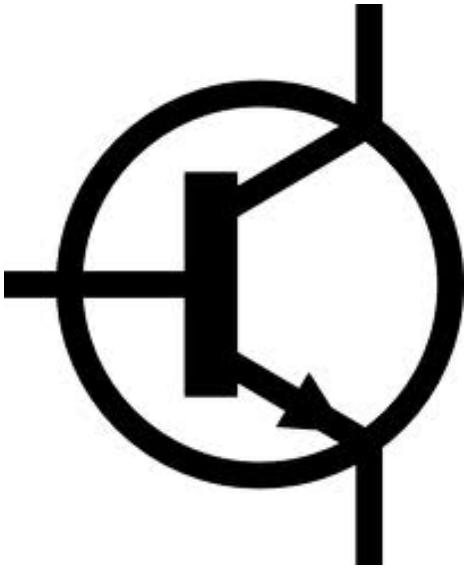
B.6 smux3

Designer: Schep
Cell Description: A scan multiplexor.

Stick Diagram



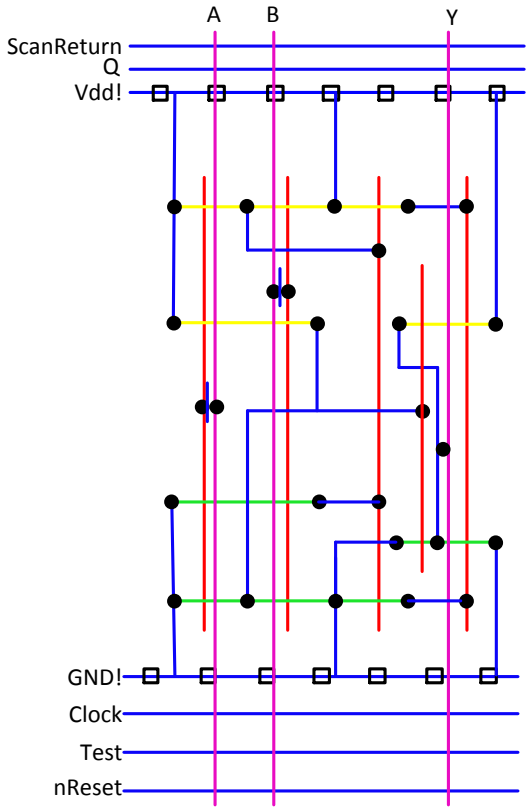
Transistor Level Circuit Diagram



B.7 xor2

Designer: Ashley Robinson
Cell Description: A 2 input XOR gate.

Stick Diagram



Transistor Level Circuit Diagram