

# Cell Library Databook

by Team S5

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## i Introduction

The set of cells contained within this library are based upon  $0.35\mu m$  unified CMOS technology. They follow a two-layer metal design on top of a p-type substrate with N-Well and P-Well regions for pull-up and pull-down networks respectively. All cells are a common  $17.2\mu m$  high, with varied widths all integer multiples of  $1.2\mu m$ . All transistors are fixed at  $W_P = 2.4\mu m$ ,  $L_P = 0.35\mu m$ ,  $W_N = 1.5\mu m$ ,  $L_N = 0.35\mu m$ .

Global signals and power rails are arranged horizontally in *metal1*. Figure 1 shows this arrangement with the dimensions of the global signals. While cell I/O signals are arranged vertically in *metal2* and aligned to a  $1.2\mu m$  grid. Power rails are  $1.25\mu m$  wide, while other horizontal signals are  $0.5\mu m$  wide. The distance between horizontal signals is  $0.8\mu m$  from centre to centre. Both rails are formed using a continuous ohmic region and line of taps.

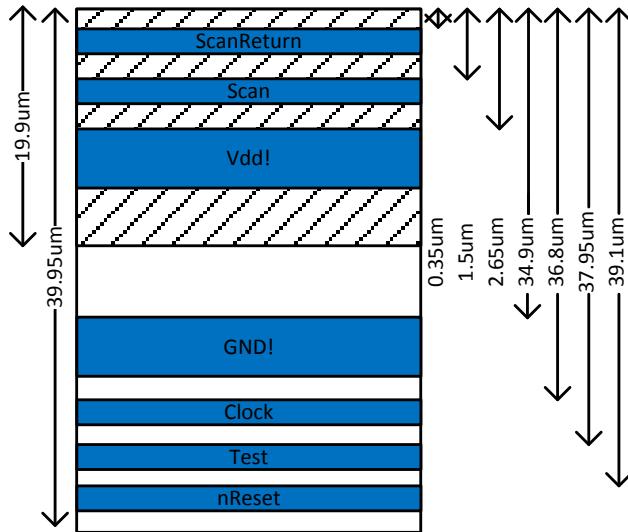


Figure 1: Global signals common to all cells

Vertical signals lines are  $0.6\mu m$  wide with position of each signal measured from the left edge of the cell to the right edge of the metal strip and detailed on each cell page.

AC characteristics of cells are measured as the propagation delay from each input to each output under normal operation conditions. This is set as having each input driven through one inverter and each output loaded by two inverters from this library. Each cell lists both the delay to correct output as a result of an input going high, as well as an input going low.

Major cells in the library have additional sections detailing the stick diagram and transistor layout of each cell as designed by the designated team member. Even though only 4 members were in the group, both the half adder and XOR2 have been included in the library and detailed.

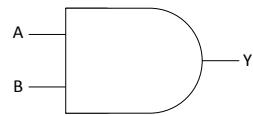
# CELL LIBRARY DATABOOK

## 1 .1 AND2

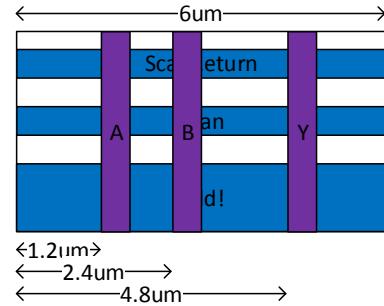
**Designer:** Constantijn Schepens

**Cell Description:** A two input AND gate

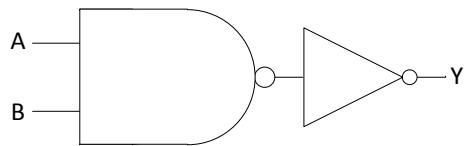
**Symbol**



**Dimensions**



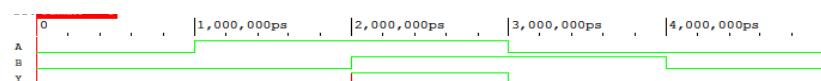
**Gate Level Diagram**



**AC Characteristics**

Signal	Average Delay (ps)
a to y	121.7
b to y	124.0

**System Verilog Simulation**



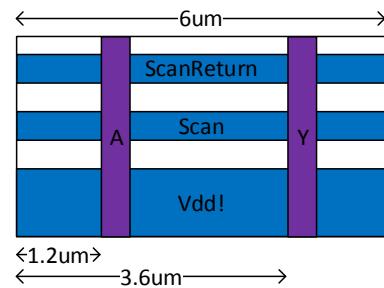
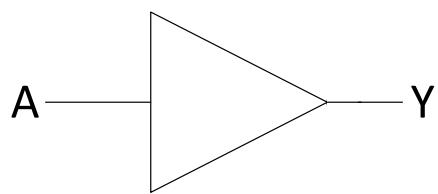
## 1 .2 BUFFER

**Designer:** Ashley Robinson

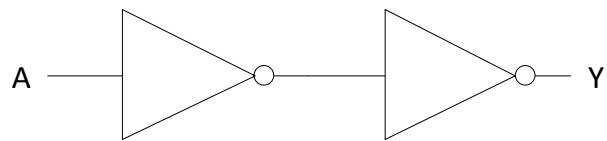
**Cell Description:** A non-inverting buffer

Dimensions

Symbol



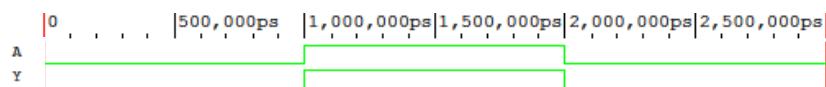
Gate Level Diagram



AC Characteristics

Signal	Average Delay (ps)
a to y	134.2

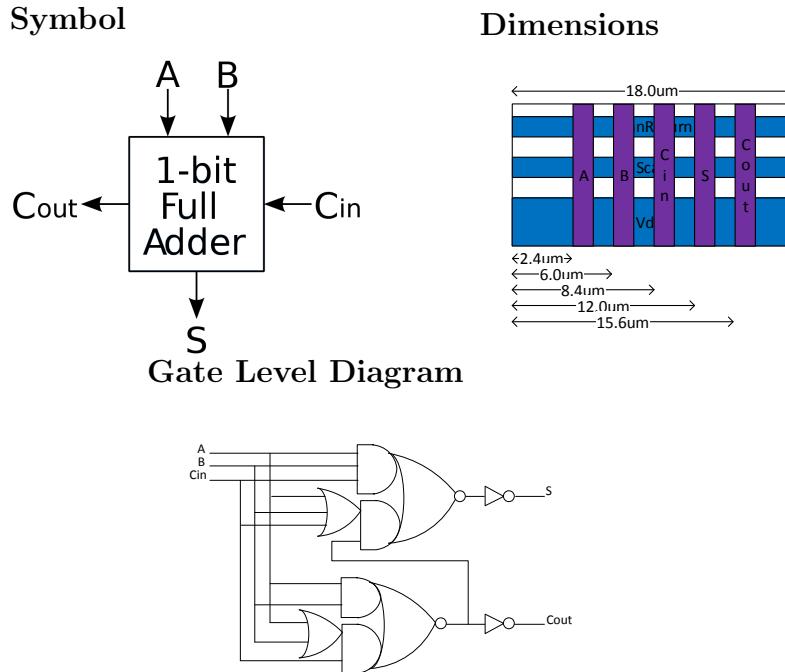
System Verilog Simulation



### 1 .3 FULLADDER

**Designer:** Martin Wearn

**Cell Description:** Adds two bit values and the previous bits clie carry out, to produce a sum and carry



### AC Characteristics

Signal	Average Delay (ps)
a to s	294.9
a to cout	285.0
b to s	262.3
b to cout	294.0
cin to s	252.7
cin to cout	274.6

### System Verilog Simulation

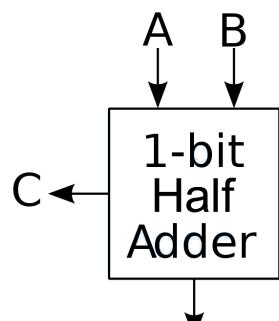


## 1 .4 HALFADDER

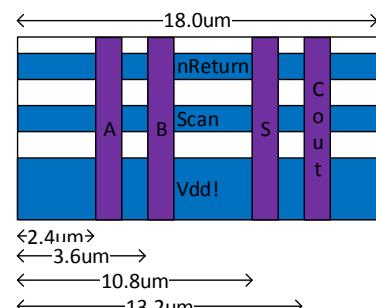
**Designer:** Martin Wearn

**Cell Description:** Adds two bits to produce a sum and carry

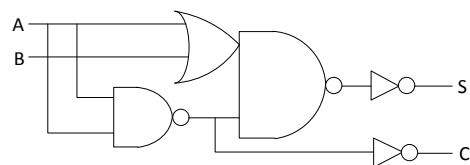
Symbol



Dimensions



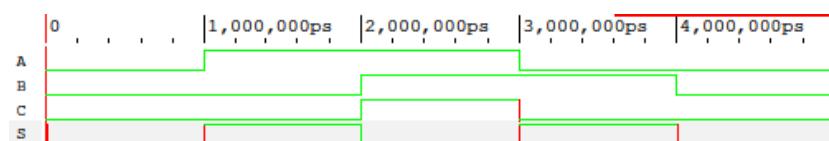
Gate Level Diagram



AC Characteristics

Signal	Average Delay (ps)
a to s	251.7
a to c	167.0
b to s	240.9
b to c	166.1

System Verilog Simulation

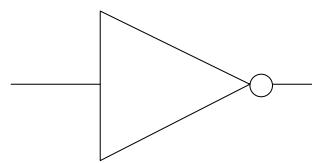


## 1 .5 INV

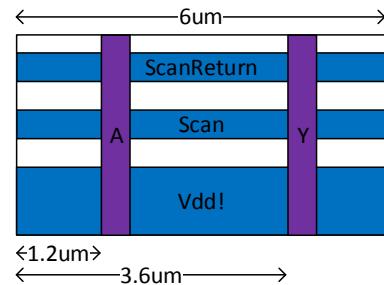
**Designer:** Henry Lovett

**Cell Description:** A basic inverter gate

**Symbol**



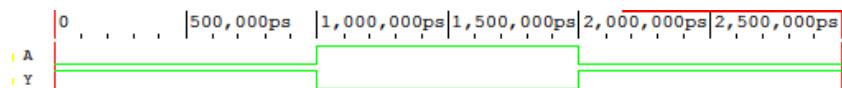
**Dimensions**



### AC Characteristics

Signal	Average Delay (ps)
a to y	94.5

### System Verilog Simulation

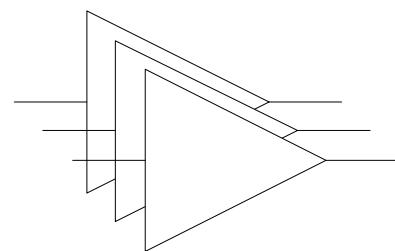


## 1 .6 LEFTBUF

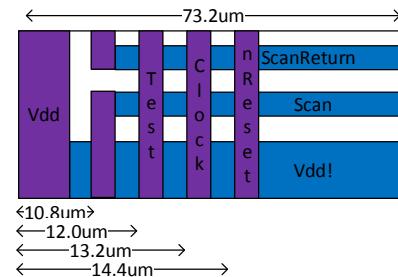
**Designer:** Henry Lovett

**Cell Description:** A start of row buffer cell.

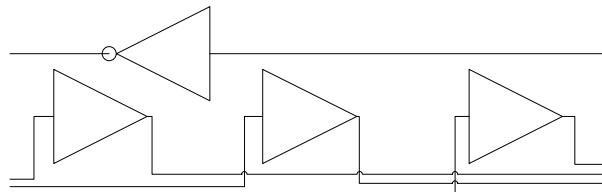
**Symbol**



**Dimensions**



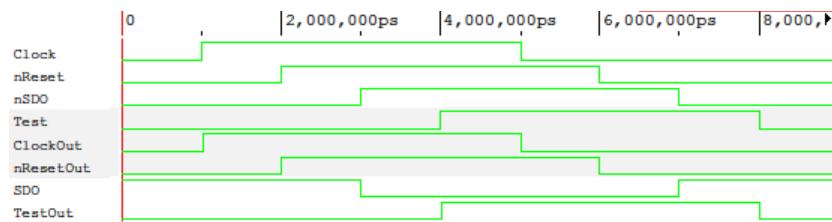
**Gate Level Diagram**



**AC Characteristics**

Signal	Average Delay (ps)
clock to clockout	279.4
test to testout	277.6
nreset to nresetout	281.9
nsdo to sdo	141.2

**System Verilog Simulation**

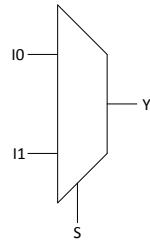


## 1 .7 MUX2

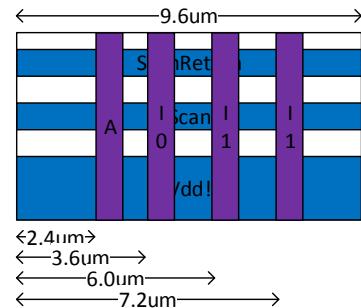
**Designer:** Constantijn Schepens

**Cell Description:** A two input Multiplexor

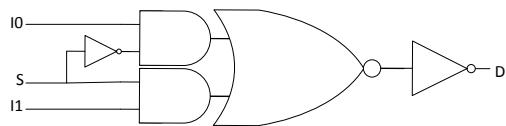
Symbol



Dimensions



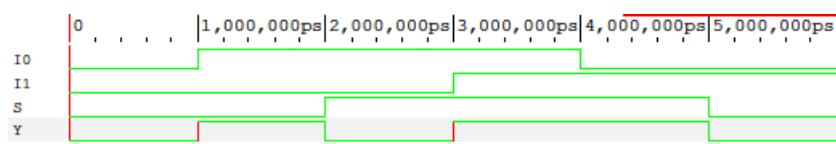
Gate Level Diagram



AC Characteristics

Signal	Average Delay (ps)
i0 to d	182.5
i1 to d	213.0
s pass i0 propagation	214.0
s pass i1 propagation	224.7

System Verilog Simulation



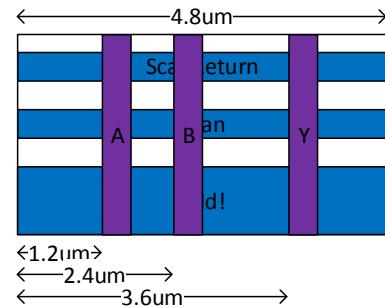
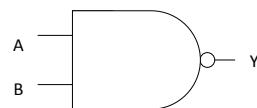
## 1 .8 NAND2

**Designer:** Constantijn Schepens

**Cell Description:** A two input NAND gate

### Dimensions

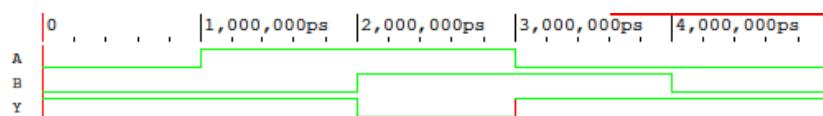
#### Symbol



### AC Characteristics

Signal	Average Delay (ps)
a to y	117.0
b to y	117.6

### System Verilog Simulation



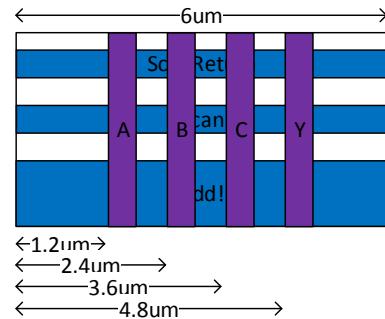
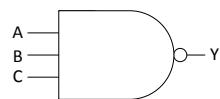
## 1 .9 NAND3

**Designer:** Constantijn Schepens

**Cell Description:** A three input NAND gate

### Dimensions

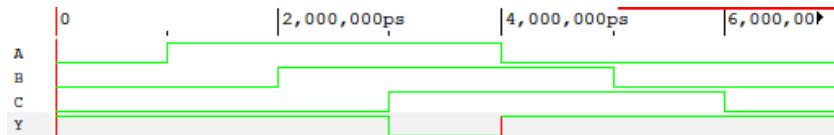
#### Symbol



### AC Characteristics

Signal	Average Delay (ps)
a to y	142.8
b to y	142.3
c to y	137.5

### System Verilog Simulation



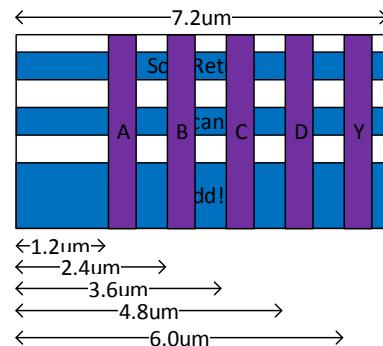
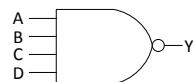
## 1 .10 NAND4

**Designer:** Constantijn Schepens

**Cell Description:** A four input NAND gate

### Dimensions

#### Symbol



### AC Characteristics

Signal	Average Delay (ps)
a to y	171.0
b to y	167.9
c to y	165.1
d to y	159.6

### System Verilog Simulation

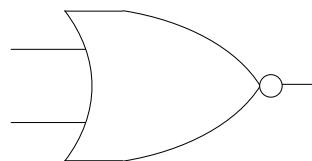


## 1.11 NOR2

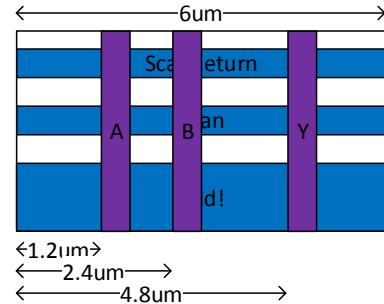
**Designer:** Henry Lovett

**Cell Description:** A two input NOR gate

**Symbol**



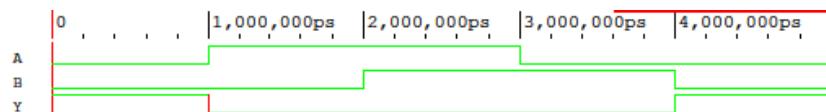
**Dimensions**



### AC Characteristics

Signal	Average Delay (ps)
a to y	144.1
b to y	140.2

### System Verilog Simulation

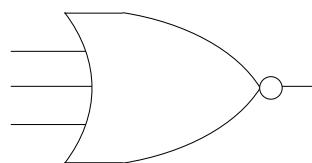


## 1.12 NOR3

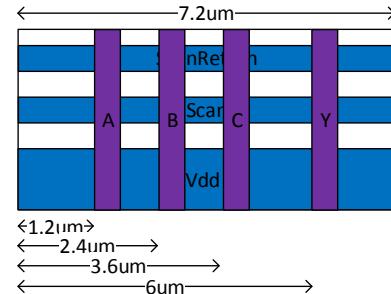
**Designer:** Henry Lovett

**Cell Description:** A three input NOR gate

**Symbol**



**Dimensions**



### AC Characteristics

Signal	Average Delay (ps)
a to y	203.1
b to y	185.4
c to y	198.1

### System Verilog Simulation

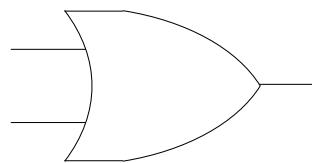


## 1 .13 OR2

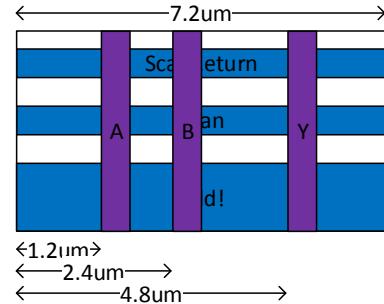
**Designer:** Henry Lovett

**Cell Description:** A two input OR gate

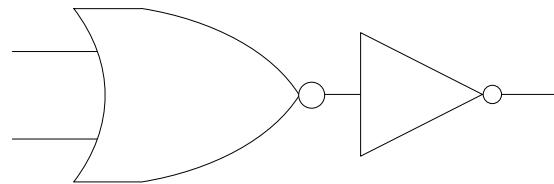
**Symbol**



**Dimensions**



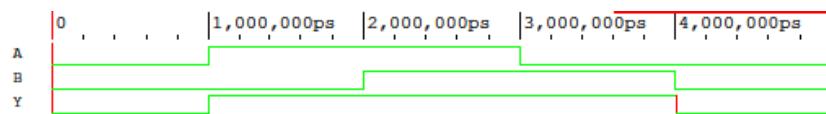
**Gate Level Diagram**



**AC Characteristics**

Signal	Average Delay (ps)
a to y	157.4
b to y	163.4

**System Verilog Simulation**

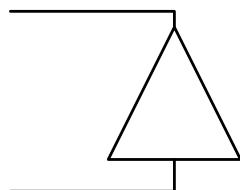


## 1 .14 RIGHTEND

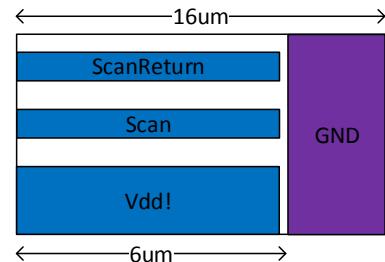
**Designer:** Henry Lovett

**Cell Description:** An end of row buffer cell.

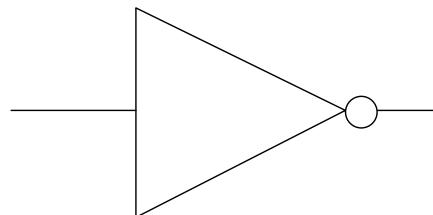
### Symbol



### Dimensions



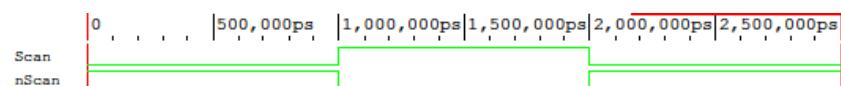
### Gate Level Diagram



### AC Characteristics

Signal	Average Delay (ps)
nsdo to sdo	67.3

### System Verilog Simulation

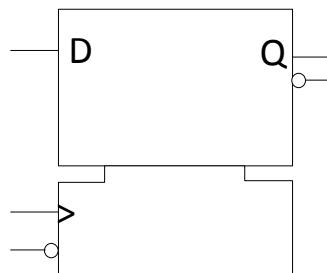


## 1 .15 SCANDTYPE

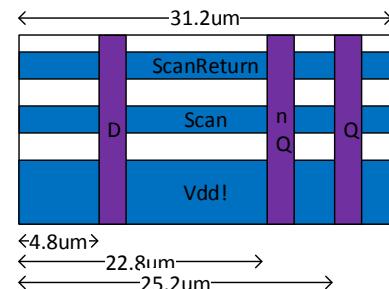
**Designer:** Constantijn Schepens

**Cell Description:** A scannable D-Type cell

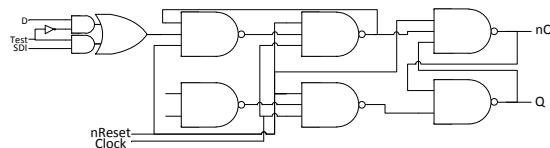
**Symbol**



**Dimensions**



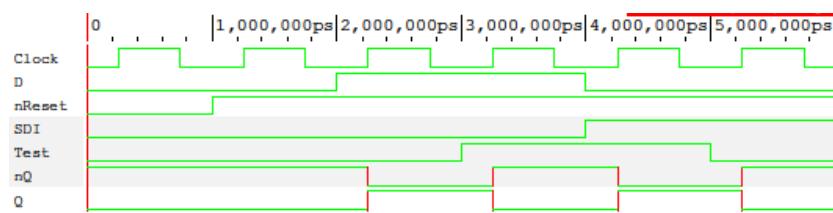
**Gate Level Diagram**



**AC Characteristics**

Signal	Average Delay (ps)
clock to q	423.3
clock to nq	446.0
nreset to clear	281.5

**System Verilog Simulation**

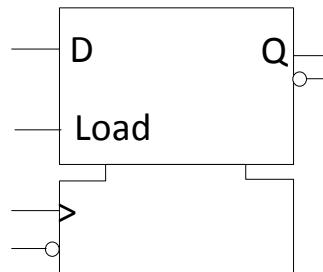


## 1 .16 SCANREG

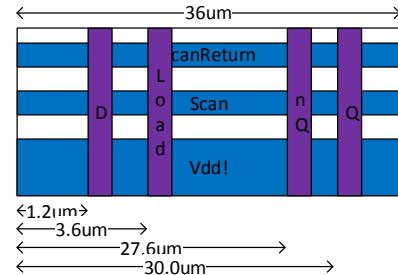
Designer: Constantijn Schepens

Cell Description: A scannable register cell

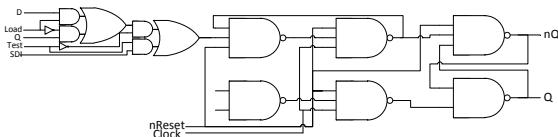
Symbol



Dimensions



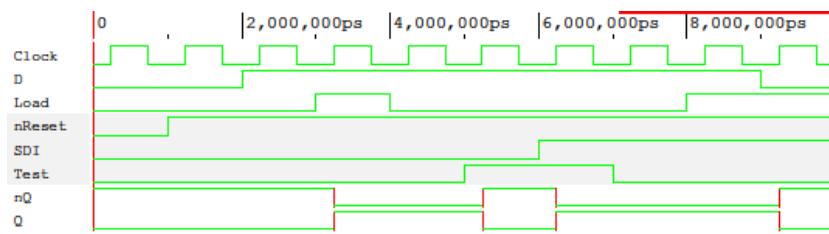
Gate Level Diagram



AC Characteristics

Signal	Average Delay (ps)
clock to q	449.6
clock to nq	459.3
nreset to clear	295.4

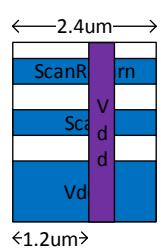
System Verilog Simulation



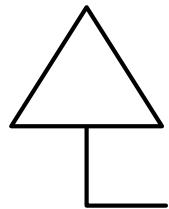
### 1 .17 TIE HIGH

**Designer:** Martin Wearn  
**Cell Description:** A tie to Vdd cell.

#### Dimensions



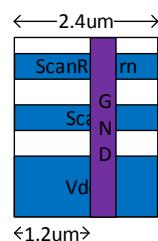
#### Symbol



### 1 .18 TIE LOW

**Designer:** Martin Wearn  
**Cell Description:** A tie to GND cell.

#### Dimensions



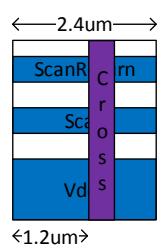
#### Symbol



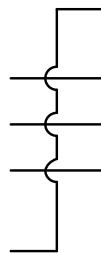
### 1 .19 ROWCROSSER

**Designer:** Martin Wearn  
**Cell Description:** A row crossing cell.

#### Dimensions



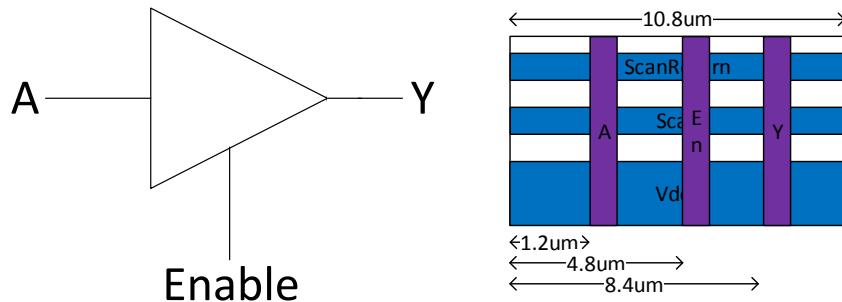
#### Symbol



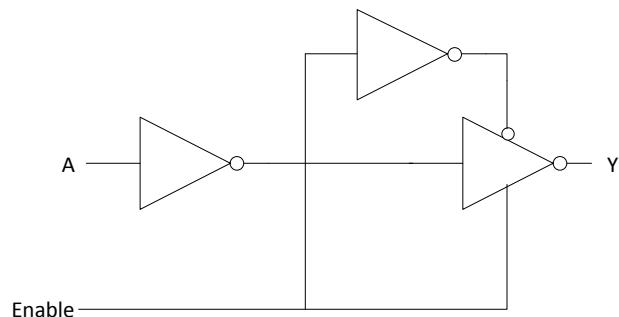
## 1 .20 TRISBUF

**Designer:** Ashley Robinson  
**Cell Description:** A tristate buffer

**Symbol**                    **Dimensions**



**Gate Level Diagram**



**AC Characteristics**

Signal	Average Delay (ps)
a to y	211.8

**System Verilog Simulation**



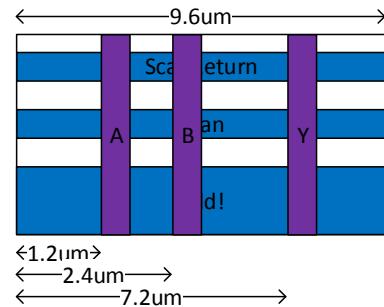
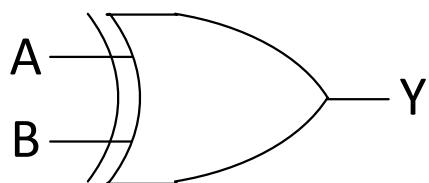
## 1 .21 XOR2

Designer: Ashley Robinson

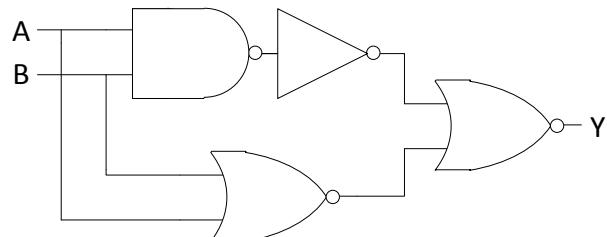
Cell Description: A two input xor gate

Dimensions

Symbol



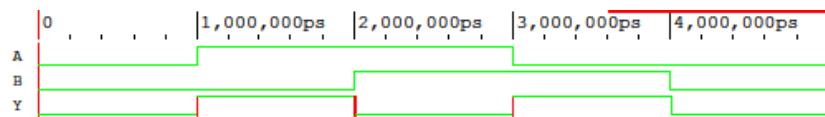
Gate Level Diagram



AC Characteristics

Signal	Average Delay (ps)
a to y	273.4
b to y	193.0

System Verilog Simulation



## A Appendix A

### A.1 Team Management

#### A.1.1 Justification of the Division of Labour

The four major cells were divided between the team as recommended in the specification. It was decided to also attempt the optional cells for teams of four. An extra person in a team of five would be in charge of designing the halfadder and xor2. The halfadder was assigned to the team member designing the fulladder as their expertise was greater for designing adder cells. The xor2 cell was assigned to the team member designing the rdtype as this cell was assumed less time consuming than the two other sets of major cells. The remaining cells were grouped and divided among the teams as shown in Table 1.

Cell Groupings	Reasoning
and2, and2, nand3, nand4	Nands and Ands are similar in design.
buffer, trisbuf	Buffers are similar in design.
inverter, nor2, nor3, or2	Nors and Ors similar in design. Inverter is a simple cell assigned to distribute load.
rowcrosswer, tiehigh, tielow	Low complexity cells assigned to team member tasked with designing both adders.

Table 1: Cell design groupings and reasoning

#### A.1.2 Version Control

The Git revision control system was used throughout the project to facilitate collaborative working. GitHub is a web-based hosting service for git. This was used to share files, allocate work and track bugs.

#### A.1.3 Process automation

The team produced a number of scripts to improve productivity by automating processes such extraction from magic, design simulation and consistency checking. Using Latex allowed the databook compilation to also be automated as separate files for each cell were stored in the hierarchy of folders. This way each designer could add their own files to the data book independently.

## A.2 Division of Labour

	Task	Percentage Effort on Each Task (%)			
		mw20g10	cs7g10	ajr2g10	hl13g10
1	RDTYPE	0	0	100	0
2	SMUX2	0	100	0	0
3	SMUX3	0	100	0	0
4	MUX2	0	100	0	0
5	FULLADDER	100	0	0	0
6	HALFADDER	100	0	0	0
7	XOR2	0	0	100	0
8	INV	0	0	0	100
9	NAND2	0	100	0	0
10	NAND3	0	100	0	0
11	NAND4	0	100	0	0
12	NOR2	0	0	0	100
13	NOR3	0	0	0	100
14	AND2	0	100	0	0
15	OR2	0	0	0	100
16	TRISBUF	0	0	100	0
17	BUFFER	0	0	100	0
18	LEFTBUF	0	0	0	100
19	RIGHTEND	0	0	0	100
20	TIEHIGH	100	0	0	0
21	TIELOW	100	0	0	0
22	ROWCROSSER	100	0	0	0
23	SCANDTYPE	0	0	0	0
24	SCANREG	0	0	0	0
25	Verilog Simulation	0	0	0	0
26	HSpice Characterization	0	0	0	0
27	Final Report (words)	0	0	0	0
28	Final Report (figures)	0	0	0	0
	OVERALL EFFORT	0	0	0	0
	Signature:				

## B Design Detail

All HSpice simulations were done using a loaded cell. All the inputs were driven by an inverter, and all outputs drove two inverters, seen in Figure 20 Measurements were done between 50% of the supply voltage between a change in the input to the cell, to a change in the output.

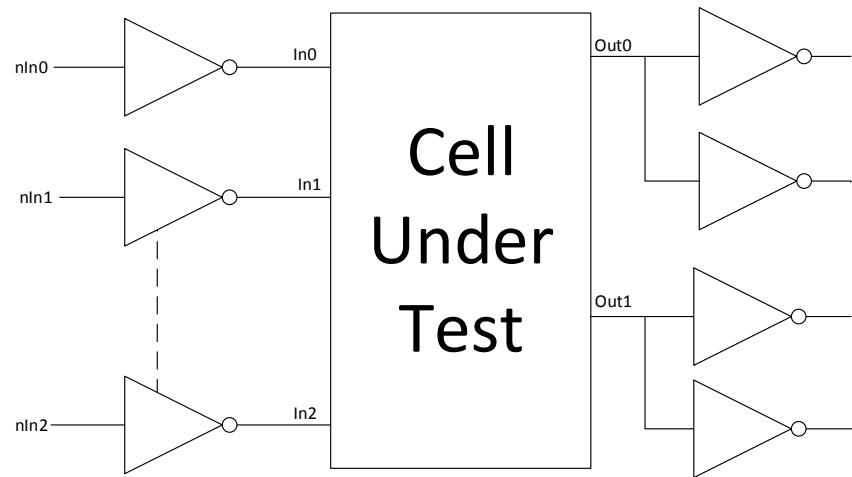


Figure 20: Block Diagram of the loaded simulations

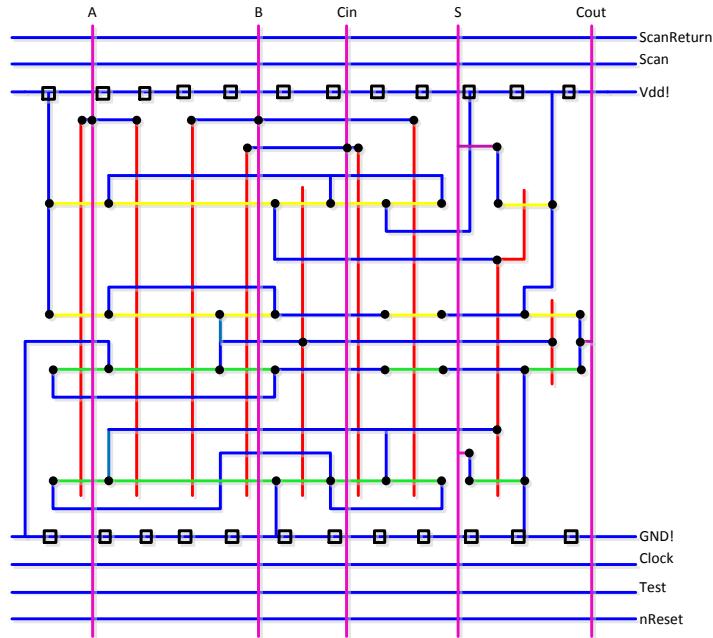
## B.1 FULLADDER

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**Designer:** Martin Wearn

**Cell Description:** Adds two bit values and the previous bitslice carry out, to produce a sum and carry

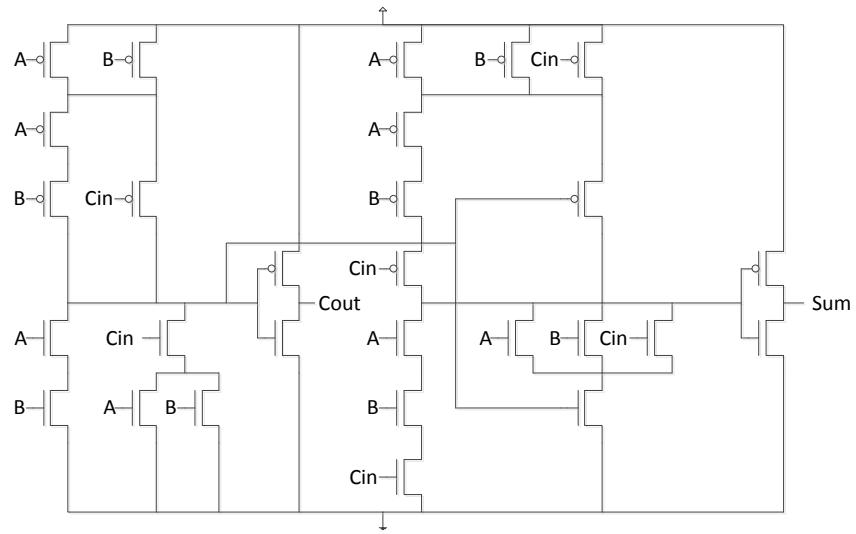
Stick Diagram



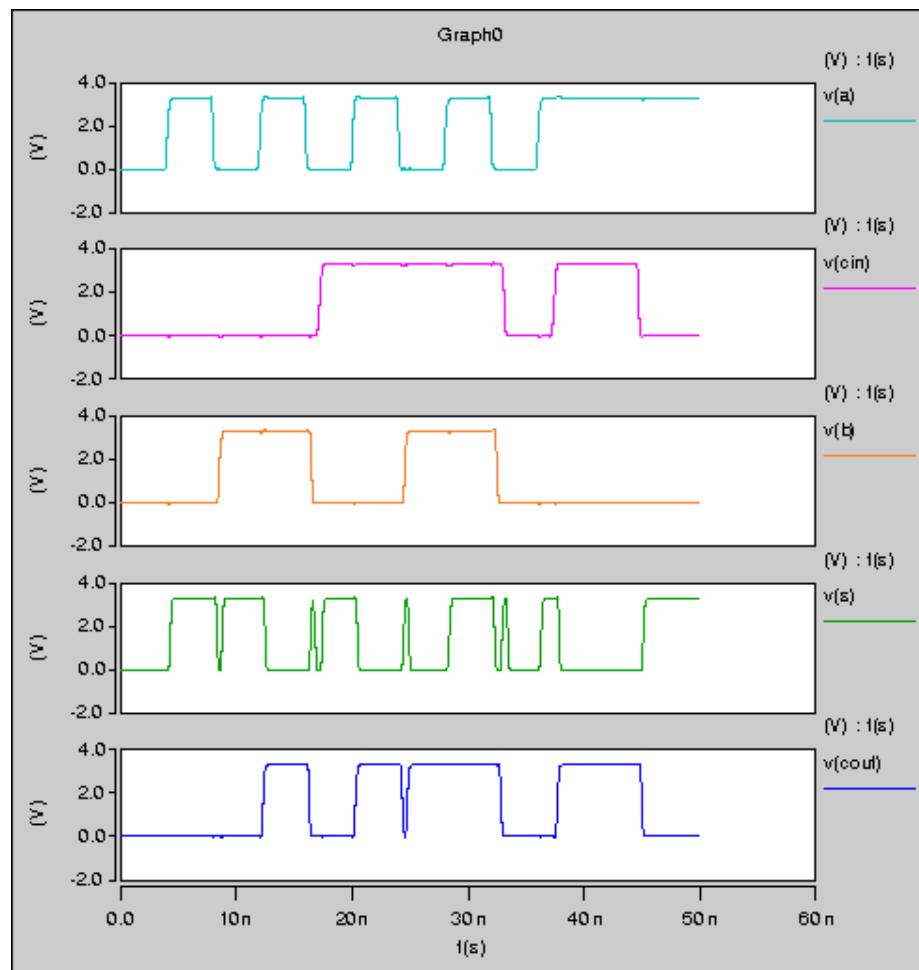
AC Characteristics

Signal	Average Delay (ps)
a to s	294.9
a to cout	285.0
b to s	262.3
b to cout	294.0
cin to s	252.7
cin to cout	274.6

## Transistor Level Circuit Diagram



## HSpice Simulation



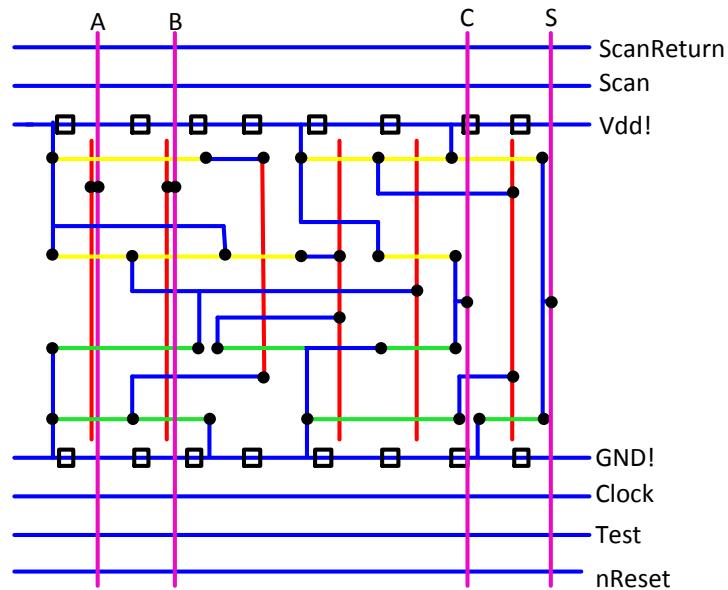
## B.2 HALFADDER

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**Designer:** Martin Wearn

**Cell Description:** Adds two bits to produce a sum and carry

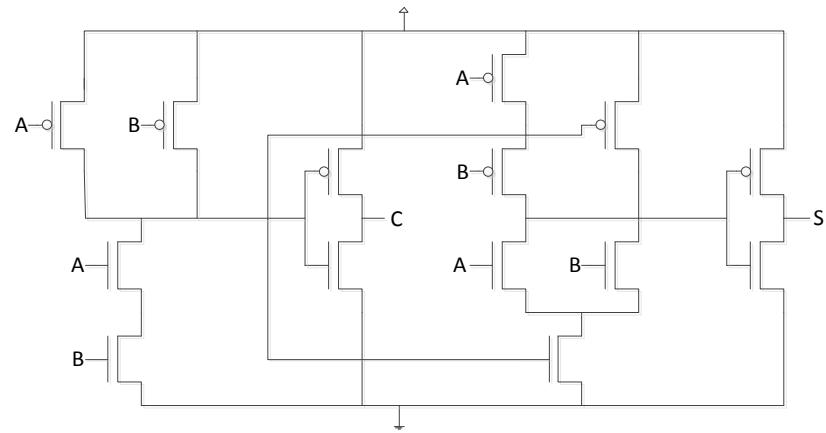
Stick Diagram



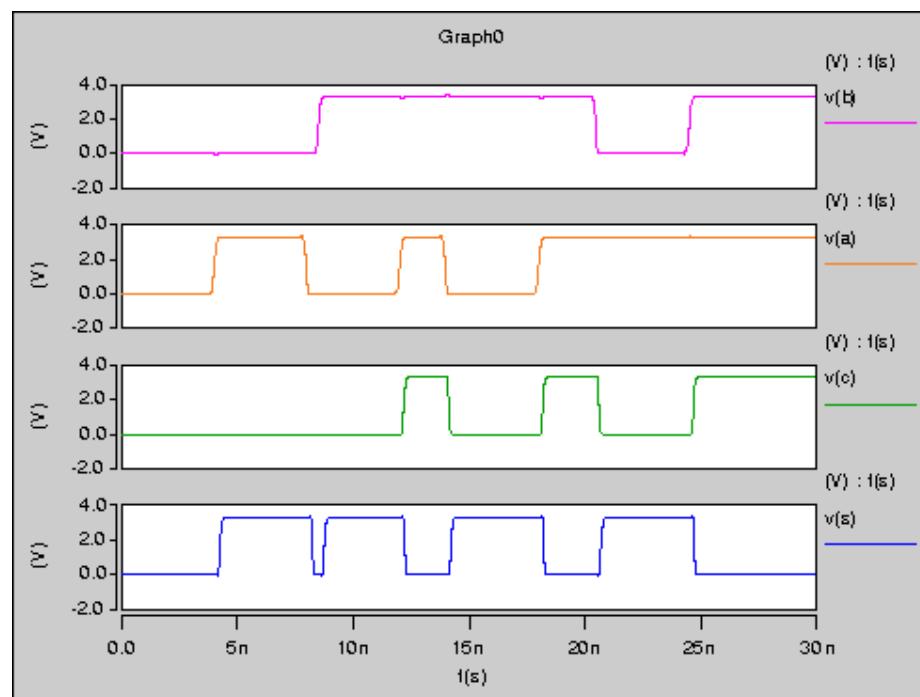
AC Characteristics

Signal	Average Delay (ps)
a to s	251.7
a to c	167.0
b to s	240.9
b to c	166.1

## Transistor Level Circuit Diagram



## HSpice Simulation



### B.3 LEFTBUF

**Designer:** Henry Lovett

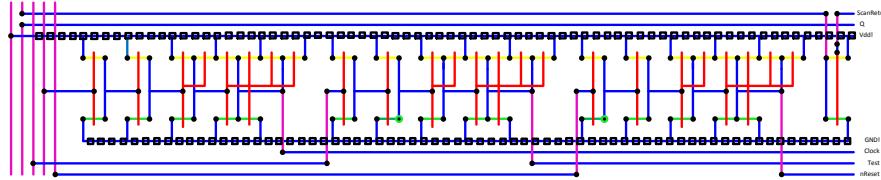
**Cell Description:** A start of row buffer cell.

This cell is to be placed at the beginning of each row of cells. The purpose of this cell is to buffer the *Clock*, *nReset* and *Test* signals to attempt to eliminate skew of the signals. They also cater for the scan path in the circuit by routing and buffering the signal.

This cell contains 3 large buffers, each made up of 4 stages. The gain of the stages are gradually increased, relative to the first. The transistors were folded to reduce the vertical height of the cell. The total, and folded sizes of the transistors are seen in the table below.

Stage	1	2	3	4
Gain	1	2.7	7.3	20
$W_n$ unfolded ( $\mu m$ )	1.0	2.7	7.3	20
$W_p$ unfolded ( $\mu m$ )	2.9	7.85	21.2	58
$W_n$ folded ( $\mu m$ )	$1 \times 1.0$	$1 \times 2.7$	$1 \times 7.3$	$2 \times 10.0$
$W_p$ folded ( $\mu m$ )	$1 \times 2.9$	$1 \times 7.85$	$2 \times 10.6$	$4 \times 14.5$

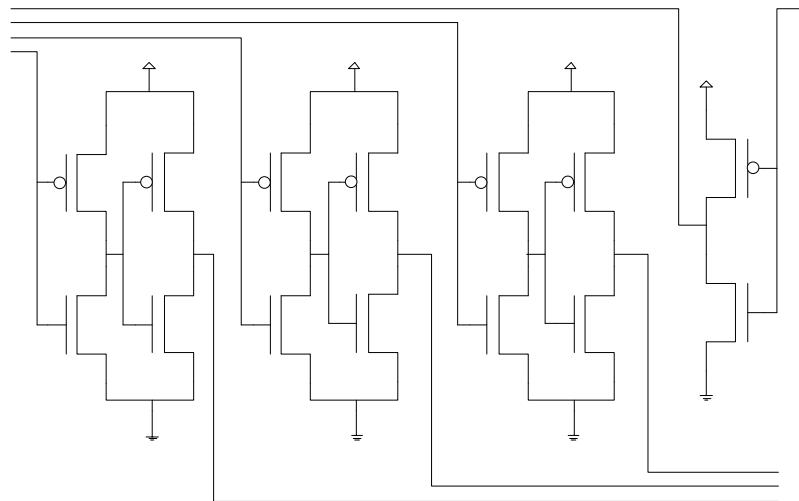
#### Stick Diagram



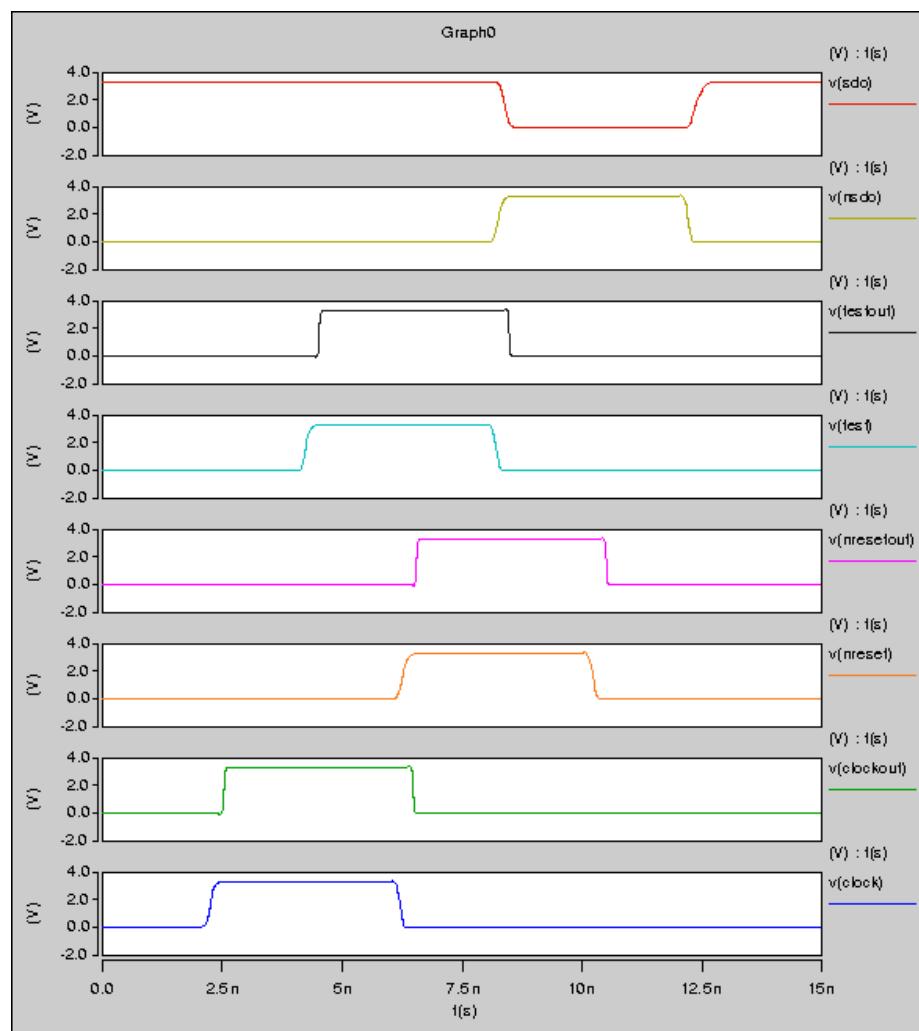
#### AC Characteristics

Signal	Average Delay (ps)
clock to clockout	279.4
test to testout	277.6
nreset to nresetout	281.9
nsdo to sdo	141.2

## Transistor Level Circuit Diagram



## HSpice Simulation



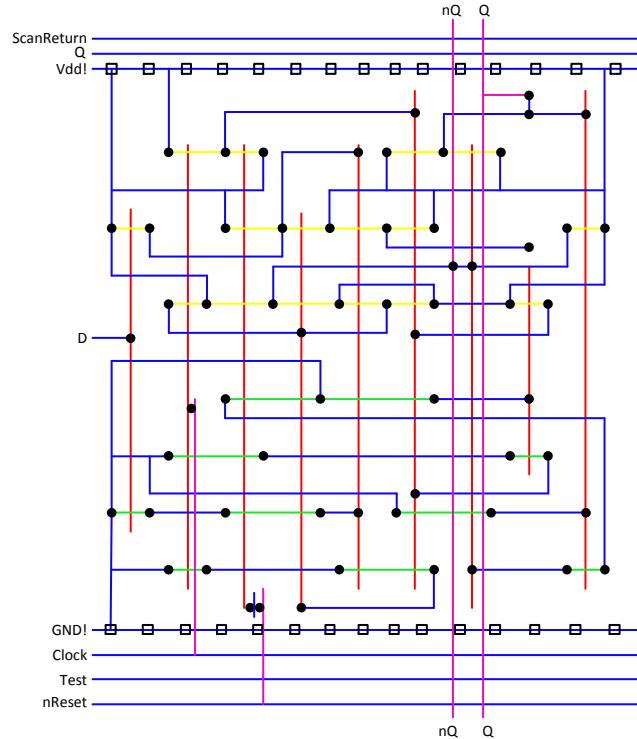
## B.4 RDTYPE

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**Designer:** Ashley Robinson  
**Cell Description:** Raw Dtype

This gate matrix design was optimised by arranging polysilicon columns to allow as many transistors to fit on a row as possible. Three rows of PMOS transistors and four rows of NMOS transistors make up cell. Routing power rails up both sides of the matrix allowed the design to be further compressed. The D input on the middle left was intentionally not surrounded leaving only metal1 to reroute when it came to dimension matching.

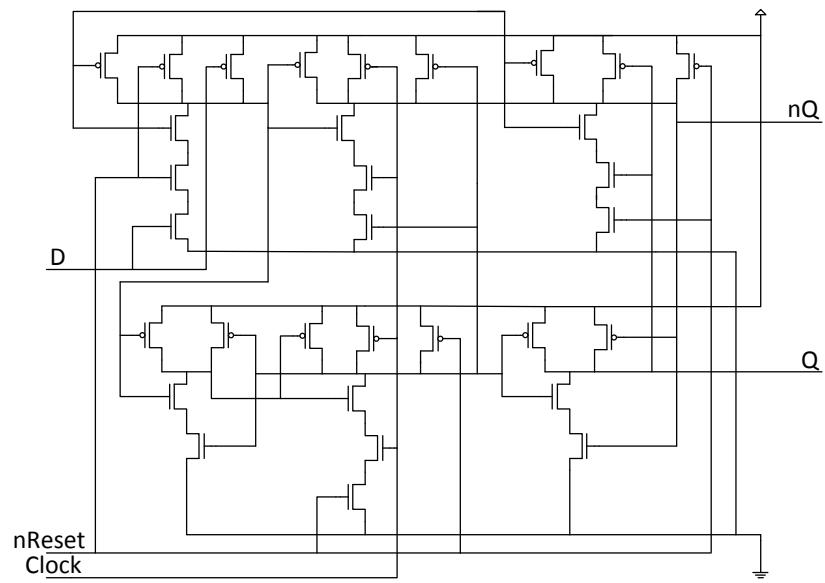
**Stick Diagram**



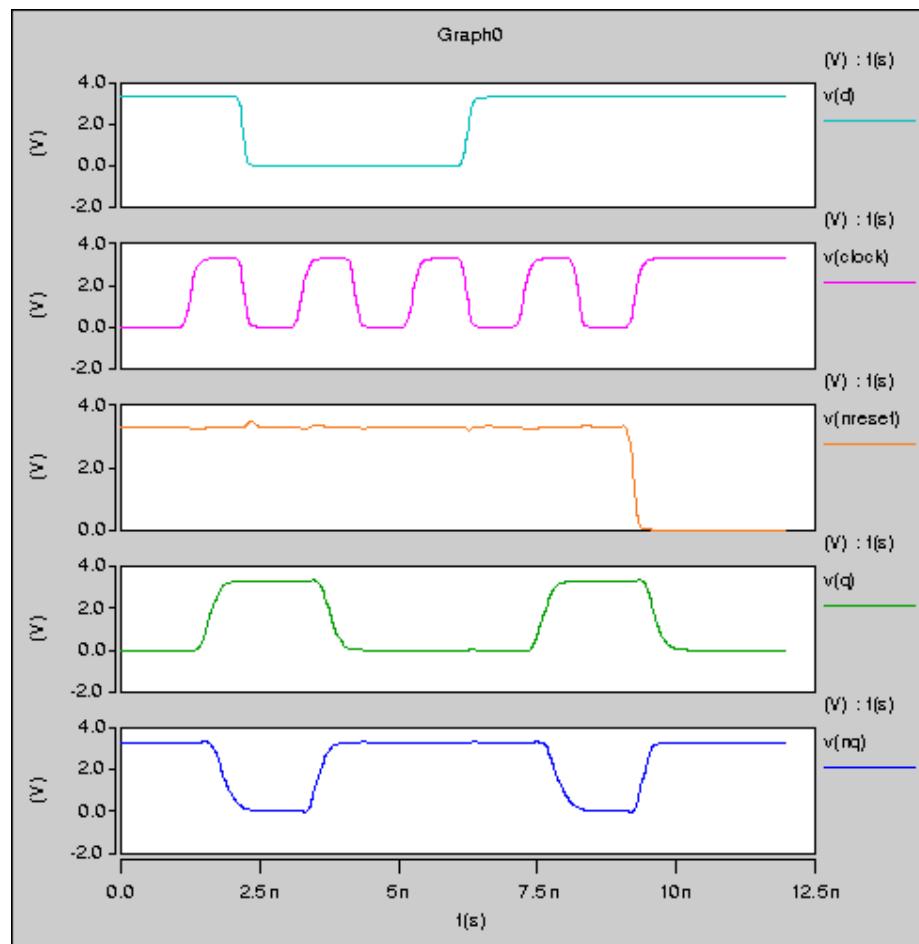
## AC Characteristics

Signal	Average Delay (ps)
Clock to Q	253.2
Clock to nQ	606.6
nReset to Q	340.1
nReset to nQ	69.54

### Transistor Level Circuit Diagram



### HSpice Simulation



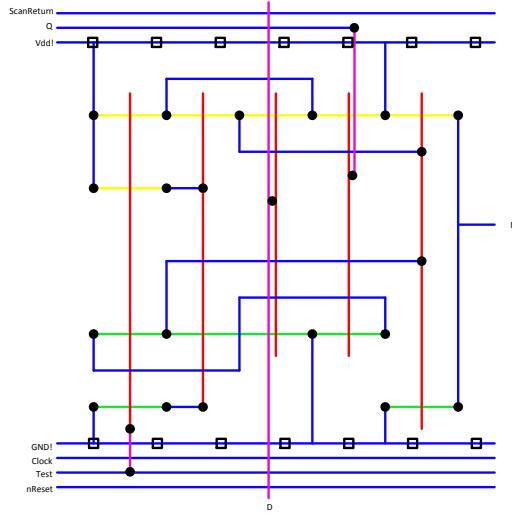
## B.5 SMUX2

**Designer:** Constantijn Schepens

**Cell Description:** A 2 input scannable multiplexer, intended to be connected to a raw D-type to create a scannable D-type.

A single Euler path was used when laying out this cell, before taking into account inverters. The Euler path (T-nT-D-S) was designed such that the output was all the way on the right side such that it could connect directly to the D input of the raw D-type. Once this was done the required internal inverters were added in by creating a gate matrix design.

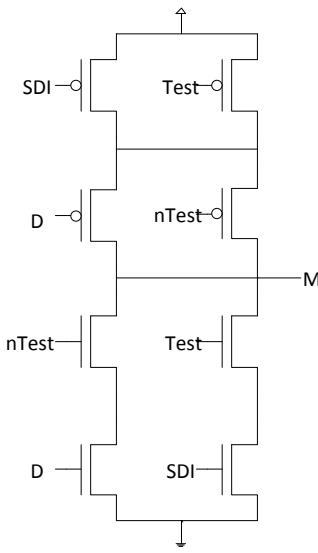
### Stick Diagram



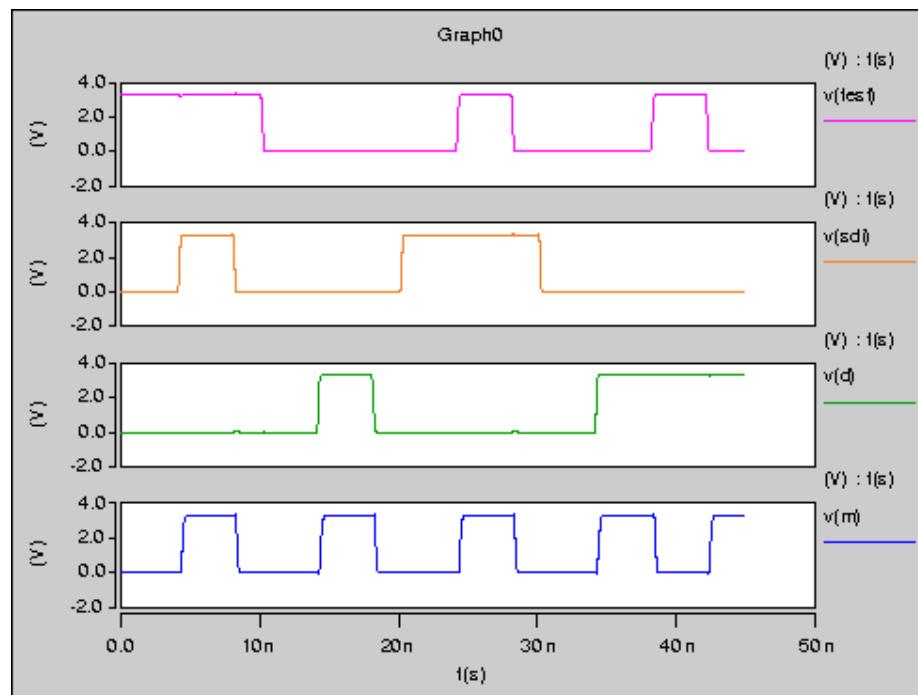
### AC Characteristics

Signal	Average Delay (ps)
sdi to m	212.5
d to m	182.1
test pass sdi	223.5
test pass d	213.8

## Transistor Level Circuit Diagram



## HSpice Simulation



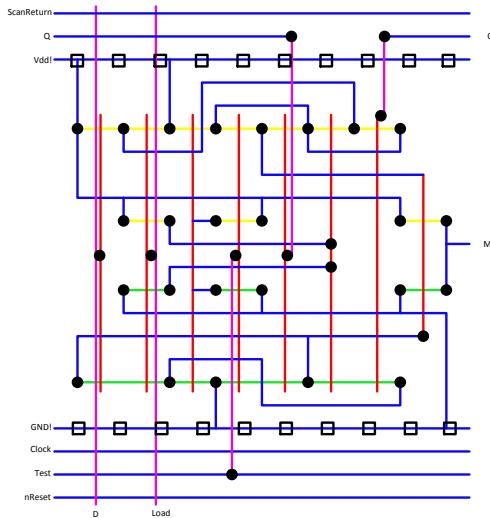
## B.6 SMUX3

**Designer:** Constantijn Schepens

**Cell Description:** A 3 input scannable multiplexer, intended to be connected to a raw D-type to create a scannable register.

A similar approach was taken for the layout of this cell as for the smux2. Initially inverters were excluded and a single Euler path (D-Load-nTest-Test-SDI-nLoad-Q) was found that both kept M and Q as close to the right side as possible (to connect to the raw D-type) and kept the Test/Load nearest to their inverted partners for easy wiring. For the internal inverter placement multiple layouts were trialed to find the most efficient one, that also allowed all the internal wiring to be done with metal 1 exclusively(to reduce the number of vias).

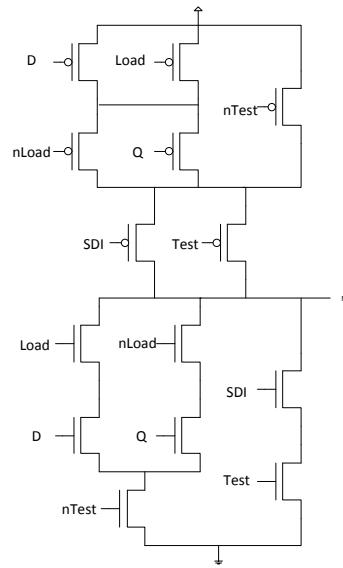
### Stick Diagram



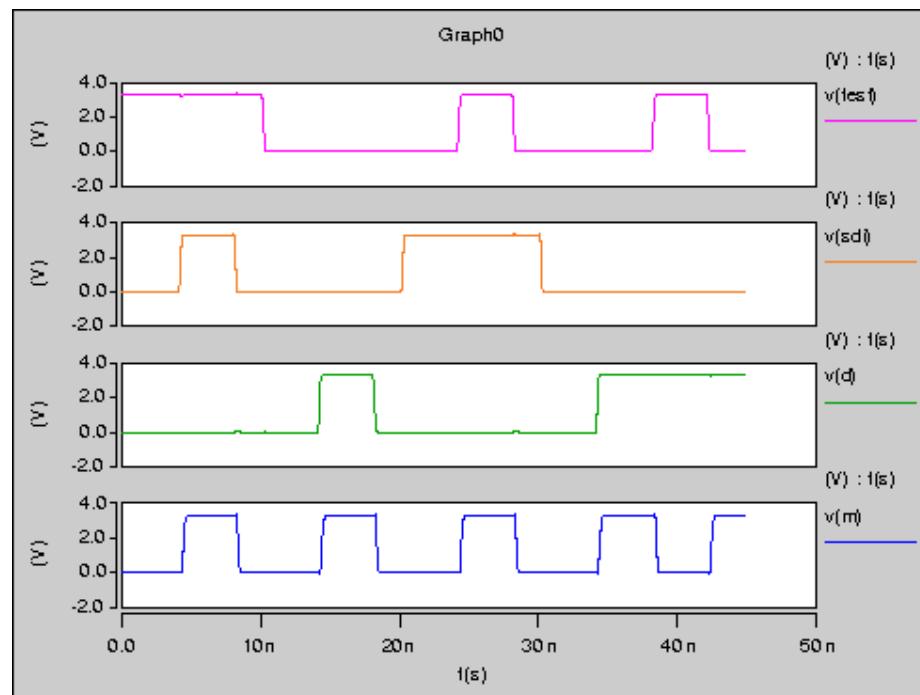
### AC Characteristics

Signal	Average Delay (ps)
sdi to m	227.0
d to m	289.4
q to m	259.1
test pass sdi	242.9
test pass d	287.0
test pass q	278.9
load pass d	296.1
load pass q	303.6

## Transistor Level Circuit Diagram



## HSpice Simulation



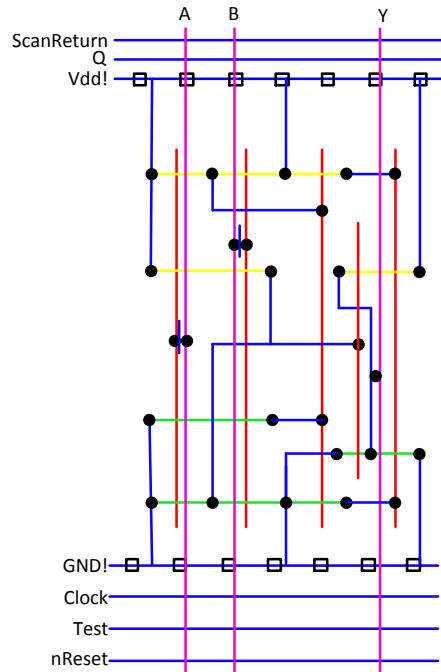
## B.7 XOR2

**Designer:** Ashley Robinson

**Cell Description:** A 2 input XOR gate.

Compound gate routed using an Euler path.

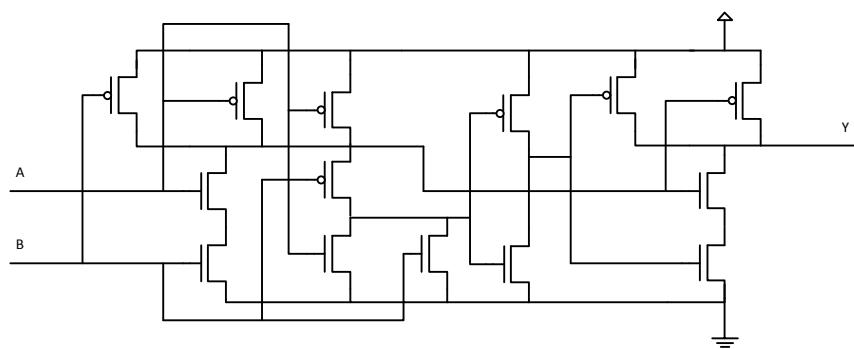
### Stick Diagram



### AC Characteristics

Signal	Average Delay (ps)
a to y	273.4
b to y	193.0

### Transistor Level Circuit Diagram



## HSpice Simulation

