COMP6033 - Individual Research Report

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***Abstract*—The abstract goes here.**

***Index Terms*—IEEEtran, journal, LaTeX, paper, template.**

I. Introduction

THE desire for low power devices has been driven by the mobile age. Companies are competing on battery life of portable devices, such as smartphones and tablets. This drive for low power has resulted in different synthesis techniques. This paper will review and explore some of the techniques used to help reduce the power consumption of a circuit, with particular interest on the synthesis techniques used to do so.

The report begins with a review of different techniques in turn. This includes a brief introduction to the theory and a discussion of synthesis problems and solutions. The report concludes by reviewing all techniques and their relevant advantages and disadvantages.

II. Power Domains

This section reviews literature about Power Domains.

III. Frequency Domains

Lorem Ipsum...

IV. Power Scaling

Lorem Ipsum...

V. Frequency Scaling

Lorem Ipsum...

VI. Clock Gating

A. Theory

The clock in a sequential circuit can contribute 15-45% of the power [1]. Therefore it is a large area of potential power saving. Clock gating is an approach of controlling the clock to individual modules of a design by either stopping or slowing down the clock with respect to a master clock [2]. An approach, seen in [3], involves stopping the clock to unused modules.

This method can be realised using two simple circuits seen in figures 1 and 2. Although figure 1 is functionally complete, in reality, a latch is needed to remove any glitches in the circuit. These are fundamentally different to load-enable registers, where the input is multiplexed between the current value or the input. The load-enable registers are still clocked at the master clock frequency.

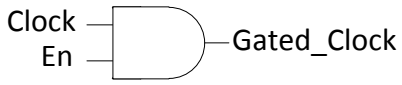

Fig. 1. Clock gating circuit using an AND gate

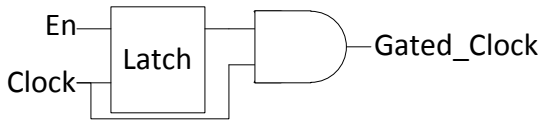

Fig. 2. Clock gating circuit using an AND gate and a latch

B. Synthesis Techniques

A gating function is typically defined by the designer within the RTL design stage. However, a more common approach is to allow the synthesis tool to obtain the gating functions from a gate-level netlist [4], [5].

The general outline for the synthesis is to find the clock gating function for each flip-flop. The flip-flops are then grouped so that they are driven by the same function. The problem of simplifying the gating function is looked at in [6]. Here, an algorithm is suggested where the gating function is shared by existing combinational logic. This was shown to reduce the logic added by introducing clock gating.

However, sometimes the addition of clock gating is not advantageous. The gating function can be large and therefore can cause timing violations, resulting in an unsuitable synthesis. If the gating function is large enough, it can also consume more power than it saves. Both of these issues are addressed in [**?**]. Here, the author proposed solutions to large gating funcitons by reducing the depth of logic by an approximation. The approximation is made such that the resulting logic does not gate the clock more than the original function. It results in the flip-flop being clocked more often, but reduces the logic so that it can be utilised, thereby saving some power.

[**?**] also proposes the use of a clustering algorithm. The algorithm looks at grouping similar gating functions. This can then reduce the overall logic needed to implement the clock gating and maximise the energy saved.

C. Conclusion

Clock gating is a simple principle to implement on a small scale. The underlying theory is to disable a module when it is not in use. This is done by identifying a gating function which disallows clock propagation if the function is asserted.

However, clock gating can produce large gating functions which violate the timing constraints of the circuit, or even consume more power than they save. This results in two problems that need solving - group formation and simplification [6], [7].

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23rd February, 2014

REFERENCES

[1] M. Pedram, "Power minimization in ic design: principles and applications," *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, vol. 1, no. 1, pp. 3–56, 1996.

[2] Q. Wu, M. Pedram, and X. Wu, "Clock-gating and its application to low power design of sequential circuits," *Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on*, vol. 47, no. 3, pp. 415–420, Mar 2000.

[3] G. E. Téllez, A. Farrahi, and M. Sarrafzadeh, "Activity-driven clock design for low power circuits," in *Proceedings of the 1995 IEEE/ACM international conference on Computer-aided design*. IEEE Computer Society, 1995, pp. 62–65.

[4] L. Benini, G. De Micheli, E. Macii, M. Poncino, and R. Scarsi, "Symbolic synthesis of clock-gating logic for power optimization of synchronous controllers," *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, vol. 4, no. 4, pp. 351–375, 1999.

[5] A. P. Hurst, "Automatic synthesis of clock gating logic with controlled netlist perturbation," in *Proceedings of the 45th annual Design Automation Conference*. ACM, 2008, pp. 654–657.

[6] I. Han and Y. Shin, "Synthesis of clock gating logic through factored form matching," in *IC Design Technology (ICICDT), 2012 IEEE International Conference on*, May 2012, pp. 1–4.

[7] S. Paik, I. Han, S. Kim, and Y. Shin, "Clock gating synthesis of pulsed-latch circuits," *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, vol. 31, no. 7, pp. 1019–1030, July 2012.

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