COMP6033 - Individual Research Report

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***Abstract*—The abstract goes here.**

***Index Terms*—IEEEtran, journal, LATEX, paper, template.**

I. Introduction

THE desire for low power devices has been driven by the mobile age. Companies are competing on battery life of portable devices, such as smartphones and tablets. This drive for low power has resulted in different synthesis techniques. This paper will review and explore some of the techniques used to help reduce the power consumption of a circuit, with particular interest on the synthesis techniques used to do so.

The report begins with a review of different techniques in turn. This includes a brief introduction to the theory and a discussion of synthesis problems and solutions. The report concludes by reviewing all techniques and their relevant advantages and disadvantages.

II. Power Techniques

A. Power Gating

1) Theory: Power gating, in principle, is where the power to a module is switched off when not in use. By doing this, the module does not consume any power. It can be achieved by using either a header or a footer switch to disable either the supply connection or the ground connection. Figure 1 shows the realisation of the power gating circuits.

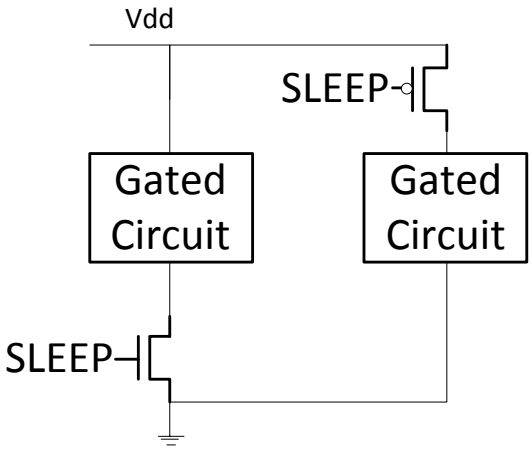

Fig. 1. Circuit diagrams showing the use of footer switches (left) or header switches (right).

Although the theory of operation is simple, the technique poses many issues in the implementation. Firstly, as the module is floating, the outputs are undefined. This can cause the gates in another module to short circuit - at an input voltage of $V_{dd}/2$, both the NMOS and PMOS transistors will be on, resulting in a direct line from supply to ground. The solution to this is is to add logic gates with a 'clamp' signal. This could be either an AND gate, of which the clamp signal is active low, or an OR gate with an active high clamp. This added logic is needed per signal output of the power gated module.

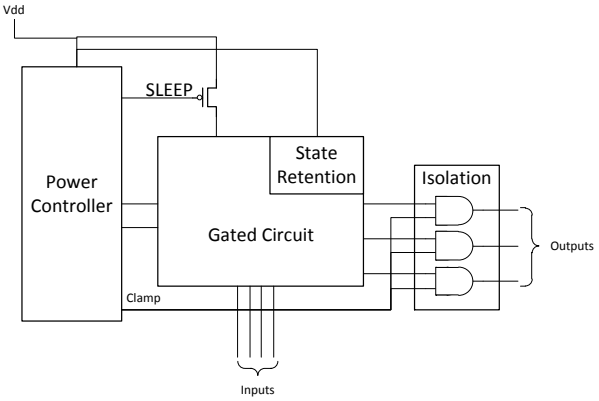

Fig. 2. The relaisation of a power gated module. State retention, isolation and a power manager are all needed

The second issue that power gating raises is when the gated module contains sequential logic. By removing the power to the sequential logic, the state is lost. This can then cause issues as state retention may be necessary, as well as low power. The solution is to use a state retention register. There is a timing overhead involved to store the register before putting the device to sleep, disabling the majority of the circuit. State retention registers also require an individual power supply, meaning all power gated modules require two supplies; one which is gated and one constant supply. A full realisation of a power gated circuit is shown in figure 2.

B. Synthesis Techniques

C. Power Scaling

III. Frequency Domains

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IV. Frequency Scaling

Lorem Ipsum...

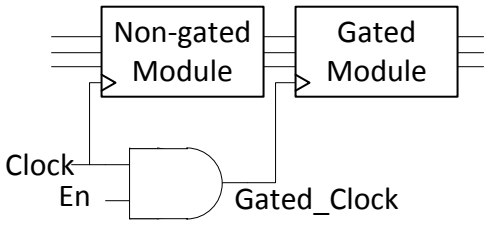

Fig. 3. Clock gating circuit using an AND gate

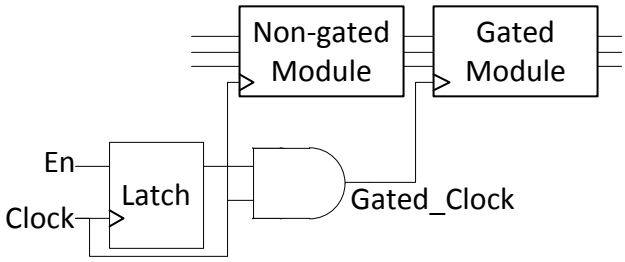

Fig. 4. Clock gating circuit using an AND gate and a latch

V. Clock Gating

A. Theory

The clock in a sequential circuit can contribute 15-45% of the power [1]. Therefore it is a large area of potential power saving. Clock gating is an approach of controlling the clock to individual modules of a design by either stopping or slowing down the clock with respect to a master clock [2]. An approach, seen in [3], involves stopping the clock to unused modules.

This method can be realised using two simple circuits seen in figures 3 and 4. Although figure 3 is functionally complete, in reality, a latch is needed to remove any glitches in the circuit. These are fundamentally different to load-enable registers, where the input is multiplexed between the current value or the input. The load-enable registers are still clocked at the master clock frequency.

B. Synthesis Techniques

A gating function is typically defined by the designer within the RTL design stage. However, a more common approach is to allow the synthesis tool to obtain the gating functions from a gate-level netlist [4], [5].

The general outline for the synthesis is to find the clock gating function for each flip-flop. The flip-flops are then grouped so that they are driven by the same function. The problem of simplifying the gating function is looked at in [6]. Here, an algorithm is suggested where the gating function is shared by existing combinational logic. This was shown to reduce the logic added by introducing clock gating.

However, sometimes the addition of clock gating is not advantageous. The gating function can be large and therefore can cause timing violations, resulting in an unsuitable synthesis. If the gating function is large enough, it can also consume more power than it saves. Both of these issues are addressed in [7]. Here, the author proposed solutions to large gating funcitons by reducing the depth of logic by an approximation. The approximation is made such that the resulting logic does not gate the clock more than the original function. It results in the flip-flop being clocked more often, but reduces the logic so that it can be utilised, thereby saving some power.

[7] also proposes the use of a clustering algorithm. The algorithm looks at grouping similar gating functions. This can then reduce the overall logic needed to implement the clock gating and maximise the energy saved.

C. Conclusion

Clock gating is a simple principle to implement on a small scale. The underlying theory is to disable a module when it is not in use. This is done by identifying a gating function which disallows clock propagation if the function is asserted.

However, clock gating can produce large gating functions which violate the timing constraints of the circuit, or even consume more power than they save. This results in two problems that need solving - group formation and simplification [6], [8].

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