COMP6033 - Individual Research Report

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***Abstract*—The abstract goes here.**

***Index Terms*—IEEEtran, journal, LaTeX, paper, template.**

I. Introduction

THE desire for low power devices has been driven by the mobile age. Companies are competing on battery life of portable devices, such as smartphones and tablets. This drive for low power has resulted in different synthesis techniques. This paper will review and explore some of the techniques used

II. Power Domains

This section reviews literature about Power Domains.

III. Frequency Domains

Lorem Ipsum...

IV. Power Scaling

Lorem Ipsum...

V. Frequency Scaling

Lorem Ipsum...

VI. Clock Gating

A. Theory

The clock in a sequential circuit can contribute 15-45% of the power [1]. Therefore it is a large area of potential power saving. Clock gating is an approach of controlling the clock to individual modules of a design by either stopping or slowing down the clock with respect to a master clock [2]. An approach, seen in [3], involves stopping the clock to unused modules.

This method can be realised using two simple circuits seen in figures 1 and 2. Although figure 1 is functionally complete, in reality, a latch is needed to remove any glitches in the circuit. These are fundamentally different to load-enable registers, where the input is multiplexed between the current value or the input. The load-enable registers are still clocked at the master clock frequency.

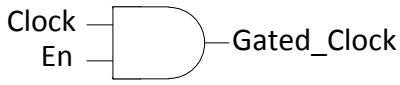

Fig. 1. Clock gating circuit using an AND gate

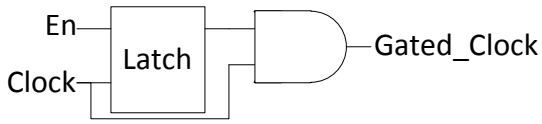

Fig. 2. Clock gating circuit using an AND gate and a latch

B. Synthesis Techniques

A gating function is typically defined by the designer within the RTL design stage. However, a more common approach is to allow the synthesis tool to obtain the gating functions from a gate-level netlist [4], [5].

The general outline for the synthesis is to find the clock gating function for each flip-flop. The flip-flops are then grouped so that they are driven by the same function. The problem of simplifying the gating function is looked at in [6]. Here, an algorithm is suggested where the gating function is shared by existing combinational logic. This was shown to reduce the logic added by introducing clock gating.

C. Advantages

Good things about using this.

D. Disadvantages

Bad things about using this.

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References

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