# Hierarchical Power Distribution With Power Tree in Dozens of Power Domains for 90-nm Low-Power Multi-CPU SoCs

Yusuke Kanno, *Member, IEEE*, Hiroyuki Mizuno, *Member, IEEE*, Yoshihiko Yasu, Kenji Hirose, Yasuhisa Shimazaki, Tadashi Hoshi, Yujiro Miyairi, Toshifumi Ishii, Tetsuya Yamada, Takahiro Irita, Toshihiro Hattori, *Member, IEEE*, Kazumasa Yanagisawa, and Naohiko Irie

***Abstract*—Hierarchical power distribution with a power tree has been developed. The key features are a power-tree structure with three power-tree management rules and a distributed common power domain implementation. The hierarchical power distribution supports a fine-grained power gating with dozens of power domains, which is analogous to a fine-grained clock gating. Leakage currents of a 1 000 000-gate power domain were effectively reduced to 1/4000 in multi-CPU SoCs with minimal area overhead.**

***Index Terms*—Common power domain, fine-grained power gating, hierarchical power distribution, leakage reduction, low power, SoC.**

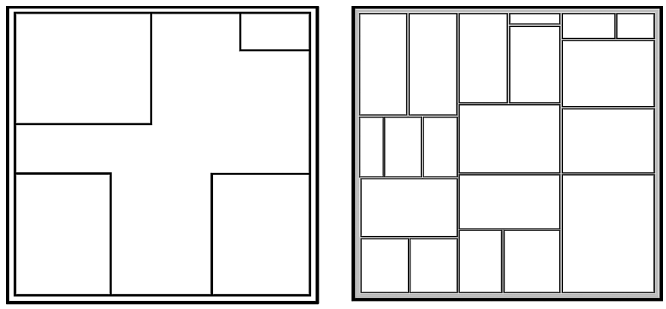


Fig. 1. Power domain partitioning of SoC. (a) Conventional power domain partitioning. (b) Power domain partitioning for 90-nm scale and smaller scale.

## I. Introduction

SCALING of fabrication process rules enables to increase the number of MOSFETs integrated on a single LSI. Thus, a system-on-a-chip (SoC), which integrates various functions for multimedia execution within a single chip, is commonly available. One-chip integration is an effective strategy, especially for mobile applications such as cellular phones, because this is a good solution to satisfy the growing demand for achieving high performance within a limited footprint.

However, devices using advanced processes bring about large leakage current due to increasing fabrication process fluctuations [1]. The leakage currents of LSIs have been increasing exponentially because of the synergistic effect of an increasing number of integrated MOSFETS. This increasing leakage presents the most crucial design challenge, especially for mobile applications, because these kinds of SoC must meet stringent leakage requirements due to a limited battery capability.

To reduce leakages, various schemes, primarily focusing on application of reverse-body bias [2]–[5], have been developed and used in products. However, these schemes mainly dealt with the subthreshold leakage of the MOSFET, thus the reduction of leakages for drain to bulk components, due to gate-induced drain leakage (GIDL) or direct tunneling from drain to bulk in transistors, is insufficient. To plug these leakages, the self-reverse biasing scheme for DRAMs [6], [7], the MT-CMOS technique [8], [9], and the power gating scheme [10], [11] have been developed. This scheme promises to reduce subthreshold leakage, GIDLs, and gate tunnel leakages. Recently, a power-gating scheme with several power-domain partitions has been developed and commonly used in low-power LSIs such as SoCs for 3G cellular phone processors [12], [13].

However, the number of CPUs, DSPs, and hardware IPs integrated on a single SoC has been steadily increasing. Thus, the conventional power gating becomes insufficient to reduce the leakage current of the entire chip in such SoCs. In an SoC, such as a cellular phone processor, integrating the maximum number of IPs on a chip is important, and the minimum number of IPs is used selectively for achieving desired functions. This implies that all functions integrated on the SoC need not be used at the same time. Based on this situation, an effective method is one in which only necessary IPs are powered on and idle IPs are powered off. Therefore, a fine-grained power-gating scheme using dozens of power domains is necessary to achieve a low-power LSI for mobile SoCs.

To achieve fine-grained power gating, we have developed a hierarchical power distribution (HPD) with a power tree, which is analogous to the structure of clock tree [14]. The reason we adopted a method similar to a clock-gating technique is that this approach is suitable for thinking logically about a fine-grained

Manuscript received April 14, 2006; revised July 31, 2006.

Y. Kanno, T. Yamada, and N. Irie are with the Central Research Laboratory, Hitachi, Ltd., Kokubunji, Tokyo 185-8601, Japan.

H. Mizuno is with the Strategy Center, R&D Group, Hitachi, Ltd., Chiyoda-ku, Tokyo 100-8220, Japan.

Y. Yasu, K. Hirose, Y. Shimazaki, T. Hoshi, Y. Miyairi, T. Irita, T. Hattori, and K. Yanagisawa are with the Renesas Technology Corp., Kodaira, Tokyo 185-8588, Japan.

T. Ishii is with the Strategy Center, R&D Group, Hitachi, Ltd., Chiyoda-ku, Tokyo 100-8220, Japan. He is also with the Renesas Technology Corp., Kodaira, Tokyo 185-8588, Japan.

Digital Object Identifier 10.1109/JSSC.2006.885057

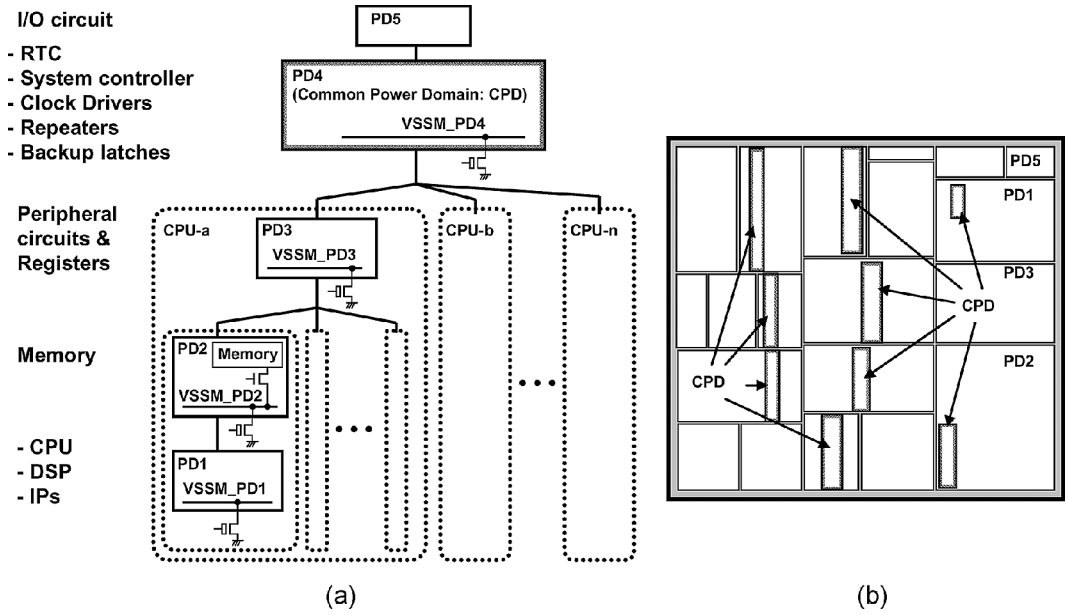


Fig. 2. Hierarchical power distribution: key features are (a) power-tree structure and (b) distributed common power domain (CPD) implementation.

power gating. The clock-gating scheme is very common for reducing switching power. Furthermore, this scheme has become more complex, advanced, and finer-grained in the pursuit of further reduction of the switching power [15], [16]. These reports demonstrate that fine-grained control is very useful for reducing power consumption. This hierarchical power distribution technique was applied to a 90-nm one-chip 3G cellular phone processor [17] and was demonstrated using 20 power domain integrations with successful leakage reduction in accordance with several operational modes.

In Section II, we discuss the concept of the hierarchical power distribution scheme and two key features: three power-tree management rules and the distributed common power domain (CPD) implementation. In Section III, we describe layout techniques for implementing the hierarchical power distribution: power switch and power line implementation, the CPD, and SRAM implementation. In Section IV, we estimate leakage reduction effect in accordance with power on and off combination. In Section V, we describe the modification of the power switch controller for applying dozens of power domain implementations. In Section VI, we describe an example of an integrated SoC. We conclude in Section VII. This paper focuses entirely on a basic technique for implementing dozens of power domain in a single LSI; the application of this work was reported in [17].

## II. Hierarchical Power Distribution

In this section, we discuss the concept of the proposed fine-grained power gating compared with the conventional power domain partitioning. A typical conventional partitioning is shown in Fig. 1(a). This partitioning has one or two constantly powered domains and three or four power domains that can be powered on and off by dedicated on-die power switches depending on the operational mode [12], [13]. The former constantly powered domains include a minimum circuit for maintaining LSI conditions such as I/O circuitry and system controllers. The latter domains include main functional circuits such as CPU, DSP, and IPs. Conventional partitioning needs one large power domain as a hub for the global signal transmission circuit, so several power domains are embedded in this domain.

However, this conventional partitioning makes it difficult to increase the number of power domains to more than a dozen. In the 90-nm generation, several CPUs, DSPs, and IPs are integrated on a single LSI. The required floor plan having dozens of power domains is shown in Fig. 1(b), which is applying the fine-grained power gating. Thus, implementing a large domain as a hub is difficult.

To implement the dozens of power domains for achieving fine-grained power gating in a LSI, there are three issues to be resolved. The first is design complexity. When the number of partitioned power domains increases, the design of isolation-cell insertion and its verification become more difficult. The isolation cell, which we call $\mu$I/O [11], is commonly used to prevent an invalid signal transmission from the power-off domain to the power-on domain. In addition, when the number of the $\mu$I/O is increased, the integration of the $\mu$I/O becomes critical for the physical design, so the reduction of the $\mu$I/O is necessary for designing with limited cost. The second issue is the long global signal transmission wiring. Even in an SoC, global signal transmissions such as those of a clock tree and signal transmissions between two distant power domains is necessary. For the global signal transmission, a buffer circuit, such as a clock buffer and repeater, is a key factor to avoid performance degradation. However, as shown in Fig. 1(b), the floor plan of an LSI having dozens of power domains does not allow implementing a large power domain as a hub in the LSI. Therefore, the establishment of a power supply scheme for clock buffers and repeaters is a challenge for realizing dozens of power domain implementation. Finally, there is a long recovery time from the power-off state to the power-on state. When a power domain enters the

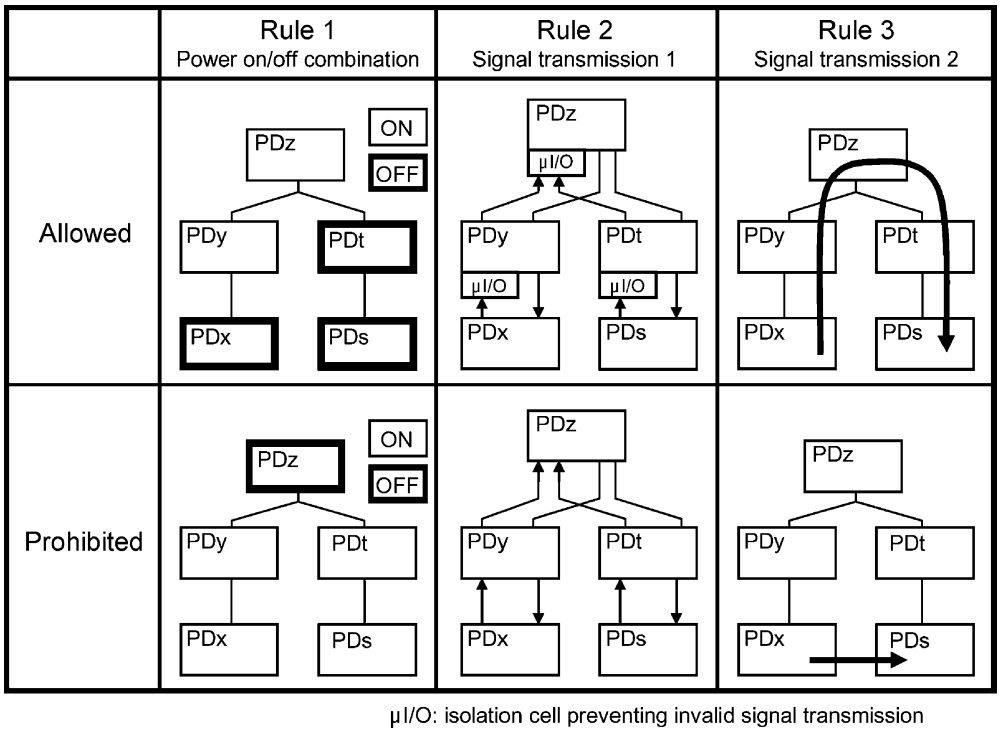


Fig. 3. Power-tree management rules.

power-off state, the information of the flip-flops (FFs) in the power domain is disappeared. Since it takes a long time to reset the key information to the FFs, this long recovery time brings about less opportunity for a power domain to enter a power-off state. Therefore, a fast recovery time from the power-off state is indispensable to maximize the effect of dozens of power domain implementations.

To address these issues, we propose a hierarchical power-distribution (HPD) scheme, shown in Fig. 2. The HPD scheme has two key features: a power-tree structure with three power-tree management rules and distributed CPD implementation. The power-tree structure with three power-tree management rules addresses the first issue, i.e., the design complexity, and the distributed CPD implementation addresses the second and third issues, i.e., global signal transmission and fast recovery time from power-off state. Also, the new power switch controller helps to address the third issue, fast recovery time. The HPD represents the logical power-on-and-off relationship between each power domain. Additionally, the HPD scheme helps us easily understand the power domain relationship, because it is analogous to the well-known clock-gating scheme that uses a "clock tree" to decrease switching power.

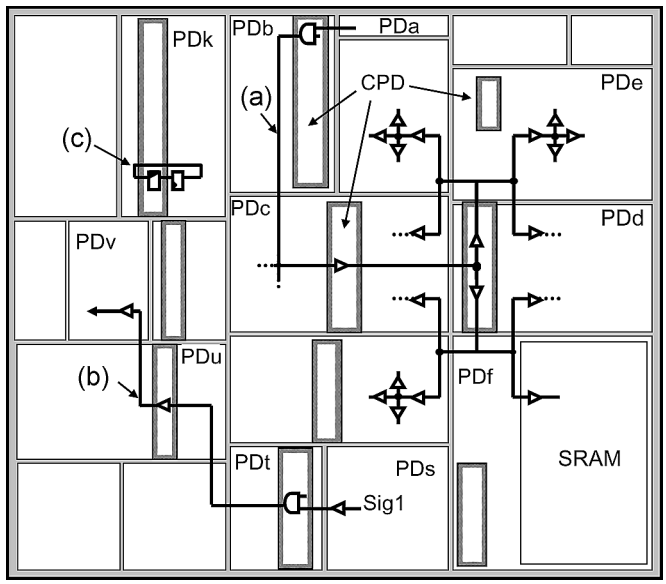


Fig. 4. CPD implementation: (a) clock buffer implementation, (b) repeater implementation, and (c) backup latch implementation.

### A. Power Tree Structure With Three Power Tree Management Rules

Fig. 2(a) shows one example of the logical relationship between each power domain, which we call power-tree structure. The power tree has several branches associated with CPUs implemented on an SoC. All power domains except for that of the top hierarchy have their own dedicated ground power lines. Each dedicated ground power line is connected to real ground via power switches. The power-off control of the power switch for each power domain is executed hierarchically. That is, the upper hierarchy can only be powered off when all of the lower hierarchy related to the same branch is powered off, which is analogous to the clock gating.

Although the power-tree structure brought about restricted power gating combinations in the hierarchy, we can easily implement dozens of power domains in a SoC. If there are no restrictions, the total number of signal transmission cases is represented as the permutation of selecting a sender and a receiver from the total number of power domains. For example,

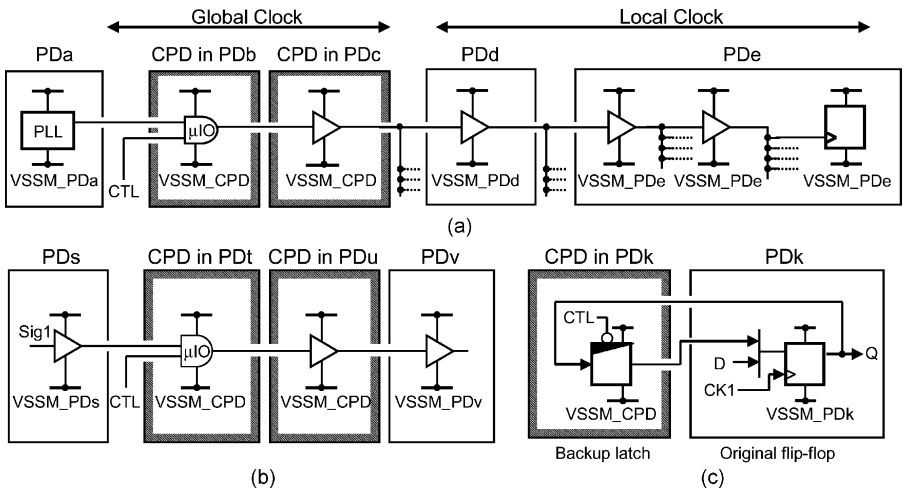


Fig. 5. Precise illustration for implementation of clock buffers, repeaters and backup latches. (a) Clock buffer implementation; (b) repeater implementation; (c) backup latch implementation.

in the case of having 20 power domains, the total permutation is ${}_{20}P_2 = 20 \times 19 = 380$. This permutation is nearly proportional to the squared number of power domains. Thus, reducing the number of power-on-and-off combinations to consider is important.

In order to reduce the number of power-on-and-off combinations to consider effectively, we defined three power-tree management rules. The rules are as follows (see Fig. 3).

1) The power on-and-off combination rule.
   This is the definition rule of the power-tree structure. Domains in lower levels of the hierarchy, e.g., PDx, can be in the powered-on state only if domains in higher levels of the hierarchy, e.g., PDy, are on. In other words, domain PDy is never powered off when domain PDx is powered on. In addition, domain PDz is only powered off when all lower level domains, e.g., PDx, PDy, PDs, PDt, are powered off.
2) The $\mu$I/O insertion rule.
   The $\mu$I/O is placed in a higher level of the hierarchy when a signal is transmitted from a lower level to a higher level in the hierarchy. $\mu$I/O is not needed when a signal is transmitted from a higher level to a lower level in the hierarchy for reducing the $\mu$I/Os. For example, the isolation cell is placed in a higher level of the hierarchy, e.g., PDy, when a signal is transmitted from a lower level, e.g., PDx, to a higher level, e.g., PDy, in the hierarchy. By using this rule, the total number of the uI/O can be reduced to 1/2 when we assume that the number of wires from one power domain to the other power domain and vice versa is the same.
3) The signal transmission rule.
   The signal transmission between two distant lower-level power domains must be routed in common upper-level power domains. For example, the signal transmission from PDy to PDs is routed via power domain PDz in the common upper hierarchy of both PDx and PDs.

### *B. Distributed CPD Implementations*

The other key feature of the HPD scheme is a distributed CPD implementation. The physical layout example is shown in the Fig. 2(b). This CPD is defined as a power domain of the second highest hierarchy as shown in Fig. 2(a), and this plays an important role to implement global signals, such as clock buffers and repeaters, and backup latches. By using the CPD, we can implement many small power domains in a single SoC while maintaining global signals and backup latches. As shown in Fig. 4, the CPD is distributed over the entire SoC for feeding the power supply for global signal transmitting circuits and backup latches, even though the surrounding power domains are in the power-off state.

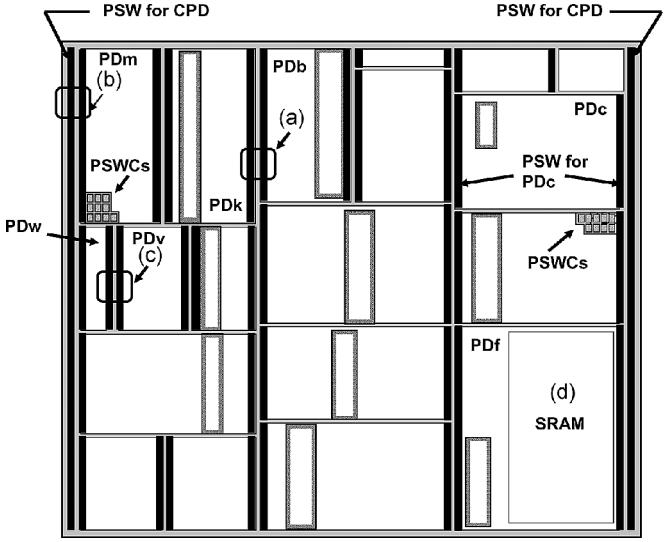


Fig. 6. Power switch implementation: (a) power switches for PDb and PDk, (b) power switches for PDm and CPD, (c) power switches for PDv and PDw, and (d) SRAM implementation.

As an example of a long global signal transmission, clock distribution must be considered. To avoid increasing the clock skew, it is necessary to implement buffers, i.e., clock buffers, in appropriate positions indicated by (a) in Fig. 4. Fig. 5(a) shows the precise implementation of the clock buffers. Using a CPD, we can implement the global clock buffers in appropriate positions independent from partitioning of the power domains. To minimize leakages in the standby mode, minimal circuits must

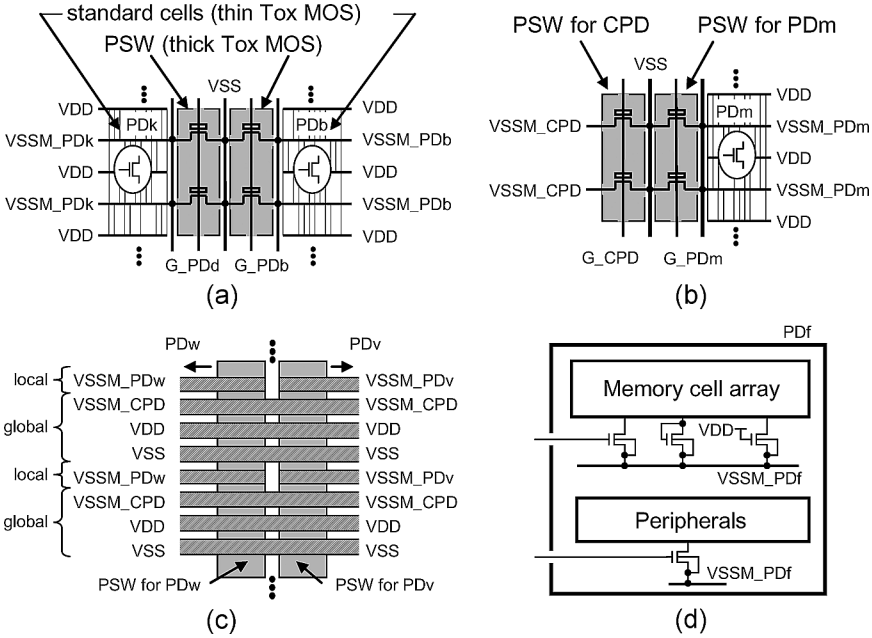


Fig. 7. Precise illustration for implementation of power switches and power lines: (a) power switches for PDb and PDk, (b) power switches for PDm and CPD, (c) power lines for PDv and PDw, and (d) power switch for low power SRAM.

be integrated in the CPD, so, local clock buffers are placed in each power domain. The $\mu$I/O is inserted in the first circuit of the CPD, as shown in Fig. 5(a), which obeys the $\mu$I/O insertion rule. Likewise, repeater circuits are also implemented in the CPD indicated by (b) in Fig. 4 and precise configuration is shown in Fig. 5(b).

Backup latches are also placed in the CPD near the original FFs, indicated by (c) in Fig. 4. Some key information, e.g., the states of the control register, the clock, and the interrupt settings, for achieving a quicker recovery is stored in the backup latches before the domain enters a power-off state. Then, the data of the backup latches is restored to the original FFs during a recovery operation. The precise circuit configuration is shown in Fig. 5(c).

## III. Layout Techniques for Implementation of Dozens of Power Domains

In this section, we discuss layout techniques for integrating fine-grained power gating using HPD scheme. The power domain partition strongly depends on the power switch implementation and the power line implementation.

### A. Power Switch and Power Line Implementation

Overall configuration of power switches (PSW) for the power domains, the CPD, and the SRAM are shown in Fig. 6 and four parts denoted (a) through (d) in the figure are shown in Fig. 7 in more detail. Power switches for each power domain are placed vertically across the chip on two opposite sides of each power domain. Power switches for the CPD are also placed vertically along two sides of the chip.

As shown in Fig. 7(a), the power switch consists of a thick-gate-oxide high-$V_{\rm TH}$ nMOS, which is used for I/O circuitry. The 3.3 V I/O supply ($V_{\rm CC}$) is applied to the gate of the power switches to provide sufficient low on-resistance, even under a low-voltage supply for core circuitry ($V_{\rm DD}$). In the 90-nm processes, the gate-tunneling current is not negligible, constituting about 10% of the total leakage at room temperature. However, the power switch more than sufficiently suppresses both the subthreshold and gate-tunneling currents. The leakage reduction ratio was about 1/4000 for a power domain with 1 000 000 gates. In addition, since the voltage level of the gate of the power switch is higher than the core logic supply $V_{\rm DD}$, this enables high noise immunity for the noises generated by the logical circuit. This high noise immunity is another advantage for high voltage driving the gate of power switches. The power switch of each power domain is controlled by dedicated power switch controller identically. The power switch controllers are gathered in several points in the LSI for easy implementation. The power switch of the CPD also consists of the same nMOS for I/Os, as shown in Fig. 7(b).

A cross-sectional illustration of the power switch of Fig. 7(a) is shown in Fig. 8. The triple-well implantation technique was used for implementing the power switches, which has been applied to achieve the back-bias controlling technique [3]. This structure has the benefit of shutting out leakage of standard cells such as GIDLs by floating the $V_{\rm SSM}$ node when turning off power switches.

The implementation of the power line is shown in Fig. 7(c). Three global power lines, $V_{\rm DD}$, $V_{\rm SS}$, and $V_{\rm SSM\_CPD}$, are laid out horizontally across the chip. The $V_{\rm SSM\_CPD}$ is the power-gated ground line for the CPD. Since we must feed the $V_{\rm SS}$ power supply to each power switch in low impedance, the $V_{\rm SS}$ is implemented as a global power line. This structure provides minimal area overhead for supplying $V_{\rm SSM\_CPD}$ in low impedance to the CPD which is distributed across the chip, because the concentration of the power switches for the CPD achieves small area overhead and simple implementation. Local power lines for each power domain such as $V_{\rm SSM\_PDv}$ and $V_{\rm SSM\_PDw}$ are also

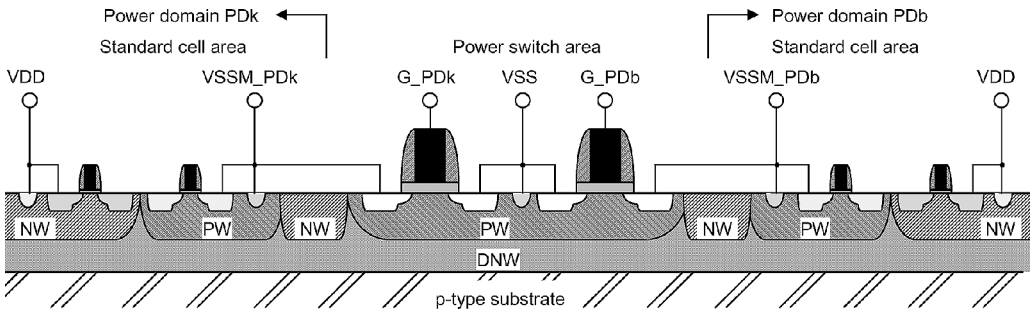


Fig. 8. Cross section in vicinity of the power switch of Fig. 7(a).

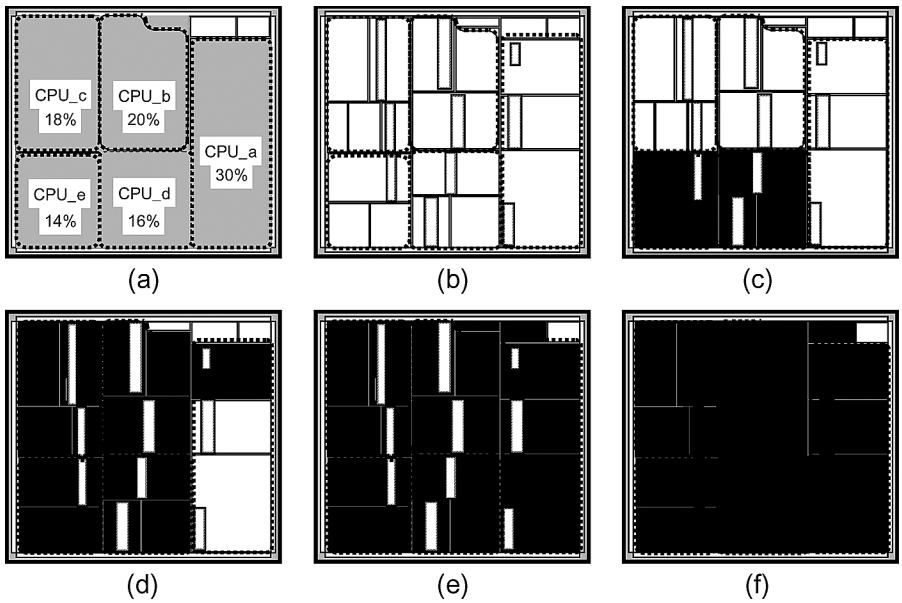


Fig. 9. Conceptual illustration of power-on-and-off combination using hierarchical power distribution scheme. (a) 5 CPU configuration example; (b) all domains powered on; (c) CPU_d and CPU_e are powered off; (d) CPU_b-e are powered off and CPU_a is in resume mode; (e) CPD and always-power-on domain are powered on; (f) only always-power-on domain is powered on.

laid out horizontally on the same layer, but each is dedicated to its own power domain.

Since the power switch is laid out vertically and power lines are laid out horizontally, the CPD is laid out in vertical stripes. This configuration brings minimal impedance of the power supply for the CPD.

### *B. SRAM Implementation*

Power reduction of the SRAM is important, especially for application to cellular phone SoCs, because the total capacity of the SRAMs in those SoCs is increasing. Therefore, low stand-by current with data retention mode is necessary for the SRAM, and low-power SRAM has been developed [15], [18], [19]. As shown in Fig. 7(d), low-power SRAM has its own embedded dedicated power lines for achieving the low-leakage retention mode. In this mode, the embedded power switches are turned off, and the diode and resistors supply a minimum current for data retention. In complete power-down mode, the thick-gate-oxide power switches are turned off, and leakages are significantly reduced. Thick-gate-oxide power switch implementation and power line implementation are the same as those of the logic circuit.

## IV. Power On/Off Combination Example

Based on the above technique, we show examples of applying the fine-grained power gating using HPD scheme in an SoC. Several examples of power on-and-off combinations are illustrated in Fig. 9. We estimated the leakage reduction effect of the HPD scheme by theoretical calculation based on the below assumptions. An SoC has five CPUs: CPU_a (30 parts), CPU_b, (20 parts), CPU_c (18 parts), CPU_d (16 parts), and CPU_e (14 parts) [see Fig. 9(a)]. The remainder consists of the CPD (1 part) and the always-power-on area (1 part). The CPU_a consists of a 8:2 mixture of high $V_{\rm TH}$ MOSFET and low $V_{\rm TH}$ MOSFET, and the other CPUs (CPU_b, CPU_c, CPU_d, and CPU_e) each consist of a 9:1 mixture of high $V_{\rm TH}$ MOSFET and low $V_{\rm TH}$ MOSFET. Furthermore, we assumed the leakage of low $V_{\rm TH}$ MOSFET is ten times larger than that of high $V_{\rm TH}$ MOSFET. The area of the low-power SRAM included in CPU_a is assumed to be 30% of the total CPU_a area.

The case in which all power domains are powered on is shown in Fig. 9(b). The case in which several power domains, such as power domains associated with CPU_d and CPU_e, are powered off is shown in Fig. 9(c). The leakage suppression effect of 1-million-gate power domain by the power switches is 1/4000,

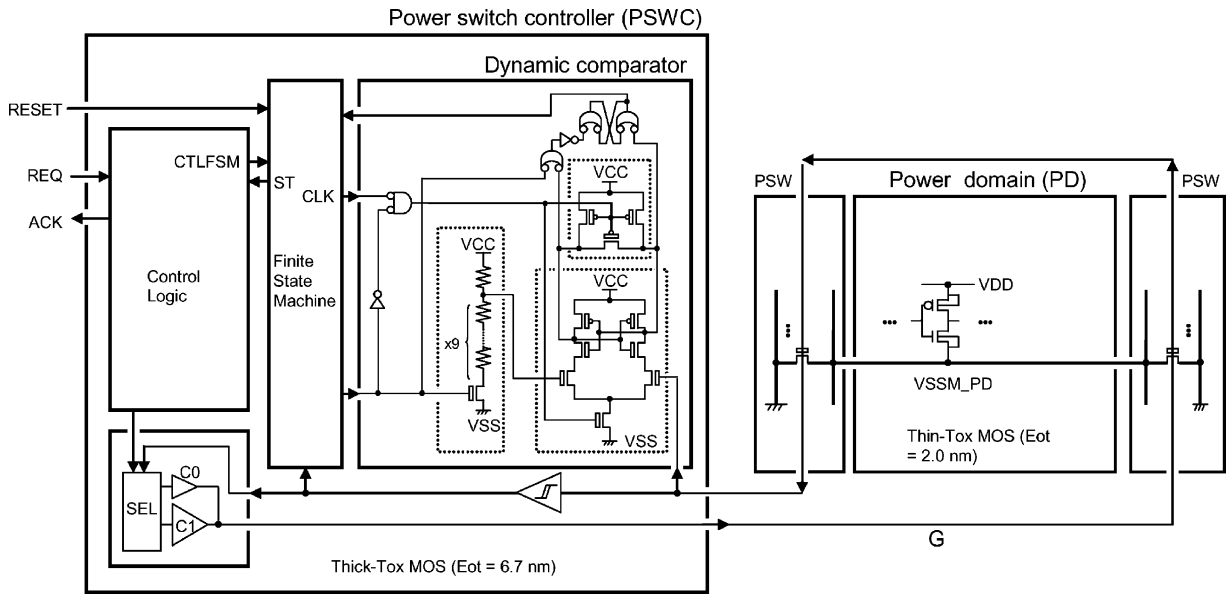


Fig. 10. Power switch controller.

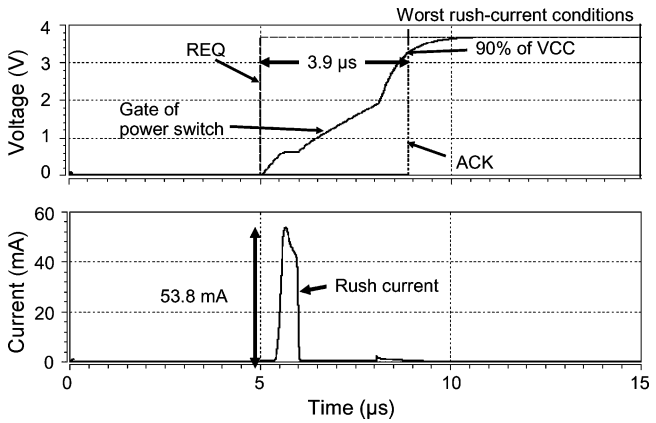


Fig. 11. Simulated waveforms of the power switch controller.

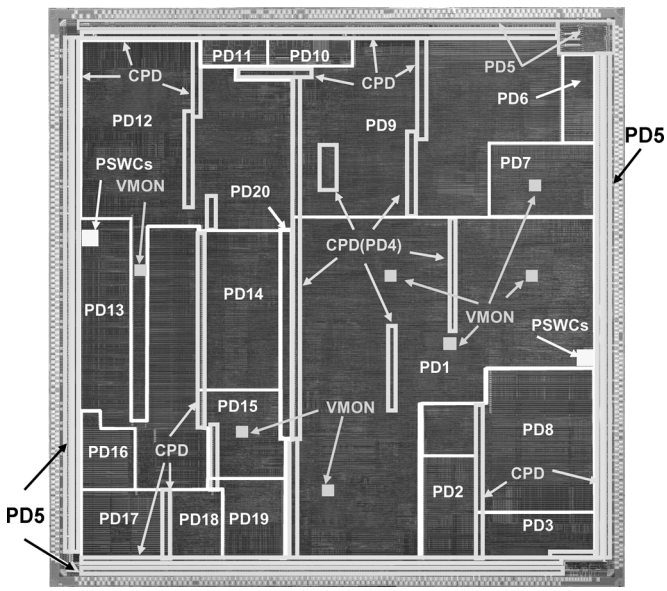


Fig. 12. Chip microphotograph.

and the remaining leakage is reduced in proportion to the powered area. We can estimate that the leakage would be reduced to 71.5% compared to that of the powered-on value of all domains, which is mainly proportional to the powered area ratio. For simplicity, we assumed the total gate width of integrated MOSFETs is proportional to the power domain area. The case in which many power domains, such as power domains associated with CPU_b through CPU_e, are powered off and several power domains associated with CPU_a are powered on is shown in Fig. 9(d). In this case, CPU_a can enter the resume-standby mode [12], [15], which is enabled by using low-power SRAMs [18]. In the resume-standby mode, only SRAMs and minimum circuits in the CPU_a domain are powered on, so the leakage can be reduced significantly and we can estimate that the leakage would be reduced to 5.9% compared to that of the powered-on value of all domains. The case in which the CPD and always-power-on domain are powered on is shown in Fig. 9(e). This mode is used for fast recovering with low leakage. We can estimate that the leakage would be reduced to 1.5% compared to that of the powered-on value of all domains, which is proportional to the still-powered circuit in the CPD and always-power-on domain. The case in which only the always-power-on domain is powered on is shown in Fig. 9(f). This mode is used for standby that exhibits ultra-low leakage. We estimate that the leakage would be reduced to 1% compared to that of the powered-on value of all domains, which is proportional to the still-powered circuit in the always-power-on domain. We assume the leakage of the I/O circuit and power switches are the same values of the always-power-on domain leakages.

## V. Power Switch Controller

Turning on the power switches may cause a large rush current in the power line. This large rush current induces a voltage drop such as an IR drop and an *Ldi/dt* drop. When designing the power switch control scheme, we must be careful not to

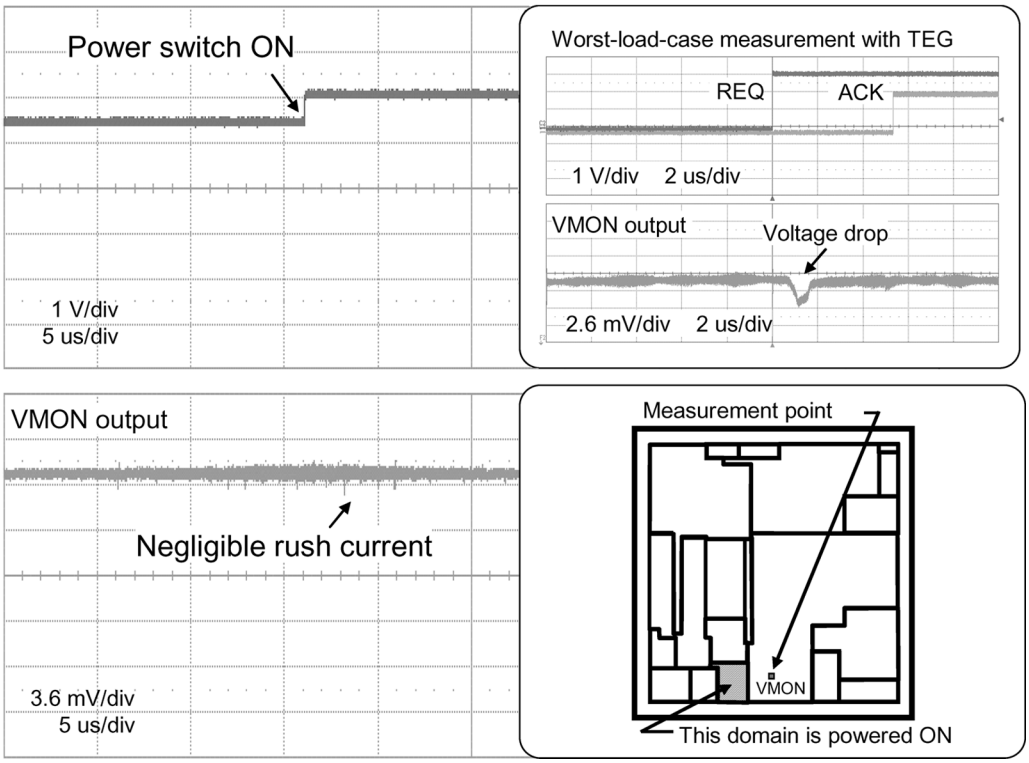


Fig. 13. Measured voltage drop in power-switch-on sequence.

flow this large rush current during the power-on sequence of the power switch. To avoid the rush current, a low-slew-rate driving scheme is the most effective method [11]. We achieved this by using a power switch controller. The main reason for using the power switch controller is that the power switch consists of a thick-gate-oxide high-$V_{\rm TH}$ nMOS, as mentioned above, the supply voltage needs $V_{\rm CC}$ for I/O circuitry, and the routing of the $V_{\rm CC}$ power supply into the chip is difficult. Therefore, to control the power switch, a dedicated power switch controller is necessary. In addition, an acknowledge signal from the power switch controller, which informs the system controller of the power switch condition, must be issued by automatic control in the power switch controller for easy implementation. Therefore, a conventional power switch controller has a timer circuit [11] that waits for the stable powered-on state based on monitoring the output of the driver for driving the gate of the power switch. However, this conventional power switch controller has long time settings to wait for a stable powered-on state, and the area penalty for integrating many flip-flops is large.

The power switch controller (PSWC) we developed is shown in Fig. 10. To achieve a fast transition time between the power-off and power-on states without a rush current, we developed an accurate gate-voltage sensing scheme in combination with a conventional low-slew-rate driving scheme. A driver increases the voltage of the gates of power switches to 90% of the $V_{\rm CC}$ voltage. This sensing scheme detects that 90% drive of the gate of the power switches using a dynamic comparator, which effectively reduces the time margin. That drive of the gate is detected at node G, which is farthest from the driver for accurate sensing. A dynamic comparator consists of the MOS for the I/O circuitry, so the process migration is made easy. In addition, the comparator can be disabled without requiring the period of the power-on sequence of the power switch. Thus, the standby current of the power switch controller can be suppressed. Furthermore, the footprint of the dynamic comparator and the reference voltage generator is small compared to the conventional timer circuit, so the area overhead can be reduced to about 1/2 compared to that of conventional areas.

The simulated results are shown in Fig. 11. A power domain with 1 000 000 gates had a 3.9-$\mu$s recovery time and a 53.8-mA rush current under worst rush-current conditions.

## VI. Implementation Example

A 90-nm one-chip 3G cellular phone processor [17], which is the first application of this hierarchical power distribution, is shown in Fig. 12. According to the reference, the chip specification is as follows. The PD1 and PD6 have two CPUs each, the PD15 has a baseband processor, and there are several dedicated IPs. The chip was fabricated using the 90-nm process rule. There were eight layers, seven Cu and one Al, using CMOS dual-$V_{\rm TH}$, low-power process technology. This chip was partitioned into 20 power domains on a single SoC, and the die size was 11.15 mm $\times$11.15 mm. The area penalties of the power switches were 3.4% of the total chip area. The operational frequency of one of the CPUs, the SH-X2 core, was 312 MHz. Furthermore, the reported measured leakages at room temperature and 1.2 V of $V_{\rm DD}$ were 849 $\mu$A when all power domains were on, 407 $\mu$A for telephony use, 299 $\mu$A for waiting for calling, and 7 $\mu$A for ultrastandby, respectively. Depending on the operational mode, these results demonstrate that by using the hierarchical power distribution, static leakage was reduced from 1/2 to 1/100 compared to all powered-on domains. Therefore,

the leakage reduction achieved by using the hierarchical power distribution was successful.

In addition, a few on-chip voltage monitors (VMONs) were implemented in several of the power domains to measure the power supply drop due to the rush current. A 1-mV decrease in voltage was successfully measured by the VMONs, which converted the local supply voltage fluctuation into a frequency-modulated oscillation. This modulated signal was sent to an external chip. The measured voltage drop obtained with the one-chip 3G cellular phone processor and that under the worst-load case in TEG are shown in Fig. 13. These results demonstrated that the voltage drop was small under the worst case and negligible under actual operating conditions.

## VII. Conclusion

To reduce the increasing leakage current, a hierarchical power distribution for implementing dozens of power domains was developed. This is analogous to clock gating for switching power reduction. This scheme includes two key features: the three power-tree management rules and the distributed common power domain (CPD) implementation. The three rules enable dozens of power domain implementations without increasing design complexity. The CPD implements repeaters for global signal transmission and backup latches. This enables fine-grained power gating without performance degradation.

An example of adopting this hierarchical power distribution scheme was reported as a 90-nm 3G cellular phone processor [17]. The reported static leakage of the processor was reduced from 1/2 to 1/100 depending on the actual mode. Thus, the leakage reduction achieved by using the hierarchical power distribution was successful.

## Acknowledgment

The authors thank M. Yamaoka, S. Komatsu, N. Morino, R. Mori, T. Ajioka, T. Sasaki, F. Shirai, Y. Taguchi, T. Kuraishi, Y. Igarashi, and Y. Tsuchihashi for their valuable technical advice, and S. Tamaki, K. Osada, K. Ishibashi, and S. Yoshioka for their support and useful comments.

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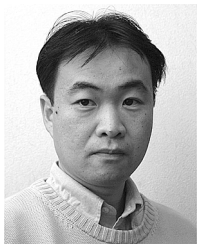
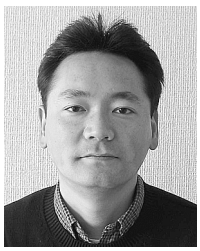


**Yusuke Kanno** (M'05) received the B.S. and M.S. degrees in physics from Tohoku University, Japan, in 1992 and 1995, respectively.

He joined the Central Research Laboratory, Hitachi, Ltd., Tokyo, Japan, in 1997, where he has been engaged in the research and development of high-speed and low-power circuits for embedded DRAMs and microprocessors. His current research is the power gating scheme for mobile SoCs.

Mr. Kanno is a member of the IEEE Solid-State Circuits Society.



**Hiroyuki Mizuno** (M'93) received the B.S., M.S., and Dr. Eng. degrees in electronic engineering from Osaka University, Osaka, Japan, in 1991, 1993, and 2001, respectively.

In 1993, he joined the Central Research Laboratory, Hitachi, Ltd., Tokyo, Japan, where he has been engaged in the research and development of high-speed and low-voltage circuits for SRAMs, microprocessors and embedded DRAMs. From 2002 to 2003, he was a visiting scholar at the Department of Computer Science, Stanford University, Stanford, CA. Since 2005, he has been with the Strategy Center, R&D group, Hitachi, Ltd., Tokyo, Japan.

Dr. Mizuno is a member of the IEEE Solid-State Circuits Society and has been a member of the Technical Program Committee of the IEEE International Solid-State Circuits Conference (ISSCC) since 2004.

**Yoshihiko Yasu** received the B.S. degree in natural sciences and M.S. degree in science and engineering from University of Tsukuba, Ibaragi, Japan, in 1979 and 1982, respectively.

He joined Semiconductor and Integrated Circuit Group, Hitachi Ltd., Tokyo, Japan in 1982, where he was engaged in the development of memories such as high-speed SRAM, pseudo-SRAM, FeRAM and embedded DRAMs, and deep-submicron CMOS logic circuit technologies. In 2003, he was transferred to Renesas Technology Corporation, Tokyo, Japan.

**Kenji Hirose** received the B.E. degree in electronics engineering from Hiroshima University, Japan, in 1986.

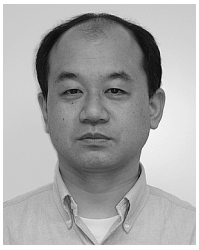
He joined Musashi Works, Hitachi Ltd., in 1986, where he was engaged in the physical layout design for low power and high speed processor, SuperH series. In 2003, he was transferred to Renesas Technology Corporation, Tokyo, Japan. He is a manager of the SOC Device Design Department, and is responsible for the physical layout design of low power application processor, SH-Mobile.

**Yasuhisa Shimazaki** (M'99) received the B.E. and M.E. degrees in electrical engineering from Nagoya University, Nagoya, Japan, in 1991 and 1993, respectively.

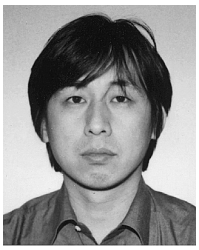
He joined Hitachi, Ltd. as a VLSI Circuit Engineer upon graduation. In 2000, he studied at the University of California, Berkeley, as a Visiting Industrial Fellow. Since 2003, he has been engaged in development of low-power microprocessors at Renesas Technology Corporation, Tokyo, Japan. Currently, he is in charge of designing an ultra-low-power embedded SRAM and high-density standard cell library. His research interests include energy-efficient digital integrated circuits.

**Tadashi Hoshi** received the B.E. degree in information engineering from the University of Electro-Communications in 1994.

He joined Semiconductor and Integrated Circuits of Hitachi, Ltd., in 1994. In 2003, he was transferred to Renesas Technology Corporation, Tokyo, Japan. His research focuses on physical layout of clocks.

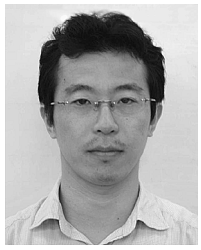


**Yujiro Miyairi** joined Hitachi MicroComputer System Ltd., Tokyo, Japan, in 1984, where he has been engaged in the physical layout design for low power and high speed processor, SuperH series. In 2002, he was transferred to Semiconductor and Integrated Circuit Group, Hitachi Ltd., Tokyo, Japan, and in 2003, he was transferred to Renesas Technology Corporation, Tokyo, Japan. His current work focuses on physical designing of power supply architecture for SH-Mobile.



**Toshifumi Ishii** received the B.S. and M.S. degrees in industrial chemistry from the Saga University, Japan, in 1987 and 1989, respectively.

He joined Hitachi ULSI Engineering, Ltd., Tokyo, Japan, in 1989 and was engaged in the development of circuit for the non-volatile memory, DRAMs, and SRAMs. He also worked on developing the logical and physical verification technology for designing SoCs. In 1998, he was transferred to Hitachi ULSI Systems Company, Ltd., Tokyo, Japan. His current work focuses on designing power supply architecture and power switch control for low-power mobile SoCs.



**Tetsuya Yamada** received the B.E. degree in information engineering and the M.E. degree in information systems from Kyushu University, Japan, in 1992 and 1994, respectively.

He joined the Central Research Laboratory of Hitachi, Ltd., Tokyo, Japan, in 1994. His research interests include micro-architecture of embedded processors.

**Takahiro Irita** received the B.E. and M.E. degrees in electronic engineering in 1993 and 1995, and received the Doctor of Engineering in information and communication engineering in 1998 from the University of Tokyo, Japan.

He joined Hitachi Ltd., in 1998 and moved to Renesas Technology Corporation, Tokyo, in 2003. He is currently working on CPU core design and SH-mobile design.

**Toshihiro Hattori** (M'88) received the B.S. and M.S. degrees in electrical engineering from Kyoto University, Japan, in 1983 and 1985, respectively.

He joined the Central Research Laboratory, Hitachi, Ltd., Tokyo, Japan, in 1985. He engaged in logic/layout tool development. From 1992 to 1993, he was a Visiting Researcher at the University of California, Berkeley, with a particular interest in CAD. He joined the Semiconductor Development Center in the Semiconductor Integrated Circuits Division in Hitachi Ltd. in 1995. He moved to Renesas Technology Corporation, Tokyo, in 2003. He was with SuperH (Japan), Ltd. from 2001 to 2004 to conduct SH processor licensing and development. He is currently working with Renesas Technology conducting CPU core design and SH-mobile design.

Mr. Hattori is a member of IEEE, ACM, IEICE, and IPSJ.

**Kazumasa Yanagisawa** received the B.S. and M.S. degrees in electronic engineering from Waseda University, Tokyo, Japan, in 1977 and 1979, respectively.

In 1979, he joined the Device Develop Center, Hitachi, Ltd., Tokyo, Japan, where he was engaged in the development of memories such as DRAMs, CMOS DRAMs, BiCMOS DRAMs/SRAMs, and embedded DRAMs. He also developed high-speed memory interface SSTL, of which he is a member of the standardization of the specification. Since 1998, he has been responsible for developing deep-submicron CMOS circuit technologies. In 2003, he was transferred to Renesas Technology Corporation, Tokyo, Japan.

Mr. Yanagisawa is a member of the Information and Communications Engineers of Japan.

**Naohiko Irie** received the B.E. degree in electrical engineering in 1988 and M.E. degree in information system technology in 1990 from Kyushu University.

He is the Department Manager of System LSI Research Department of Central Research Laboratory, Hitachi, Ltd. He joined the Central Research Laboratory of Hitachi, Ltd., Tokyo, in 1990. He has worked on computer architecture and micro-architecture for large scale multi-processor systems and processor cores for embedded systems. He has also worked on low-power technology from circuit level to system level.