A Method to Evaluate Power Domain Problems in SoC

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Abstract— **Noise of the power supply voltage can disturb SoC operation by modulating signal frequency of its individual blocks related to their drive current. This disturbance typically results from the complex functions of the SoC combined with their low pin count and current routing not supporting the power demand in the different sections of the die. The pin count, minimized to help take advantage of die area reduction due to technology shrinks calls for fewer power domains resulting in an increase of the current per domain. This, combined with the larger resistance and inductance of the wiring to the target location on the die, due to the increased functionality, gives rise to the DC (IR) and transient ($L^{di}/_{dt}$) voltage droop, the severity of which increases with every product generation. At the same time, the "hot spots" of power distribution are difficult to identify due to the distributed nature of the power supply current and voltage. In this work, we propose a novel approach to evaluate power domain problems in SoC, based on a multi-level analysis of the distribution of total die power to help determine what design tools should be engaged and at which complexity level. Starting from the initial criterion i.e., silicon verification, we recommend that power domain analysis is not required for the domains proven on silicon. We then show that the analysis at a rudimentary level is sufficient if adequate static and dynamic power safety margins can be proven. In such analysis, one may need to perform a relatively simple block level assessment to ensure product functionality in a standard package, depending on the line inductance and operating frequency. For the high die current levels, one would be required to use advanced design tools to resolve problems within every current node and voltage loop, and the preliminary analysis can help define the critical domains. We show how the noise of the power supply system should be considered throughout the design review process.**

I. Introduction

PERFORMANCE of a System-on-a-Chip containing sensitive analog blocks requires a noise-free power network in order to avoid frequency mismatch among the different functional blocks. Unfortunately, this requirement is increasingly difficult to meet. Reduced die geometries make it possible to add more functional blocks to the die without increasing its area. At the same time, the shrinking die size and increasing cost of silicon drive the reduction of the number of power pins. This, in turn, increases average current per pin which combined with the higher power net mutual inductance due to the reduced spaces on the die has the potential to create power surges. Without in-depth analysis of the die or the system, with both the Chip-Designer and the System-Designer resolving the problems, the complexity of the interactions affecting the Power Distribution System (PDS) make it a common practice to simply add a "judgment margin" to the design characteristics, e.g., by assuming the total power noise not exceeding a predefined and acceptable value. This technique, or its failure, is often the reason for marginal behavior when the parts are used in unfamiliar systems.

The definition and description of the power supply becomes more difficult as the system becomes more complex. In earlier designs, the system often dictated the chip behavior, and the chip behavior defined the block requirements. In such a top-down scheme, if the system was known, the power supply characteristics could be extracted and used for circuit design. If the whole chip plan was available, the power supply requirements for individual blocks could be extracted and used for circuit design and simulation of those individual blocks. However, this is not the case for complex SoC products where a bottoms-up approach, from the block to the system level, should be taken instead.

In this work, we present Power Domain Modeling (PDM) methodology as a multiphase process. It starts with defining the assumptions and requirements for the key stages of design development. Individual IP-block requirements may include portions of this information. The phases of PDM analysis are aligned with the design flow and make it possible to first define the severity of the power distribution problem, followed by its engineering evaluation combined with the resource allocation for its solution.

II. Product Power Domains: Die and System Level

Power domain analysis needs to be developed throughout the design process. There are several groups of compromises the need to be decided upon when proposing the power grid architecture, such as the die size, the pin count, and the package inductance. However, at the early stages of product definition and design, there may not be enough information to capture and resolve power distribution problems, although they should remain visible at all times to avoid last moment changes in the product architecture. In this work, we propose a four-level PDM analysis to ensure proper attention to the power distribution throughout the design process.

The System Power Domain Model shown in Fig.1 is a simplified representation of the power supply system of the printed circuit board (PCB) designed for product application, and the chip connected through it. This simple model helps

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minimize the simulation time and allows abstraction to separate the "requirements" from the "behavior". The "Bypass Capacitor Model" should be a realistic model of all bypass components planned for the board. In addition to the voltages resulting from the current demanded by the IP blocks on the chip, the System PDM includes an estimate of the power distribution and voltage-source impedances, which are required to connect the chip through the PCB. In cases of the extremely high rush current values, i.e., the $^{di}/_{dt}$, the bypass capacitors placed at defined locations are often required to make the application work.

The power domain block diagram of the product power domain system in Fig.1, viewed from right to left, starts from the packaged IC product. This product has its resistances and capacitances as well as the piece-wise-linear (PWL) current source. These elements should ensure that the internal die architecture would prevent from power distribution problems. If that condition is not met, no compensation using bypass capacitors at the PCB level can mitigate the on-die noise of the power supply. The next step is to consider the packaged IC product in the context of a subsystem, which supplies the power through on-board, local power distribution, possibly impacted by the aggressor noises, which can be compensated by the bypass capacitors on the PCB. This subsystem, in turn, is connected to the global power distribution, which uses the VDD from the voltage regulator module (VRM).

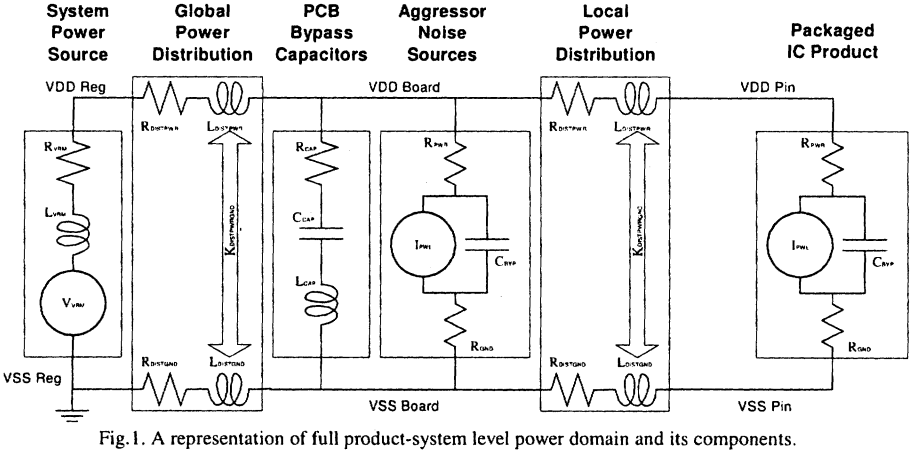

Fig.1. A representation of full product-system level power domain and its components.

Power domain components at all levels are expected to have all of the RLC elements, except the ones on the die which due to the physical dimensions of the domains being smaller than their interaction range, are usually considered inductance-free. However, this presumption needs to be verified for small geometry circuits such that, in a full product application, the entire system, as well as its all components, would be represented by all types of parasitic elements over a range of frequencies.

The within-die PDM analysis can be based on a the architecture model as shown in Fig.2. The die level PDM diagram focuses on the individual domains,as an extension to the system level representation. Each of the on-chip domains should be individually compensated over the frequency range by the on-die capacitors. To that end, one should extract the equivalent circuit impedance Z(f) and compare it with the predetermined value Z_0 based on the maximum allowed voltage droop calculated from the supply current requirements of the product. One can modify the compensating capacitance as required to ensure $Z(f)<Z_0$ for all frequencies of interest.

Such simple analysis is compromised by the difficulty in obtaining the lumped RLC values for every electrical node within the die based on the distributed schematic representation of the product. Depending on the required accuracy, it becomes necessary to use engineering evaluation as first step or specialized tools as the final approach to resolve the PDM problem.

III. Multi-Phase Power Domain Analysis

If the PDM analysis is not to become a task as complex as the chip design itself, its significant portion has to rely on the proper engineering estimation. Its accuracy increases as the product design cycle. General PDS requirements should be known at the beginning of the design process. For example, the new part may use low power and its architecture would not be impacted by the noise precautions related to the DC or transient current. As a starting point, one can assess the design risk based on the similarity of the new part to the parts existing on silicon. Towards the end of the design cycle, sufficient details should be available to confirm this assumption or to enable detailed power distribution analysis. If the consecutive PDM steps have been followed throughout the design process, the requirements of power domain compensation should not become a surprise.

IV. Power Domain Requirements and Expectations

The PDM process should ensure that the part under analysis meets customer specifications, e.g., power noise

levels as reference points. These requirements should be specified for each domain, for both DC and transient currents, in mV or % of the nominal power supply. The task to meet the specifications is of different complexity for the DC and for the transient power. In the first case, it is related to the simple analysis of the IR drop, in the second, it requires complex Ldi/dt calculations for which the circuit schematic may not provide enough information due to the distributed nature of the power problem.

One method of PDM analysis showing that the design passes the requirements is to ensure that the block, chip, and system-level estimations converge with good accuracy. (The criterion for "good" accuracy should be defined in mV of voltage droop, mA of current demand, or as a % of the power supply). It is unlikely that all the estimations early in design cycle will match on the first try, so a plan should be devised to ensure passing of the subsequent review only upon meeting the matching thresholds. For instance, the current demand of the various IP blocks must match that of the chip level. However, this method would not take into account the overall power requirements related to the die specifications.

The method we propose below is to divide the problem into several steps. The first one is to determine if the product belongs to one of three groups. The first group, the low-power products, would draw such low currents – DC and transient, that it would be easy to prove that the static and dynamic voltage droops would be well within the margins required by the product function. The second group, the high power devices, would require complex analysis and tools, for which the engineering estimates can only help identify the problem level and how much capacitor compensation is needed. The third group, the "borderline", would include devices where power distribution may be a problem for some domains. The initial analysis would help define them and verify if the compensation is necessary. The methodology outlined is intended to be independent of the tools used to perform the analysis.

For the medium and high-power devices, one should avoid overcompensation by adding an large number of decoupling capacitors to the circuit or system. Too high decoupling capacitance may introduce ringing and the involved power domains may need to be divided instead. As discussed above, the on-board capacitors should compensate the VRM (voltage regulator module), not the power noise within the die. Both on-die and on-board capacitors should be placed according to the design rules developed to ensure that the physical area or volume occupied by them is not too large for the product application.

V. PDM Problem Severity and Resolution

The goal of the PDM analysis is to identify and resolve the power noise problems regardless of the target power consumption of the die. If done in a comprehensive way, this analysis can take multiple man-weeks and require expensive, specialized tools. However, in many cases, e.g., for the low power products, it should be possible to quickly obtain a PASS/FAIL answer to the required criteria based on a simplified engineering analysis. The following is a procedure, which should help approve the design or identify the issues with the PDS. While the proposed numbers may be arbitrary, they should be based on the best engineering judgment and need to be verified on die. The key benefit of the procedure is the simplicity and time to solution and its key risk, the lack of the underlying physical criteria, should be resolved based on the calibration to silicon.

The proposed simple engineering analysis is focused on first reducing the PDM problem to the appropriate severity level. For the low severity, the procedure shows how to approve the existing product design. For the medium and high severity, it helps identify the issues to be resolved with more advanced tools. Based on the foregoing discussion, this can be done on four levels:

Level 0: No PDM problem exists, as proven out on silicon. The reference part performs well within the assumed frequency range and the new product is its very close derivative. For example, the new product is similar or less critical than the existing one, in terms of total power consumption, PCB applications, the package and pinout, the VRM, and the socket. It can be e.g., a subsection of the existing part with lower memory density at the same size and pinout, and therefore, lower total power and power per pin. For such a close product derivative, PDM analysis is not required as long as there is no potential for surprise failures.

Level 1: There is no reference part on silicon, but no PDM problem should exist for the current part, based on the most pessimistic engineering estimates for each power domain separately and all domains combined. The new product draws such low static and dynamic power that the IR droop over the routing and the *Ldi/dt* noise is insignificant. No disturbance to the SoC components based on the operating frequency dependence on power supply is expected.

Examples:

DC voltage droop analysis:
10 mA of total ICC
1 ohm for longest routing resistance
resulting in 10 mV of max IR drop
as compared to
product requirement of 5% of VCC of 1.2 V, i.e., 60 mV
600% safety margin

Transient voltage noise analysis:
10 mA of current burst (di)
over 1 ns (dt)
corresponds to max AC current noise of 10MA/s, which
over the inductance path from the pad to the device of 1 nH
results in 10 mV of Ldi/dt voltage noise
as compared to
product requirement of 25 mV of VCC
250% safety margin

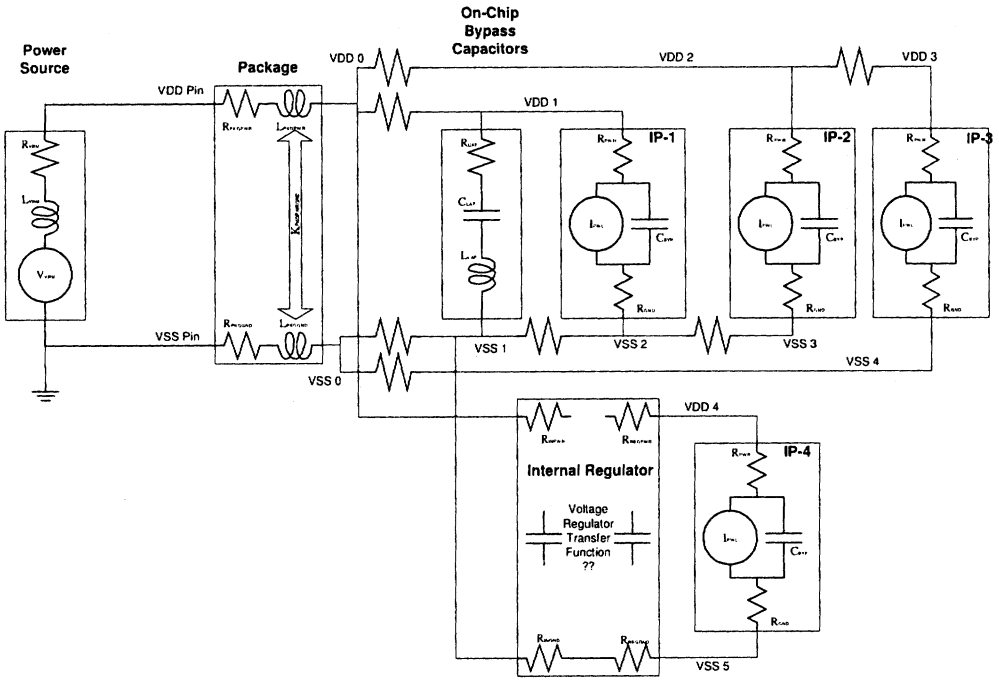

Fig.2. Die power domain, with VDD and VSS connections. Multiple power connections or voltages must be included in the Whole-Chip Power Domain Model.

If the safety margin calculated above is close to or less than 0, some power domains on the die do not meet product requirements. One should identify these domains and analyze them separately. The impact of the bonding, package, and VRM inductances needs to be verified as well, to ensure PDM compliance at system level. When excluding the domains from the more detailed analysis, one should ensure that none of them shares ground. The ground bounce is a key PDM failure mode and to prevent it, only the domains with very low currents (e.g., 10 mA) are allowed to share the Vss node.

The analysis at level 1 would first make it necessary to list all the power domains and specify their voltages and currents. It would then allow dismissing all the power domains, which already exist on silicon and do not cause any problems, except the ones which are sharing grounds. One should also verify the number of pads, to ensure that the current per pad is not too high.

For the AC/transient current analysis at level 1, it is necessary to first define the max allowed voltage by which the power supply can be disturbed, called max ripple voltage, based on product requirements. Its value is compared to the VCC and the outcome should not exceed the predetermined percentage of the power supply voltage. As the next step, one would estimate the AC power noise, ACPN, based on:

- the clock frequency f, the number of cycles from sleep to active N, the average drive current per gate I_{DG}, and the number of logic gates in the domain N_G:

$$ACPN = f \cdot N \cdot I_{DG} \cdot N_G$$

- the arbitrary, expected ratio of DC to AC current AC/DC, and the die DC current, IDC:

$$ACPN = AC / DC \cdot I_{DC}$$

- manual entry of $L \cdot {}^{di}/_{dt}$, if readily known from the simulations.

These values are then compared to the specified power noise numbers.

Level 2: Some power domains of the new product may draw large currents resulting in power noise exceeding the specified limits. Such domains should be easy to compensate by the on-die decoupling capacitors. For this level, CAD tools are limited to Spice simulations and simple engineering assessments to ensure proper compensation across the frequency range.

Level 3: Multiple domains on the die draw large currents, potentially giving rise to severe power distribution and noise problem. Specialized tools are required to determine the compensation of the PDS network by the capacitors or architectural changes.

VI. Alignment With Design Review

One can align PDM information flow corresponding to the design review stages with the PDM severity analysis at four levels (0 to 3). The advantage is to have a step-by-step correlation of the design progress to the PDM analysis. For example, at the beginning of the design cycle, one should have enough information to decide if the new product would require high or low power, making it possible to perform the

analysis at level 0 and create plans for the subsequent levels. Then, in addition to confirming level 0, one should be able to list the power domains and proceed with the preliminary analysis at level 1. Should the higher levels be required for medium- or high-power parts, these could be performed based on the information available later in the design process. One can recommend an alignment structure, which interlocks the design review and analysis.

VII. Conclusions

We proposed how to divide the product power domain analysis effort into different levels to expedite the process especially for the low or medium power parts. Chip-IP Power Domain Model including Static and Dynamic Current demand from the IP block circuits can be performed in four stages, where the DC network and the distribution impedances internal to the block or external to the chip define the system transient voltage levels (at the terminals of the Chip-IP). Power Domain distribution resistance and reactance, and VRM dynamic effects can be successfully compensated using the proposed routine.

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