Low Power Synthesis Techniques

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Introduction

- The mobile age has resulted in companies competing on battery life. As devices become increasingly complex, they require a better performance. However, complexity consumes more power. As battery technology is progressing more slowly than the digital systems, the digital systems must carefully manage their energy.
- This research review investigates techniques used to reduce the power consumption of a device.
- There are two main areas of power consumption:
- Dynamic Power - The power consumed when the module is active and switching.
- Leakage Power – The power consumed when the module is not switching and is caused by non-ideal characteristics of CMOS technology. This only becomes a significant problem with technologies below 100nm with around 22% of total power consumed on a 90nm FPGA being from leakage.

Power Gating

- Power gating is where individual modules are turned off.
- This is done by using either a PMOS or NMOS transistor in series with the Power or Ground rail respectively.
- This reduces the leakage power of the module
- Issues are encountered due to:
  - Outputs floating
  - State Retention
  - Power manager
- Floating output are solved by using a clamping AND or OR gate.
- State Retention Registers can be used to save the state when powering down the module.
- Scan path can also be used to quickly clock the state in/out.
- Where state retention is needed, time overheads to wake the module are increased.
- Power manager is used to control state retention and clamp signals.

- [2] uses a technique called Sub Clock Power Gating to gate combinational logic for half of every clock cycle.
- State retention and power manager are not needed.
- Isolation and gating are functions of the clock.

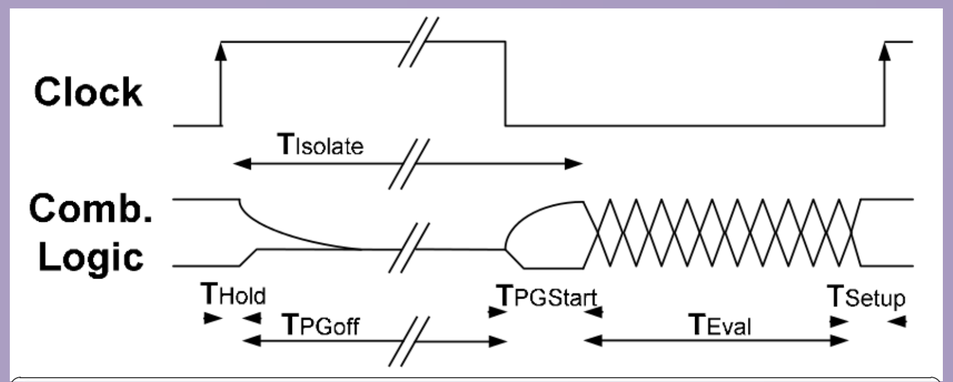

Fig. 2 – The timing of signals for Sub Clock Power Gating [2]

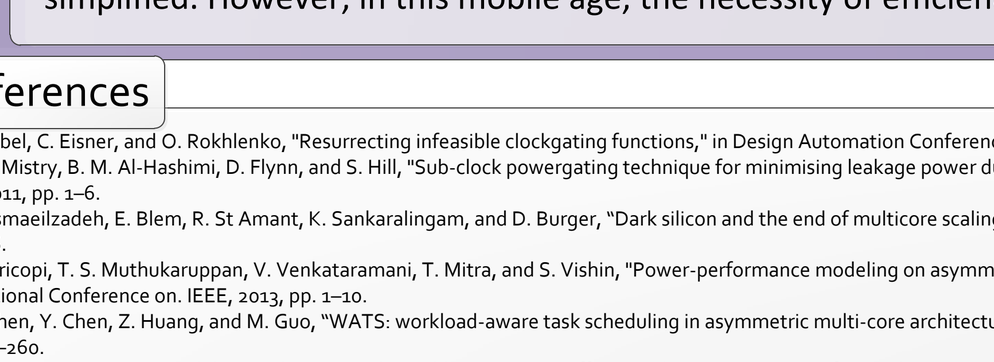

Fig. 3 – The Architecture for the ARM big.LITTLE processor

Clock Gating

- Clock gating is where the clock to a module is disabled.
- This is done by and AND gate and a latch.
- It saves dynamic power as the module does not switch internally as the state does not change.
- Issues encountered:
- The gating function
- The decision of when to gate can be done in logic.
- This logic can be very large and even consume more power than the clock gating saves.
- Two techniques can be used to help this:
- Grouping – modules with similar gating functions are placed near each other to share logic
- Approximation – smaller logic functions are used where the module is gated less, but results in a smaller gating function and still saves power. [1]

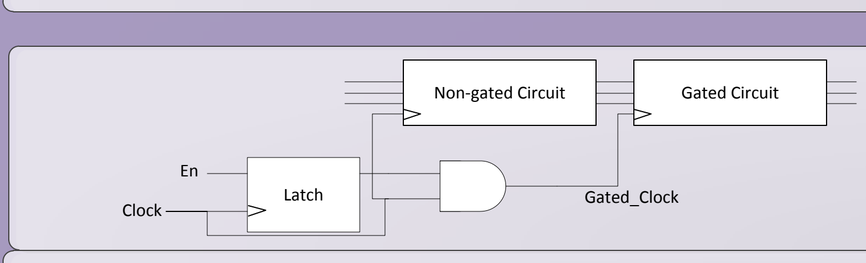

Fig. 1 – The circuit to implement Clock Gating

Asymmetric Multi-cores

- Asymmetric multi-cores are processors with two or more cores.
- The cores are architecturally different with one another.
- The cores can be optimised for different operations.
- The ARM big.LITTLE processor has two cores: an A15 performance core and an A7 energy efficient core.
- The cores are very different – A15 is an out of order processor with hardware performance counters. The A7 is an in order processor with a smaller cache than the A15.
- Cores in an asymmetric system must both support the same instruction set.
- ARM big.LITTLE also supports Power Gating of the cores.
- The main issues with asymmetric multi-cores is the task allocation to the cores.
- Some solutions include:
- Memory intensive tasks are given to the small core and computationally heavy tasks to the large. Although this is simple, it is suboptimal [3].
- Using run time statistics to estimate the performance on the other core, such as cache hits, branch misprediction. However, the two cores may not both have hardware counters for these. Cycles Per Instruction (CPI) can be used to measure performance [4].
- Task stealing policies can be used for a core to take tasks from the other when it is idle [5].
- Compiler directives can also be used.

Conclusion

- Clock gating is simple to implement with little hardware over heads. Dynamic power is saved here with potentially 44.6% reduction is dynamic power on an eight bit microprocessor [6].
- Power gating is more complex, requiring a manager to decide if a sleep state should be entered. A larger hardware over head is needed for traditional power gating. Sub Clock Power Gating can increase energy efficiency 2.5× in a microprocessor [2].
- The ARM big.LITTLE combines a few lower level power saving designs. The high level idea of two cores is a promising approach to give a high performance, energy efficient processor. It will only be a success with correct scheduling of tasks, however.
- A good low power design can utilise one or more techniques, depending on the application of the system. Where performance is not key, the problem is simplified. However, in this mobile age, the necessity of efficiency and power is requiring techniques to break the power/speed compromise.

References

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