Overview of Mixed Signal Methodology for Digital Full-Chip Design/Verification

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ABSTRACT

In conventional chip design digital simulation and analog simulation are carried out separately by digital designers and analog designers. Digital designers run block simulation on RTL code and SDF back-annotation post layout simulation which includes the timing information in digital simulator such as ModelSIM. Analog designers simulate the circuit in transistor level analog simulator. Several interface problems are missed in designs because of lack in a true verification between analog and digital blocks till the silicon comes out of the fab. The new digital full-chip design / verification flow combines both digital and analog simulation in a single environment. It provides a critical bridge which links analog and digital blocks and performs the true full chip design and verification. Using this new flow digital designers and analog designers can work closely together and check the full-chip function and interface between digital blocks and analog blocks. Analog behavioral models can be introduced to replace transistor level block which can save simulation time by hundreds of hours on the initial design cycle for functional design. Fast-spice simulator which also has been integrated into Mixed-Signal flow can be used in the final full chip simulation in which the transistor level simulation is required.

INTRODUCTION

With the rapid development of the CMOS technology low-cost, high-performance and high integration density are the goals that are driven by IC industry. More and more digital and analog blocks need to be integrated together to form mixed-signal block and these two parts cannot be separated [1-2]. Modern IC chips usually consist of analog and digital function blocks, either with big analog portion (big A) or big digital portion (big D). For example, in communication systems, when micro-integrated systems receive input signals from real world the data conversion must be accomplished. The preprocessing of input analog signals to digital signal is often required and this leads to the mixed-signal integrated system. DSP block always processes digital signal and the final digital signal will be converted into analog signal using the D/A converter. Digital blocks have some advantages such as highly automated design, less sensitive to noise especially to substrate noise in the chips, which makes digital blocks almost 90% or more in the modern IC chips. Even though analog partition in IC has only less than 10% occupation, the design of analog blocks is more complex and time-consuming [3-5]. This paper focuses on the full chip design and verification with big D emphasis.

Figure 1 shows the current digital design simulation flow used by designers. Both digital and analog blocks are simulated for system functional re-checks. For timing information, custom blocks are different from standard cell blocks. For Standard cell based designs, industry has complete flow from verilog code to layout that can be provided by foundry. In post-layout simulation, a commercial tool called Primetime can generate timing information into file and this kind of file format is called Standard Delay Format (SDF). However, for custom digital block designer runs transistor level simulation and conducts timing analysis using commercial tools such as Pathmill. A flow with tools that handle the transistor timing analysis and generate the Synopsys library is not readily available from EDA vendors due to the non-standard signal path in the custom digital cell which makes it difficult to automate the flow. (Synopsys lib is used in Primetime to generate SDF files for custom digital cell post layout simulation.) For custom digital cell post layout simulation, we use the same methodology as it for standard cell but with a special home grown tool to first generate Synposys library. We then use PrimeTime to create SDF file as shown in Figure 3. Because there is no complete automation solution available some work must be done manually and it is time-consuming.

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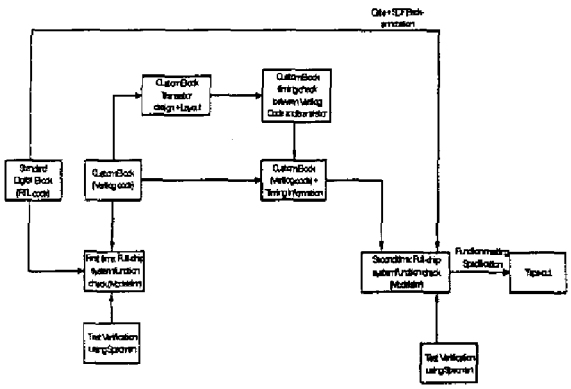

Figure 1: Current Digital design flow

Designer using the current flow in Figure 1 faces one challenge — the fact that the function of full-chip works fine doesn't guarantee that blocks using transistor level simulation would work as well in the chip. The issue can be attributed to the mismatch in interface between digital blocks and customer digital blocks which is represented by the behavioral model and not the transistor level netlist. For example, PLL circuits are widely used to generate clock function in the digital design. In the full-chip simulation, digital designer uses Verilog code to describe the behaviors of PLL and assumes that function within PLL will always work (Verilog code just describes the behavior of PLL); however in reality PLL's frequency divider and VCO are more complicated and their functions may not function well when interfacing with other digital blocks. Verilog code alone is not capable of catching this problem. Therefore it is imperative to develop a full chip design and verification flow which combines the true analog and true digital simulation capability into a single simulation environment to carry out the Mixed Signal simulation before tapeout.

Digital Full Chip Design/Verification Simulation Flow

We propose a new digital full-chip design/verification, or so call big D/small A flow, to address the current pure RTL code digital and analog verification issues. We define the requirements for the flow: mixed signal simulator should support both analog and digital simulations simultaneously; the A/D and D/A converters should be capable of automatically converting digital signal to analog signal and vise versa, and the tools should support Mixed-signal language such as VHDL-AMS and Verilog-AMS [6-8] as well as transistor simulation. ADVance MSS (ADMS) [9] tool from Mentor Graphics is one of the tools that satisfy the above requirements. Figure 2 shows the component of Mentor ADMS. It is obvious that ELDO kernel and MODELSIM kernel are combined together and forms ADMS simulator. This tool is capable of running pure analog, pure digital and mixed-signal simulations.

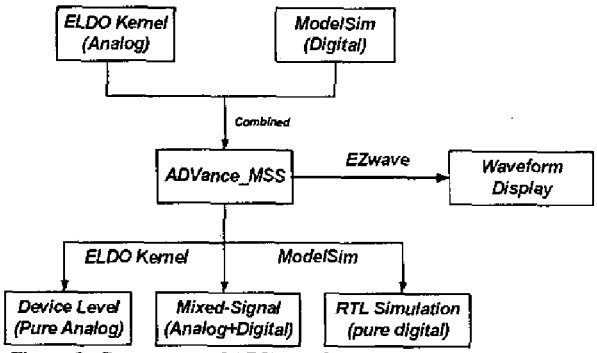

Figure 2: Component of ADVance MSS simulator

The proposed flow suggests three types of functional checks: The first type of check is **RTL** full chip functional check. In this check each block written in Verilog code is simulated in ADMS for full-chip function verification. Second type of check is the digital to custom block interface check where the targeted custom block is replaced with transistor level netlist. This check is performed with **RTL and Transistor Level Simulation** to ensure the validity of the block interfacing. However, we do not include the extracted parasitic RC information here as this is time consuming. The last type of the checks is the **Post Layout Function Check** which includes timing information (in SDF) for standard cell and custom block in RTL and parasitic RC for custom block in transistor level netlist. This check is time consuming but the results provide comprehensive view of the circuit performance.

RTL Check: If the block is composed of standard cell library there exists the complete standard flow from verilog to layout in the industry and the required files can be provided by the foundry. For example, the foundry provides Verilog code, transistor level netlist, GDS layout files and Synposys library for standard cells. However, the same library is not readily available for custom digital block. Design engineer needs to generate RTL Verilog code according to the block function spec. Combined with standard digital block and custom block, full-chip system function is checked or simulated by ADMS. This is pure digital simulation and the functional verification environment is in SPECMAN.

RTL/Transistor Level Check: After RTL functional check custom block is passed to designer to realize the function in transistor level and this step is called customer block transistor design. Replace some custom block with transistor level netlist and keep others in verilog format, designers can start the second-time system function check or simulation (without parasitic and timing information) in ADMS. If full-chip has more than one custom digital block, designer can replace the interested blocks by transistor netlist and the others still keep in behavioral model with RTL code. This is a truly mixed signal simulation which combines the digital and the analog simulation in a single environment.

Post Layout Function Check: For post-layout simulation designer uses PrimeTime to generate timing information (in SDF) based on synposys library for standard cell and custom block in RTL and then back-annotate the SDF file to RTL netlist. As for custom blocks using transistor level netlist designer extracts the parasitic RC from layout and then back annotates to pre layout transistor level netlist in post layout function check. As we know, when transistor netlist is included in the simulation the speed will be greatly influenced. In order to improve the speed, the fast spice simulator should be used or analog behavioral model that replaces the transistor block should be generated for MS simulation. We will introduce the analog behavioral model generation in the next section.

There are many fast spice simulators available commercially— HSIM from NASSADA, MachTA from Mentor, STARSIMXT/Nanosim from Synopsys and Ultrasim from Cadence. Mach TA form Mentor has already included and HSIM is announced to be integrated into ADMS. [10]

Analog Behavioral modeling and Calibration

When more and more transistor netlists are included in full-chip, the simulation speed will be very slow even if fast simulators are used. To overcome the speed issue, analog behavioral modeling is introduced. Analog behavioral modeling describes the function of analog transistor block using Verilog-A, Verilog-AMS or VHDL-AMS. We generate raw behavioral model with generic parameters and these generic parameters are left to adjust the behavior of model. Based on circuit behavior in transistor-level netlist, we adjust the generic parameter to generate the same behavior as transistor level and the procedure is called behavioral model calibration. Figure 4 shows the model calibration procedure and Figure 5 shows comparison of OP-AMP functional curves, before and after model calibration [11].

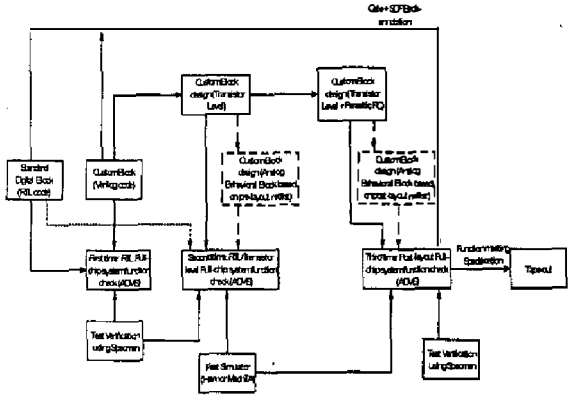

Figure 3: Digital full-chip design / verification flow with pre- and post-layout

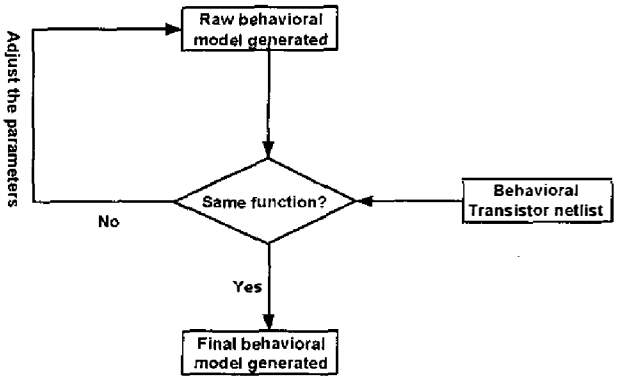

Figure 4: Procedure of behavioral model calibration chart

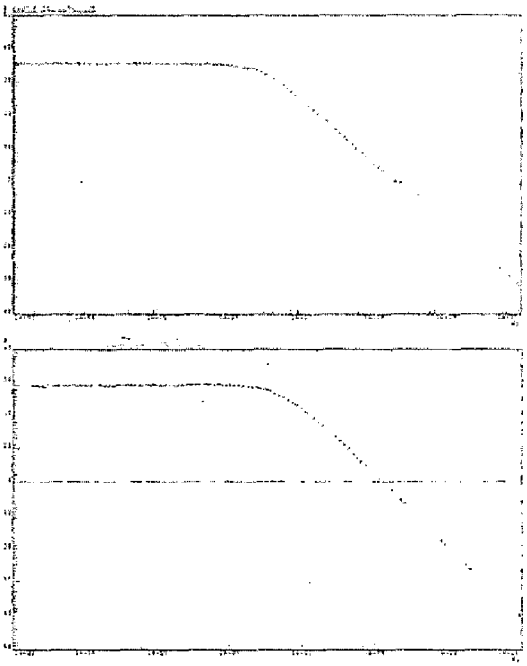

Figure 5: Comparison of OP-AMP functional curves before and after model calibration: Symbol curves from transistor level and line from behavioral model. (x axis is frequency and y axis is output voltage in db scale)

A Case study

In this section we will demonstrate our proposed digital full-chip design/verification flow through use of the test bench to perform the RTL/Transistor level full chip verification. (No SDF back-annotation for Gate level and no parasitic RC for transistor level invloved). In this test case, we have full chip coded in Verilog code and frequency divider in transistor netlist. The clock time function is generated by PLL. First we perform the RTL function check. Then we replaced the frequency divider in PLL with transistor level subcircuit netlist to check the validity of the frequency divider interfacing with other blocks. Frequency divider netlist comes from Cadence schematic netlist in HSPICE format (HSPICE netlist is completely compatible with ELDO).

Figure 6 is the flow chart to run digital verification flow in ADMS. Figure 7 shows the different frequencies output from frequency divider (DIVOUT100 is almost 200MHz, DIVOUT300 is almost 600MHz, DIVOUT900 is almost 1.8GHz and DIVOUT1200 is almost 2.4GHz) and Figure 8 shows the function waveform in top level.

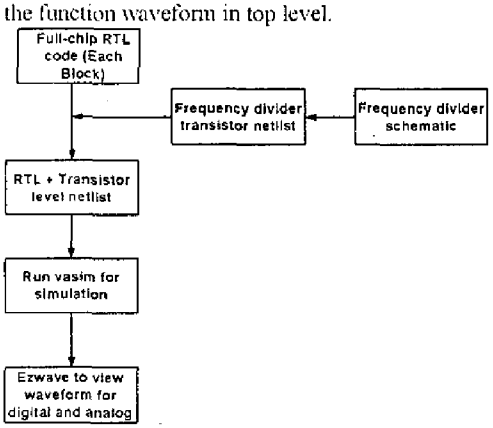

Figure 6: Test case flow chart to run digital verification flow

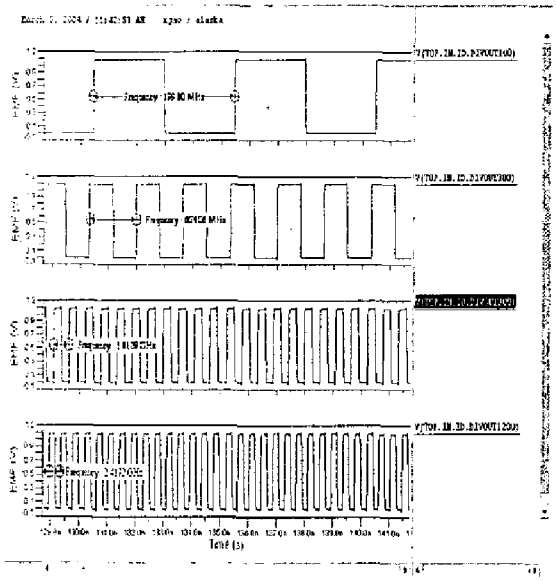

Figure 7: Different frequency output from frequency divider

Summary

A newly developed digital full-chip design/verification flow is introduced. In this flow, we include three types of function checks for the full-system verification based on the design needs: pure RTL, full-system function checking by pre-layout netlist and gate level, and the full-chip function checking by post-layout (Gate + SDF back annotation for standard cell block and custom blok in RTL and parasitic RC + transistor netlist for custom block in transistor netlist). To improve simulation speed in the flow, the built-in fast spice simulator and/or behavioral model methodology can be selected. Behavioral modeling calibration is also presented in this paper. Finally test case is chosen to demonstrate this methodology. The flow will help digital and analog designers work more efficiently and reduce overall design cycle time.

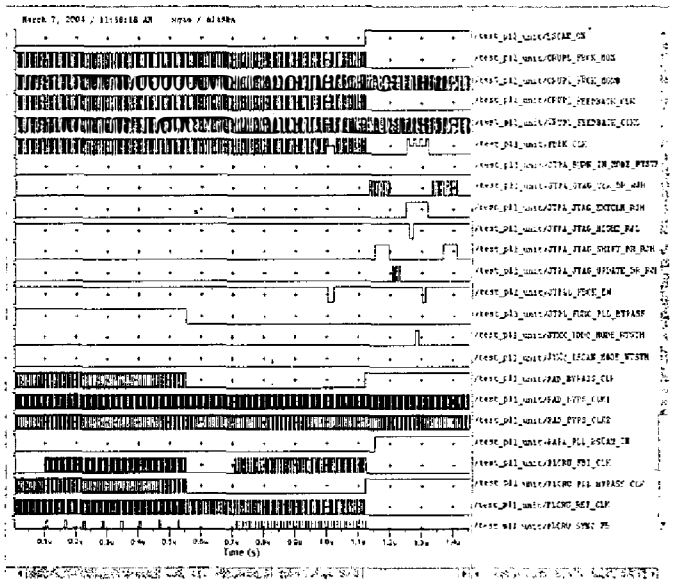

Figure 8: Function wave in top level block

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