Bilkent University
Computer Science Department
CS224 – COMPUTER ORGANIZATION
Preliminary Design Report
Lab 6
Section 4

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1)

No.	Cache Size KB	N way cache	Word Size in bits	Block size (no. of words)	No. of Sets	Tag Size in bits	Index Size (Set No.) in bits	Word Block Offset Size in bits1	Byte Offset Size in bits2	Block Replacement Policy Needed (Yes/No)
1	128	1	32	4	2^13	15	13	2	2	No
2	128	4	32	16	2^9	17	9	4	2	Yes
3	128	Full	32	16	2^0	26	0	4	2	Yes
4	256	2	64	8	2^11	15	11	3	3	Yes
5	256	4	64	32	2^8	16	8	5	3	Yes
6	256	Full	16	16	2^0	27	0	4	1	Yes

2)

Memory Address Accessed (hex)	Set No.	Hit (yes/no)
00 00 20 24	00	No
00 00 20 42	00	No
00 00 20 68	01	No
00 00 20 04	00	No
00 00 20 0C	01	No
00 00 20 4C	01	No

3)

Memory Address Accessed (hex)	Set No.	Hit (yes/no)
00 00 00 2C	01	No
00 00 00 48	01	No
00 00 00 44	00	No
00 00 00 0C	01	No
00 00 00 04	00	No
00 00 00 0C	01	yes

4)

Physical memory size is 4 GB.
Word size is 2 bytes.
Block size is 32 words.
Cache memory data area size= 1KB.
N= 8. Assume that LRU is used for block replacement.
D (dirty bit) is used to keep track of the changes in the cache blocks.

4.1)

Tag: 25 bits
Set: 1bit

Byte Offset: 1 bit
Block Offset:5 bits

4.2)

Data: 32 x 16 bits
Tag: 25 bits
Lru: 3 bits
Valid: 1 bit
Dirty: 1 bit
Number of LRU bit per block: 3 – log2N

Block Size: 32 x 16 (Data) + 25 (Tag) + 1 (Valid) + 1 (Dirty) + 3 (LRU)= 542 bits

4.3)
Set Size = 542(Block Size) x 8 (Associativity) = 4336 bits
SRAM Size = 4336 (Set Size) x 2 (Size) = 8672 bits

4.4) The total number of blocks in the cache and the size of each block determine the Static Random Access Memory (SRAM) capacity of a cache memory. We can do away with the three bits per block that are usually used for LRU tracking if we take into consideration a cache that has a random replacement strategy. Assume for the moment that each cache block is 539 bits in size. Each block has the same size when LRU tracking bits are not required. Thus, the following formula can be used to get the overall SRAM size: Block size * number of blocks * number of sets equals the total SRAM size. The number of sets doesn't change because we are simply taking into account the effect on the SRAM size. Assume there are eight sets in the cache. Block count is equal to (number of sets) * (associativity). The number of blocks in a 2-way set-associative cache would be: Block count is 8 * 2 = 16. Changing the values in the SRAM size formula: Total SRAM bit count is 16 * 539. SRAM size total: 8624 bits Thus, the overall SRAM size would be 8624 bits if a random replacement policy was used and LRU tracking bits were not required. When compared to a cache with the same block size and a replacement policy that necessitates LRU tracking, this signifies a 48 bit reduction.