

Verified Compilation of Noninterference for Shared-Memory Concurrent Programs

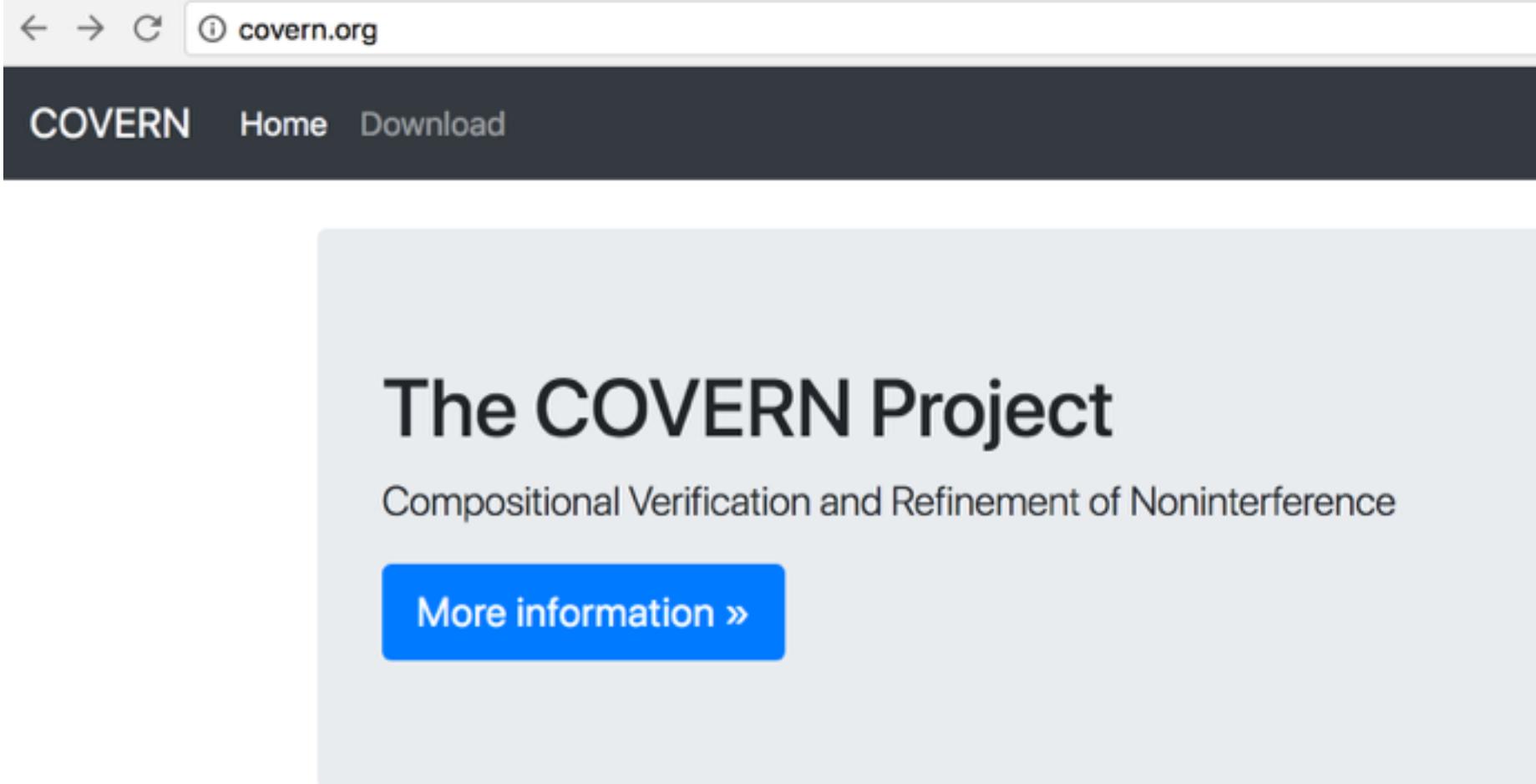


Toby Murray

University of Melbourne &
Data61 (formerly NICTA), CSIRO



<http://covern.org>



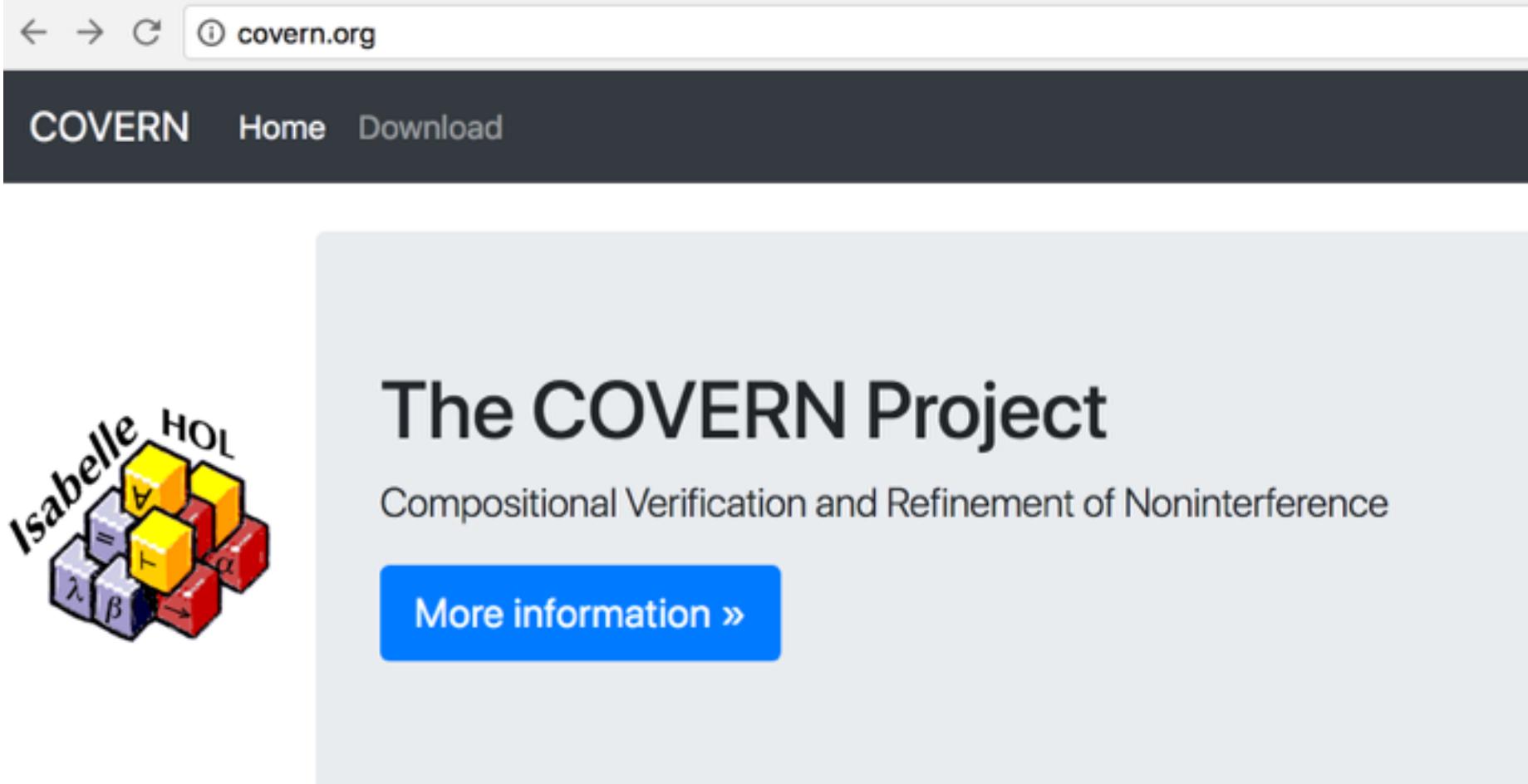
The screenshot shows a web browser window with the URL "covern.org" in the address bar. The page has a dark header bar with the text "COVERN" and "Home Download". The main content area features a large title "The COVERN Project" in bold black font, followed by the subtitle "Compositional Verification and Refinement of Noninterference". Below the subtitle is a blue button with the text "More information »".

The COVERN Project

Compositional Verification and Refinement of Noninterference

More information »

<http://covern.org>



The screenshot shows a web browser window with the URL "covern.org" in the address bar. The page has a dark header with the word "COVERN" and navigation links for "Home" and "Download". To the left, there is a logo for Isabelle HOL, featuring a 3D cube composed of smaller colored cubes (yellow, purple, red) with mathematical symbols like λ , β , $=$, \vdash , and α on them. The main content area has a light gray background. It features a large title "The COVERN Project" in bold black font, followed by a subtitle "Compositional Verification and Refinement of Noninterference". Below the subtitle is a blue button with white text that says "More information »".

The COVERN Project

Compositional Verification and Refinement of Noninterference

More information »

Confidentiality (Information Flow) Proofs

Confidentiality (Information Flow) Proofs



Security. Performance. Proof.



Confidentiality (Information Flow) Proofs



CoCon



Confidentiality (Information Flow) Proofs



CoCon

CoSMed



Confidentiality (Information Flow) Proofs



CoCon

CoSMed



SAFE



Confidentiality (Information Flow) Proofs



CoCon

CoSMed



SAFE



Quark



Confidentiality (Information Flow) Proofs



CoCon

CoSMed



CERTIKOS



SAFE



Quark



The Cross Domain Desktop Compositor



Australian Government

Department of Defence

Defence Science and Technology Group





Mark Beaumont



The Cross Domain Desktop Compositor



Australian Government

Department of Defence

Defence Science and Technology Group

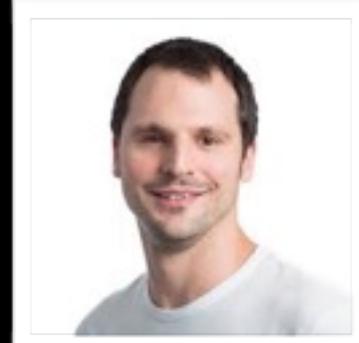




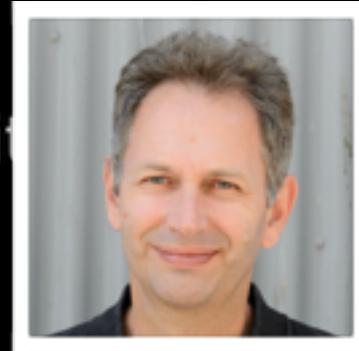
Mark Beaumont



The Cross Domain Desktop Composite



Toby Murray



Kevin Elphinstone



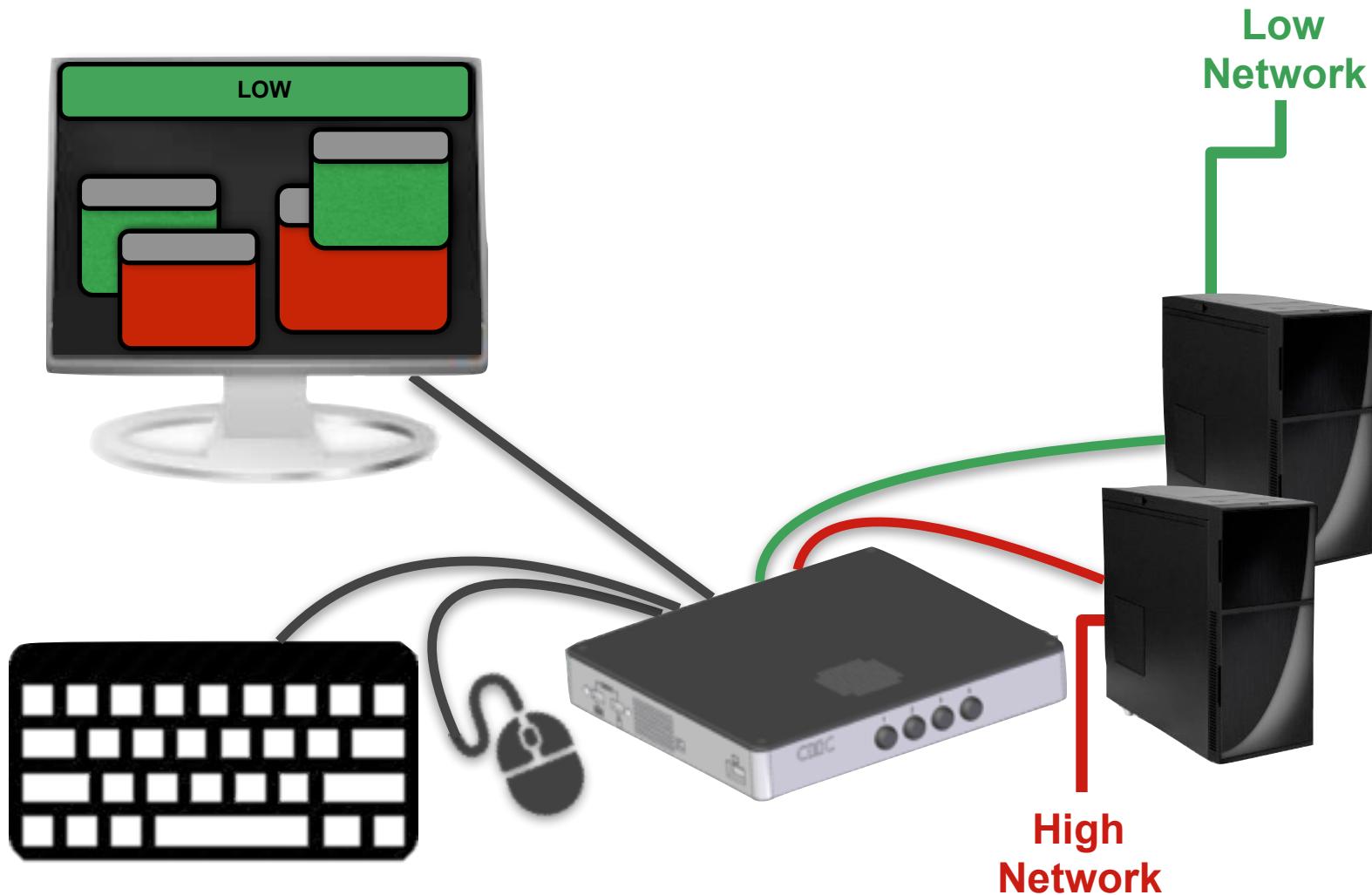
Australian Government

Department of Defence

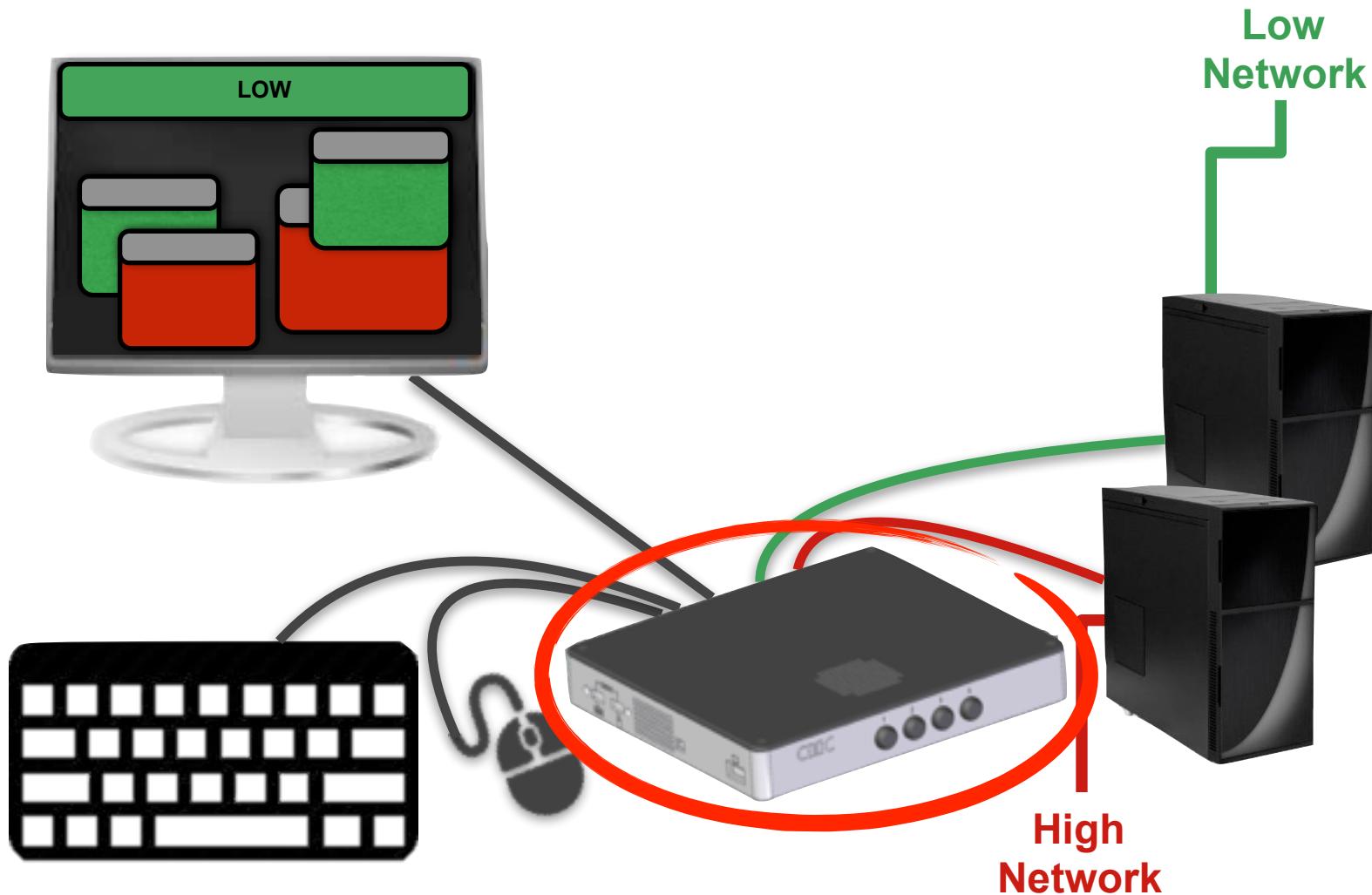
Defence Science and Technology Group



Cross Domain Desktop Compositor



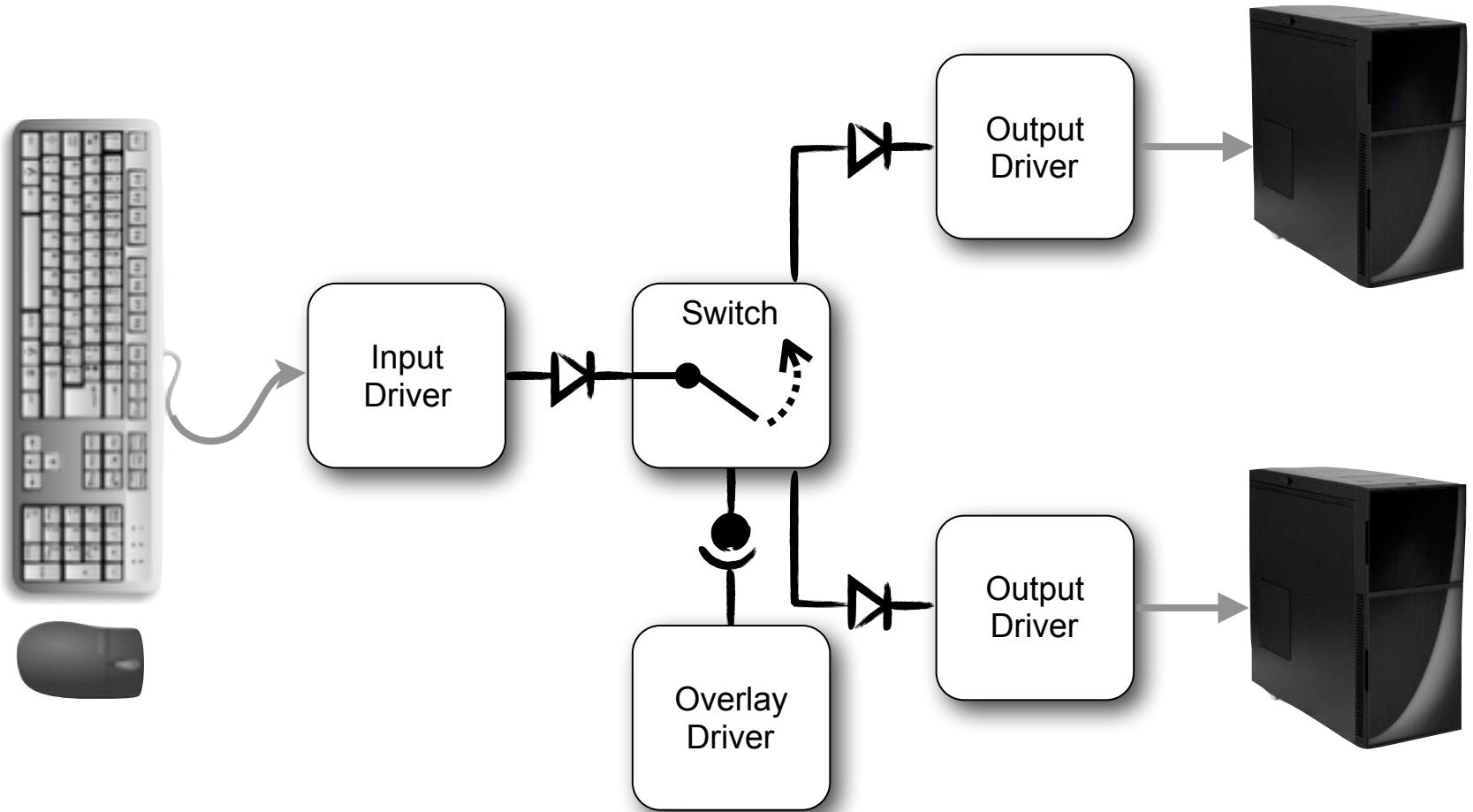
Cross Domain Desktop Compositor



CDDC

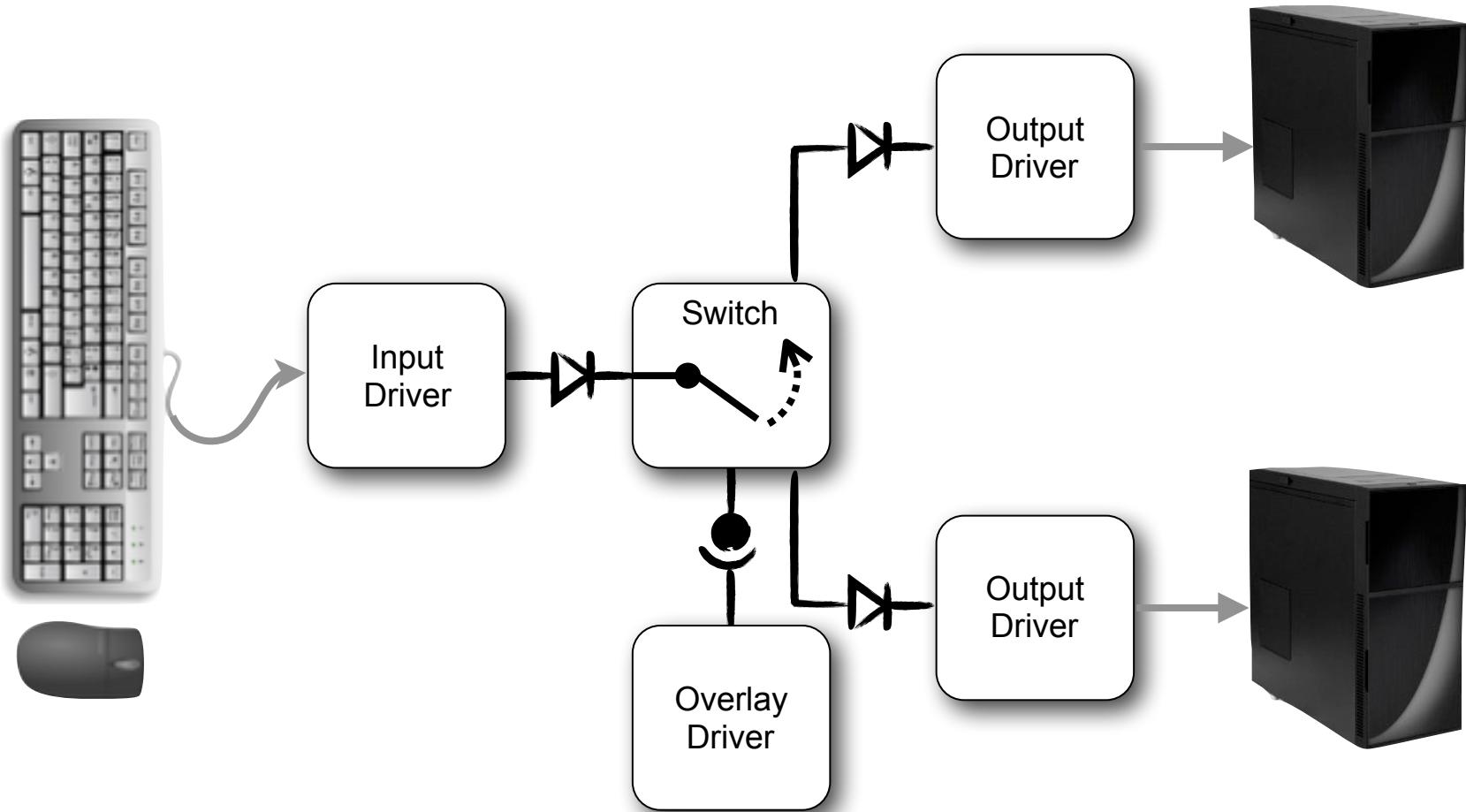


seL4-Based Software Architecture



seL4-Based Software Architecture

(ignoring device administration and configuration,
plus keyboard LED control)



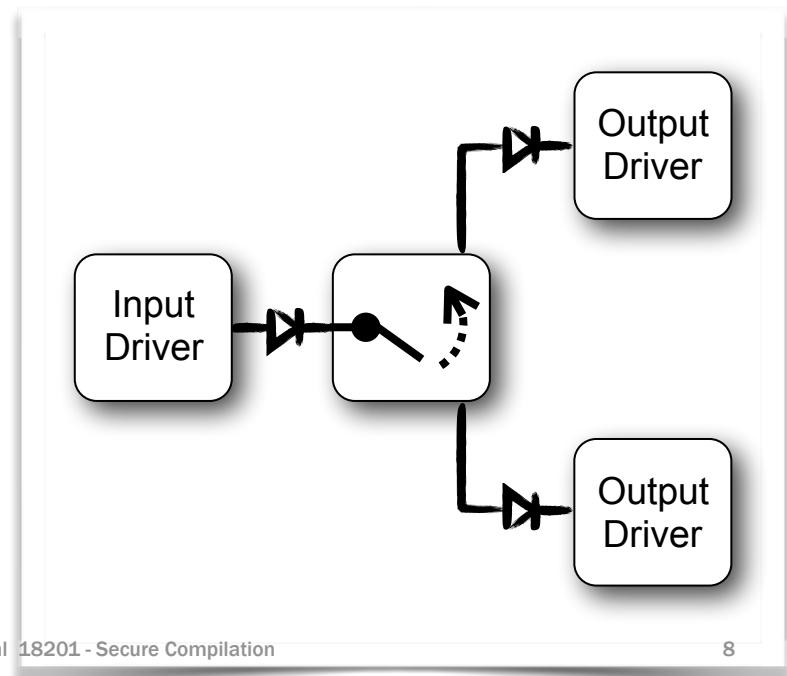
Verification Framework: Requirements

Verification Framework: Requirements

Compositional Security Property

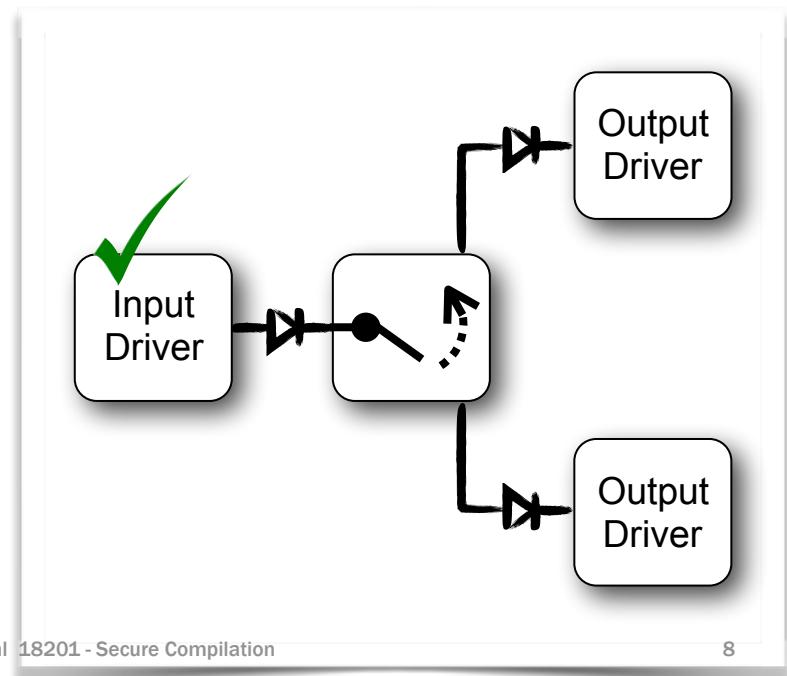
Verification Framework: Requirements

Compositional Security Property



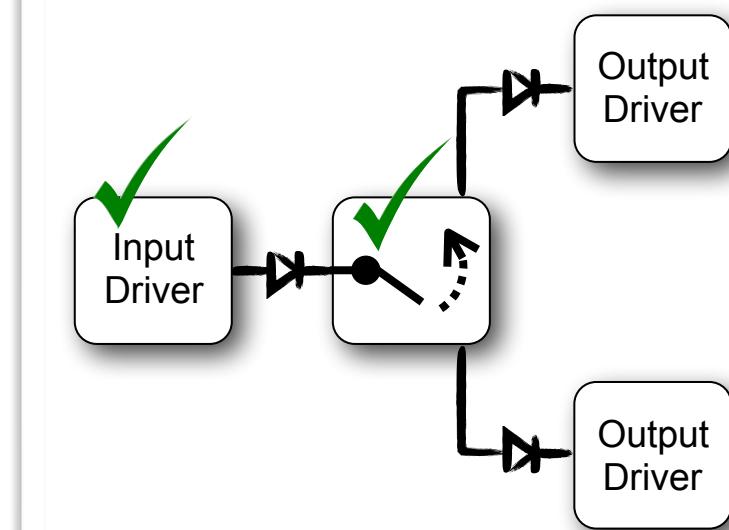
Verification Framework: Requirements

Compositional Security Property



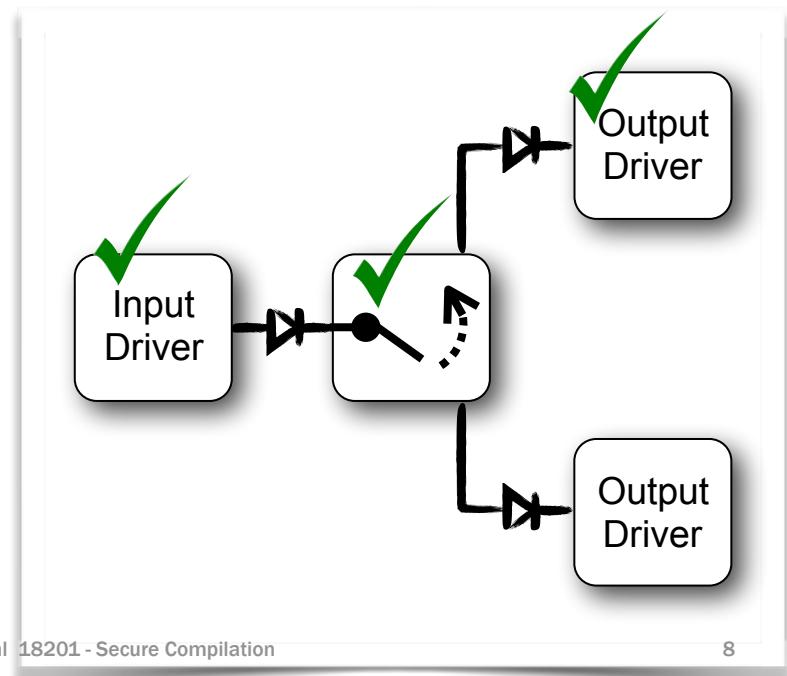
Verification Framework: Requirements

Compositional Security Property



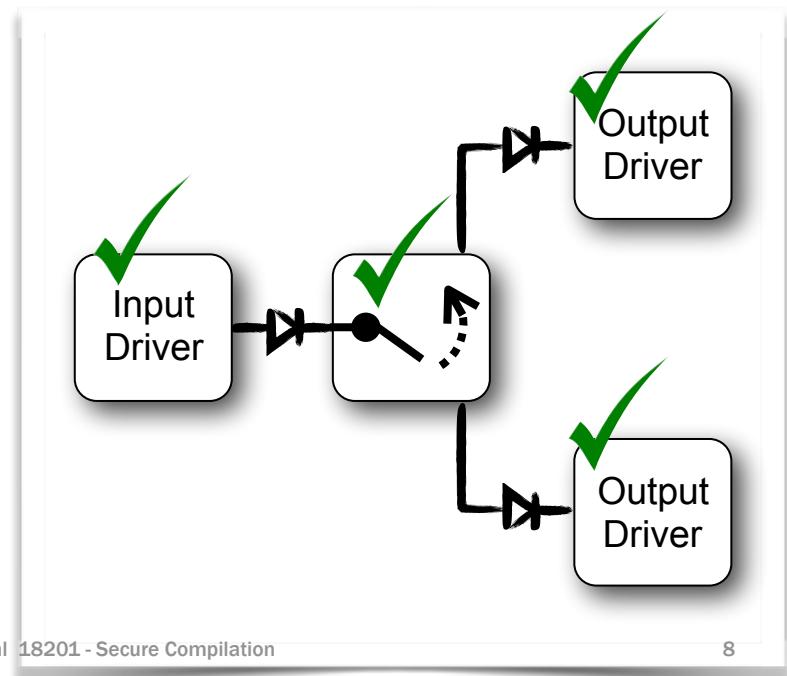
Verification Framework: Requirements

Compositional Security Property



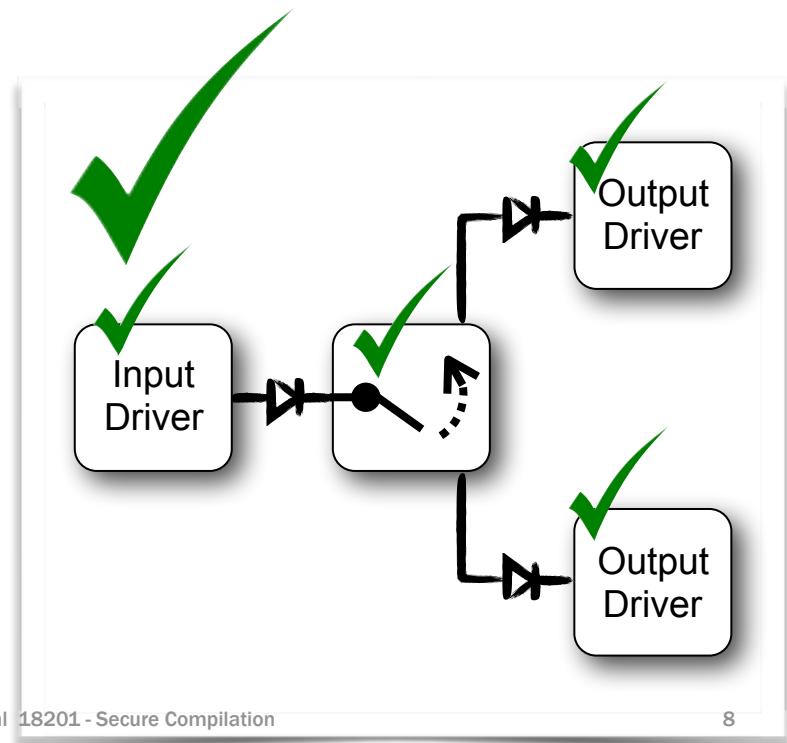
Verification Framework: Requirements

Compositional Security Property



Verification Framework: Requirements

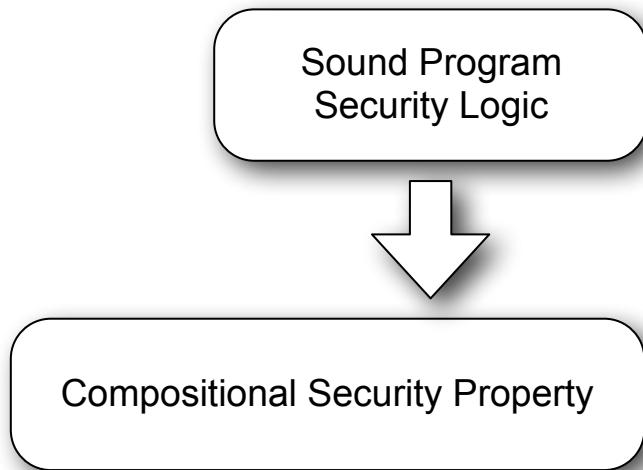
Compositional Security Property



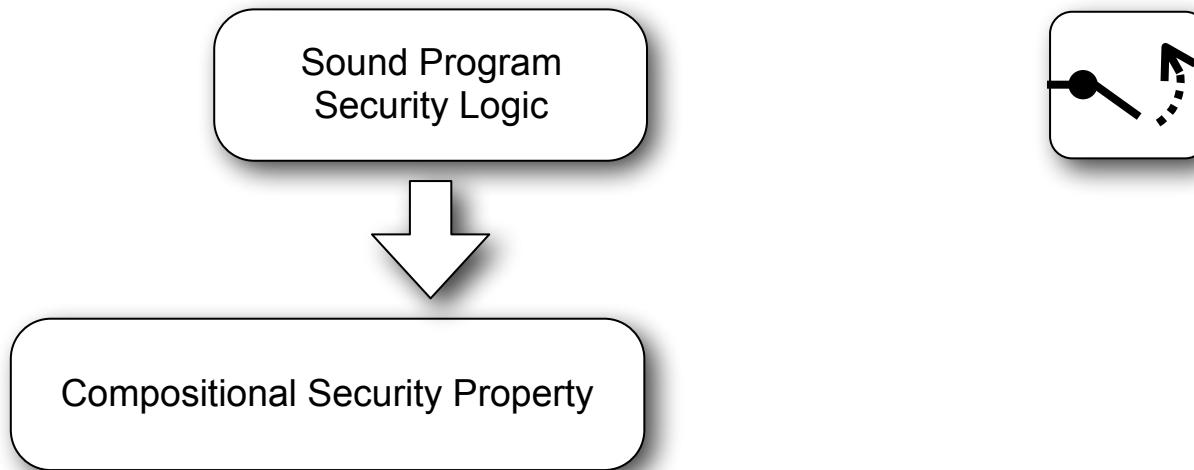
Verification Framework: Requirements

Compositional Security Property

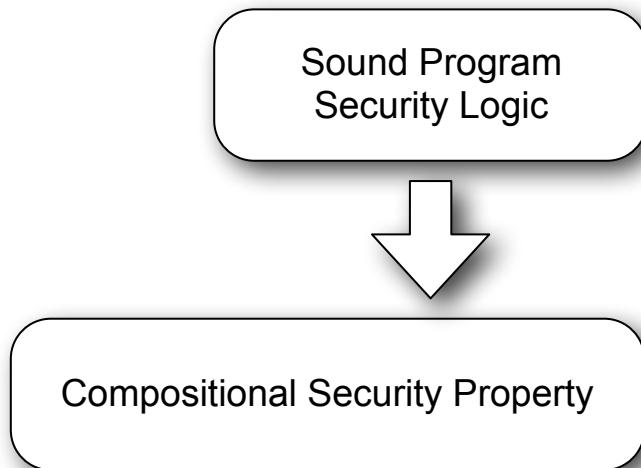
Verification Framework: Requirements



Verification Framework: Requirements

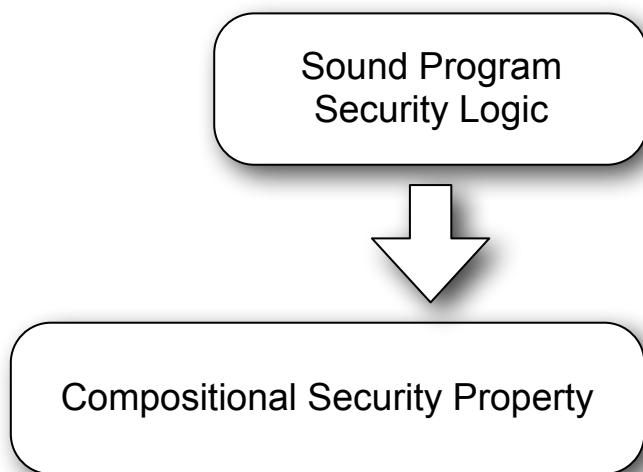


Verification Framework: Requirements



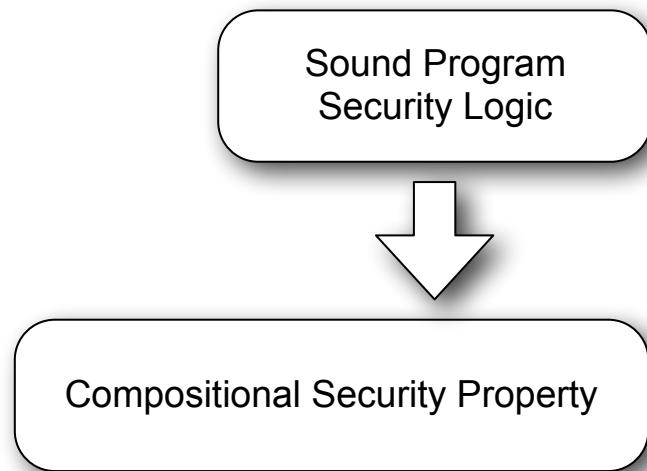
```
skip /* control +=_m AsmNoW */;
skip /* temp +=_m AsmNoRW */;
temp := buffer;
if control == 0 then
    low-var := temp
else
    high-var := temp
endif;
temp := 0;
skip /* temp -=_m AsmNoRW */;
```

Verification Framework: Requirements

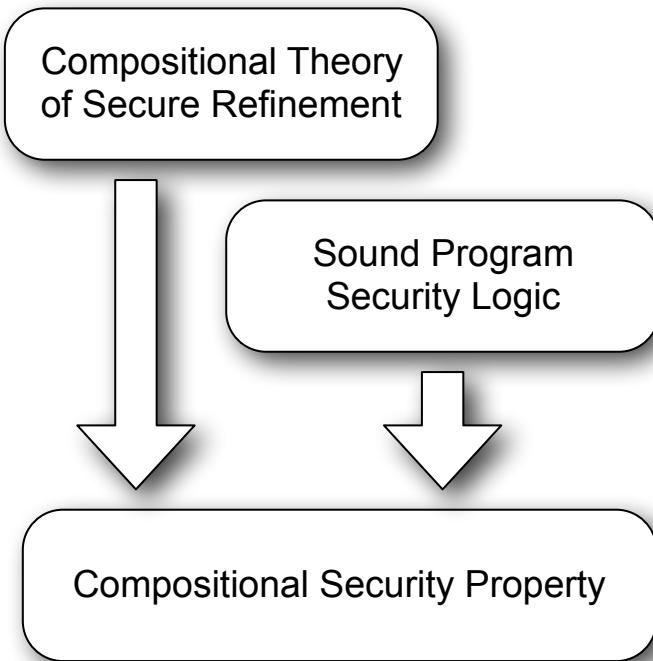


skip /* control $+=_m$ AsmNoW */;
skip /* temp $+=_m$ AsmNoRW */;
temp := buffer;
if control == 0 then
 low-var := temp
else
 high-var := temp
endif;
temp := 0;
skip /* temp $-=_m$ AsmNoRW */

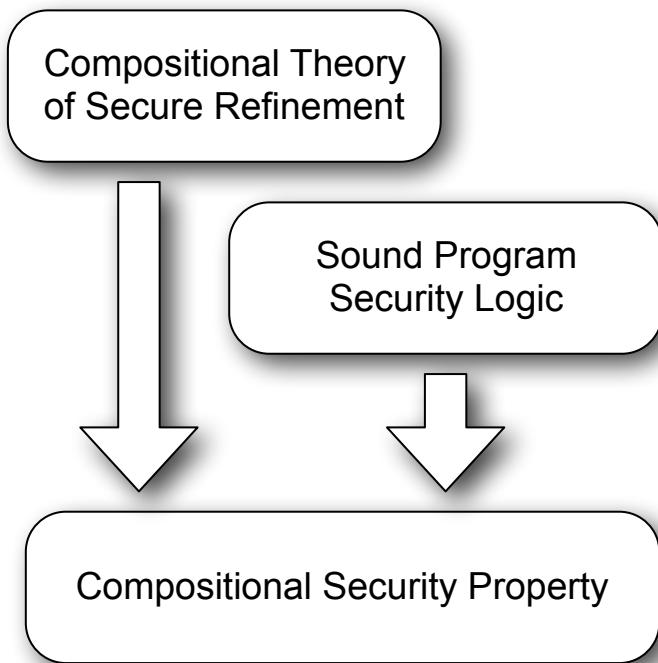
Verification Framework: Requirements



Verification Framework: Requirements

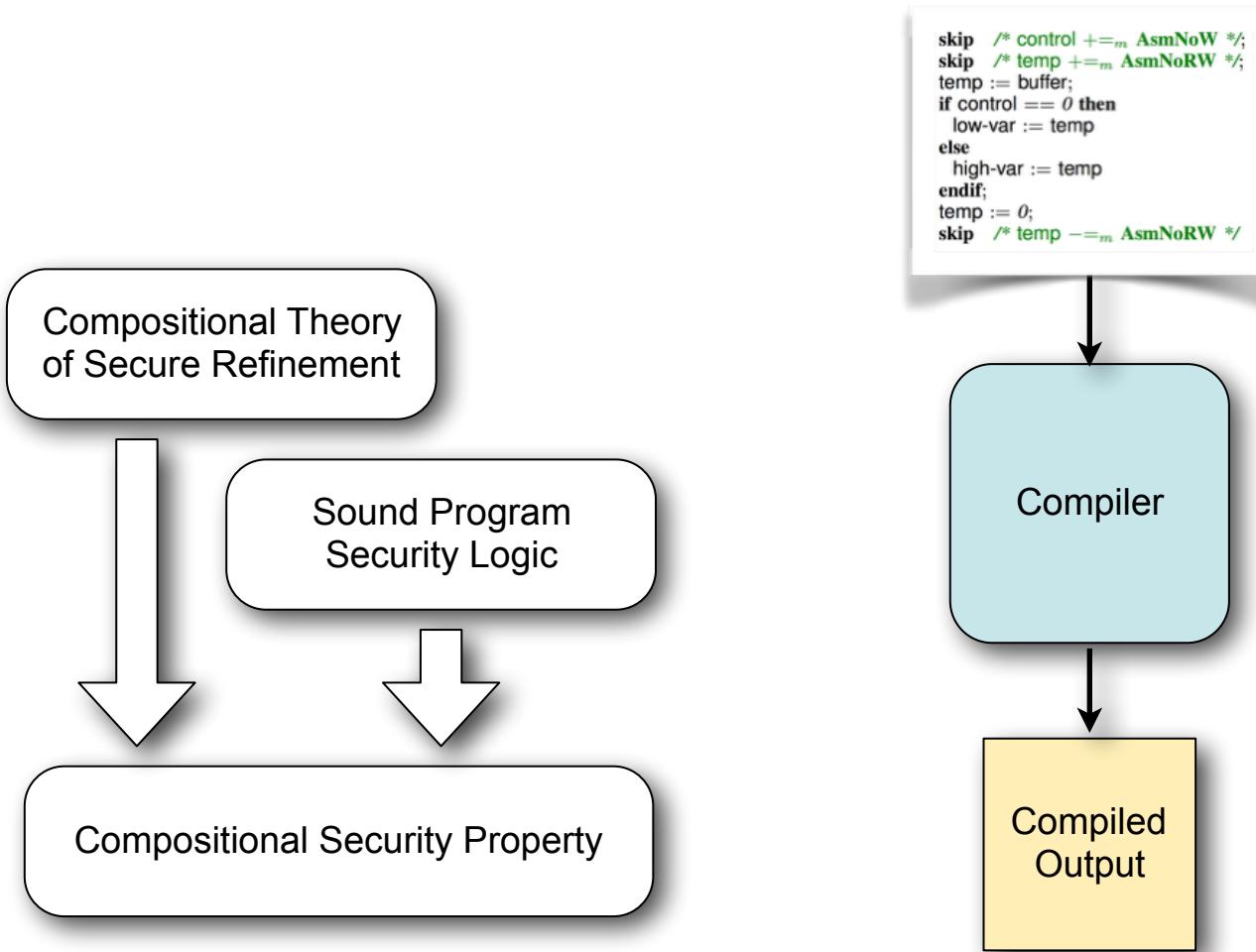


Verification Framework: Requirements

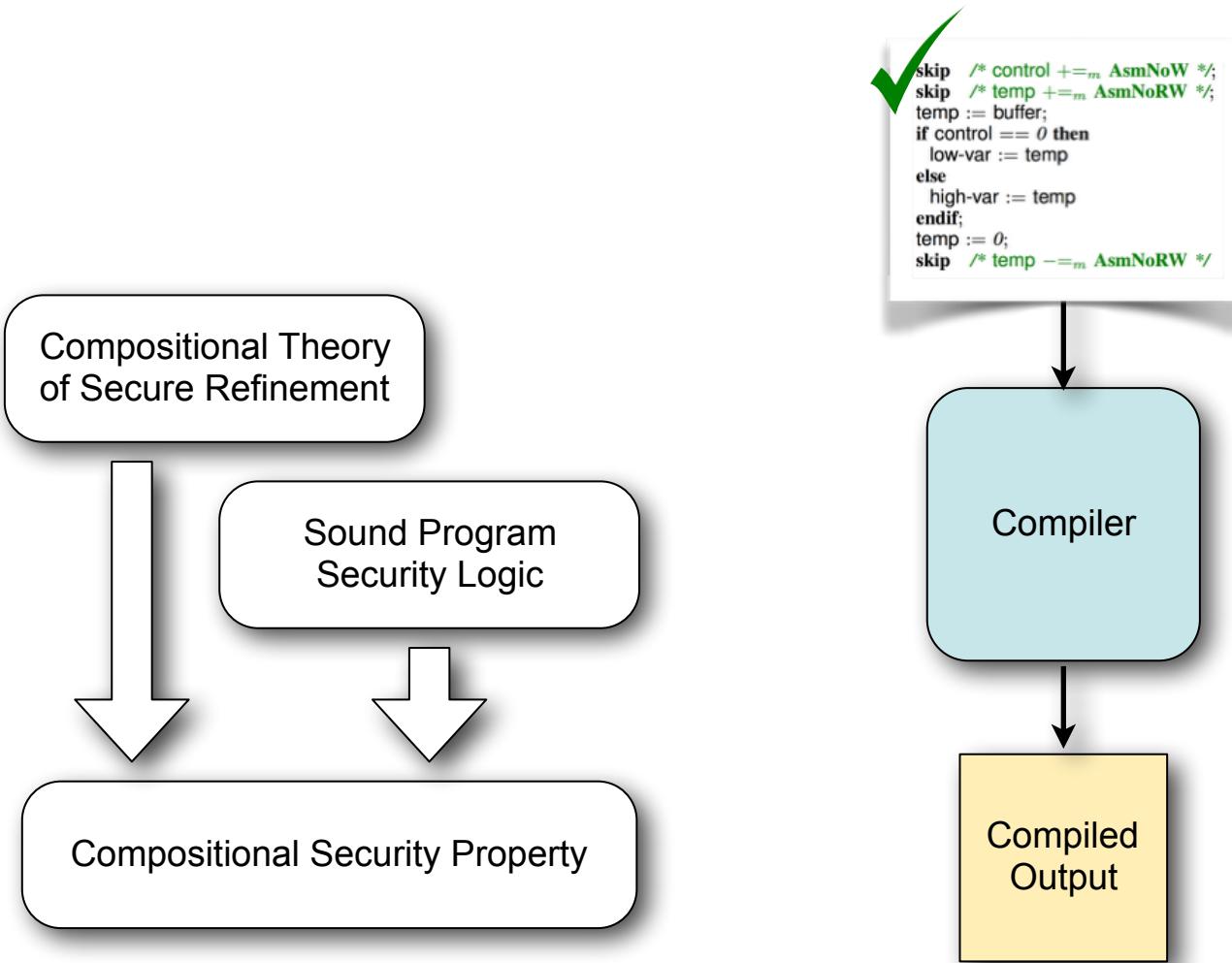


```
skip /* control +=_m AsmNoW */;  
skip /* temp +=_m AsmNoRW */;  
temp := buffer;  
if control == 0 then  
    low-var := temp  
else  
    high-var := temp  
endif;  
temp := 0;  
skip /* temp -=_m AsmNoRW */;
```

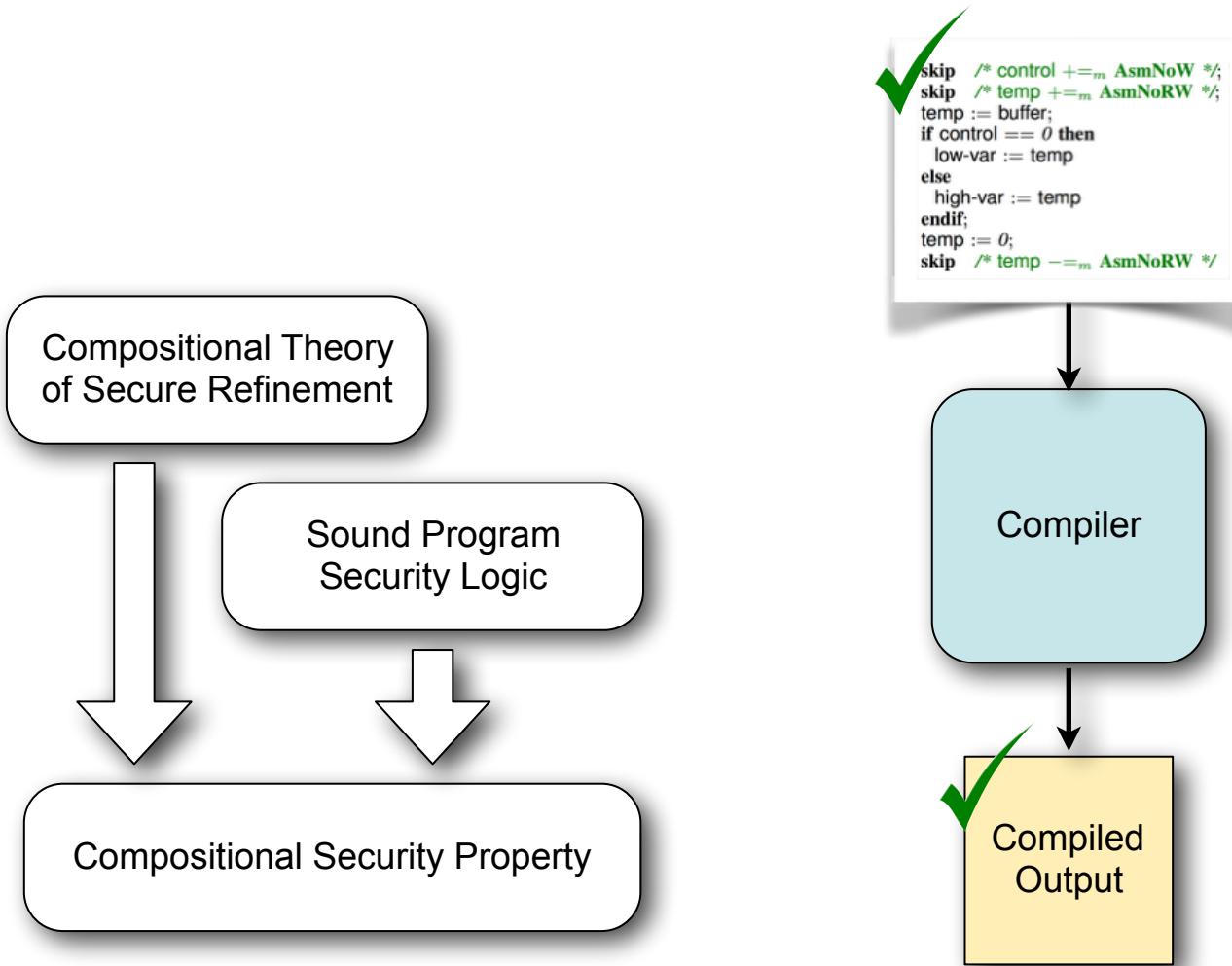
Verification Framework: Requirements



Verification Framework: Requirements

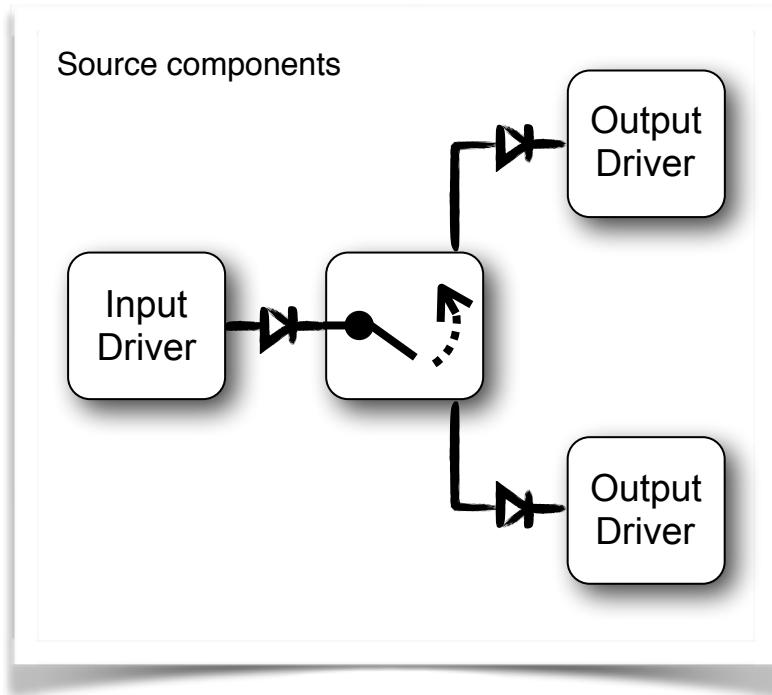


Verification Framework: Requirements

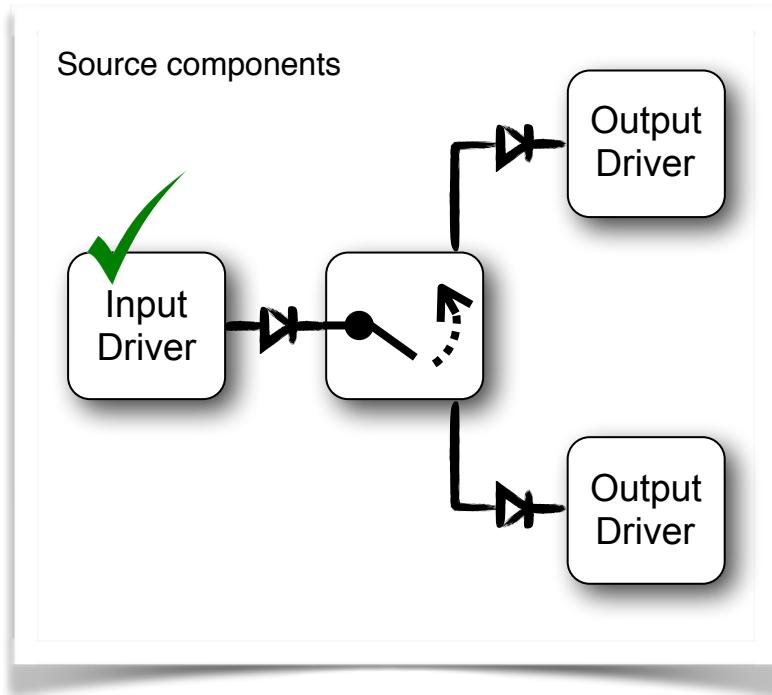


Verification Framework: Operation

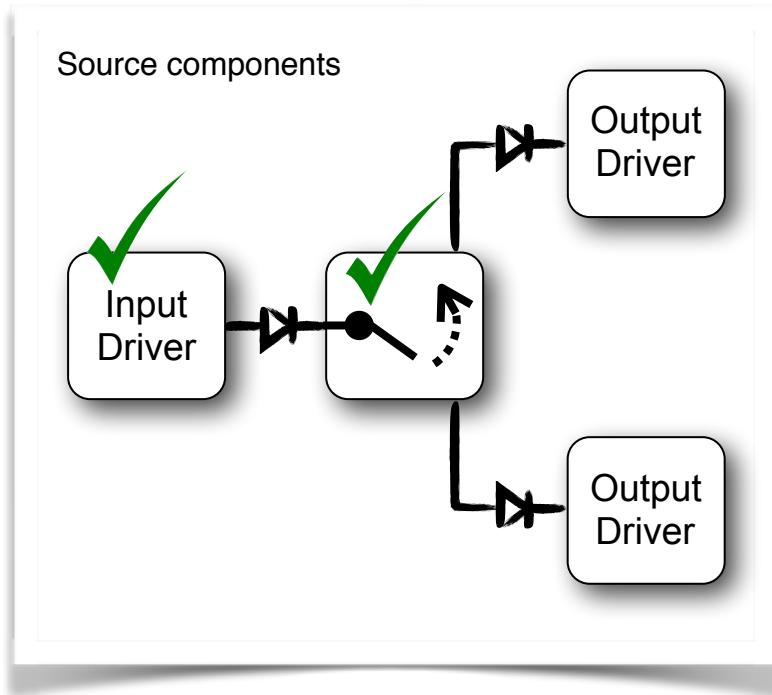
Verification Framework: Operation



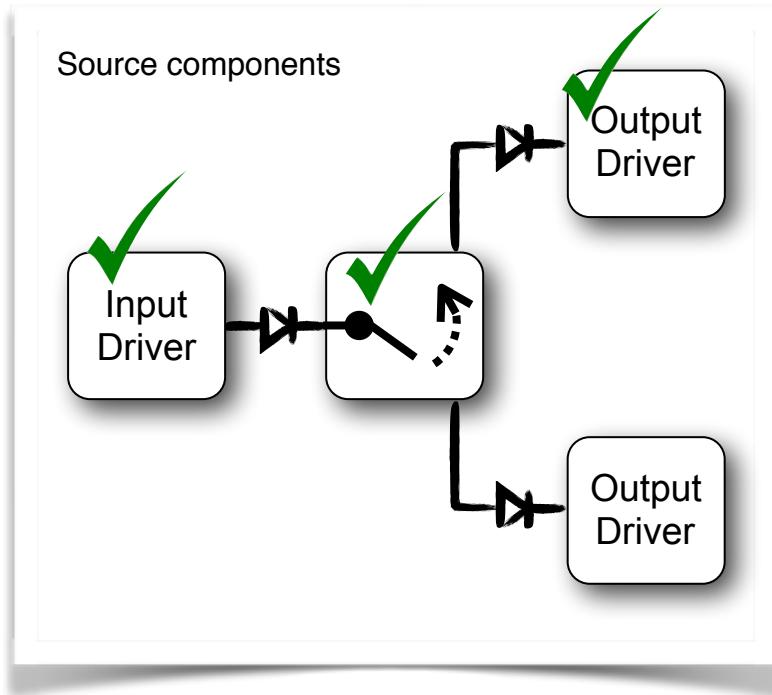
Verification Framework: Operation



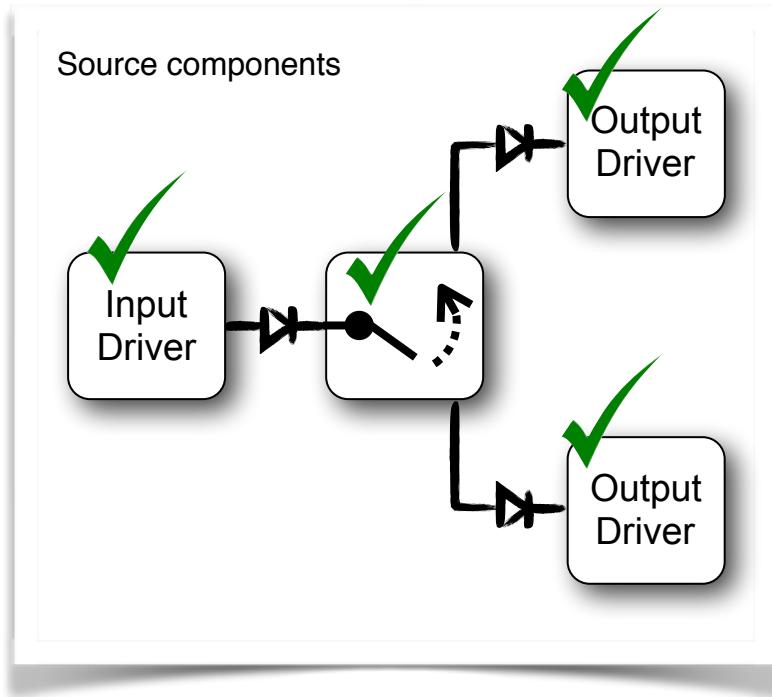
Verification Framework: Operation



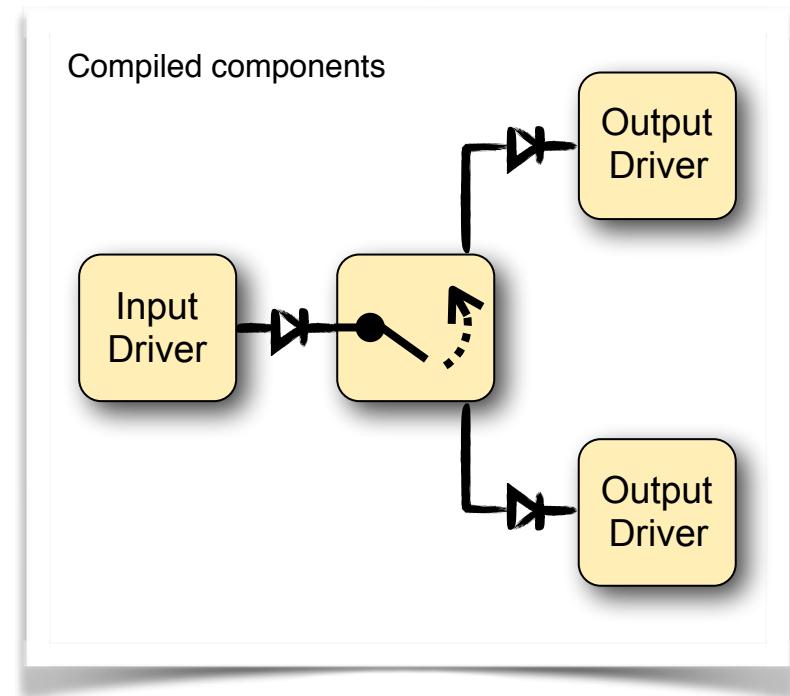
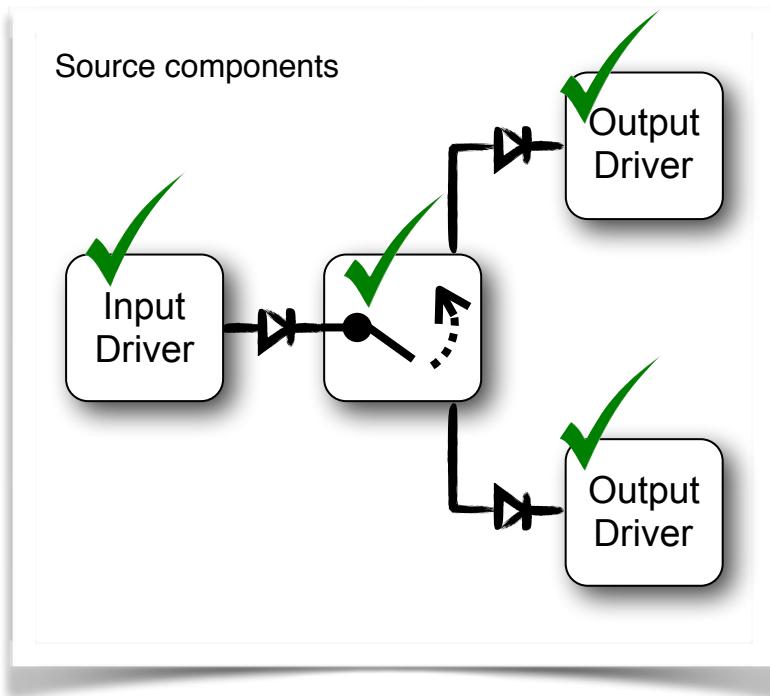
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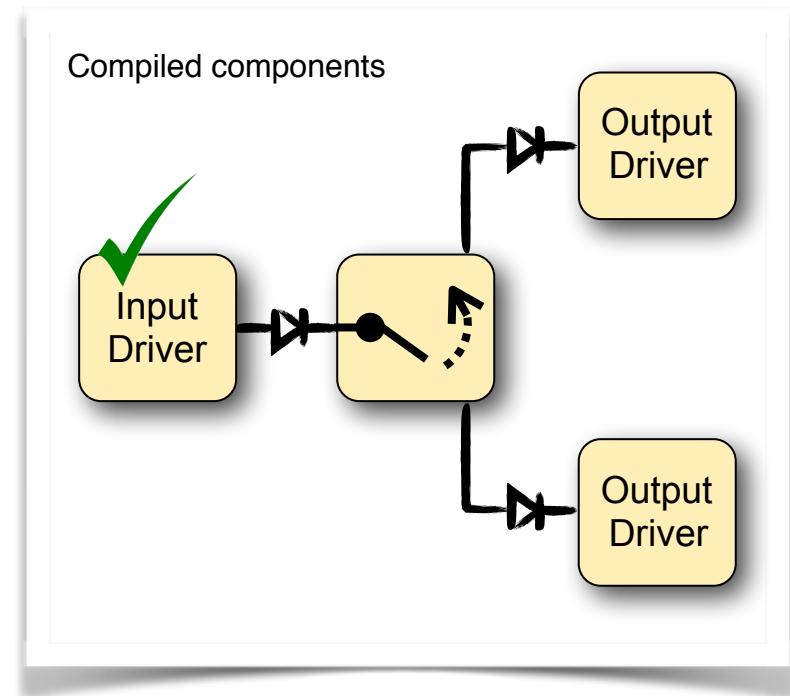
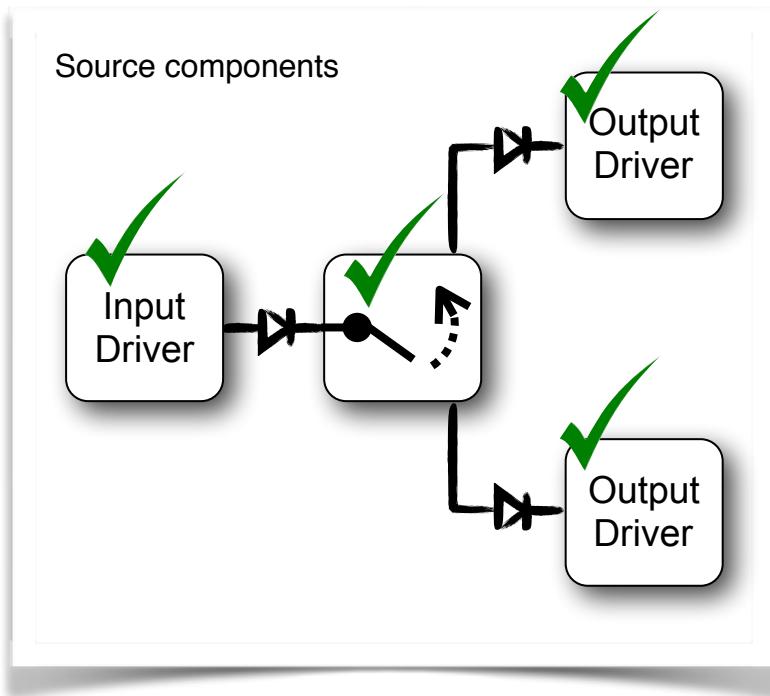
Verification Framework: Operation



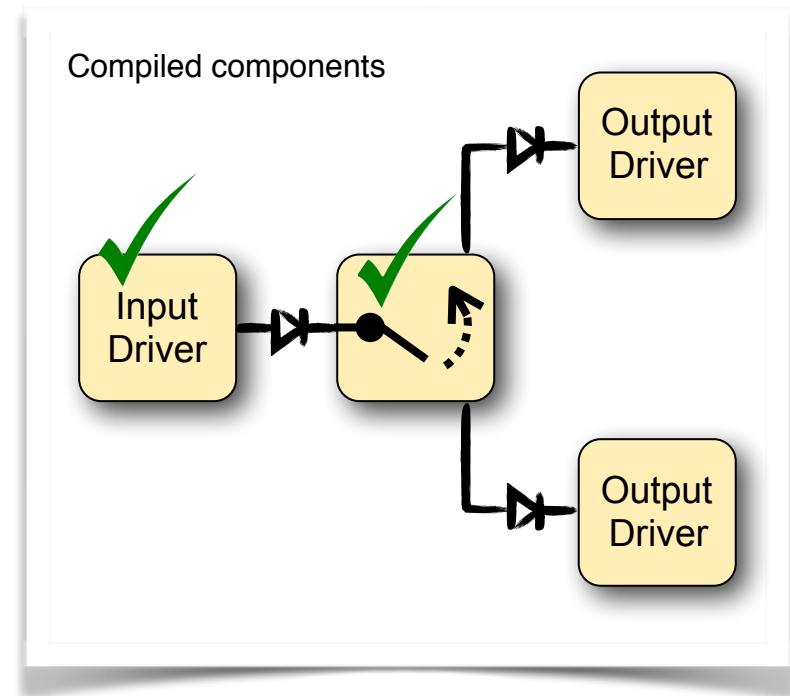
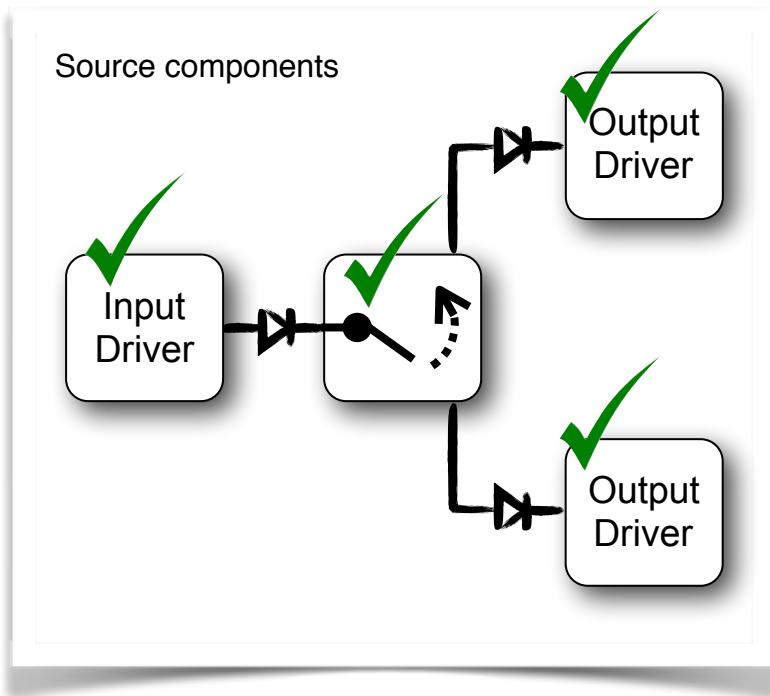
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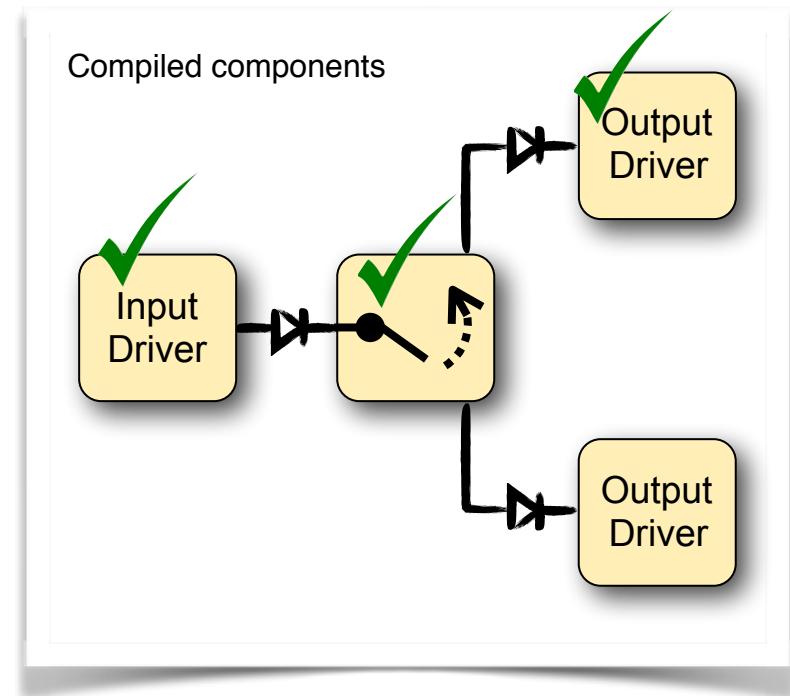
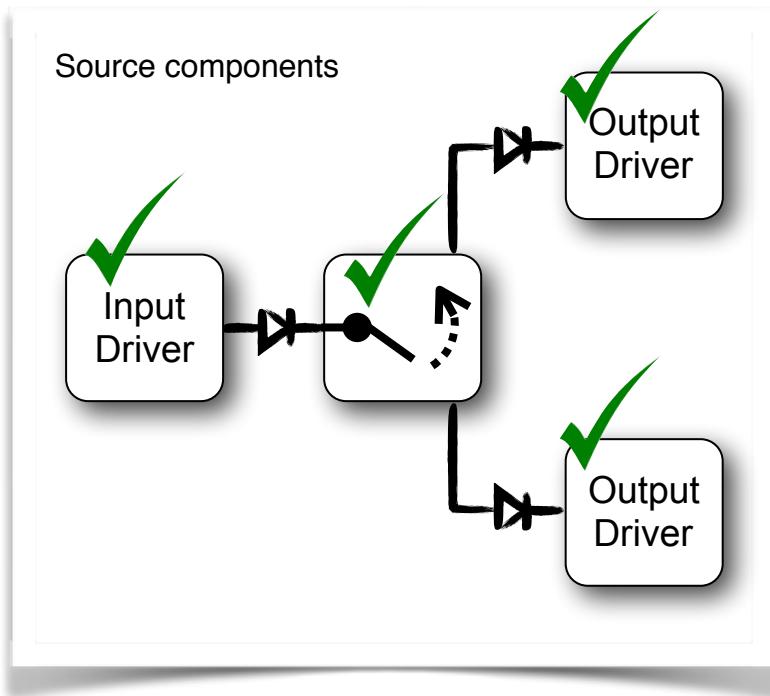
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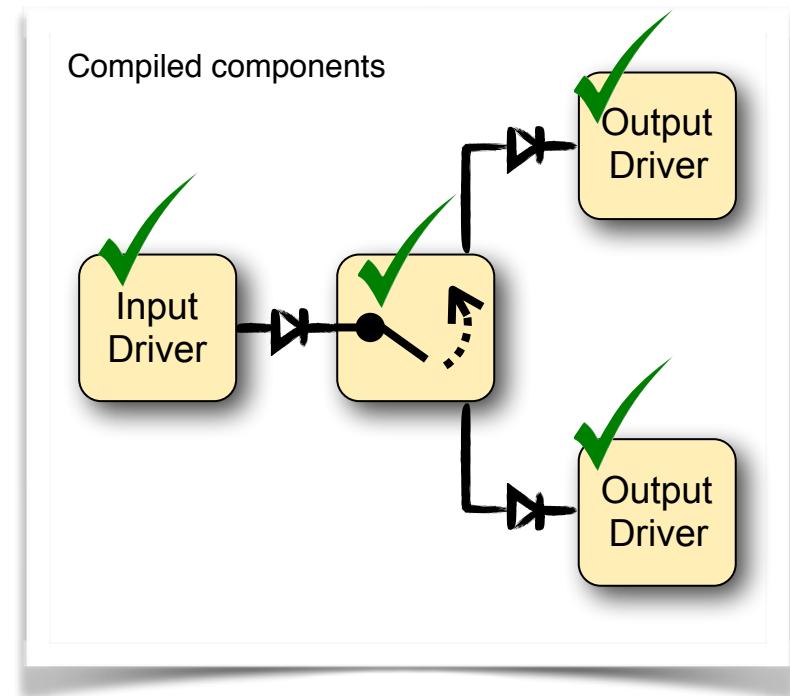
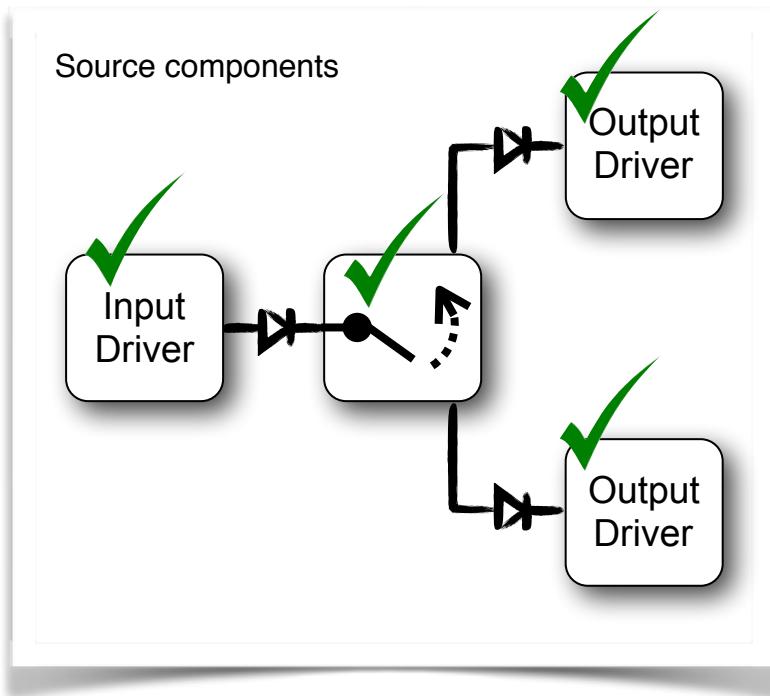
Verification Framework: Operation



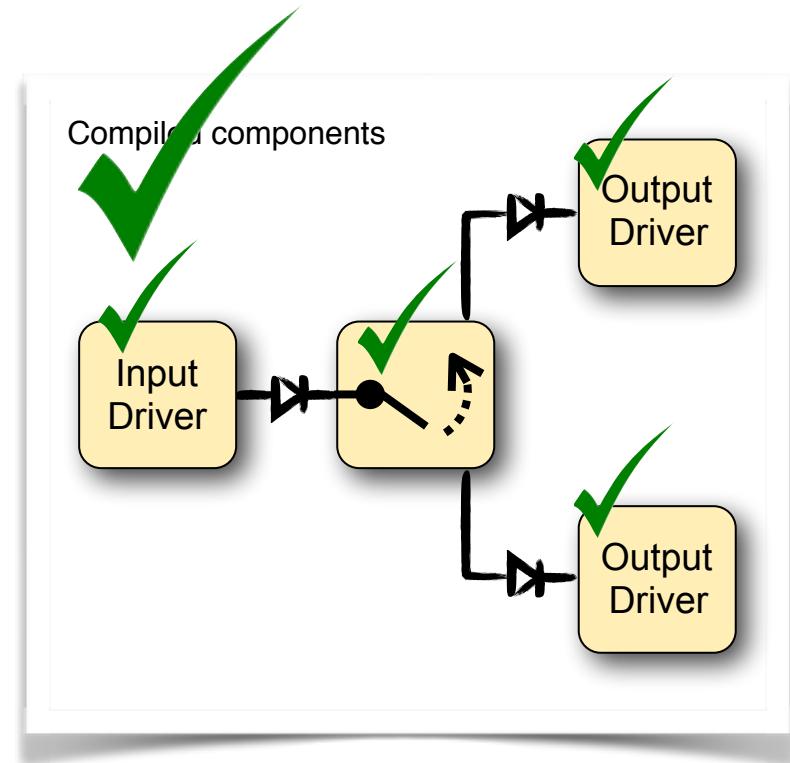
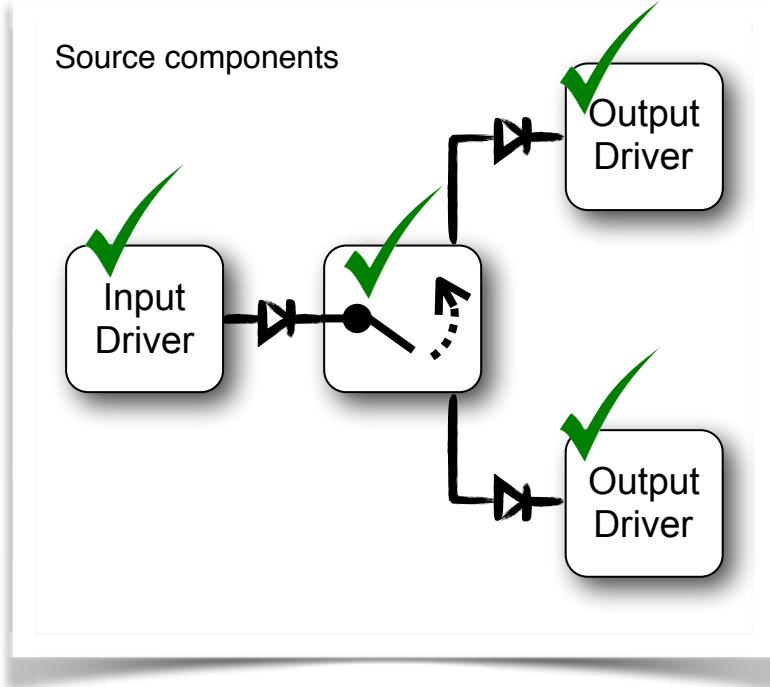
Verification Framework: Operation



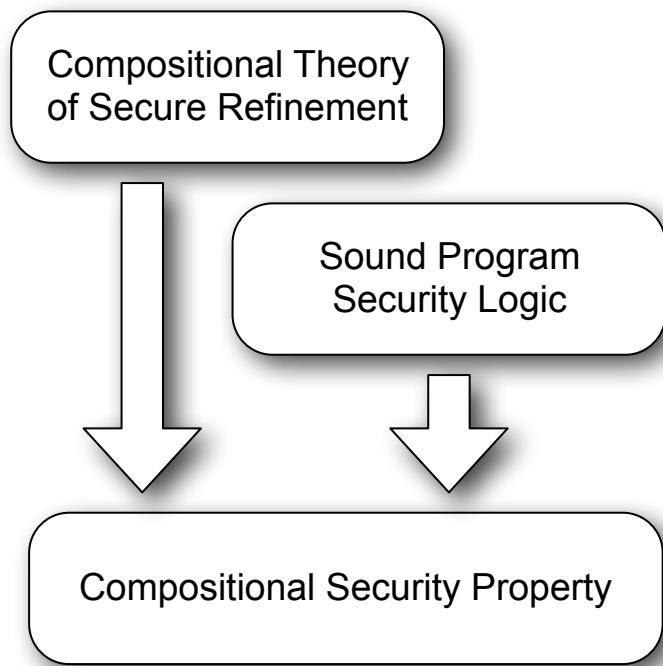
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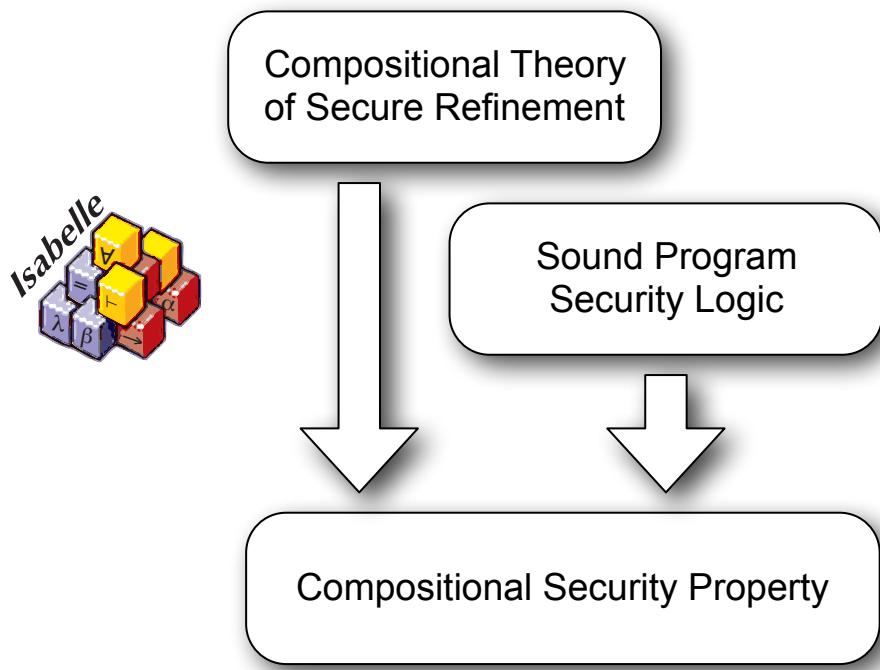
Verification Framework: Operation



Verification Framework: Status

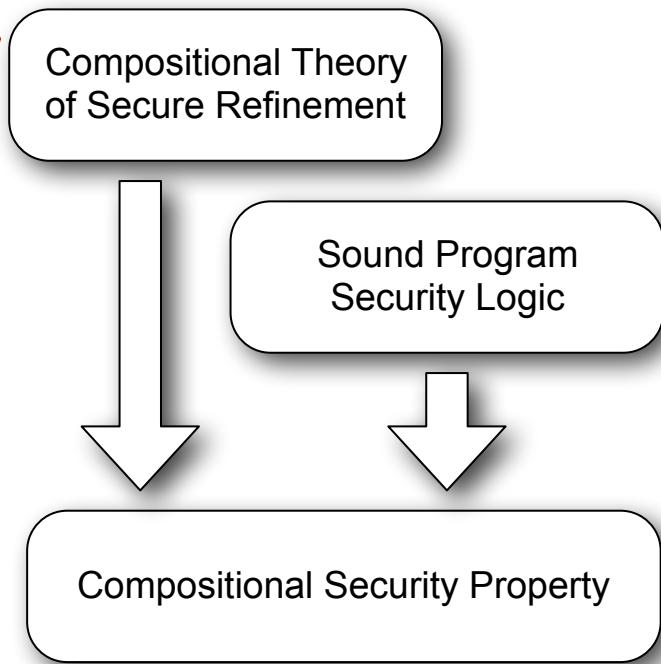
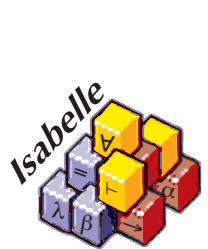


Verification Framework: Status

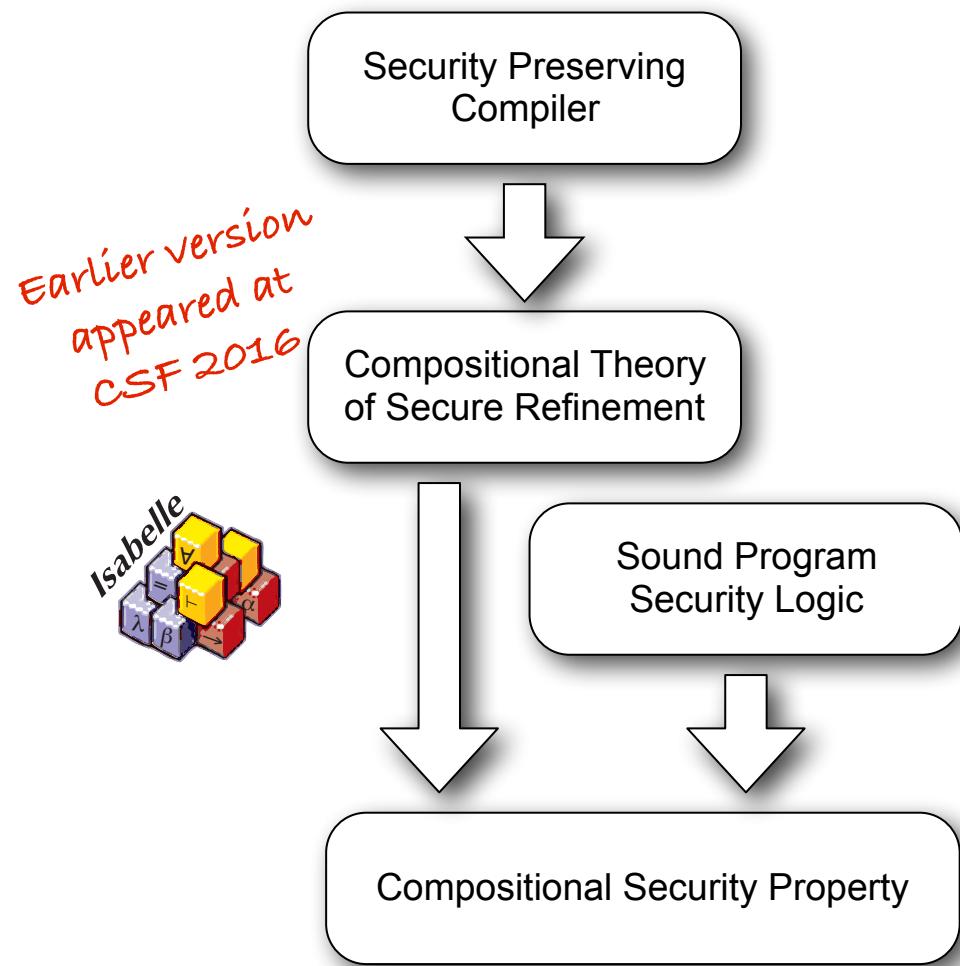


Verification Framework: Status

Earlier version
appeared at
CSF 2016



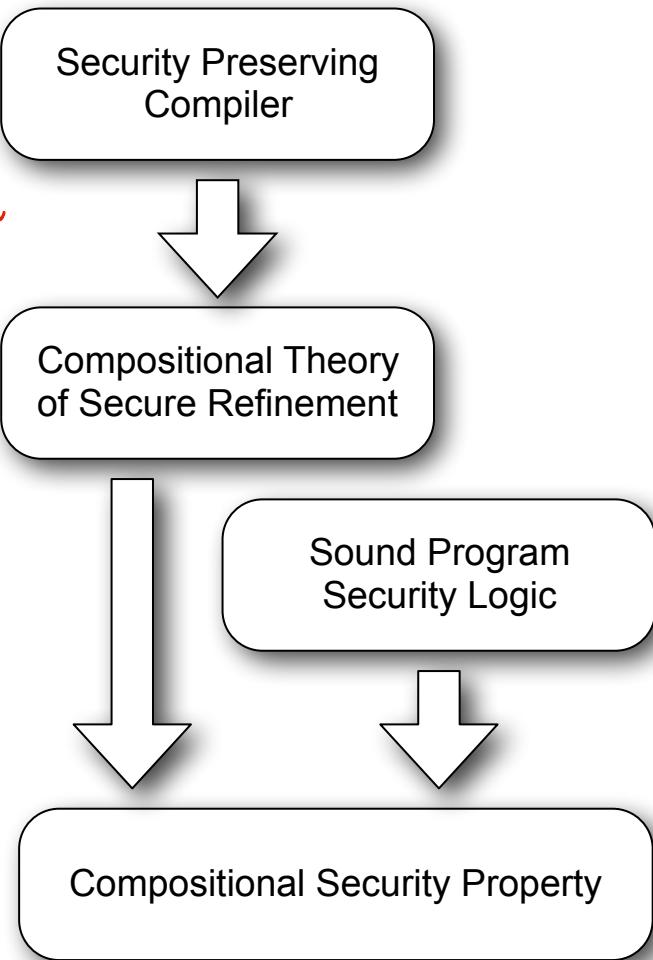
Verification Framework: Status



Verification Framework: Status



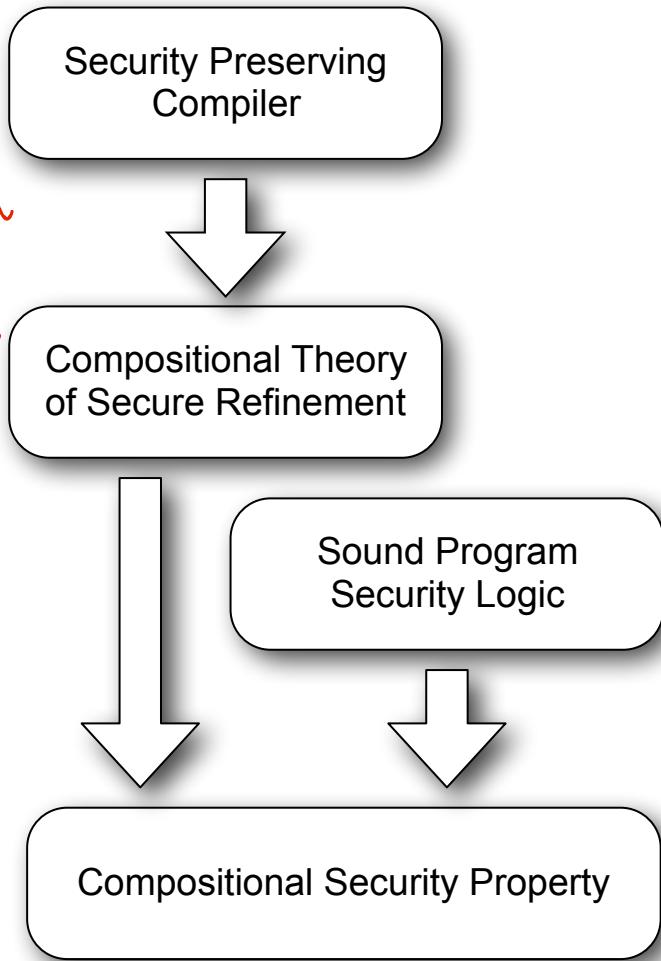
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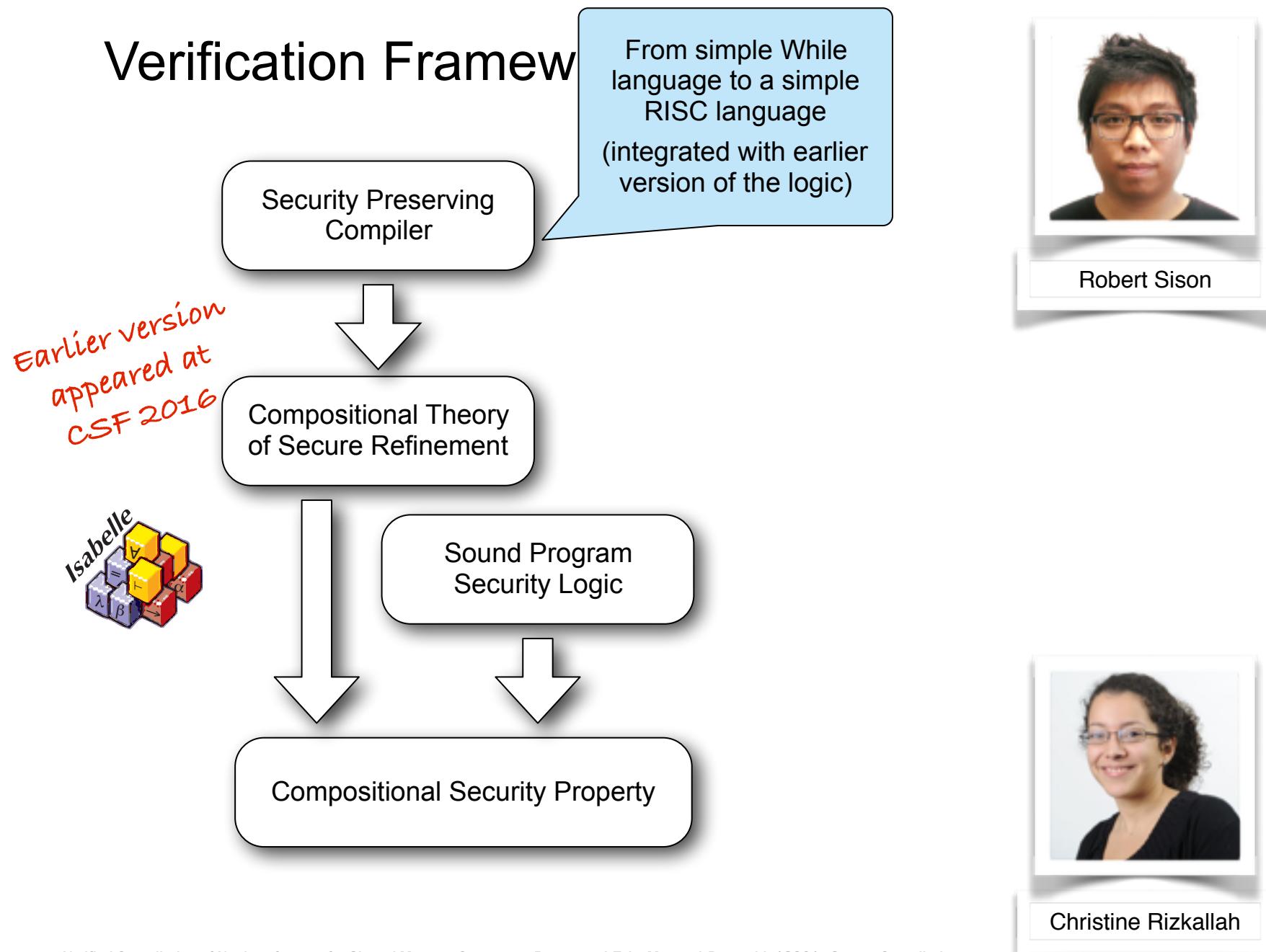
Verification Framework: Status



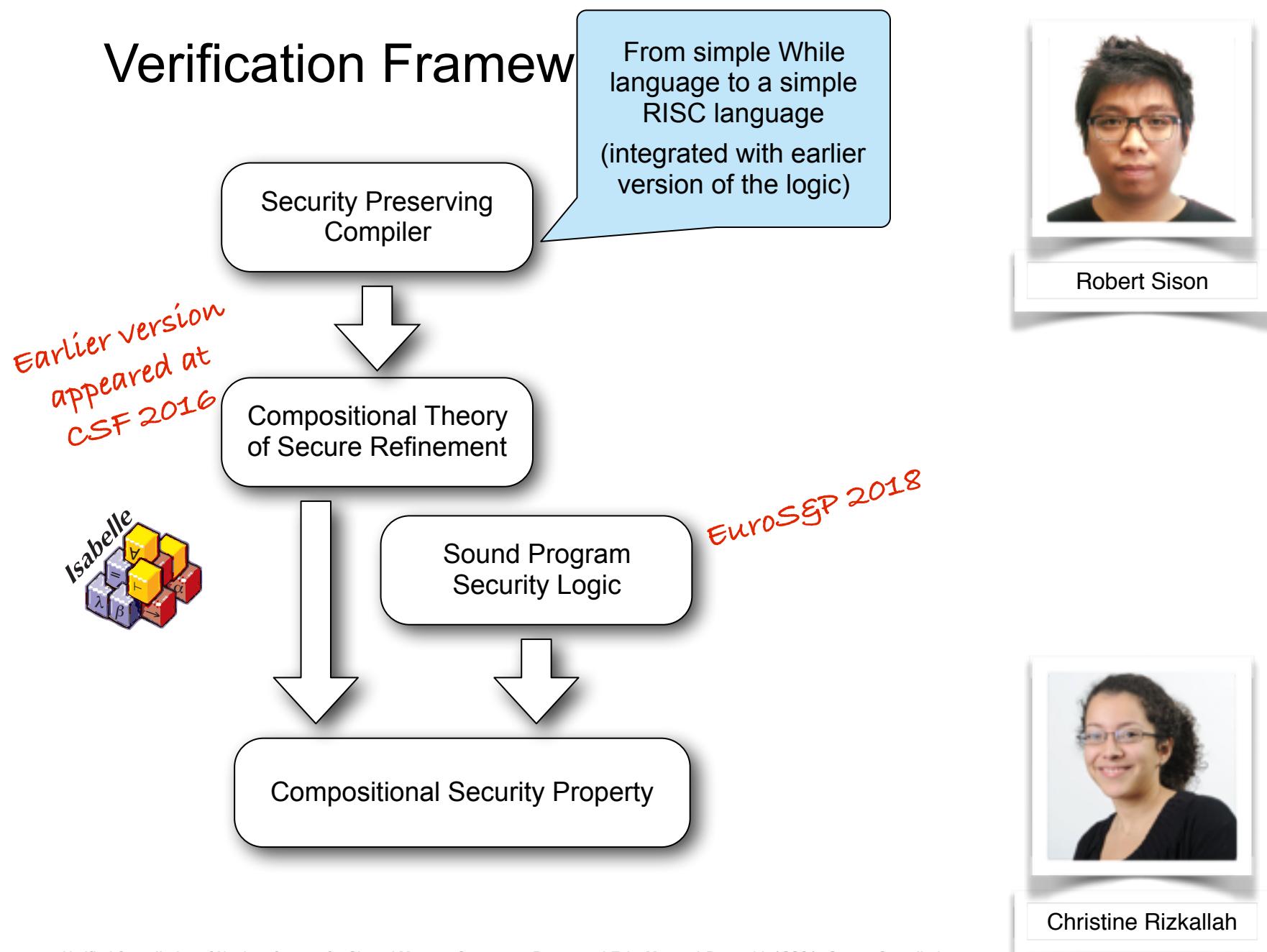
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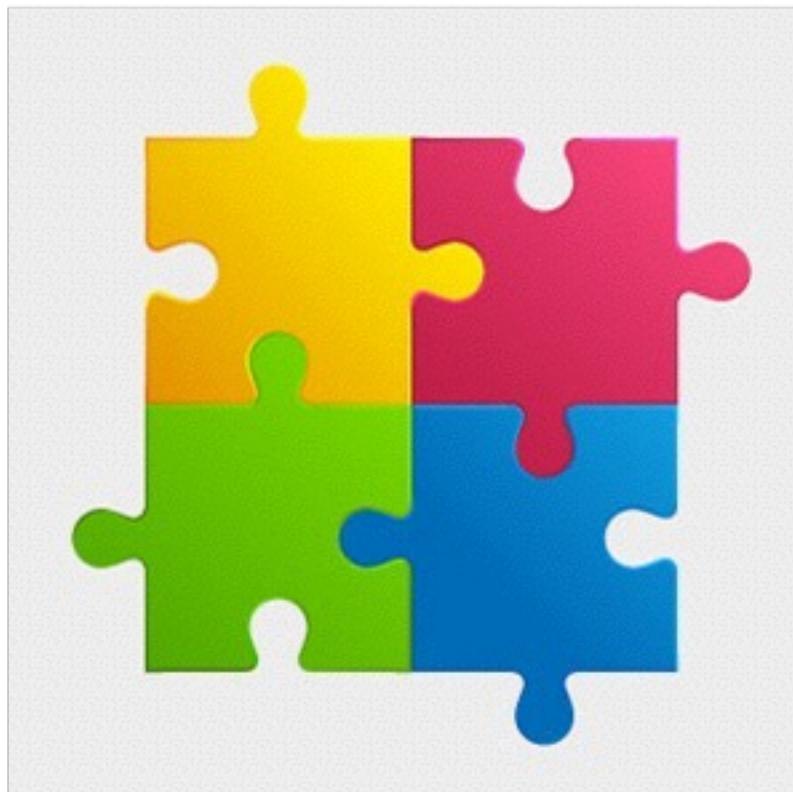
Verification Framework



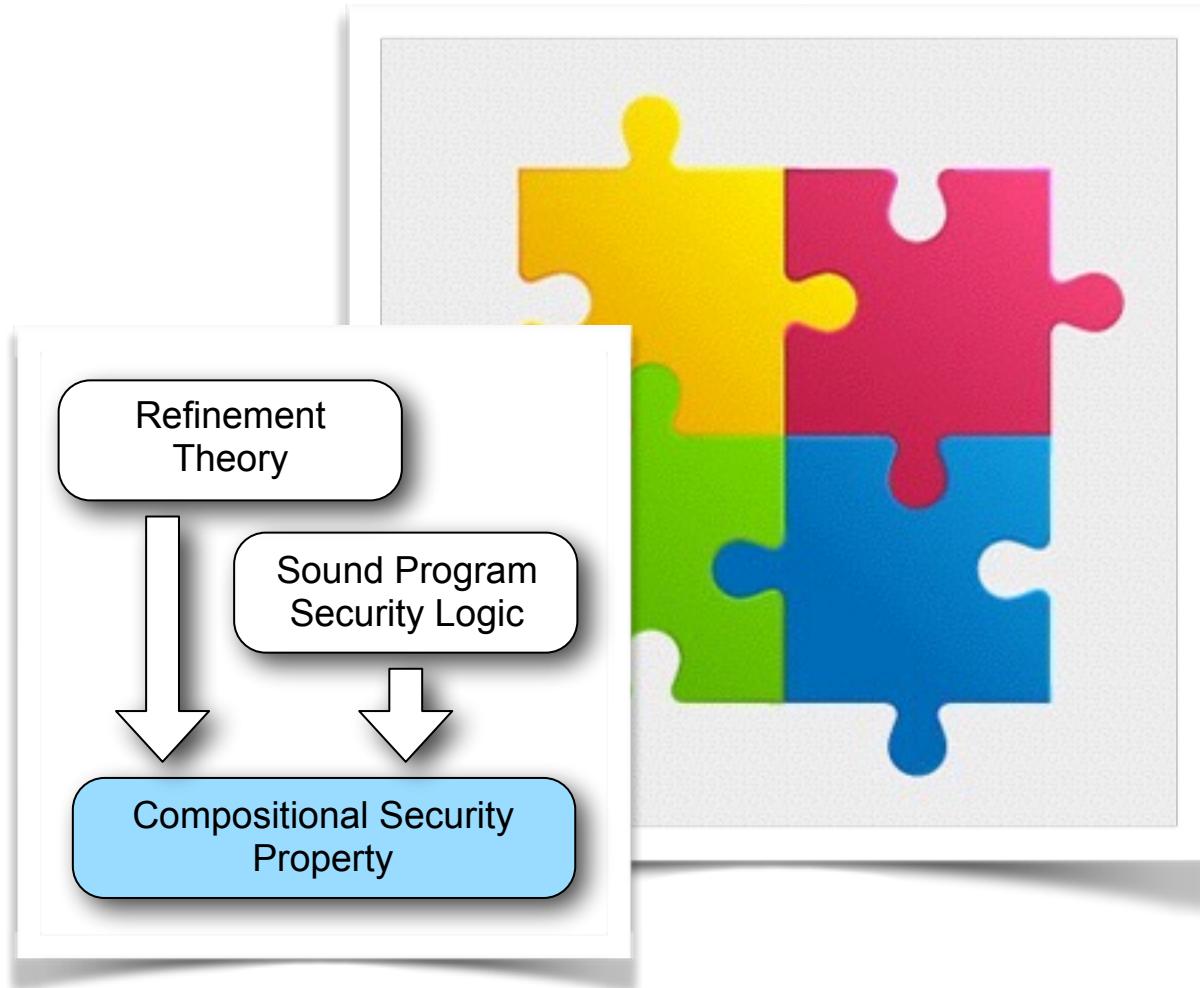
Verification Framework



COMPOSITIONAL SECURITY



COMPOSITIONAL SECURITY



Minimum Requirements

```
l = 0;  
if (h){  
    h = 0;  
}  
l = 1;
```

Minimum Requirements

```
l = 0;  
if (h){  
    h = 0;  
}  
l = 1;
```

Secure?

Minimum Requirements

```
l = 0;  
if (h){  
    h = 0;  
}  
l = 1;
```

Secure?

Timing-Insensitive Security:

Minimum Requirements

```
l = 0;  
if (h){  
    h = 0;  
}  
l = 1;
```

Secure?

Timing-Insensitive Security: **YES**

Minimum Requirements

```
l = 0;  
if (h){  
    h = 0;  
}  
l = 1;
```

Secure?

Timing-Insensitive Security: **YES**

Timing-Sensitive Security:

Minimum Requirements

```
l = 0;  
if (h){  
    h = 0;  
}  
l = 1;
```

Secure?

Timing-Insensitive Security: **YES**

Timing-Sensitive Security: **NO**

Minimum Requirements

```
l = 0;  
if (h){  
    h = 0;  
}  
l = 1;
```

```
print(l);
```



Secure?

Timing-Insensitive Security:

Minimum Requirements

```
l = 0;  
if (h){  
    h = 0;  
}  
l = 1;
```

```
print(l);
```

Secure?

Timing-Insensitive Security: **NO**

Minimum Requirements

```
l = 0;  
if (h){  
    h = 0;  
}  
l = 1;
```

```
print(l);
```



Secure?

Timing-Insensitive Security: **NO**

Timing-Sensitive Security:

Minimum Requirements

```
l = 0;  
if (h){  
    h = 0;  
}  
l = 1;
```

```
print(l);
```

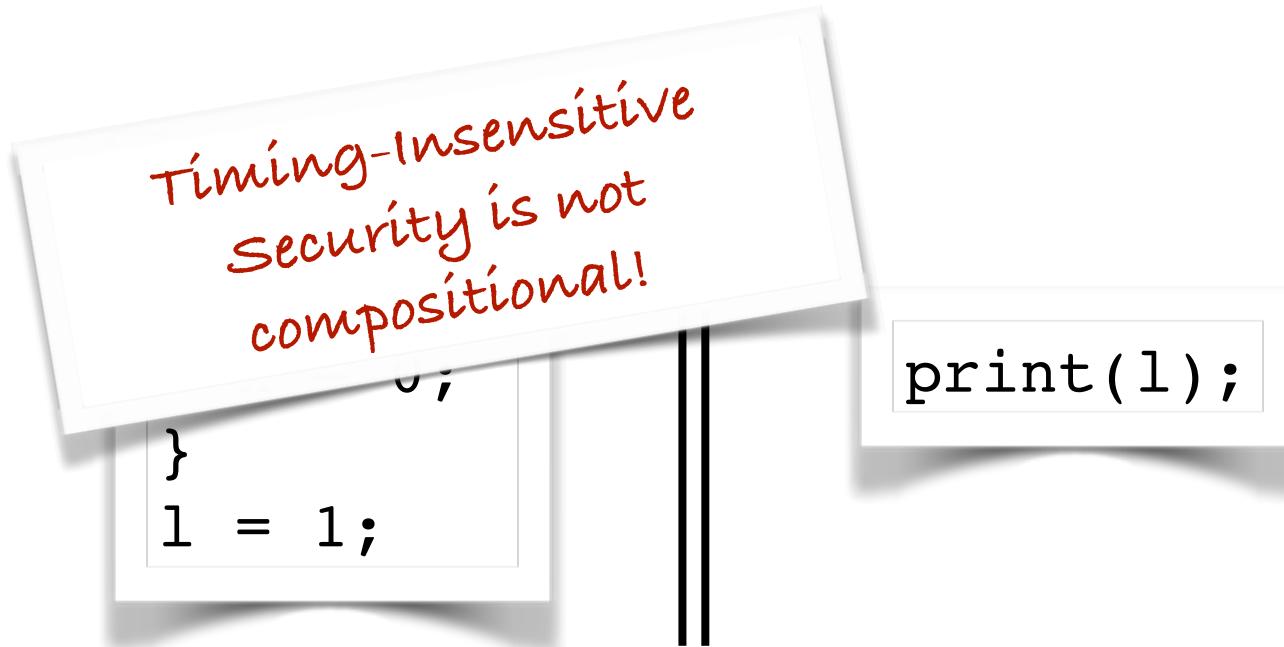


Secure?

Timing-Insensitive Security: **NO**

Timing-Sensitive Security: **NO** (trivially)

Minimum Requirements



Secure?

Timing-Insensitive Security: **NO**

Timing-Sensitive Security: **NO** (trivially)

Minimum Requirements

Timing-insensitive
security is not
compositional!

```
    }  
    l = 1;  
};
```

```
print(l);
```

Security not only
struggles to refine, but
also to compose!

Timing-Insensitive Security: **NO**

Timing-Sensitive Security: **NO** (trivially)

Minimum Requirements

Timing-insensitive
security is not
compositional!

```
    }  
    l = 1;  
};
```

```
print(l);
```

Security not only
struggles to refine, but
also to compose!

Timing-Insensitive Security: **NO**

(known since
Volpano & Smith,
CSFW 1998)

Timing-Sensitive Security: **NO** (trivially)

Minimum Requirements

Timing-insensitive
security is not
compositional!

```
    }  
    l = 1;  
};
```

```
print(l);
```

Security not only
struggles to refine, but
also to compose!

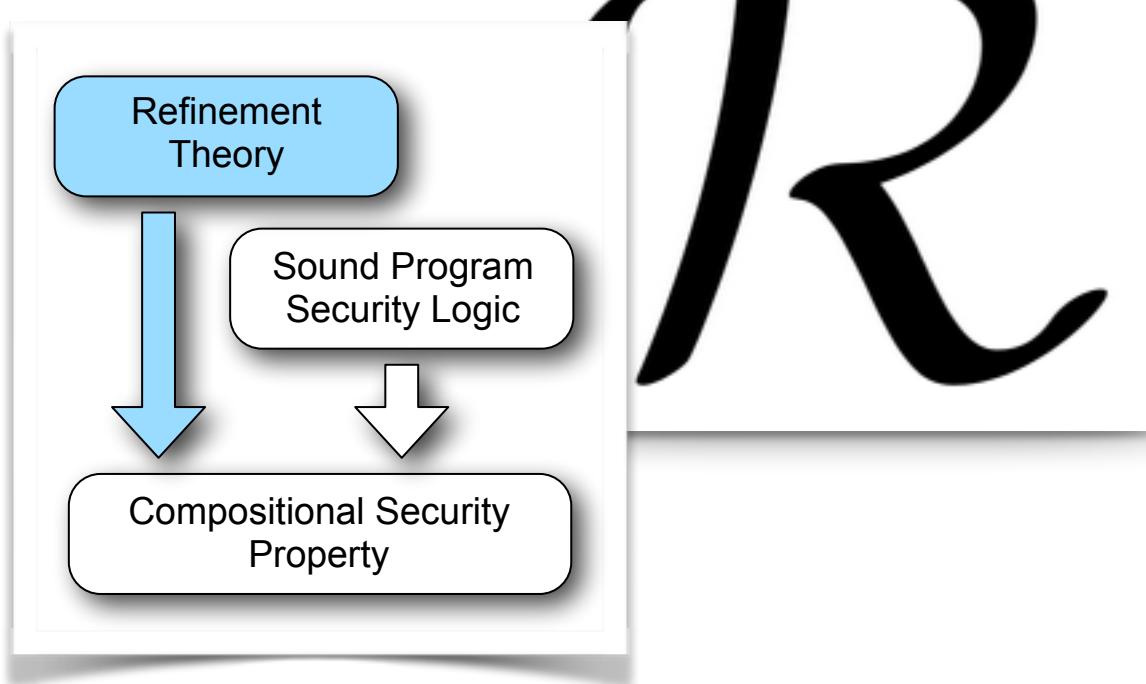
Timing-Insensitive Security: **NO**

Timing-Sensitive Security: **NO** (trivially)

COMPOSITIONAL REFINEMENT

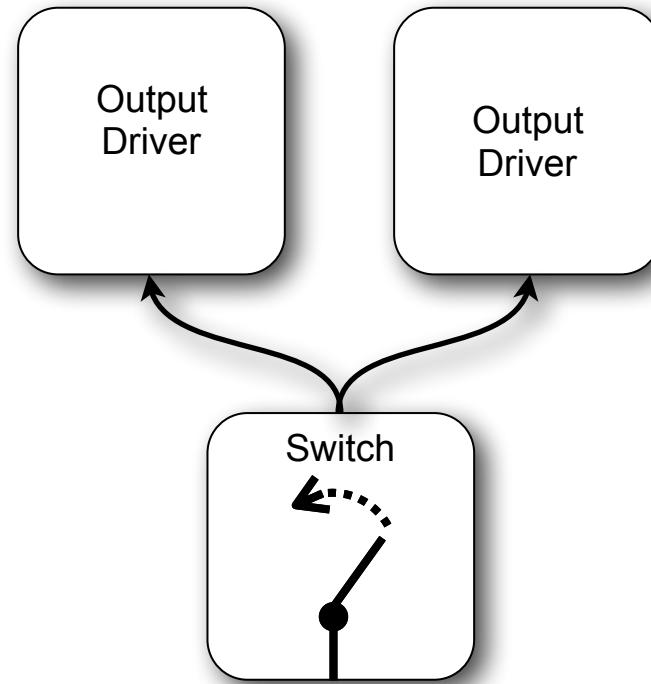
R

COMPOSITIONAL REFINEMENT

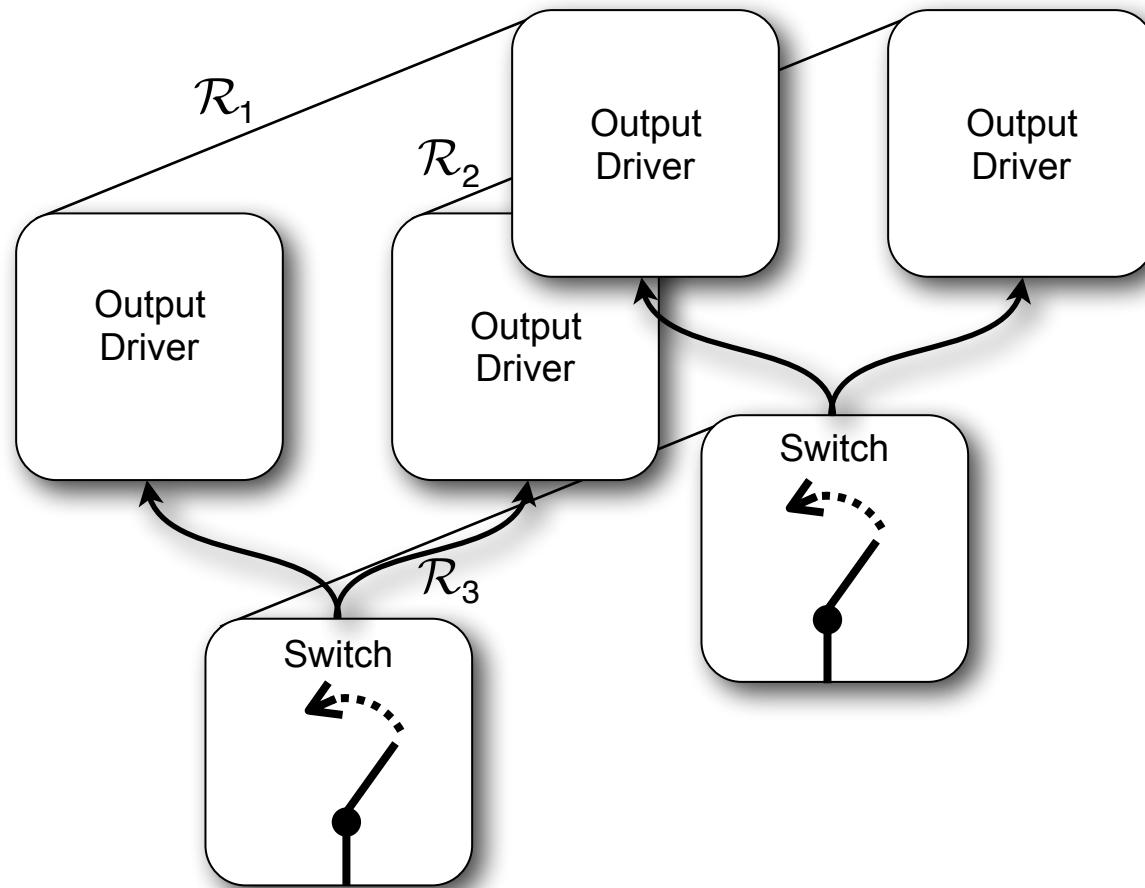


R

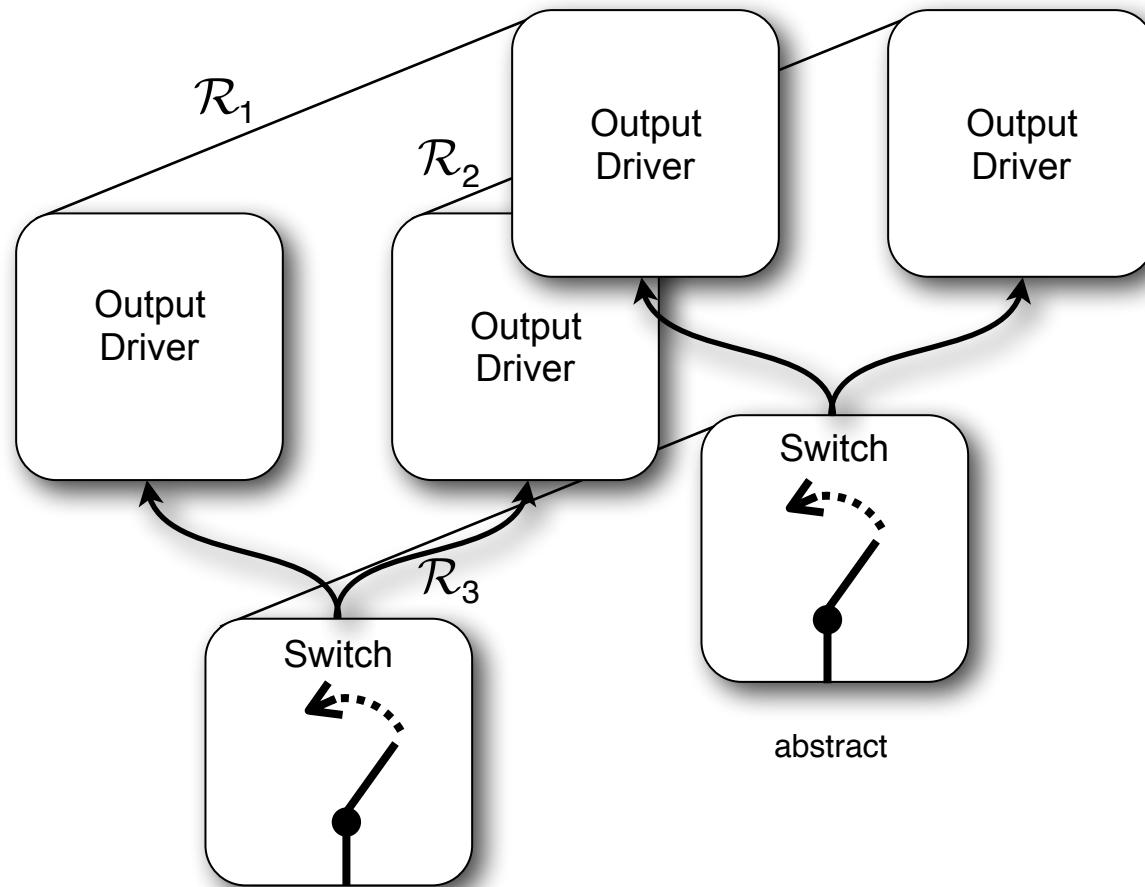
Secure Componentwise Refinement



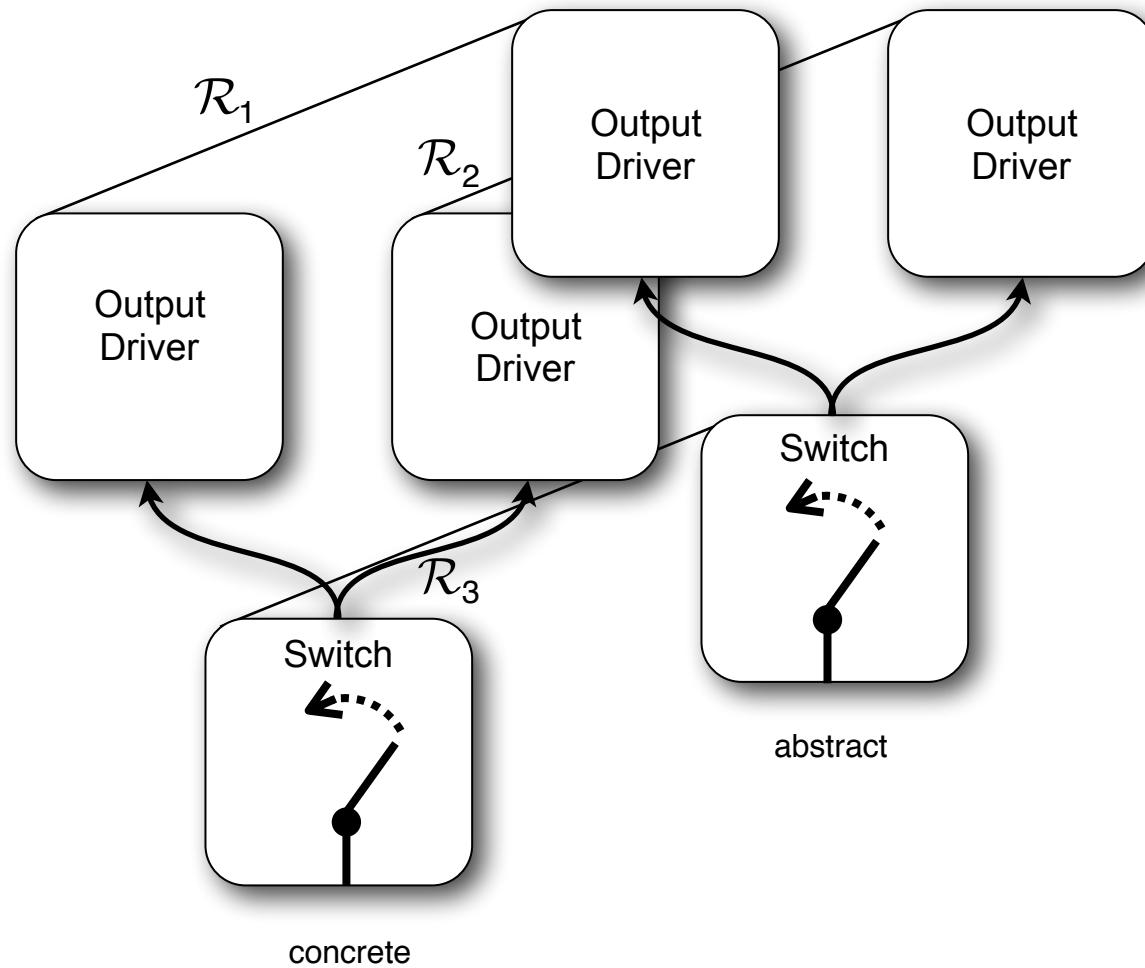
Secure Componentwise Refinement



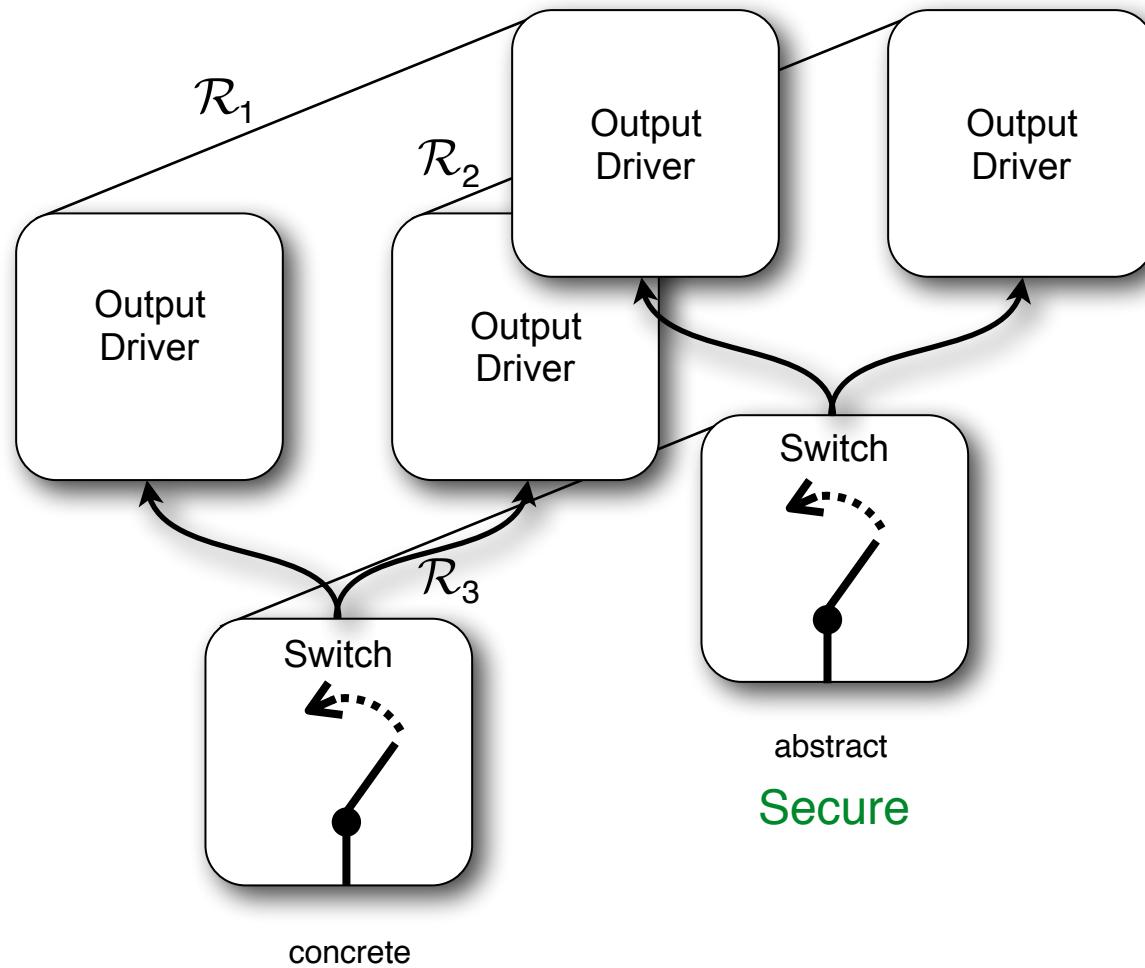
Secure Componentwise Refinement



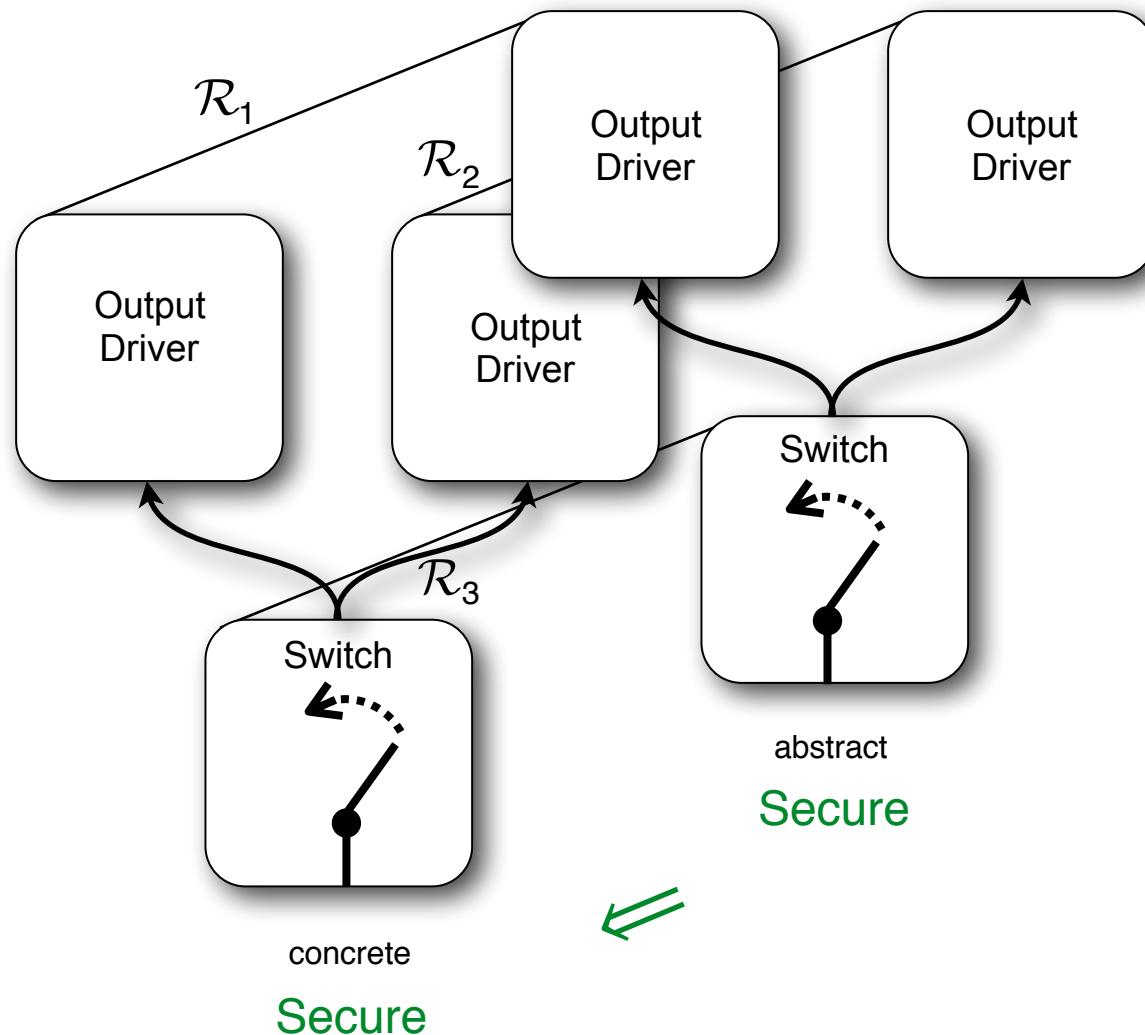
Secure Componentwise Refinement



Secure Componentwise Refinement



Secure Componentwise Refinement



Component Refinement

```
skip /* control +=_m AsmNoW */;
skip /* temp +=_m AsmNoRW */;
temp := buffer;
if control == 0 then
    low-var := temp
else
    high-var := temp
endif;
temp := 0;
skip /* temp -=_m AsmNoRW */
```

```
skip /* control_C +=_m AsmNoW */;
skip /* temp_C +=_m AsmNoRW */;
temp_C := buffer_C;
reg_C := control_C;
if reg_C == 0 then
    low-var_C := temp_C
else
    high-var_C := temp_C
endif;
temp_C := 0;
skip /* temp_C -=_m AsmNoRW */
```

Component Refinement

Original Program

```
skip /* control +=_m AsmNoW */;
skip /* temp +=_m AsmNoRW */;
temp := buffer;
if control == 0 then
    low-var := temp
else
    high-var := temp
endif;
temp := 0;
skip /* temp -=_m AsmNoRW */
```

```
skip /* control_C +=_m AsmNoW */;
skip /* temp_C +=_m AsmNoRW */;
temp_C := buffer_C;
reg_C := control_C;
if reg_C == 0 then
    low-var_C := temp_C
else
    high-var_C := temp_C
endif;
temp_C := 0;
skip /* temp_C -=_m AsmNoRW */
```

Component Refinement

Original Program

```
skip /* control +=_m AsmNoW */;
skip /* temp +=_m AsmNoRW */;
temp := buffer;
if control == 0 then
    low-var := temp
else
    high-var := temp
endif;
temp := 0;
skip /* temp -=_m AsmNoRW */
```

A Trivial Refinement

```
skip /* control_C +=_m AsmNoW */;
skip /* temp_C +=_m AsmNoRW */;
temp_C := buffer_C;
reg_C := control_C;
if reg_C == 0 then
    low-var_C := temp_C
else
    high-var_C := temp_C
endif;
temp_C := 0;
skip /* temp_C -=_m AsmNoRW */
```

Component Refinement

concrete
variables
implementing
abstract ones

Original Program A Trivial Refinement



```
skip /* control +=_m AsmNoW */;
skip /* temp +=_m AsmNoRW */;
temp := buffer;
if control == 0 then
    low-var := temp
else
    high-var := temp
endif;
temp := 0;
skip /* temp -=_m AsmNoRW */
```

```
skip /* control_C +=_m AsmNoW */;
skip /* temp_C +=_m AsmNoRW */;
temp_C := buffer_C;
reg_C := control_C;
if reg_C == 0 then
    low-var_C := temp_C
else
    high-var_C := temp_C
endif;
temp_C := 0;
skip /* temp_C -=_m AsmNoRW */
```

Component Refinement

Original Program concrete variables implementing abstract ones A Trivial Refinement

```
skip /* control +=_m AsmNoW */;
skip /* temp +=_m AsmNoRW */;
temp := buffer;
if control == 0 then
    low-var := temp
else
    high-var := temp
endif;
temp := 0;
skip /* temp -=_m AsmNoRW */
```

```
skip /* control_C +=_m AsmNoW */;
skip /* temp_C +=_m AsmNoRW */;
temp_C := buffer_C;
reg_C := control_C;
if reg_C == 0 then
    low-var_C := temp_C
else
    high-var_C := temp_C
endif;
temp_C := 0;
skip /* temp_C -=_m AsmNoRW */
```

Component Refinement

Original Program

```
skip /* control +=_m AsmNoW */;
skip /* temp +=_m AsmNoRW */;
temp := buffer;
if control == 0 then
    low-var := temp
else
    high-var := temp
endif;
temp := 0;
skip /* temp -=_m AsmNoRW */
```

A Trivial Refinement

```
skip /* control_C +=_m AsmNoW */;
skip /* temp_C +=_m AsmNoRW */;
temp_C := buffer_C;
reg_C := control_C;
if reg_C == 0 then
    low-var_C := temp_C
else
    high-var_C := temp_C
endif;
temp_C := 0;
skip /* temp_C -=_m AsmNoRW */
```

Component Refinement

Original Program

```
skip /* control +=_m AsmNoW */;
skip /* temp +=_m AsmNoRW */;
temp := buffer;
if control == 0 then
    low-var := temp
else
    high-var := temp
endif;
temp := 0;
skip /* temp -=_m AsmNoRW */
```

A Trivial Refinement

```
skip /* control_C +=_m AsmNoW */;
skip /* temp_C +=_m AsmNoRW */;
temp_C := buffer_C;
reg_C := control_C;
if reg_C == 0 then
    low-var_C := temp_C
else
    high-var_C := temp_C
endif;
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skip /* temp_C -=_m AsmNoRW */
```

Component Refinement

Original Program

```
skip /* control +=_m AsmNoW */;
skip /* temp +=_m AsmNoRW */;
temp := buffer;
if control == 0 then
    low-var := temp
else
    high-var := temp
endif;
temp := 0;
skip /* temp -=_m AsmNoRW */
```

A Trivial Refinement

```
skip /* control_C +=_m AsmNoW */;
skip /* temp_C +=_m AsmNoRW */;
temp_C := buffer_C;
reg_C := control_C;
if reg_C == 0 then
    low-var_C := temp_C
else
    high-var_C := temp_C
endif;
temp_C := 0;
skip /* temp_C -=_m AsmNoRW */
```

Abstract Program Security: Bisimulation

```
if (h) {
    h = 0;
    l = 1;
} else {
    skip;
    l = 1;
}
```

Abstract Program Security: Bisimulation

```
if (h) {                                if (h) {
    h = 0;                                h = 0;
    l = 1;                                l = 1;
} else {                                } else {
    skip;                                skip;
    l = 1;                                l = 1;
}
```

Abstract Program Security: Bisimulation

```
if (h) {  
    h = 0;  
    l = 1;  
} else {  
    skip;  
    l = 1;  
}
```

β

```
if (h) {  
    h = 0;  
    l = 1;  
} else {  
    skip;  
    l = 1;  
}
```

Abstract Program Security: Bisimulation

```
if (h) {  
    h = 0;  
    l = 1;  
} else {  
    skip;  
    l = 1;  
}
```

β

```
if (h) {  
    h = 0;  
    l = 1;  
} else {  
    skip;  
    l = 1;  
}
```

Important:

β must guarantee that
the two memories are
always Low-
equivalent

Abstract Program Security: Bisimulation

```
if (h) {  
    h = 0;  
    l = 1;  
} else {  
    skip;  
    l = 1;  
}
```

β

```
if (h) {  
    h = 0;  
    l = 1;  
} else {  
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}
```

Important:

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the two memories are
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equivalent

Abstract Program Security: Bisimulation

```
if (h) {  
    h = 0;  
    l = 1;  
} else {  
    skip;  
    l = 1;  
}
```

β

```
if (h) {  
    h = 0;  
    l = 1;  
} else {  
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}
```

Important:

β must guarantee that
the two memories are
always Low-
equivalent

Abstract Program Security: Bisimulation

```
if (h) {  
    h = 0;  
    l = 1;  
} else {  
    skip;  
    l = 1;  
}
```

β

```
if (h) {  
    h = 0;  
    l = 1;  
} else {  
    skip;  
    l = 1;  
}
```

Important:

β must guarantee that
the two memories are
always Low-
equivalent

Abstract Program Security: Bisimulation

```
if (h) {  
    h = 0;  
    l = 1;  
} else {  
    skip;  
    l = 1;  
}
```

\mathcal{B}

```
if (h) {  
    h = 0;  
    l = 1;  
} else {  
    skip;  
    l = 1;  
}
```

(the soundness proof for the security logic constructs an appropriate \mathcal{B})

Important:

\mathcal{B} must guarantee that the two memories are always Low-equivalent

Refining High Conditionals

```
if (h) {
    h = 0;
    l = 1;
} else {
    skip;
    l = 1;
}
```

Refining High Conditionals

A Secure Program

```
if (h) {  
    h = 0;  
    l = 1;  
} else {  
    skip;  
    l = 1;  
}
```

Refining High Conditionals

A Secure Program

```
if (h) {  
    h = 0;  
    l = 1;  
} else {  
    skip;  
    l = 1;  
}  
  
branches need  
to do the same  
Low things at  
the same time
```

Refining High Conditionals

A Secure Program

```
if (h) {  
    h = 0;  
    l = 1;  
} else {  
    skip;  
    l = 1;  
}
```

branches need
to do the same
Low things at
the same time

A Trivial Refinement

```
if (h) {  
    h = 0;  
    l = 1;  
} else {  
    l = 1;  
}
```

Refining High Conditionals

A Secure Program

branches need
to do the same
Low things at
the same time

```
if (h) {  
    h = 0;  
    l = 1;  
} else {  
    skip;  
    l = 1;  
}
```

A Trivial Refinement

```
if (h) {  
    h = 0;  
    l = 1;  
} else {  
    l = 1;  
}
```

insecure

Refining High Conditionals

A Secure Program

branches need
to do the same
Low things at
the same time

```
if (h) {  
    h = 0;  
    l = 1;  
} else {  
    skip;  
    l = 1;  
}
```

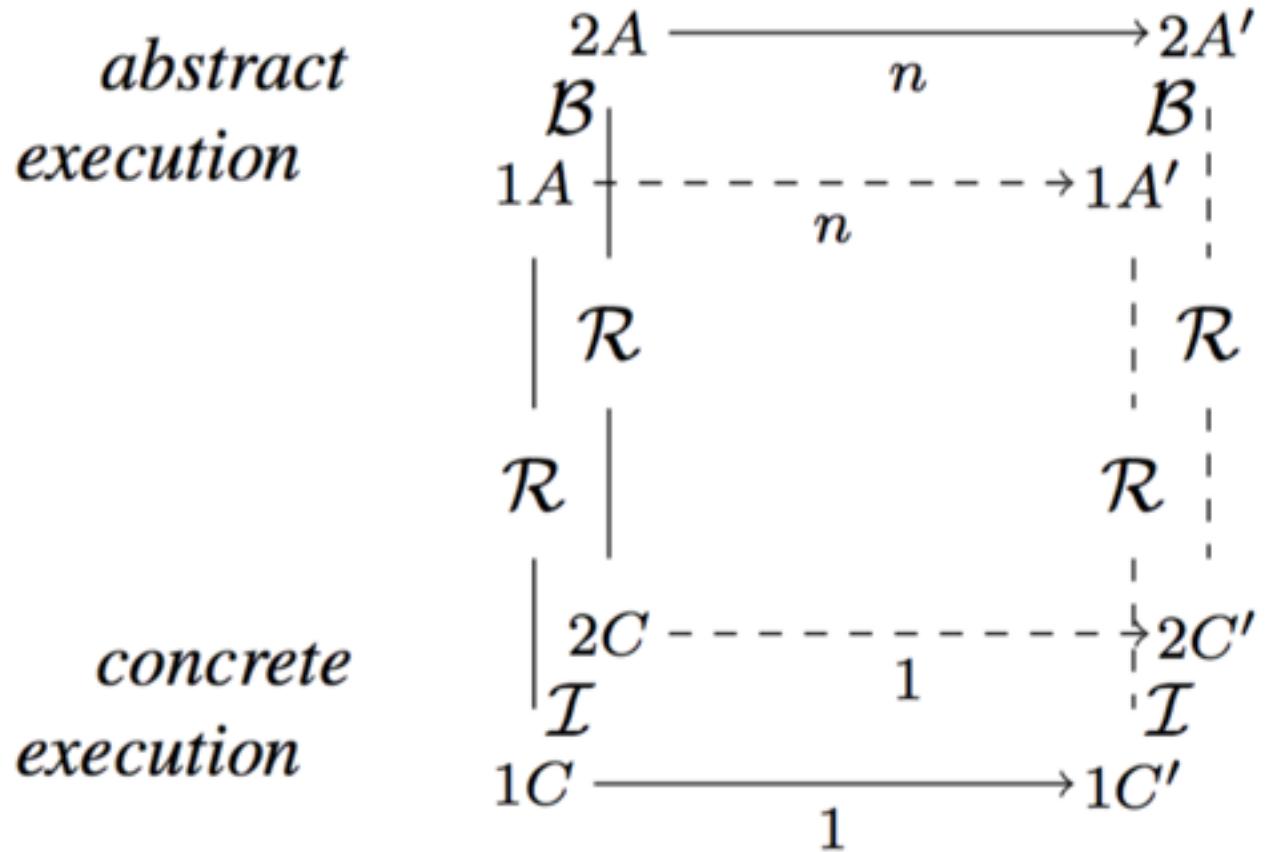
A Trivial Refinement

```
if (h) {  
    h = 0;  
    l = 1;  
} else {  
    l = 1;  
}
```

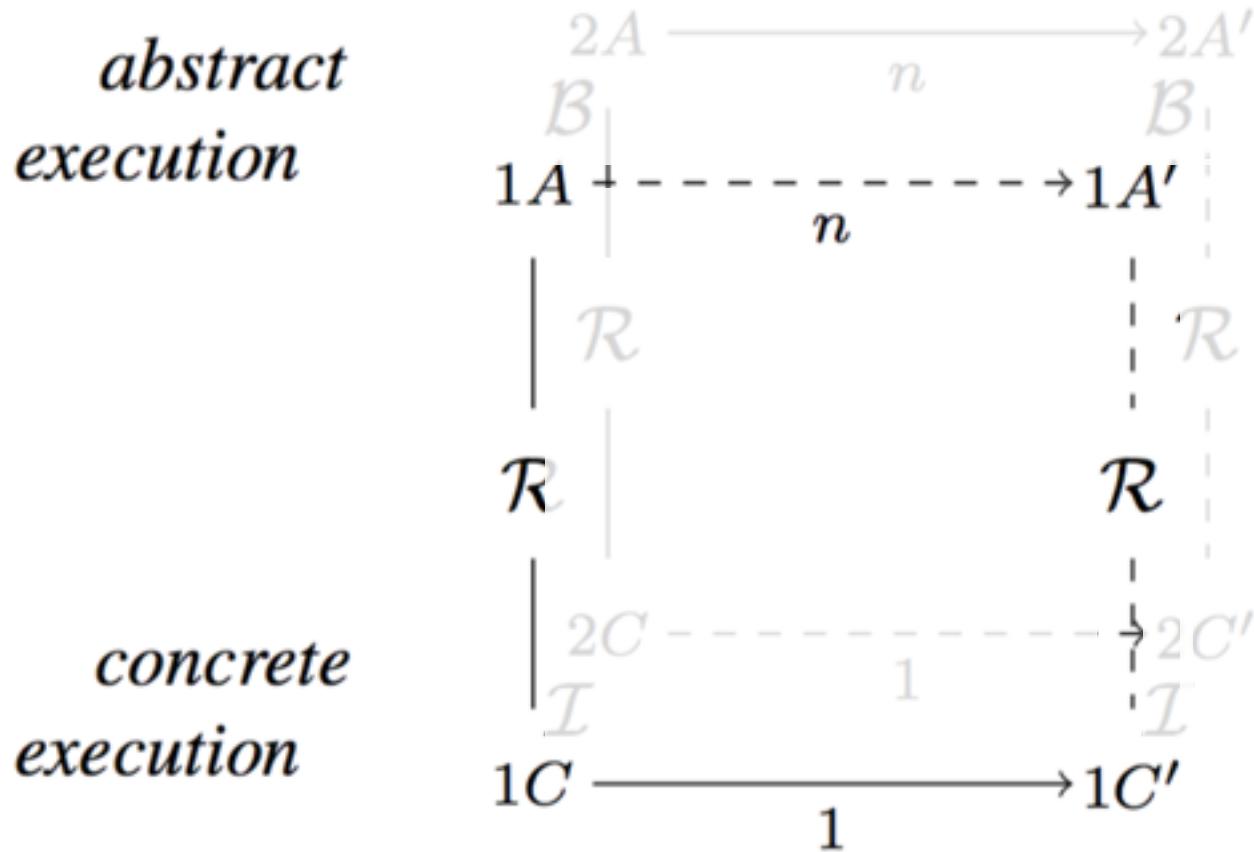
insecure

Need to make sure that the
concrete executions stay in sync.

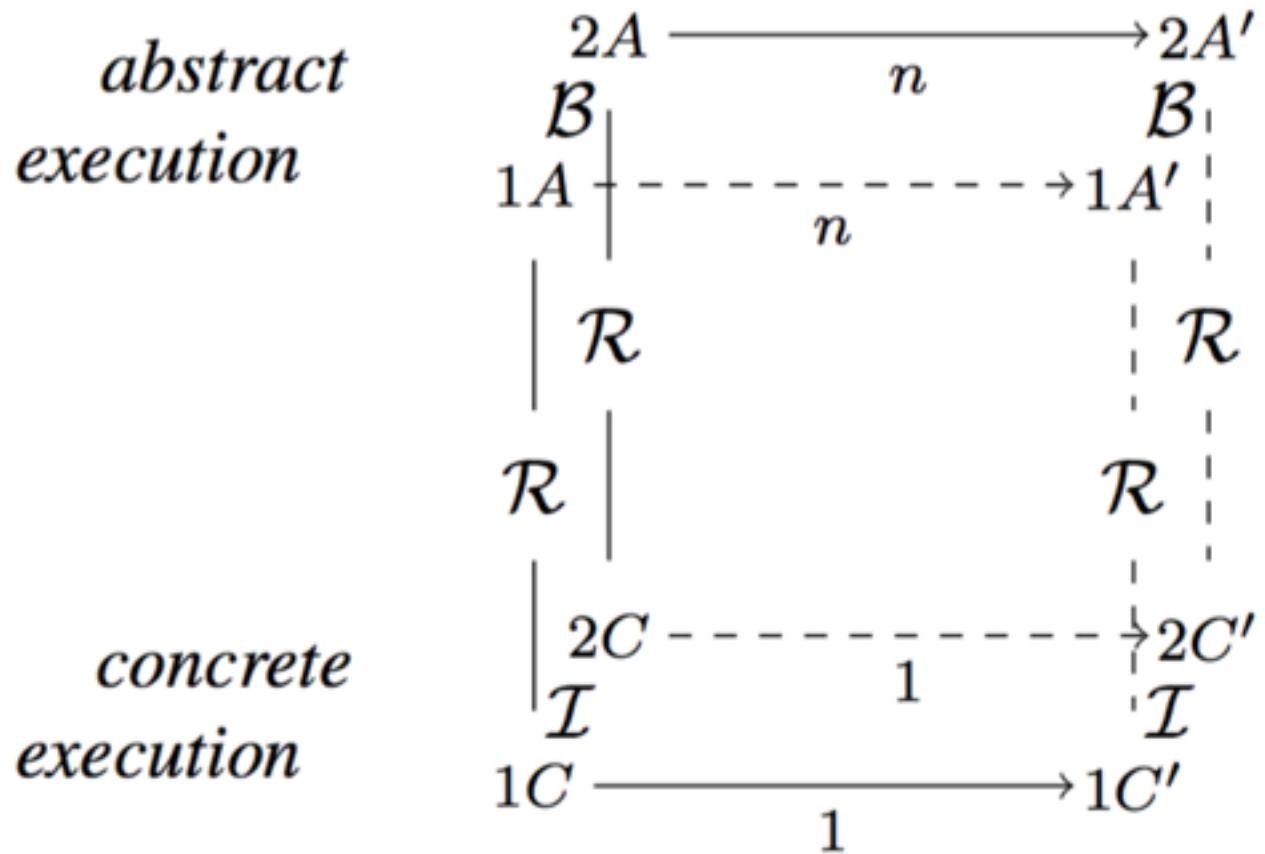
Secure Refinement via Coupling



Secure Refinement via Coupling



Secure Refinement via Coupling



Coupling Invariant: \mathcal{I}

```
skip /* h +=_m AsmNoW */;
skip /* y +=_m AsmNoW */;
skip /* z +=_m AsmNoW */;

y := 0;
z := 0;
x := y;
if h != 0 then
    x := y
else
    x := y + z
endif
```

Coupling Invariant: \mathcal{I}

```
skip /*  $h_C \mathrel{+}=_m \text{AsmNoW}$  */;
skip /*  $y_C \mathrel{+}=_m \text{AsmNoW}$  */;
skip /*  $z_C \mathrel{+}=_m \text{AsmNoW}$  */;

 $y_C := 0$ ;
 $z_C := 0$ ;
 $x_C := y_C$ ;
reg3 $_C := h_C$ ;
if reg3 $_C \neq 0$  then
    skip;
    skip;
    reg0 $_C := y_C$ ;
     $x_C := \text{reg0}_C$ 
else
    reg1 $_C := y_C$ ;
    reg2 $_C := z_C$ ;
    reg0 $_C := \text{reg1}_C + \text{reg2}_C$ ;
     $x_C := \text{reg0}_C$ 
endif
```

Coupling Invariant: \mathcal{I}

```
skip /*  $h_C +=_m \text{AsmNoW}$  */;
skip /*  $y_C +=_m \text{AsmNoW}$  */;
skip /*  $z_C +=_m \text{AsmNoW}$  */;

 $y_C := 0$ ;
 $z_C := 0$ ;
 $x_C := y_C$ ;
reg3 $_C := h_C$ ;
if reg3 $_C != 0$  then
    skip;
    skip;
    reg0 $_C := y_C$ ;
     $x_C := \text{reg0}_C$ 
else
    reg1 $_C := y_C$ ;
    reg2 $_C := z_C$ ;
    reg0 $_C := \text{reg1}_C + \text{reg2}_C$ ;
     $x_C := \text{reg0}_C$ 
endif
```

```
skip /*  $h_C +=_m \text{AsmNoW}$  */;
skip /*  $y_C +=_m \text{AsmNoW}$  */;
skip /*  $z_C +=_m \text{AsmNoW}$  */;

 $y_C := 0$ ;
 $z_C := 0$ ;
 $x_C := y_C$ ;
reg3 $_C := h_C$ ;
if reg3 $_C != 0$  then
    skip;
    skip;
    reg0 $_C := y_C$ ;
     $x_C := \text{reg0}_C$ 
else
    reg1 $_C := y_C$ ;
    reg2 $_C := z_C$ ;
    reg0 $_C := \text{reg1}_C + \text{reg2}_C$ ;
     $x_C := \text{reg0}_C$ 
endif
```

Coupling Invariant: \mathcal{I}

```
skip /*  $h_C +=_m \text{AsmNoW}$  */;  
skip /*  $y_C +=_m \text{AsmNoW}$  */;  
skip /*  $z_C +=_m \text{AsmNoW}$  */;  
 $y_C := 0;$   
 $z_C := 0;$   
 $x_C := y_C;$   
 $\text{reg3}_C := h_C;$   
if  $\text{reg3}_C != 0$  then  
    skip;  
    skip;  
     $\text{reg0}_C := y_C;$   
     $x_C := \text{reg0}_C$   
else  
     $\text{reg1}_C := y_C;$   
     $\text{reg2}_C := z_C;$   
     $\text{reg0}_C := \text{reg1}_C + \text{reg2}_C;$   
     $x_C := \text{reg0}_C$   
endif
```

```
skip /*  $h_C +=_m \text{AsmNoW}$  */;  
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 $y_C := 0;$   
 $z_C := 0;$   
 $x_C := y_C;$   
 $\text{reg3}_C := h_C;$   
if  $\text{reg3}_C != 0$  then  
    skip;  
    skip;  
     $\text{reg0}_C := y_C;$   
     $x_C := \text{reg0}_C$   
else  
     $\text{reg1}_C := y_C;$   
     $\text{reg2}_C := z_C;$   
     $\text{reg0}_C := \text{reg1}_C + \text{reg2}_C;$   
     $x_C := \text{reg0}_C$   
endif
```

Coupling Invariant: \mathcal{I}

```
skip /*  $h_C +=_m \text{AsmNoW}$  */;  
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skip /*  $z_C +=_m \text{AsmNoW}$  */;  
 $y_C := 0;$   
 $z_C := 0;$   
 $x_C := y_C;$   
 $\text{reg3}_C := h_C;$   
if  $\text{reg3}_C != 0$  then  
    skip;  
    skip;  
     $\text{reg0}_C := y_C;$   
     $x_C := \text{reg0}_C$   
else  
     $\text{reg1}_C := y_C;$   
     $\text{reg2}_C := z_C;$   
     $\text{reg0}_C := \text{reg1}_C + \text{reg2}_C;$   
     $x_C := \text{reg0}_C$   
endif
```

```
skip /*  $h_C +=_m \text{AsmNoW}$  */;  
skip /*  $y_C +=_m \text{AsmNoW}$  */;  
skip /*  $z_C +=_m \text{AsmNoW}$  */;  
 $y_C := 0;$   
 $z_C := 0;$   
 $x_C := y_C;$   
 $\text{reg3}_C := h_C;$   
if  $\text{reg3}_C != 0$  then  
    skip;  
    skip;  
     $\text{reg0}_C := y_C;$   
     $x_C := \text{reg0}_C$   
else  
     $\text{reg1}_C := y_C;$   
     $\text{reg2}_C := z_C;$   
     $\text{reg0}_C := \text{reg1}_C + \text{reg2}_C;$   
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endif
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Coupling Invariant: \mathcal{I}

```
skip /*  $h_C +=_m \text{AsmNoW}$  */;  
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 $y_C := 0;$   
 $z_C := 0;$   
 $x_C := y_C;$   
 $\text{reg3}_C := h_C;$   
if  $\text{reg3}_C != 0$  then  
    skip;  
    skip;  
     $\text{reg0}_C := y_C;$   
     $x_C := \text{reg0}_C$   
else  
     $\text{reg1}_C := y_C;$   
     $\text{reg2}_C := z_C;$   
     $\text{reg0}_C := \text{reg1}_C + \text{reg2}_C;$   
     $x_C := \text{reg0}_C$   
endif
```

```
skip /*  $h_C +=_m \text{AsmNoW}$  */;  
skip /*  $y_C +=_m \text{AsmNoW}$  */;  
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 $y_C := 0;$   
 $z_C := 0;$   
 $x_C := y_C;$   
 $\text{reg3}_C := h_C;$   
if  $\text{reg3}_C != 0$  then  
    skip;  
    skip;  
     $\text{reg0}_C := y_C;$   
     $x_C := \text{reg0}_C$   
else  
     $\text{reg1}_C := y_C;$   
     $\text{reg2}_C := z_C;$   
     $\text{reg0}_C := \text{reg1}_C + \text{reg2}_C;$   
     $x_C := \text{reg0}_C$   
endif
```

Coupling Invariant: \mathcal{I}

```
skip /*  $h_C +=_m \text{AsmNoW}$  */;  
skip /*  $y_C +=_m \text{AsmNoW}$  */;  
skip /*  $z_C +=_m \text{AsmNoW}$  */;  
  
 $y_C := 0;$   
 $z_C := 0;$   
 $x_C := y_C;$   
 $\text{reg3}_C := h_C;$   
if  $\text{reg3}_C \neq 0$  then  
    skip;  
    skip;  
     $\text{reg0}_C := y_C;$   
     $x_C := \text{reg0}_C$   
else  
     $\text{reg1}_C := y_C;$   
     $\text{reg2}_C := z_C;$   
     $\text{reg0}_C := \text{reg1}_C + \text{reg2}_C;$   
     $x_C := \text{reg0}_C$   
endif
```

```
skip /*  $h_C +=_m \text{AsmNoW}$  */;  
skip /*  $y_C +=_m \text{AsmNoW}$  */;  
skip /*  $z_C +=_m \text{AsmNoW}$  */;  
  
 $y_C := 0;$   
 $z_C := 0;$   
 $x_C := y_C;$   
 $\text{reg3}_C := h_C;$   
if  $\text{reg3}_C = 1$  then
```

Important:
 \mathcal{I} need not talk at all
about memory
contents being secure

```
 $\text{reg0}_C := \text{reg1}_C + \text{reg2}_C;$   
 $x_C := \text{reg0}_C$   
endif
```

Concurrency-Aware Refinement

$$x := y + z$$

Concurrency-Aware Refinement

$$x := y + z$$

*Source language semantics
evaluates $y + z$ atomically*

Concurrency-Aware Refinement

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Source language semantics
evaluates $y + z$ atomically

Imagine we compile to a simple
stack machine:

```
PUSH y;  
PUSH z;  
ADD;  
POP x;
```

Concurrency-Aware Refinement

$$x := y + z$$

Source language semantics
evaluates $y + z$ atomically

Imagine we compile to a simple
stack machine:

```
PUSH y;  
PUSH z;  
ADD;  
POP x;
```

This compilation is valid only if
no other thread concurrently
modifies y and z

Concurrency-Aware Refinement

$$x := y + z$$

Source language semantics
evaluates $y + z$ atomically

Imagine we compile to a simple
stack machine:

```
PUSH y;  
PUSH z;  
ADD;  
POP x;
```

This compilation is valid only if
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modifies y and z

Idea: require y and z to be
assumes not-writable by others

Concurrency-Aware Refinement

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Source language semantics
evaluates $y + z$ atomically

Imagine we compile to a simple
stack machine:

```
PUSH y;  
PUSH z;  
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POP x;
```

This compilation is valid only if
no other thread concurrently
modifies y and z

Idea: require y and z to be
assumes not-writable by others

i.e. that the refinement relation is
preserved by potential actions of
other threads

Concurrency-Aware Refinement

$$x := y + z$$

Source language semantics
evaluates $y + z$ atomically

Imagine we compile to a simple
stack machine:

```
PUSH y;  
PUSH z;  
ADD;  
POP x;
```

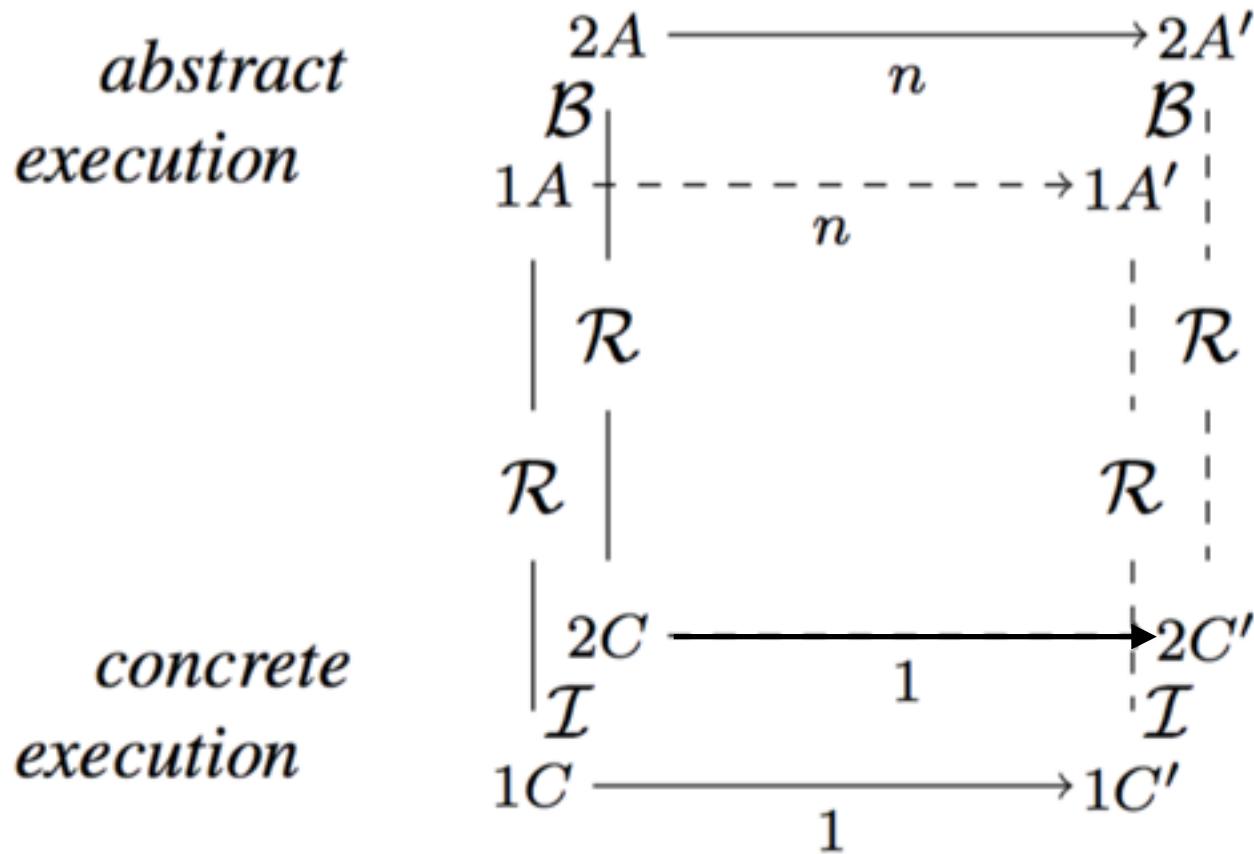
This compilation is valid only if
no other thread concurrently
modifies y and z

Idea: require y and z to be
assumes not-writable by others

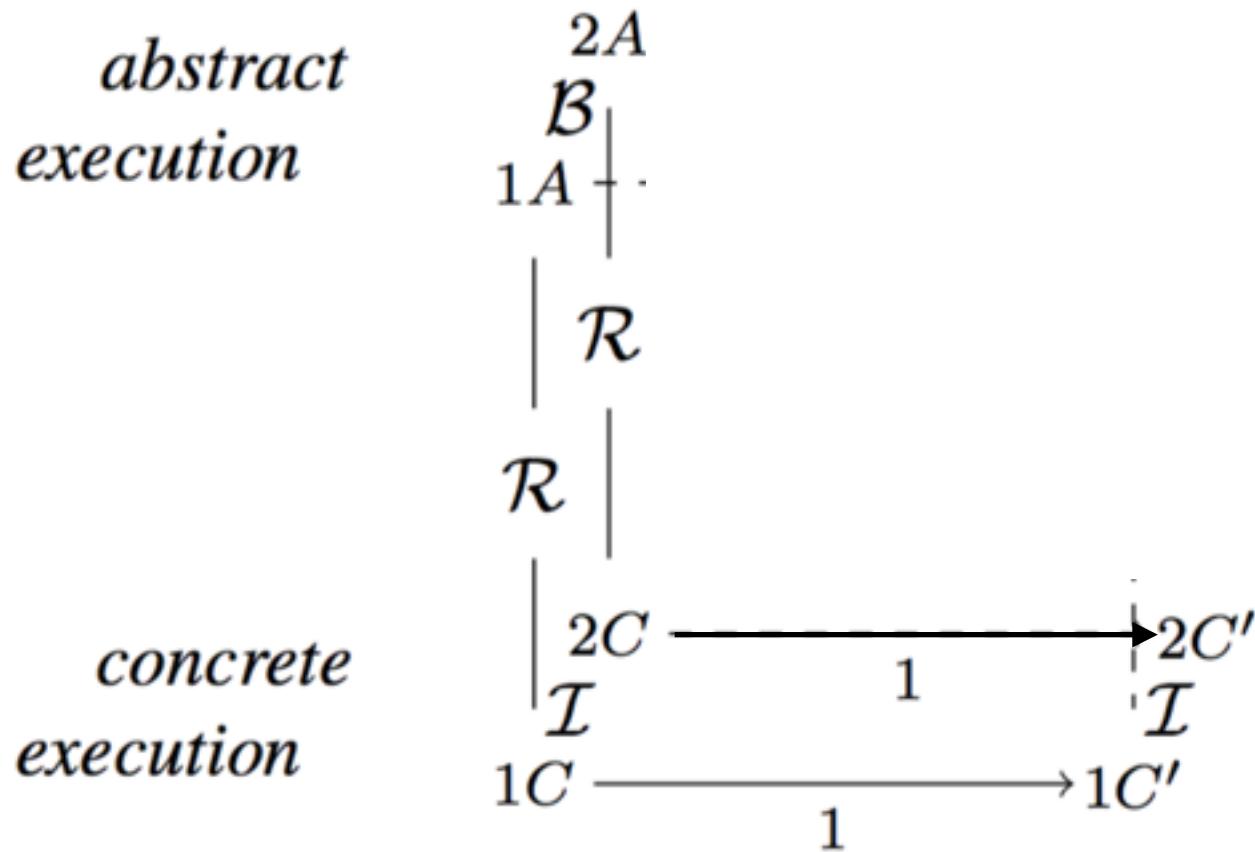
(see Liang et al., TOPLAS 2014)

i.e. that the refinement relation is
preserved by potential actions of
other threads

Leveraging Determinism

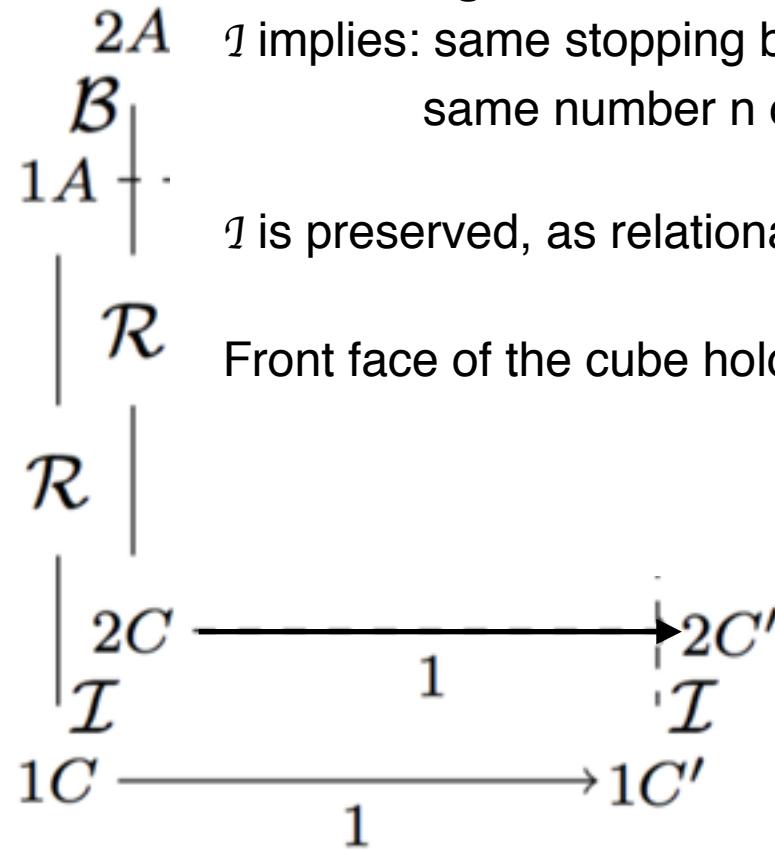


Leveraging Determinism



Leveraging Determinism

*abstract
execution*



Proof Obligations:

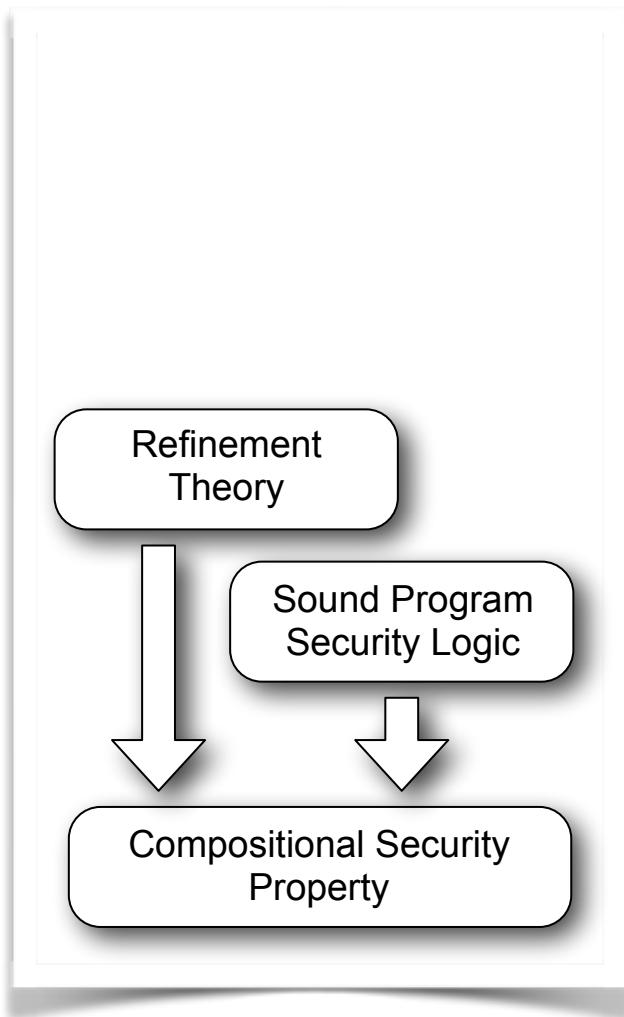
\mathcal{I} implies: same stopping behaviour
same number n of abstract steps

\mathcal{I} is preserved, as relational invariant

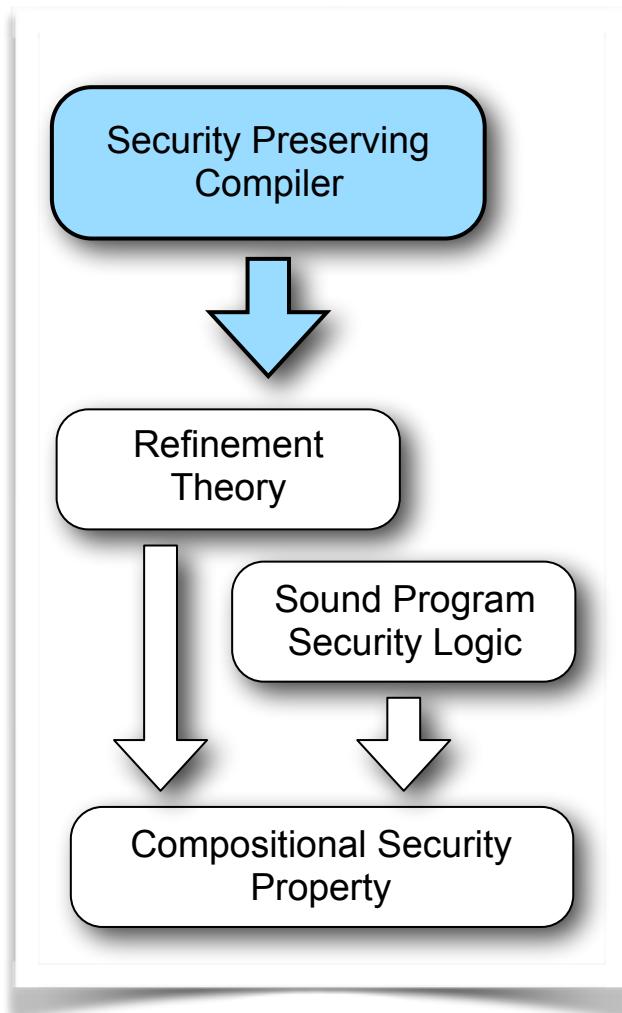
Front face of the cube holds

SECURITY-PRESERVING COMPILATION

SECURITY-PRESERVING COMPIRATION



SECURITY-PRESERVING COMPIRATION



Case Study: Compilation to Idealised RISC

```
instr ::= lock |  
        release |  
        load reg x  
        store x reg  
        Jump label  
        Jz label  
        Noop  
        MoveK reg w  
        Mov reg reg  
        Binop op reg reg
```

Case Study: Compilation to Idealised RISC

```
instr ::= lock |  
        release |  
        load reg x  
        store x reg  
        Jump label  
        Jz label  
        Noop  
        MoveK reg w  
        Mov reg reg  
        Binop op reg reg
```



Current Status

- Proof finished for source programs that are secure and never branch on High data
 - This is the simple case where the compiler doesn't have to do anything except compile the program properly to preserve noninterference
- Sufficient for the CDDC model we have verified
- First example compiler for shared-memory concurrent programs proved to preserve noninterference
- Next steps: High conditionals, weak memory, ...

CONCLUSION

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Moving from verified secure kernels
to verified secure systems:

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Moving from verified secure kernels
to verified secure systems:

- concurrency ~> compositionality ~>
timing-sensitivity, assume-guarantee reasoning
- dynamic policies (value-dependence)
- compositional secure refinement ~>
coupling invariants for preservation of timing-sensitive security

CONCLUSION

Moving from verified secure kernels
to verified secure systems:

- concurrency ~> compositionality ~>
timing-sensitivity, assume-guarantee reasoning
- dynamic policies (value-dependence)
- compositional secure refinement ~>
coupling invariants for preservation of timing-sensitive security

Still lots more to be done.

Thank You



toby.murray@unimelb.edu.au

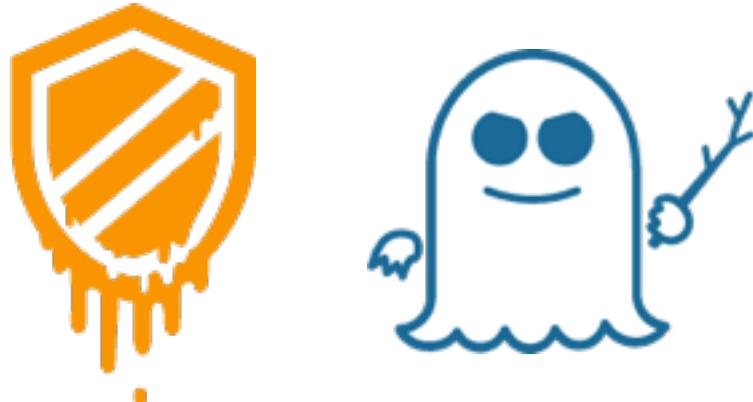


<http://people.eng.unimelb.edu.au/tobym>



@tobycmurray

What about ... ?



and various other **intra-device** timing
channels?

What about ... ?



and various other **intra-device** timing channels?

Untrusted

Legacy Apps

Linux Server

Trusted

Sensitive App

Trusted Service

seL4

Hardware

What about ... ?

Trusted



Sensitive App

Trusted Service

and various other **intra-device** timing
channels?

seL4

Hardware

Minimum Requirements

```
l = 0;  
if (h){  
    h = 0;  
}  
l = 1;
```

```
print(l);
```

Minimum Requirements

```
l = 0;  
if (h){  
    h = 0;  
}  
l = 1;
```

```
print(l);
```

Secure?

Minimum Requirements

```
l = 0;  
if (h){  
    h = 0;  
}  
l = 1;
```

```
print(l);
```

Secure?

Timing-Insensitive Security:

Minimum Requirements

3
pc →

($h = 0$)

```
l = 0;  
if (h){  
    h = 0;  
}  
l = 1;
```

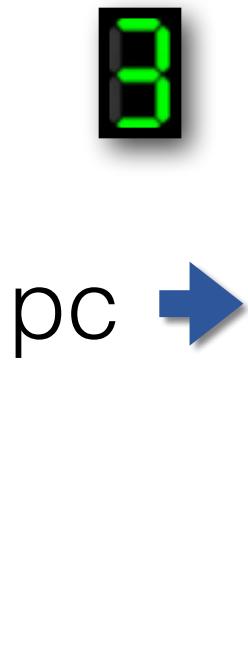


```
print(l);
```

Secure?

Timing-Insensitive Security:

Minimum Requirements



($h = 0$)

```
l = 0;  
if (h){  
    h = 0;  
}  
l = 1;
```

```
print(l);
```

Secure?

Timing-Insensitive Security:

Minimum Requirements

2
pc →

($h = 0$)

```
l = 0;  
if (h){  
    h = 0;  
}  
l = 1;
```



```
print(l);
```

Secure?

Timing-Insensitive Security:

Minimum Requirements

2

($h = 0$)

```
l = 0;  
if (h){  
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}  
l = 1;
```

pc →



```
print(l);
```

Secure?

Timing-Insensitive Security:

Minimum Requirements

8

($h = 0$)

```
l = 0;  
if (h){  
    h = 0;  
}  
l = 1;
```

pc →



```
print(l);
```

Secure?

Timing-Insensitive Security:

Minimum Requirements

8

($h = 0$)

```
l = 0;  
if (h){  
    h = 0;  
}  
l = 1;
```

pc →



```
print(l);
```

Secure?

Timing-Insensitive Security:

Minimum Requirements

0

($h = 0$)

```
l = 0;  
if (h){  
    h = 0;  
}  
l = 1;
```

pc →

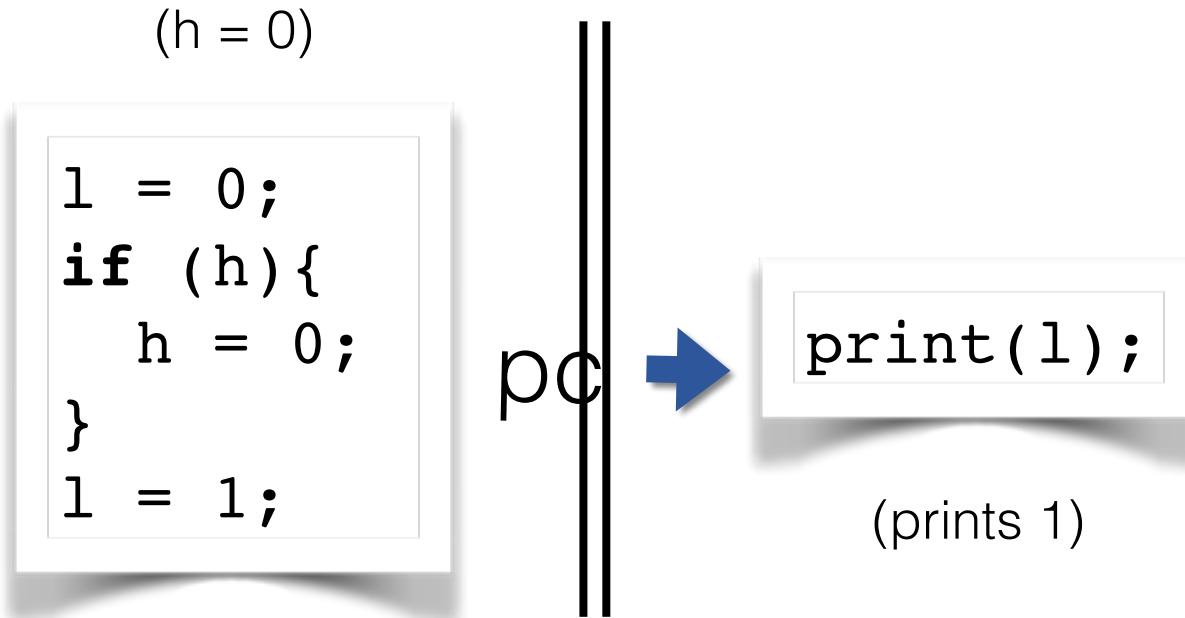
||

```
print(l);
```

Secure?

Timing-Insensitive Security:

Minimum Requirements



Secure?

Timing-Insensitive Security:

Minimum Requirements

3
pc →

($h = 1$)

```
l = 0;  
if (h){  
    h = 0;  
}  
l = 1;
```

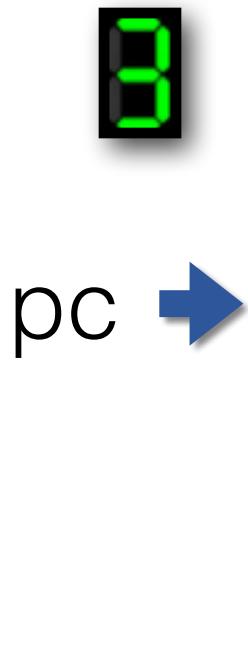


```
print(l);
```

Secure?

Timing-Insensitive Security:

Minimum Requirements



Secure?

Timing-Insensitive Security:

Minimum Requirements

2
pc →

($h = 1$)

```
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    h = 0;  
}  
l = 1;
```



```
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```

Secure?

Timing-Insensitive Security:

Minimum Requirements

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pc →

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}  
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```
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Secure?

Timing-Insensitive Security:

Minimum Requirements

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```
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Secure?

Timing-Insensitive Security:

Minimum Requirements

8

($h = 1$)

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l = 0;  
if (h){  
    h = 0;  
}  
l = 1;
```

pc →



```
print(l);
```

Secure?

Timing-Insensitive Security:

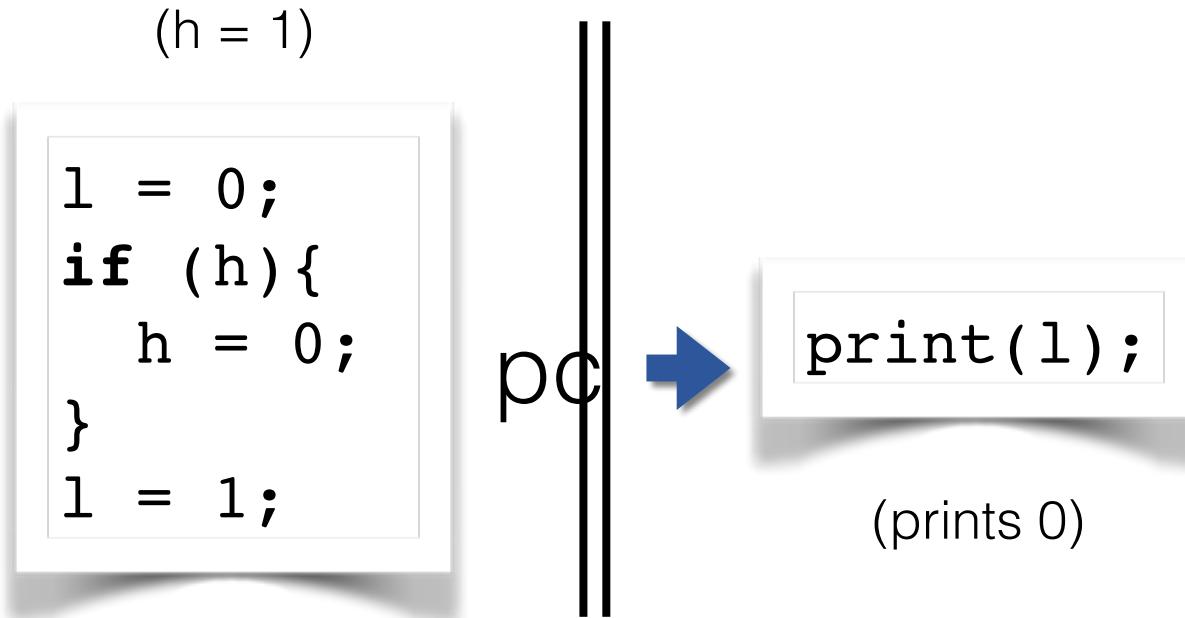
Minimum Requirements



Secure?

Timing-Insensitive Security:

Minimum Requirements



Secure?

Timing-Insensitive Security: