

# DSP cache architectures and optimization

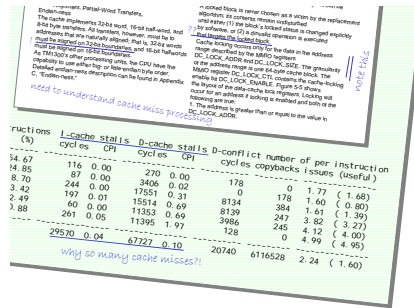


## DSP Extension

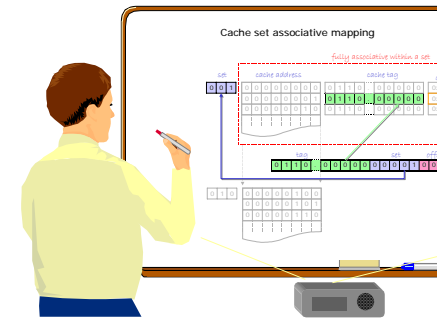
### Benefits

- Understand cache architectures
- Optimize cache usage
- Avoid cache pitfalls

Learn how to write programs that use cache architectures efficiently, and avoid common pitfalls.



### Missing something?



### We show you the map

### Contents

We describe and explain cache architectures and their impact on program execution speed. We also explain the question of 'cache coherency' due to the operation of peripherals that bypass the cache to access memory directly.

### Cache architecture

Learn the background to cache design including how and why caches can increase program execution speed. Including consideration of how certain types of pattern in data access can be very efficiently handled by caching, and when caching may be inappropriate.

- Purpose of a cache
- Temporal and spatial locality

### Cache coherency

Understand cache coherency and how to cope with it.

- Cache coherency
- invalidation and copyback

### Cache mapping

Learn how data is mapped into a cache: and the compromises that have to be accepted in the interests of economy and their impact on performance.

- Cache mapping
- Direct mapping
- Associative mapping
- Set associative mapping
- Sets and ways

### Cache hits and misses

How a cache handles cache hits and cache misses (i.e. when data is not found already in the cache). Including explanation of what happens when a cache miss occurs, and an indication of how to calculate and measure the delays involved.

- Cache search mechanisms
- Least Recently Used status
- Copyback and copythrough
- Cache hits and misses
- Dirty and invalid status
- Pre-fetching
- Mini-caches
- Cache levels

### Cache profiling

Tools to measure and estimate the effect of cache.

- Cache profiling
- Software tools for cache profiling

### Optimization

Learn to make best use of caches, by organising your data and by arranging the flow of execution within your programs to take best advantage of the cache and register files available.

- The memory hierarchy
- Using the register file
- Data size
- Cache lines
- Data organization
- Cache sets and ways
- Optimizing for cache ways

### Time and arrangements

This class takes 1 day.

It is presented 'on-site' by arrangement - the material can be adapted if you have specific needs (at extra cost).

Sometimes we arrange 'public' classes: schedules are posted on the Internet:

<http://www.bores.com/schedule.htm>

### DSP Foundation

For a good grounding in the basics of DSP we recommend our 4-day 'DSP Foundation' class that covers DSP, FIR and IIR filters, and C programming.

Contact us for details and advice:

[chris@bores.com](mailto:chris@bores.com)

### Booking and questions

Call us by 'phone or send email to book or to ask questions.

- contact: Dr Chris Bore
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- mobile: +44 (0)7921 153219
- email: [chris@bores.com](mailto:chris@bores.com)

### About us

BORES Signal Processing train managers, engineers and programmers to understand and use DSP and streaming media processing.

- established 17 years
- excellent reputation
- worldwide activities
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