

**Gebze Technical University
Computer Engineering**

**CSE 331
Computer Organization**

PROJECT 3 REPORT

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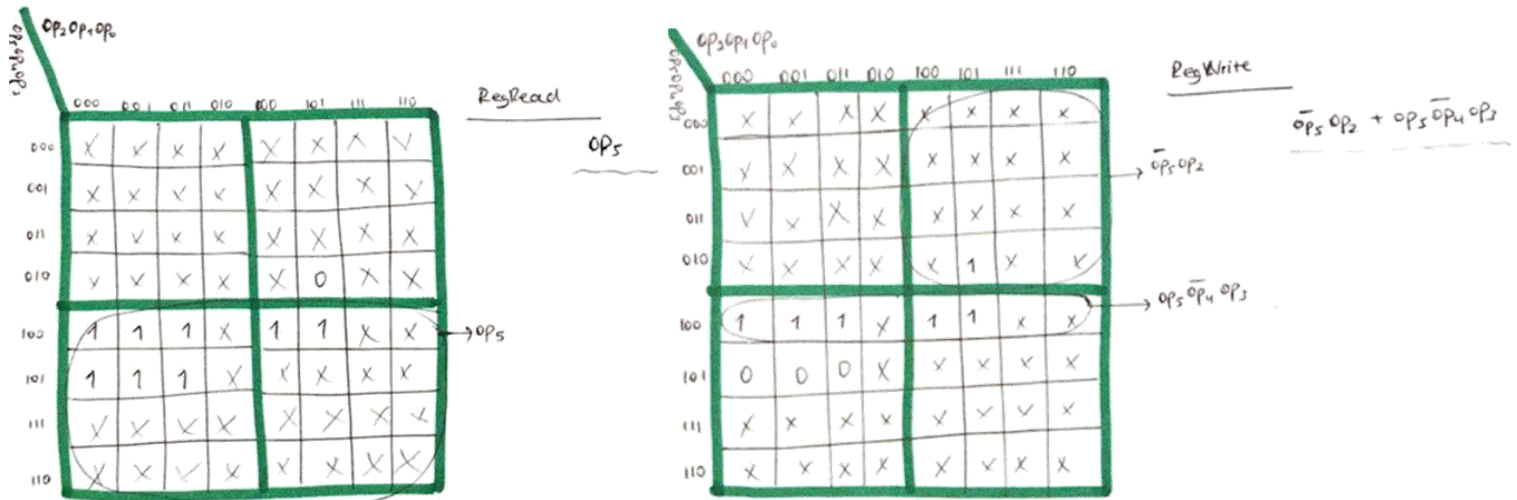
Problem Definition and Solution

In this homework, ask us to design Datapath especially 9 of I type instructions. To design these instructions, I draw two datapath, one for load and other one for store instructions. This project includes 9 modules also does not include any ALU, because of me, my design. If I will do this project correctly, I will use adder to do all the calculating operations inside of extender.v file. Also I added sign_extender and zero_extender files even I could not use them. I could not use time efficiently.

Modules and Definition

- mips32_testbench : creates clock and determines delays every instructions and reads files to arrays
- mips32 : the main file, parses instruction respect their opcode, rs, rt, immediate fields, calculates PC, calls other modules and writes some information and result on screen
- instruction_memory_block : takes instructions and PC, gives new instruction according to index which is PC
- control_unit : takes signals and calculates their value respect opcode of the instruction
- extender : takes instruction and calculates the extended value, in fact, this function should be structural with sign_extender and zero_extender files, but I could not do this type, I got some errors while calling sign_extender and zero_extender files
- sign_extender : the file added project but does not used
- zero_extender : the file added project but does not used
- data_memory_block : adds data.mem file if store instructions, reads from data.mem file if load instructions
- registers_block : updates registers.mem file if load instructions, hold the register contents if store instructions

Design of control_unit:




```
Transcript
File Edit View Bookmarks Window Help
# Loading work_data_memory_block
# Loading work_registers_block
VSM70> run -all
# PC: 0
# opcode: 000000
# rs: 00000, rs content: 00000000000000000000000000000000
# rt: 00000, rt content: 00000000000000000000000000000000
# result: 00000000000000000000000000000000
# address: 00000000000000000000000000000000
#
# PC: 1
# opcode: 100000
# rs: 00010, rs content: 00000000000000000000000000000010
# rt: 00010, rt content: 00000000000000000000000000000010
# result: 000000000000000000000000000000110
# address: 000000000000000000000000000000110
#
# PC: 2
# opcode: 100000
# rs: 00110, rs content: 000000000000000000000000000000110
# rt: 00010, rt content: 00000000000000000000000000000010
# result: 000000000000000000000000000000010
# address: 000000000000000000000000000000111
#
# PC: 3
# opcode: 100100
# rs: 00000, rs content: 00000000000000000000000000000010
# rt: 01000, rt content: 000000000000000000000000000000111
# result: 000000000000000000000000000000110
# address: 000000000000000000000000000000110
#
# PC: 4
# opcode: 100100
# rs: 00101, rs content: 00000000000000000000000000000000
# rt: 00000, rt content: 00000000000000000000000000000010
# result: 000000000000000000000000000000101
# address: 000000000000000000000000000000101
#
# PC: 5
# opcode: 100001
# rs: 00010, rs content: 000000000000000000000000000000010
# rt: 01000, rt content: 000000000000000000000000000000110
# result: 000000000000000000000000000000111
# address: 000000000000000000000000000000110
#
# PC: 6
# opcode: 100001
# rs: 00011, rs content: 000000000000000000000000000000101
# rt: 00010, rt content: 000000000000000000000000000000010
# result: 000000000000000000000000000000101
# address: 0000000000000000000000000000001000
#
# PC: 7
# opcode: 100101
# rs: 00010, rs content: 000000000000000000000000000000010
# rt: 01000, rt content: 000000000000000000000000000000110
# result: 000000000000000000000000000000010
# address: 0000000000000000000000000000001011
#
# PC: 8
# opcode: 100101
# rs: 00101, rs content: 000000000000000000000000000000000
# rt: 00000, rt content: 0000000000000000000000000000001010
# result: 0000000000000000000000000000001011
# address: 0000000000000000000000000000001010
#
# PC: 9
# opcode: 010101
# rs: 00000, rs content: 000000000000000000000000000000000
# rt: 00000, rt content: 00000000000000000000000000000001010
# result: 000000000000000000000000000000000
# address: 0000000000000000000000000000000000
#
# PC: 10
# opcode: 010101
# rs: 00001, rs content: 000000000000000000000000000000000
# rt: 00000, rt content: 0000000000000000000000000000001010
# result: 000000000000000000000000000000000
# address: 0000000000000000000000000000000000
#
# PC: 11
# opcode: 100011
# rs: 00000, rs content: 0000000000000000000000000000001010
# rt: 01000, rt content: 0000000000000000000000000000001011
# result: 000000000000000000000000000000010
# address: 0000000000000000000000000000001111
#
# PC: 12
# opcode: 100011
# rs: 00110, rs content: 000000000000000000000000000000110
# rt: 00010, rt content: 000000000000000000000000000000010
# result: 000000000000000000000000000000010
```

Here is the test results.

Parsed fields, rs and rt register's contents, the result of all the instructions, and their address in data.mem file are shown on the left side of the screen.

PS: THE .MEM FILES ARE IN MIPS32/SIMULATION/MODELSIM