OLED Smart Watch Display Driver IC Specification

ICNA3312

Specification Version

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Chipone Technology (Beijing) Co.,Ltd.

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Version	Description	Prepared By	Checked By	Date
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0.01	Update Power on off sequence	Xueling Gao	Lingguo Wang	2024/02/20

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1. Description

This purpose of this document has been created to provide complete reference specifications for the ICNA3312. Major of purpose for customers refer to these specifications for system design, quality performance control, and IC applications.

The ICNA3312 device is a single-chip with RAM display driver integration IC for LTPS AMOLED that incorporates gate drivers, a timing controller with glass interface level-shifters, and a glass power supply circuit that is capable of 540RGBx540， 480RGBx480, 454RGBx454, 400RGBx400, 390RGBx390, 360RGBx480, 360RGBx360, 340RGBx340, 320RGBx360, 320RGBx320, 320RGBx480, 300RGBx300, 272RGBx480, 240RGBx240, 240RGBx320, 192RGBx960, 180RGBx560, 180RGBx540, 180RGBx360， 128RGBx432 with internal GRAM including of a 2,332,800 bits internal memory.

The ICNA3312 supports MIPI Interface, 8-bit system interfaces, serial peripheral interfaces (SPI), dual serial peripheral interfaces (Dual-SPI), quad serial peripheral interfaces (Quad-SPI). The source resolution can be adjusted 540RGB and the gate resolution only can be set 540 lines. For the detailed resolution setting, please refer to ICNA3312 Application Note. The specified GRAM window area can be updated selectively, so that moving pictures can be displayed simultaneously independent of the still picture area.

The ICNA3312 is also able to make gamma correction settings separately for RGB dots to allow benign adjustments to panel characteristics, resulting in higher display qualities. ICNA3312 includes internal boosters that generate the AMOLED driving voltage, breeder resistance and voltage follower circuit for the AMOLED driver. ICNA3312 possesses internal GRAM with compression IP that stores 540 x 540 x 1/3 x 24 bits for 16.7M-color images. A deep standby mode is also supported for lower power consumption.

The ICNA3312 also supports ACL function for the AMOLED brightness control. It's able to reduce the total power consumption of display module significantly and keep AMOLED life time.

This LSI is suitable for wearable device applications, including watch and smart band.

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2. Features

- **Single chip wearable device AMOLED controller/driver with internal RAM**
- **Display Resolution support. For detail settings, need to check Application Note**
  - 540RGB x 540 (1:9 Multiplexer for source driver)
  - 480RGB x 480 (1:6/1:9/1:12 Multiplexer for source driver)
  - 454RGB x 454 (1:6/1:12 Multiplexer for source driver)
  - 400RGB x 400 (1:6/1:12 Multiplexer for source driver)
  - 390RGB x 390 (1:6/1:12 Multiplexer for source driver)
  - 360RGB x 480 (1:6/1:9/1:12 Multiplexer for source driver)
  - 360RGB x 360 (1:6/1:12 Multiplexer for source driver)
  - 340RGB x 340 (1:6/1:12 Multiplexer for source driver)
  - 320RGB x 360 (1:6/1:12 Multiplexer for source driver)
  - 320RGB x 320 (1:6/1:12 Multiplexer for source driver)
  - 320RGB x 480 (1:6/1:12 Multiplexer for source driver)
  - 300RGB x 300 (1:6/1:12 Multiplexer for source driver)
  - 272RGB x 480 (1:6/1:12 Multiplexer for source driver)
  - 270RGB x 270 (1:6/1:9/1:12 Multiplexer for source driver)
  - 240RGB x 240 (1:6/1:12 Multiplexer for source driver)
  - 240RGB x 320 (1:6/1:12 Multiplexer for source driver)
  - 192RGB x 960 (1:6/1:9/1:12 Multiplexer for source driver)
  - 180RGB x 560 (1:6/1:12 Multiplexer for source driver)
  - 180RGB x 540 (1:6/1:12 Multiplexer for source driver)
  - 128RGB x 432 (1:6/1:12 Multiplexer for source driver)

- **Display data RAM (frame memory): 2,332,800 bits**

- **Display mode (Color mode)**
  - Full color mode: 16.7M-colors
  - Reduced Color Mode: 262K-colors
  - Reduced Color Mode: 65K-colors
  - Supported Normal/Idle Display Mode
  - Normal mode: 16.7M-colors, 262K-colors, 65K-colors
  - Idle mode: 16.7M-colors, 4096-colors, 8-colors

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Interface

- MIPI DSI Interface (D-PHY: V1.0 , DSI:1.01.00, DCS:1.01.00)

  MIPI I/F Supported 2 data lanes (Lane numbers are selected by register xxh of CMD2 in MIPI LP mode, and this register can be programmed by MTP)

  - Support 1lane/2lane (1lane/2lane: 900Mbps)
  - Support two MIPI PORTS, control by MIPI_SEL from Hardware

    0: select MIPI1; 1:select MIPI2
  - Support switching between two ports when 1 lane

    Swap port @lp11 or Swap port @lp00
  - Support one port of two lanes(default 1lane)
  - Maximum total bit rate is 900Mbps with 24-bit data format, 700Mbps with 18-bit data format, 620Mbps with 16-bit data format
- Serial peripheral interface (SPI)
- Dual serial peripheral interface (Dual-SPI)
- Quad serial peripheral interface (Quad-SPI)
- Quad-SPI DDR (1swire: 65Mbps)

Display Feature

- Individual gamma correction settings for RGB dots
- Partial display function

On chip

- DC/DC converter
- Supports control signals (VSR_L[16:1], VSR_R[16:1],) to gate driver in the AMOLED panel
- Internal Oscillator for display clock generation
- On module checksum checking
- Sunlight readable technology
- VREFP5/VREFN5/VREFN5_2 voltage generator for panel voltage
- VGHR1/VGLR1/VGHR2/VGLR2 voltage for gate control signal
- Source output MUX[6:1]/MUX[9:1]/MUX[12:1] with 240/180/120ch source output pins
- Supports gate control signals to gate driver in the panel

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- **Built-in OTP function to adjust panel setting**
  - Provide MTP (2 times) to store related Power, GOA timing, Gamma1~8 settings
  - Provide MTP (3 times) to store ID1, ID2, ID3, DDB

- **Self-Diagnostic Function**
  - ESD detection
  - Low Voltage Detection

- **Control power IC by one-wire interface(S-Wire Control)**

- **Supply Voltage Range**
  - Logic / interface power supply voltage VDDI = 1.65V ~ 3.3V
  - Analog power supply voltage VCI = 2.7V ~ 3.6V
  - Logic / interface power supply voltage VDDD = 1.2V±50mV

- **Output voltage levels**
  - Positive gate driver voltage range for VGHR1/VGHR2: 3V ~ 12V, step 0.2V
  - Negative gate driver voltage range for VGLR1/VGLR2: -2V ~ -12V, step 0.2V
  - VREFP panel voltage range: 0V, 0.5~5.5V, step 0.05V (Max<=AVDD-0.3V)
  - VREFN/VREFN_2 panel voltage range:0V, -0.5~-5V, step 0.05V (Min>=VCL+0.3V)
  - Step-up 1,2 output voltage range for

    AVDD: 4.0 ~ 6.0V, step 0.1V; VCL: -3.5 ~ -5.5V, step 0.5V
  - Gamma high/low voltage range for

    VGMP: 2.0V ~ 5.8V (Max<=AVDD-0.2V), step 10.0mV , VGSP: 0V, 0.2V ~ 4.5V, step 10.0mV

- **Package: COF/COP**

- **Chip size evaluation : 8218um x 1556um(including scribe line)**

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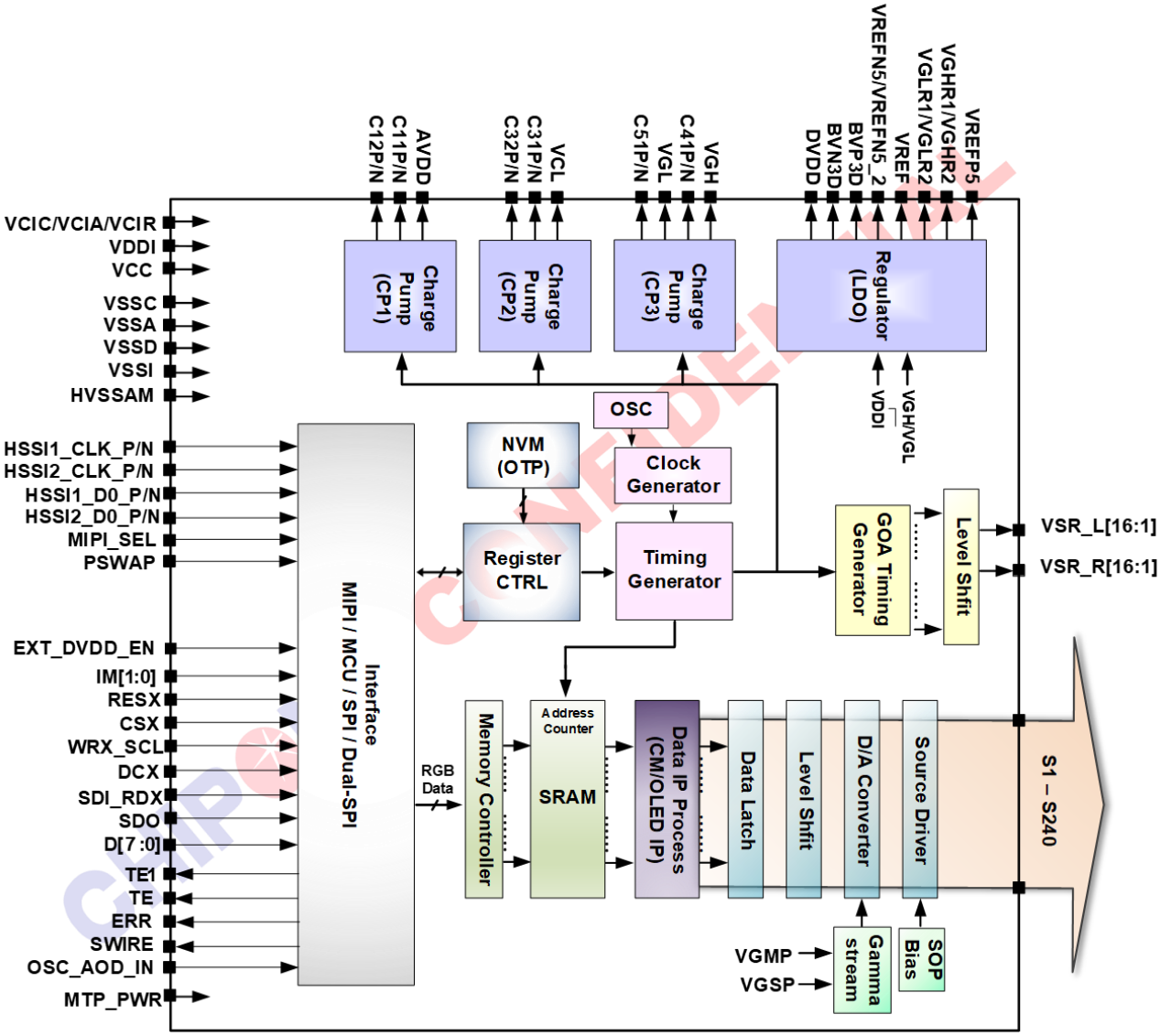
3. Device Overview

3.1 Block diagram

ICNA3312 Block diagram



4. Pin Description

4.1 Pins for Power Input

Symbol	I/O Type	Description
VCIC	Power Supply	- Power supply to DCDC power for DDIC use. - It can be supported by “external PMIC”. - VCIC= 2.7V ~ 3.6V. - VCIC, VCIA, VCIR should be the same input voltage level to system VCI.
VCIA	Power Supply	- Power supply to analog power for DDIC use. - It can be supported by “external PMIC”. - VCIA= 2.7V ~ 3.6V. - VCIC, VCIA, VCIR should be the same input voltage level to system VCI.
VCIR	Power Supply	- Power supply to LDO for DDIC use. - It can be supported by “external PMIC”. - VCIR= 2.7V ~ 3.6V. - VCIC, VCIA, VCIR should be the same input voltage level to system VCI.
VDDI	Power Supply	- Power supply to I/O. - VDDI= 1.65V ~ 3.3V.
VCC	Power Supply	- Power supply for DVDD regulator. - In case of COF, connect VCC to VDDI on the FPC.
VSSC	Power GND	- Ground for DC/DC converter. VSSC=0V.
VSSA	Power GND	- Ground for analog system. VSSA=0V. - In case of COF, connect VSSA to VSS on the FPC to prevent noise.
HVSSAM	Power GND	- Ground for MIPI interface. - In case of COF, connect HVSSAM to system VSS on the FPC to prevent noise.
VSSI	Power GND	- Ground for I/O except MIPI interface. - In case of COF, connect VSSI to system VSS on the FPC to prevent noise.
VSSD	Power GND	- Ground for internal digital system. VSSD=0V. - In case of COF, connect VSSD to system VSS on the FPC to prevent noise.
MTP_PWR	Power Supply	- MTP programming power supply pin. (6.0V typical) - Must be left open or connected to VSSD in normal condition.

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4.2 Pins for MPU and SPI Interface

Symbol	I/O Type	Description
CSX	Digital Input (VDDI - VSSI)	- Chip select input pin (“Low” enable) in 80-series MPU I/F and SPI I/F. - If not used, please connect to VDDI.
WRX_SCL	Digital Input (VDDI - VSSI)	- WRX: Writes strobe signal to write data when WRX is “Low” in 80-series MPU I/F. - SCL: A synchronous clock signal in SPI I/F. - If not used, please connect to VSSI.
D/CX	Digital Input (VDDI - VSSI)	- Display data / command selection in 80-series MPU I/F and 4-wire SPI I/F. D/CX = ”0” : Command D/CX = ”1” : Display data or Parameter - If not used, please connect to VSSI.
SDI_RDX	Digital I/O (VDDI - VSSI)	- SDI: Serial input signal in SPI I/F. The data is input on the rising edge of the SCL signal. - RDX: Reads strobe signal to write data when RDX is “Low” in 80-series MPU interface. - If not used, please open this pin.
SDO	Digital Output (VDDI - VSSI)	- Serial output signal in SPI I/F. The data is output on the rising/falling edge of the SCL signal. If the host places the SDI line into high-impedance state during the read interval, the SDI and SDO can be tied together. - If not used, please open this pin.
D[7:0]	Digital I/O (VDDI - VSSI)	- 8-bit bi-directional data bus for 80-series MPU I/F and 8-bit input data bus for RGB I/F. - These pins are not used for SPI, MIPI, please open this pin.

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4.3 Pins for MIPI Interface

<table>
<tr><th>Symbol</th><th>I/O Type</th><th>Description</th></tr>
<tr><td>HSSI1_CLK_P
HSSI1_CLK_N</td><td>MIPI Input</td><td>- DSI CLK+/- differential clock signals.
- HSSI1_CLK_P/N are differential signals. To be ensure the trace length is shortest so that COF and FPC resistance is less than 10 Ohm.
- For MIPI I/F, please pull HSSI1_CLK_P/N to LP-00 or VSSI when enter deep standby mode.
- If not used, please connect these pins to HVSSAM.</td></tr>
<tr><td>HSSI2_CLK_P
HSSI2_CLK_N</td><td>MIPI Input</td><td>- DSI CLK+/- differential clock signals.
- HSSI2_CLK_P/N are differential signals. To be ensure the trace length is shortest so that COF and FPC resistance is less than 10 Ohm.
- For MIPI I/F, please pull HSSI2_CLK_P/N to LP-00 or VSSI when enter deep standby mode.
- If not used, please connect these pins to HVSSAM.</td></tr>
<tr><td>HSSI1_D0_P
HSSI1_D0_N</td><td>MIPI I/O</td><td>- DSI D0+/- differential clock signals.
- HSSI1_D0_P/N are differential signals. To be ensure the trace length is shortest so that COF and FPC resistance is less than 10 Ohm.
- For MIPI I/F, please pull HSSI1_D0_P/N to LP-00 or VSSI when enter deep standby mode.
- If not used, please connect these pins to HVSSAM.</td></tr>
<tr><td>HSSI2_D0_P
HSSI2_D0_N</td><td>MIPI I/O</td><td>- DSI D0+/- differential clock signals.
- HSSI2_D0_P/N are differential signals. To be ensure the trace length is shortest so that COF and FPC resistance is less than 10 Ohm.
- For MIPI I/F, please pull HSSI2_D0_P/N to LP-00 or VSSI when enter deep standby mode.
- If not used, please connect these pins to HVSSAM.</td></tr>
<tr><td>MIPI_SEL</td><td>Digital Input
(VDDI - VSSI)</td><td>- Input pin to select HSSI1_D0/HSSI2_D0 data lane sequence and polarity in high speed interface only.
<table>
<tr><th colspan="2">Pin Name</th><th>HSSI2 _D0_P</th><th>HSSI2 _D0_N</th><th>HSSI2 _CLK_P</th><th>HSSI2 _CLK_N</th><th>HSSI1 _CLK_P</th><th>HSSI1 _CLK_N</th><th>HSSI1 _D0_P</th><th>HSSI1 _D0_N</th></tr>
<tr><td rowspan="2">MIPI_SEL=0</td><td>PSWAP=0</td><td>Host Keep LP11 or enter ULPS</td><td>Host Keep LP11 or enter ULPS</td><td>Host Keep LP11 or enter ULPS</td><td>Host Keep LP11 or enter ULPS</td><td>DSI CLK+</td><td>DSI CLK-</td><td>DSI D0+</td><td>DSI D0-</td></tr>
<tr><td>PSWAP=1</td><td>Host Keep LP11 or enter ULPS</td><td>Host Keep LP11 or enter ULPS</td><td>Host Keep LP11 or enter ULPS</td><td>Host Keep LP11 or enter ULPS</td><td>DSI CLK-</td><td>DSI CLK+</td><td>DSI D0-</td><td>DSI D0+</td></tr>
<tr><td rowspan="2">MIPI_SEL=1</td><td>PSWAP=0</td><td>DSI D0+</td><td>DSI D0-</td><td>DSI CLK+</td><td>DSI CLK-</td><td>Host Keep LP11 or enter ULPS</td><td>Host Keep LP11 or enter ULPS</td><td>Host Keep LP11 or enter ULPS</td><td>Host Keep LP11 or enter ULPS</td></tr>
<tr><td>PSWAP=1</td><td>DSI D0-</td><td>DSI D0+</td><td>DSI CLK-</td><td>DSI CLK+</td><td>Host Keep LP11 or enter ULPS</td><td>Host Keep LP11 or enter ULPS</td><td>Host Keep LP11 or enter ULPS</td><td>Host Keep LP11 or enter ULPS</td></tr>
</table>
- If not used, please connect to VSSI.</td></tr>
</table>

NOTE: "1" = VDDI level, "0" = VSSI level.

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4.4 Pins for Interface Logic Control

<table>
<tr><th>Symbol</th><th>I/O Type</th><th>Description</th></tr>
<tr><td>RESX</td><td>Digital Input
(VDDI - VSSI)</td><td>- This signal will reset the device and must be applied to properly initialize the chip. Signal is active low.
- There is no internal pull high resistor for this pin.</td></tr>
<tr><td>IM[1:0]</td><td>Digital Input
(VDDI - VSSI)</td><td>- Interface type selection. The connections of IM[1:0] which not shown in table are invalid.
<table>
<tr><th>IM[1:0]</th><th>Display Data</th><th>Command</th></tr>
<tr><td>00</td><td>MIPI / 3-wire SPI</td><td>MIPI / 3-wire SPI</td></tr>
<tr><td>01</td><td>MIPI / 4-wire SPI</td><td>MIPI / 4-wire SPI</td></tr>
<tr><td>10</td><td>MIPI / QUAD-SPI</td><td>MIPI / QUAD-SPI</td></tr>
<tr><td>11</td><td>MCU 8-bit</td><td>MCU 8-bit</td></tr>
</table></td></tr>
<tr><td>OSC_AOD_IN</td><td>Digital Input
(VDDI - VSSI)</td><td>- The oscillator input of self-clock function for AOD mode. (crystal oscillator= 32.768kHz)
- If not used, please connect to VSSI.</td></tr>
<tr><td>TE</td><td>Digital Output
(VDDI - VSSI)</td><td rowspan="2">- Tearing effect output pin to synchronize MCU to frame writing, activated by S/W command.
- When this pin is not activated, this pin is output low.
- If not used, please open this pin.</td></tr>
<tr><td>TE1</td><td>Digital Output
(VDDI - VSSI)</td></tr>
<tr><td>SWIRE</td><td>Digital Output
(VDDI - VSSI)</td><td>- Swire protocol setting pin of Power IC, If not used, please open this pin.</td></tr>
<tr><td>ERR</td><td>Digital Output
(VDDI - VSSI)</td><td>- Output pin used to monitor display driver state and error status, If not used, please open this pin.</td></tr>
<tr><td>EXT_DVDD_EN</td><td>Digital Input
(VDDI - VSSI)</td><td>- This signal use for 3 power mode ,if used,please connect to VDDI.
- If not used, please open this pin or connect to VSSI.</td></tr>
</table>

NOTE: "1" = VDDI level, "0" = VSSI level.

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4.5 Pins for Analog Output of OLED Display Driving

Symbol	I/O Type	Description
S1 ~ S240	Analog Output	- OLED pixel electrode driving output. - If not used, please keep these pins floating.
DMY[48:1]	N.A.	- These pins are used dummy for GOA Film routing on the COF. - If not used, please keep these pins floating.
DUMMY_R[13:1] DUMMY_L[13:1]	N.A.	- These pins are used source dummy. - If not used, please keep these pins floating.
VSR_L[16:1] VSR_R[16:1]	Analog Output (VGHR - VGLR)	- These pins are used OLED panel control signal. - If not used, please keep these pins floating.

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4.6 Pins for DC/DC Convert Pins

Symbol	I/O Type	Description
AVDD	CP Output	- Output voltage from step-up circuit 1, generated from VCIC. - Connect a capacitor for stabilization.
VCL	CP Output	- Output voltage from step-up circuit 4, generated from VCIC. - Connect a capacitor for stabilization.
VGH	CP Output	- Output voltage from step-up circuit 2. - Connect a capacitor for stabilization.
VGL	CP Output	- Output voltage from step-up circuit 3. - Connect a capacitor for stabilization.
C11P, C11N C12P, C12N	Analog Output	- Capacitor connection pins for the step-up circuit which generate AVDD. - Connect capacitor as requirement. When not in used, please open these pins.
C41P, C41N C42P, C42N	Analog Output	- Capacitor connection pins for the step-up circuit which generate VCL. - Connect capacitor as requirement.
C21P, C21N	Analog Output	- Capacitor connection pins for the step-up circuit which generate VGH. - Connect capacitor as requirement.
C31P, C31N	Analog Output	- Capacitor connection pins for the step-up circuit which generate VGL. - Connect capacitor as requirement.
VGHR1/VGHR2	LDO Output	- Output voltage generated from VGH. LDO output used for panel voltage. - Connect a capacitor for stabilization. - When not in use, please open this pin.
VGLR1/VGLR2	LDO Output	- Output voltage generated from VGL. LDO output used for panel voltage. - Connect a capacitor for stabilization. - When not in use, please open this pin.
VGMP	LDO Output	- Output voltage generated from AVDD. LDO output for positive gamma high voltage generator.
VGSP	LDO Output	- Output voltage generated from AVDD. LDO output for positive gamma low voltage generator.
VREF	LDO Output	- LDO output for internal reference voltage. - Connect capacitor for stabilization.
DVDD	LDO Output	- LDO output for logic system power. - Connect a capacitor for stabilization.
VREFP5	LDO Output	- LDO output used for OLED panel display. - Connect a capacitor for stabilization.
VREFN5/ VREFN5_2	LDO Output	- LDO output used for OLED panel display. - Connect a capacitor for stabilization.
BVP3D (I_ELVDD)	LDO Output	- Positive output voltage generated from AVDD. LDO output used for OLED panel display. Connect a capacitor for stabilization. When not in use,

		please open this pin. - Connect a capacitor for stabilization.
BVN3D (I_ELVSS)	**LDO Output**	- Negative output voltage generated from VCL. LDO output used for OLED panel display Connect a capacitor for stabilization. When not in use, please open this pin. - Connect a capacitor for stabilization.
VREFX	**LDO Output**	- Output for VREFN5 or VREFP5

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4.7 Test Pins

Symbol	I/O Type	Description
ANALOG_TEST[2:1]	Analog Output	- Test pin, must be left open. - ANALOG_TEST1 (AVDD --- VSSA) - ANALOG_TEST2 (VSSA --- VCL)
PCD_DET	Anolog Input	- Panel crack detect pin, If not used, please open this pin.
TEST1~3	Digital I/O	- Test pin, must be left open.
TESTEN	Digital Input	- Test pin, must be tied low by COF or FPC.
EXTCLK	Digital Input	- Test pin, must be left open.
DUMMY_C1[48:1] DUMMY_C2[48:1] DUMMY_R1*2 DUMMY_R2*2 DUMMY_R3*2 DUMMY_R4*2	N.A.	- Dummy PAD, must be left open.

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5. Function Description

5.1 Interface Selection

The ICNA3312 provides Interface type selection, which is determined by hardware connection pins of IM[1:0] as shown in table are below.

IM[1:0]	Display Data	Command
00	MIPI / 3-wire SPI	MIPI / 3-wire SPI
01	MIPI / 4-wire SPI	MIPI / 4-wire SPI
10	MIPI / QUAD-SPI	MIPI / QUAD-SPI
11	MCU 8-bit	MCU 8-bit

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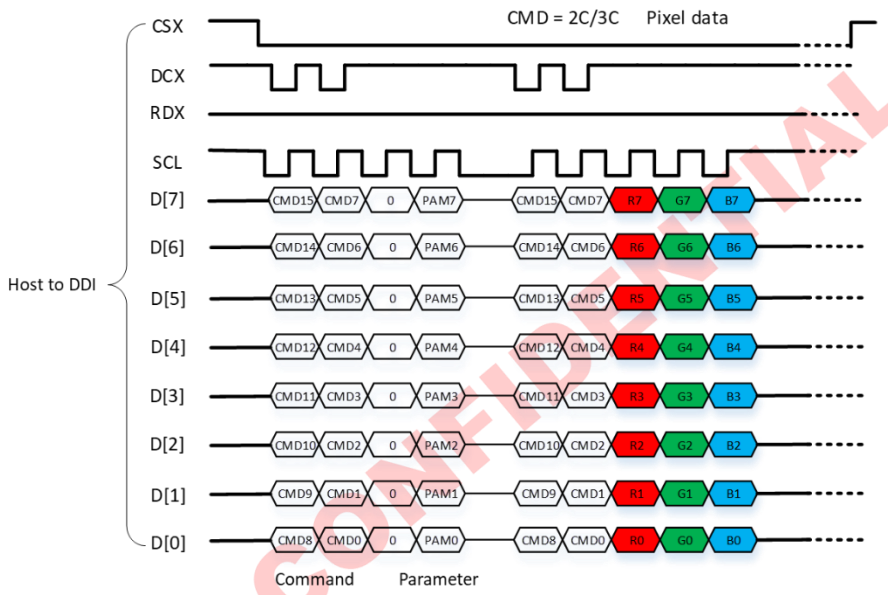
5.2 MCU Interface

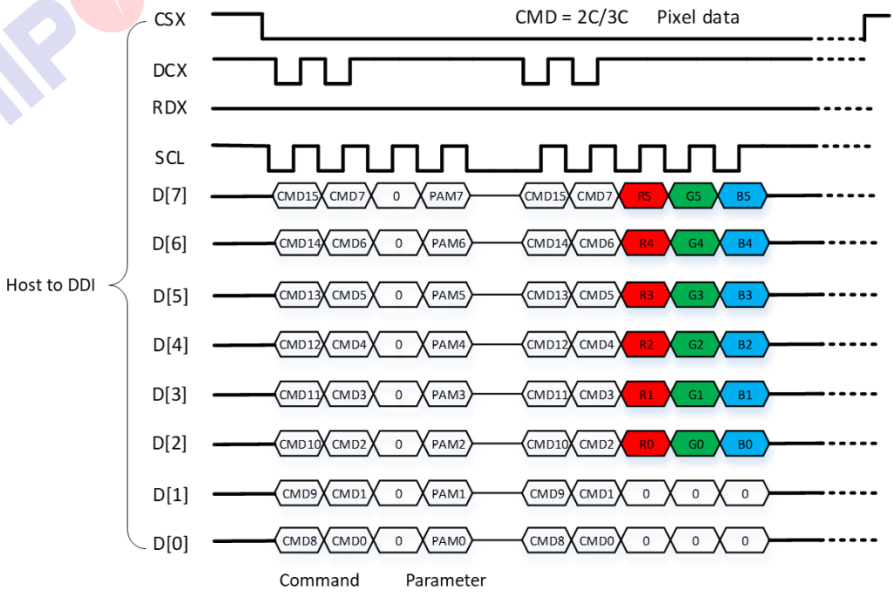
5.2.1 Write Cycle and Sequence

The MCU interface utilizes 12-wire 8-bit data for parallel transmission, including CSX, DCX, RDX, SCL and D[7:0] signals. The CSX (active low) enables and disables the parallel interface. SCL is driven from high to low then pulled back to high during the write cycle. The DDIC captures host processor command and data on the rising edge of SCL.

The IFPF (0x3A00) defines the pixel format of the MCU interface, which is configured as 7: **RGB888**



The IFPF (0x3A00) defines the pixel format of the MCU interface, which is configured as 6: **RGB666**



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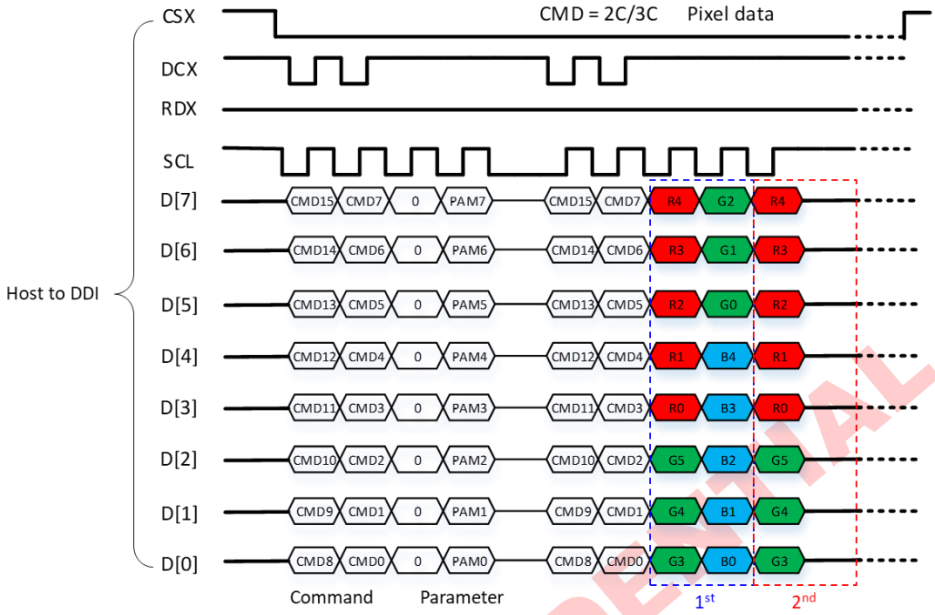
The IFPF (0x3A00) defines the pixel format of the MCU interface, which is configured as 5: **RGB565**



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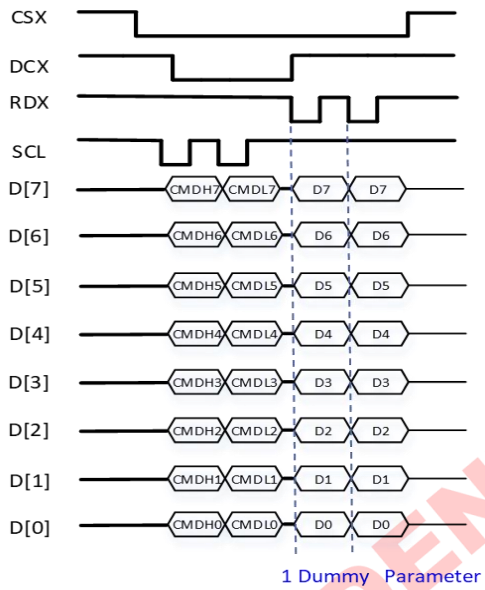
5.2.2 MCU Read Cycle and Sequence

The following read cycle (RDX high-low-high sequence) specifies the timing for the host to read command and data from the display module through the MCU interface.



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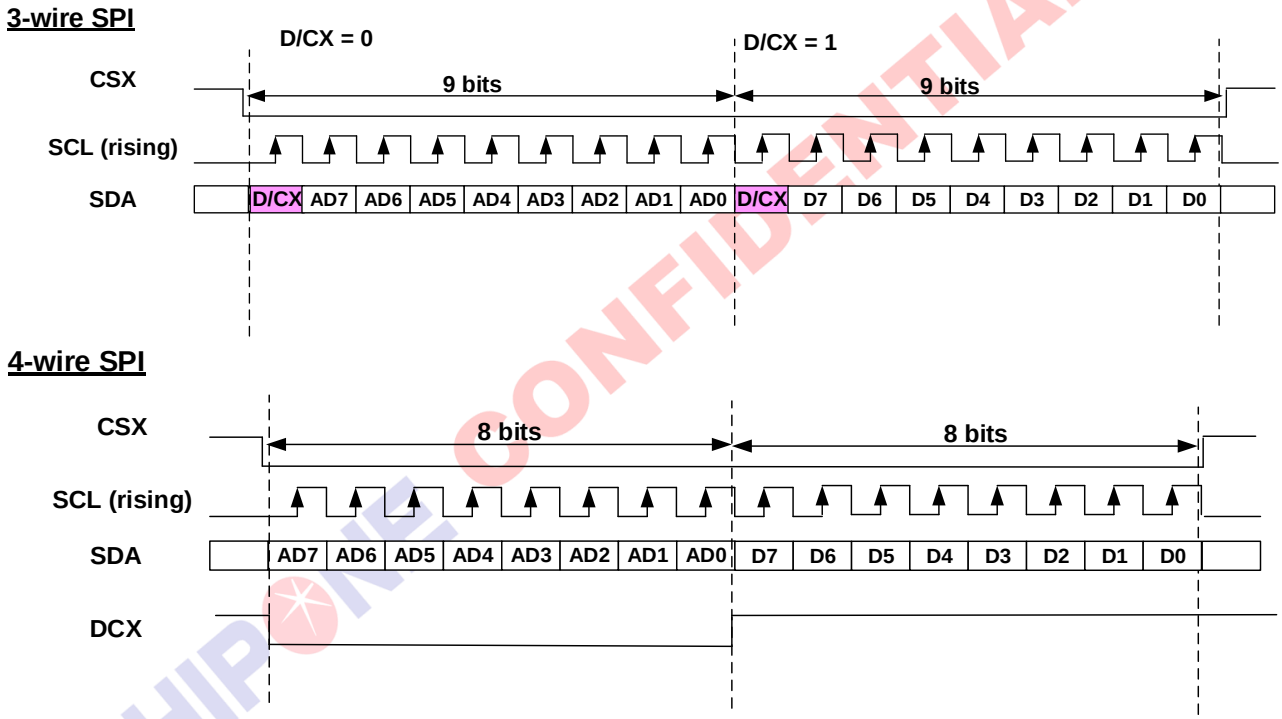
5.3 3-wire/4-wire SPI Interface

The ICNA3312 supports 3-wire/4-wire SPI interface. (Refer to the below figures)

5.3.1 Write Cycle and Sequence

The 3-wire/4-wire SPI interface utilizes DCX, CSX, SCL and SDA signals. SCL is driven from high to low then pulled back to high during the write cycle. The host processor provides information during the write cycle while the display module reads the host processor information on the rising edge of SCL.

The 3-wire/4-wire SPI interface write command sequences are described in the following figure as below.



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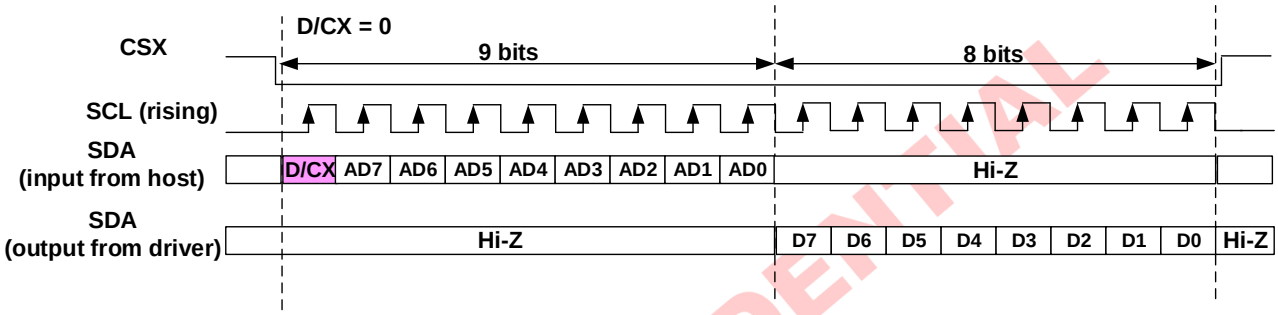
5.3.2 Read Cycle and Sequence

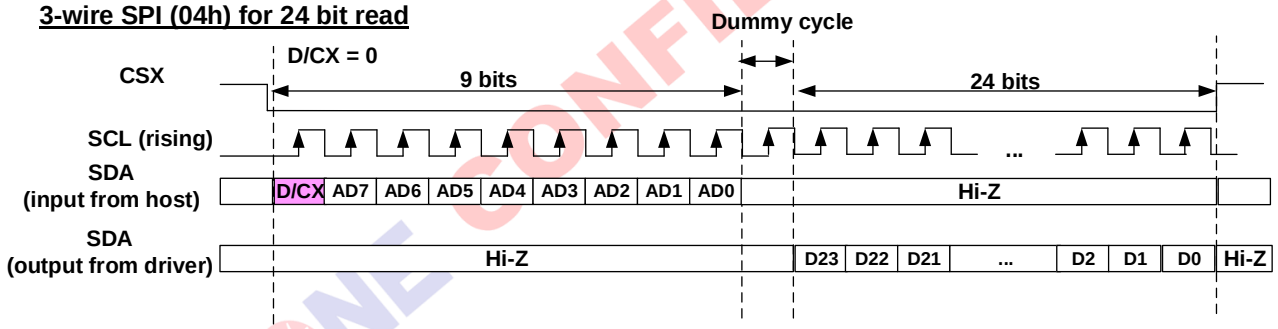
The 3-wire/4-wire SPI interface utilizes DCX, CSX, SCL and SDA signals. SCL is driven from high to low then pulled back to high during the read cycle. The host processor provides information during the read cycle while the display module reads the host processor information on the rising edge of SCL.

The 3-wire/4-wire SPI interface read command sequences are described in the following figure as below.

3-wire SPI (05h/0Ah/0B/0Ch/0Dh/0Eh/0Fh/52h/54h/56h/59h/64h/ AAh/AFh/DAh/DBh/DCh/E1h/E2h/E3h) for 8 bit read



3-wire SPI (04h) for 24 bit read



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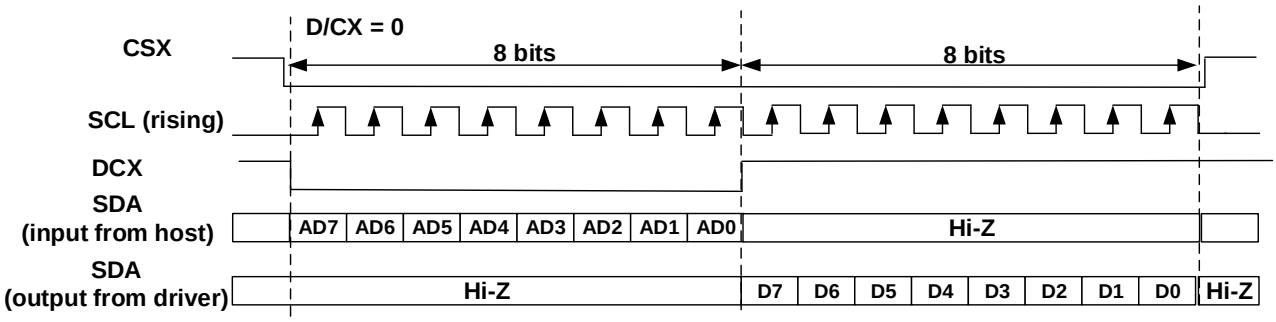
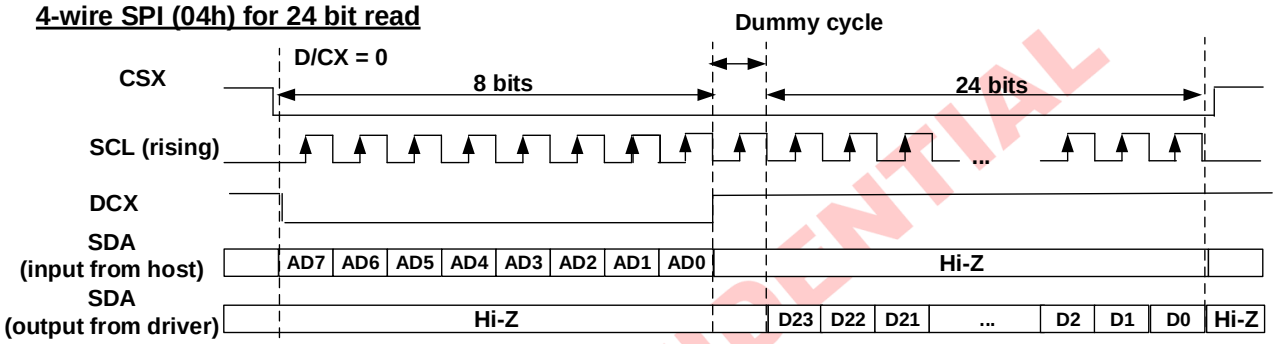
4-wire SPI (05h/0Ah/0B/0Ch/0Dh/0Eh/0Fh/52h/54h/56h/59h/64h/ AAh/AFh/DAh/DBh/DCh/E1h/E2h/E3h) for 8 bit read



4-wire SPI (04h) for 24 bit read



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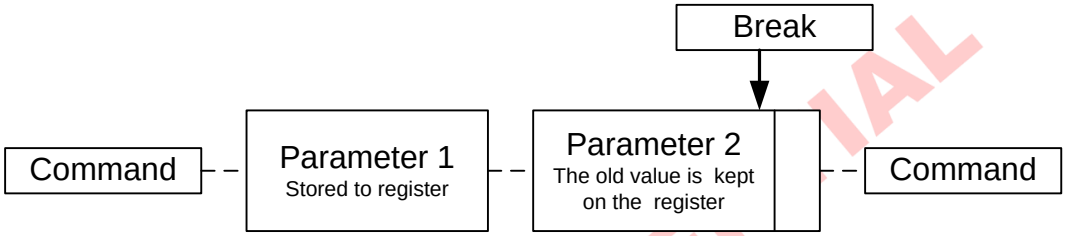
5.3.3 Break and Pause Sequence

The host processor can break a read or write sequence by pulling the CSX signal high during a command or data byte. The display module shall reset its interface so it will be ready to receive the same byte when CSX is again driven low.

The host processor can pause a read or write sequence by pulling the CSX signal high between command or data bytes. The display module shall wait for the host processor to drive CSX low before continuing the read or write sequence at the point where the sequence was paused.

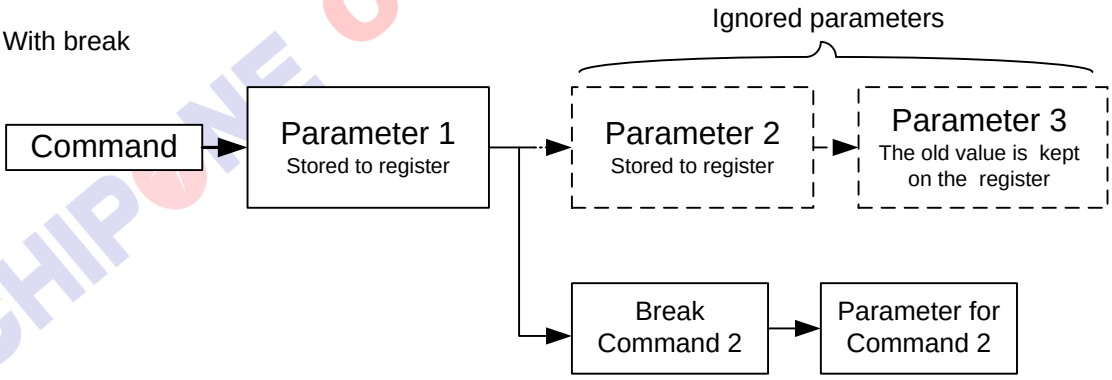
1. Middle of frame



2. Between frames

Without break

With break



Break can be e.g. another command or noise pulse.

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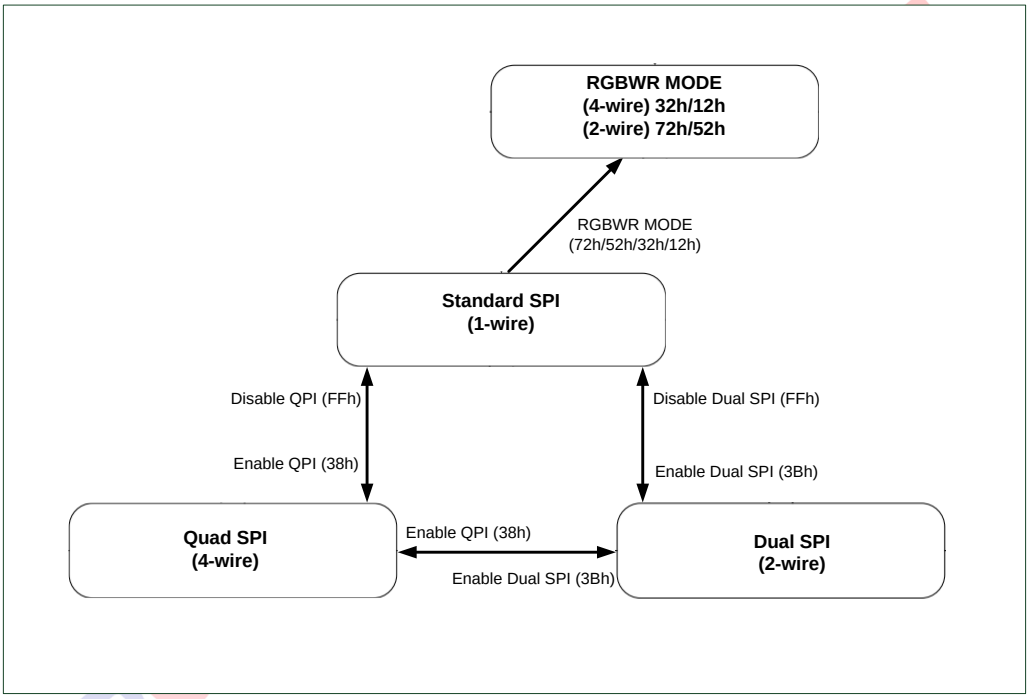
5.4 QUAD SPI Interface

ICNA3312 would support QUAD SPI interface (Refer to the below figures). QUAD SPI provides 1-wire for writing / reading command, and 4-wire for writing pixel data. CSX is the chip selection and it is low active property. SCL is driven from high to low then pulled back to high during the write cycle. The host processor provides information during the write cycle while the display module reads the host processor information on the rising edge of SCL.

5.4.1 **QUAD SPI command format**

The QUAD SPI interface contains three operating modes, Standard SPI, Dual SPI and Quad SPI. These modes structure as below.



The QUAD SPI interface instruction code as below:

Instruction code	Description
0xFF	Reset dual & quad SPI to single SPI
0x3B	Enter dual SPI
0x38	Enter quad SPI
0x02	Command / pixel write
0x03	Command / pixel read
0x32	4-wire pixel write (address: 24clk)
0x12	4-wire pixel write (address: 6clk)
0x72	2-wire pixel write (address: 24clk)
0x52	2-wire pixel write (address: 12clk)

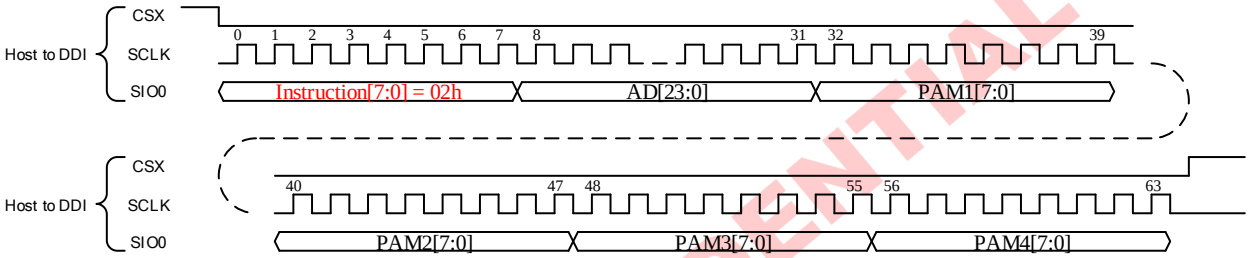
5.4.2 Write Cycle and Sequence

The QUAD SPI interface write command sequences are described in the following figure as below.

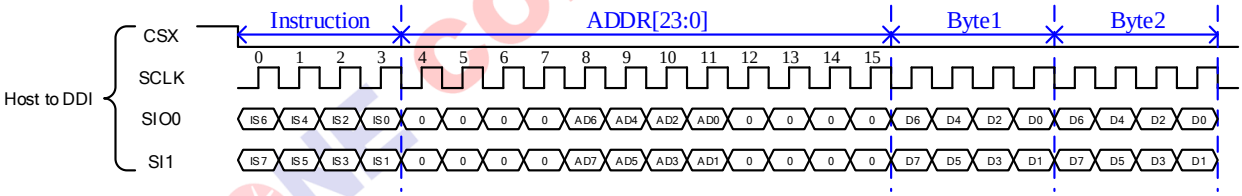
QSPI write protocol contain as below：

Instruction[7:0] = 02h	Command write
AD[23:0] = {8'h00, CMD[7:0], 8'h00}	Driver IC command address
PAM[7:0]	Driver IC parameters

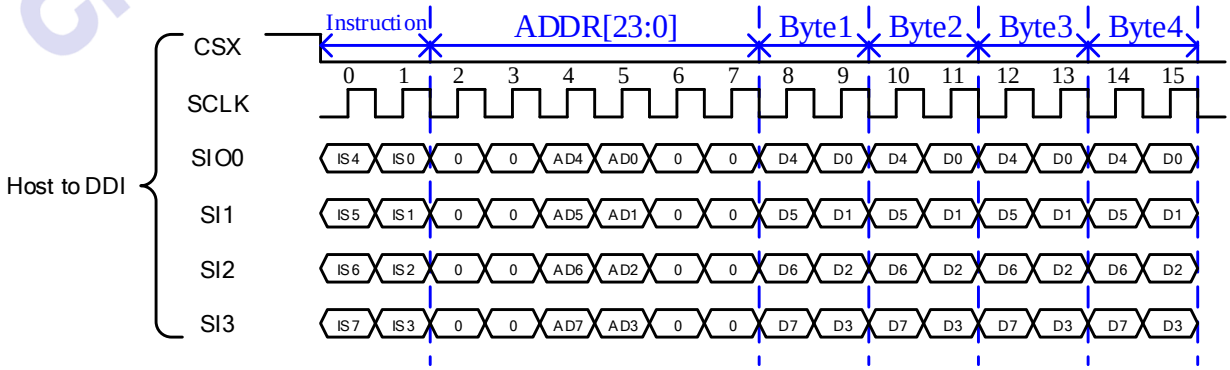
QSPI 1-wire write



QSPI 2-wire write



QSPI 4-wire write



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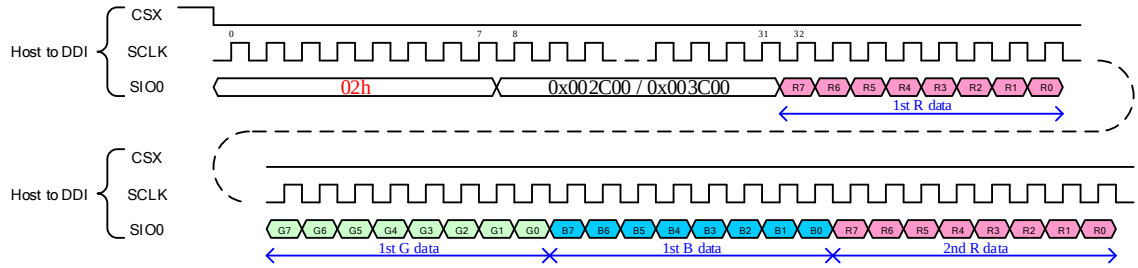
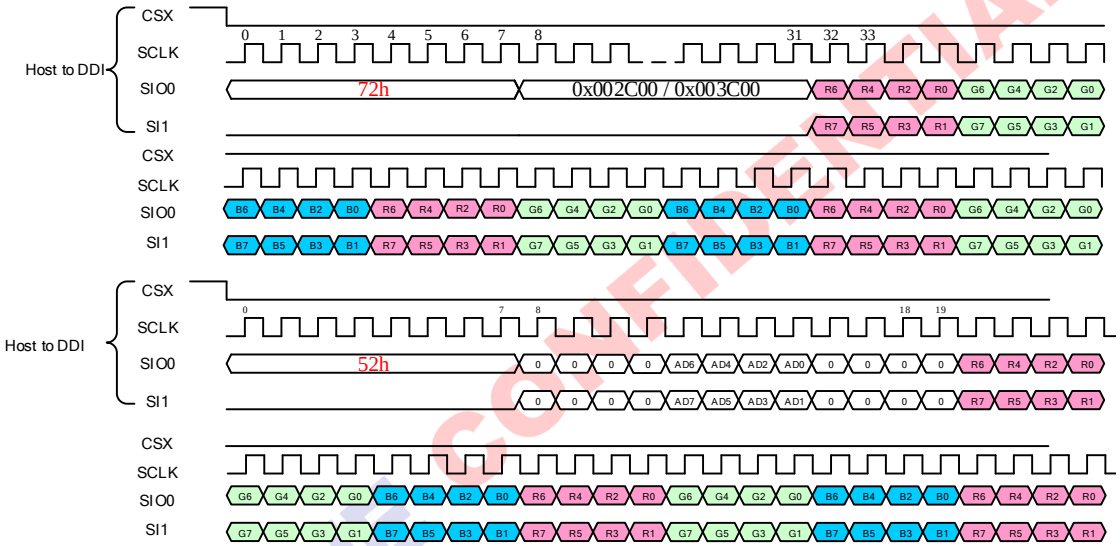
The QUAD SPI interface supports different display data formats with six color depths, RGB888, RGB666, RGB565, RGB332, RGB111, GRAY256.

RGB888:

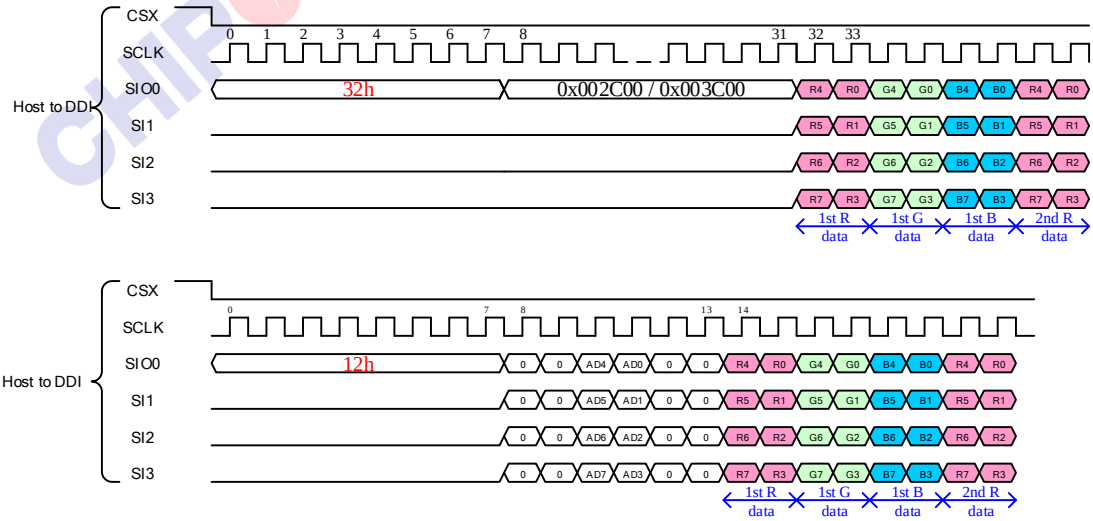
1-wire



2-wire



4-wire



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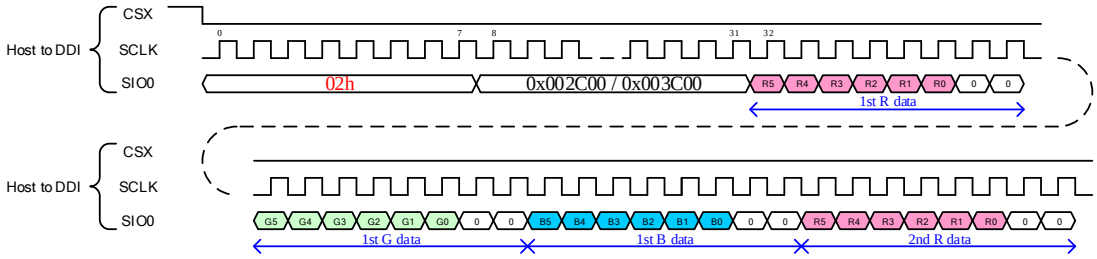
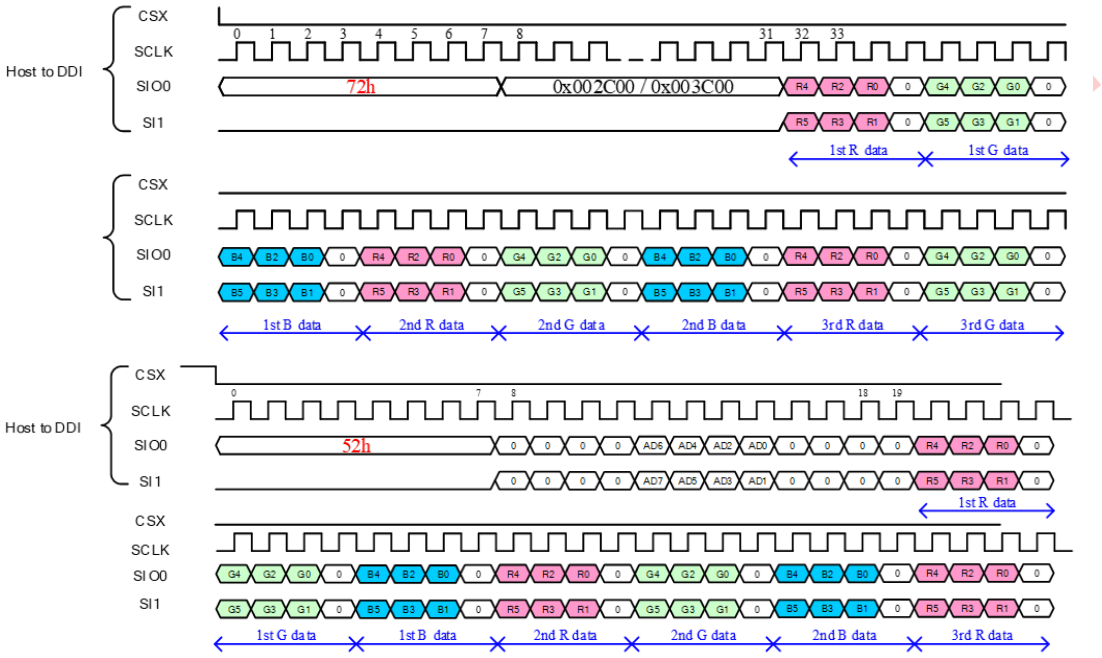
RGB666:

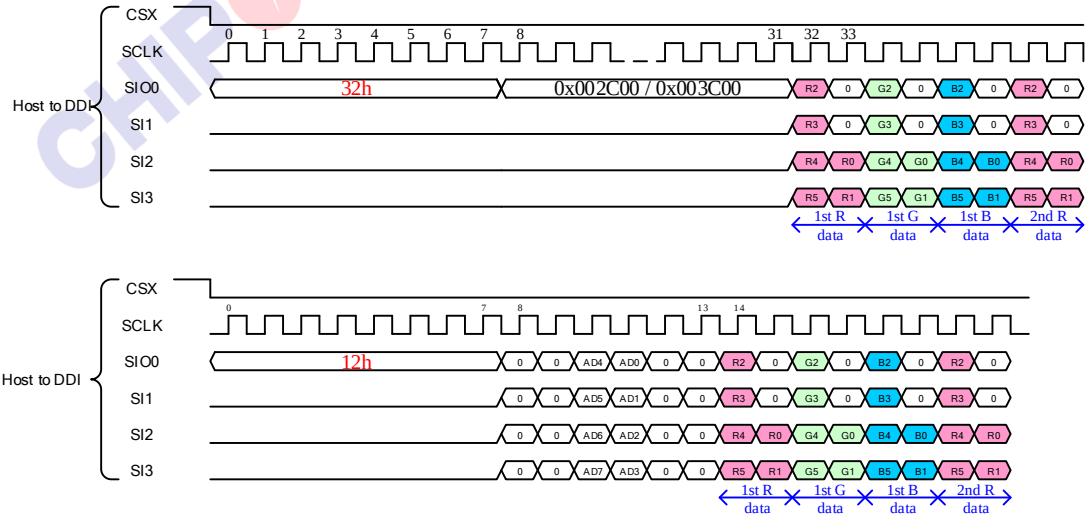
1-wire



2-wire

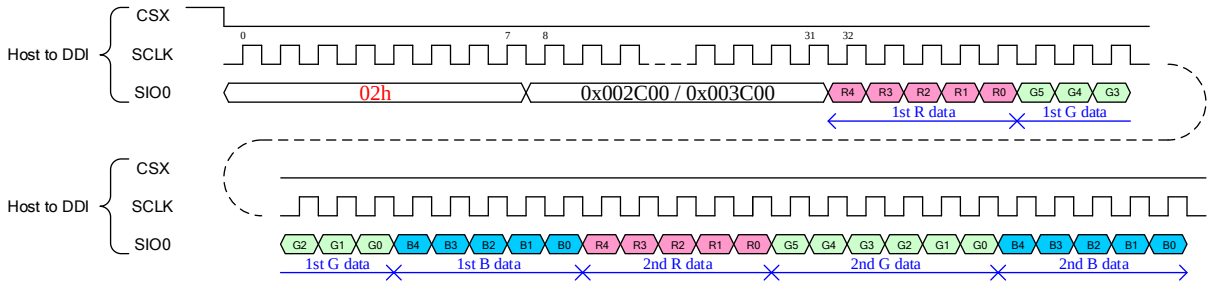


4-wire

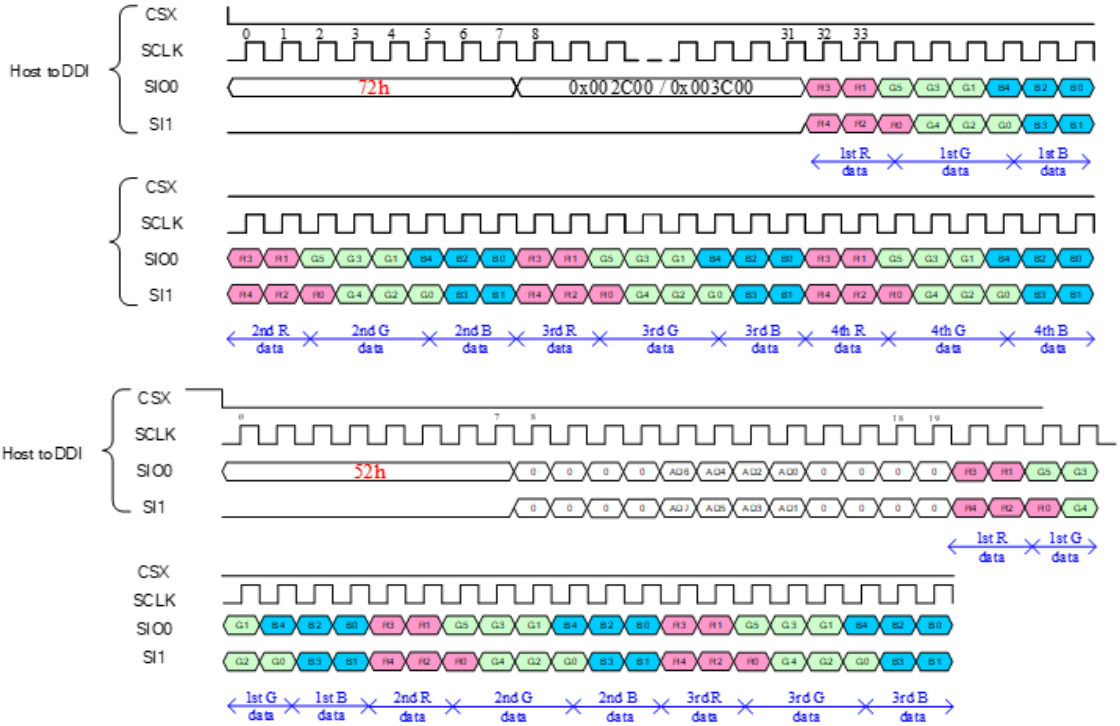


RGB565:

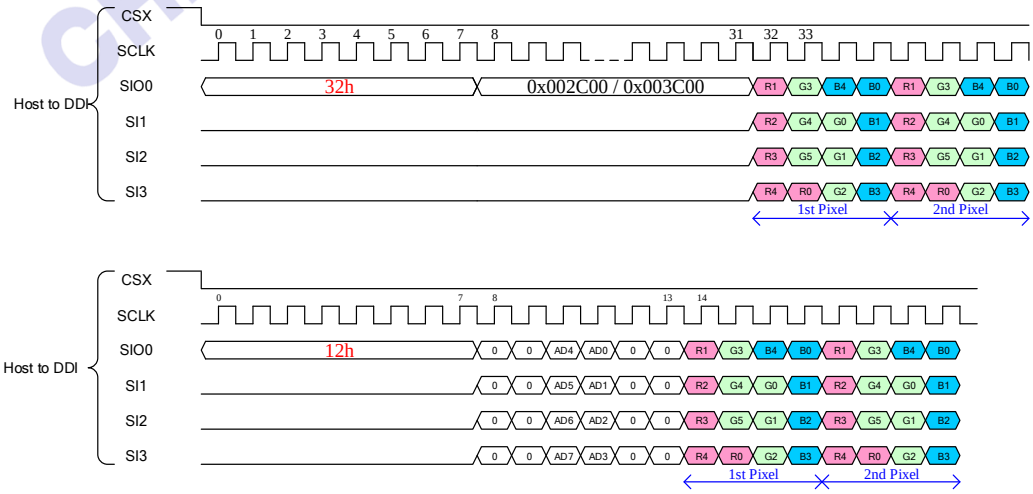
1-wire



2-wire

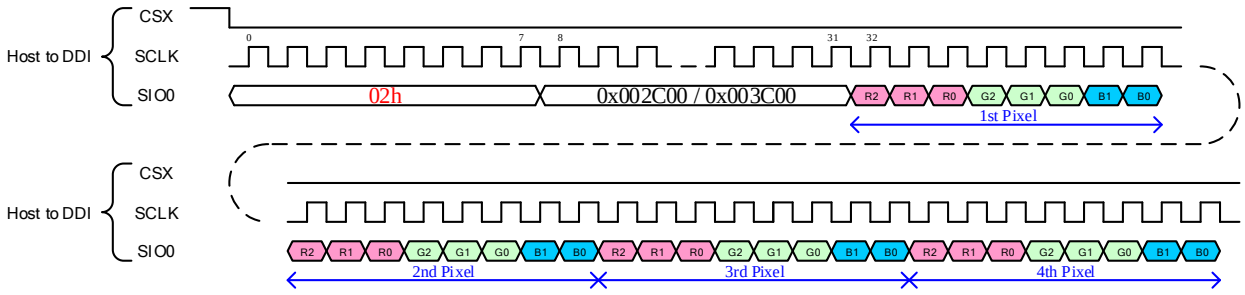


4-wire

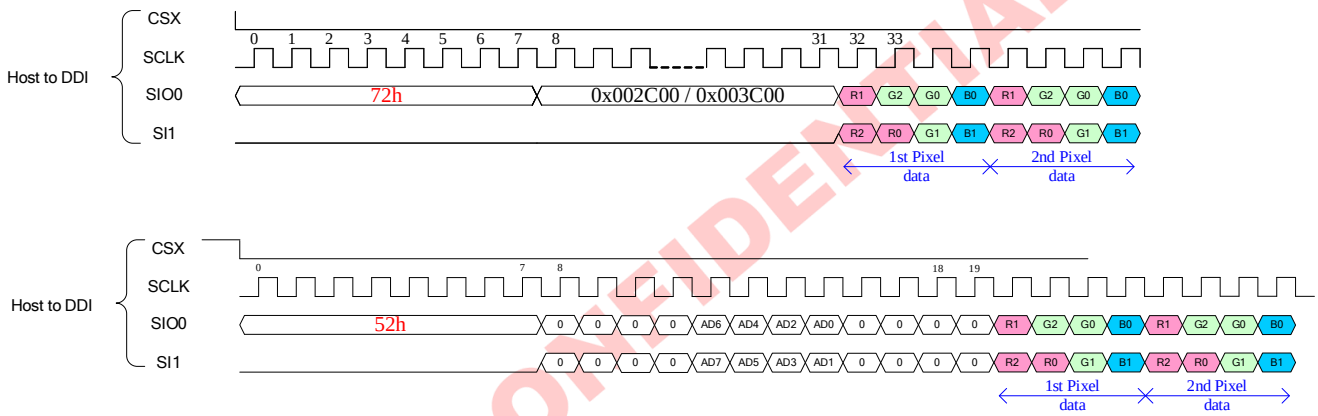


RGB332:

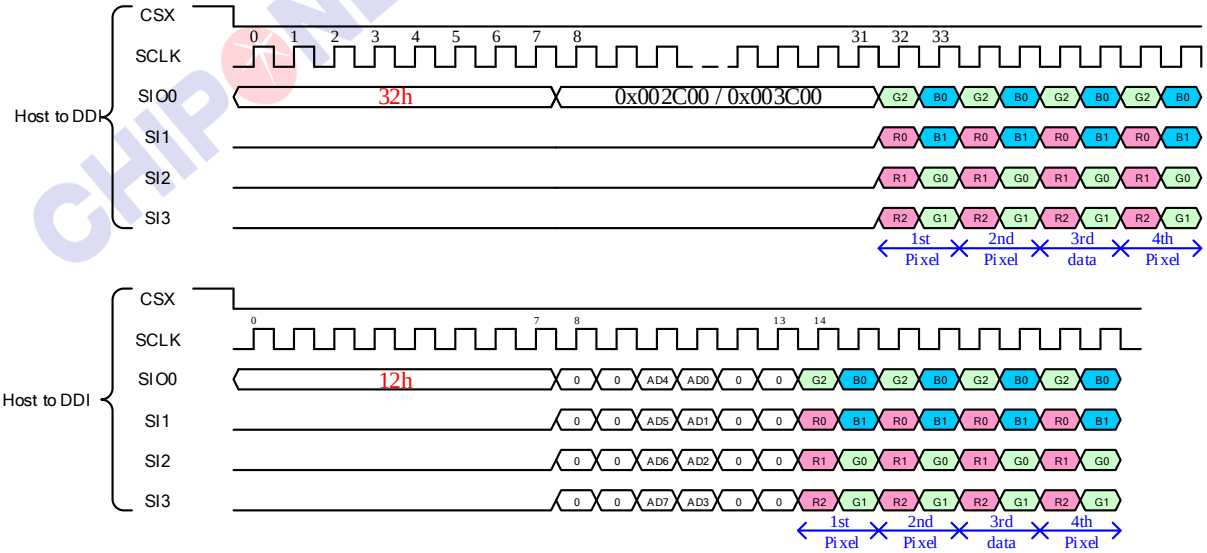
1-wire



2-wire



4-wire



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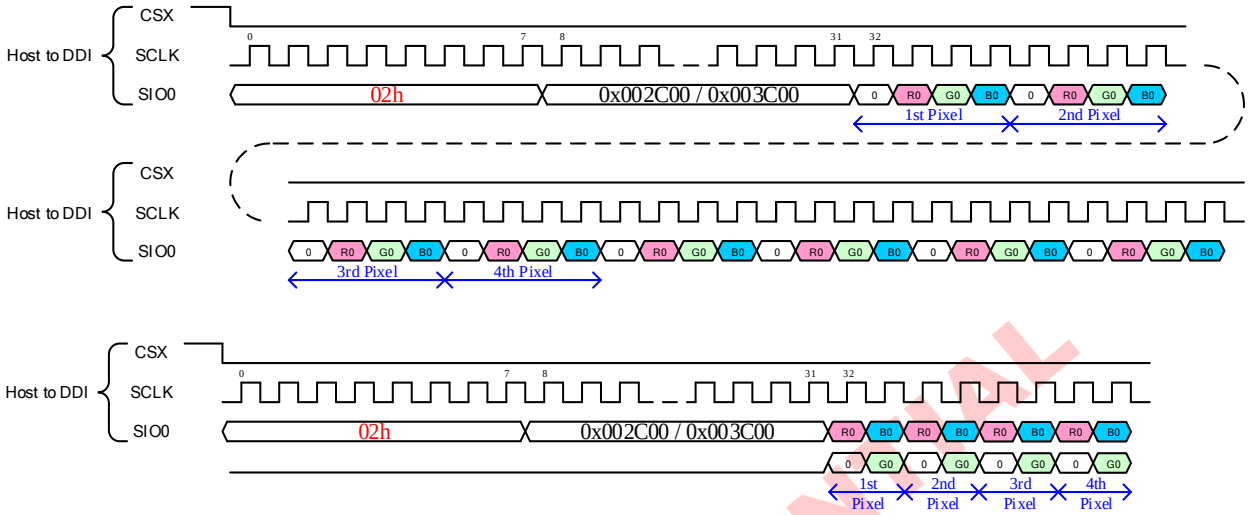
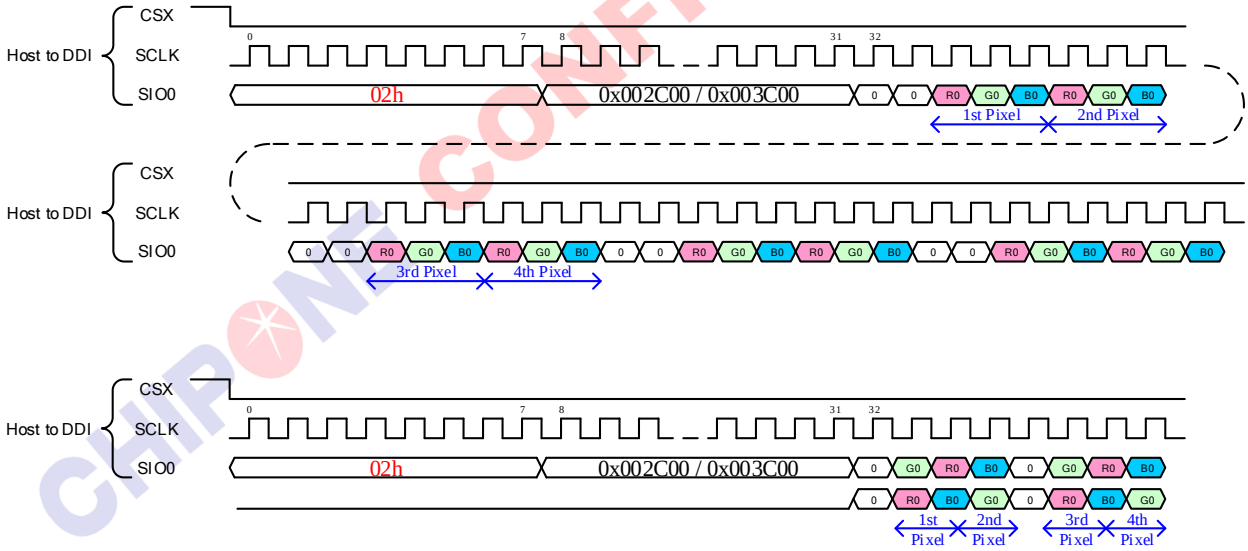
RGB111:

0RGB0RGB



00RGBRGB



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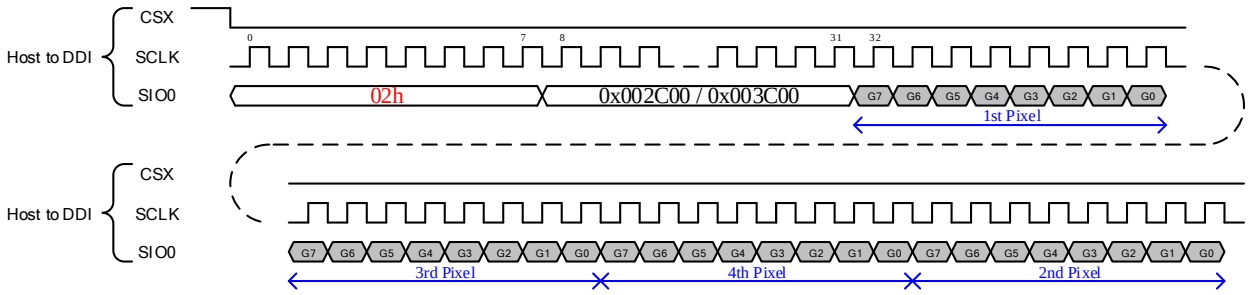
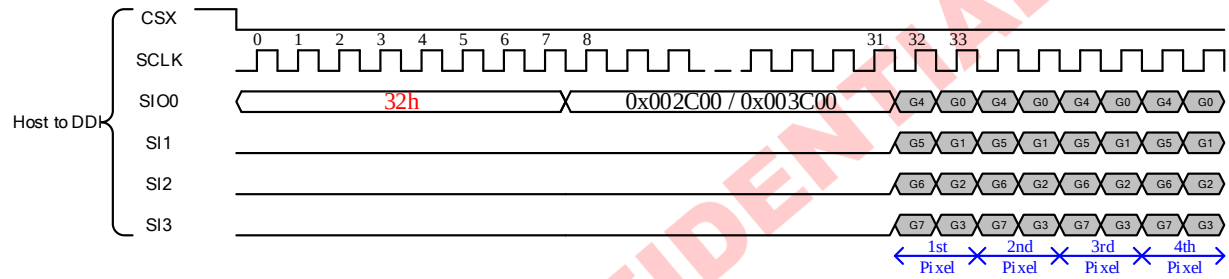
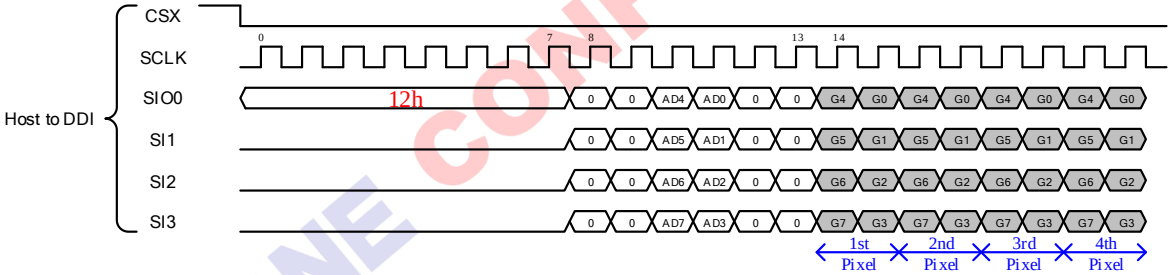
GRAY256:

1-wire



4-wire





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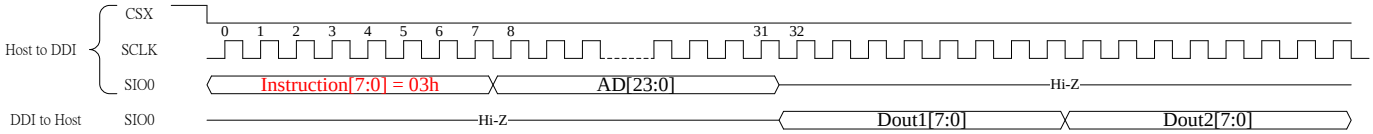
5.4.3 Read Cycle and Sequence

The QUAD SPI interface read mode are described in the following figure as below.

Instruction[7:0] = 03h	Command read
AD[23:0] = {8'h00, CMD[7:0], 8'h00}	Driver IC command address
Dout[7:0]	Driver IC output to host



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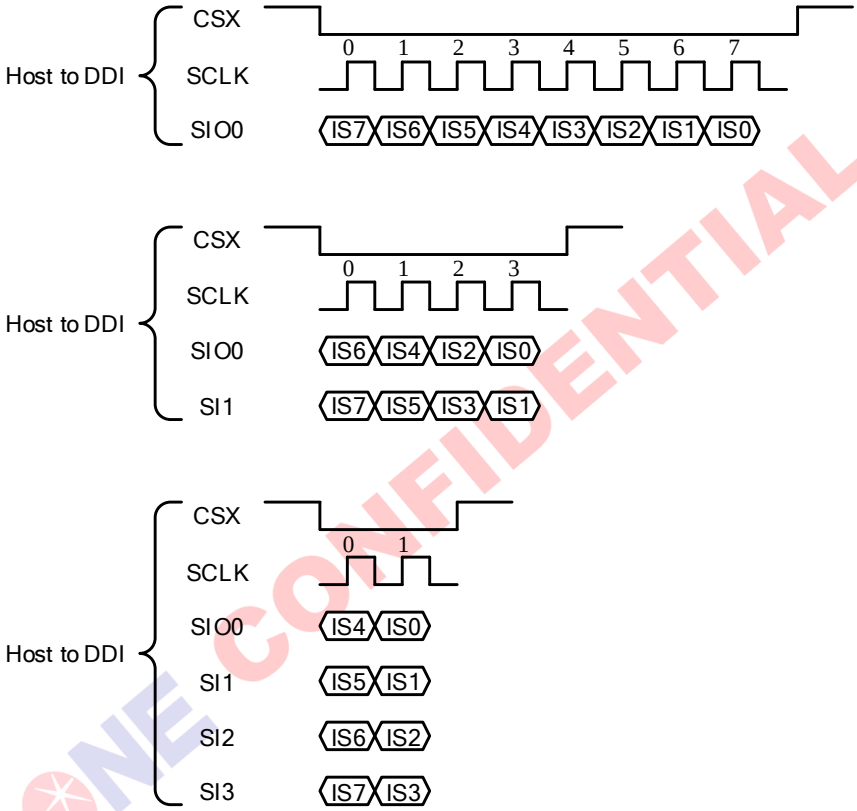
5.4.4 QUAD SPI Function

1.work mode change

The QUAD SPI interface utilizes CSX, SCL, SIO0, SI1, SI2 and SI3 signals. SCL is driven from high to low then pulled back to high during the write cycle. The host processor provides information during the write cycle while the display module reads the host processor information on the rising edge of SCL.

The QUAD SPI interface Send instruction in current mode to change to new mode.



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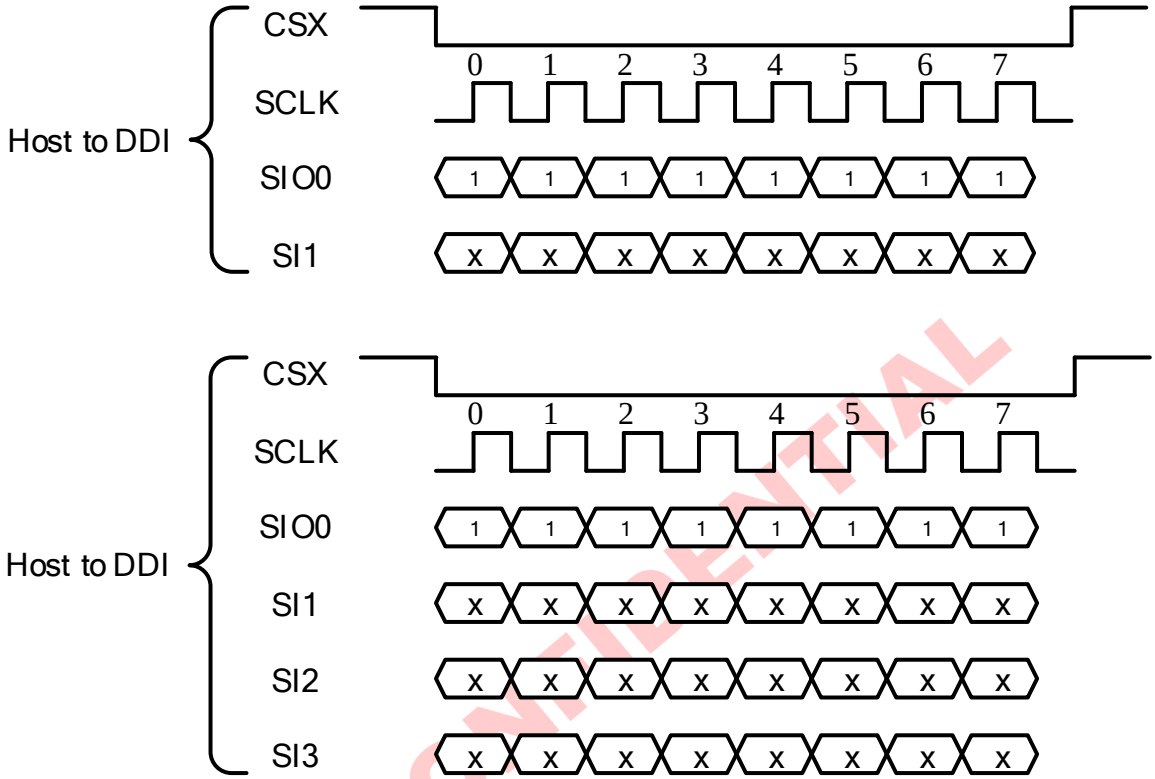
2.Reset Function

If the host is operating in 1-wire SPI protocol and the driver IC is operating in 2-wire or 4-wire SPI protocol, then the DDIC interface is reset to 1-wire SPI.



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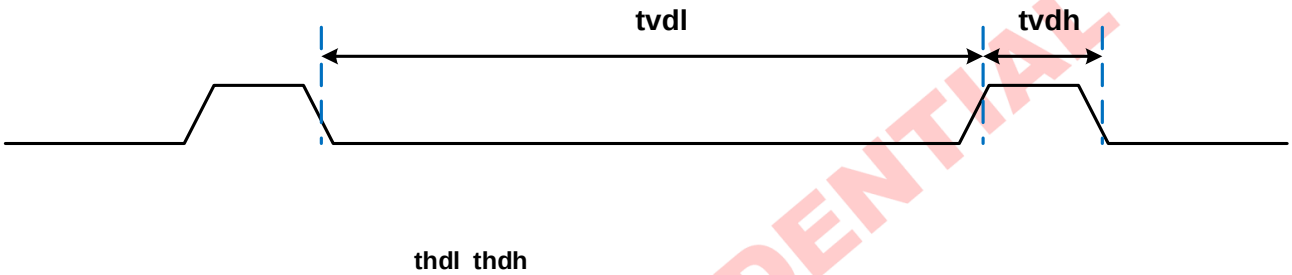
5.5 Tearing Effect Output

The tearing effect output line supplies to the HOST a panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line off and on commands. The mode of the tearing effect signal is defined by the parameter of the set_tear_on (35h) and set_tear_scanline(44h) commands. The signal can be used by the HOST to synchronize internal VSYNC when displaying video images.

5.5.1 **Tearing Effect Line Mode**

Mode 1,

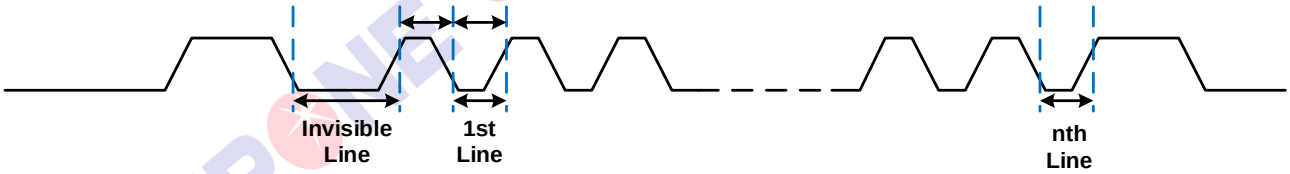
The tearing effect output signal consist of V-sync and V-Blanking information only:



tvdh = The LCD display is not updated from the frame memory.
tvdl = The LCD display is updated from the frame memory.

Mode 2,

The tearing effect output signal consist of V-Blanking and H-Blanking which are included of V-sync and H-sync information:



thdh = The display is not updated from the frame memory.
thdl = The display is updated from the frame memory.
n = Vertical scanning resolution

Mode 3,

This mode turn on the tearing effect output signal when vertical scanning reaches line N. In below figure, it shows that TE only output one line period pulse that can be selected from 2nd line to 1280th line by register 44h.

N = The N-th scanning line which set by register N[15:0] of command STESL(44h).
n = Vertical scanning resolution

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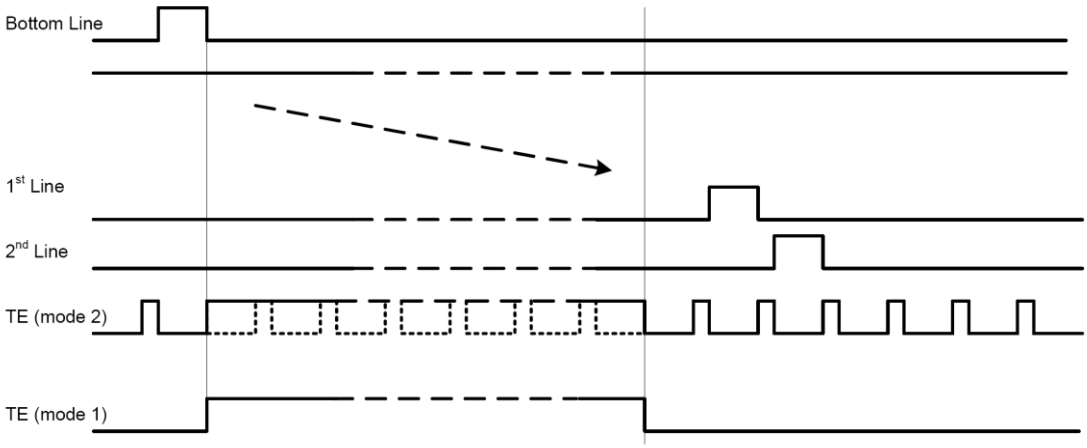

Note. During Sleep In mode, the tearing effect output signal is active low.

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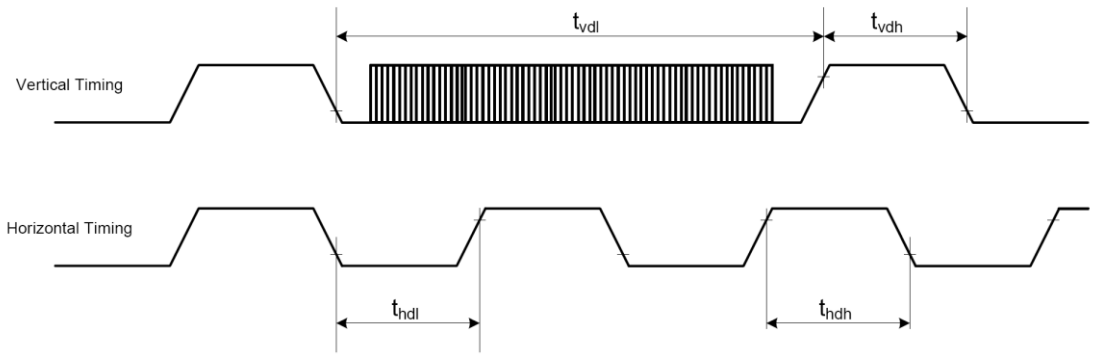
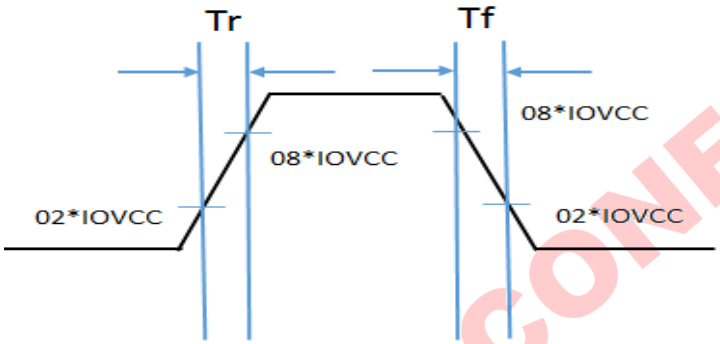
5.5.2 Tearing Effect Line Timing

The tearing effect signal is described as below:



AC characteristics of Tearing Effect Signal (Frame Rate = 60Hz)
Notes:
The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.



The Tearing Effect Output Line is fed back to the HOST and should be used as shown below to avoid tearing effect:

The below is described TE output Position by Register 35h and 44h.

Reg. 35h	Reg. 44h	TE Output Position
M	N	
0	0	TE high in V-porch region including of VBP and VFP for TE mode 1
1	0	TE high in all V-porch including of VBP and VFP/H-porch including of HBP and HFP region for TE mode 2
0	≠0	TE high at N-th line for TE mode 3
1	≠0	TE high in all V-porch including of VBP and VFP/H-porch including of HBP and HFP region for TE mode 2

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5.6 Display Serial Interface (DSI) MIPI Interface

5.6.1 Interface Level Communication

5.6.1.1 General

The display module uses data and clock lane differential pairs for DSI (DSI-1M). Both differential lane pairs can be driven to Low Power (LP) or High Speed (HS) mode.
Low Power mode means that each line of the differential pair is used in the single ended mode, a differential receiver is disable (a termination resistor of the receiver is disable), and it can be driven into a low power mode.

High Speed mode means that differential pairs (the termination resistor of the receiver is enable) are not used in the single ended mode.
Different modes and protocols are used in each mode when transferring information from the MCU to the display module and vice versa.
The State Codes of the High Speed (HS) and Low Power (LP) lane pair are defined below.

The State Codes of the High Speed (HS) and Low Power (LP) lane pair define

Lane Pair State Code	Line DC Voltage Levels		High Speed (HS)	Low Power	
	DATA_P	DATA_N	Burst Mode	Control Mode	Escape Mode
HS-0	Low (HS)	High (HS)	Differential - 0	Note1	Note1
HS-1	High (HS)	Low (HS)	Differential – 1	Note1	Note1
LP-00	Low (LP)	Low (LP)	Not Defined	Bridge	Space
LP-01	Low (LP)	High (LP)	Not Defined	HS-Request	Mark-0
LP-10	High (LP)	Low (LP)	Not Defined	LP-Request	Mark-1
LP-11	High (LP)	High (LP)	Not Defined	Stop	Note 2

Note 1: *Low-Power Receivers (LP-Rx) of the lane pair will check the LP-00 state code when the Lane Pair is in the High Speed (HS) mode.*

Note 2 : *If Low-Power Receivers (LP-Rx) of the lane pair recognizes the LP-11 state code, then the lane pair will return to LP-11 of the Control Mode.*

Note 3: *n = 0, and 1(D1P/N, and D2 P/N lanes only for HS-0 and HS-1).*

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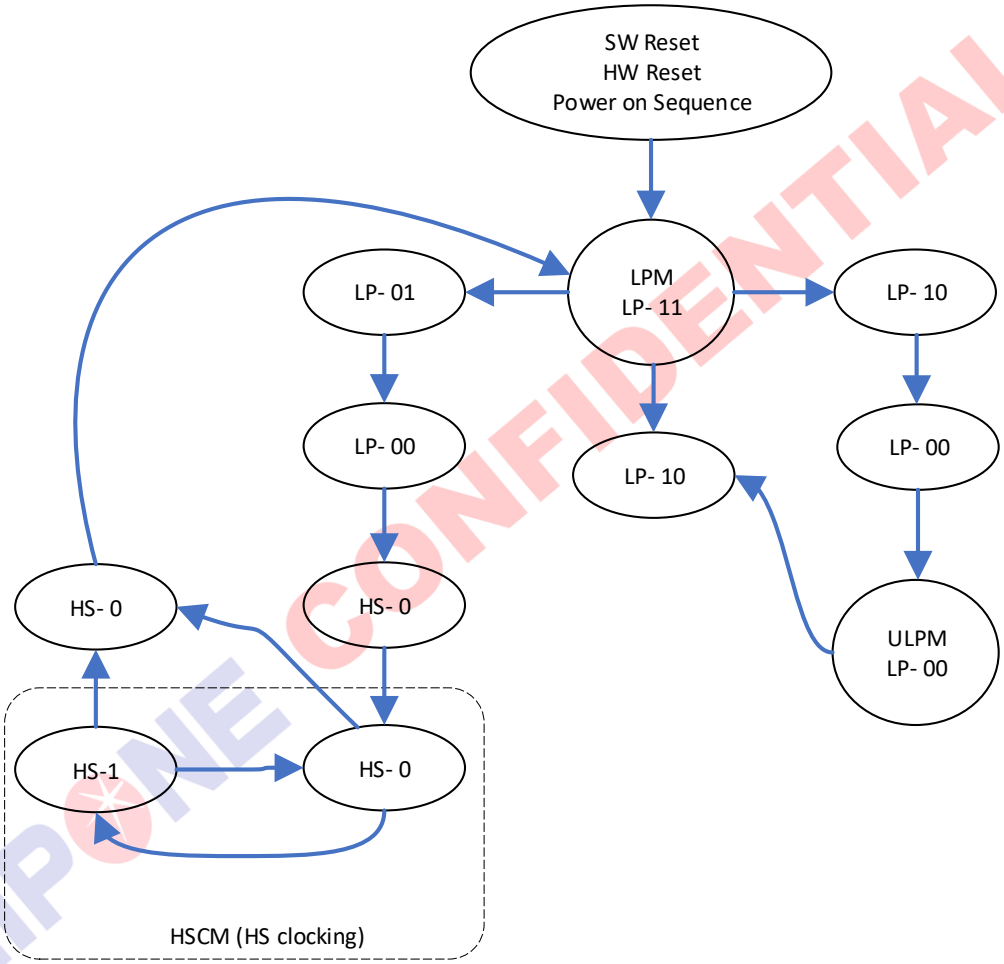
5.6.1.2 DSI CLK Lanes

CLKP/N lanes can be driven into three different power modes: Low Power Mode (LPM), Ultra-Low Power Mode (ULPM) and High Speed Clock Mode (HSCM). Clock lane is in the single ended mode (LP = Low Power) when entering or leaving Low Power Mode (LPM) or Ultra-Low Power Mode (ULPM). Clock lane is in the single ended mode (LP = Low Power) when entering in or leaving High Speed Clock Mode (HSCM). These entering and leaving protocols use Clock lane in the single ended mode to generate an entering or leaving sequence. The principal flow chart of the different Clock lane power modes is illustrated below.



Clock Lane Power Modes

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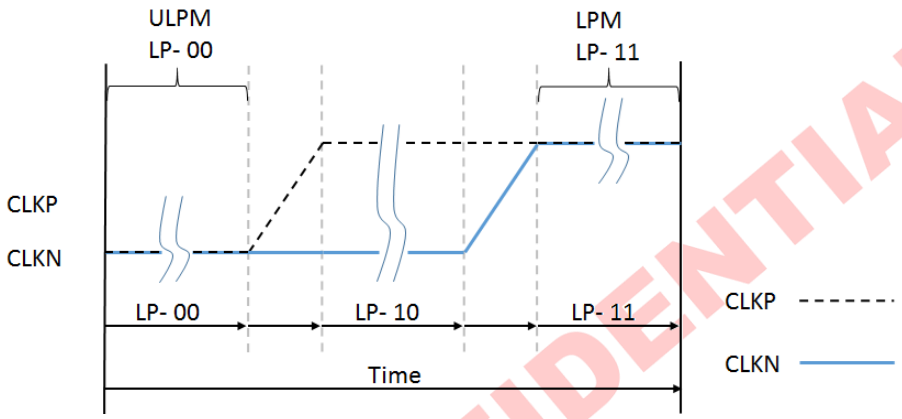
5.6.1.3 Low Power Mode (LPM)

CLKP/N lanes can be driven to the Low Power Mode (LPM), when CLKP/N lanes enter LP-11 State Code, in three different ways:

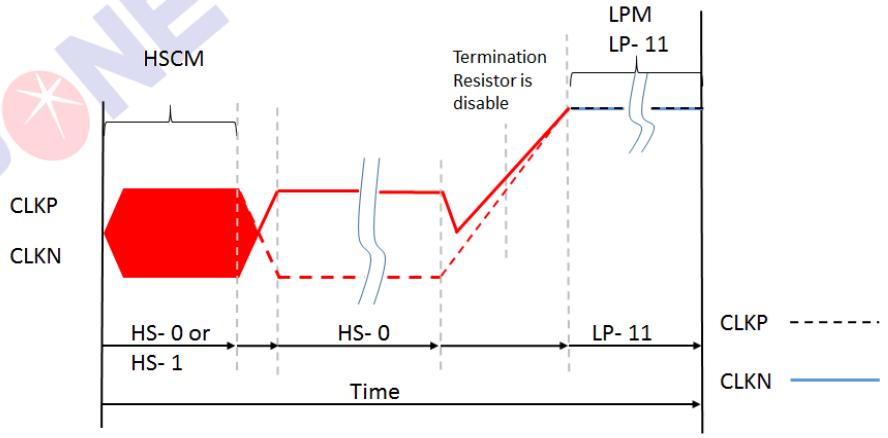
1) After SW Reset, HW Reset or Power On Sequence => LP-11.

2) After CLKP/N lanes leave Ultra-Low Power Mode (ULPM, LP-00 State Code) => LP-10 => LP-11 (LPM). This sequence is illustrated below.



From ULPM to LPM

3) After CLKP/N lanes leave High Speed Clock Mode (HSCM, HS-0 or HS-1 State Code) => HS-0=> LP-11 (LPM). This sequence is illustrated below.



From High Speed Clock Mode (HSCM) to LPM

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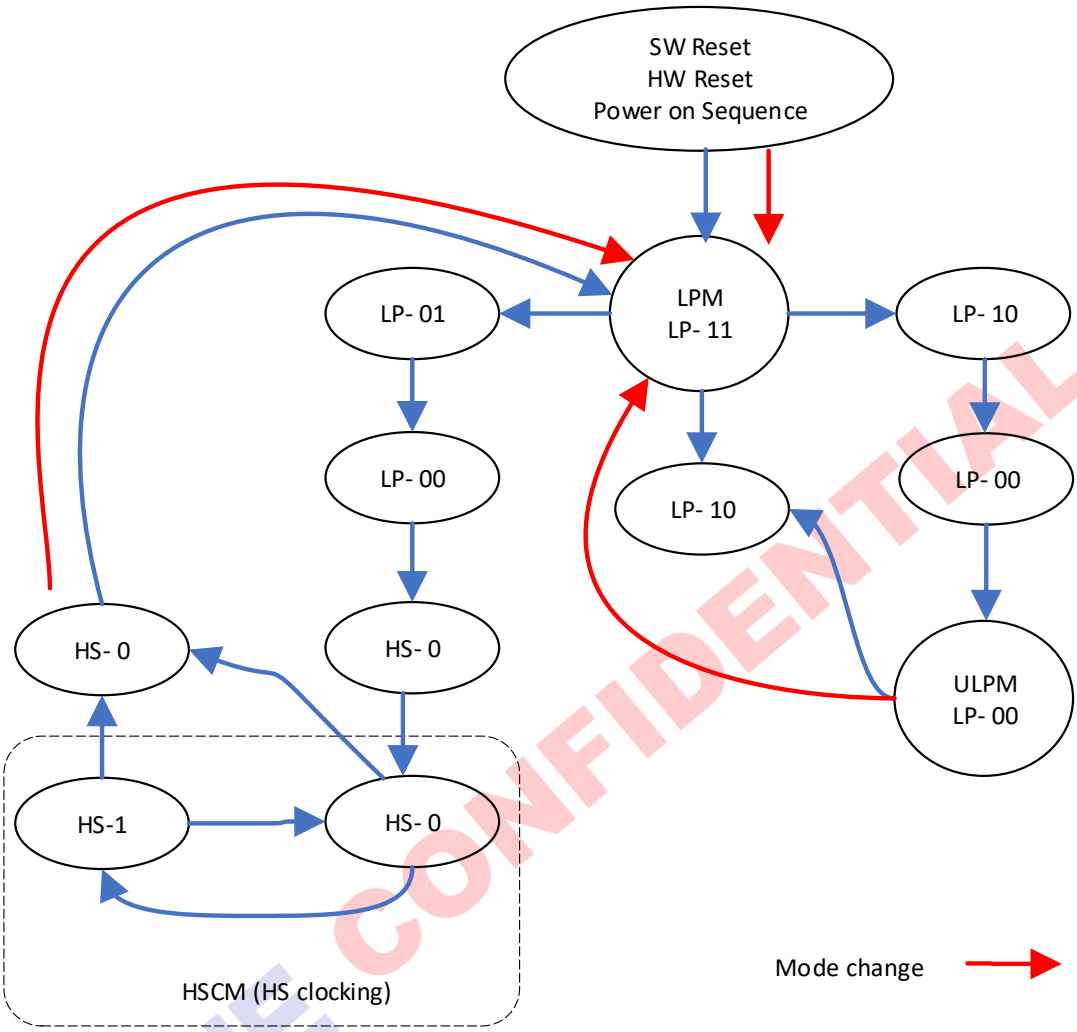
The changes of all the three modes are illustrated in the flow chart below.



All Three Mode Changes to LPM

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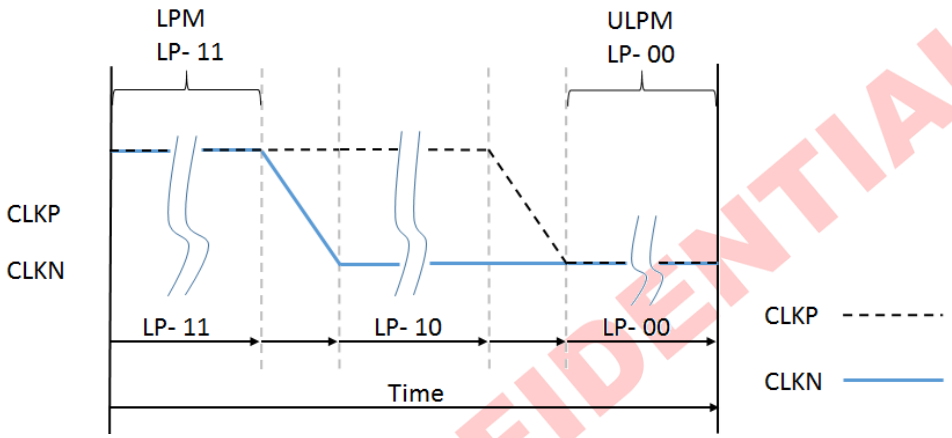
5.6.1.4 Ultra- Low Power Mode (ULPM)

CLKP/N lanes can be driven to the Ultra- Low Power Mode (ULPM), when CLKP/N lanes enter LP-11 State Code, in three different ways:

1) After SW Reset, HW Reset or Power On Sequence => LP-11.

2) After CLKP/N lanes leave Low Power Mode (LPM, LP-11 State Code) => LP-10 => LP-00 (ULPM). This sequence is illustrated below.



From LPM to ULPM

The mode change is also illustrated below.

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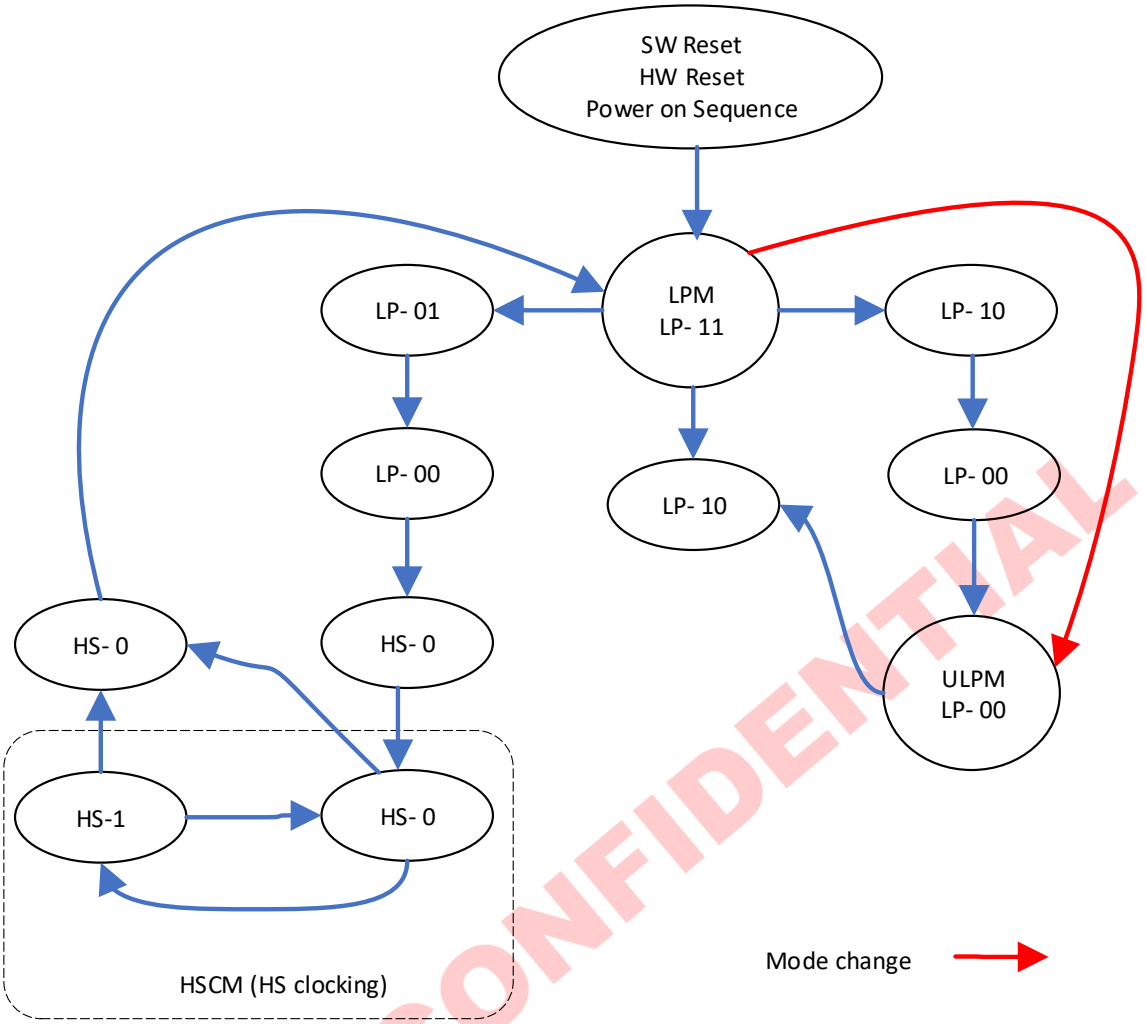

Mode Change from LPM to ULPM

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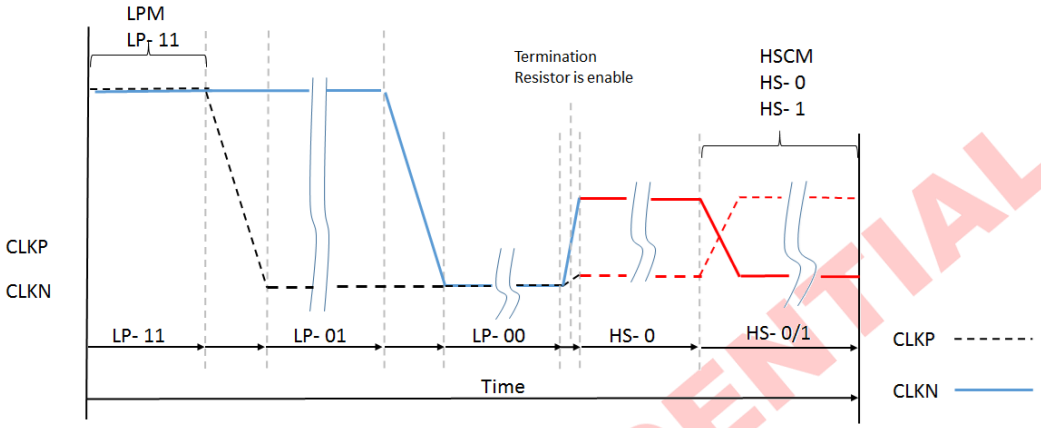
5.6.1.5 High- Speed Clock Mode (HSCM)

CLKP/N lanes can be driven to the High Speed Clock Mode (HSCM) when CLK lanes start to function between HS-0 and HS-1 State Codes. The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) => LP-01 => LP-00 => HS-0 => HS-0/1 (HSCM).

This sequence is illustrated below.



From LPM to HSCM

The mode change is also illustrated below.

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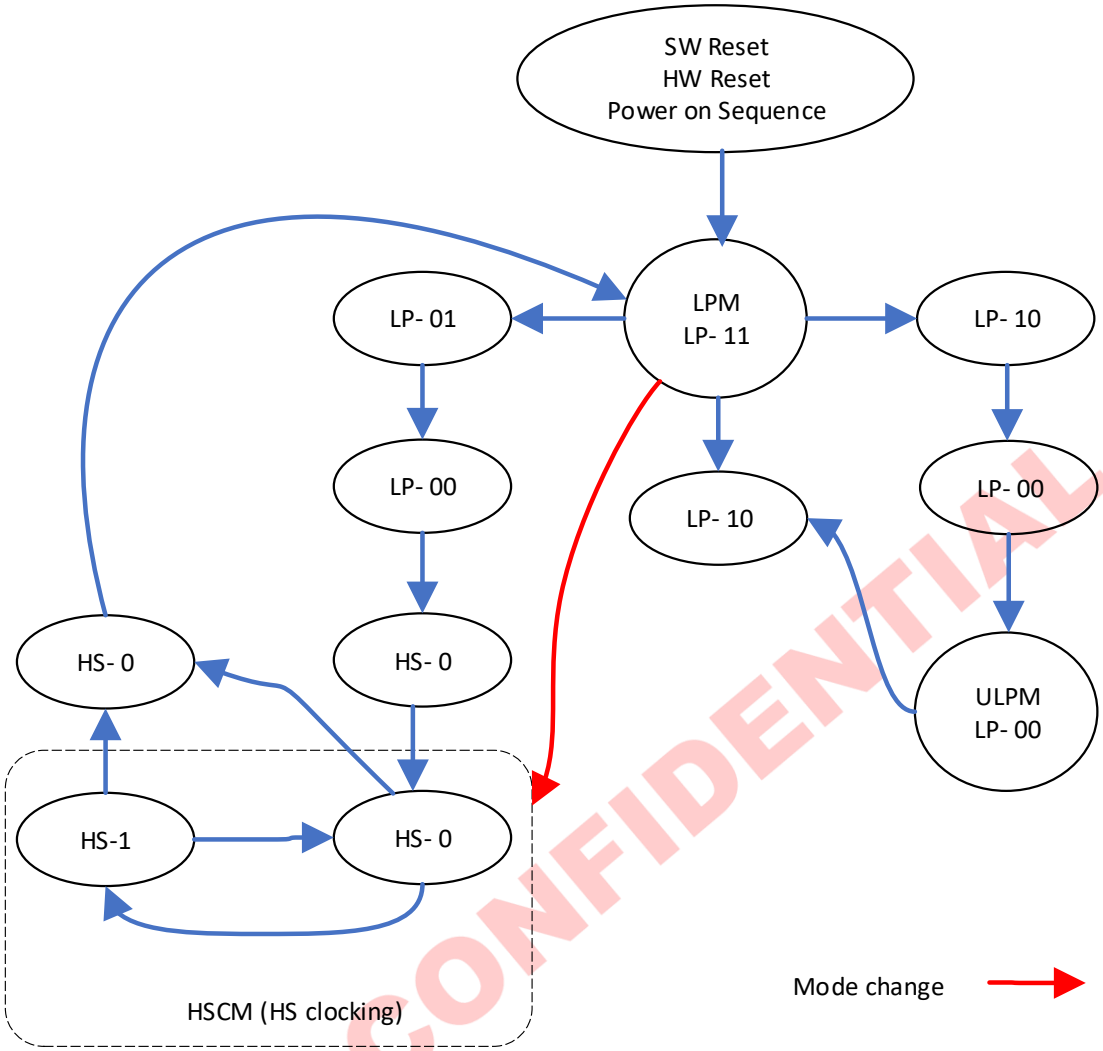

Mode Change from LPM to HSCM

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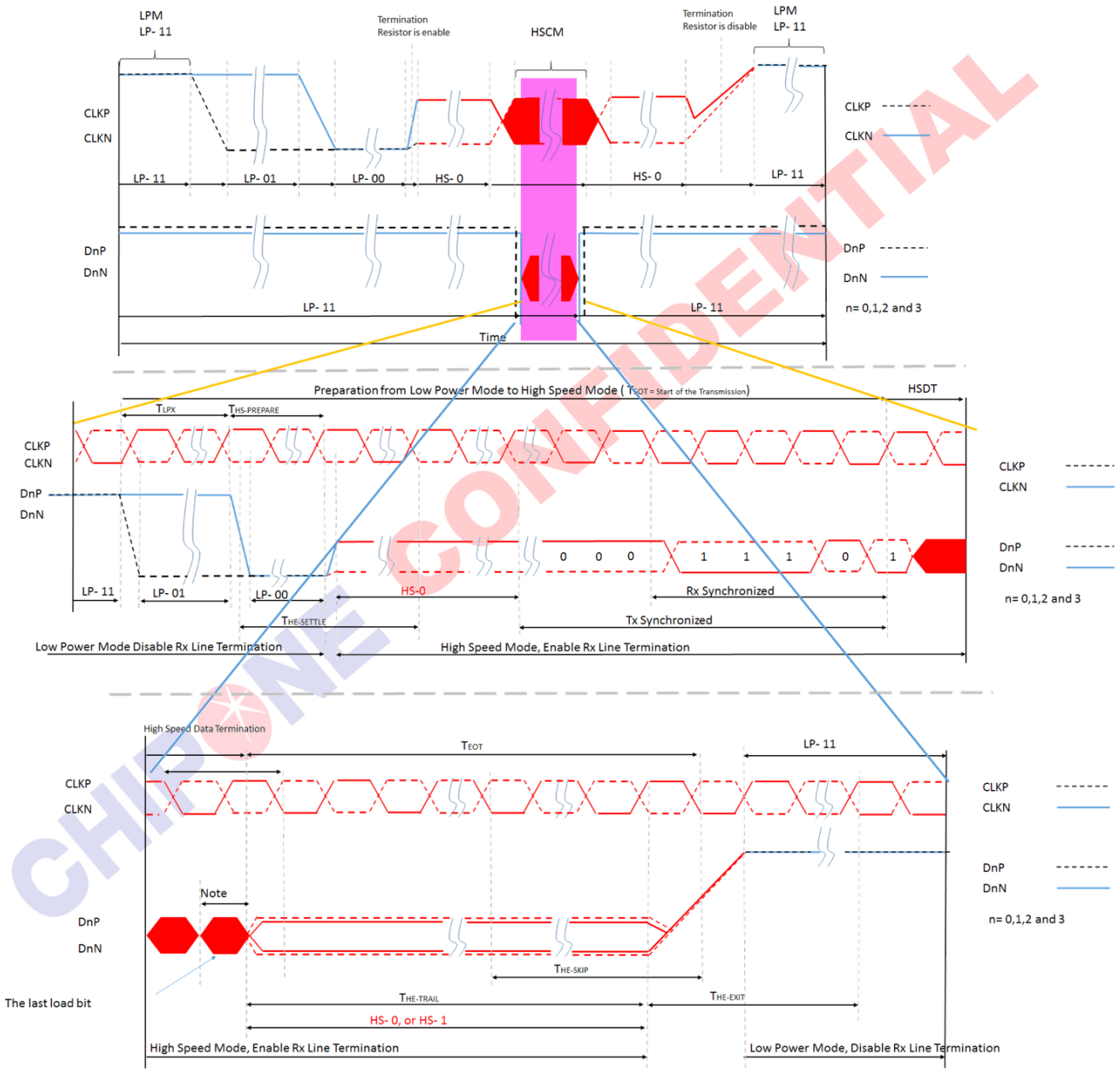
The high speed clock (CLKP/N) starts before high speed data is sent via data lanes. The high speed clock continues clocking after the high speed data sending is stopped.

The burst of the high speed clock consists of:

- Even number of transitions.
- Start state is HS- 0.
- End state is HS- 0.



Note:
If the last load bit is HS- 0, the transmitter changes from HS- 0 to HS- 1.
If the last load bit is HS- 1, the transmitter changes from HS- 1 to HS- 0

High Speed Clock Burs

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5.6.2 Interface Level Communication - DSI Data Lane

5.6.2.1 General

D0P/N, and D1P/N Data lanes can be driven into different modes:

- Escape Mode (Only D0P/N data lane is used).
- High- Speed Data Transmission (all data lanes are used).
- Bus Turnaround Request (Only D0P/N data lane are used).

These modes and their entering codes are defined in the following table.

Modes and entering code define

Mode	Entering Mode Sequence	Leaving Mode Sequence
Escape Mode	LP- 11→ LP- 10→ LP- 00 → LP- 01 → LP- 00	LP- 00→ LP- 10→ LP- 11 (Mark-1)
High- Speed Data Transmission	LP- 11→ LP- 01 → LP- 00 → HS- 0	(HS- 0 or HS- 1)→ LP11
Bus Turnaround Request	LP- 11→ LP- 10→ LP- 00 → LP- 10→ LP- 00	Hi- Z

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5.6.2.2 Escape Modes

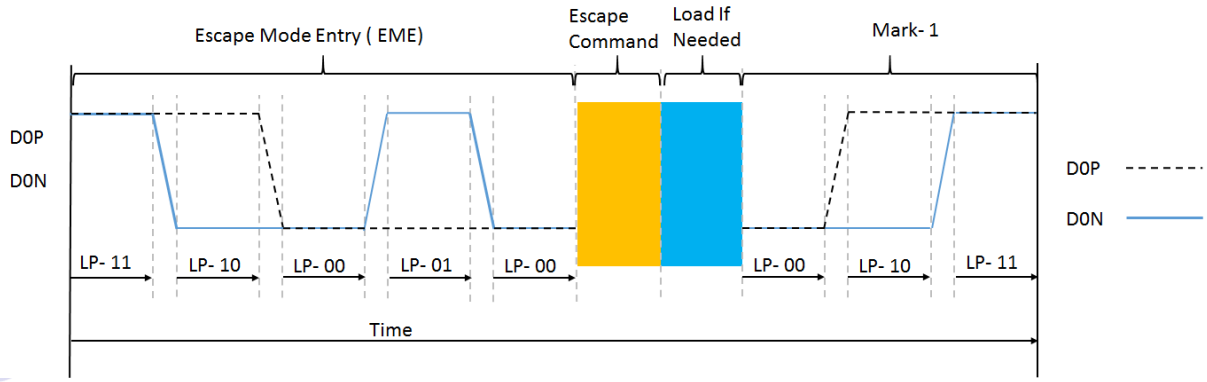
D0P/N data lanes can be used in different Escape Modes when data lanes are in the Low Power (LP) mode. These Escape Modes are used to:

- Send “Low-Power Data Transmission” (LPDT) from the MCU to the display module.
- Drive data lanes to “Ultra-Low Power State” (ULPS).
- Indicate “Remote Application Reset” (RAR), which can reset the display module.
- Indicate “Acknowledge” (ACK), which is used to transmit a non-error event from the display module to the MCU.

The basic sequence of the Escape Mode is as follows:

- Start: LP-11.
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00.
- Escape Command (EC), which is coded, when one of the data lanes changes from low-to-high-to-low then this changed data lane presents the value of the current data bit (D0P = 1, D0N= 0). When DSI-D0 changes from low-to-high-to-low, the receiver will latch a data bit, which value is logical 0. The receiver will use this low-to-high-to-low transition as its internal clock.
- A load if it is needed.
- Exit Escape (Mark-1) LP-00 => LP-10 => LP-11.
- End: LP-11.

This basic construction is illustrated below.



General Escape Mode Sequence

A total of eight Escape Commands (EC) are divided into two types: Mode and Trigger, as shown in below Table.

An example of the Mode type Escape Command is „Ultra-Low Power Mode", where the MCU instructs the display module to enter its Ultra-Low Power Mode.

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Escape commands are defined in the following table.

Escape commands define

Escape Command	Command Type Mode / Trigger	Entry command Pattern (First Bit→ Last Bit Transmitted)	Dn	D0
Low- Power Data Transmission	Mode	1110 0001 bin		x
Ultra- Low Power Mode	Mode	0001 1110 bin	x	x
Underfined- 1, Note1	Mode	1001 1111 bin		
Underfined- 2, Note1	Mode	1101 1110 bin		
Remote Application Reset	Trigger	0110 0010 bin		x
Acknowledge	Trigger	0010 0001 bin		x
UnKnow- 5, Note1	Trigger	1010 0000 bin		

Note 1: *This Escape command support is not implemented on the display module.*

Note 2: *n=1.*

Note 3: *x= supported.*

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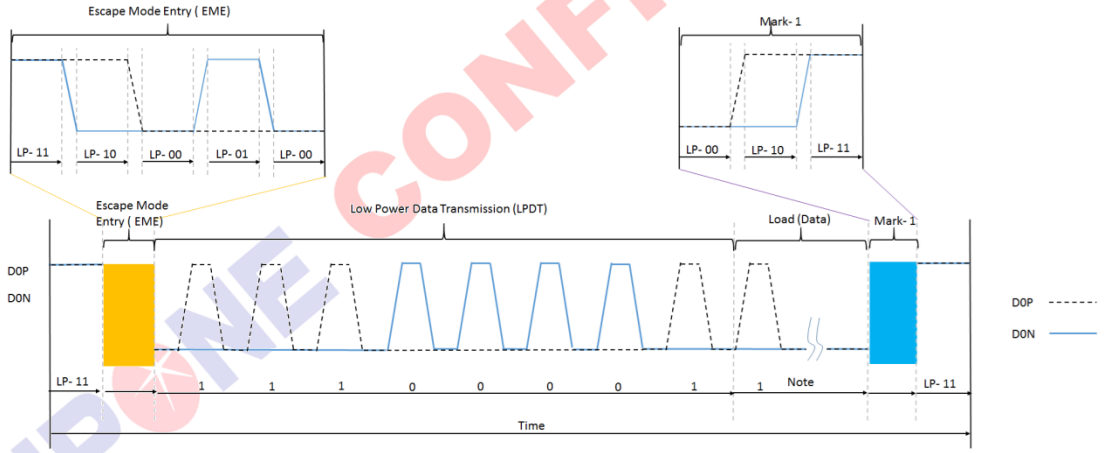
5.6.2.3 Low- Power Data Transmission (LPDT)

The MCU can send data to the display module in the Low-Power Data Transmission (LPDT) mode when data lanes enter the Escape Mode and Low-Power Data Transmission (LPDT) command is sent to the display module.

The display module also uses the same sequence when it sends data to the MCU. The Low Power Data Transmission (LPDT) uses the following sequence:

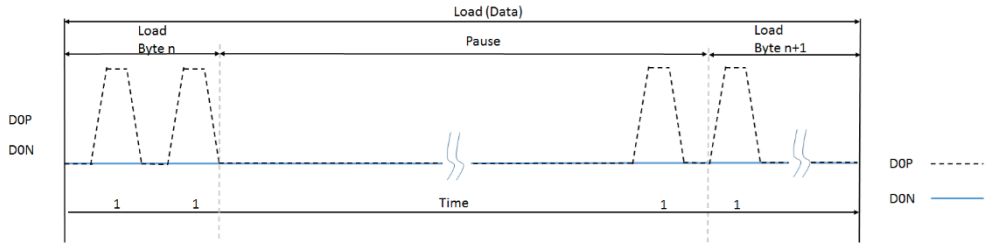
- Start: LP-11.
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00.
- Low-Power Data Transmission (LPDT) command in the Escape Mode: 1110 0001 (first to last bit).
- Load (Data).
- One or more bytes (one byte = 8 bit).
- Data lanes are in pause mode when data lanes are stopped (both lanes are low) between bytes.
- Mark-1: LP-00 => LP-10 => LP-11.
- End: LP-11.

This sequence is illustrated for reference purposes below.



Low- Power Data Transmission (LPDT)

Note: *Load (Data) presents that the first bit is the logical 1 in this example.*



Pause (Example)

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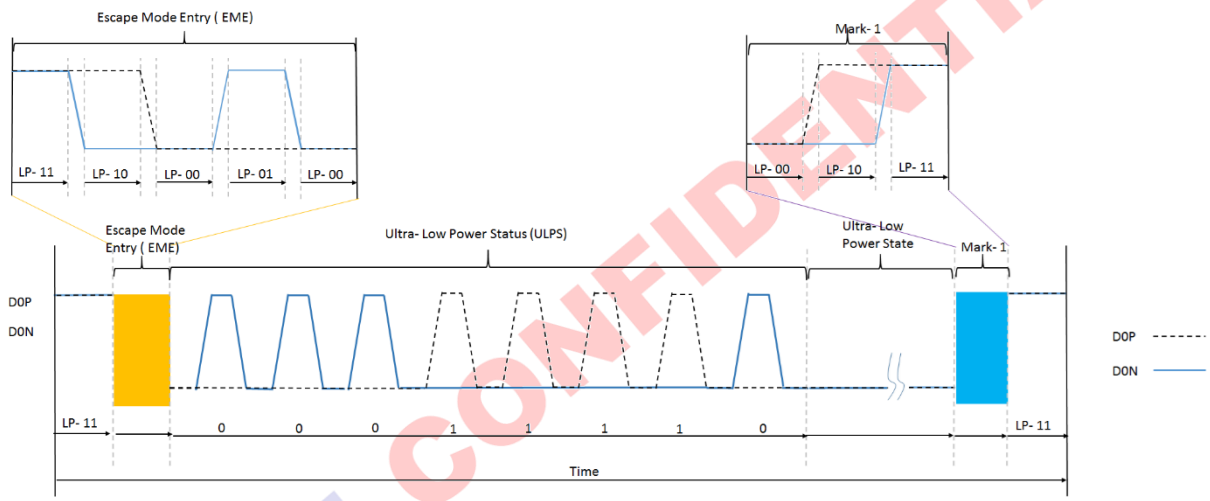
5.6.2.4 Ultra- Low Power State (ULPS)

The MCU can force data lanes get into the Ultra-Low Power State (ULPS) mode when data lanes enter the Escape Mode. The Ultra-Low Power State (ULPS) uses the following sequence:

- Start: LP-11.
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00.
- Ultra-Low Power State (ULPS) command in the Escape Mode: 0001 1110 (first to last bit).
- Ultra-Low Power State (ULPS) when the MCU keeps data lanes low.
- Mark-1: LP-00 => LP-10 => LP-11.
- End: LP-11 (Next command must wait 100us after data lanes leave ULPS).

This sequence is illustrated for reference purposes below.



Ultra- Low Power State (ULPS)

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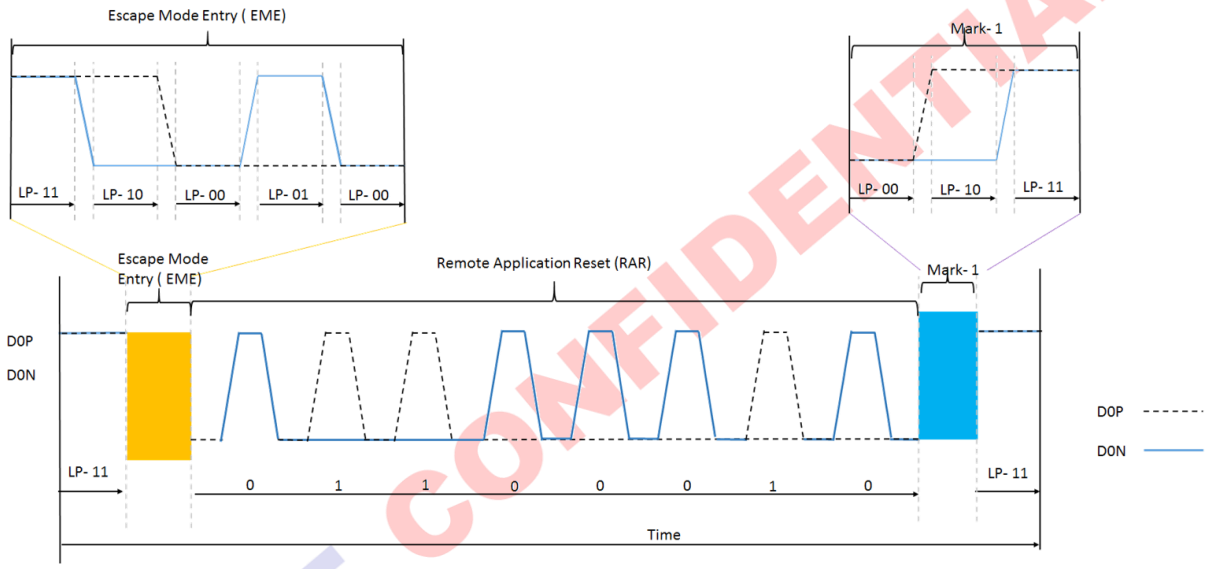
5.6.2.5 Remote Application Reset (RAR)

The MCU can inform the display module that it should be reset in Remote Application Reset (RAR) trigger when data lanes enter the Escape Mode. The Remote Application Reset (RAR) uses the following sequence:

- Start: LP-11.
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00.
- Remote Application Reset (RAR) command in Escape Mode: 0110 0010 (first to last bit).
- Mark-1: LP-00 => LP-10 => LP-11.
- End: LP-11.

This sequence is illustrated for reference purposes below.



Remote Application Reset (RAR)

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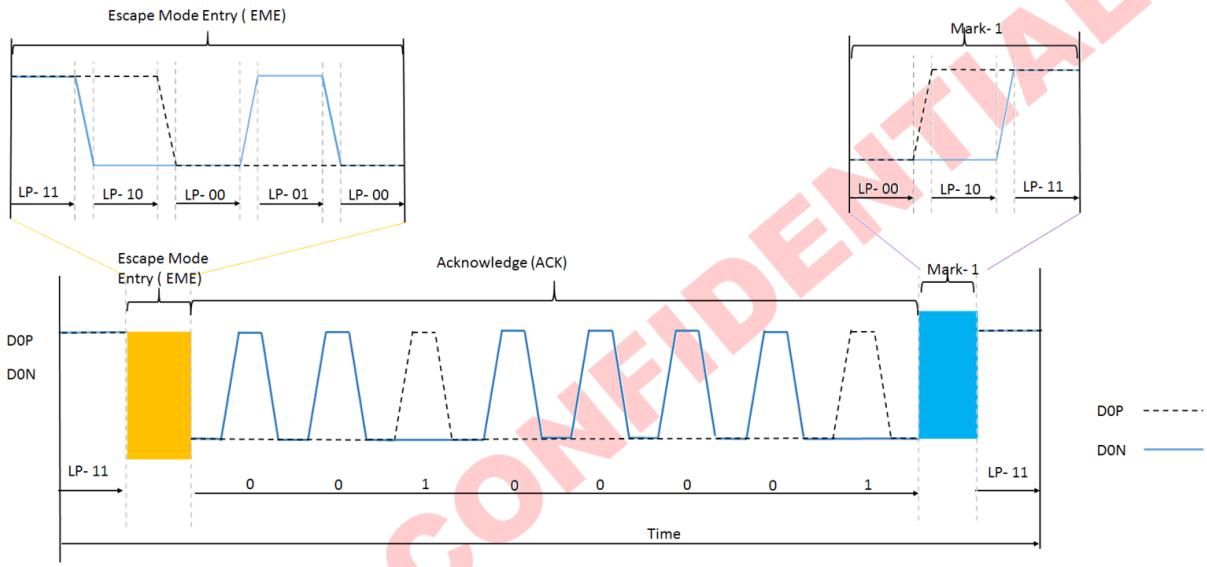
5.6.2.6 Acknowledge (ACK)

The display module can inform the MCU an error is not recognized by Acknowledge (ACK). The display module sends the Acknowledge (ACK) with the following sequence:

- Start: LP-11.
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00.
- Acknowledge (ACK) command in the Escape Mode: 0010 0001 (first to last bit).
- Mark-1: LP-00 => LP-10 => LP-11.
- End: LP-11.
-

This sequence is illustrated for reference purposes below.



Acknowledge (ACK)

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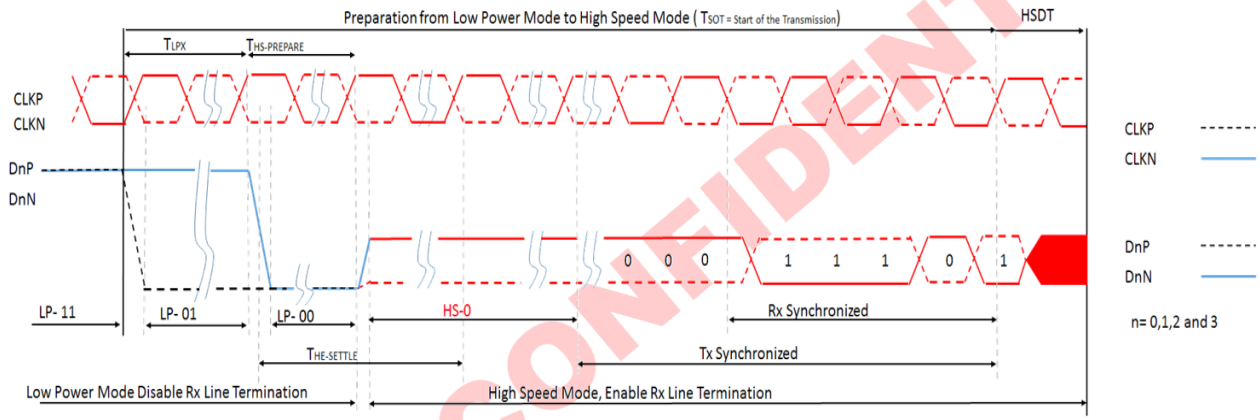
5.6.2.7 Entering High- Speed Data Transmission (TSOT of HSDT)

The display module enters High-Speed Data Transmission (HSDT) when Clock lane CLKP/N have already entered the High-Speed Clock Mode (HSCM) by the MCU. See more information in the section “High-Speed Clock Mode (HSCM)”. Data lanes D0P/N and D1P/N of the display module enter the High-Speed Data Transmission (TSOT of HSDT) as follows:

- Start: LP-11.
- HS-Request: LP-01.
- HS-Settle: LP-00 => HS-0 (Rx: Lane Termination Enable).
- Rx Synchronization: 011101 (Tx (= MCU) Synchronization: 0001 1101).
- End: High-Speed Data Transmission (HSDT) – Ready to receive High-Speed Data Load.

The sequence of entering High-Speed Data Transmission (TSOT of HSDT) is illustrated below.



Entering High- Speed Data Transmission (TSOT of HSDT)

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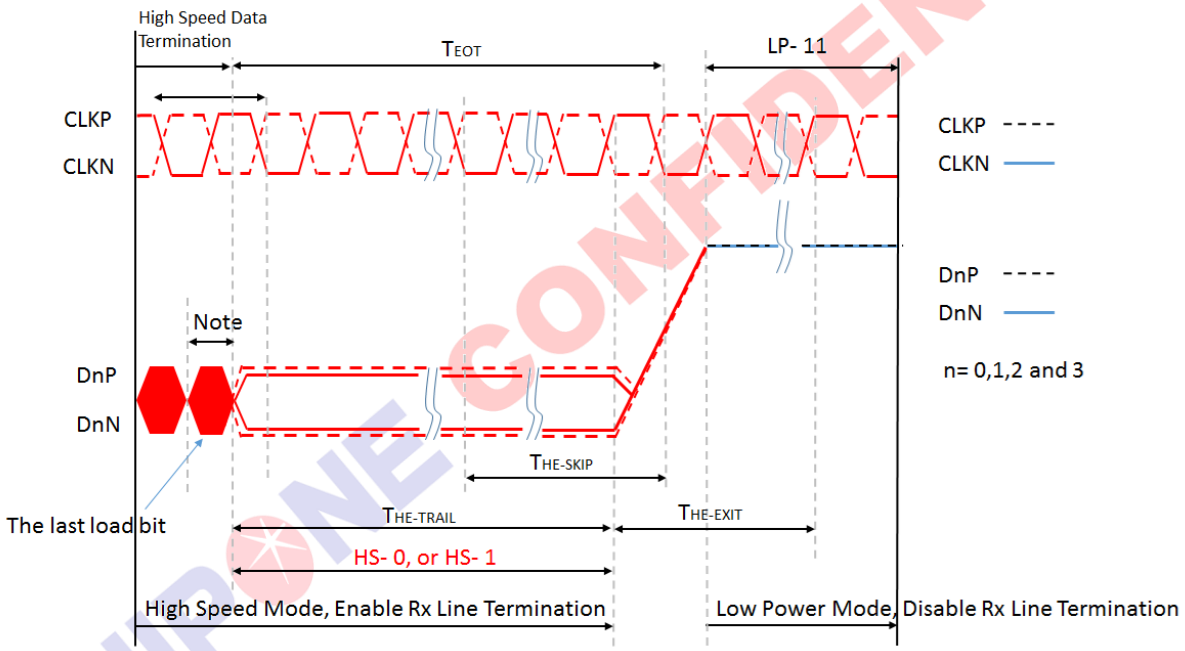
5.6.2.8 Leaving High- Speed Data Transmission (TEOP of HSDT)

The display module leaves the High-Speed Data Transmission (TEOT of HSDT) when Clock lane DSICLKP/N are in the High-Speed Clock Mode (HSCM) by the MCU, and this HSCM is kept until data lanes D0P/N and D1P/N are in the LP-11 mode. See more information in the section “High-Speed Clock Mode (HSCM)”. Data lanes D0P/N and D1P/N of the display module leave the High-Speed Data Transmission (TEOT of HSDT) as follows:

- Start: High-Speed Data Transmission (HSDT).
- Stops High-Speed Data Transmission.
- MCU changes to HS-1, if the last load bit is HS-0.
- MCU changes to HS-0, if the last load bit is HS-1.
- End: LP-11 (Rx: Lane Termination Disable).

The sequence of leaving High-Speed Data Transmission (TEOT of HSDT) is illustrated below.



Note:
If the last load bit is HS- 0, the transmitter changes from HS- 0 to HS- 1.
If the last load bit is HS- 1, the transmitter changes from HS- 1 to HS- 0

Leaving High- Speed Data Transmission (TEOT of HSDT)

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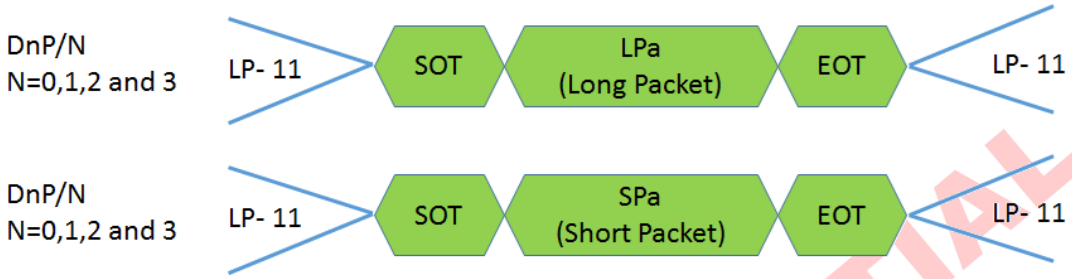
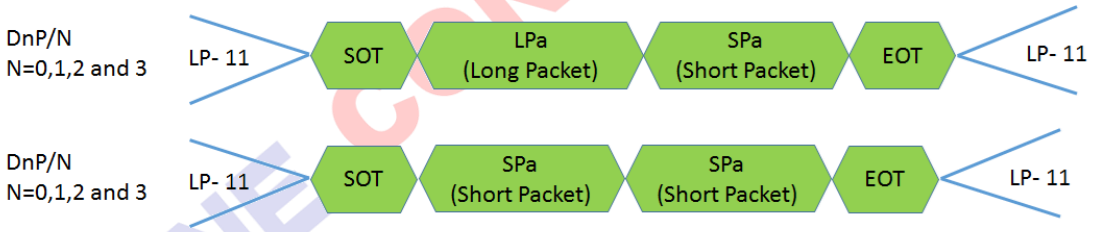
5.6.2.9 Burst of the High- Speed Data Transmission (HSDT)

The burst of the “High-Speed Data Transmission” (HSDT) can consist of one or several data packet(s). These data packets can be Long (LPa) or Short (SPa) packets. These packets are defined in the section “Short Packet (SPa) and Long Packet (LPa) Structures”. These different burst of the High-Speed Data Transmission (HSDT) cases are illustrated for reference purposes below.



Single Packet in High- Speed Data Transmissions

The multiple packets in High-Speed Data Transmission are illustrated for reference purposes below.



Multiple Packets in High- Speed Data Transmission – Example

Explanations of Packet Abbreviation

Abbreviation	Explanation
EOT	End of the Transmission
LPa	Long Packet
LP-11	Low Power Mode, Both of Data lanes stay at “1” (Stop Mode)
SPa	Short Packet
SOT	Start of the Transmission

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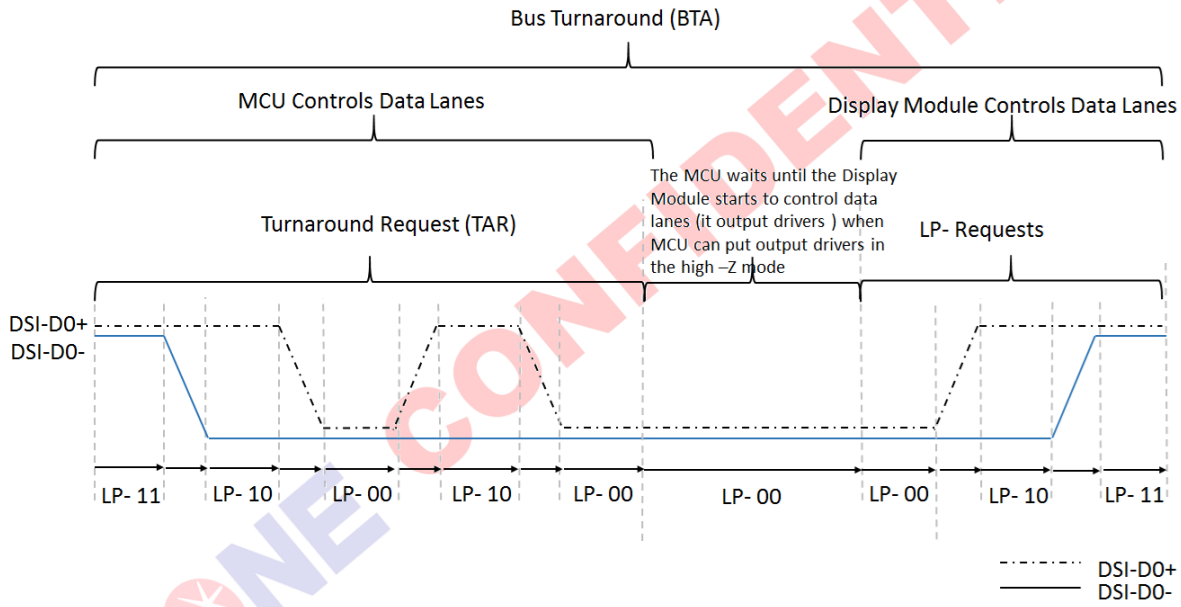
5.6.2.10 Bus Turnaround (BTA)

The MCU or display module, which controls D0P/N Data Lanes, can start a bus turnaround procedure when it requires information from a receiver, which can be the MCU or display module. The MCU and display module use the same sequence when this bus turnaround procedure is used. The sequence, when the MCU wants to do the bus turnaround procedure to the display module, is described for reference purposes as follows:

- Start (MCU): LP-11.
- Turnaround Request (MCU): LP-11 => LP-10 => LP-00 => LP-10 => LP-00.
- The MCU waits until the display module starts to control D0P/N data lanes and the MCU stops to control D0P/N data lanes (= High-Z).
- The display module changes to the stop mode: LP-00 => LP-10 => LP-11.

The bus turnaround procedure (from the MCU to the display module) is illustrated below.



Bus Turnaround Procedure

MCU and display module terms can be switched on above figure, if the Bus Turnaround (BTA) is from the display module to the MCU.

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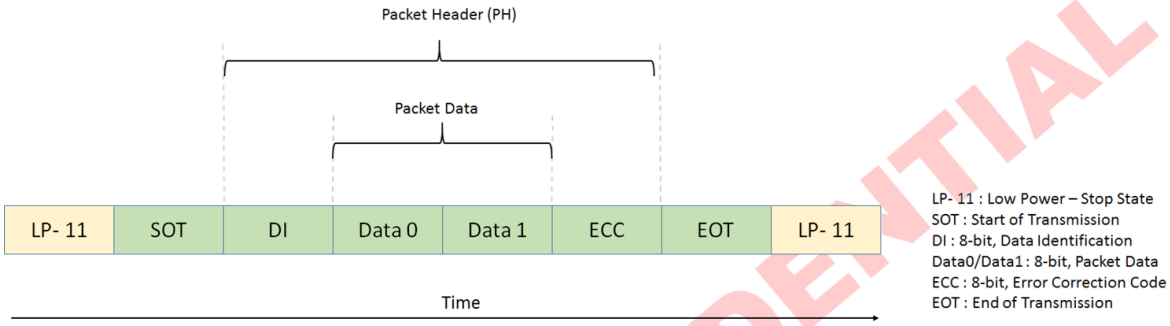
5.6.3 Packet Level Communication

5.6.3.1 Short Packet (SPa) and Long Packet (LPa) Structures

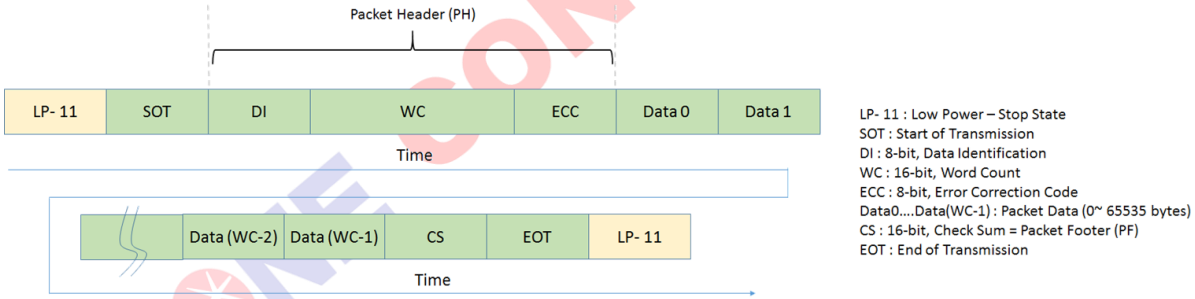
Short Packet (SPa) and Long Packet (LPa) are always used when data transmission is done in Low Power Data Transmission (LPDT) or High-Speed Data Transmission (HSDT) modes. The lengths of the packets are:

- Short Packet (SPa): 4 bytes.
- Long Packet (LPa): 6 to 65,541 bytes.

The type (SPa or LPa) of the packet can be recognized from their package headers (PH).



Short Packet (SPa) Structure



Long Packet (LPa) Structure

Notes 1. *Short Packet (SPa) Structure and Long Packet (LPa) Structure present a single packet sending (= Includes LP-11, SOT and EOT for each packet sending).*

Notes 2. *The other possibility is that SOT, EOT and LP-11 are not needed between packets if packets are sent in multiple packet format, e.g:*

- *LP-11 → SOT → SPa → LPa → SPa → SPa → EOT → LP-11*
- *LP-11 → SOT → SPa → SPa → SPa → EOT → LP-11*
- *LP-11 → SOT → LPa → LPa → LPa → EOT → LP-11*

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5.6.3.2 Bit Order of the Byte on Packet

The bit order of the byte, what is used in packets, is that the Least Significant Bit (LSB) of the byte is sent first, and the Most Significant Bit (MSB) is sent last. The order is illustrated for reference purposes below.

DI (Data Identification)								WC - LSB (Word Count – LSB)								WC – MSB (Word Count – MSB)								ECC (Error Correction Code)							
8'b 29H								8'b 01H								8'b 00H								8'b 06H							
1	0	0	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Bit order of the byte on packet

5.6.3.3 Byte Order of the Multiple Byte Information on Packets

Byte order of the multiple bytes information, what is used in packets, is that the Least Significant (LS) Byte of the information is sent first and the Most Significant (MS) Byte is sent last. For example, Word Count (WC) consists of 2 bytes (= 16 bits); while the LS byte is sent first and the MS byte is sent last. The order is illustrated for reference purposes below.

WC - LSB (Word Count – LSB)								WC – MSB (Word Count – MSB)							
8'b 01H								8'b 00H							
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB

Time

Order of the multiple byte information on packets

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5.6.3.4 Packet Header (PH)

The packet header always consists of 4 bytes. The content of these 4 bytes are different for Short Packet (SPa) and Long Packet (LPa).

- Short Packet (SPa) :
  - 1st byte: Data Identification (DI) => Identify that this is a Short Packet (SPa).
  - 2nd and 3rd bytes: Packet Data (PD), Data 0 and 1.
  - 4th byte: Error Correction Code (ECC).

DI (Data Identification)								Data 0 (Packet Data)								Data 1 (Packet Data)								ECC (Error Correction Code)							
8'b 15H								8'b 3AH								8'b 07H								8'b 18H							
1	0	1	0	1	0	0	0	0	1	0	1	1	1	0	0	1	1	1	0	0	0	0	0	0	0	0	1	1	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Packet Header (PH) in a Short Packet (SPa)

- Long Packet (LPa) :
  - 1st byte: Data Identification (DI) => Identify that this is a Long Packet (LPa).
  - 2nd and 3rd bytes: Word Count (WC).
  - 4th byte: Error Correction Code (ECC).

DI (Data Identification)								WC - LSB (Word Count – LSB)								WC – MSB (Word Count – MSB)								ECC (Error Correction Code)							
8'b 29H								8'b 01H								8'b 00H								8'b 06H							
1	0	0	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Packet Header (PH) in a Long Packet (LPa)

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5.6.3.5 Data Identification (DI)

Data Identification (DI) is a part of the Packet Header (PH), and it consists of 2 parts:

- Virtual Channel (VC), 2 bits, DI [7...6].
- Data Type (DT), 6 bits, DI [5…0].

The Data Identification (DI) structure is illustrated, see the figure below.

DI (Data Identification)							
VC (Virtual Channel Identifier)		DT (Data Type)					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Data Identification (DI) Structure

Data Identification (DI) in the Packet Header (PH) is illustrated for reference purposes below.

DI (Data Identification)								WC - LSB (Word Count – LSB)								WC – MSB (Word Count – MSB)								ECC (Error Correction Code)							
8’b 29H								8’b 01H								8’b 00H								8’b 06H							
1	0	0	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Data Identification (DI) on the Packet Header (PH)

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5.6.3.6 Virtual Channel (VC)

Virtual Channel (VC) is a part of Data Identification (DI [7:6]) structure, and it is used to address where a packet is to be sent from the MCU. Bits of the Virtual Channel (VC) are illustrated for reference purposes below.

DI (Data Identification)								WC - LSB (Word Count – LSB)								WC – MSB (Word Count – MSB)								ECC (Error Correction Code)							
8'b 29H								8'b 01H								8'b 00H								8'b 06H							
1	0	0	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

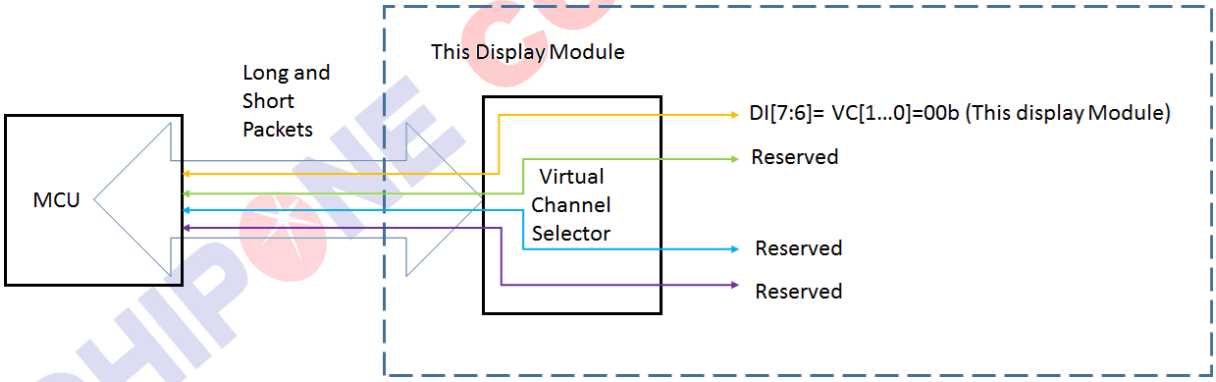
Time

Virtual Channel (VC) on the Packet Header (PH)

Virtual Channel (VC) can assign 4 different channels for 4 different display modules. Devices will use the same virtual channel as which the MCU uses to send packets to them, e.g.

- The MCU uses the virtual channel 0 when it sends packets to the ICNA3312.
- The ICNA3312 also uses the virtual channel 0 when it sends packets to the MCU.

This functionality is illustrated below.



Illustrate of Virtual Channel (VC)

Virtual Channel (VC) is always 0 (DI [7:6] = VC [1:0] = 00b) when the MCU sends "End of Transmission Packet" to the display module. See the section "End of Transmission Packet (EoTP)". This display module does not support the virtual channel selector for other devices (1 to 3) when the only possible virtual channel (VC [1:0]) is 00b for the ICNA3312.

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5.6.3.7 Data Type (DT)

Data Type (DT) is a part of Data Identification (DI [5…0]) structure, and it is used to define the type of the used data in a packet. Bits of the Data Type (DT) are illustrated for reference purposes below.

DI (Data Identification)								WC - LSB (Word Count – LSB)								WC – MSB (Word Count – MSB)								ECC (Error Correction Code)							
8'b 29H								8'b 01H								8'b 00H								8'b 06H							
1	0	0	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Data Type (DT) on the Packet Header (PH)

This Data Type (DT) also defines the used packet is a Short Packet (SPa) or a Long Packet (LPa). Data Types (DT) are different from the MCU to the display module (or other devices) and vice versa. These Data Types (DT) are defined in the tables below.

Data Types (DT) define List

From the MCU to the Display Module		
Hex	Description	Short / Long Packet
01	Sync Even, V Sync Start	SPa (Short Packet)
11	Sync Even, V Sync End	SPa (Short Packet)
21	Sync Even, H Sync Start	SPa (Short Packet)
31	Sync Even, H Sync End	SPa (Short Packet)
08	End of Transmission Packet (EOTP) Note1	SPa (Short Packet)
02	Color Mode Off Command	SPa (Short Packet)
12	Color Mode On Command	SPa (Short Packet)
22	Shut Down Peripheral Command	SPa (Short Packet)
32	Turn On Peripheral Command	SPa (Short Packet)
03	Generic Short WRITE, no parameters	SPa (Short Packet)
13	Generic Short WRITE, 1 parameters	SPa (Short Packet)
23	Generic Short WRITE, 2 parameters	SPa (Short Packet)
04	Generic Short READ, no parameters	SPa (Short Packet)
14	Generic Short READ, 1 parameters	SPa (Short Packet)
24	Generic Short READ, 2 parameters	SPa (Short Packet)
05	DCS Write, No Parameter	SPa (Short Packet)
15	DCS Write, 1 Parameter	SPa (Short Packet)
06	DCS Read, No Parameter	SPa (Short Packet)
37	Set Maximum Return Packet Size	SPa (Short Packet)

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From the MCU to the Display Module		
09	Null Packet, No Data, Note2	LPa (Long Packet)
19	Blanking Packet, no data	LPa (Long Packet)
29	Generic Long Write	LPa (Long Packet)
39	DCS Write Long	LPa (Long Packet)
1E	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	LPa (Long Packet)
2E	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	LPa (Long Packet)
3E	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	LPa (Long Packet)
X0 XF	DO NOT USE All unspecified codes are reserved	

Note 1: *This can be used when the MCU wants to make sure that it is the end of the transmission in High Speed Data Transferring (HSDT) mode.*

Note 2. *This can be used when data lanes are to be kept in High Speed Data Transferring (HSDT) Mode.*

Data Type (DT) from the Display Module (or Other Devices) to the MCU.

Data Type (DT) from the Display Module (or Other Devices) to the MCU

From the Display Module to the MCU		
Hex	Description	Short / Long Packet
02h	Acknowledge with Error Report	SPa (Short Packet)
1Ch	DCS Read Long Response	LPa (Long Packet)
21h	DCS Read Short Response, 1 byte returned	SPa (Short Packet)
22h	DCS Read Short Response, 2 byte returned	SPa (Short Packet)
1Ah	Generic Read Long Response	LPa (Long Packet)
11h	Generic Read Short Response, 1 byte returned	SPa (Short Packet)
12h	Generic Read Short Response, 2 byte returned	SPa (Short Packet)

Note: *The data type for Generic write/read: 1Ah, 11h, 12 will be disable (ignored packet) if bit DSIG is set to "0".*

The receiver will ignore other Data Type (DT) if they are not defined on tables: "Data Type (DT) from the MCU to the Display Module (or Other Devices)" or "Data Type (DT) from the Display Module (or Other Devices) to the MCU".

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5.6.3.8 Packet Data (PD) in a Short Packet (SPa)

Packet Data (PD) of the Short Packet (SPa) is placed after Data Type (DT) of the Data Identification (DI) and indicates a Short Packet (SPa) is to be sent. Packet Data (PD) of a Short Packet (SPa) consists of 2 data bytes: Data 0 and Data 1. The sending order of the Packet Data (PD) is that Data 0 is sent first and the Data 1 is sent last. Bits of Data 1 are set to 0 if the information length is 1 byte. Packet Data (PD) of a Short Packet (SPa), when the length of the information is 1 or 2 bytes and Virtual Channel (VC) is 0, are illustrated for reference purposes below.

- Packet Data (PD) information:
  - Data 0: 26Hex (Display Command Set (DCS) with 1 Parameter => DI (Data Type (DT)) = 15Hex).
  - Data 1: 01Hex (DCS's Parameter).

DI (Data Identification)								Data 0 (Packet Data)								Data 1 (Packet Data)								ECC (Error Correction Code)							
8'b 15H								8'b 26H								8'b 01H								8'b 3EH							
1	0	1	0	1	0	0	0	0	1	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Packet Data (PD) for Short Packet (SPa), 2 Bytes Information

- Packet Data (PD) information:
  - Data 0: 10Hex (DCS without Parameter => DI (Data Type (DT)) = 05Hex).
  - Data 1: 00Hex (Null).

DI (Data Identification)								Data 0 (Packet Data)								Data 1 (Packet Data)								ECC (Error Correction Code)							
8'b 05H								8'b 10H								8'b 00H								8'b 2CH							
1	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Packet Data (PD) for Short Packet (SPa), 1 Byte Information

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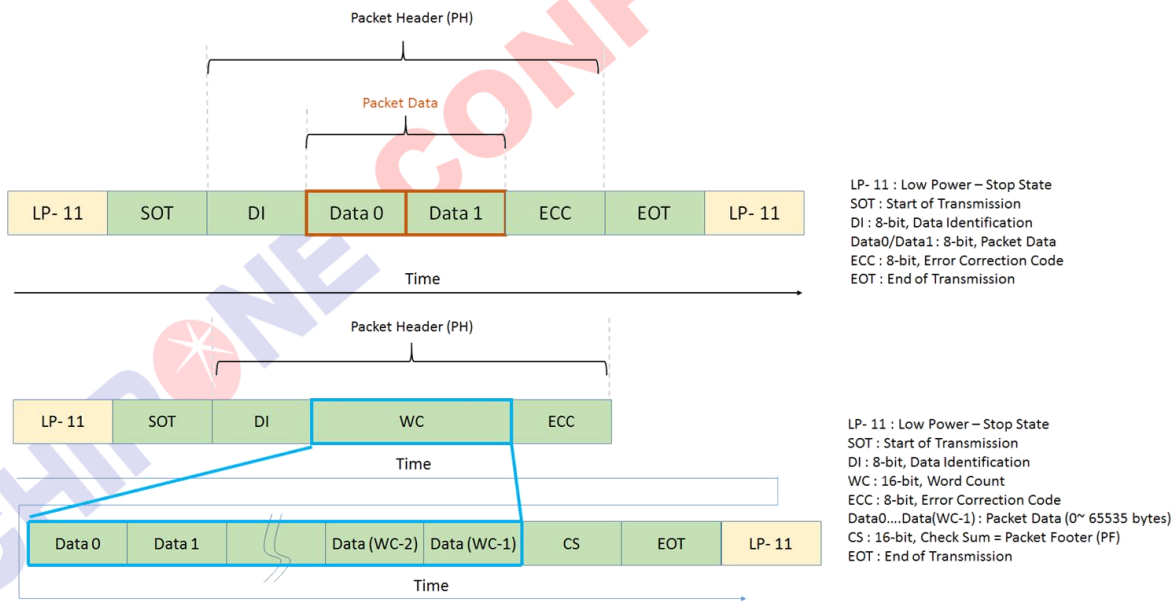
5.6.3.9 Word Count (WC) in a Long Packet (LPa)

Word Count (WC) of the Long Packet (LPa) is placed after Data Type (DT) of the Data Identification (DI) and indicates that a Long Packet (LPa) is to be sent. Word Count (WC) indicates the amount of data bytes of the Packet Data (PD) that is to be sent after the Packet Header (PH). The location of the Word Count (WC) in a Long Packet is the same as which of the Packet Data (PD) in a Short Packet (SPa), as shown in Figure 5.4.9-2. Word Count (WC) of the Long Packet (LPa) consists of 2 bytes. The sending order of these 2 bytes of the Word Count (WC) is that the Least Significant (LS) Byte is sent first, and the Most Significant (MS) Byte is sent last. Word Count (WC) of a Long Packet (LPa) is illustrated for reference purposes below.

DI (Data Identification)								WC - LSB (Word Count – LSB)								WC – MSB (Word Count – MSB)								ECC (Error Correction Code)							
8’b 29H								8’b 01H								8’b 00H								8’b 06H							
1	0	0	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Word Count (WC) in a Long Packet (LPa)



Packet Data in Short and Long Packets

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5.6.3.10 Error Correction Code (ECC)

The Error Correction Code (ECC) is a part of Packet Header (PH) and its purpose is to identify an error or errors. The ECC protects the following fields:

- Short Packet (SPa): Data Identification (DI) byte (8 bits: D [0…7]), Packet Data (PD) bytes (16 bits: D [8…23]) and ECC (8 bits: P [0…7]).
- Long Packet (LPa): Data Identification (DI) byte (8 bits: D [0…7]), Word Count (WC) bytes (16 bits: D [8…23]) and ECC (8 bits: P [0…7]) D [23…0] and P [7…0] are illustrated for reference purposes below.

DI (Data Identification)								Data 0 (Packet Data)								Data 1 (Packet Data)								ECC (Error Correction Code)							
8’b 05H								8’b 10H								8’b 00H								8’b 2CH							
1	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

D [23:0] and D 7:0] in a Short Packet (SPa)

DI (Data Identification)								WC - LSB (Word Count – LSB)								WC – MSB (Word Count – MSB)								ECC (Error Correction Code)							
8’b 29H								8’b 01H								8’b 00H								8’b 06H							
1	0	0	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

D [23:0] and D 7:0] in a Long Packet (LPa)

Error Correction Code (ECC) can recognize one or several error(s) and can only correct one-bit error. Bits (P [7…0]) of the Error Correction Code (ECC) are defined, where the symbol „^" presents the XOR function (Pn is 1 if there is odd number of 1, and Pn is 0 if there is even number of 1) as follows.

- P7 = 0.
- P6 = 0.
- P5 = D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23.
- P4 = D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23.
- P3 = D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23.
- P2 = D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22.
- P1 = D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23.
- P0 = D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23.

P7 and P6 are set to 0 because Error Correction Code (ECC) is based on 64 bit value (D

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[63…0]), but this implementation is based on 24 bit value (D [23…0]). Therefore, only 6 bits are needed (P [5…0]) for Error Correction Code (ECC).

DI (Data Identification)								Data 0								Data 1								ECC (Error Correction Code)							
8'b 05H								8'b 10H								8'b 00H								8'b 2CH							
1	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0
D0	D1	D2		D4	D5		D7			D10	D11		D13			D16				D20	D21	D22	D23	P0							
D0	D1		D3	D4		D6		D8		D10		D12		D14			D17			D20	D21	D22	D23		P1						
D0		D2	D3		D5	D6			D9		D11	D12			D15			D18		D20	D21	D22				P2					
	D1	D2	D3				D7	D8	D9				D13	D14	D15				D19	D20	D21		D23				P3				
				D4	D5	D6	D7	D8	D9							D16	D17	D18	D19	D20		D22	D23					P4			
										D10	D11	D12	D13	D14	D15	D16	D17	D18	D19		D21	D22	D23						P5		
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

XOR Function on Short Packet (SPa)

DI (Data Identification)								WC - LSB (Word Count – LSB)								WC – MSB (Word Count – MSB)								ECC (Error Correction Code)							
8'b 29H								8'b 01H								8'b 00H								8'b 06H							
1	0	0	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
D0	D1	D2		D4	D5		D7			D10	D11		D13			D16				D20	D21	D22	D23	P0							
D0	D1		D3	D4		D6		D8		D10		D12		D14			D17			D20	D21	D22	D23		P1						
D0		D2	D3		D5	D6			D9		D11	D12			D15			D18		D20	D21	D22				P2					
	D1	D2	D3				D7	D8	D9				D13	D14	D15				D19	D20	D21		D23				P3				
				D4	D5	D6	D7	D8	D9							D16	D17	D18	D19	D20		D22	D23					P4			
										D10	D11	D12	D13	D14	D15	D16	D17	D18	D19		D21	D22	D23						P5		
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

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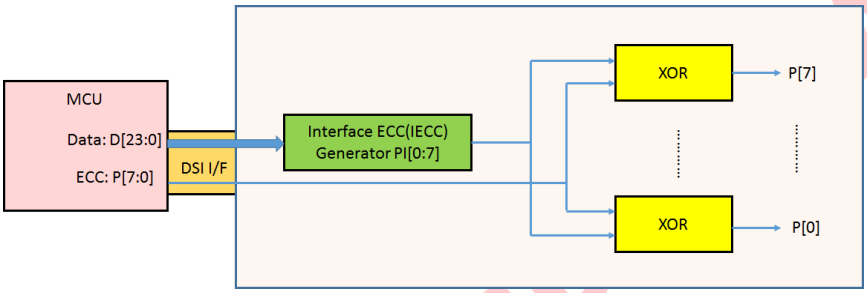
Time

XOR Function on Long Packet (LPa)

The transmitter (= the MCU or the Display Module) will send data bits D [23…0] and Error Correction Code (ECC) P [7…0]. The receiver (= the Display module or the MCU) will calculate the Internal Error Correction Code (IECC) and compare the received Error Correction Code (ECC) and the Internal Error Correction Code (IECC). This comparison is done when each power bit of ECC and IECC have performed the XOR function. The result of this function is PO [7…0]. This functionality, where the transmitter is the MCU and the receiver is the display module, is illustrated for reference purposes below.



Internal Error Correction Code (IECC) on the Display Module (= the Receiver)

The sent data bits (D [23…0]) and ECC (P [7…0]) are correctly received if the value of the PO [7…0]) is 00h.

The sent data bits (D [23…0]) and ECC (P [7…0]) are not correctly received if the value of the PO [7…0]) is not 00h.

ECC P [7:0]	1	1	0	0	0	0	0	0	03h
IECC PI [7:0]	1	1	0	0	0	0	0	0	03h
XOR (ECC, IECC) => PO[7:0]	0	0	0	0	0	0	0	0	= 00h => No Error
	L S B							M S B	

Internal XOR Calculation between ECC and IECC Values – No Error

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ECC P [7:0]	1	1	0	0	0	0	0	0	03h
IECC PI [7:0]	1	1	1	1	0	0	0	0	0Fh
XOR (ECC, IECC) => PO[7:0]	0	0	1	1	0	0	0	0	= 0Ch => Error
	L S B							M S B	

Internal XOR Calculation between ECC and IECC Values – Error

The received Error Correction Code (ECC) can be 00h when the Error Correction Code (ECC) function is not used for data values D [23…0] on the transmitter side. The number of the errors (one or more) can be defined when the value of the PO [7…0] is compared to the values in the following table.

The number of the errors define

Data Bit	PO7	PO6	PO5	PO4	PO3	PO2	PO1	PO0	Hex
D [0]	0	0	0	0	0	1	1	1	07h
D [1]	0	0	0	0	1	0	1	1	0Bh
D [2]	0	0	0	0	1	1	0	1	0Dh
D [3]	0	0	0	0	1	1	1	0	0Eh
D [4]	0	0	0	1	0	0	1	1	13h
D [5]	0	0	0	1	0	1	0	1	15h
D [6]	0	0	0	1	0	1	1	0	16h
D [7]	0	0	0	1	1	0	0	1	19h
D [8]	0	0	0	1	1	0	1	0	1Ah
D [9]	0	0	0	1	1	1	0	0	1Ch
D [10]	0	0	1	0	0	0	1	1	23h
D [11]	0	0	1	0	0	1	0	1	25h
D [12]	0	0	1	0	0	1	1	0	26h
D [13]	0	0	1	0	1	0	0	1	29h
D [14]	0	0	1	0	1	0	1	0	2Ah
D [15]	0	0	1	0	1	1	0	0	2Ch
D [16]	0	0	1	1	0	0	0	1	31h
D [17]	0	0	1	1	0	0	1	0	32h
D [18]	0	0	1	1	0	1	0	0	34h
D [19]	0	0	1	1	1	0	0	0	38h
D [20]	0	0	0	1	1	1	1	1	1Fh
D [21]	0	0	1	0	1	1	1	1	2Fh
D [22]	0	0	1	1	0	1	1	1	37h
D [23]	0	0	1	1	1	0	1	1	3Bh

An error is detected if the value of the PO [7…0] is in Table, and the receiver can correct this one bit error because this found value also defines the location of the corrupt bit, e.g.

- PO [7…0] = 0Eh.
- The bit of the data (D [23…0]), that is not correct, is D [3] More than one error is detected if the value of the PO [7…0] is not in Table for example, PO [7…0] = 0Ch.

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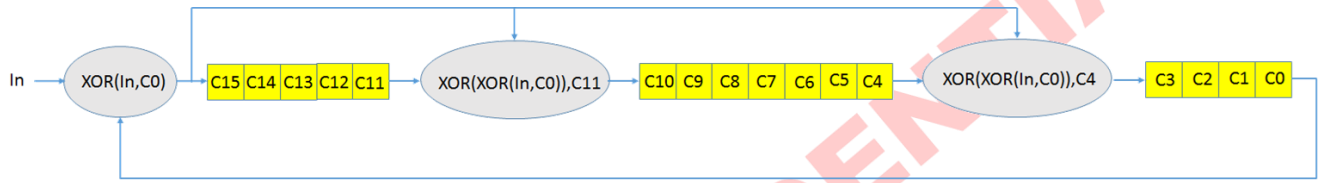
5.6.3.11 Packet Data (PD) in a Long Packet (LPa)

Packet Data (PD) of a Long Packet (LPa) is placed after the Packet Header (PH) of a Long Packet (LPa). The amount of the data bytes is defined in the section “Word Count (WC) in a Long Packet (LPa)”.

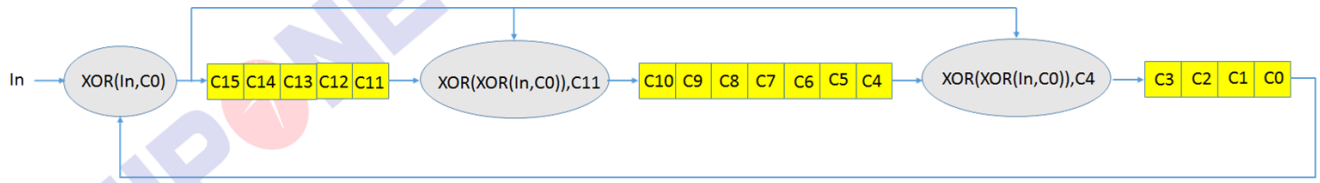
5.6.3.12 Packet Footer (PF) in a Long Packet (LPa)

Packet Footer (PF) of a Long Packet (LPa) is placed after the Packet Data (PD) of a Long Packet (LPa). The Packet Footer (PF) is a checksum value that is calculated from the Packet Data of the Long Packet (LPa). The checksum uses a 16-bit Cyclic Redundancy Check (CRC) value which is generated by a polynomial X16+X12+X5+X0, as illustrated below.



16-bit Cyclic Redundancy Check (CRC) Calculation

The 16-bit Cyclic Redundancy Check (CRC) generator is initialized to FFFFh before calculations. The Most Significant Bit (MSB) of the data byte of the Packet Data (PD) is the first bit which is inputted into the 16-bit Cyclic Redundancy Check (CRC). An example of the 16-bit Cyclic Redundancy Check (CRC), where the Packet Data (PD) of a Long Packet (LPa) is 01h, is illustrated (step-by-step) below.



Step	In	XOR(in,C0)	C15	C14	C13	C12	C11	XOR(XOR(In,C0),C11,(Step-1))	C10	C9	C8	C7	C6	C5	C4	XOR(XOR(In,C0),C4,(Step-1))	C3	C2	C1	C0	C0
0	X	X	1	1	1	1	1	X	1	1	1	1	1	1	1	X	1	1	1	1	X
1	1(LSB)	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2	0	1	1	0	1	1	1	0	0	1	1	1	1	1	1	0	0	1	1	1	1
3	0	1	1	1	0	1	1	0	0	0	1	1	1	1	1	0	0	0	1	1	1
4	0	1	1	1	1	0	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1
5	0	1	1	1	1	1	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0
6	0	0	0	1	1	1	1	0	0	0	0	0	0	1	1	0	1	0	0	0	0
7	0	0	0	0	1	1	1	1	1	0	0	0	0	0	1	0	1	1	0	0	0
8	0(MSB)	0	0	0	0	1	1	1	1	1	0	0	0	0	0	1	1	1	1	0	0
	1byte	CRC result	0	0	0	1	1		1	1	0	0	0	0	0		1	1	1	0	
			MSB																	LSB	

CRC Calculation – Packet Data (PD) is 01h

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The value of the Packet Footer (PF) is 1E0Eh in this example (Command 01h has been sent), and is illustrated below.

DI (Data Identification)								WC - LSB (Word Count – LSB)								WC – MSB (Word Count – MSB)								ECC (Error Correction Code)							
8’b 39H								8’b 01H								8’b 00H								8’b 15H							
1	0	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Data 0 (Packet Data)								CRC- LSB								CRC- MSB							
8’b 00H								8’b 0EH								8’b 1EH							
0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	1	1	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB

Time

Packet Footer (PF) Example

The receiver calculates its checksum value from the received Packet Data (PD). The receiver compares its checksum and the Packet Footer (PF) that the transmitter has sent. The received Packet Data (PD) and Packet Footer (PF) are correct if the checksum of the receiver and Packet Footer (PF) are equal. The received Packet Data (PD) and Packet Footer (PF) are not correct if the checksum of the receiver and Packet Footer (PF) are not equal.

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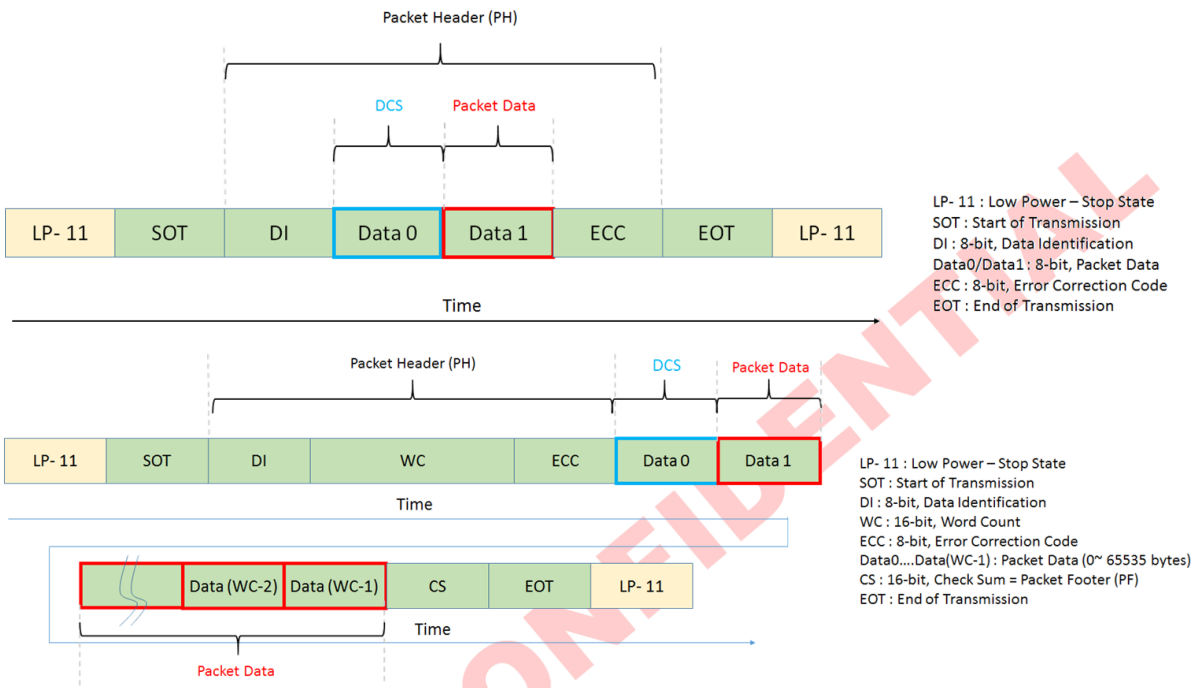
5.6.4 Packet Transmissions

5.6.4.1 Display Command Set (DCS)

Display Command Set (DCS), defined in the section “Command 1 Description”, is used from the MCU to the display module. This Display Command Set (DCS) is always defined in the Data 0 of the Packet Data (PD), and is included in Short Packet (SPa) and Long packet (LPa), as illustrated below.



Display Command Set (DCS) in Short Packet (SPa) and Long Packet (LPa)

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5.6.4.2 Display Command Set (DCS) Write, No Parameter (DSCWN-S)

"Display Command Set (DCS) Write, No Parameter", which is defined in Data Type (DT, 00 0101b), is always used in a Short Packet (SPa) from the MCU to the display module. These commands are defined in a table below:

DSCWN-S Commands

Command
NOP (00h)
Software Reset (01h)
Sleep In (10h)
Sleep Out (11h)
Normal Display Mode On (13h)
INVOff (20h)
INVOn (21h)
All Pixel Off (22h)
All Pixel On (23h)
Display Off (28h)
Display On (29h)
Tearing Effect Line Off (34h)
Idle Mode Off (38h)
Idle Mode On (39h)

A Short Packet (SPa) is defined as:

- Data Identification (DI):
  - Virtual Channel (VC, DI [7…6]): 00b.
  - Data Type (DT, DI [5…0]): 00 0101b.
- Packet Data (PD):
  - Data 0: "Sleep In (10h)", Display Command Set (DCS).
  - Data 1: Always 00hex.
- Error Correction Code (ECC).

DI (Data Identification)								Data 0 (Packet Data)								Data 1 (Packet Data)								ECC (Error Correction Code)							
8'b 05H								8'b 10H								8'b 00H								8'b 2CH							
1	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Display Command Set (DCS) Write, No Parameter (DCSWN-S) – Example

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5.6.4.3 Display Command Set (DCS) Write, 1 Parameter (DSCW1-S)

"Display Command Set (DCS) Write, 1 Parameter" (DCSW1-S), which is defined in Data Type (DT, 01 0101b), is always used in a Short Packet (SPa) from the MCU to the display module. These commands are defined in the table below.

DSCW1-S Commands

Command
Gamma Curve Set (26h)
TEON (35h)
MADCTR (36h)
COLMOD (3Ah)
WRDISBV (51h)
WRCTRLD (53h)
WRCABC (55h)
WRCABCMB (5Eh)

Short Packet (SPa) is defined e.g.

- Data Identification (DI):
  - Virtual Channel (VC, DI[7…6]): 00b.
  - Data Type (DT, DI[5…0]): 01 0101b.
- Packet Data (PD):
  - Data 0: "PMCSET (3Ah)", Display Command Set (DCS).
  - Data 1: 01hex, Parameter of the DCS.
- Error Correction Code (ECC).

This is defined on the Short Packet (SPa) as follows.

DI (Data Identification)								Data 0 (Packet Data)								Data 1 (Packet Data)								ECC (Error Correction Code)							
8'b 15H								8'b 3AH								8'b 01H								8'b 1EH							
1	0	1	0	1	0	0	0	1	0	1	0	1	1	0	0	1	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Display Command Set (DCS) Write, 1 Parameter (DCSW1-S) – Example

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5.6.4.4 Display Command Set (DCS) Write, Long (DCSW-L)

"Display Command Set (DCS) Write Long" (DCSW-L), which is defined in Data Type (DT, 11 1001b), is always used in a Long Packet (LPa) from the MCU to the display module. Command (No Parameters) and Write (1 or more parameters) are defined in a table below.

DCSW-L Commands

Command
NOP (00h) Note 1
Software Reset (01h), Note 1
Sleep In (10h) , Note 1
Sleep Out (11h) , Note 1
Normal Display Mode On (13h) , Note 1
INVOff (21h) , Note 1
INVOn (22h) , Note 1
All Pixel Off (22h) , Note 1
All Pixel On (23h) , Note 1
GAMSET (26h) , Note 2
Display Off (28h) , Note 1
Display On (29h) , Note 1
Tearing Effect Line Off (34h) , Note 1
Tearing Effect Line On (35h) , Note 2
MADCTR (36h)
Idle Mode Off (38h) , Note 1
Idle Mode On (39h) , Note 1
COLMOD (3Ah) , Note 2
Tearline (44h)
WRDISBV (51h) , Note 2
WRCTRLD (53h)
WRCABC (55h) , Note 2
WRCABCMB (5Eh)

Notes 1. *Also Long Packet (LPa) can be used; See Display Command Set (DCS) Write, No Parameter.*

Notes 2. *Also Long Packet (LPa) can be used; See Display Command Set (DCS) Write, 1 Parameter.*

Long Packet (LPa), when a command (No Parameter) was sent, is defined e.g.

- Data Identification (DI):
  - Virtual Channel (VC, DI[7…6]): 00b.
  - Data Type (DT, DI[5…0]): 11 1001b.
- Word Count (WC):
  - Word Count (WC): 0001h.
- Error Correction Code (ECC).
- Packet Data (PD):
  - Data 0: "Sleep In (10h)", Display Command Set (DCS).
- Packet Footer (PF).

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This is defined on the Long Packet (LPa) as follows.

DI (Data Identification)								WC - LSB (Word Count – LSB)								WC – MSB (Word Count – MSB)								ECC (Error Correction Code)							
8’b 39H								8’b 01H								8’b 00H								8’b 15H							
1	0	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Data 0 (Packet Data)								CRC- LSB								CRC- MSB							
8’b 10H								8’b 06H								8’b 1FH							
0	0	0	0	1	0	0	0	0	1	1	0	0	0	0	0	1	1	1	1	1	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB

Time

Display Command Set (DCS) Write, Long (DCSWL-S) with DCS Only– Example

A Long Packet (LPa) with one Write (1 parameter) is defined as:

- Data Identification (DI):
  - Virtual Channel (VC, DI [7…6]): 00b.
  - Data Type (DT, DI [5…0]): 11 1001b.
- Word Count (WC):
  - Word Count (WC): 0002h.
- Error Correction Code (ECC).
- Packet Data (PD):
  - Data 0: “Gamma Set (26h)”, Display Command Set (DCS).
  - Data 1: 01hex, Parameter of the DCS.
- Packet Footer (PF).

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DI (Data Identification)								WC – LSB (Word Count – LSB)								WC – MSB (Word Count – MSB)								ECC (Error Correction Code)							
8'b 39H								8'b 05H								8'b 00H								8'b 36H							
1	0	0	1	1	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Data 0 (DCS)								Data 1 (1st Parameter)								Data 2 (2nd Parameter)								Data 3 (3rd Parameter)							
8'b 2AH								8'b 00H								8'b 12H								8'b 01H							
0	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	1	0	0	0	0	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Data 4 (4th Parameter)								CRC – LSB								CRC – MSB							
8'b EFH								8'b BDH								8'b 2AH							
1	1	1	1	0	1	1	1	1	0	1	1	1	1	0	1	0	1	0	1	0	1	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB

Time

Display Command Set (DCS) Write, Long with DCS and 4 Parameter – Example

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5.6.4.5 Display Command Set (DCS) Read, No Parameter (DCSRN-S)

"Display Command Set (DCS) Read, No Parameter" (DCSRN-S), which is defined in Data Type (DT, 00 0110b), is always used in a Short Packet (SPa) from the MCU to the display module. These commands are defined in the table below.

DCSRN-S Commands

Command
RDDID (04h)
RDDPM (0Ah)
RDDMADCTR (0Bh)
RDDCOLMOD (0Ch)
RDDIM (0Dh)
RDDSM (0Eh)
RDDSDR (0Fh)
GSL (45h)
RDDISBV (52h)
RDCTRLD (54h)
RDCABC (56h)
RDCABCMB (5Fh)
RDID1 (DAh)
RDID2 (DBh)
RDID3 (DCh)

The MCU has to define to the display module the maximum size of the returned packet. The command, which is used for this purpose, is "Set Maximum Return Packet Size" (SMRPS-S), which Data Type (DT) is 11 0111b and is used in a Short Packet (SPa) before the MCU can send "Display Command Set (DCS) Read, No Parameter" to the display module. This sequence is illustrated for reference purposes below.

- Step1

The MCU sends "Set Maximum Return Packet Size" (Short Packet (SPa)) (SMRPS-S) to the display module when it wants to return one byte from the display module.

- Data Identification (DI):
  - Virtual Channel (VC, DI [7…6]): 00b.
  - Data Type (DT, DI [5…0]): 11 0111b.
- Maximum Return Packet Size (MRPS)
  - Data 0: 01h.
  - Data 1: 00h.
- Error Correction Code (ECC).

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DI (Data Identification)								MRPS – LSB								MRPS – MSB								ECC (Error Correction Code)							
8’b 37H								8’b 01H								8’b 00H								8’b 1DH							
1	1	1	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Set Maximum Return Packet Size (SMRPS-S) – Example

- Step 2

The MCU wants to receive the value of the “Read ID1 (DAh)” from the display module when the MCU sends “Display Command Set (DCS) Read, No Parameter” to the display module.

- Data Identification (DI):
  - Virtual Channel (VC, DI [7…6]): 00b.
  - Data Type (DT, DI [5…0]): 00 0110b.
- Packet Data (PD):
  - Data 0: “Read ID1 (DAh)”, Display Command Set (DCS).
  - Data 1: Always 00hex.
- Error Correction Code (ECC).

DI (Data Identification)								Data 0 (DCS)								Data 1 (Always 8’b 00H)								ECC (Error Correction Code)							
8’b 06H								8’b DAH								8’b 00H								8’b 1FH							
0	1	1	0	0	0	0	0	0	1	0	1	1	0	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Display Command Set (DCS) Read, No Parameter (DCSRN – S) – Example

- Step 3

The display module can send 2 different information to the MCU after Bus Turnaround (BTA):

1) An acknowledge with Error Report (AwER), which is used in a Short Packet (SPa), if there is an error when receiving a command. See the section “Acknowledge with Error Report (AwER)”.
2) Information of the received command, which can be a Short Packet (SPa) or a Long Packet (LPa).

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5.6.4.6 Null Packet, No Data (NP-L)

"Null Packet, No Data" (NP-L), which is defined in Data Type (DT, 001001b), is always used in a Long Packet (LPa) from the MCU to the display module. The purpose of this command is to keep data lanes in the high speed mode (HSDT) if necessary. The display module can ignore the Packet Data (PD) that the MCU sends.

A Long Packet (LPa) with 5 random data bytes of the Packet Data (PD) is defined as:

- Data Identification (DI):
  - Virtual Channel (VC, DI [7…6]): 00b.
  - Data Type (DT, DI [5…0]): 001001b.
- Word Count (WC):
  - Word Count (WC): 0005h.
- Error Correction Code (ECC).
- Packet Data (PD):
  - Data 0: 89h (Random data).
  - Data 1: 23h (Random data).
  - Data 2: 12h (Random data).
  - Data 3: A2h (Random data).
  - Data 4: E2h (Random data).
- Packet Footer (PF).

DI (Data Identification)								WC – LSB (Word Count – LSB)								WC – MSB (Word Count – MSB)								ECC (Error Correction Code)							
8'b 09H								8'b 05H								8'b 00H								8'b 30H							
1	0	0	1	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Data 0								Data 1								Data 2								Data 3							
8'b 89H								8'b 23H								8'b 12H								8'b A2H							
1	0	0	1	0	0	0	1	1	1	0	0	0	1	0	0	0	1	0	0	1	0	0	0	0	1	0	0	0	1	0	1
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

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Data 4								CRC – LSB								CRC – MSB							
8'b E2H								8'b 59H								8'b 29H							
0	1	0	0	0	1	1	1	1	0	0	1	1	0	1	0	1	0	0	1	0	1	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB

Time

Null Packet, No Data (NP- L) – Example

5.6.4.7 End of Transmission Packet (EoTP)

"End of Transmission Packet" (EoTP), which is an interface level function and defined in Data Type (DT, 00 1000b), is always used in a Short Packet (SPa) from the MCU to the display module. The purpose of this command is to terminate the high Speed Data Transmission (HSDT) mode properly when EoTP is added after the last payload packet before "End of Transmission" (EoT).The MCU can decide if it wants to use the "End of Transmission Packet" (EoTP) or not. The display shall have the capability to support both. That is, if the MCU applies the EoTP, it shall report the "DSI Protocol Violation Error" when the EoTP is not detected in the High-Speed (HS). The display module error reporting shall be enabled/disabled statistically, according to the module application. The display module does or does not receive "End of Transmission Packet" (EoTP) from the MCU during the Low Power Data Transmission (LPDT) mode before "Mark-1" (= leaving the Escape mode) which ends the Low Power Data Transmission (LPDT) mode. The display module is not allowed to send "End of Transmission Packet" (EoTP) to the MCU during the Low Power Data Transmission (LPDT) mode. The summary of the receiving and transmitting EoTP is listed below.

The summary of the receiving and transmitting EoTP

Direction	Display Module (DM) in High Speed Data Transmission (HSDT)	Display Module (DM) in Low Power Data Transmission (LPDT)
MCU=> Display Module	Support with and without EoTP	Support with and without EoTP
Display Module => MCU	HS mode is not available (EoTP is not available)	EoTP cannot be sent by the Display Module (DM)

A Short Packet (SPa) using a fixed format is as follows:

- Data Identification (DI):
  - Virtual Channel (VC, DI [7…6]): 00b.
  - Data Type (DT, DI [5…0]): 001000b.
- Packet Data (PD):
  - Data 0: 0Fh.
  - Data 1: 0Fh.
- Error Correction Code.

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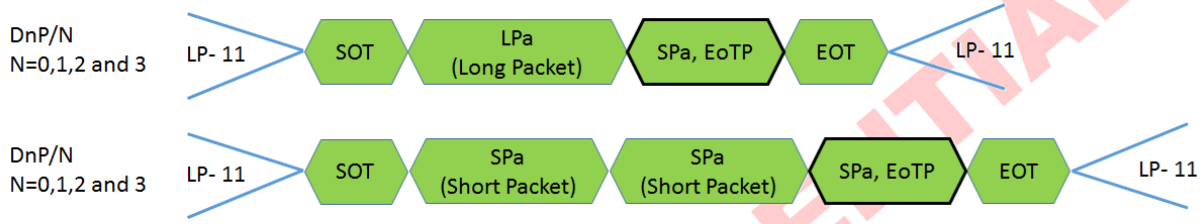
DI (Data Identification)								Data 0								Data 1								ECC (Error Correction Code)							
8'b 08H								8'b 0FH								8'b 0FH								8'b 01H							
0	0	0	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	0	0	0	0	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

End of Transmission Packet (EoTP)

Some examples of the "End of Transmission Packet" (EoTP) are illustrated for reference purposes below.



End of Transmission Packet (EoTP) – Example

5.6.4.8 Acknowledge with Error Report (AwER)

"Acknowledge with Error Report" (AwER), which is defined in Data Type (DT, 00 0010b), is always used in a Short Packet (SPa) from the display module to the MCU. The Packet Data (PD) can include bits, which define the current error, when the corresponding bit is set to 1, as defined in the following table.

Acknowledge with Error Report

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Any Protocol Timer Time-Out
6	False Control Error
7	Contention is Detected on the Display Module
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Checksum Error (Long Packet only)
11	DSI Data Type (DT) Not Recognized
12	DSI Virtual Channel (VC) ID Invalid
13	Invalid Transmission Length
14	Reserved, Set to 0 internally
15	DSI Protocol Violation

These errors are included in all packages that have been received from the MCU to the display module before the Bus Turnaround (BTA). The display module ignores the received

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packet which includes error or errors.

Acknowledge with Error Report (AwER) of a Short Packet (SPa) is defined as:

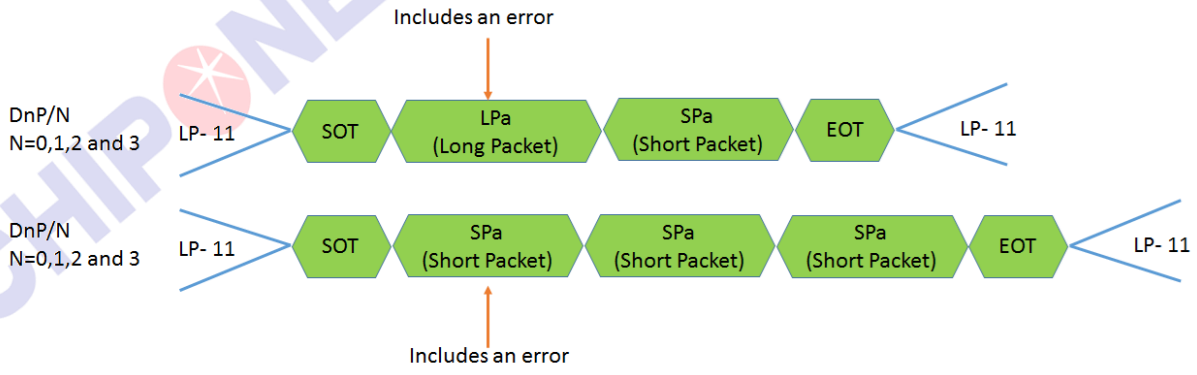
- Data Identification (DI):
  - - Virtual Channel (VC, DI [7…6]): 00b.
  - - Data Type (DT, DI [5…0]): 000010b.
- Packet Data (PD):
  - - Bit 8: ECC Error, single-bit (detected and corrected).
  - - AwER: 0100h.
- Error Correction Code (ECC).

DI (Data Identification)								AwER – LSB								AwER – MSB								ECC (Error Correction Code)							
8'b 02H								8'b 00H								8'b 01H								8'b 3AH							
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	1	1	1	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Acknowledge with Error Report (AwER) – Example

It is possible that the display module receives several packets, which include errors, from the MCU before the MCU performs the Bus Turnaround (BTA). Some examples are illustrated for reference purposes below.



Error Packets

Therefore, a method is needed to check if there are errors in the previous packets. These errors of the previous packets can be detected by "Read Display Signal Mode (0Eh)" and "Read Number of the Errors on DSI (05h)" commands. The bit D0 of the "Read Display Signal Mode (0Eh)" command will be set to 1 if a received packet includes an error. The amount of packets,

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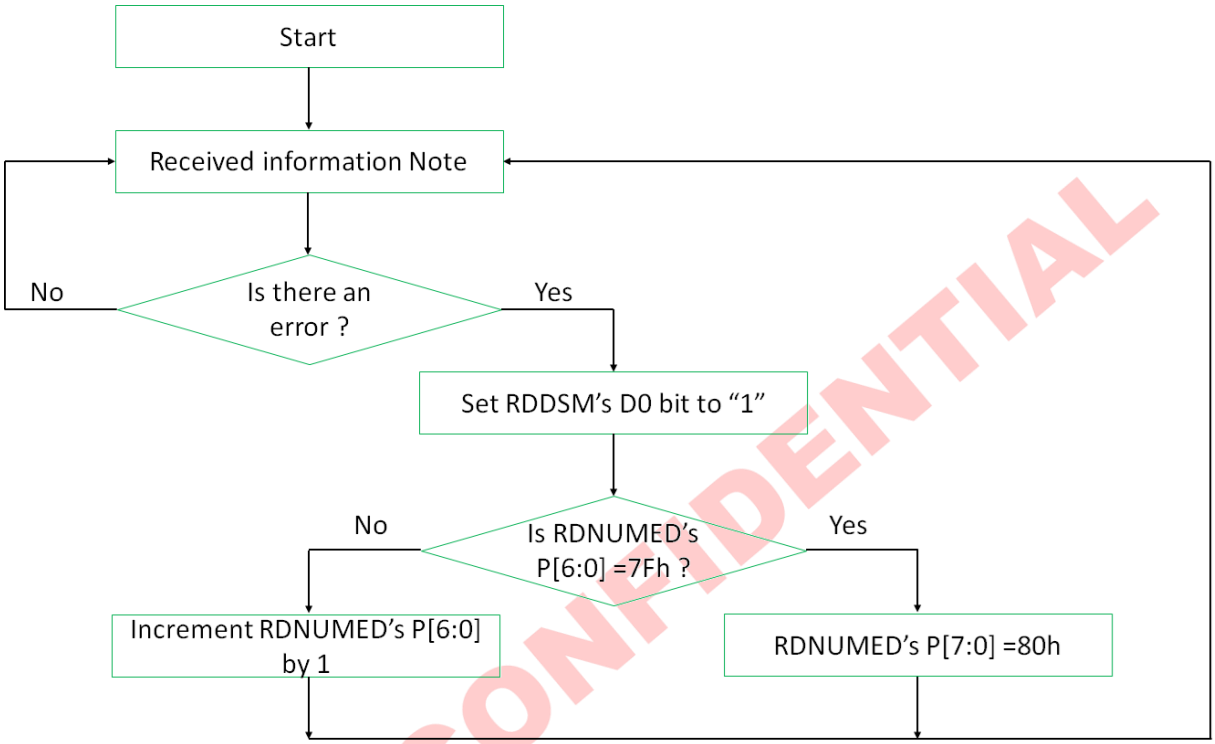
which include an ***ECC*** *or* ***CRC*** error, is calculated in the RDNUMED register, which can read "Read Number of the Errors on DSI (05h)" command. This command also sets the RDNUMED register to 00h and set the bit D0 of the "Read Display Signal Mode (0Eh)" command to 0 after the MCU has read the RDNUMED register from the display module. The functionality of the RDNUMED register is illustrated for reference purposes below.



Flow Chart for Errors on DSI

Notes 1. *This information can be Interface or Packet Level Communication, but it is always from the MCU to the display module.*

Notes 2. *CRC or ECC error*

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5.6.4.9 DCS Read Long Response (DCSRR-L)

"DCS Read Long Response" (DCSRR-L), which is defined in Data Type (DT, 011100b), is always used in a Long Packet (LPa) from the display module to the MCU. "DCS Read Long Response" (DCSRR-L) is used when the display module wants to respond to a DCS Read command, which the MCU has sent to the display module.

A Long Packet (LPa), which includes 5 data bytes of the Packet Data (PD), defined as:

- Data Identification (DI)
- Virtual Channel (VC, DI [7…6]): 00b
- Data Type (DT, DI [5…0]): 01 1100b
- Word Count (WC)
- Word Count (WC): 0005hex
- Error Correction Code (ECC)
- Packet Data (PD):
- Data 0: 89hex
- Data 1: 23hex
- Data 2: 12hex
- Data 3: A2hex
- Data 4: E2hex
- Packet Footer (PF)

DI (Data Identification)								WC – LSB (Word Count – LSB)								WC – MSB (Word Count – MSB)								ECC (Error Correction Code)							
8'b 1CH								8'b 05H								8'b 00H								8'b 29H							
0	0	1	1	1	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Data 0								Data1								Data2								Data3							
8'b 89H								8'b 23H								8'b 12H								8'b A2H							
1	0	0	1	0	0	0	1	1	1	0	0	0	1	0	0	0	1	0	0	1	0	0	0	0	1	0	0	0	1	0	1
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Data 4								CRC – LSB								CRC – MSB							
8'b E2H								8'b 59H								8'b 29H							
0	1	0	0	0	1	1	1	1	0	0	1	1	0	1	0	1	0	0	1	0	1	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB

Time

Figure 5-1 DCS Read Long Response (DCSRR-L) – Example

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5.6.4.10 DCS Read Short Response, 1 Byte Returned (DCSRR1-S)

"DCS Read Short Response, 1 Byte Returned" (DCSRR1-S), which is defined in Data Type (DT, 10 0001b), is always used in a Short Packet (SPa) from the display module to the MCU. "DCS Read Short Response, 1 Byte Returned (DCSRR1-S) is used when the display module wants to respond to a DCS Read command, which the
MCU has sent to the display module.

A Short Packet (SPa) is defined as:

- Data Identification (DI).
- Virtual Channel (VC, DI [7…6]): 00b.
- Data Type (DT, DI [5…0]): 100001b.
- Packet Data (PD).
- Data 0: 45h.
- Data 1: 00h (Always).
- Error Correction Code (ECC).

DI (Data Identification)								Data0 (Packet Data)								Data1 (Always 8'b 00h)								ECC (Error Correction Code)							
8'b 21H								8'b 45H								8'b 00H								8'b 01H							
1	0	0	0	0	1	0	0	1	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

DCS Read Short Response, 1Byte Return (DCSRR1-S) – Example

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5.6.4.11 DCS Read Short Response, 2 Byte Returned (DCSRR2-S)

"DCS Read Short Response, 2 Bytes Returned" (DCSRR2-S), which is defined in Data Type (DT, 10 0010b), is always used in a Short Packet (SPa) from the display module to the MCU. "DCS Read Short Response, 2 Bytes Returned" (DCSRR2-S) is used when the display module wants to respond to a DCS Read command, which the MCU has sent to the display module.

A Short Packet (SPa) is defined as:

- Data Identification (DI).
- Virtual Channel (VC, DI [7…6]): 00b.
- Data Type (DT, DI [5…0]): 10 0010b.
- Packet Data (PD)
- Data 0: 45h.
- Data 1: 32h.
- Error Correction Code (ECC).

DI (Data Identification)								Data 0 (Packet Data)								Data1								ECC (Error Correction Code)							
8'b 22H								8'b 45H								8'b 32H								8'b 0FH							
0	1	0	0	0	1	0	0	1	0	1	0	0	0	1	0	0	1	0	0	1	1	0	0	1	1	1	1	0	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

DCS Read Short Response, 2Byte Returned (DCSRR2-S) – Example

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5.6.5 Communication Sequences

5.6.5.1 General

The communication sequences can be done on interface or packet levels between the MCU and the display module. See sections “Interface Level Communication” and “Packet Level Communication”. This communication sequence description is for DSI data lanes (D0P/N and D1P/N), and it is assumed that the needed low level communication is done on DSI Clock lane (CLKP/N) automatically. See the section “DSI CLK Lanes”. Functions of the interface level communication are described in the following table.

Interface Level Communication

Interface Mode	Abbreviation	Interface Action Description
Low Power	LP-11	Stop state
	LPDT	Low power data transmission
	ULPS	Ultra- Low power state
	RAR	Remote application reset
	TEE	Tearing effect event (Not supported)
	ACK	Acknowledge (No error)
	BTA	Bus turnaround
High Speed	HSDT	High speed data transmission

Functions of the packet level communication are described on the following table.

Packet level communication

Packet Sender	Abbreviation	Packet Size	Packet Description
MCU	DCSW1-S	SPa	DCS Write, 1 Parameter
	DCSWN-S	SPa	DCS Write, No Parameter
	DCSW-L	LPa	DCS Write, Long
	DCSRN-S	SPa	DCS Read, No Parameter
	SMRPS-S	SPa	Set maximum return packet size
	NP-L	LPa	Null packet, No data
Display Module	AwER	SPa	Acknowledge with error report
	DCSRR-L	LPa	DCS Read, Long Response
	DCSRR1-S	SPa	DCS Read, Short Response
	DCSRR2-S	SPa	DCS Read, Short Response

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5.6.5.2 Sequences –DCS Write, 1 Parameter Sequence

A Short Packet (SPa) of “Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)” is defined on chapter “Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)” and example sequences, how this packet is used is described on following tables.

DCS Write,1 parameter Sequence – Example 1

Line	MCU		Interface Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	DCSW1-S	LPDT	→	-	-	
3	-	LP-11	→	-	-	End

DCS Write,1 parameter Sequence – Example 2

Line	MCU		Interface Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	DCSW1-S	HSDT	→	-	-	
3	EoTP	HSDT	→	-	-	End of Transmission Packet
4	-	LP-11	→	-	-	End

DCS Write,1 parameter Sequence – Example 3

Line	MCU		Interface Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	DCSW1-S	HSDT	→	-	-	
3	EoTP	HSDT	→	-	-	End of Transmission Packet
4		LP-11	→			
5		BTA	←/→	BTA		Interface control change from the MCU to the display module
6		-	←	LP-11		If no error => goto line 8 If error => goto line 13
7						
8		-	←	ACK		No error
9		-	←	LP-11		
10		BTA	←/→	BTA		Interface control change from the display module to the MCU
11		LP-11	→	-		End
12						
13		-	←	LPDT	AwER	Error report
14		-	←	LP-11		
15		BTA	←/→	BTA		
16	-	LP-11	→	-	-	End

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5.6.5.3 Sequences –DCS Write, No Parameter Sequence

A Short Packet (SPa) of “Display Command Set (DCS) Write, No Parameter (DCSWN-S)” is defined on chapter “Display Command Set (DCS) Write, No Parameter (DCSWN-S)” and example sequences, how this packet is used, is described on following tables.

DCS Write, No parameter Sequence – Example 1

Line	MCU		Interface Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	DCSWN-S	LPDT	→	-	-	
3	-	LP-11	→	-	-	End

DCS Write, No parameter Sequence – Example 2

Line	MCU		Interface Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	DCSWN-S	HSDT	→	-	-	
3	EoTP	HSDT	→	-	-	End of Transmission Packet
4	-	LP-11	→	-	-	End

DCS Write, No parameter Sequence – Example 3

Line	MCU		Interface Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	DCSWN-S	HSDT	→	-	-	
3	EoTP	HSDT	→	-	-	End of Transmission Packet
4		LP-11	→			
5		BTA	←/→	BTA		Interface control change from the MCU to the display module
6		-	←	LP-11		If no error => goto line 8 If error => goto line 13
7						
8		-	←	ACK		No error
9		-	←	LP-11		
10		BTA	←/→	BTA		Interface control change from the display module to the MCU
11		LP-11	→	-		End
12						
13		-	←	LPDT	AwER	Error report
14		-	←	LP-11		
15		BTA	←/→	BTA		
16	-	LP-11	→	-	-	End

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5.6.5.4 Sequences –DCS Write, Long Sequence

A Long Packet (LPa) of “Display Command Set (DCS) Write Long (DCSW-L)” is defined on chapter “Display Command Set (DCS) Write Long (DCSW-L)” and example sequences, how this packet is used, is described on following tables.

DCS Write, Long Sequence – Example 1

Line	MCU		Interface Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	DCSW-L	LPDT	→	-	-	
3	-	LP-11	→	-	-	End

DCS Write, Long Sequence – Example 2

Line	MCU		Interface Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	DCSW-L	HSDT	→	-	-	
3	EoTP	HSDT	→	-	-	End of Transmission Packet
4	-	LP-11	→	-	-	End

DCS Write, Long Sequence – Example 3

Line	MCU		Interface Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	DCSW-L	HSDT	→	-	-	
3	EoTP	HSDT	→	-	-	End of Transmission Packet
4		LP-11	→			
5		BTA	←/→	BTA		Interface control change from the MCU to the display module
6		-	←	LP-11		If no error => goto line 8 If error => goto line 13
7						
8		-	←	ACK		No error
9		-	←	LP-11		
10		BTA	←/→	BTA		Interface control change from the display module to the MCU
11		LP-11	→	-		End
12						
13		-	←	LPDT	AwER	Error report
14		-	←	LP-11		
15		BTA	←/→	BTA		
16	-	LP-11	→	-	-	End

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Sequences –DCS Read, No Parameter Sequence

A Short Packet (SPa) of “Display Command Set (DCS) Read, No Parameter (DCSRN-S)” is defined on chapter “Display Command Set (DCS) Read, No Parameter (DCSRN-S)” and example sequences, how this packet is used, is described on following tables.

DCS Read, No Parameter Sequence – Example 1

Line	MCU		Interface Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	SMRPS-S	HSDT	→	-	-	Define how many data byte is wanted to read: 1 byte
3	DCSRN-S	HSDT	→	-	-	wanted to get a response ID1 (DAh)
4	EoTP	HSDT	→	-	-	End of Transmission Packet
5	-	LP-11	→	-	-	
6	-	BTA	←/→	BTA	-	Interface control change from the MCU to the display module
7	-	-	←	LP-11	-	If no error => goto line 9 If error => goto line 14 If error is corrected by ECC => go to line 19
8						
9	-	-	←	LPDT	DCSRR1-S	Responded 1 byte return
10	-	-	←	LP-11	-	
11	-	BTA	←/→	BTA	-	Interface control change from the display module to the MCU
12	-	LP-11	→	-	-	End
13						
14	-	-	←	LPDT	AwER	Error report
15	-	-	←	LP-11	-	
16	-	BTA	←/→	BTA	-	Interface control change from the display module to the MCU
17	-	LP-11	→	-	-	End
18						
19	-	-	←	LPDT	DCSRR1-S	Responded 1 byte return
20	-	-	←	LPDT	AwER	Error Report (Error is Corrected by ECC)
21	-	-	←	LP-11	-	
22	-	BTA	←/→	BTA	-	Interface control change from the display module to the MCU
23	-	LP-11	→		-	End

5.6.5.5 Sequences –Null Packet, No Data Sequence

A Long Packet (LPa) of “Null Packet, No Data (NP-L)” is defined on chapter “Null Packet,

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No Data (NP-L)" and example sequences, how this packet is used, is described on following tables.

Null Packet, No Data Sequence – Example

Line	MCU		Interface Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	➔	-	-	Start
2	NP-L	HSDT	➔	-	-	Only high speed data transmission is used.
3	EoTP	HSDT	➔			End of transmission Packet
4	-	LP-11	➔	-	-	End

5.6.5.6 Sequences –End of Transmission Packet

A Short Packet (SPa) of "End of Transmission (EoT)" is defined on chapter "End of Transmission Packet (EoT)" and an example sequences, how this packet is used, is described on following tables.

End of Transmission Packet – Example

Line	MCU		Interface Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	➔	-	-	Start
2	NP-L	HSDT	➔	-	-	Only high speed data transmission is used.
3	EoTP	HSDT	➔			End of transmission Packet
4	-	LP-11	➔	-	-	End

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5.6.6 Video Mode Communication

Video Mode peripherals require pixel data delivered in real time. This section specifies the format and timing of DSI traffic for this type of display module.

5.6.6.1 Transmission Packet Sequences

DSI supports several formats, or packet sequences, for Video Mode data transmission. The peripheral's timing requirements dictate which format is appropriate. In the following sections, *Burst Mode* refers to time-compression of the RGB pixel (active video) portion of the transmission. In addition, these terms are used throughout the following sections:

- Non-Burst Mode with Sync Pulses – enables the peripheral to accurately reconstruct original video timing, including sync pulse widths.
- Non-Burst Mode with Sync Events – similar to above, but accurate reconstruction of sync pulse widths is not required, so a single Sync Event is substituted.
- Burst mode – RGB pixel packets are time-compressed, leaving more time during a scan line for LP mode (saving power) or for multiplexing other transmissions onto the DSI link.

In the following figures the Blanking or Low-Power Interval (BLLP) is defined as a period during which video packets such as pixel-stream and sync event packets are not actively transmitted to the peripheral. To enable PHY synchronization the host processor should periodically end HS transmission and drive the Data Lanes to the LP state. This transition should take place at least once per frame; shown as LPM in the figures in this section. It is recommended to return to LP state once per scan-line during the horizontal blanking time. Regardless of the frequency of BLLP periods, the host processor is responsible for meeting all documented peripheral timing requirements. Note, at lower frequencies BLLP periods will approach, or become, zero, and burst mode will be indistinguishable from non-burst mode.
During the BLLP the DSI Link may do any of the following:

- Remain in Idle Mode with the host processor in LP-11 state and the peripheral in LP-RX.
- Transmit one or more non-video packets from the host processor to the peripheral using Escape Mode.
- Transmit one or more non-video packets from the host processor to the peripheral using HS Mode.
- If the previous processor-to-peripheral transmission ended with BTA, transmit one or more packets from the peripheral to the host processor using Escape Mode.
- Transmit one or more packets from the host processor to a different peripheral using a different Virtual Channel ID.

The sequence of packets within the BLLP or RGB portion of a HS transmission is arbitrary. The host processor may compose any sequence of packets, including iterations, within the limits of the packet format definitions. For all timing cases, the first line of a frame shall start with VS; all other lines shall start with HS. This is also true in the special case when VSA+VBP=0. Note that the position of synchronization packets, such as VS and HS, in time is of utmost importance since this has a direct impact on the visual performance of the display panel.

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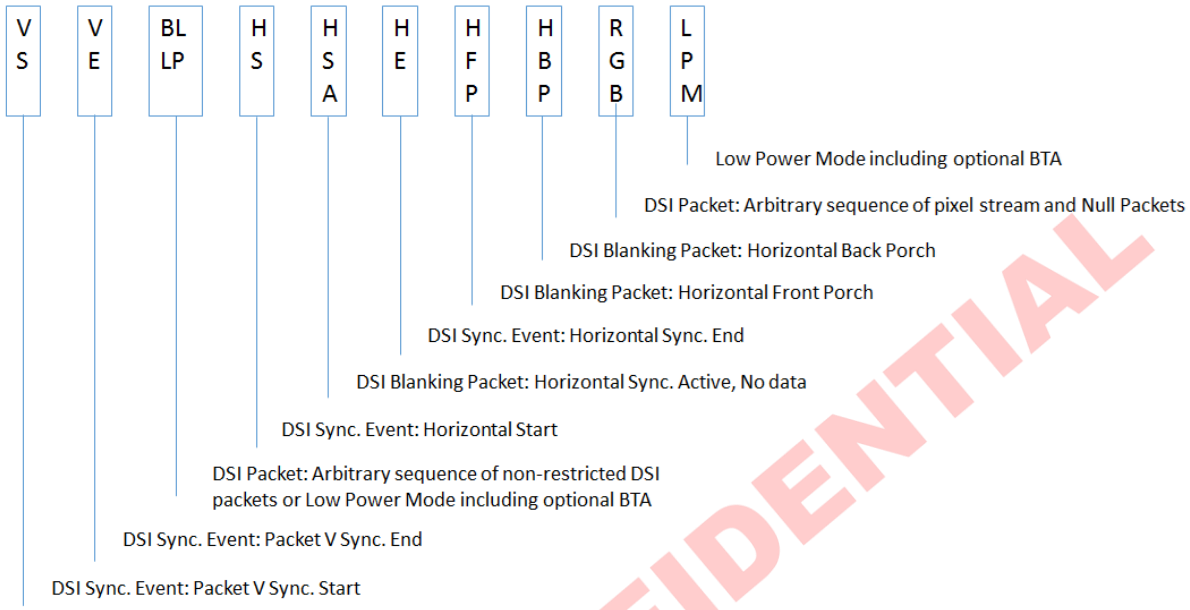
Normally, RGB pixel data is sent with one full scan line of pixels in a single packet. If necessary, a horizontal scan-line of active pixels may be divided into two or more packets. However, individual pixels shall not be split across packets.

Transmission packet components used in the figures in this section are defined in Figure below unless otherwise specified.



DSI Video Mode Interface Timing Legend

If a peripheral timing specification for HBP or HFP minimum period is zero, the corresponding Blanking Packet may be omitted. If the HBP or HFP maximum period is zero, the corresponding blanking packet shall be omitted.

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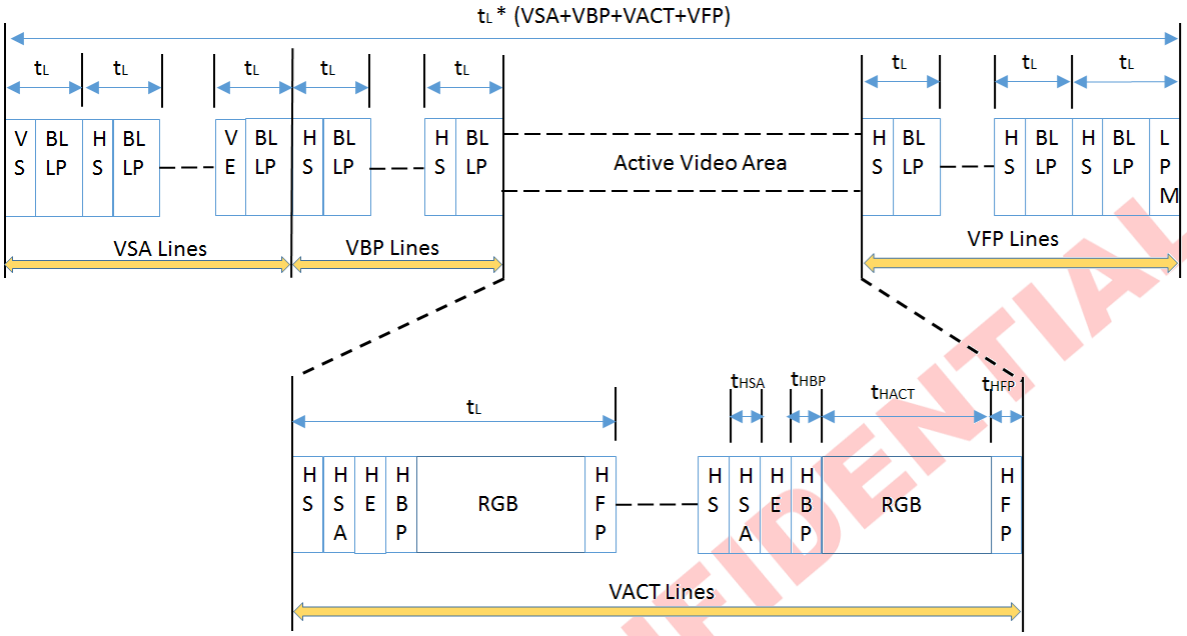
5.6.6.2 Non-Burst Mode with Sync Pulses

With this format, the goal is to accurately convey DPI-type timing over the DSI serial Link. This includes matching DPI pixel-transmission rates, and widths of timing events like sync pulses. Accordingly, synchronization periods are defined using packets transmitting both start and end of sync pulses. An example of this mode is shown in figure below.



DSI Video Mode Interface Timing: Non-Burst Transmission with Sync Start and End

Normally, periods shown as HSA (Horizontal Sync Active), HBP (Horizontal Back Porch) and HFP (Horizontal Front Porch) are filled by Blanking Packets, with lengths (including packet overhead) calculated to match the period specified by the peripheral's data sheet.

Alternatively, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

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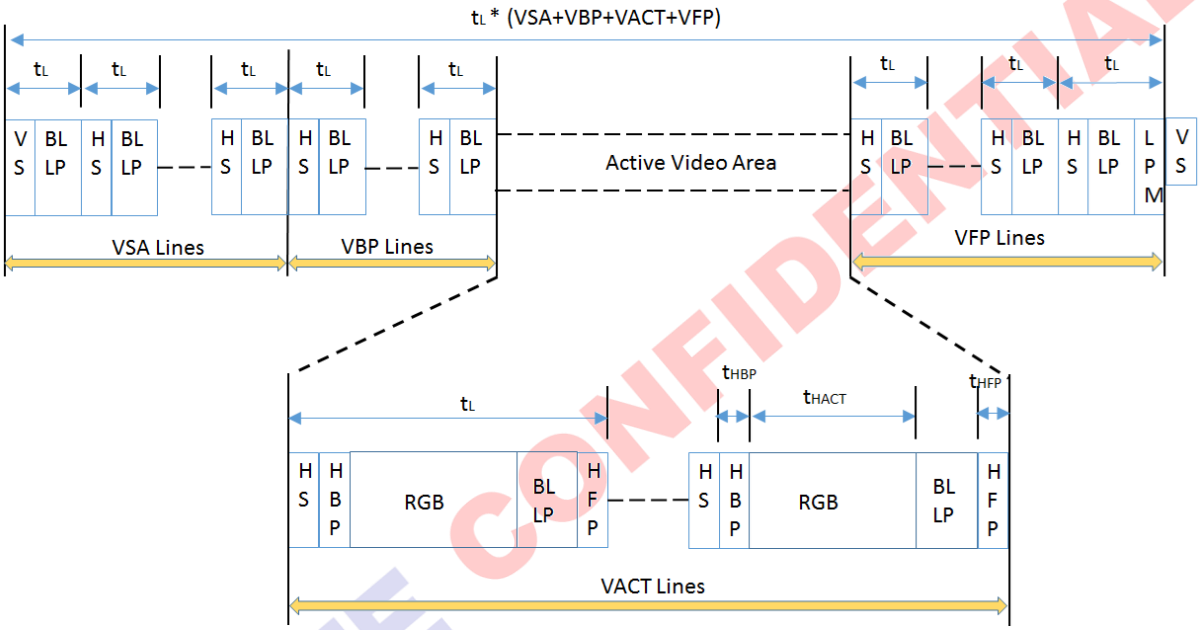
5.6.6.3 Burst Mode

In this mode, blocks of pixel data can be transferred in a shorter time using a time-compressed burst format. This is a good strategy to reduce overall DSI power consumption, as well as enabling larger blocks of time for other data transmissions over the Link in either direction. There may be a line buffer or similar memory on the peripheral to accommodate incoming data at high speed. Following HS pixel data transmission, the bus goes to Low Power Mode, during which it may remain idle, i.e. the host processor remains in LP-11 state, or LP transmission may take place in either direction. If the peripheral takes control of the bus for sending data to the host processor, its transmission time shall be limited to ensure data underflow does not occur from its internal buffer memory to the display device. An example of this mode is shown in figure below.



DSI Video Mode Interface Timing: Burst Transmission

Similar to the Non-Burst Mode scenario, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

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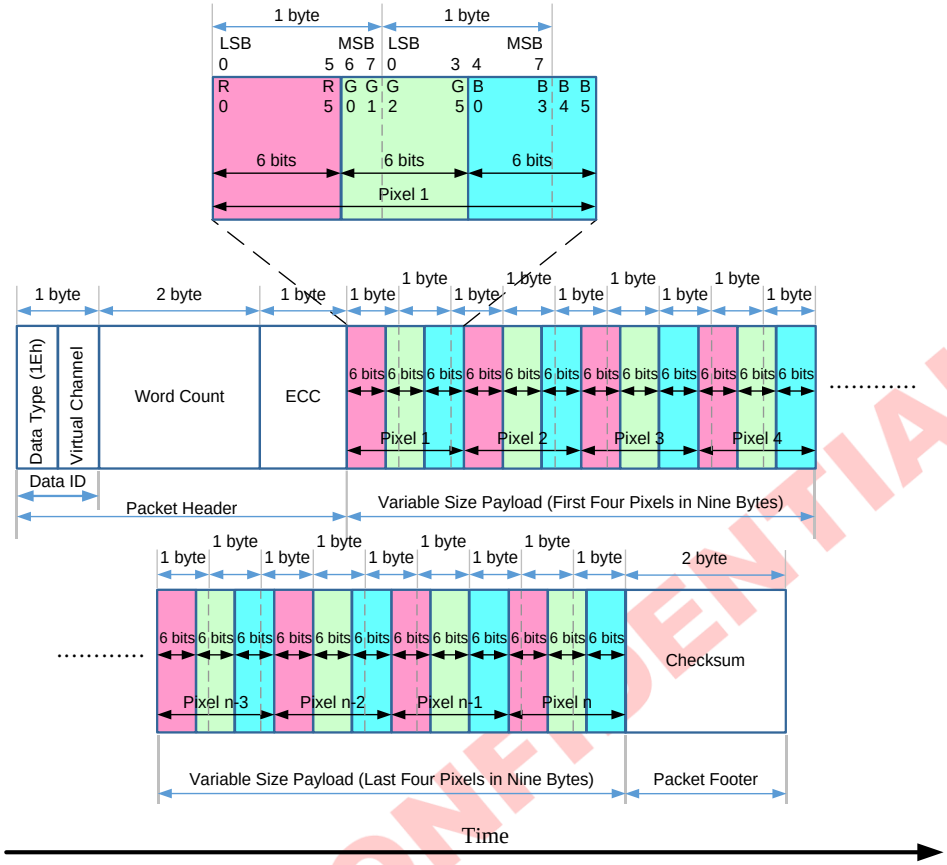
5.6.7 Display Data Format

5.6.7.1 18-bit per Pixel, Long Packet, Data Type 011110 (1Eh)



18-bit per Pixel – RGB Color Format, Long Packet

Packed Pixel Stream 18-Bit Format (Packed) is a Long packet. It is used to transmit RGB image data formatted as pixels to a Video Mode display module that displays 18-bit pixels The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. Pixel format is red (6 bits), green (6 bits) and blue (6 bits), in that order. Within a color component, the LSB is sent first, the MSB last. Note that pixel boundaries only align with byte boundaries every four pixels (nine bytes). Preferably, display modules employing this format have a horizontal extent (width in pixels) evenly divisible by four, so no partial bytes remain at the end of the display line data. If the active (displayed) horizontal width is not a multiple of four pixels, the transmitter shall send additional fill pixels at the end of the display line to make the transmitted width a multiple of four pixels. The receiving peripheral shall not display the fill pixels when refreshing the display device.

For example, if a display device has an active display width of 399 pixels, the transmitter should send 400 pixels in one or more packets. The receiver should display the first 399 pixels and discard the last pixel of the transmission.
With this format, the total line width (displayed plus non-displayed pixels) should be a multiple of four pixels (nine bytes).

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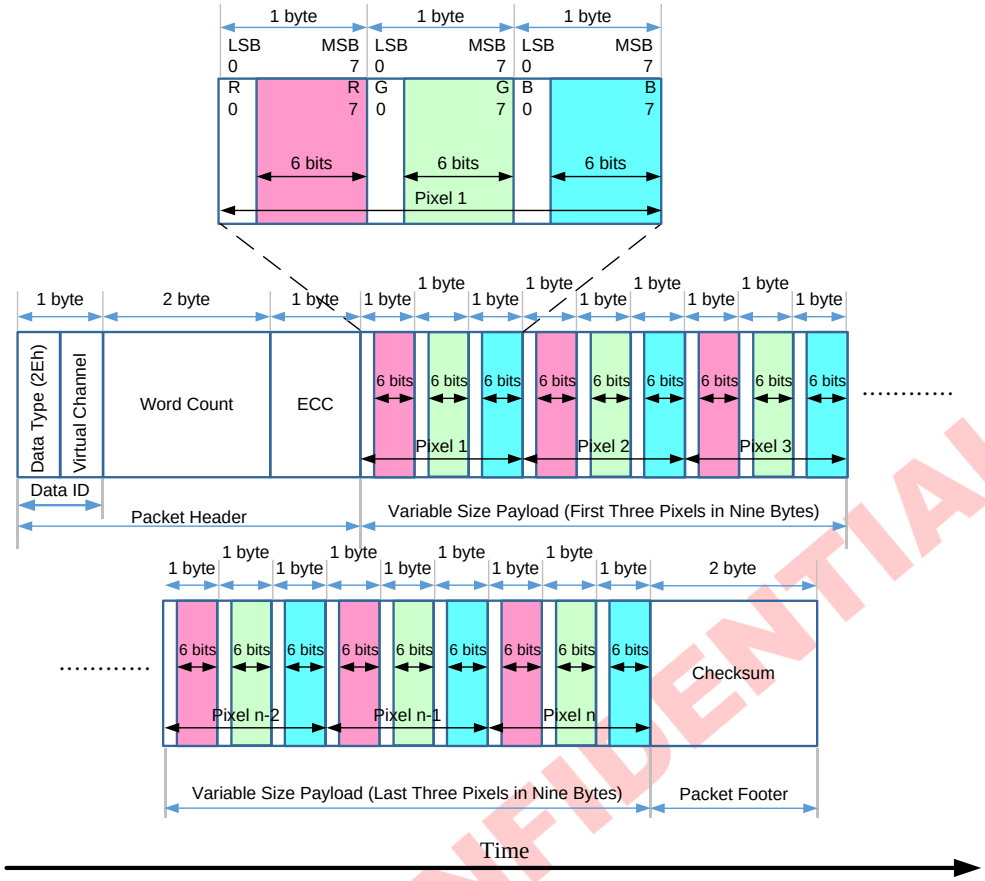
5.6.7.2 18-bit per Pixel, Long Packet, Data Type 101110 (2Eh)



18-bit per Pixel (Loosely Packed) – RGB Color Format, Long Packet

In the 18-bit Pixel Loosely Packed format, each R, G, or B color component is six bits but is shifted to the upper bits of the byte, such that the valid pixel bits occupy bits [7:2] of each byte. Bits [1:0] of each payload byte representing active pixels are ignored. As a result, each pixel requires three bytes as it is transmitted across the Link. This requires more bandwidth than the "packed" format, but requires less shifting and multiplexing logic in the packing and unpacking functions on each end of the Link.

This format is used to transmit RGB image data formatted as pixels to a Video Mode display module that displays 18-bit pixels. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. The pixel format is red (6 bits), green (6 bits) and blue (6 bits) in that order. Within a color component, the LSB is sent first, the MSB last. With this format, pixel boundaries align with byte boundaries every three bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of three bytes.

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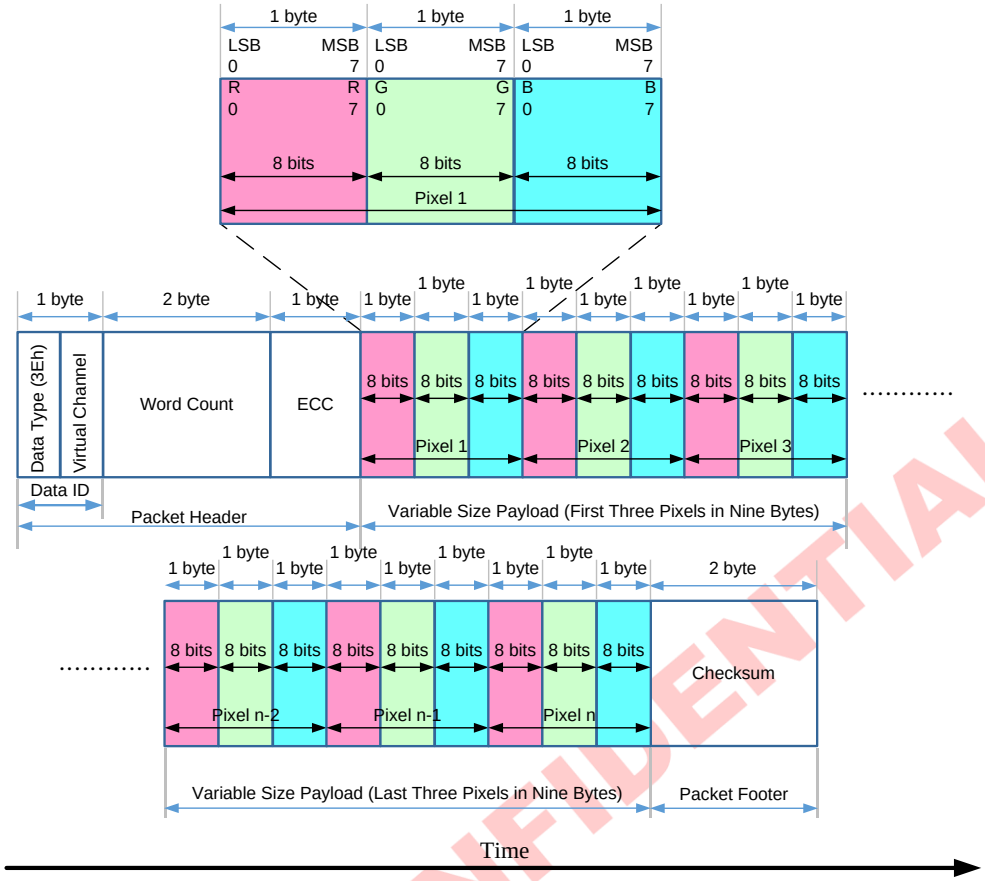
5.6.7.3 24-bit per Pixel, Long Packet, Data Type 111110 (3Eh)



24-bit per Pixel – RGB Color Format, Long Packet

Packed Pixel Stream 24-Bit Format is a Long packet. It is used to transmit image data formatted as 24-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. The pixel format is red (8 bits), green (8 bits) and blue (8 bits), in that order. Each color component occupies one byte in the pixel stream; no components are split across byte boundaries. Within a color component, the LSB is sent first, the MSB last. With this format, pixel boundaries align with byte boundaries every three bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of three bytes.

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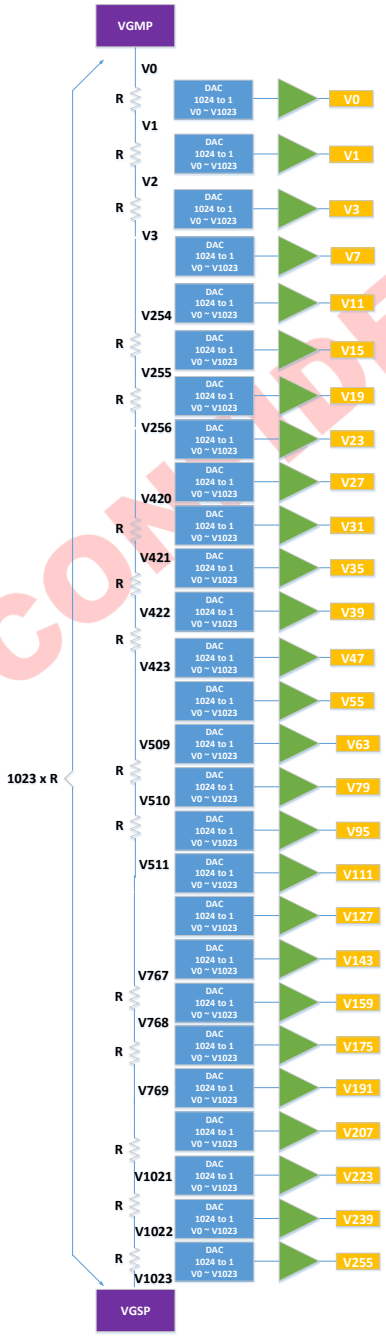
5.7 Gamma Function

The structure of grayscale amplifier is shown as below. ICNA3312 have support Separated Gamma Correction function for R/G/B data.

There are 27 voltage levels between VGMP/VGSP and Gamma GND (VGS), which are determined by the reference adjustment register.

ICNA3312 Gamma Structure as below:



Gamma register stream and Gamma reference voltage

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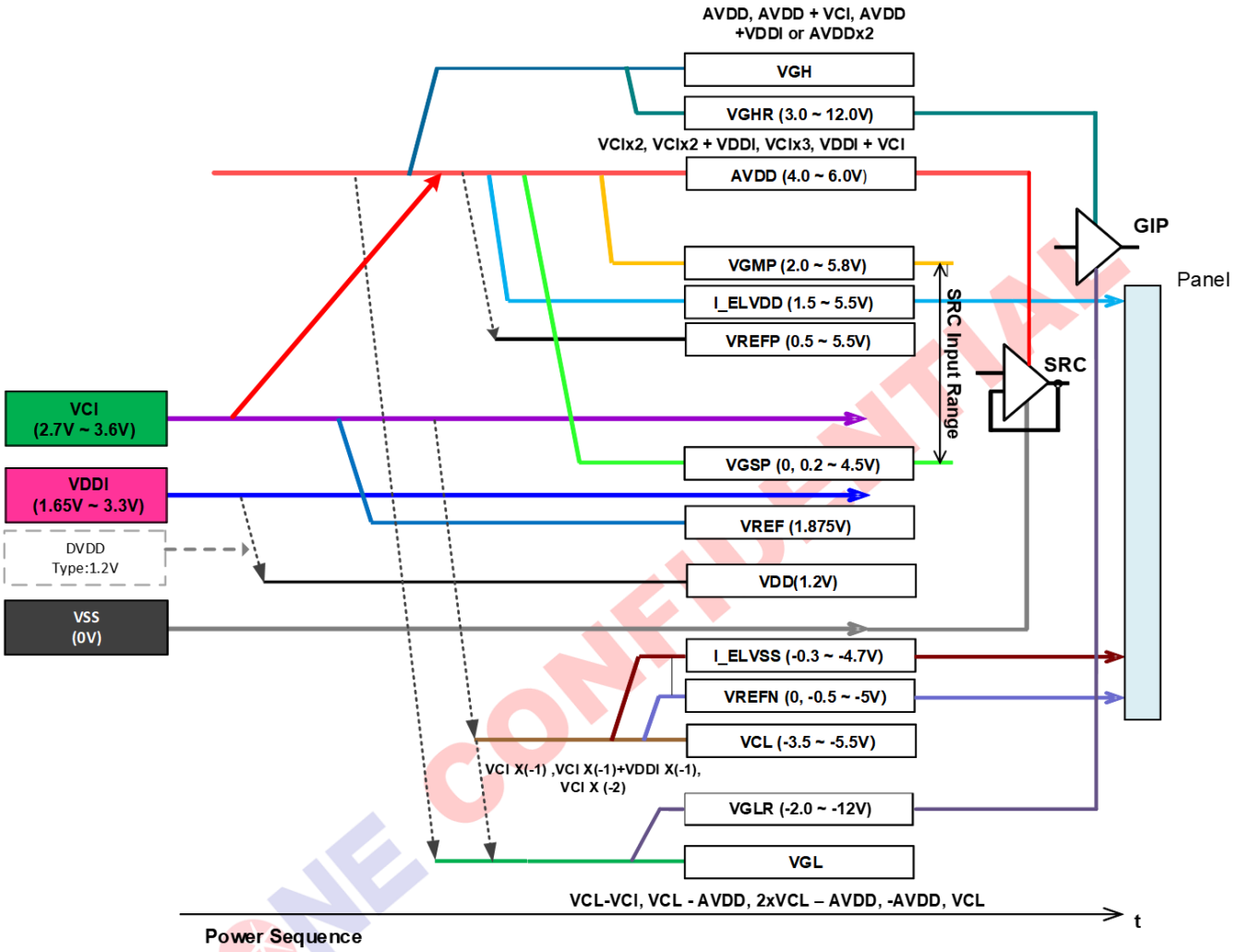
5.8 Power On/ OFF Sequence

5.8.1 Power Stage Diagram



Power Stage Diagram

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5.8.2 Power ON Sequence

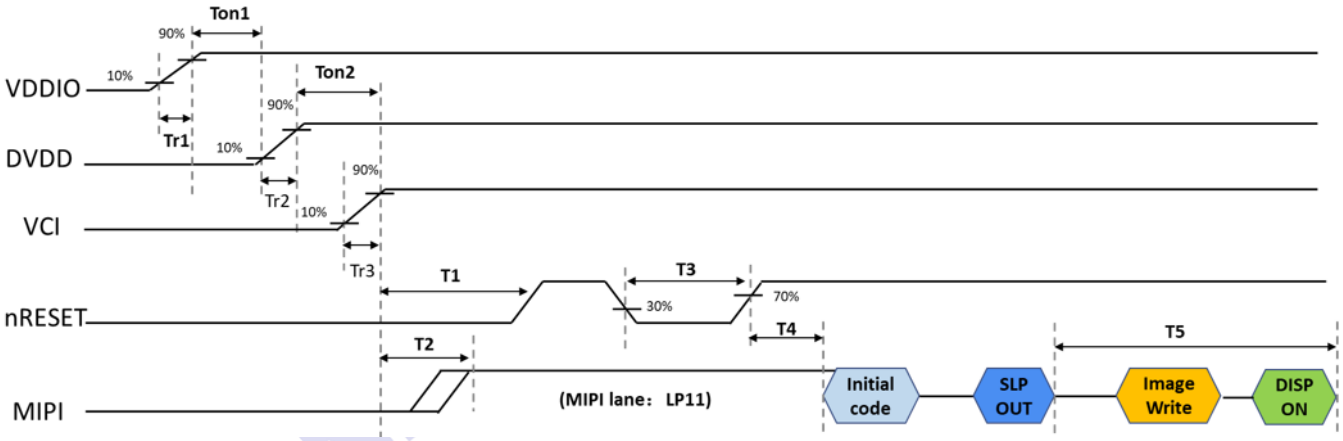
The power on sequence for different power input modes are shown below figures.

Power ON Sequence Timing

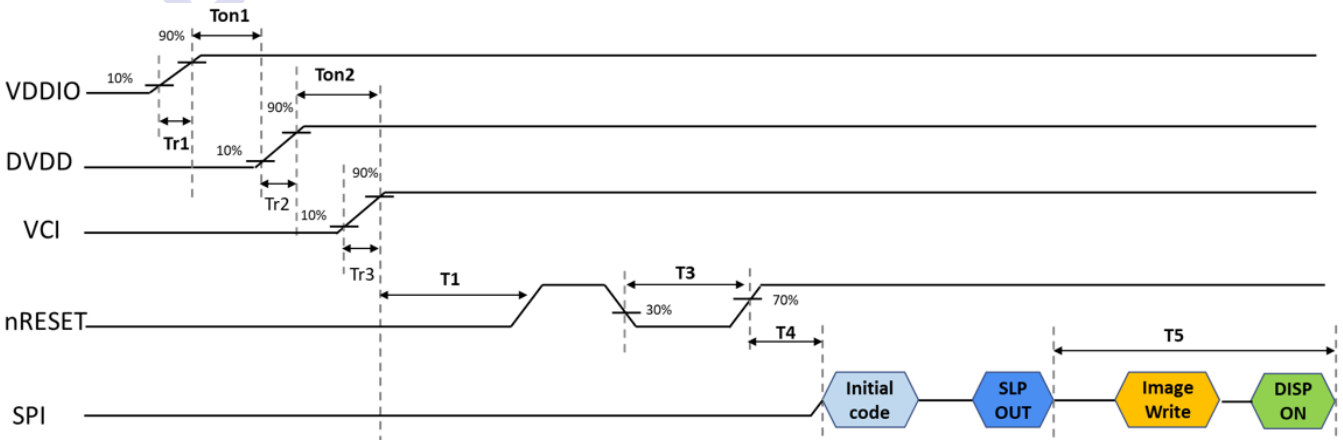
Symbol	Description	Value			Unit	Remark
		Min.	Typ.	Max.		
Ton1	VDDI on to DVDD on delay	>0	-	-	us	
Ton2	DVDD on to VCI on power delay time	>0	-	-	ms	
T1	VCI on to valid to nRESET high	10	-	-	ms	
T2	VCI to MIPI bus ready delay	0	-	T1	ms	
T3	nRESET low period	50	-	-	us	
T4	nRESET high to OTP code re-load ready	10	-	-	ms	
T5	Sleep-out command received to Display on command received.	50	-	-	ms	
Tr1	VDDI power rising time	0.3	-	2	ms	
Tr2	DVDD power rising time	0.3	-	2	ms	
Tr3	VCI power rising time	0.3	-	2	ms	

The Power on sequence is shown as below.

MIPI CASE:



SPI CASE:



Note 1: *Unless otherwise specified, timings herein show cross point at 50% of signal/power level.*

Note 2: *This power-on sequence is based on adding Schottky diode on VGL pin to ground.*

5.8.3 Power OFF Sequence

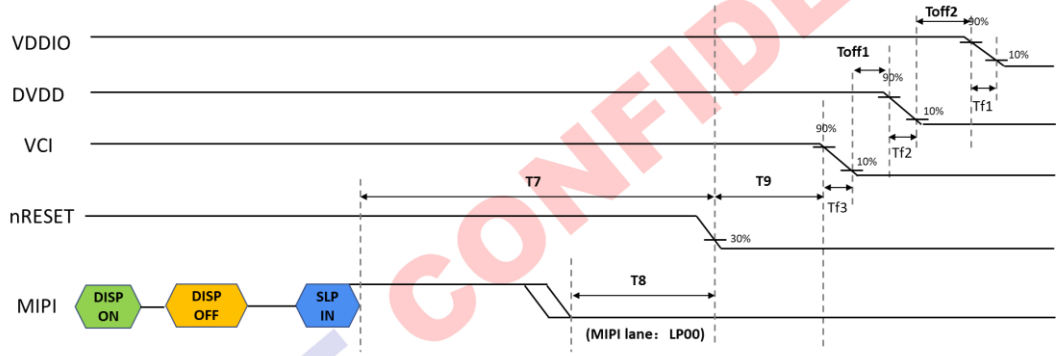
The power off sequence for different power input modes are shown below figures.

Power OFF Sequence Timing

Symbol	Description	Value			Unit	Remark
		Min.	Typ.	Max.		
Toff1	VCI off to DVDD off delay	>0	-	-	us	
Toff2	DVDD off to VDDI off delay	>0	-	-	us	
T7	Sleep-in command received to valid to nRESET low	100	-	-	ms	
T8	MIPI ultra low power mode to valid to nRESET low	0	-	-	us	
T9	nRESET low to VCI off delay	0	-	-	us	
Tf1	VDDI power falling time	0.1	-	5	ms	
Tf2	DVDD power falling time	0.1	-	5	ms	
Tf3	VCI power falling time	0.1	-	5	ms	

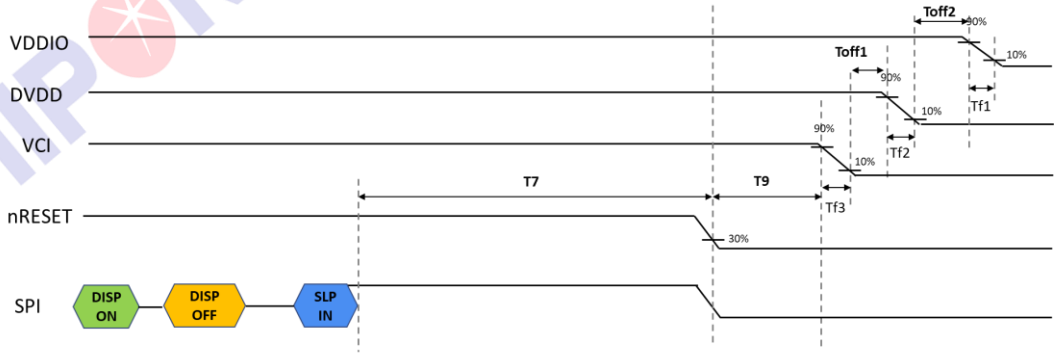
The power off sequence is shown as below:

MIPI CASE:



MIPI Power OFF Sequence

SPI CASE:



SPI Power OFF Sequence

Note 1: *Unless otherwise specified, timings herein show cross point at 50% of signal/power level.*

Note 2: *Keep VGH is equal to or larger than VCI during power off sequence.*

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6. Electrical Characteristics

6.1 Absolute Maximum Ratings

The absolute maximum rating is listed in below table. It may lead permanently damaged when the ICNA3312 is used out of the absolute maximum rating.

To use the ICNA3312 within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the ICNA3312 will malfunction and be poor reliability.

Absolute Maximum Ratings List

Item	Symbol	Rating			Unit
		Min.	Typ.	Max.	
Power supply voltage	VDDI ~ VSSD	-0.3	-	+5.5	V
Power supply voltage	VCI (VCIA, VCIC, VCIR) ~ VSSA	-0.3	-	+5.5	V
Supply voltage	AVDD ~ VSSA	-0.3	-	+6.6	V
Supply voltage	AVSS ~ VCL	-0.3	-	+5.0	V
Supply voltage	VGH ~ VGL	|VGH-VGL| ≦30			V
Operating temperature	Topr	-40		+85	℃
Storage temperature	Tstg	-55		+125	℃
Input voltage	Vin	-0.3		VDDI+0.3	V

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6.2 DC Characteristics

Condition : Ta =25°C

DC Characteristics List

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit	Notes
Power generation & Operation Voltage							
AVDD booster voltage	AVDD	Operating Voltage	4.0	-	6.0	V	
VCL booster voltage	VCL	Operating Voltage	-5.5	-	-3.5	V	
Analog Operating voltage	VREFP	Operating Voltage	0.5	-	5.5	V	
Analog Operating voltage	VREFN	Operating Voltage	-5.0	-	-0.5	V	
Analog Operating voltage	I_ELVDD	Operating Voltage	1.5	-	5.5	V	
Analog Operating voltage	I_ELVSS	Operating Voltage	-4.7	-	-0.3	V	
Gamma reference voltage	VGMP	Operating Voltage	2	-	5.8	V	
Gamma reference voltage	VGSP	Operating Voltage	0.2	-	4.5	V	
VGH booster voltage	VGH	Operating Voltage	3		12.0	V	
VGL booster voltage	VGL	Operating Voltage	-12		-2	V	
Voltage difference between VGH and VGL	VGH-VGL	|VGH-VGL| ≦30			30	V	
I/O operating voltage	VDDI	I/O supply voltage	1.65	-	3.3	V	
LOGIC INPUT/ OUTPUT							
Logic High level input voltage	V_{IH}		0.8× VDDI	-	VDDI	V	1
Logic Low level input voltage	V_{IL}	-	VSS	-	0.2× VDDI	V	1
Logic High level output voltage	V_{OH}	I_{OH} = -0.1mA	0.8× VDDI	-	VDDI	V	2
Logic Low level output voltage	V_{OL}	IOL = +0.1mA	VSS	-	0.2× VDDI	V	2
Logic High level leakage	I_{LIH1}	Vin = 0 to *VDDI*	-	-	1	μA	1,2
Logic Low level leakage	I_{LIL1}	Vin = 0 to *VDDI*	-1	-	-	μA	1,2
Source OP Output							
Output deviation voltage	V_{dev}	Sout≧4.2V Sout≦0.8V			TBD	mV	
Output deviation voltage	V_{dev}	4.2V>Sout>0.8V			TBD	mV	
Output offset voltage	V_{OFSET}				TBD	mv	
Stand-by Current							
Sleep In mode	I_{stlp1}	DSI LP mode VDDI Current		110		μA	
		DSI LP mode VCI Current		25		μA	1
	I_{stul1}	DSI Ultra Low power VDDI Current		85		μA	
		DSI Ultra Low power VCI Current		25		μA	1
Oscillator Output							
Oscillator tolerance	△OSC	All Temperature	-2%	-	2%	%	3

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Note 1: *Including of all logic I/O pins.*
Note 2: *Including of TE, TE1, SWIRE.*
Note 3: *Oscillator = 24MHz.*

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6.3 MIPI DC Characteristics

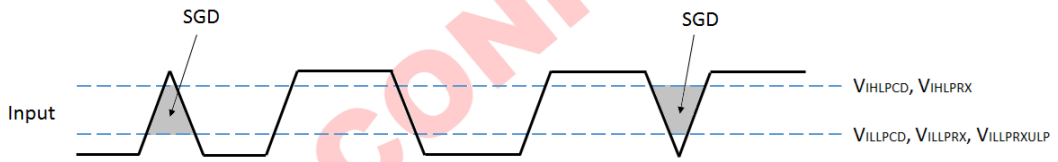
6.3.1 DC Characteristics for DSI LP Mode

Condition : Ta =25℃,VDDI =1.65V~3.3V, VCI =2.7V~3.6V,

DC Characteristics List for DSI LP Mode

Parameter	Symbol	Conditions	Specification			Unit	Notes
			MIN	TYP	MAX		
Logic high level input voltage	V_{IHLPCD}	LP-CD	450		1350	mV	
Logic Low level input voltage	V_{ILLPCD}	LP-CD	0		200	mV	
Logic high level input voltage	V_{IHLPRX}	LP-RX (CLK,D0)	880		1350	mV	
Logic Low level input voltage	V_{ILLPRX}	LP-RX (CLK,D0)	0		550	mV	
Logic Low level input voltage	$V_{ILLPRXULP}$	LP-RX(CLK ULP mode)	0		300	mV	
Logic high level input voltage	V_{OHLPTX}	LP-TX(D0)	1.1		1.3	V	
Logic Low level input voltage	V_{OLLPTX}	LP-TX(D0)	-50		50	mV	
Logic high level input voltage	I_{IH}	LP-RX,Vin =0~1.3V			10	µA	
Logic Low level input voltage	I_{IL}	LP-RX,Vin =0~1.3V	-10			µA	
Input pulse rejection	SGD	DSI-CLKP/N,DSI-DnP/N			300	Vps	1

Note 1: Peak interference amplitude max. 200mV and interference frequency min. 450MHz.



Spike/Glitch Rejection

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6.3.2 DC Characteristics for DSI HS Mode

Condition : Ta =25℃,VDDI =1.65V~3.3V, VCI =2.7V~3.6V.

DC Characteristics List for DSI HS Mode

Parameter	Symbol	Conditions	Specification			Unit	Notes
			MIN	TYP	MAX		
Input voltage common mode range	V_{CMCLK} V_{CMDATA}	CLKP/N, DnP/N	70		330	mV	1,2
Input voltage common mode variation (≦450MHz)	$V_{CMRCLKL}$ $V_{CMRDATAL}$	CLKP/N, DnP/N	-50		50	mV	3
Input voltage common mode variation (≧450MHz)	$V_{CMRCLKM}$ $V_{CMRDATAM}$	CLKP/N, DnP/N			100	mV	
Low-level differential input voltage threshold	V_{THLCLK} $V_{THLDATA}$	CLKP/N, DnP/N	-70			mV	
High-level differential input voltage threshold	V_{THHCLK} $V_{THHDATA}$	CLKP/N, DnP/N			70	mV	
Single-ended input low voltage	V_{ILHS}	CLKP/N, DnP/N	-40			mV	2
Single-ended input high voltage	V_{IHHS}	CLKP/N, DnP/N			460	mV	2
Differential input termination resistor	R_{TERM}	CLKP/N, DnP/N	80	100	125	Ω	
Single-ended threshold voltage for termination enable	V_{TERM_EN}	CLKP/N, DnP/N			450	mV	
Termination capacitor	C_{TERM}	CLKP/N, DnP/N			14	pF	

Note 1: Includes 50mV (-50mV to 50mV) ground difference.

Note 2: Without VCMRCLKM / VCMRDATAM .

Note3: Without 50mV (-50mV to 50mV) ground difference.

Note4: Dn =D0,and D1.

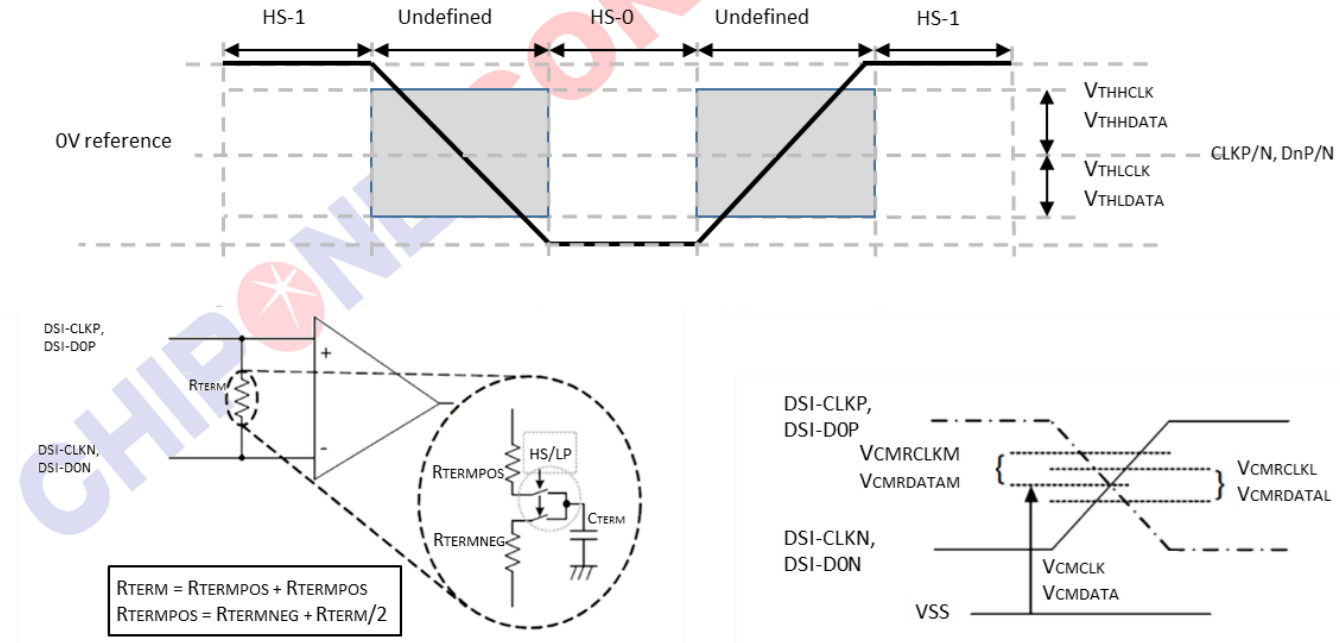

Figure 6-1 Differential voltage range, termination resistor and Common mode voltage

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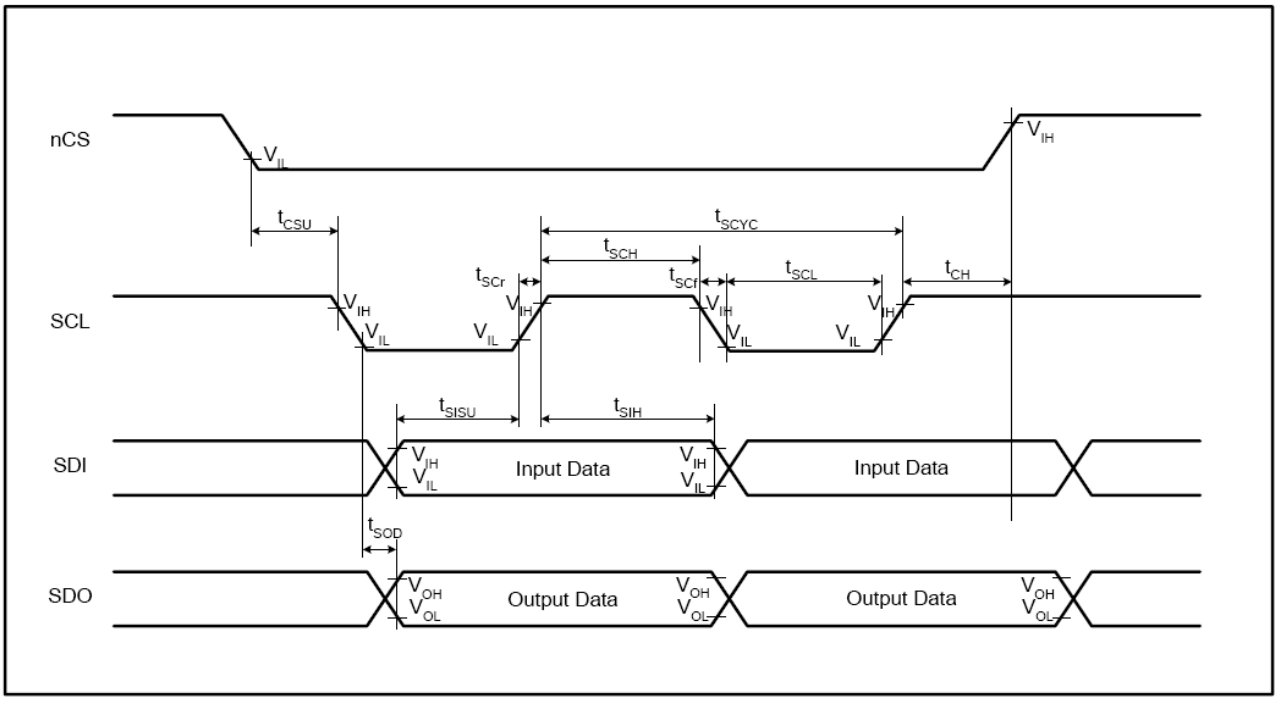
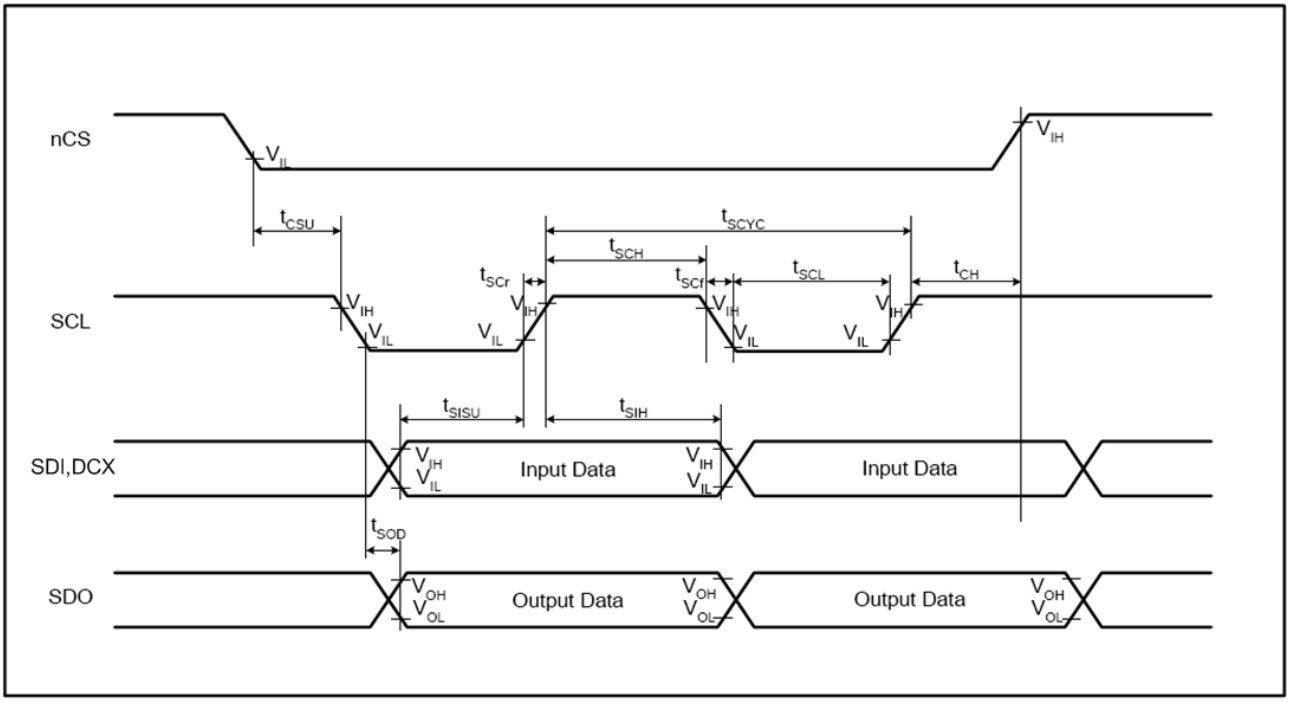
6.4 AC Timings Characteristics

6.4.1 Serial Interface Characteristics (3/4-wire SPI)

3-Wire SPI Serial Interface Characteristics



4-Wire SPI Serial Interface Characteristics



Parameter	Symbol	Conditions	Specification			Unit	Notes
			MIN	TYP	MAX		
SCL	T_{SCYC}	Clock cycle (Write)	20	-	-	ns	
	T_{SCYC}	Clock cycle (Read)	300		-	ns	
	T_{SCH}	Clock “H” pulse width (Write)	9	-	-	ns	
	T_{SCH}	Clock “H” pulse width (Read)	140	-	-	ns	
	T_{SCL}	Clock “L” pulse width (Write)	9	-	-	ns	
	T_{SCL}	Clock “L” pulse width (Read)	140	-	-	ns	
	T_{SCr}	Clock rise time	-	-	2	ns	
	T_{SCf}	Clock fall time	-	-	2	ns	
CSX	T_{CSU}	Chip select setup time	10	-	-	ns	
	T_{CH}	Chip select hold time	10	-	-	ns	
SDI	T_{SISU}	Data input setup time	5	-	-	ns	
	T_{SIH}	Data input hold time	5	-	-	ns	
SDO	T_{SOD}	Data output setup time	-	-	120	ns	
	T_{SOH}	Data output hold time	5	-	-	ns	

***Note 1**: Logic high and low levels are specified as 20% and 80% of VDDI for Input signals.*

***Note 2**: Ta = -30 to 85 °C, VDDI=1.65V to 3.3V, VCI=2.7V to 3.6V, GND=0V*

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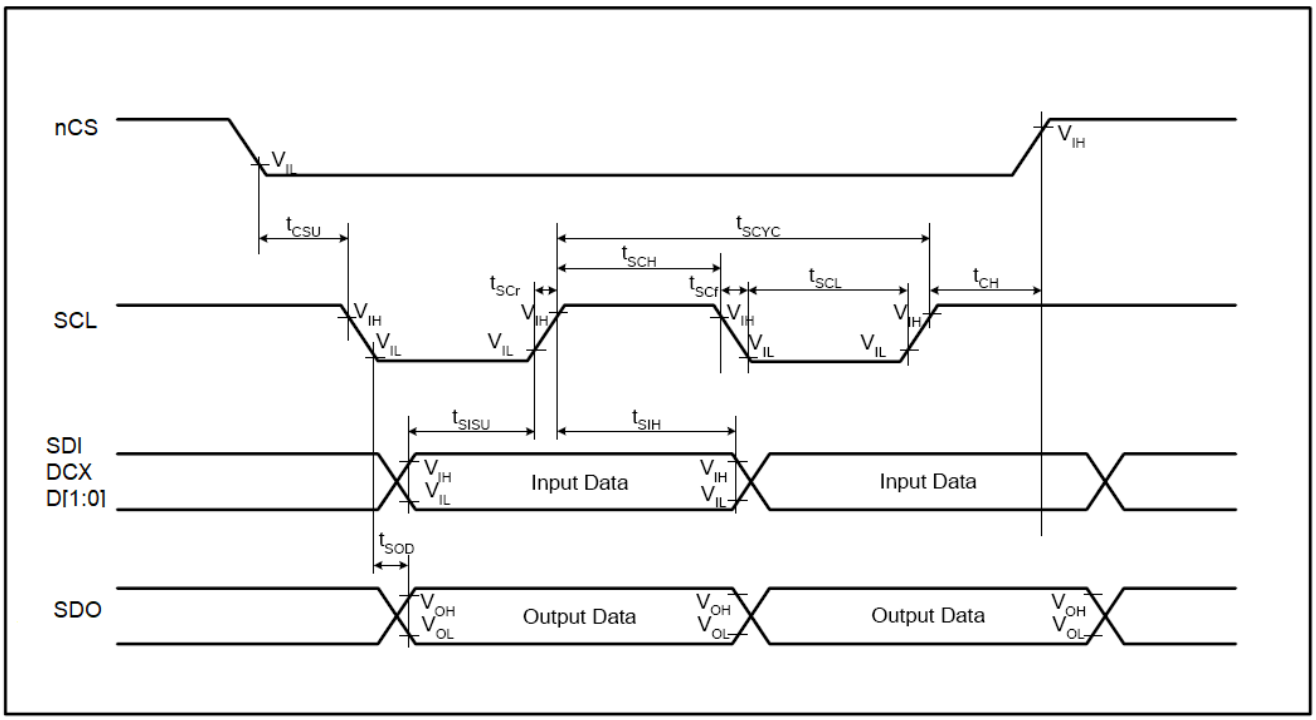
6.4.2 Serial Interface Characteristics (QUAD SPI)



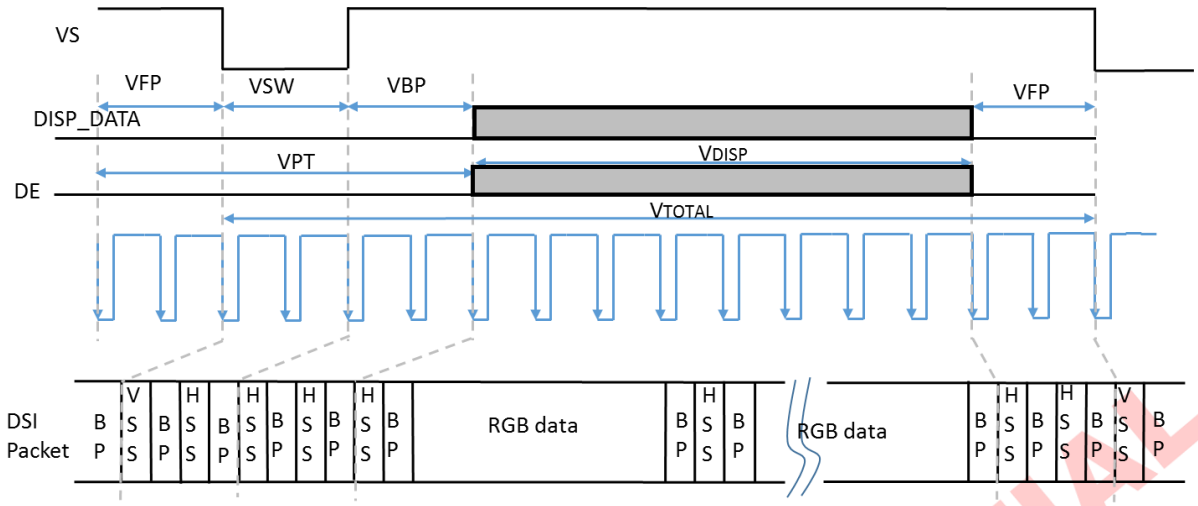
Parameter	Symbol	Conditions	Specification			Unit	Notes
			MIN	TYP	MAX		
SCL	T_{SCYC}	Clock cycle (Write)	20	-	-	ns	
	T_{SCYC}	Clock cycle (Read)	100		-	ns	
	T_{SCH}	Clock "H" pulse width (Write)	6.5	-	-	ns	
	T_{SCH}	Clock "H" pulse width (Read)	45	-	-	ns	
	T_{SCL}	Clock "L" pulse width (Write)	6.5	-	-	ns	
	T_{SCL}	Clock "L" pulse width (Read)	45	-	-	ns	
	T_{SCr}	Clock rise time	-	-	3.5	ns	
	T_{SCf}	Clock fall time	-	-	3.5	ns	
CSX	T_{CSU}	Chip select setup time	10	-	-	ns	
	T_{CH}	Chip select hold time	10	-	-	ns	
SDI DCX D[1:0]	T_{SISU}	Data input setup time	4	-	-	ns	
	T_{SIH}	Data input hold time	4	-	-	ns	
SDO	T_{SOD}	Data output setup time	-	-	45	ns	
	T_{SOH}	Data output hold time	5	-	-	ns	

***Note 1**: Logic high and low levels are specified as 20% and 80% of VDDI for Input signals.*

***Note 2**: Ta = -30 to 85 °C, VDDI=1.65V to 3.3V, VCI=2.7V to 3.6V, GND=0V*

***Note 3**: The max SCL sequence of 4-wire QSPI transferring RGB888, RGB666 and RGB555 is 50Mhz.*

6.4.3 Vertical Timings for DSI video mode



Vertical timings for DSI interface

Condition : Ta =25°C,Resolution = 454(RGB)* 454

Vertical Timings List for DSI video mode

Parameter	Symbol	Conditions	Specification			Unit	Notes
			MIN	TYP	MAX		
Vertical Total	VTOTAL			TBD		Line	
Vertical low pulse width	VSW			TBD		Line	1
Vertical front porch	VFP			TBD		Line	
Vertical back porch	VBP			TBD		Line	1
Vertical data start point		VSW+VBP		TBD		Line	1
Vertical blanking period	VPT	VSW+VBP+VFP		TBD		Line	
Vertical active area	VDISP			454		Line	
Vertical Frame rate	VFR			60		Hz	

Note 1: *The VSW and VBP pulse width are related to GOA timing. The GOA timing must be set at corresponding position for normal display.*

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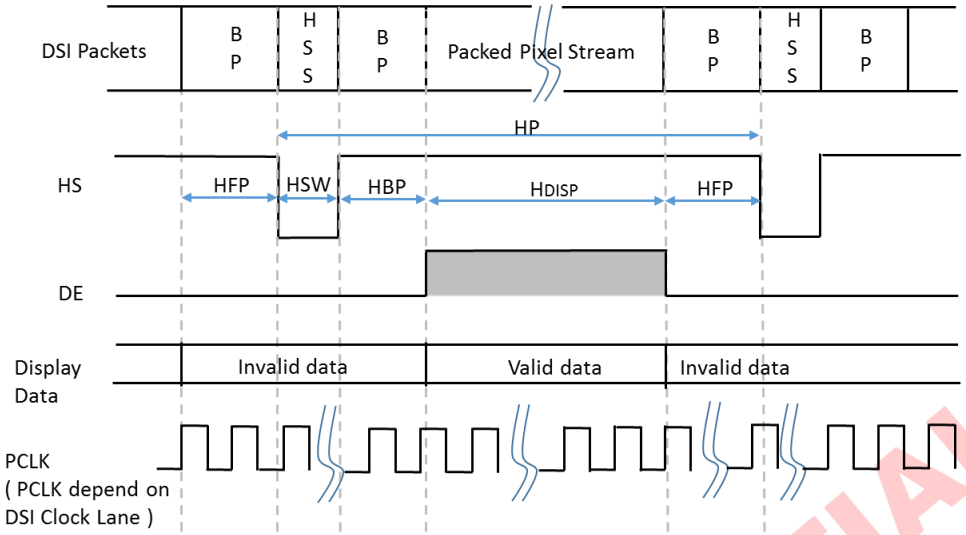
6.4.4 Horizontal Timings for DSI video mode



Horizontal timings for DSI video mode

Condition : Ta =25°C,Resolution = 454(RGB)* 454

Horizontal Timings List for DSI video mode

Parameter	Symbol	Conditions	Specification			Unit	Notes
			MIN	TYP	MAX		
HS low pulse width	HSW			TBD		nS	
Horizontal back porch	HBP			TBD		nS	
Horizontal front porch	HFP			TBD		nS	
Horizontal data start point		HSW+HBP		TBD		nS	
Horizontal blanking period	HBLK	HSW+HBP+HFP		TBD		nS	
Horizontal active area	HDISP			454		DCLK	

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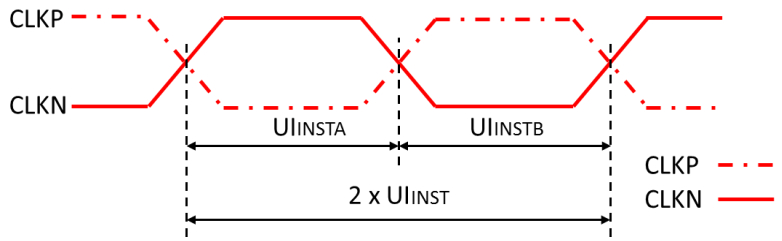
6.5 MIPI AC Characteristics

6.5.1 High Speed Mode - Clock Timings



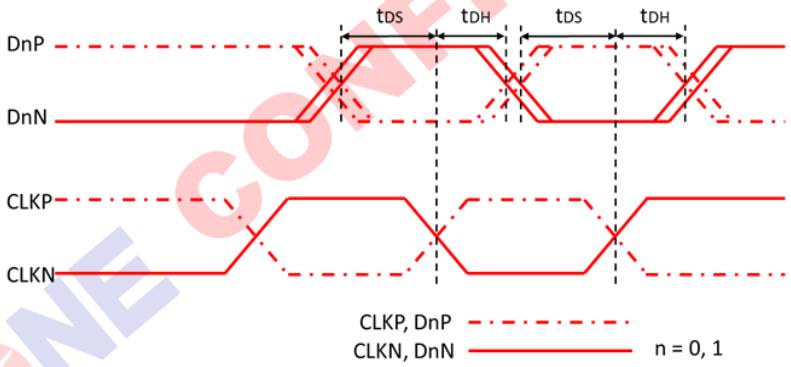
Clock Timing

High Speed Mode - Clock Timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
CLK P/N	2xUIINST	Double UI instantaneous	4		25	nS	
CLK P/N	UIINSTA, UIINSTB	UI instantaneous Half	2		12.5	nS	1

Note 1: *UI = UIINSTA = UIINSTB.*

6.5.2 High Speed Mode - Clock / Data Timings



DSI Clock / Data Timings

High Speed Mode - Clock / Data Timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
Dn P/N	tDS	Data to Clock Setup time	0.15*UI			UI	
(n=0, and1)	tDH	Clock to Data Hold time	0.15*UI			UI	

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6.5.3 High Speed Mode - Rising and Falling Timings

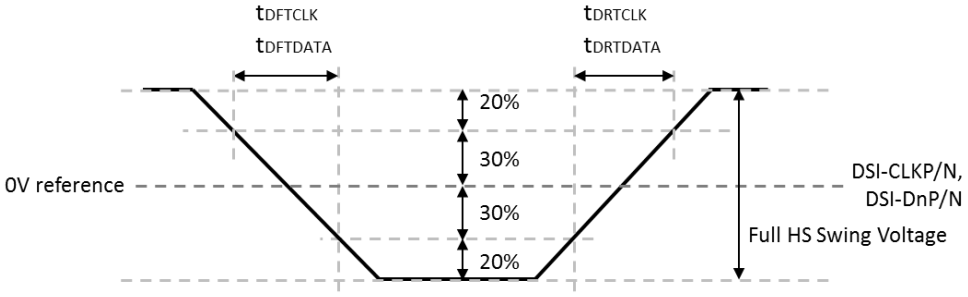

Figure 6-2 Rising and Falling Timings

High Speed Mode - Rising and Falling Timing

Parameter	Symbol	Conditions	Specification			Unit	Notes
			MIN	TYP	MAX		
Differential Rise Time for Clock	t_{DRTCLK}	CLKP/N	150pS		0.3*UI		2,3
Differential Rise Time for Data	$t_{DRTDATA}$	DnP/N	150pS		0.3*UI		1,2,3
Differential Fall Time for Clock	t_{DFTCLK}	CLKP/N	150pS		0.3*UI		2,3
Differential Fall Time for Data	$t_{DFTDATA}$	DnP/N	150pS		0.3*UI		1,2,3

Note 1: *DnP/N, n =0, and 1.*

Note 2: *The display module has to meet timing requirements, which are defined for the transmitter (MCU) on MIPI D-PHY standard.*

Note 3: *DSI-CLK+ = CLKP.*
DSI-CLK- =CLKN.
DSI-D0+ =D0P.
DSI-D0- =D0N.

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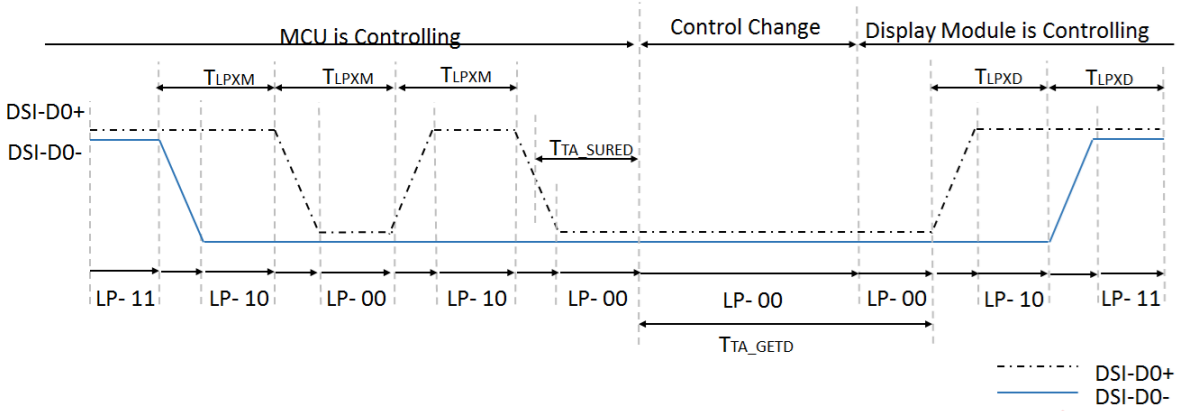
6.5.4 Low Speed Mode - Bus Turn Around



Bus Turnaround (BTA) from MCU to display module Timing

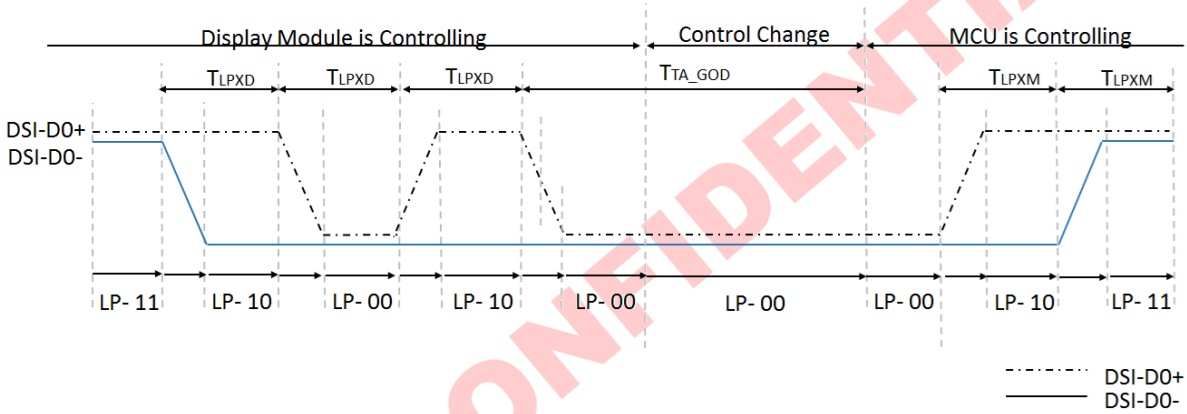


Figure 6-3 Bus Turnaround (BTA) from Display module to MCU Timing

Low Speed Mode - Bus Turn Around Timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
D0P/N	T_{LPXM}	Length of LP-00,LP-01,LP-10 or LP11 periods MCU to Display Module	50		75	nS	1
D0P/N	T_{LPXD}	Length of LP-00,LP-01,LP-10 or LP11 periods Display Module to MCU	50		75	nS	1
D0P/N	T_{TA_SURED}	Time-out before the Display Module starts driving	T_{LPXD}		2* T_{LPXD}	nS	1
D0P/N	T_{TA_GETD}	Time to drive LP-00 by Display Module	5* T_{LPXD}			nS	1
D0P/N	T_{TA_GOD}	Time to drive LP-00 after turnaround request -MCU	4 * T_{LPXD}			nS	1

Note 1: *D0P = DSI-D0+, D0N = DSI-D0-.*

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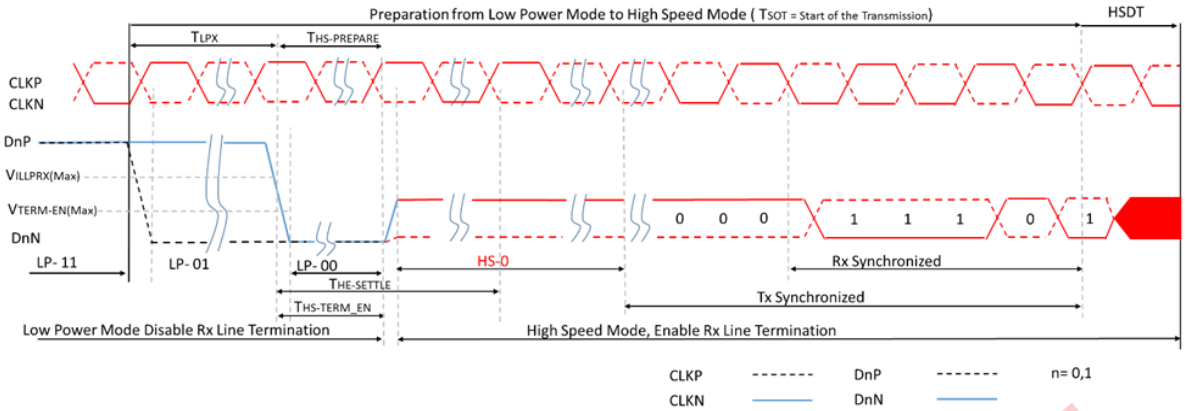
6.5.5 Data Lanes from Low Power Mode to High Speed Mode



Data Lanes from High Speed Mode to Low Power Mode Timing

Data Lanes from Low Power Mode to High Speed Mode Timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
DnP/N	T_{LPX}	Length of any Low Power State Period	50			nS	1
DnP/N	$T_{HS\text{-}PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	40+4*UI		85+6*UI	nS	1
DnP/N	$T_{HS\text{-}TREM\text{-}EN}$	Time to enable Data lane Receiver line termination measured from when Dn crosses VILMAX			35+4*UI	nS	1

Note 1: DnP/N, n=*0,and 1*

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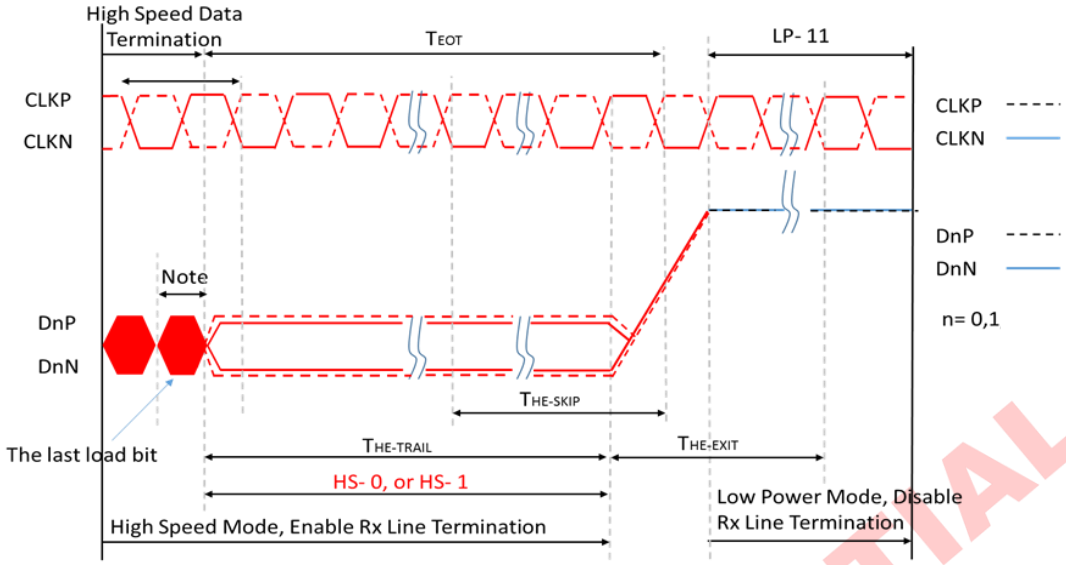
6.5.6 Data Lanes from High Speed Mode to Low Power Mode



Note:
If the last load bit is HS- 0, the transmitter changes from HS- 0 to HS- 1.
If the last load bit is HS- 1, the transmitter changes from HS- 1 to HS- 0

Data Lanes from High Speed Mode to Low Power Mode Timing

Data Lanes from High Speed Mode to Low Power Mode Timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
DnP/N	$T_{HS-SKIP}$	Time-Out at Display Module to ignore transition period of EoT	40		55+4*UI	nS	1
DnP/N	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100			nS	1

Note 1: DnP/N, n=*0, and 1.*

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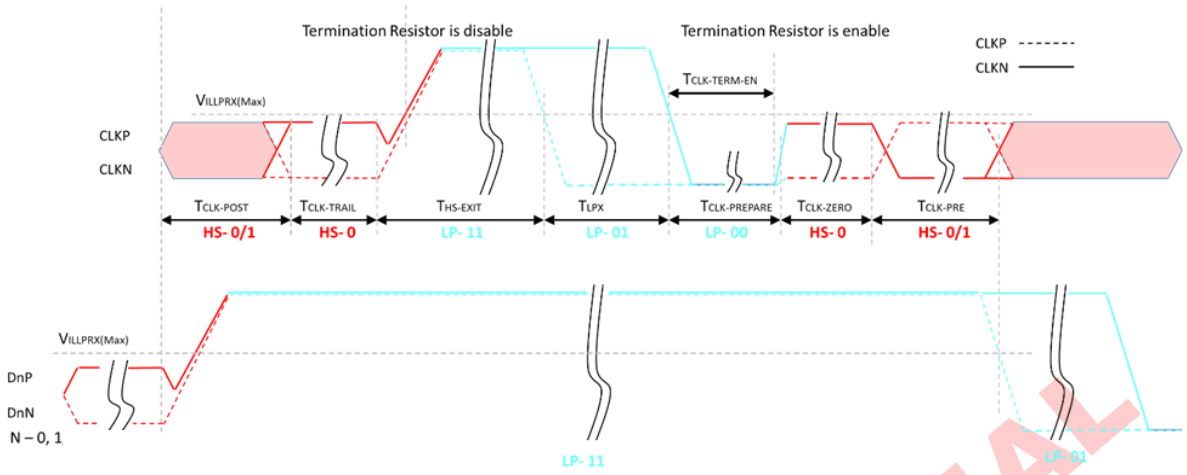
6.5.7 DSI Clock Burst – High speed mode to /from Low Power Mode



Clock Lane –High speed mode to / from Low Power Mode Timing

DSI Clock Burst – High speed mode to /from Low Power Mode Timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
CKP/N	$T_{CLK-POST}$	Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52*UI			nS	
CKP/N	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60			nS	
CKP/N	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100			nS	
CKP/N	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38		95	nS	
CKP/N	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination			38	nS	
CKP/N	$T_{CLK-PREPARE}$+ $T_{CLK-ZERO}$	Minimum lead HS-0 drive period before starting Clock	300			nS	
CKP/N	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8*UI			nS	

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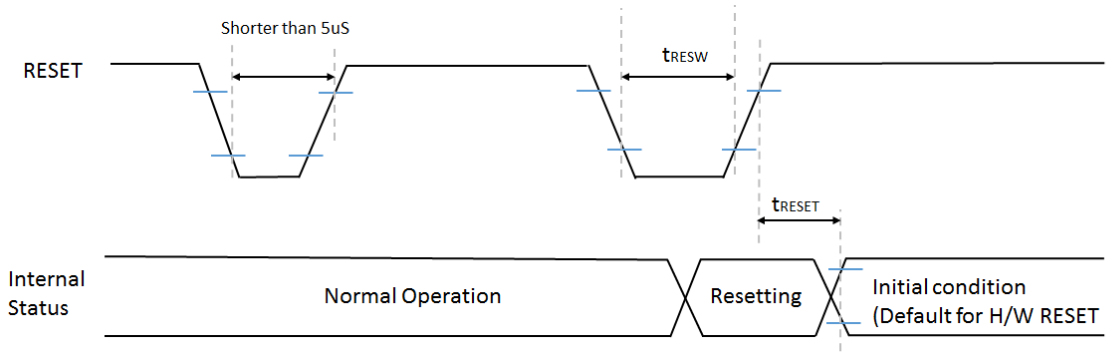
6.6 Reset Input Timing



Reset Input Timing

Condition : Ta =25℃

Reset Input Timing

Signal	Symbol	Parameter	Description	Specification			Unit	Notes
				MIN	TYP	MAX		
RESET	tRESW	Reset "L" pulse width		10			µS	1
	tRESET	Reset complete time	When reset applied during Sleep in mode			5	mS	2
			When reset applied during Sleep Out mode			120	mS	5

Note 1: *Spike due to an electrostatic discharge on RESET line does not cause irregular system reset according to the table below.*

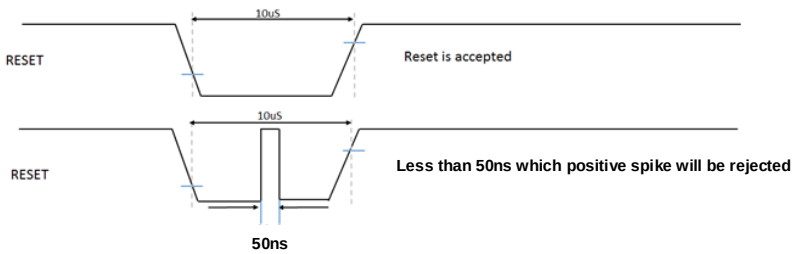
Reset Input Actions

RESET Pulse	Action
Short than 5us	Reset Rejected
Long than 10µS	Reset
Between 5us and 10µS	Reset Start

Note 2: *During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120ms, when Reset Starts in sleep out mode. The display remains the blank state in sleep in mode) and then return to Default condition for H/W RESET.*

Note3: *During Reset Complete Time, values in OTP memory will be latched to internal register during this period. This loading is done every time when there is H/W RESET complete time(tRESET) within 5ms after a rising edge of RESET.*

Note4: *Spike Rejection also applies during a valid reset pulse as shown below.*



Note5: *It is necessary to wait 5ms after releasing RESET before sending commands. Also Sleep Out command cannot be sent for 120msec.*

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7. Command

7.1 Command Table Switch Flow

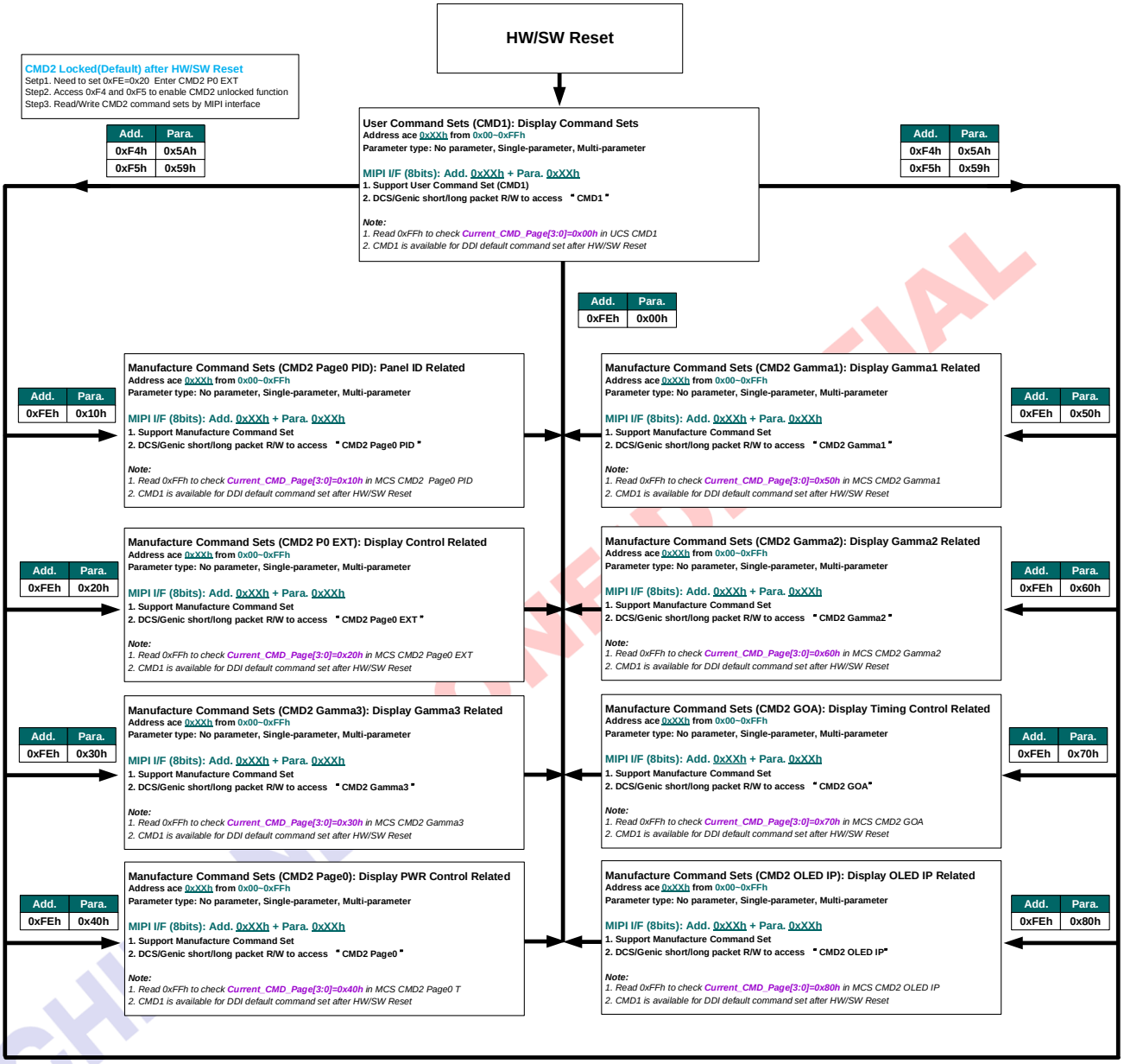


Figure shown Switching Flow for Accessing Registers in UCS / MCS by MIPI interface.

Note:

1. *After power on or HW/SW reset, the default page is in CMD1.*
2. *After power on or HW/SW reset, CMD2 Register Pages are locked.*
   Setp1. Need to set 0xFE=0x20 → Enter CMD2 P0 EXT
   Step2. Access 0xF4 and 0xF5 to enable CMD2 pages unlocked function
   Step3. Read/Write CMD2 page by MIPI interface

7.2 Pass Word Command Description in UCS (Command1)

7.2.1 PASSWD1

(CMD2, F4h)

Command set		PASSWD1								
Inst / Para	**W/R**	**D[7]**	**D[6]**	**D[5]**	**D[4]**	**D[3]**	**D[2]**	**D[1]**	**D[0]**	**Default Value**
PASSWD1	W/R	1	1	1	1	0	1	0	0	F4h
Parameter 1		PASSWORD1[7:0]								00h

(CMD2, F5h)

Command set		PASSWD1								
Inst / Para	**W/R**	**D[7]**	**D[6]**	**D[5]**	**D[4]**	**D[3]**	**D[2]**	**D[1]**	**D[0]**	**Default Value**
PASSWD2	W/R	1	1	1	1	0	1	0	1	F5h
Parameter 1		PASSWORD2[7:0]								00h

NOTE: *"-"Don't care.*

Description

This command is used to lock or unlock the User Command Sets in CMD2.

- Enable CMD1(UCS) command lock/unlock Function (0xFE=0x80)

Setp1. Set 0xFE=0x80 → enter CMD2 page

Step2. Access 0xF4 and 0xF5 to enable lock and unlock function

Address	Parameter	Value	Description
0xF4h	**PASSWORD1[7:0]**	**00h(Default)**	**CMD1(UCS) Unlocked**
		ACh	**CMD1(UCS) locked**
0xF5h	**PASSWORD2[7:0]**	**00h(Default)**	**CMD1(UCS) Unlocked**
		E1h	**CMD1(UCS) locked**

Note:

- Unlocked State

PASSWORD1 [7:0]: This register should be set to "**00h**" for writing / reading Command 1 registers.

PASSWORD2 [7:0]: This register should be set to "**00h**" for writing / reading Command 1 registers.

- Locked State

PASSWORD1 [7:0]: This register should be set to "**ACh**" for Command 1 registers locked.

PASSWORD2 [7:0]: This register should be set to "**E1h**" for Command 1 registers locked.

Restriction

- Must write password 1 first and password 2 last

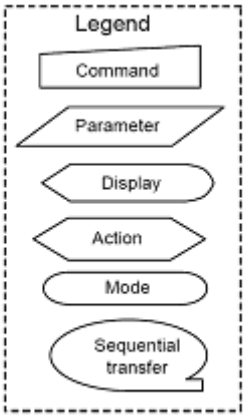
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	F4h	F5h
Power On Sequence	00h	00h
S/W Reset	00h	00h
H/W Reset	00h	00h

Flow Chart



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7.3 Pass Word Command Description in MCS (Command2)

7.3.1 PASSWD2

(CMD2, F4h)

Command set		PASSWD2								
Inst / Para	**W/R**	**D[7]**	**D[6]**	**D[5]**	**D[4]**	**D[3]**	**D[2]**	**D[1]**	**D[0]**	**Default Value**
PASSWD2	W/R	1	1	1	1	0	1	0	0	F4h
Parameter 1		PASSWORD1[7:0]								5Ah

(CMD2, F5h)

Command set		PASSWD2								
Inst / Para	**W/R**	**D[7]**	**D[6]**	**D[5]**	**D[4]**	**D[3]**	**D[2]**	**D[1]**	**D[0]**	**Default Value**
PASSWD2	W/R	1	1	1	1	0	1	0	1	F5h
Parameter 1		PASSWORD2[7:0]								59h

NOTE: *"-"Don't care.*

Description

This command is used to lock or unlock the Manufacture Command Sets in CMD2.

- Enable CMD2(MCS) command lock/unlock Function (0xFE=0x20)

Setp1. Set 0xFE=0x20 → enter CMD2 page

Step2. Access 0xF4 and 0xF5 to enable lock and unlock function

Address	Parameter	Value	Description
0xF4h	**PASSWORD1[7:0]**	**5A**	**CMD1(MCS) Unlocked**
		A5h(Default)	**CMD1(UCS) locked**
0xF5h	**PASSWORD2[7:0]**	**59**	**CMD1(MCS) Unlocked**
		A5h(Default)	**CMD1(UCS) locked**

Note:

- Unlocked State

PASSWORD1 [7:0]: This register should be set to "**5Ah**" for writing / reading Command 1 registers.

PASSWORD2 [7:0]: This register should be set to "**59h**" for writing / reading Command 1 registers.

- Locked State

PASSWORD1 [7:0]: This register should be set to "**A5h**" for Command 2 registers locked.

PASSWORD2 [7:0]: This register should be set to "**A5h**" for Command 2 registers locked.

Restriction

- Must write password 1 first and password 2 last

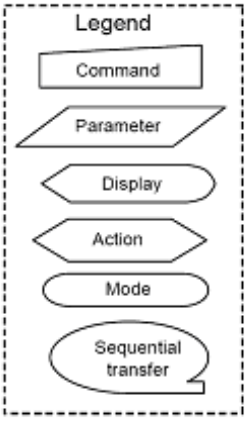
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	F4h	F5h
Power On Sequence	A5h	A5h
S/W Reset	A5h	A5h
H/W Reset	A5h	A5h

Flow Chart



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7.4 Command List

Command			W/R	Function	D7	D6	D5	D4	D3	D2	D1	D0	Default	MTP
Page	Add.	Para.											(hex)	
CMD1	00h	-	W	NOP	No Argument								-	-
CMD1	01h	-	W	Software reset	No Argument								-	-
CMD1	04h	1st	R	Read display identification information	ID1[7:0]								33h	-
CMD1	04h	2nd			ID2[7:0]								11h	-
CMD1	04h	3rd			ID3[7:0]								00h	-
CMD1	05h	-	R	Read number of the errors on DSI	P[7:0]								00h	-
CMD1	0Ah	1st	R	Read display power mode	BSTON	IDMON	PTLON	SLPOUT	NORON	DISPON	-	-	08h	-
CMD1	0Bh	1st	R	Read display MADCTR	MY	MX	-	-	RGB	-	-	-	00h	-
CMD1	0Ch	1st	R	Read display pixel format	SPI_IFPF_SEL	VIPF[2:0]			-	IFPF[2:0]			77h	-
CMD1	0Dh	1st	R	Read display image mode	0	0	INVON	ALLPON	ALLPOFF	0	0	0	00h	-
CMD1	0Eh	1st	R	Read display signal mode	TEON	M	0	0	0	0	0	ERR	00h	-
CMD1	0Fh	1st	R	Read display self-diagnostic result	0	0	0	0	0	0	0	checksum_comp	00h	-
CMD1	10h	-	W	Sleep-in	No Argument								-	-
CMD1	11h	-	W	Sleep-out	No Argument								-	-
CMD1	12h	-	W	Partial display mode on	No Argument								-	-
CMD1	13h	-	W	Normal display mode on	No Argument								-	-
CMD1	20h	-	W	Display inversion off	No Argument								-	-
CMD1	21h	-	W	Display inversion on	No Argument								-	-
CMD1	22h	-	W	All pixel off	No Argument								-	-
CMD1	23h	-	W	All pixel on	No Argument								-	-
CMD1	28h	-	W	Display off	No Argument								-	-
CMD1	29h	-	W	Display on	No Argument								-	-
CMD1	2Ah	1st	W/R	Set column start address	-						SC[9:8]		00h	-
CMD1		2nd			SC[7:0]								00h	-
CMD1		3rd			-						EC[9:8]		01h	-
CMD1		4th			EC[7:0]								C5h	-
CMD1	2Bh	1st	W/R	Set row start address	-						SP[9:8]		00h	-
CMD1		2nd			SP[7:0]								00h	-
CMD1		3rd			-						EP[9:8]		01h	-
CMD1		4th			EP[7:0]								C5h	-
CMD1	2Ch	-	W	Memory Start Write	No Argument								-	-
CMD1	2Eh	-	R	Memory Start Read	No Argument								-	-
CMD1	30h	1st	W/R	Partial area	-						PSL[9:8]		00h	-
CMD1		2nd			PSL[7:0]								00h	-
CMD1		3rd			-						PEL[9:8]		01h	-

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CMD1		4th			PEL[7:0]								C5h	-
CMD1	31h	1st	W/R	Vertical partial area	-						PSC[9:8]		00h	-
CMD1		2nd			PSC[7:0]								00h	-
CMD1		3rd			-						PEC[9:8]		01h	-
CMD1		4th			PEC[7:0]								C5h	-
CMD1	34h	-	W	Tearing effect line off	No Argument								-	-
CMD1	35h	1st	W	Tearing effect line on	-							M	00h	-
CMD1	36h	1st	W	Scan direction control	MY	MX	-	-	RGB	-	-	-	00h	-
CMD1	38h	-	W	Idle mode off	No Argument								-	-
CMD1	39h	-	W	Enter idle mode	No Argument								-	-
CMD1	3Ah	1st	W	Interface Pixel Format	SPI_IFPF_SEL	VIPF[2:0]			0	IFPF[2:0]			77h	-
CMD1	3Ch	-	W	Memory Continuous Write	No Argument								-	-
CMD1	3Eh	-	R	Memory Continuous Read	No Argument								-	-
CMD1	44h	1st	W/R	Set tear scan-line	N[15:8]								00h	-
CMD1		2nd	W		N[7:0]								00h	-
CMD1	45h	1st	R	Get scan line	N[15:8]								00h	-
CMD1		2nd			N[7:0]								00h	-
CMD1	4Fh	1st	W	Deep standby	0	0	0	0	0	0	0	DSTB	00h	-
CMD1	51h	1st	W	Write display brightness	DBV[7:0]								00h	-
CMD1	52h	1st	R	Read display brightness	DBV[7:0]								00h	-
CMD1	53h	1st	W	Write CTRL display	0	0	BC_EN	0	DIM_EN	0	0	0	28h	-
CMD1	54h	1st	R	Read CTRL display	0	0	BC_EN	0	DIM_EN	0	0	0	28h	-
CMD1	55h	1st	W	Write ACL function	0	0	0	0	0	0	ACL[1:0]		00h	
CMD1	56h	1st	R	Read ACL function	0	0	0	0	0	0	ACL[1:0]		00h	
CMD1	58h	1st	W	Set color enhancement	0	0	0	0	0	SLR_EN	SLR_LEVEL[1:0]		00h	-
CMD1	59h	1st	R	Read color enhancement	0	0	0	0	0	SLR_EN	SLR_LEVEL[1:0]		00h	-
CMD1	5Fh	1st	R/W	Read Loacl HBM	-	-	-	-	-	-	-	Local_hbm_en	40h	
CMD1	60h	1st	R/W	Dynamic Frame rate control	-	normal_level[2:0]			-	-	idle_level[1:0]		00h	
CMD1	61h	1st	R/W	Enable Dynamic Frame rate	-	-	-	-	-	-	dynf_en_B	dynf_en_A	00h	
CMD1	63h	1st	W	Write HBM display brightness	DBV_HBM[7:0]								00h	
CMD1	64h	1st	R	Read HBM display brightness	DBV_HBM[7:0]								00h	
CMD1	66h	1st	W	HBM enable	-	-	-	-	-	-	HBM_EN	-	00h	
CMD1	70h	1st	W/R	COLSET	R_0000[7:0]								00h	
CMD1		2nd		COLSET	G_0000[7:0]								00h	
CMD1		3rd		COLSET	B_0000[7:0]								00h	
CMD1	71h	1st	W/R	COLSET	R_0001[7:0]								00h	
CMD1		2nd		COLSET	G_0001[7:0]								00h	
CMD1		3rd		COLSET	B_0001[7:0]								FFh	
CMD1	72h	1st	W/R	COLSET	R_0010[7:0]								00h	
CMD1		2nd		COLSET	G_0010[7:0]								FFh	

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CMD1		3rd		COLSET	B_0010[7:0]						00h	
CMD1		1st		COLSET	R_0011[7:0]						00h	
CMD1	73h	2nd	W/R	COLSET	G_0011[7:0]						FFh	
CMD1		3rd		COLSET	B_0011[7:0]						FFh	
CMD1		1st		COLSET	R_0100[7:0]						FFh	
CMD1	74h	2nd	W/R	COLSET	G_0100[7:0]						00h	
CMD1		3rd		COLSET	B_0100[7:0]						00h	
CMD1		1st		COLSET	R_0101[7:0]						FFh	
CMD1	75h	2nd	W/R	COLSET	G_0101[7:0]						00h	
CMD1		3rd		COLSET	B_0101[7:0]						FFh	
CMD1		1st		COLSET	R_0110[7:0]						FFh	
CMD1	76h	2nd	W/R	COLSET	G_0110[7:0]						FFh	
CMD1		3rd		COLSET	B_0110[7:0]						00h	
CMD1		1st		COLSET	R_0111[7:0]						FFh	
CMD1	77h	2nd	W/R	COLSET	G_0111[7:0]						FFh	
CMD1		3rd		COLSET	B_0111[7:0]						FFh	
CMD1		1st		COLSET	R_1000[7:0]						00h	
CMD1	78h	2nd	W/R	COLSET	G_1000[7:0]						00h	
CMD1		3rd		COLSET	B_1000[7:0]						00h	
CMD1		1st		COLSET	R_1001[7:0]						00h	
CMD1	79h	2nd	W/R	COLSET	G_1001[7:0]						00h	
CMD1		3rd		COLSET	B_1001[7:0]						FFh	
CMD1		1st		COLSET	R_1010[7:0]						00h	
CMD1	7Ah	2nd	W/R	COLSET	G_1010[7:0]						FFh	
CMD1		3rd		COLSET	B_1010[7:0]						00h	
CMD1		1st		COLSET	R_1011[7:0]						00h	
CMD1	7Bh	2nd	W/R	COLSET	G_1011[7:0]						FFh	
CMD1		3rd		COLSET	B_1011[7:0]						FFh	
CMD1		1st		COLSET	R_1100[7:0]						FFh	
CMD1	7Ch	2nd	W/R	COLSET	G_1100[7:0]						00h	
CMD1		3rd		COLSET	B_1100[7:0]						00h	
CMD1		1st		COLSET	R_1101[7:0]						FFh	
CMD1	7Dh	2nd	W/R	COLSET	G_1101[7:0]						00h	
CMD1		3rd		COLSET	B_1101[7:0]						FFh	
CMD1		1st		COLSET	R_1110[7:0]						FFh	
CMD1	7Eh	2nd	W/R	COLSET	G_1110[7:0]						FFh	
CMD1		3rd		COLSET	B_1110[7:0]						00h	
CMD1		1st		COLSET	R_1111[7:0]						FFh	
CMD1	7Fh	2nd	W/R	COLSET	G_1111[7:0]						FFh	
CMD1		3rd		COLSET	B_1111[7:0]						FFh	
CMD1	80h	1st	W	GRAY256_COLOR	-	RGB111_opt	-	-	RGB4bit_en	Gray256_color[2:0]	07h	
CMD1	A1h	1st	R	Read DDB	SID[7:0]						33h	-

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CMD1		2nd			SID[15:8]								10h	-
CMD1		3rd			MID[7:0]								00h	-
CMD1		4th			MID[15:8]								00h	-
CMD1		5th			1	1	1	1	1	1	1	1	FFh	-
CMD1		1st			SID[7:0]								33h	-
CMD1		2nd			SID[15:8]								10h	-
CMD1	A8h	3rd	R	Read DDB Continuous	MID[7:0]								00h	-
CMD1		4th			MID[15:8]								00h	-
CMD1		5th			1	1	1	1	1	1	1	1	FFh	-
CMD1	AAh	1st	R	Read first checksum	FCS[7:0]								00h	-
CMD1	AFh	1st	R	Read continuous checksum	CCS[7:0]								00h	-
CMD1	C2h	1st	W/R	Set_DSIP Mode	0	0	0	0	0	0	DM[1:0]		00h	-
CMD1	C4h	1st	W/R	Set_DSPI Mode	SPI_WRAM_CMD1	0	DSPI_CFG[1:0]		0	0	DSPI_single_DCX	DSPI_SPI_EN	00h	-
CMD1	DAh	1st	R	Read display identification	ID1[7:0]								33h	-
CMD1	DBh	1st	R	information	ID2[7:0]								10h	-
CMD1	DCh	1st	R	(the same as 04h)	ID3[7:0]								00h	-
CMD1	E1h	1st	R		CHIP_ID1[7:0]								33h	
CMD1	E2h	1st	R	CHIPONE ID	CHIP_ID2[7:0]								10h	
CMD1	E3h	1st	R		CHIP_ID3[7:0]								00h	
CMD1	FEh	1st	W	Write CMD mode page	0	0	0	0	CMD_Page_Selection[3:0]				00h	-
CMD1	FFh	1st	R	Read CMD page Status	0	0	0	0	Current_CMD_Page[3:0]				00h	-

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7.5 Command Description

7.5.1 NOP: NOP (00h)

Command set		NOP								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
NOP	W	0	0	0	0	0	0	0	0	00h
Parameter 1		No Parameter								

NOTE: *"-"Don't care*

Description	This command is empty command. It does not have effect on the display module.
Restriction	-
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart	-

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7.5.2 SWRESET: Software Reset (01h)

Command set		SWRESET								
Inst / Para	**W/R**	**D[7]**	**D[6]**	**D[5]**	**D[4]**	**D[3]**	**D[2]**	**D[1]**	**D[0]**	**Default Value**
SWRESET	W	0	0	0	0	0	0	0	1	00h
Parameter 1		No Parameter								

NOTE: *"-"Don't care*

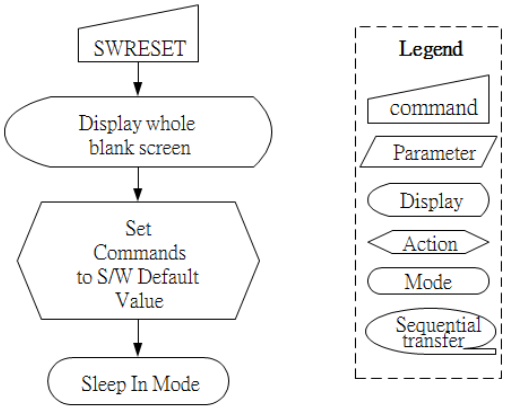
Description	When the Software Reset command is written, it causes software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.)
Restriction	It will be necessary to wait 5msec before sending new command following software reset. The display module loads all display suppliers' factory default values to the registers during 5msec. If Software Reset is applied during Sleep Out mode, it will be necessary to wait 120msec before sending Sleep Out command. Software Reset command cannot be sent during Sleep Out sequence.
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

Flow Chart



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7.5.3 RDDID: Read Display ID (04h)

Command set		RDDID								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
RDDID	R	0	0	0	0	0	1	0	0	04h
Parameter 1		ID1[7:0]								33h
Parameter 2		ID2[7:0]								11h
Parameter 3		ID3[7:0]								00h

NOTE: *"-"Don't care*

Description

This command is used to read Driver ID

- ID1[7:0]:ID1: the driver version ID
- ID2[7:0]:ID2: the driver version ID
- ID3[7:0]:ID3: the driver version ID

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

If ID1/ID2/ID3 OTP are not yet programmed:

Status	Default Value		
	ID1	ID2	ID3
Power On Sequence	33h	10h	00h
S/W Reset	33h	10h	00h
H/W Reset	33h	10h	00h

If ID1/ID2/ID3 OTP were programmed:

Status	Default Value		
	ID1	ID2	ID3
Power On Sequence	(OTP value)	(OTP value)	(OTP value)
S/W Reset	(OTP value)	(OTP value)	(OTP value)
H/W Reset	(OTP value)	(OTP value)	(OTP value)

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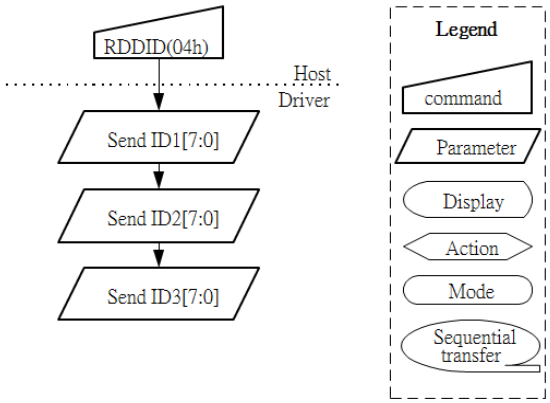
Flow Chart	

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7.5.4 RDNUMED: Read Number of Errors on DSI (05h)

Command set		RDNUMED								
Inst / Para	**W/R**	**D[7]**	**D[6]**	**D[5]**	**D[4]**	**D[3]**	**D[2]**	**D[1]**	**D[0]**	**Default Value**
RDNUMED	R	0	0	0	0	0	1	0	1	05h
Parameter 1		P[7:0]								00h

NOTE: *"-"Don't care*

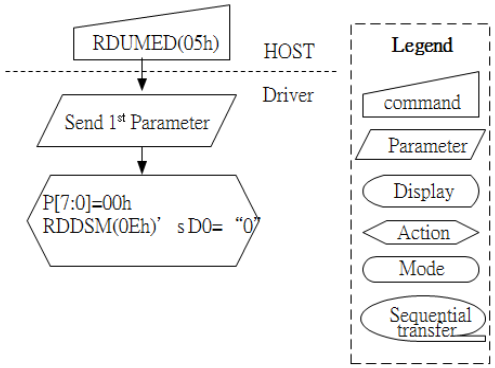
Description	The first parameter is telling a number of the parity errors on DSI. The more detailed description of the bits is below. P[6..0] bits are telling a number of the parity errors. P[7] is set to "1" if there is overflow with P[6..0] bits. P[7..0] bits are set to "0"s (as well as RDDSM(0Eh)'s D0 are set "0" at the same time) after there is sent the first parameter information (= The read function is completed). See also section "Acknowledge with Error Report (AwER)" and command RDDSM 0Eh.
Restriction	-
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



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7.5.5 RDDPM: Read Display Power Mode (0Ah)

Command set		RDDST								
Inst / Para	**W/R**	**D[7]**	**D[6]**	**D[5]**	**D[4]**	**D[3]**	**D[2]**	**D[1]**	**D[0]**	**Default Value**
RDDST	R	0	0	0	0	1	0	1	0	0Ah
Parameter 1		BSTON	IDMON	PTLON	SLPOUT	NORON	DISPON	-	-	08h

NOTE: *"-"Don't care*

Description

This command indicates the current status of the display as described in the table below.

- BSTON:BSTON: Booster Voltage Status
- IDMON:IDMON: Idle Mode On/Off
- PTLON:PTLON: Partial Mode On/Off
- SLPOUT:SLPOUT: Sleep In/Out
- NORON:NORON: Display Normal Mode On/Off
- DISPON:DISON: Display On/Off

Bit	Description	Value
D7	Booster ON/OFF	"1": Booster ON, "0": Booster OFF
D6	Idle Mode ON/OFF	"1": Idle Mode ON, "0": Idle Mode OFF
D5	Partial Mode ON/OFF	"1": Partial Mode ON, "0": Partial Mode OFF
D4	Sleep Out	"1": Sleep Out, "0": Sleep In
D3	Normal Mode ON/OFF	"1": Normal Display, "0": Partial Display
D2	Display Mode ON/OFF	"1": Display ON, "0": Display OFF
D1	Not Used	"0"
D0	Not Used	"0"

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h,71h,00h,00h
S/W Reset	00h,71h,00h,00h
H/W Reset	00h,71h,00h,00h

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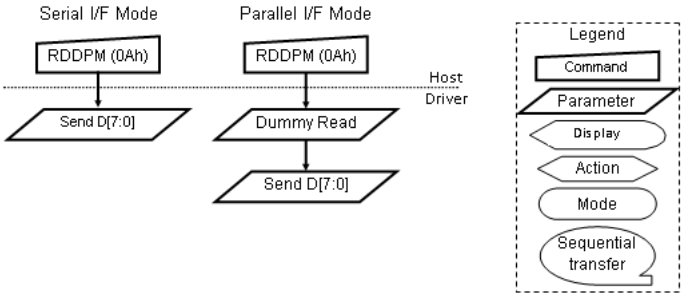
Flow Chart	

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7.5.6 RDDMADCTR: Read Display MADCTR (0Bh)

Command set		RDDMADCTR								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
RDDMADCTR	R	0	0	0	0	1	0	1	1	0Bh
Parameter 1		MY	MX	-	-	RGB	-	-	-	00h

NOTE: *"-"Don't care*

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	MY: Row Address Increment	"1": Increasing in vertical, "0": Decreasing in vertical
D6	MX: Column Address Increment	"1": Increasing in horizontal, "0": Decreasing in horizontal
D5	Not Used	"0"
D4	Not Used	"0"
D3	RGB/BGR Order	"1"=BGR, "0"=RGB
D2	Not Used	"0"
D1	Not Used	"0"
D0	Not Used	"0"

Restriction

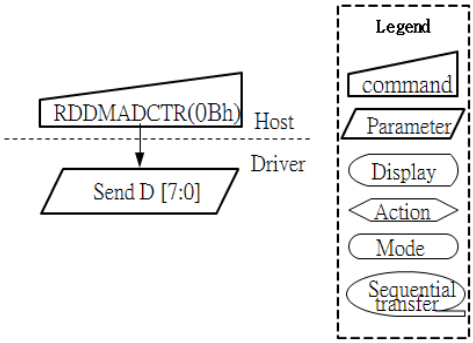
-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart	

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7.5.7 RDDCOLMOD: Read Display Pixel Format (0Ch)

Command set		RDDCOLMOD								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
RDDCOLMOD	R	0	0	0	0	1	1	0	0	0Ch
Parameter 1		SPI_IFPF_SEL	VIPF[2:0]	-	IFPF[2:0]	SPI_IFPF_SEL	VIPF[2:0]	-	IFPF[2:0]	77h

NOTE: *"-"Don't care*

Description

This command indicates the current status of the display as described in the table below:

- To return the status of 0x3A00.

This command sets the pixel format for the RGB image data used by the interface.

If SPI_IFPF_SEL(3Ah-B7) = 1: The VIPF[2:0] pixel format used by the SPI interface

If SPI_IFPF_SEL(3Ah-B7) = 0: The IFPF[2:0] pixel format used by the SPI / MCU interface

If not used DPI interface, then the corresponding bits in the parameter are ignored.

- SPI_IFPF_SEL: Sets the pixel format for the RGB image data used by the interface.

Value	Description
0	The IFPF[2:0] pixel format used by the SPI / MCU interface
1	The VIPF[2:0] pixel format used by the SPI interface

- VIPF[2:0]:Pixel Format(Control Interface Color Format) for RGB_IF and SPI

Value	Description
001	SPI 256 Gray / pixel
010	SPI 3-3-2 / pixel
011	SPI 1-1-1 / pixel
101	16-bits / pixel
110	18-bits / pixel
111	24-bits / pixel

- IFPF[2:0]:Pixel Format(Control Interface Color Format) for MCU and SPI

Value	Description
001	SPI 256 Gray / pixel
010	SPI 3-3-2 / pixel
011	SPI 1-1-1 / pixel
101	16-bits / pixel
110	18-bits / pixel
111	24-bits / pixel

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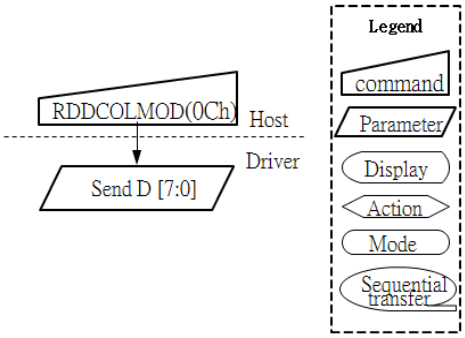
Restriction	-
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	77h
S/W Reset	77h
H/W Reset	77h

Flow Chart



7.5.8 RDDIM: Read Display Image Mode (0Dh)

Command set		RDDIM								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
RDDIM	R	0	0	0	0	1	1	0	1	0Dh
Parameter 1		0	0	INVON	ALLPON	ALLPOFF	0	0	0	00h

NOTE: *"-"Don't care*

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Not Used	"0"
D6	Not Used	"0"
D5	Inversion On/Off	"1": Inversion ON, "0": Inversion OFF
D4	All Pixels On	"1": White display, "0": Normal display
D3	All Pixels Off	"1": Black Display, "0": Normal display
D2	Not Used	"0"
D1	Not Used	"0"
D0	Not Used	"0"

Restriction

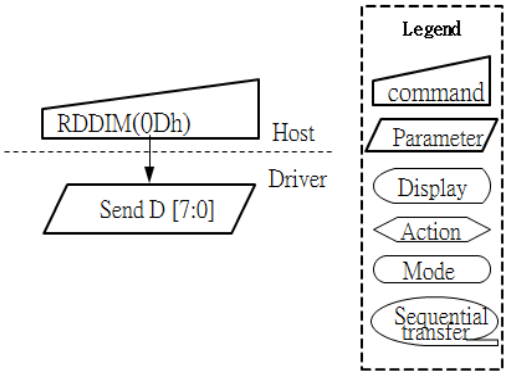
-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart	

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7.5.9 RDDIM: Read Display Signal Mode (0Eh)

Command set		RDDIM								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
RDDSM	R	0	0	0	0	1	1	1	0	0Eh
Parameter 1		TEON	M	0	0	0	0	0	ERR	00h

NOTE: *"-"Don't care*

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Tearing Effect Line On/Off	"1" = ON, "0" = OFF
D6	Tearing effect line mode	"1" = Mode 2, "0" =Mode 1
D5	Not Used	"0"
D4	Not Used	"0"
D3	Not Used	"0"
D2	Not Used	"0"
D1	Not Used	"0"
D0	Error on DSI	"1" = Error, "0" = No Error

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

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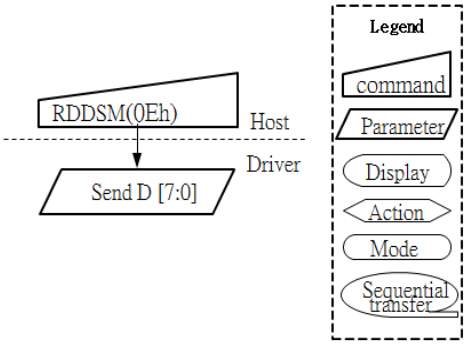
Flow Chart	

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7.5.10 RDDSDR: Read Display Self-Diagnostic Result (0Fh)

Command set		RDDSDR								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
RDDSDR	R	0	0	0	0	1	1	1	1	0Fh
Parameter 1		0	0	0	0	0	0	0	checksum_comp	00h

NOTE: *"-"Don't care*

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Not Used	"0"
D6	Not Used	"0"
D5	Not Used	"0"
D4	Not Used	"0"
D3	Not Used	"0"
D2	Not Used	"0"
D1	Not Used	"0"
D0	Checksum compare result flag	"1" = Error, "0" = No Error

Restriction

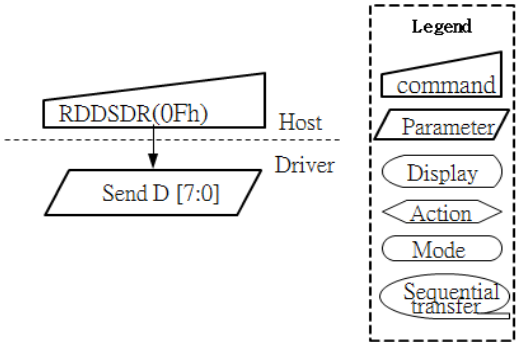
-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart	

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7.5.11 SLPIN: Sleep In (10h)

Command set		SLPIN								
Inst / Para	**W/R**	**D[7]**	**D[6]**	**D[5]**	**D[4]**	**D[3]**	**D[2]**	**D[1]**	**D[0]**	**Default Value**
SLPIN	W	0	0	0	1	0	0	0	0	10h
Parameter 1		No Parameter								

NOTE: *"-"Don't care*

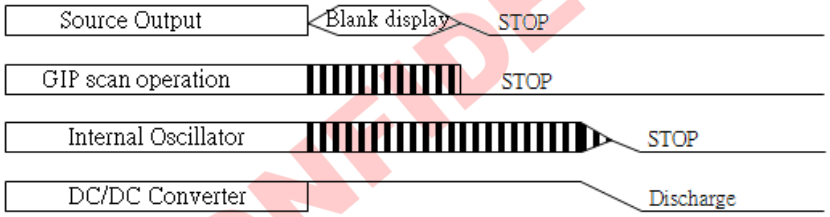
Description

This command causes the LCD module to enter the minimum power consumption mode.

In this mode the DC/DC converter is stopped, Internal display oscillator is stopped, and panel scanning is stopped.

After Sleep in command, user can send PCLK, HS and VS information on RGB I/F for blank display and this information is valid during 2 frames if there is used Normal Mode On in Sleep Out-mode.

There is used an internal oscillator for blank display.



Restriction

This command has no effect when module is already in sleep in mode. Sleep In Mode can only be exit by the Sleep Out Command (11h).

It will be necessary to wait 5msec before sending next command; this is to allow time for the supply voltages and clock circuits to stabilize.

It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep In mode
S/W Reset	Sleep In mode
H/W Reset	Sleep In mode

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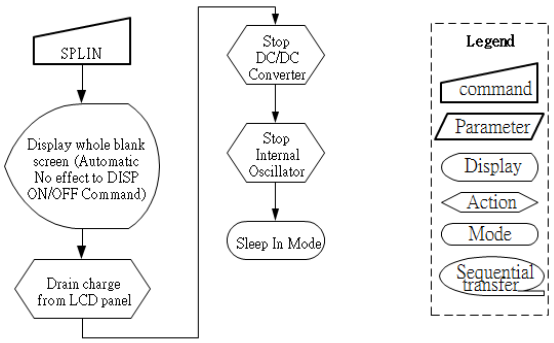
Flow Chart	It takes about 120msec to get into Sleep In mode (booster off state) after SLPIN command issued. The results of booster off can be check by RDDST (09h) command Bit 31. 

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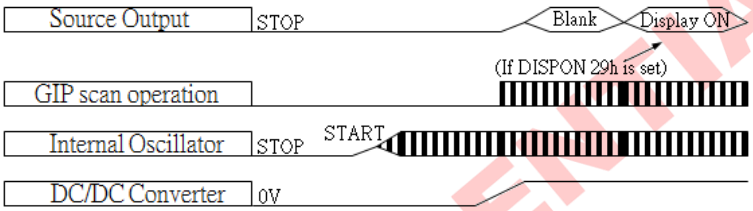
7.5.12 SLPOUT: Sleep Out (11h)

Command set		SLPOUT								
Inst / Para	**W/R**	**D[7]**	**D[6]**	**D[5]**	**D[4]**	**D[3]**	**D[2]**	**D[1]**	**D[0]**	**Default Value**
SLPOUT	W	0	0	0	1	0	0	0	1	11h
Parameter 1		No Parameter								

NOTE: *"-"Don't care*

Description

This command causes the display module to exit Sleep mode. All blocks inside the display module are enabled. The host processor sends PCLK, HS and VS information to display modules two frames before this command is sent when the display module is in Normal Mode.



Restriction

This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be exit by the Sleep In Command (10h).

It will be necessary to wait 5msec before sending next command; this is to allow time for the supply voltages and clock circuits to stabilize.

ICNA3312 loads all default values of extended and test command to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if those default and register values are same when this load is done and when the ICNA3312 is already Sleep Out –mode.

ICNA3312 is doing self-diagnostic functions during this 5msec. It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep Out mode
S/W Reset	Sleep Out mode
H/W Reset	Sleep Out mode

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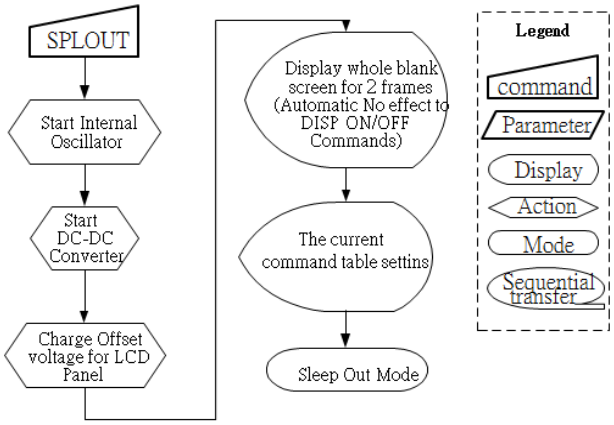
Flow Chart	It takes 120msec to become Sleep Out mode (booster on mode) after SLPOUT command issued. 

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7.5.13 PARON: Partial Display Mode ON (12h)

Command set		PARON								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
NORON	W	0	0	0	1	0	0	1	0	12h
Parameter 1		No Parameter								

NOTE: *"-"Don't care*

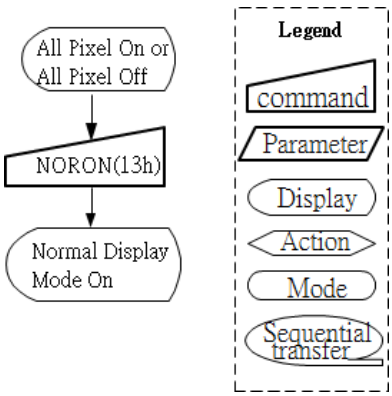
Description	This command causes the display module to enter the Partial Display Mode. The Partial Display Mode window is described To leave Partial Display Mode, the Normal Display Mode On (13h) command should be written. The host processor continues to send PCLK, HS and VS information to display modules for two frames after this command is sent when the display module is in Normal Display Mode.
Restriction	This command has no effect when Normal Display mode is active.
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Normal Mode On
S/W Reset	Normal Mode On
H/W Reset	Normal Mode On

Flow Chart



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7.5.14 NORON: Normal Display Mode ON (13h)

Command set		NORON								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
NORON	W	0	0	0	1	0	0	1	1	13h
Parameter 1		No Parameter								

NOTE: *"-"Don't care*

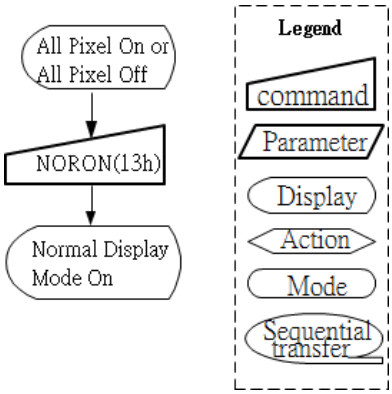
Description	This command causes the display module to enter the Normal mode. Normal Mode is defined as Partial Display mode. The host processor sends PCLK, HS and VS information to Type 2 display modules two frames before this command is sent when the display module is in Partial Display Mode.
Restriction	This command has no effect when Normal Display mode is active.
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Normal Mode On
S/W Reset	Normal Mode On
H/W Reset	Normal Mode On

Flow Chart



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7.5.15 INVOFF: Display Inversion OFF (20h)

Command set		INVOFF								
Inst / Para	**W/R**	**D[7]**	**D[6]**	**D[5]**	**D[4]**	**D[3]**	**D[2]**	**D[1]**	**D[0]**	**Default Value**
INVOFF	W	0	0	1	0	0	0	0	0	20h
Parameter 1		No Parameter								

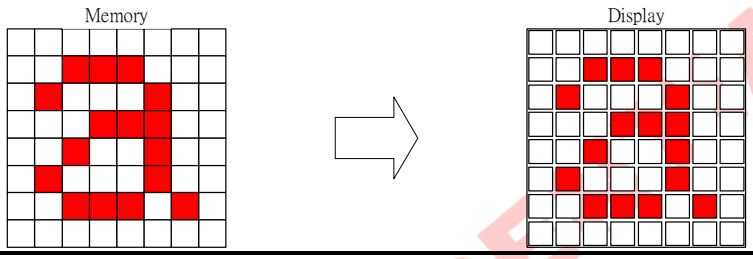
NOTE: *"-"Don't care*

Description

This command causes the display module to stop inverting the image data on the display device.

No status bits are changed.

(Example)



Restriction

This command has no effect when module is already inversion off mode.

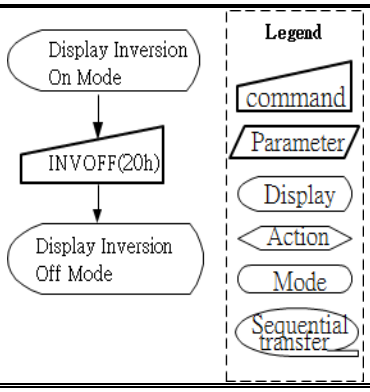
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Inversion Off
S/W Reset	Display Inversion Off
H/W Reset	Display Inversion Off

Flow Chart



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7.5.16 INVON: Display Inversion ON (21h)

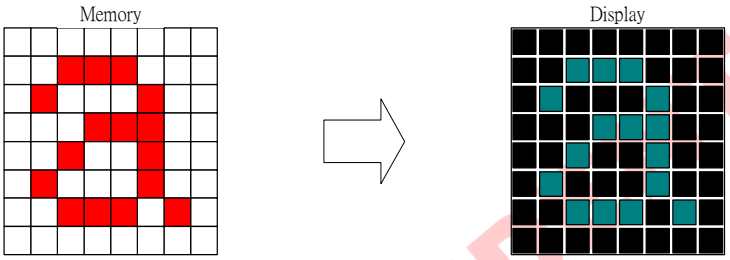
Command set		INVON								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
INVON	W	0	0	1	0	0	0	0	1	21h
Parameter 1		No Parameter								

NOTE: *"-"Don't care*

Description

This command causes the display module to invert the image data only on the display device. No status bits are changed.

(Example)



Restriction

This command has no effect when module is already inversion On mode.

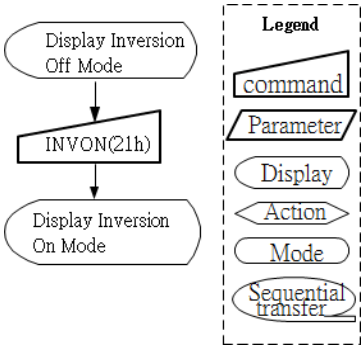
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Inversion Off
S/W Reset	Display Inversion Off
H/W Reset	Display Inversion Off

Flow Chart



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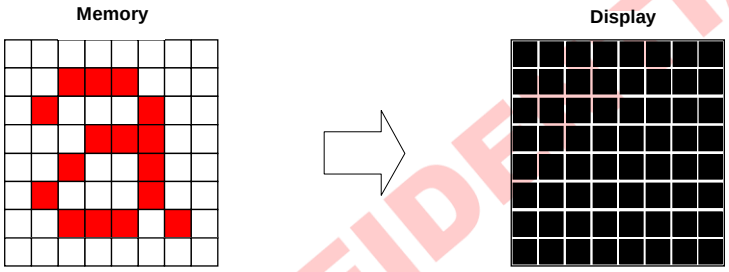
7.5.17 ALLPOFF: All Pixel OFF (22h)

Command set		ALLPOFF								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
ALLPOFF	W	0	0	1	0	0	0	1	0	22h
Parameter 1		No Parameter								

NOTE: *"-"Don't care*

Description	This command turns the display panel black in Sleep Out mode and a status of the Display On/Off register can be on or off. This command makes no change of contents of frame memory. This command does not change any other status. **(Example)**  "All Pixels On", "Normal Display Mode On" commands are used to leave this mode. The display panel is showing the content of the frame memory after "Normal Display On" command.
Restriction	This command has no effect when module is already in All Pixel Off mode.
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	All Pixels Off
S/W Reset	All Pixels Off
H/W Reset	All Pixels Off

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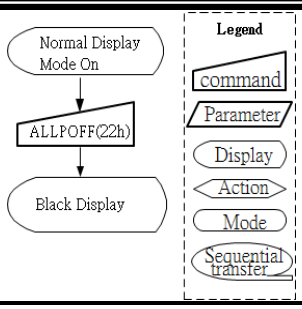
Flow Chart	

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7.5.18 ALLPON: All Pixel ON (23h)

Command set		ALLPON								
Inst / Para	**W/R**	**D[7]**	**D[6]**	**D[5]**	**D[4]**	**D[3]**	**D[2]**	**D[1]**	**D[0]**	**Default Value**
ALLPON	W	0	0	1	0	0	0	1	1	23h
Parameter 1		No Parameter								

NOTE: *"-"Don't care*

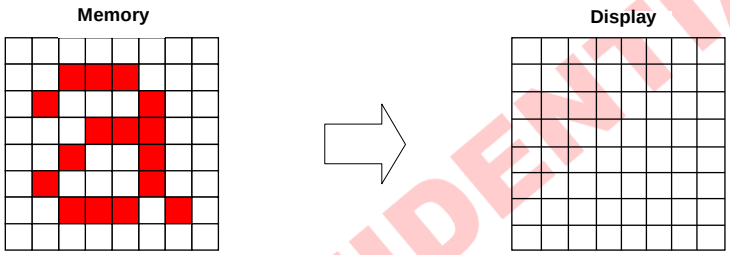
Description

This command turns the display panel white in Sleep Out mode and a status of the Display On/Off register can be on or off.

This command makes no change of contents of frame memory.

This command does not change any other status.

(Example)



"All Pixels OFF", "Normal Display Mode On" commands are used to leave this mode. The display panel is showing the content of the frame memory after "Normal Display On" command.

Restriction

This command has no effect when module is already in All Pixel On mode.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	All Pixels Off
S/W Reset	All Pixels Off
H/W Reset	All Pixels Off

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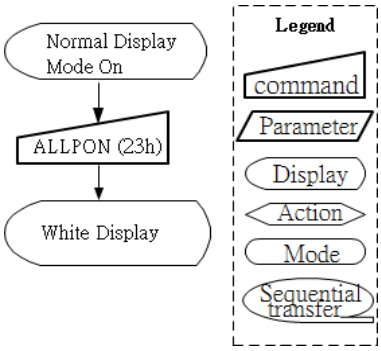
Flow Chart	

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7.5.19 DISPOFF: Display OFF (28h)

Command set		DISPOFF								
Inst / Para	**W/R**	**D[7]**	**D[6]**	**D[5]**	**D[4]**	**D[3]**	**D[2]**	**D[1]**	**D[0]**	**Default Value**
DISPOFF	W	0	0	1	0	1	0	0	0	28h
Parameter 1		No Parameter								

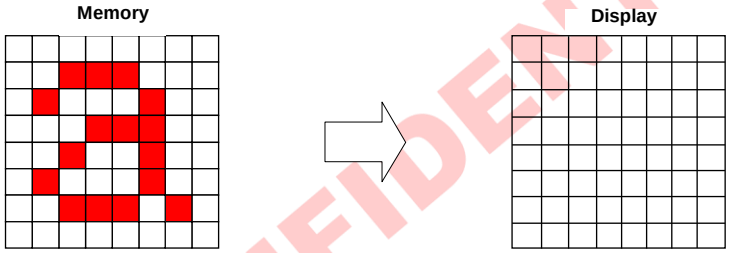
NOTE: *"-"Don't care*

Description

This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted.

This command makes no change of contents of frame memory. This command does not change any other status. There will be no abnormal visible effect on the display.

(Example)



Restriction

This command has no effect when module is already in Display Off mode.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Off
S/W Reset	Display Off
H/W Reset	Display Off

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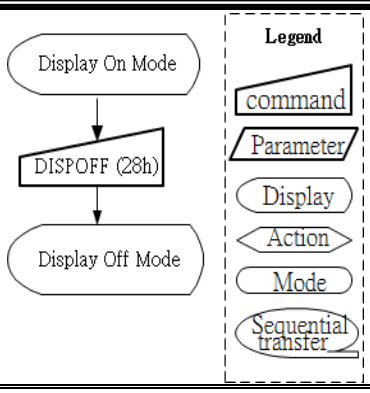
Flow Chart	

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7.5.20 DISPON: Display ON (29h)

Command set		DISPON								
Inst / Para	**W/R**	**D[7]**	**D[6]**	**D[5]**	**D[4]**	**D[3]**	**D[2]**	**D[1]**	**D[0]**	**Default Value**
DISPON	W	0	0	1	0	1	0	0	1	29h
Parameter 1		No Parameter								

NOTE: *"-"Don't care*

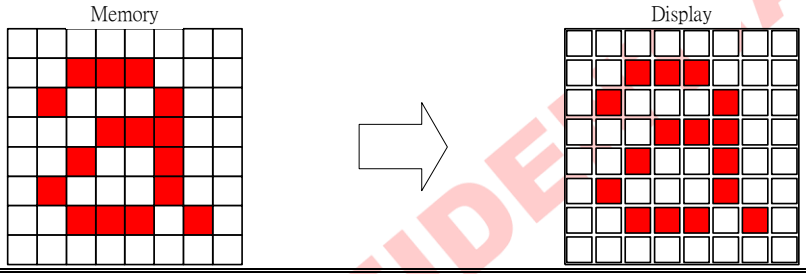
Description

This command is used to recover from DISPLAY OFF mode.

This command makes no change of contents of frame memory.

This command does not change any other status.

(Example)



Restriction

This command has no effect when module is already in Display On mode.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Off
S/W Reset	Display Off
H/W Reset	Display Off

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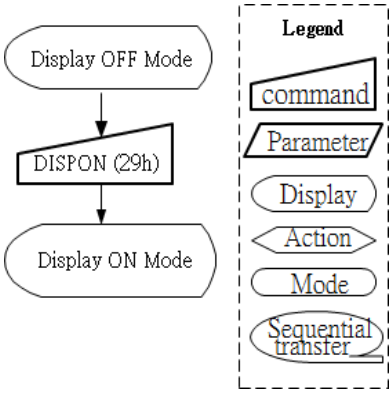
Flow Chart	

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7.5.21 CASET: Set Column Start Address (2Ah)

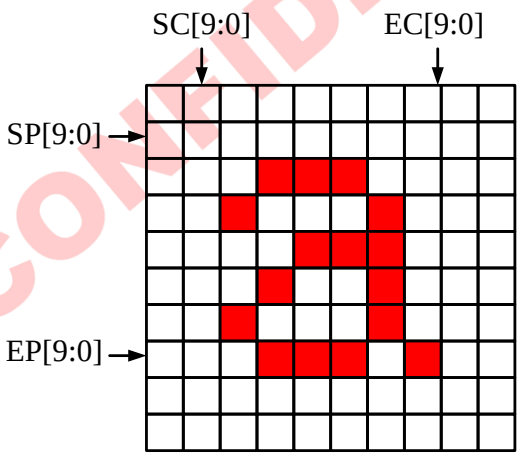
Command set		CASET								
Inst / Para	**W/R**	**D[7]**	**D[6]**	**D[5]**	**D[4]**	**D[3]**	**D[2]**	**D[1]**	**D[0]**	**Default Value**
CASET	W/R	0	0	1	0	1	0	1	0	2Ah
Parameter 1								SC[9:8]		00h
Parameter 2		SC[7:0]								00h
Parameter 3								SE[9:8]		01h
Parameter 4		SE[7:0]								C5h

NOTE: *"-"Don't care*

Description

This command defines the column extent of the frame memory accessed by the host processor with the read_memory_continue and write_memory_continue

This command makes no change on the other driver status. The values of SC[9:0] and EC[9:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory.



Restriction

- SC[9:0] always must be equal to or less than EC[9:0].
- The SC[9:0] and EC[9:0]-SC[9:0]+1 must can be divisible by 2.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

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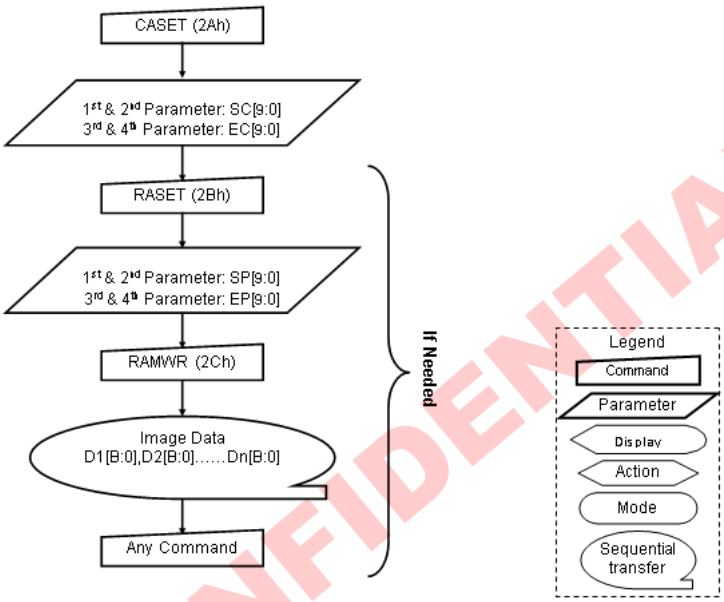
Default

Status	Default Value	
	SC[9:0]	SE[9:0]
Power On Sequence	0000h	01C5h
S/W Reset	0000h	01C5h
H/W Reset	0000h	01C5h

Flow Chart



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7.5.22 RASET: Set Row Start Address (2Bh)

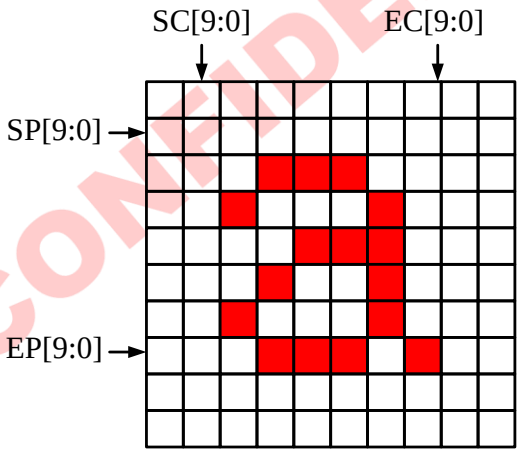
Command set		RASET								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
RASET	W/R	0	0	1	0	1	0	1	0	2Bh
Parameter 1		SP[9:8]								00h
Parameter 2		SP[7:0]								00h
Parameter 3		EP[9:8]								01h
Parameter 4		EP[7:0]								C5h

NOTE: *"-"Don't care*

Description

This command defines the column extent of the frame memory accessed by the host processor with the read_memory_continue and write_memory_continue

This command makes no change on the other driver status. The values of SP[9:0] and EP[9:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory.



Restriction

- SP[9:0] always must be equal to or less than EC[9:0].
- The SCP9:0] and EP[9:0]-SP[9:0]+1 must can be divisible by 2.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

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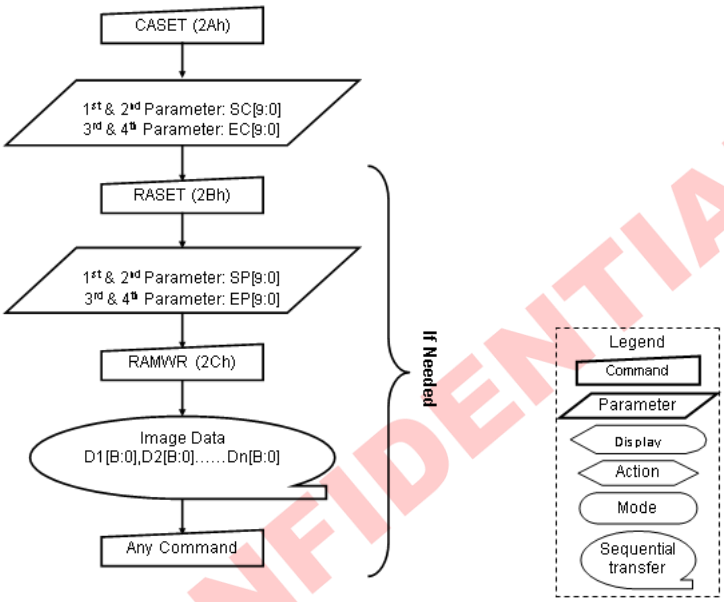
Default

Status	Default Value	
	SP[9:0]	EP[9:0]
Power On Sequence	0000h	01C5h
S/W Reset	0000h	01C5h
H/W Reset	0000h	01C5h

Flow Chart



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7.5.23 RAMWR: Memory Start Write (2Ch)

Command set		RAMWR								
Inst / Para	**W/R**	**D[7]**	**D[6]**	**D[5]**	**D[4]**	**D[3]**	**D[2]**	**D[1]**	**D[0]**	**Default Value**
RAMWR	W	0	0	1	0	1	1	0	0	2Ch
Parameter 1		D_{17}	D_{16}	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	-
…		…								-
…		…								-
Parameter n		D_{N7}	D_{N6}	D_{N5}	D_{N4}	D_{N3}	D_{N2}	D_{N1}	D_{N0}	-

NOTE: *"-"Don't care*

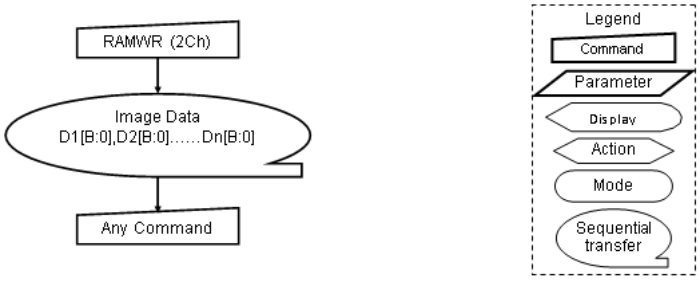
Description	This command transfers image data from the host processor to the display module's frame memory starting at the pixel location specified by preceding CASET (2Ah) and RASET (2Bh) commands.
Restriction	A Memory Write should follow a CASET(2Ah), RASET(2Bh) or MADCTR(36h) to define the write location. Otherwise, data written with RAMWR(2Ch) and any following RAMWRC(3Ch) commands is written to undefined locations.
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Memory is set randomly
S/W Reset	Memory is not cleared
H/W Reset	Memory is not cleared

Flow Chart



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7.5.24 RAMWR: Memory Start Read (2Eh)

Command set		RAMRD								
Inst / Para	**W/R**	**D[7]**	**D[6]**	**D[5]**	**D[4]**	**D[3]**	**D[2]**	**D[1]**	**D[0]**	**Default Value**
RAMRD	R	0	0	1	0	1	1	1	0	2Eh
Parameter 1		D_{17}	D_{16}	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	-
…		…								-
…		…								-
Parameter n		D_{N7}	D_{N6}	D_{N5}	D_{N4}	D_{N3}	D_{N2}	D_{N1}	D_{N0}	-

NOTE: *"-"Don't care*

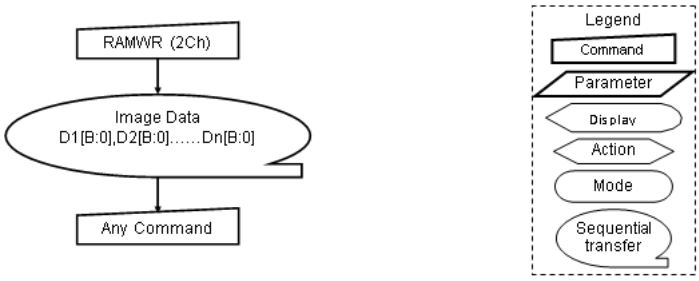
Description	This command transfers image data from the display module's frame memory to the host processor starting at the pixel location specified by preceding CASET (2Ah) and RASET (2Bh) commands.
Restriction	A Memory Write should follow a CASET(2Ah), RASET(2Bh) or MADCTR(36h) to define the write location. Otherwise, data written with RAMWR(2Eh) and any following RAMWRC(3Eh) commands is written to undefined locations.
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Memory is set randomly
S/W Reset	Memory is not cleared
H/W Reset	Memory is not cleared

Flow Chart



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7.5.25 PTLAR: Set Vertical Partial Area (30h)

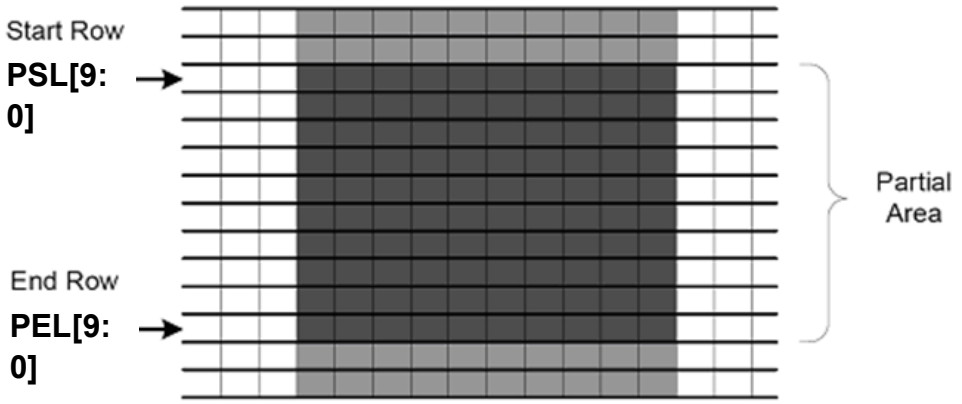
Command set		PTLAR								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
PTLAR	W/R	0	0	1	1	0	0	0	0	30h
Parameter 1		-						PSL[9:8]		00h
Parameter 2		PSL[7:0]								00h
Parameter 3		-						PEL[9:8]		01h
Parameter 4		PEL[7:0]								C5h

NOTE: *"-"Don't care*

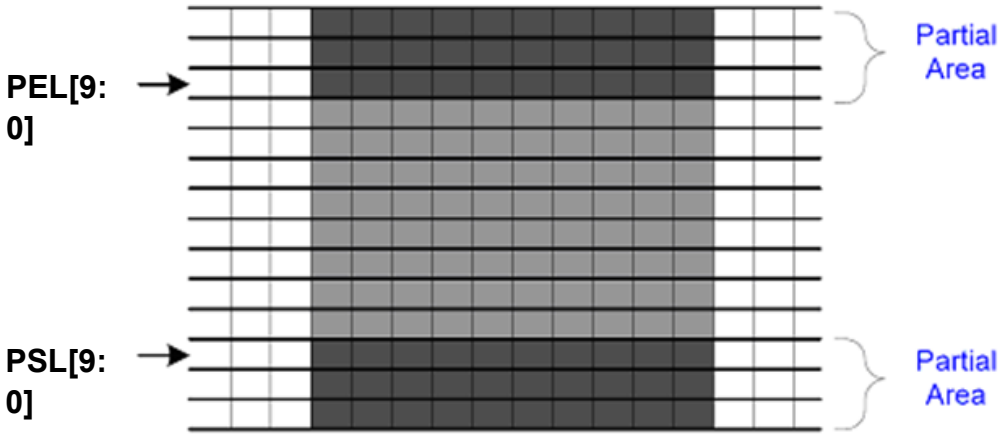
Description

This command defines the Partial Display mode's display area. There are two parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER).

If End Row > Start Row



If End Row < Start Row



If End Row = Start Row then the Partial Area will be one row deep.

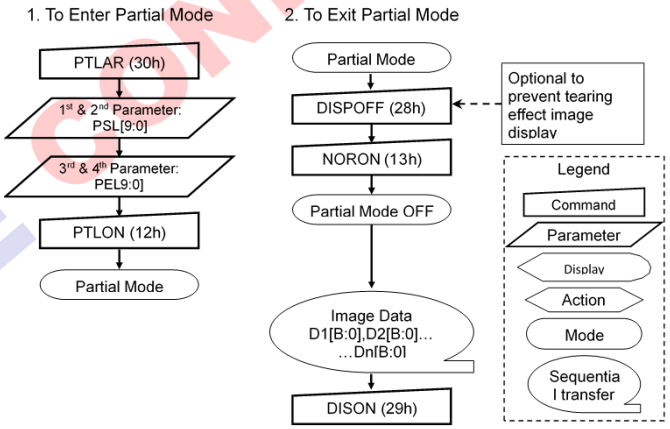
Restriction	PSL[9:0] and PEL[9:0] settings should be based on max available Display Area.
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	PSL[9:0]	PEL[9:0]
Power On Sequence	0000h	01C5h
S/W Reset	0000h	01C5h
H/W Reset	0000h	01C5h

Flow Chart



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7.5.26 PTLAR_H: Set Horizontal Partial Area (31h)

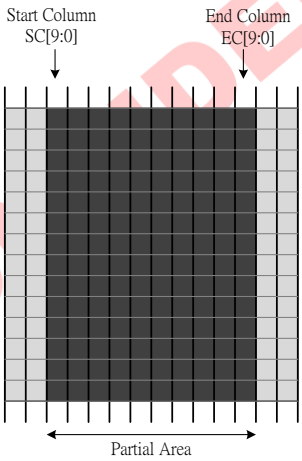
Command set		PTLAR_H								
Inst / Para	**W/R**	**D[7]**	**D[6]**	**D[5]**	**D[4]**	**D[3]**	**D[2]**	**D[1]**	**D[0]**	**Default Value**
PTLAR_H	W/R	0	0	1	1	0	0	0	1	31h
Parameter 1		-							PSC[8]	00h
Parameter 2		PSC[7:0]								00h
Parameter 3		-							PEC[8]	01h
Parameter 4		PEC[7:0]								C5h

NOTE: *"-"Don't care*

Description

This command defines the Horizontal Partial Display mode's display area. There are two parameters associated with this command, the first defines the Start Column (PSC) and the second the End Column (PEC).

If End Column > Start Column



If End Column < Start Column

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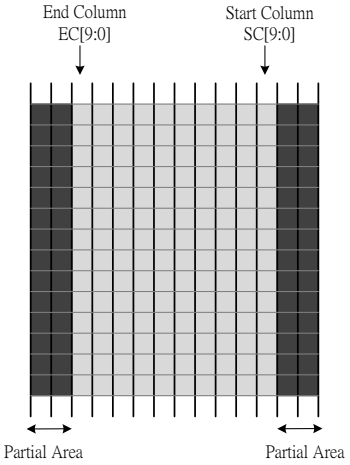


If End Column = Start Column then the Partial Area will be one column deep.

Restriction

PSL[9:0] and PEL[9:0] settings should be based on max available Display Area.

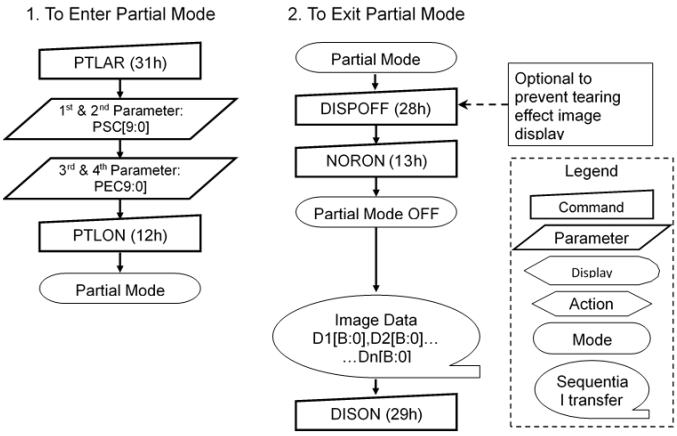
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	PSL[9:0]	PEL[9:0]
Power On Sequence	0000h	01C5h
S/W Reset	0000h	01C5h
H/W Reset	0000h	01C5h

Flow Chart



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7.5.27 TEOFF: Tearing Effect Line OFF (34h)

Command set		TEOFF								
Inst / Para	**W/R**	**D[7]**	**D[6]**	**D[5]**	**D[4]**	**D[3]**	**D[2]**	**D[1]**	**D[0]**	**Default Value**
TEOFF	W	0	0	1	1	0	1	0	0	34h
Parameter 1		No Parameter								

NOTE: *"-"Don't care*

Description

This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.

Restriction

This command has no effect when Tearing Effect output is already OFF.

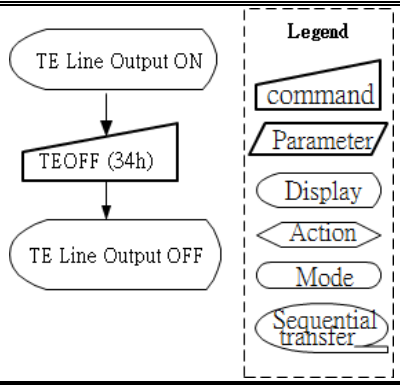
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Tearing Effect off
S/W Reset	Tearing Effect off
H/W Reset	Tearing Effect off

Flow Chart



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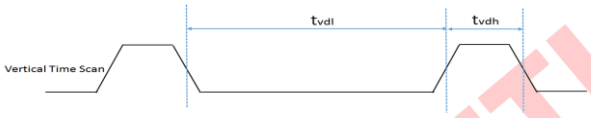
7.5.28 TEON: Tearing Effect Line ON (35h)

Command set		TEON								
Inst / Para	**W/R**	**D[7]**	**D[6]**	**D[5]**	**D[4]**	**D[3]**	**D[2]**	**D[1]**	**D[0]**	**Default Value**
TEON	W	0	0	1	1	0	1	0	1	35h
Parameter 1		-	-	-	-	-	-	-	M	00h

NOTE: *"-"Don't care*

Description	This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by changing MADCTL bit ML. The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line. When M = "0": The Tearing Effect Output line consists of V-Blanking information only.  When M = "1": The Tearing Effect Output line consists of both V-Blanking and H-Blinking information. ***Note:*** *During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.*
Restriction	This command has no effect when Tearing Effect output is already ON.
Register Availability	**Status** / **Availability** Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In: Yes
Default	**Status** / **Default Value** Power On Sequence: Tearing Effect off S/W Reset: Tearing Effect off H/W Reset: Tearing Effect off

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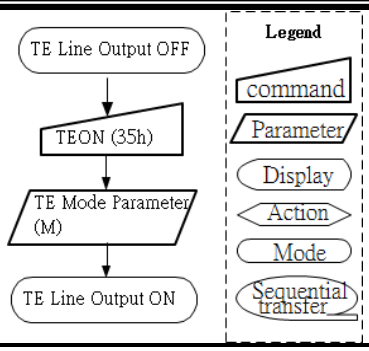
Flow Chart	

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7.5.29 MADCTL: Memory Data Access Control (36h)

Command set		MADCTL								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
MADCTL	W/R	0	0	1	1	0	1	1	0	36h
Parameter		MY	MX	-	-	RGB	-	-	-	00h

NOTE: *"-"Don't care*

Description

This command defines display direction of image.

This command makes no change on the other driver status.

- MY: Row Address Increment

Value	Description
0	Increasing in vertical
1	Decreasing in vertical

- MX: Column Address Increment

Value	Description
0	Increasing in horizontal
1	Decreasing in horizontal

- RGB: RGB/BGR Order

Value	Description
0	RGB
1	BGR

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

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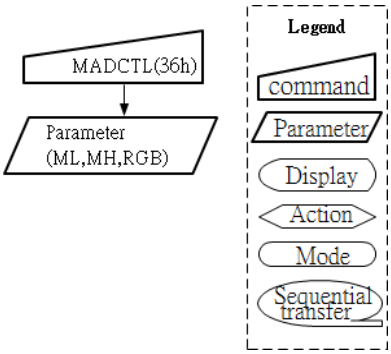
Flow Chart	

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7.5.30 IDMOFF: Idle mode OFF (38h)

Command set		IDMOFF								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
IDMOFF	W	0	0	1	1	1	0	0	0	38h
Parameter 1		No Parameter								

NOTE: *"-"Don't care*

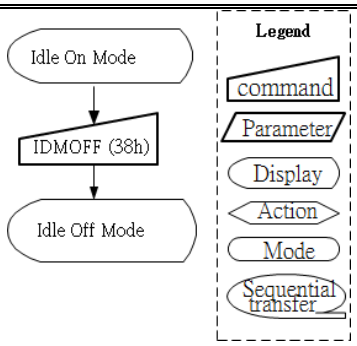
Description	This command is used to recover from Idle mode on. In the idle off mode, display panel can display maximum 16.7M colors.
Restriction	This command has no effect when module is already in Idle Off mode.
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle mode Off
S/W Reset	Idle mode Off
H/W Reset	Idle mode Off

Flow Chart



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7.5.31 IDMON: Idle mode ON (39h)

Command set		IDMON								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
IDMON	W	0	0	1	1	1	0	0	1	39h
Parameter 1		No Parameter								

NOTE: *"-"Don't care*

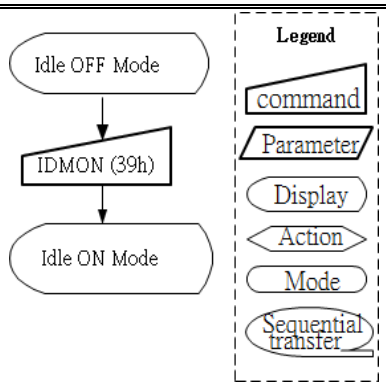
Description	This command is used to enter into Idle mode on. In the idle on mode, color expression is reduced. The display color is determined by MSB of R, G, and B.
Restriction	This command has no effect when module is already in Idle On mode.
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle mode Off
S/W Reset	Idle mode Off
H/W Reset	Idle mode Off

Flow Chart



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7.5.32 COLMOD: Interface Pixel Format (3Ah)

Command set		COLMOD								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
COLMOD	W	0	0	1	1	1	0	1	0	3Ah
Parameter 1		SPI_IFPF_SEL	VIPF[2:0]			-	IFPF[2:0]			77h

NOTE: *"-"Don't care*

Description

This command is used to define the format of RGB picture data.

The formats are shown in the table:

- SPI_IFPF_SEL:sets the pixel format for the RGB image data used by the interface.

Value	Description
0	The IFPF[2:0] pixel format used by the SPI / MCU interface
1	The VIPF[2:0] pixel format used by the SPI interface

- IFPF[2:0]:IFPF:Control Interface Color Format

Value	Description
001	SPI 8 bit/pixel (256 colors); SPI 256 Gray (Support IF: SPI3/SPI4)
010	SPI 8 bit/pixel (256 colors); SPI 3-3-2 (Support IF: SPI3/SPI4)
011	SPI 3 bit/pixel (8 colors); SPI 1-1-1 (Support IF: SPI3/SPI4)
101	16bit/pixel (65,536 colors)
110	18bit/pixel (262,144 colors)
111	24bit/pixel (16.7M colors)
001	SPI 8 bit/pixel (256 colors); SPI 256 Gray (Support IF: SPI3/SPI4)

Restriction

There is no visible effect until the Frame Memory is written to.

Register Availability

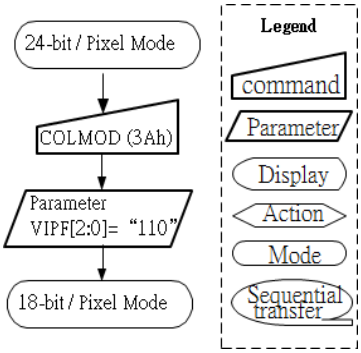
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

CHIPONE CONFIDENTIAL

Default

Status	Default Value
Power On Sequence	70h
S/W Reset	70h
H/W Reset	70h

Flow Chart



CHIPONE CONFIDENTIAL

7.5.33 RAMWR: Memory Continuous Write (3Ch)

Command set		RAMWRC								
Inst / Para	**W/R**	**D[7]**	**D[6]**	**D[5]**	**D[4]**	**D[3]**	**D[2]**	**D[1]**	**D[0]**	**Default Value**
RAMWRC	W	0	0	1	1	1	1	0	0	3Ch
Parameter 1		D_{17}	D_{16}	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	-
…		…								-
…		…								-
Parameter n		D_{N7}	D_{N6}	D_{N5}	D_{N4}	D_{N3}	D_{N2}	D_{N1}	D_{N0}	-

NOTE: *"-"Don't care*

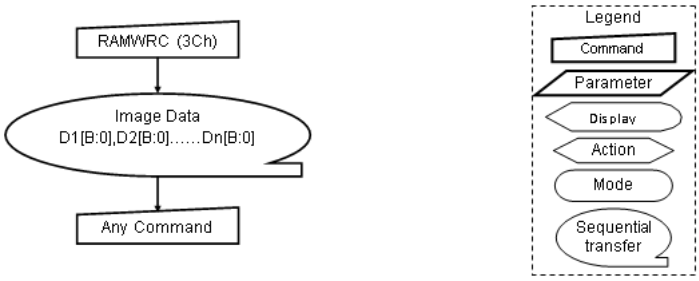
Description	This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous write_memory_continue or write_memory_start command.
Restriction	A Memory Write should follow a CASET(2Ah), RASET(2Bh) or MADCTR(36h) to define the write location. Otherwise, data written with RAMWR(2Ch) and any following RAMWRC(3Ch) commands is written to undefined locations.
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Memory is set randomly
S/W Reset	Memory is not cleared
H/W Reset	Memory is not cleared

Flow Chart



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7.5.34 RAMWR: Memory Continuous Read (3Eh)

Command set		RAMRDC								
Inst / Para	**W/R**	**D[7]**	**D[6]**	**D[5]**	**D[4]**	**D[3]**	**D[2]**	**D[1]**	**D[0]**	**Default Value**
RAMRDC	R	0	0	1	1	1	1	1	0	3Eh
Parameter 1		D_{17}	D_{16}	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	-
…		…								-
…		…								-
Parameter n		D_{N7}	D_{N6}	D_{N5}	D_{N4}	D_{N3}	D_{N2}	D_{N1}	D_{N0}	-

NOTE: *"-"Don't care*

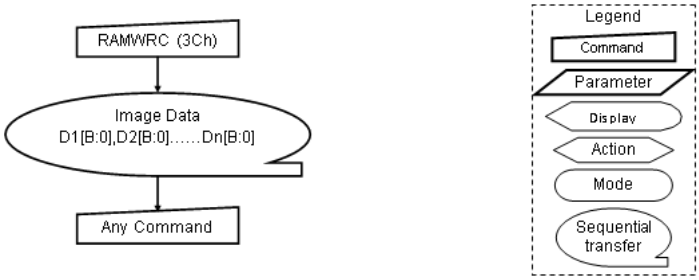
Description	This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous read_memory_continue or read_memory_start command.
Restriction	A Memory Write should follow a CASET(2Ah), RASET(2Bh) or MADCTR(36h) to define the write location. Otherwise, data written with RAMWR(2Eh) and any following RAMWRC(3Eh) commands is written to undefined locations.
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Memory is set randomly
S/W Reset	Memory is not cleared
H/W Reset	Memory is not cleared

Flow Chart



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7.5.35 STESL: Set Tearing Effect Scan Line (44h)

Command set		STESL								
Inst / Para	**W/R**	**D[7]**	**D[6]**	**D[5]**	**D[4]**	**D[3]**	**D[2]**	**D[1]**	**D[0]**	**Default Value**
STESL	W/R	0	1	0	0	0	1	0	0	44h
Parameter 1		N15	N14	N13	N12	N11	N10	N9	N8	00h
Parameter 2		N7	N6	N5	N4	N3	N2	N1	N0	00h

NOTE: *"-"Don't care*

Description	This command turns on the display module's Tearing Effect output signal on the TE signal line when the display module reaches line N. The TE signal is not affected by changing MADCTL bit ML. The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line mode. The Tearing Effect Output line consists of V-Blanking information only. ***Note 1:*** *STESL with N[15:0]="0000h" is equivalent to TEON with M="0"The Tearing Effect Output line shall be active low when the display module is in Sleep in mode.* ***Note 2:*** *This command takes effect on the frame following the current frame. Therefore, if the TE output is already on, the TE output shall continue to operate as programmed by the previous "TEON (35h)" or "STESL (44h) command" until the end of the frame.*
Restriction	Parameter range 1 ≤ N[15:0] ≤ 1280+Porch Line.
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000h
S/W Reset	0000h
H/W Reset	0000h

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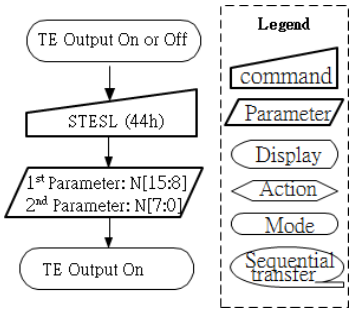
Flow Chart	

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7.5.36 GSL: Get Scan Line (45h)

Command set		GSL								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
GSL	R	0	1	0	0	0	1	0	1	45h
Parameter 1		N15	N14	N13	N12	N11	N10	N9	N8	00h
Parameter 2		N7	N6	N5	N4	N3	N2	N1	N0	00h

NOTE: *"-"Don't care*

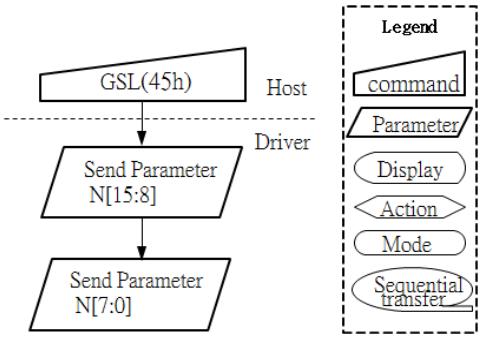
Description	This command returns the current scan line, N, used to update the display module. The total number of scan lines on display is defined as Vdisplay + Vporch. The first scan line is defined as the first line of V Sync and is denoted as Line 0. When in Sleep in mode, the returned value is undefined.
Restriction	-
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000h
S/W Reset	0000h
H/W Reset	0000h

Flow Chart



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7.5.37 DSTBON: Deep Standby Mode On (4Fh)

Command set		DSTBON								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
DSTBON	W	0	1	0	0	1	1	0	0	4Fh
Parameter 1		-	-	-	-	-	-	-	DSTB	00h

NOTE: *"-"Don't care*

Description

This command is used to enter deep standby mode.

DSTB="1", enter deep standby mode.

Notes:

1. To exit Deep Standby Mode, input low pulse more than 3 msec to pin RESX.
2. For MIPI IF, if deep standby mode is used, please pull HSSI_CLK_P/N & HSSI_D0~D1_P/N to GND after executing deep standby command.

Restriction

-

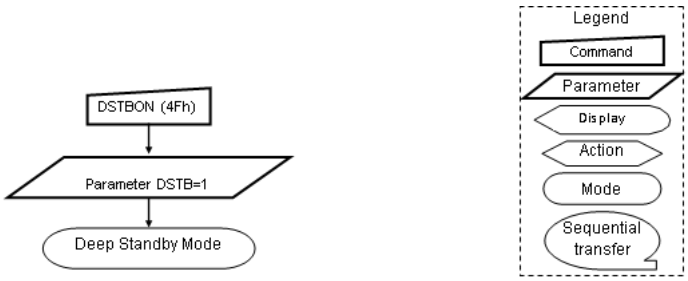
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



CHIPONE CONFIDENTIAL

7.5.38 WRDISBV: Write Display Brightness (51h)

Command set		WRDISBV								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
WRDISBV	W	0	1	0	1	0	0	0	1	51h
Parameter 1		DBV[7:0]								00h

NOTE: *"-"Don't care*

Description

This command is used to adjust brightness value.

In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.

BV[7:0]	Brightness (Ratio)	Brightness (%)
00h	0/256	0 %
01h	2/256	0.78 %
……	……	……
FEh	255/256	99.6%
FFh	256/256	100%

Restriction

The display supplier cannot use this command for tuning (e.g. factory tuning, etc.).

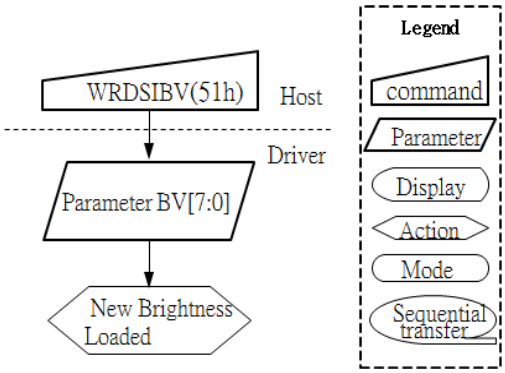
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



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7.5.39 RDDISBV: Read Display Brightness (52h)

Command set		RDDISBV								
Inst / Para	**W/R**	**D[7]**	**D[6]**	**D[5]**	**D[4]**	**D[3]**	**D[2]**	**D[1]**	**D[0]**	**Default Value**
RDDISBV	R	0	1	0	1	0	0	1	0	52h
Parameter 1		DBV[7:0]								00h

NOTE: *"-"Don't care*

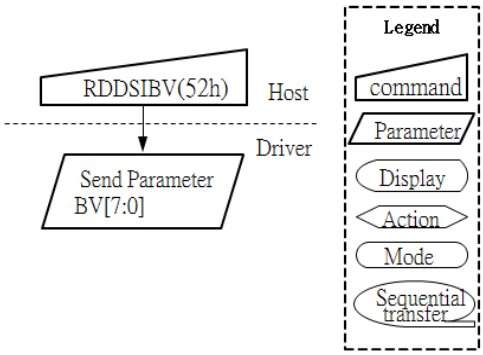
Description	This command returns brightness value. In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.
Restriction	-
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



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7.5.40 WRCTRLD: Write CTRL Display (53h)

Command set		WRCTRLD								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
WRCTRLD	W	0	1	0	1	0	0	1	1	53h
Parameter 1		-	-	BCTRL	-	DD	-	-	-	28h

NOTE: *"-"Don't care*

Description	This command is used to control display brightness. BCTRL: Brightness Control Block On/Off. The BCTRL bit is always used to switch brightness for display with dimming effect (according to DIM_EN bit). BCTRL =0, dBV[7:0] value disable. BCTRL =1,d BV[7:0] value enable. DD: Display Dimming Control On/Off. DD = 0, Display dimming is off. DD =1, Display dimming is on. The dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD ="1", e.g. BCTRL: 0_1 or 1_0. *Note: All read and write commands are valid, but there is no effect (except registers can be changed) when write commands are used.*
Restriction	-
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

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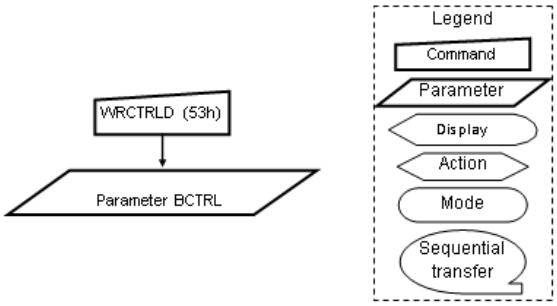
Flow Chart	

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7.5.41 RDCTRLD: Read CTRL Display (54h)

Command set		RDCTRLD								
Inst / Para	**W/R**	**D[7]**	**D[6]**	**D[5]**	**D[4]**	**D[3]**	**D[2]**	**D[1]**	**D[0]**	**Default Value**
RDCTRLD	R	0	1	0	1	0	1	0	0	54h
Parameter 1		-	-	BCTRL	-	DD	BL	-	-	28h

NOTE: *"-"Don't care*

Description	This command is used to control display brightness. BCTRL: Brightness Control Block On/Off. The BCTRL bit is always used to switch brightness for display with dimming effect (according to DIM_EN bit). BCTRL =0, dBV[7:0] value disable. BCTRL =1,d BV[7:0] value enable. DD: Display Dimming Control On/Off. DD = 0, Display dimming is off. DD =1, Display dimming is on. The dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD ="1", e.g. BCTRL: 0_1 or 1_0. *Note: All read and write commands are valid, but there is no effect (except registers can be changed) when write commands are used.*
Restriction	-
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

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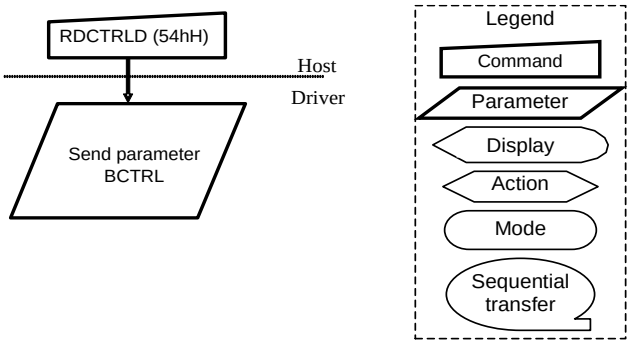
Flow Chart	

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7.5.42 WRACL: Read ACL Control (55h)

Command set		WRACL								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
WRACL	W	0	1	0	1	0	1	0	1	55h
Parameter 1		-	-	-	-	-	-	RAD_ACL[1:0]		00h

NOTE: *"-"Don't care*

Description

This command is used to control ACL (Auto Current Limit) function

- ACL[1:0]: control ACL (Auto Current Limit) function.

Value	Description
00	Disable ACL function.
11	Enable ACL function.

Restriction

-

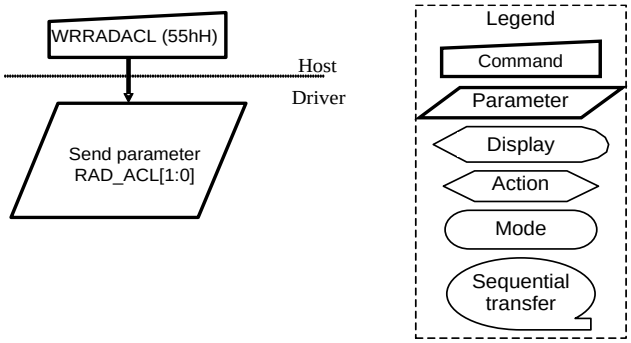
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



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7.5.43 RDACL: Read ACL Control (56h)

Command set		RDACL								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
RDACL	R	0	1	0	1	0	1	1	0	56h
Parameter 1		-	-	-	-	-	-	RAD_ACL[1:0]		00h

NOTE: *"-"Don't care*

Description

This command is used to control ACL (Auto Current Limit) function

- ACL[1:0]: control ACL (Auto Current Limit) function.

Value	Description
00	Disable ACL function.
11	Enable ACL function.

Restriction

-

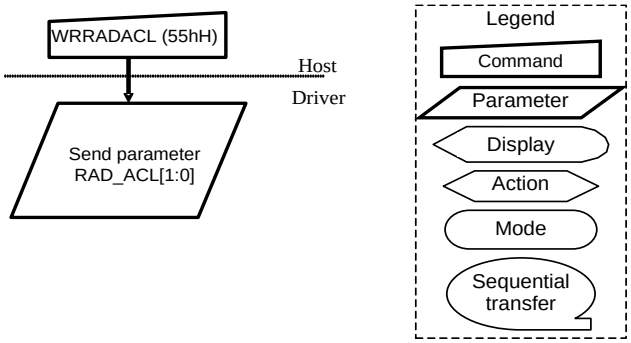
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



CHIPONE CONFIDENTIAL

7.5.44 WRIMGEHCCTR: Set Color Enhance Control (58h)

Command set		SRIMGEHCCTR								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
WRIMGEHCCTR	W	0	1	0	1	1	0	0	0	58h
Parameter 1		-	-	-	-	-	SLR_EN	SLR_LEVEL[1:0]		00h

NOTE: *"-"Don't care*

Description

This command is used to control ACL (Auto Current Limit) function

- SLR_EN: Sunlight Readable Enhancement enable function.

Value	Description
0	Disable SRE function.
1	Enable SRE function.

- SLR_LEVEL[1:0]: Sunlight Readable Enhancement Enable

Value	Description
0	Low
1	Medium
2	High

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

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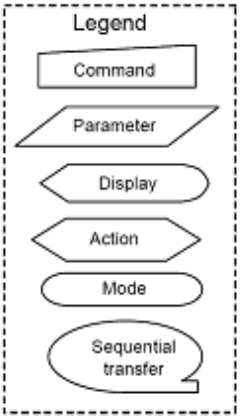
Flow Chart	

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7.5.45 RDIMGEHCCTR: Read Color Enhance Control (59h)

Command set		RDIMGEHCCTR								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
RDIMGEHCCTR	R	0	1	0	1	1	0	0	1	59h
Parameter 1		-	-	-	-	-	SLR_EN	SLR_LEVEL[1:0]		00h

NOTE: *"-"Don't care*

Description

This command is used to control ACL (Auto Current Limit) function

- SLR_EN: Read Sunlight Readable Enhancement enable function.

Value	Description
0	Disable SRE function.
1	Enable SRE function.

- SLR_LEVEL[1:0]: Read Sunlight Readable Enhancement level

Value	Description
0	Low
1	Medium
2	High

Restriction

-

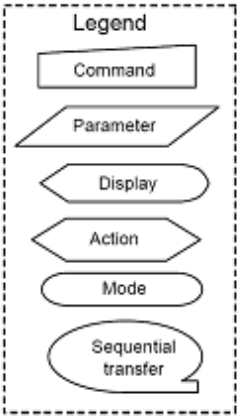
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

CHIPONE CONFIDENTIAL

Flow Chart	

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7.5.46 RDIMGEHCCTR: Local HBM Control (5Fh)

Command set		RDIMGEHCCTR								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
RDIMGEHCCTR	R/W	0	1	0	1	1	1	1	1	5Fh
Parameter 1		-	-	-	-	-	-	-	Loacl_hbm_en	00h

NOTE: *"-"Don't care*

Description

This command is used to control Local hbm function

- Loacl hbm: Loacl hbm enable function.

Value	Description
0	Disable Loacl hbm function.
1	Enable Local hbm function.

Restriction

-

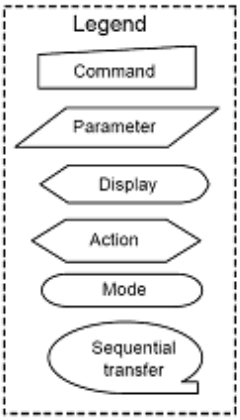
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



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7.5.47 WRHBMDISBV: Frame Rate level Control (60h)

Command set		RDIMGEHCCTR								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
RDIMGEHCCTR	R/W	0	1	1	0	0	0	0	0	60h
Parameter 1		-	normal_level[2:0]			-	-	idle_level[1:0]		00h

NOTE: *"-"Don't care*

Description

This command is used to control Frame Rate level function

Value	Description
Normal_level[2:0]	0: Normal mode base level 1: Normal mode level 1 2: Normal mode level 2 3: Normal mode level 3 4: Normal mode level 4 Others: Reserved
Idle_level[1:0]	0: IDLE mode base level 1: IDLE mode level 1 2: IDLE mode level 2 Others: Reserved

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

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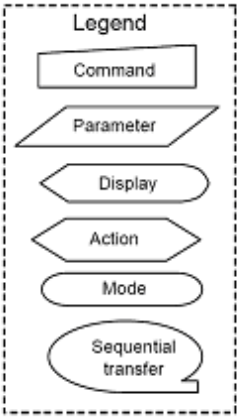
Flow Chart	

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7.5.48 WRHBMDISBV: Dynamic Frame Rate Enable (61h)

Command set		WRHBMDISBV								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
WRHBMDISBV	W	0	1	1	0	0	0	0	1	61h
Parameter 1		-	-	-	-	-	-	dynf_en_B	dynf_en_A	00h

NOTE: *"-"Don't care*

Description

This command is used to enable dynamic Frame Rate function

Value	Description
dynf_en_A	1: Enable dynamic frame rate switching between pre-configured level in normal mode 0: Disable dynamic frame rate function in normal mode
dynf_en_B	1: Enable dynamic frame rate switching between pre-configured level in IDLE mode 0: Disable dynamic frame rate function in IDLE mode

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

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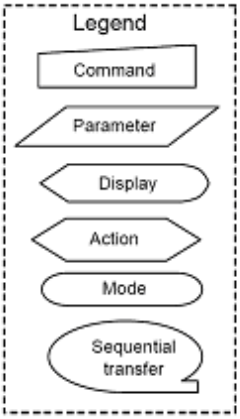
Flow Chart	

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7.5.49 WRHBMDISBV: Write HBM Display Brightness (63h)

Command set		WRHBMDISBV								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
WRHBMDISBV	W	0	1	1	0	0	0	1	1	63h
Parameter 1		DBV_HBM[7:0]								00h

NOTE: *"-"Don't care*

Description	This command is used to adjust HBM mode brightness value. In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.

BV[7:0]	Brightness (Ratio)	Brightness (%)
00h	0/256	0 %
01h	2/256	0.78 %
……	……	……
FEh	255/256	99.6%
FFh	256/256	100%

Restriction	-
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

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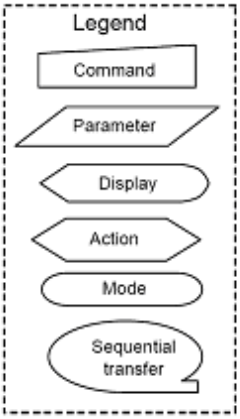
Flow Chart	

7.5.50 WRDISBV: Read HBM Display Brightness (64h)

Command set		RDCABC								
Inst / Para	**W/R**	**D[7]**	**D[6]**	**D[5]**	**D[4]**	**D[3]**	**D[2]**	**D[1]**	**D[0]**	**Default Value**
RDCABC	R	0	1	1	0	0	1	0	0	64h
Parameter 1		DBV_HBM[7:0]								00h

NOTE: *"-"Don't care*

Description	This command is used to read HBM mode brightness value. In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness. BV[7:0] / Brightness (Ratio) / Brightness (%) 00h / 0/256 / 0 % 01h / 2/256 / 0.78 % …… / …… / …… FEh / 255/256 / 99.6% FFh / 256/256 / 100%
Restriction	-
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out / Yes Normal Mode On, Idle Mode On, Sleep Out / Yes Partial Mode On, Idle Mode Off, Sleep Out / Yes Partial Mode On, Idle Mode On, Sleep Out / Yes Sleep In / Yes

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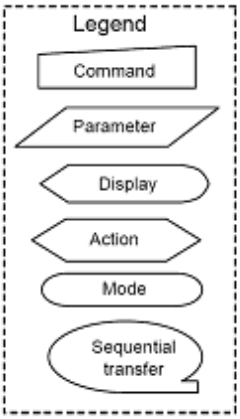
Default	

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



7.5.51 RDHBMDISBV: Read HBM Display Brightness (65h)

Command set		RDHBMDISBV								
Inst / Para	**W/R**	**D[7]**	**D[6]**	**D[5]**	**D[4]**	**D[3]**	**D[2]**	**D[1]**	**D[0]**	**Default Value**
RDHBMDISBV	R	0	1	1	0	0	1	0	1	66h
Parameter 1		DBV_HBM[7:0]								00h

NOTE: *"-"Don't care*

Description

This command is used to read HBM mode brightness value.

In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.

BV[7:0]	Brightness (Ratio)	Brightness (%)
00h	0/256	0 %
01h	2/256	0.78 %
……	……	……
FEh	255/256	99.6%
FFh	256/256	100%

Restriction -

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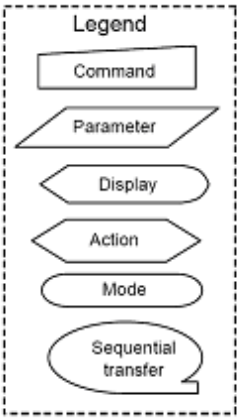
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



7.5.52 HBM Mode: Set HBM Mode (66h)

Command set		HBM Enable								
Inst / Para	**W/R**	**D[7]**	**D[6]**	**D[5]**	**D[4]**	**D[3]**	**D[2]**	**D[1]**	**D[0]**	**Default Value**
HBMEN	W	0	1	1	0	0	1	1	0	66h
Parameter 1		-	-	-	-	-	-	HBM_EN	-	00h

NOTE: *"-"Don't care*

Description

This command is used to read HBM mode eanble.

ps. This command causes the display module to enter/exit HBM mode (enter/exit normal, and idle mode)

- HBM_EN: HBM enable function.

Value	Description
0	Disable HBM mode function.
1	Enable HBM mode function.

Restriction

-

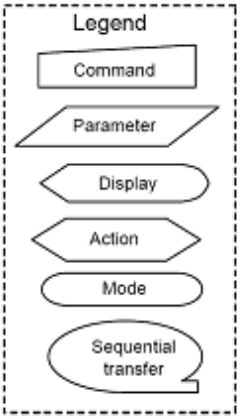
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



7.5.53 COLSET: Interface Pixel Format Set (70~7Fh)

Command set		Pixel Format Set								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
70h	W/R	0	1	1	1	0	0	0	0	70h
Parameter 1		R_0000[7:0]								00h
Parameter 2		G_0000[7:0]								00h
Parameter 3		B_0000[7:0]								00h
71h		0	1	1	1	0	0	0	1	71h
Parameter 1		R_0001[7:0]								00h
Parameter 2		G_0001[7:0]								00h
Parameter 3		B_0001[7:0]								FFh
72h		0	1	1	1	0	0	1	0	72h

Parameter 1		R_0010[7:0]								00h
Parameter 2		G_0010[7:0]								FFh
Parameter 3		B_0010[7:0]								00h
73h		0	1	1	1	0	0	1	1	73h
Parameter 1		R_0011[7:0]								00h
Parameter 2		G_0011[7:0]								FF
Parameter 3		B_0011[7:0]								FF
74h		0	1	1	1	0	1	0	0	74h
Parameter 1		R_0100[7:0]								FFh
Parameter 2		G_0100[7:0]								00h
Parameter 3		B_0100[7:0]								00h
75h		0	1	1	1	0	1	0	1	75h
Parameter 1		R_0101[7:0]								FFh
Parameter 2		G_0101[7:0]								00h
Parameter 3		B_0101[7:0]								FFh
76h		0	1	1	1	0	1	1	0	76h
Parameter 1		R_0110[7:0]								FFh
Parameter 2		G_0110[7:0]								FFh
Parameter 3		B_0110[7:0]								00h
77h		0	1	1	1	0	1	1	1	77h
Parameter 1		R_0111[7:0]								FFh
Parameter 2		G_0111[7:0]								FFh
Parameter 3		B_0111[7:0]								FF
78h		0	1	1	1	1	0	0	0	78h
Parameter 1		R_1000[7:0]								00h
Parameter 2	W/R	G_1000[7:0]								00h
Parameter 3		B_1000[7:0]								00h
79h		0	1	1	1	1	0	0	1	79h
Parameter 1		R_1001[7:0]								00h
Parameter 2		G_1001[7:0]								00h
Parameter 3		B_1001[7:0]								FFh
7Ah		0	1	1	1	1	0	1	0	7Ah

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Parameter 1		R_1010[7:0]								00h
Parameter 2		G_1010[7:0]								FFh
Parameter 3		B_1010[7:0]								00h
7Bh		0	1	1	1	1	0	1	1	7Bh
Parameter 1		R_1011[7:0]								00h
Parameter 2		G_1011[7:0]								FFh
Parameter 3		B_1011[7:0]								FFh
7Ch		0	1	1	1	1	1	0	0	7Ch
Parameter 1		R_1100[7:0]								FFh
Parameter 2		G_1100[7:0]								00h
Parameter 3		B_1100[7:0]								00h
7Dh		0	1	1	1	1	1	0	1	7Dh
Parameter 1		R_1101[7:0]								FFh
Parameter 2		G_1101[7:0]								00h
Parameter 3		B_1101[7:0]								FFh
7Eh		0	1	1	1	1	1	1	0	7Eh
Parameter 1		R_1110[7:0]								FFh
Parameter 2		G_1110[7:0]								FFh
Parameter 3		B_1110[7:0]								00h
7Fh		0	1	1	1	1	1	1	1	7Fh
Parameter 1	W/R	R_1111[7:0]								FFh
Parameter 2		G_1111[7:0]								FFh
Parameter 3		B_1111[7:0]								FFh

NOTE: *"-"Don't care*

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Description

This command set the SPI 1-1-1 color format map directly to 24 bits by CMD 7000h-7F00h

RGB 1-1-1 Color Format Mapping	R [7:0]	G [7:0]	B [7:0]
0000 (70h)	R_0000[7:0]	G_0000[7:0]	B_0000[7:0]
0001 (71h)	R_0001[7:0]	G_0001 [7:0]	B_0001[7:0]
0010 (72h)	R_0010[7:0]	G_0010[7:0]	B_0010[7:0]
0011 (73h)	R_0011[7:0]	G_0011[7:0]	B_0011[7:0]
0100 (74h)	.	.	.
0101 (75h)	.	.	.
0110 (76h)	.	.	.
0111 (77h)	.	.	.
1000 (78h)	R_1000[7:0]	G_1000[7:0]	B_1000[7:0]
1001 (79h)	.	.	.
1010 (7Ah)	.	.	.
1011 (7Bh)	.	.	.
1100 (7Ch)	R_1100[7:0]	G_1100[7:0]	B_1100[7:0]
1101 (7Dh)	R_1101[7:0]	G_1101[7:0]	B_1101[7:0]
1110 (7Eh)	R_1110[7:0]	G_1110[7:0]	B_1110[7:0]
1111 (7Fh)	R_1111[7:0]	G_1111[7:0]	B_1111[7:0]

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value				
	70h	71h	…	7Eh	7Fh
Power On Sequence	Refer to above table				
S/W Reset	Refer to above table				
H/W Reset	Refer to above table				

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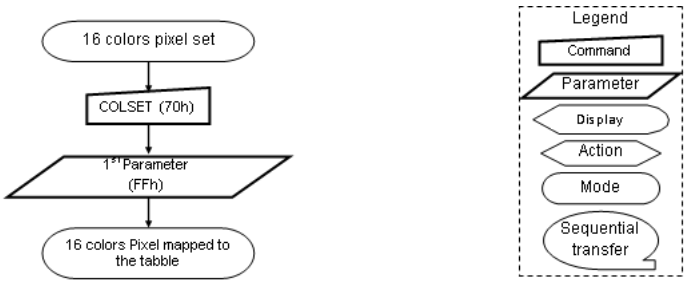
Flow Chart	

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7.5.54 COLOPT: Interface Pixel Format Option (80h)

Command set		COLOPT								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
COLOPT	W	1	0	0	0	0	0	0	0	80h
Parameter 1		-	-	RGB111 _opt	-	-	RGB4bit _en	gray256 _color[2]	gray256 _color[1]	07h

NOTE: *"-"Don't care*

Description

This command sets the 1-1-1/256 gray color format option used by SPI interface.

RGB111_opt = 0:

Supporting in IFPF[2:0]=011 case setting by 3A00h (interface pixel format is SPI 1-1-1).

RGB111	DCX	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
CMD WR (0x2C)	0	0	0	1	0	1	1	0	0
1st RAM Data Write(1,2 pixel)	1	x	x	R1[0]	G1[0]	B1[0]	R2[0]	G2[0]	B2[0]
2st RAM Data Write(3,4 pixel)	1	x	x	R3[0]	G3[0]	B3[0]	R4[0]	G4[0]	B5[0]
3st RAM Data Write(5,6 pixel)	1	x	x	R5[0]	G5[0]	B5[0]	R6[0]	G6[0]	B6[0]
……	…	x	x	…	…	…	…	…	…
nst RAM Data Write(n-1,n pixel)	1	x	x	Rn-1[0]	Gn-1[0]	Bn-1[0]	Rn[0]	Gn[0]	Bn[0]

RGB111_opt = 1:

Supporting in IFPF[2:0]=011 case setting by 3A00h (interface pixel format is SPI 1-1-1).

RGB111	DCX	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
CMD WR (0x2C)	0	0	0	1	0	1	1	0	0
1st RAM Data Write(1,2 pixel)	1	x	R1[0]	G1[0]	B1[0]	x	R2[0]	G2[0]	B2[0]
2st RAM Data Write(3,4 pixel)	1	x	R3[0]	G3[0]	B3[0]	x	R4[0]	G4[0]	B5[0]
3st RAM Data Write(5,6 pixel)	1	x	R5[0]	G5[0]	B5[0]	x	R6[0]	G6[0]	B6[0]
……	…	x	…	…	…		…	…	.
nst RAM Data Write(n-1,n pixel)	1	x	Rn-1[0]	Gn-1[0]	Bn-1[0]	x	Rn[0]	Gn[0]	Bn[0]

- RGB4bit_en:control the RGB111 bit number

Value	Description
1	RGB 1-1-1-1
0	RGB 1-1-1

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RGB4bit_en = 0:

Supporting in IFPF[2:0]=011 case setting by 3A00h (interface pixel format is SPI 1-1-1).

Three bits per pixel formats map directly to 24bits by CMD 7000h-7700h

RGB111	DCX	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
CMD WR (0x2C)	0	0	0	1	0	1	1	0	0
1st RAM Data Write(1,2 pixel)	1	x	x	P1[2]	P1[1]	P1[0]	P2[2]	P2[1]	P2[0]
2st RAM Data Write(3,4 pixel)	1	x	x	P3[2]	P3[1]	P3[0]	P4[2]	P4[1]	P5[0]
3st RAM Data Write(5,6 pixel)	1	x	x	P5[2]	P5[1]	P5[0]	P6[2]	P6[1]	P6[0]
……	…	x	x	…	…	…	…	…	…
nst RAM Data Write(n-1,n pixel)	1	x	x	Pn-1[2]	Pn-1[1]	Pn-1[0]	Pn[2]	Pn[1]	Pn[0]

Example:

P1[2:0] = 3'b101 = { R_0101[7:0], G_0101[7:0], B_0101[7:0] } by CMD1: 7500h-7502h

RGB4bit_en = 1:

Supporting in IFPF[2:0]=011 case setting by 3A00h (interface pixel format is SPI 1-1-1).

Four bits per pixel formats map directly to 24bits by CMD1: 7000h-7F00h

RGB111	DCX	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
CMD WR (0x2C)	0	0	0	1	0	1	1	0	0
1st RAM Data Write(1,2 pixel)	1	P1[3]	P1[2]	P1[1]	P1[0]	P2[3]	P2[2]	P2[1]	P2[0]
2st RAM Data Write(3,4 pixel)	1	P3[3]	P3[2]	P3[1]	P3[0]	P4[3]	P4[2]	P4[1]	P5[0]
3st RAM Data Write(5,6 pixel)	1	P5[3]	P5[2]	P5[1]	P5[0]	P6[3]	P6[2]	P6[1]	P6[0]
……	…	…	…	…	…	…	…	…	…
nst RAM Data Write(n-1,n pixel)	1	Pn-1[3]	Pn-1[2]	Pn-1[1]	Pn-1[0]	Pn[3]	Pn[2]	Pn[1]	Pn[0]

Example:

P1[3:0] = 4'b1101 = { R_1101[7:0], G_1101[7:0], B_1101[7:0] } by CMD1: 7D00h-7D02h

- gray256_color[2:0]:256gray color format

Supporting in IFPF[2:0]=001 case setting by 3A00h (interface pixel format is SPI 256 Gray).

Value	Description
000	{8'h0, 8'h0, 8'h0}
001	{8'h0, 8'h0,gray[7:0]}
010	{8'h0,gray[7:0], 8'h0}
011	{8'h0,gray[7:0],gray[7:0]}
100	{gray[7:0],8'h0,8'h0}
101	{gray[7:0],8'h0,gray[7:0]}
110	{gray[7:0],gray[7:0],8'h0}
111	{gray[7:0],gray[7:0],gray[7:0]}

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This command sets the valid red, green and blue 256 grayscale

gray256_color[2:0]	Red Grayscale	Green Grayscale	Blue Grayscale
000	00000000	00000000	00000000
001	00000000	00000000	P [7:0]
010	00000000	P [7:0]	00000000
011	00000000	P [7:0]	P [7:0]
100	P [7:0]	00000000	00000000
101	P [7:0]	00000000	P [7:0]
110	P [7:0]	P [7:0]	00000000
111	P [7:0]	P [7:0]	P [7:0]

Restriction

-

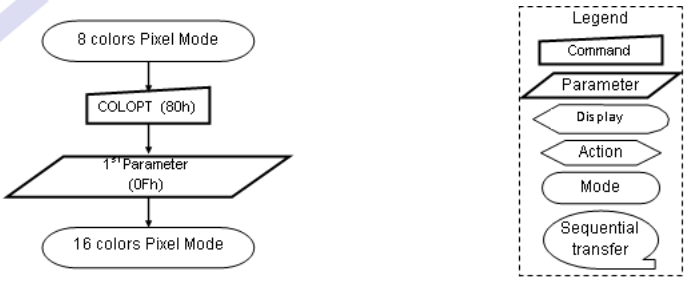
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	07h
S/W Reset	07h
H/W Reset	07h

Flow Chart



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7.5.55 RDDDBS: Read DDB Start (A1h)

Command set		RDDDBS								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
RDDDBS	R	1	0	1	0	0	0	0	0	A1h
Parameter 1		SID[7:0]								33h
Parameter 2		SID[7:0]								11h
Parameter 3		MID[7:0]								00h
Parameter 4		MID[15:8]								00h
Parameter 5		1	1	1	1	1	1	1	1	FFh

NOTE: *"-"Don't care*

Description

This command returns the supplier identification and display module mode/revision information

- SID [7:0]:SID: Driver ID code
- MID[7:0]:MID: Module ID

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	w/ MTP	w/o MTP
Power On Sequence	MTP Value	33h, 11h, 00h, 00h, FFh
S/W Reset	MTP Value	33h, 11h, 00h, 00h, FFh
H/W Reset	MTP Value	33h, 11h, 00h, 00h, FFh

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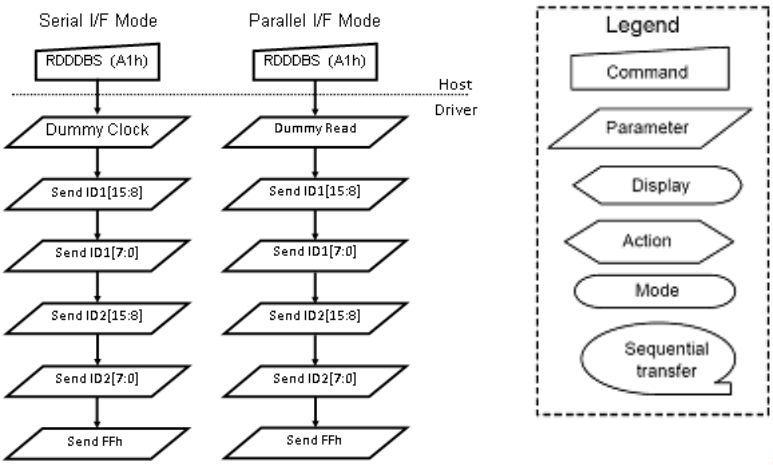
Flow Chart	

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7.5.56 RDDDBC: Read DDB Continuous (A8h)

Command set		RDDDBC								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
RDDDBC	R	1	0	1	0	1	0	0	0	A8h
Parameter 1		SID[7:0]								33h
Parameter 2		SID[7:0]								10h
Parameter 3		MID[7:0]								00h
Parameter 4		MID[15:8]								00h
Parameter 5		1	1	1	1	1	1	1	1	FFh

NOTE: *"-"Don't care*

Description

This command returns the supplier identification and display module mode/revision information from the point where RDDDBS command was interrupted by another command.

- SID [7:0]:SID: Driver ID code

- MID[7:0]:MID: Module ID

Note: Parameter 0xFF is an "Exit Code", this means that there is no more data in the DDB block.

Note: For use example,

1. Set maximum return packet size=3
2. Read 0xA1, return 3 bytes SID[7:0], SID[15:8], MID[7:0]
3. Read 0xA8, return 2 bytes MID[15:8],RID[7:0], RID[15:8] and 0xFF

Restriction

Read DDB Start command (RDDDBS) should be executed at least once before a Read DDB Continue command (RDDDBC) to define the read location. Otherwise, data read with a Read DDB Continue command is undefined.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	w/ MTP	w/o MTP
Power On Sequence	MTP Value	33h, 11h, 00h, 00h, FFh
S/W Reset	MTP Value	33h, 11h, 00h, 00h, FFh
H/W Reset	MTP Value	33h, 11h, 00h, 00h, FFh

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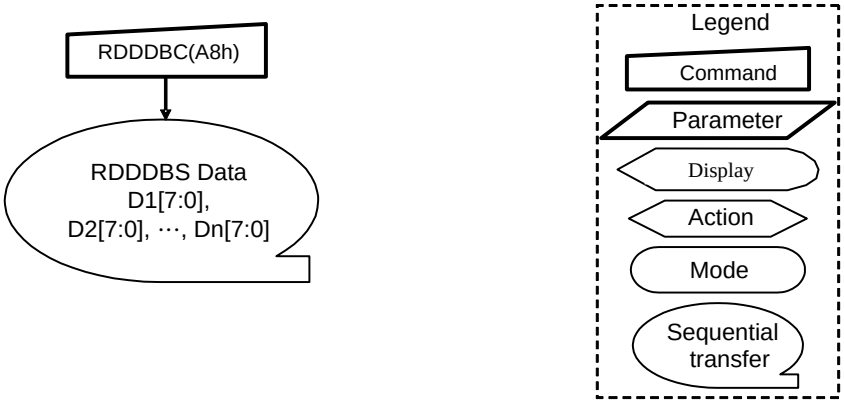
Flow Chart	

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7.5.57 RDFCS: Read First Checksum (AAh)

Command set		RDFCS								
Inst / Para	**W/R**	**D[7]**	**D[6]**	**D[5]**	**D[4]**	**D[3]**	**D[2]**	**D[1]**	**D[0]**	**Default Value**
RDFCS	R	1	0	1	0	1	1	0	0	AAh
Parameter 1		FCS[7:0]								00h

NOTE: *"-"Don't care*

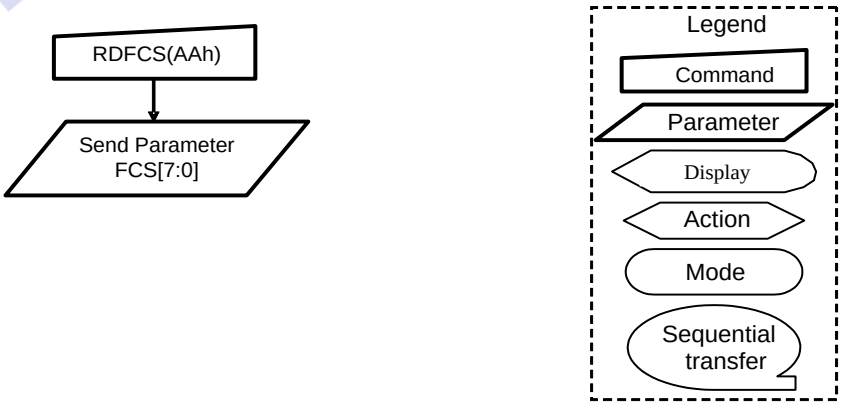
Description	This command returns the first checksum what has been calculated from "User Command Set" area registers (not include "Manufacture Command Set) and the frame memory after the write access to those registers and/or frame memory has been done.
Restriction	It will be necessary to wait 150ms after there is the last write access on "User Command Set" area registers before there can read this checksum value.
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



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7.5.58 RDCCS: Read Continuous Checksum (AFh)

Command set		RDCCS								
Inst / Para	**W/R**	**D[7]**	**D[6]**	**D[5]**	**D[4]**	**D[3]**	**D[2]**	**D[1]**	**D[0]**	**Default Value**
RDCCS	R	1	0	1	0	1	1	1	1	AFh
Parameter 1		CCS[7:0]								00h

NOTE: *"-"Don't care*

Description

This command returns the continue checksum what has been calculated continuously after the first checksum has calculated from "User Command Set" area registers and the frame memory after the write access to those registers and/or frame memory has been done.

Restriction

It will be necessary to wait 300ms after there is the last write access on "User Command Set" area registers before there can read this checksum value in the first time.

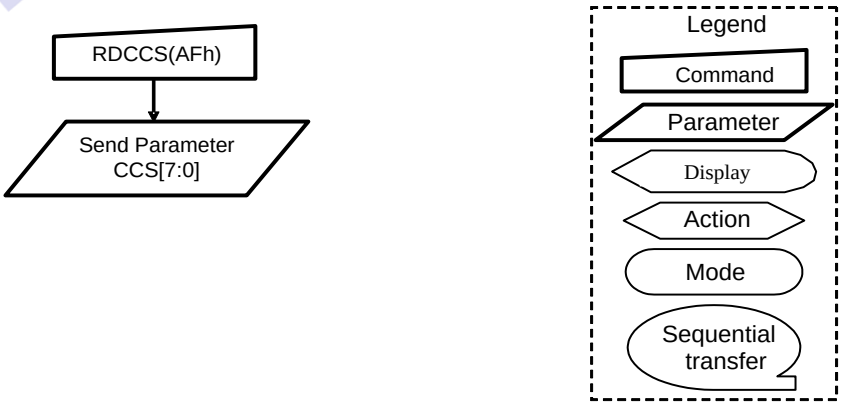
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



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7.5.59 SetDISPMode: Set Display Mode (C2h)

Command set		RDCCS								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
RDCCS	W	1	1	0	0	0	0	1	0	C2h
Parameter 1						RM_B		DM[1:0]		00h

NOTE: *"-"Don't care*

Description

- RM [1:0]: Display RAM selection

Value	Description
0	Via RAM
1	Bypass RAM

- DM [1:0]: Display timing mode selection

Value	Description
00	internal timing
01	reserved
10	reserved
11	external timing(VSYNC + HSYNC align mode)

Restriction

Note: If video mode, need to set DM[1:0] = 2'b11.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

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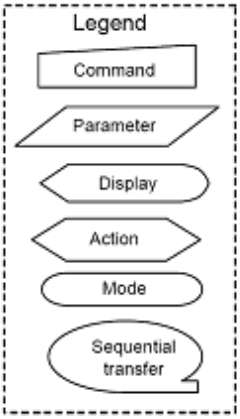
Flow Chart	

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7.5.60 SetDSPIMode:Set Dual SPI Mode (C4h)

Command set		RDCCS								
Inst / Para	**W/R**	**D[7]**	**D[6]**	**D[5]**	**D[4]**	**D[3]**	**D[2]**	**D[1]**	**D[0]**	**Default Value**
RDCCS	W/R	1	1	0	0	0	1	0	0	C4h
Parameter 1		SPI_WRAM	0	DSPI_CFG [1:0]		0	0	Dual_single_DCX	DSPI_EN	00h

NOTE: *"-"Don't care*

Description

- SPI_WRAM_cmd1: SPI write SRAM control

Value	Description
1	SPI write SRAM enable
0	SPI write SRAM disable

- Dual_CFG [1:0]: DUAL_SPI transmission format

Value	Description
00	Single wire
01	1P2T (only for RGB666)
10	1P1T
11	2P3T

- Dual_single_DCX: DUAL_SPI DCX control

Value	Description
1	DUAL_SPI single DCX enable
0	DUAL_SPI single DCX disable

- SPI_WRAM_cmd1: SPI write sram control

Value	Description
1	DUAL_SPI enable
0	DUAL_SPI disable

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes

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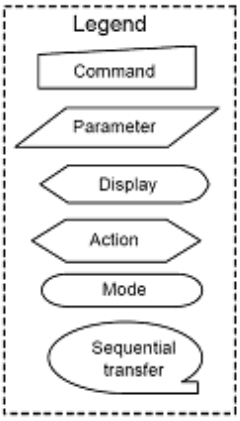
	Sleep In: Yes
Default	

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



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7.5.61 RDID1: Read ID1 Value (DAh)

Command set		RDID1								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
RDID1	R	1	1	0	1	1	0	1	0	DAh
Parameter 1		ID1 [7:0]								33h

NOTE: *"-"Don't care*

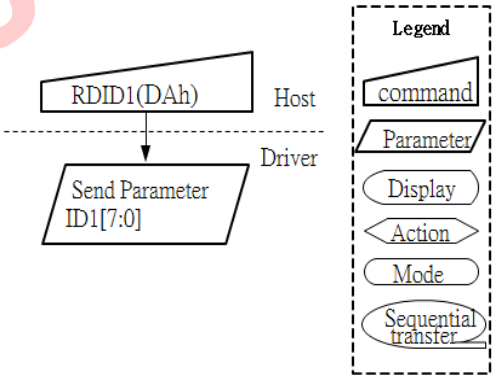
Description	This read byte identifies the OLED LCD module's manufacture ID.
Restriction	-
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	33h
S/W Reset	33h
H/W Reset	33h

Flow Chart



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7.5.62 RDID2: Read ID2 Value (DBh)

Command set		RDID2								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
RDID2	R	1	1	0	1	1	0	1	1	DBh
Parameter 1		ID2 [7:0]								11h

NOTE: *"-"Don't care*

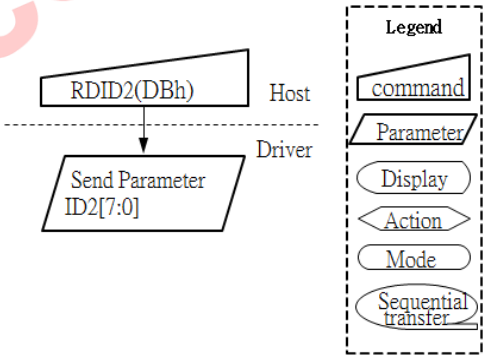
Description	This read byte identifies the OLED LCD module's manufacture ID.
Restriction	-
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	11h
S/W Reset	11h
H/W Reset	11h

Flow Chart



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7.5.63 RDID3: Read ID3 Value (DCh)

Command set		RDID3								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
RDID3	R	1	1	0	1	1	1	0	0	DCh
Parameter 1		ID3 [7:0]								00h

NOTE: *"-"Don't care.*

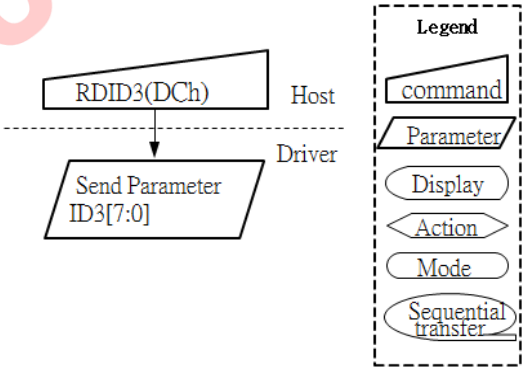
Description	This read byte identifies the OLED LCD module's manufacture ID.
Restriction	-
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



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7.5.64 CMD Page Switch (FEh)

Command set		MCS (Manufacture Command Set Control)								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
CMD Page Switch	W	1	1	1	1	1	1	1	0	FEh
Parameter 1		CMD_Page_Selection[3:0]				-	-	-	-	00h

NOTE: *"-"Don't care.*

Description

This command is used to switch the Manufacture Command Pages and User Commands sets.

CMD_Page_Selection [3:0]	Value	Description
0000	00h	UCS CMD1 (default page after power-on)
0001	10h	MCS CMD2 Page0 Panel ID
0010	20h	MCS CMD2 Page0 extension
0011	30h	MCS CMD2 Page0 Gamma3
0100	40h	MCS CMD2 Page0
0101	50h	MCS CMD2 Page0 Gamma1
0110	60h	MCS CMD2 Page0 Gamma2
0111	70h	MCS CMD2 Page0 GOA timing in Normal mode
1000	80h	MCS CMD2 Page0 BC/ACL

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

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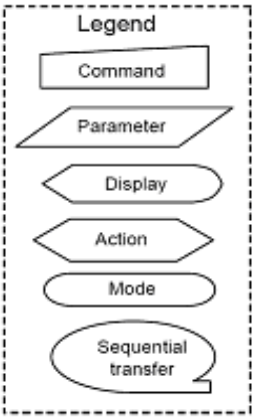
Flow Chart	

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7.5.65 CMD Page Switch (FFh)

Command set		MCS (Manufacture Command Set Control)								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
CMD Page Switch	R	1	1	1	1	1	1	1	1	FFh
Parameter 1		Current_CMD_Page[3:0]				-	-	-	-	00h

NOTE: *"-"Don't care.*

Description

This command is used to read the Manufacture Command Pages and User Commands sets.

Current_CMD_Page[3:0]	Value	Description
0000	00h	UCS CMD1 (default page after power-on)
0001	10h	MCS CMD2 Page0 Panel ID
0010	20h	MCS CMD2 Page0 extension
0011	30h	MCS CMD2 Page0 Gamma3
0100	40h	MCS CMD2 Page0
0101	50h	MCS CMD2 Page0 Gamma1
0110	60h	MCS CMD2 Page0 Gamma2
0111	70h	MCS CMD2 Page0 GOA timing in Normal mode
1000	80h	MCS CMD2 Page0 BC/ACL

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

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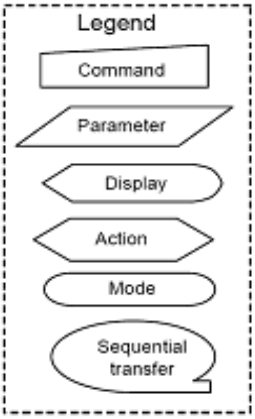
Flow Chart	

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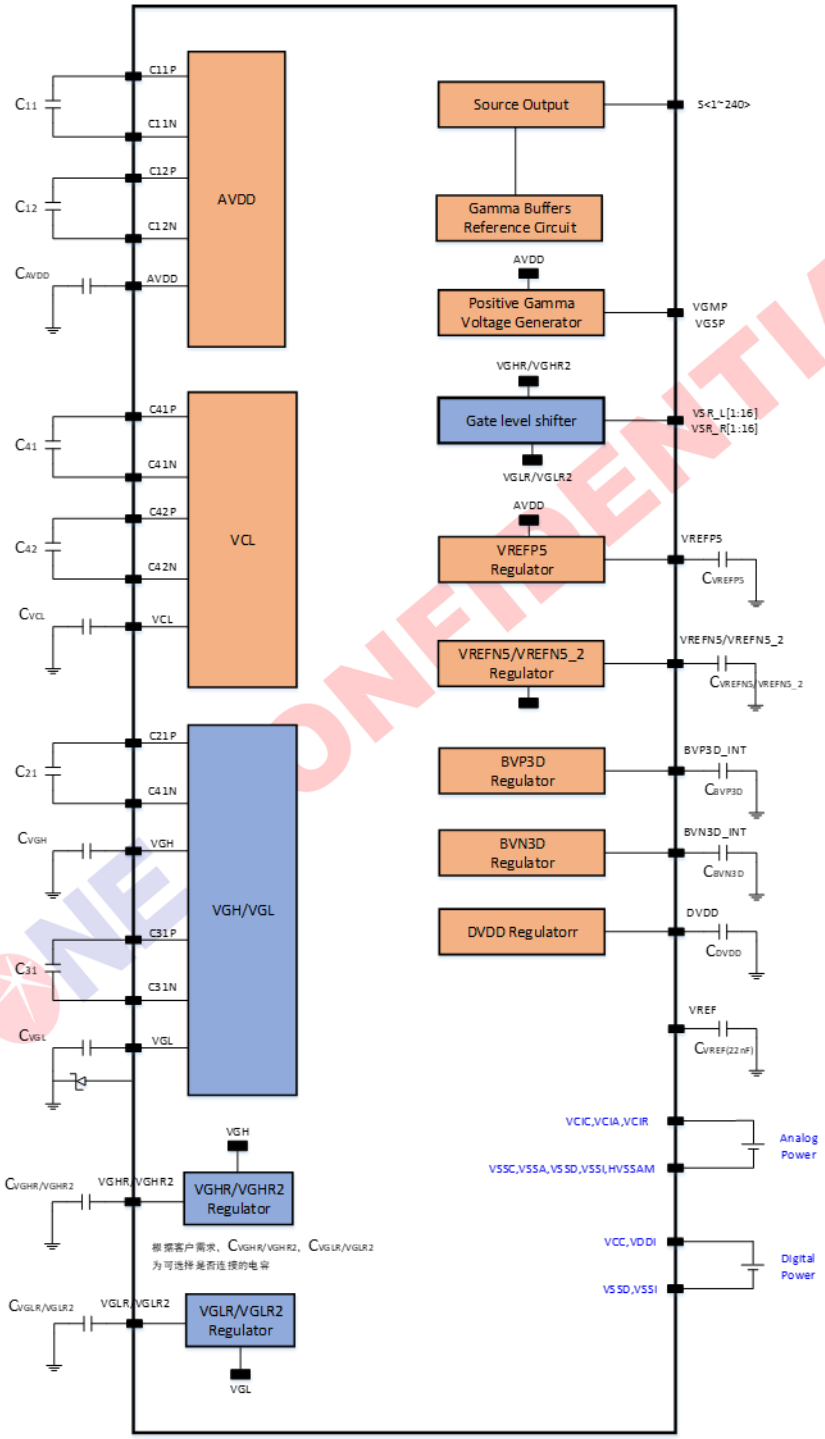
8. Application

8.1 DC/DC Converter Circuit



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8.2 EXTERNAL COMPONENTS CONNECTION

The Following components are necessary connected on the module to make sure the ICNA3312 can provided high performance and reliability.

Pad Name	Connection	Typical Value
VCI	Connect to Capacitor (Max 6.3V) : VCI -----||----- GND	2.2uF
VDDI	Connect to Capacitor (Max 6.3V) : VDDI -----||----- GND	2.2uF
VREF	Connect to Capacitor (Max 6.3V) : VREF -----||----- GND	22nF
VDD	Connect to Capacitor (Max 6.3V) : VDD -----||----- GND	1.0uF
VREFP	Connect to Capacitor (Max 10V) : VREFP -----||----- GND	1.0uF
VREFN5	Connect to Capacitor (Max 10V) : VREFN5 -----||----- GND	1.0uF
VREFN5_2	Connect to Capacitor (Max 10V) : VREFN5_2 -----||----- GND（非必须连接 cap，见下方 remark）	1.0uF
VGHR1	Connect to Capacitor (Max 16V) : VGHR1 -----||----- GND	2.2uF
VGHR2	Connect to Capacitor (Max 16V) : VGHR2 -----||----- GND（非必须连接 cap，见下方 remark）	2.2uF
VGLR1	Connect to Capacitor (Max 16V) : VGLR1 -----||----- GND	2.2uF
VGLR2	Connect to Capacitor (Max 16V) : VGLR2 -----||----- GND（非必须连接 cap，见下方 remark）	2.2uF
BVP3D	Connect to Capacitor (Max 10V) : ELVDD -----||----- GND	2.2uF
BVN3D	Connect to Capacitor (Max 10V) : ELVSS -----||----- GND	2.2uF
C11P/C11N	Connect to Capacitor (Max 6.3V) : C11P-----||----- C11N	1.0uF
C12P/C12N	Connect to Capacitor (Max 6.3V) : C12P-----||----- C12N	1.0uF
AVDD	Connect to Capacitor (Max 10V) : AVDD -----||-----GND	2.2uF
C41P/C41N	Connect to Capacitor (Max 6.3V) : C41P -----||----- C41N	1.0uF
C42P/C42N	Connect to Capacitor (Max 6.3V) : C42P -----||----- C42N	1.0uF
VCL	Connect to Capacitor (Max 10V) : VCL -----||----- GND	2.2uF
C21P/C21N	Connect to Capacitor (Max 16V) : C21P -----||----- C21N	1.0uF
VGH	Connect to Capacitor (Max 16V) : VGH -----||----- GND	2.2uF

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C31P/C31N	Connect to Capacitor (Max 16V) : C31P -----||----- C31N	1.0uF
VGL	Connect to Capacitor (Max 16V) : VGL -----||----- GND	2.2uF
VGL-GND	Connect to Schottky diode: VGL -----▶|-----GND	D4(RB520G-30)

Necessary External Components Connection Table

Remark: 根据客户需求，C_{VGHR2}，C_{VGLR2}，C_{VREFN5_2} 为可选择的是否需要连接的电容；如果没有 VGHR2，VGLR2，VREFN5_2 的需求，可以将 PAD 浮空，不连接电容 C_VGHR2、C_VGLR2、C_VREFN_5.

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