EXPERIMENT NO. 04

DATE OF PERFORMANCE: GRADE:

DATE OF ASSESSMENT: SIGNATURE OF LECTURER/ TTA:

AIM: Implementation Of Shift Microoperations and Arithmetic Logic Shift Unit.

THEORY:

Shift micro-operations are those micro-operations that are used for serial transfer of information. These are also used in conjunction with arithmetic micro-operation, logic micro-operation, and other data-processing operations.

There are three types of shifts micro-operations:

1. Logical :
It transfers the 0 zero through the serial input. We use the symbols shl for logical shift-left and shr for shift-right.
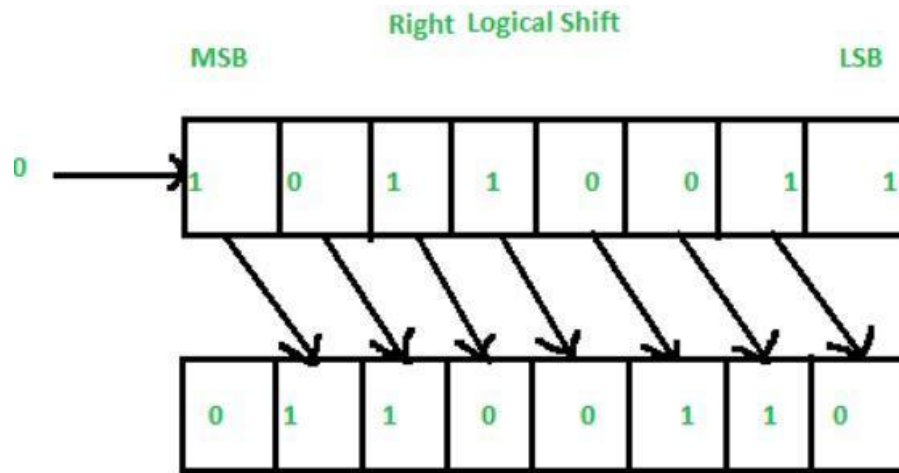
> 1. **Logical Shift Left –**
>   In this shift one position moves each bit to the left one by one. The Empty least significant bit (LSB) is filled with zero (i.e, the serial input), and the most significant bit (MSB) is rejected.
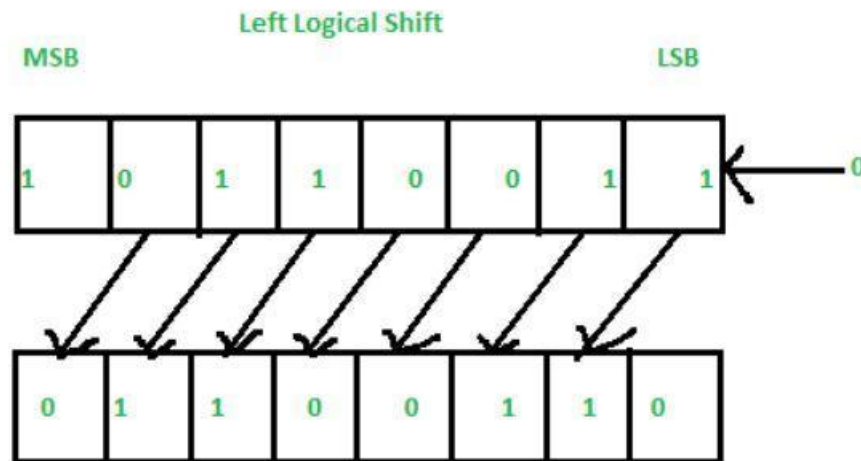
2. **Right Logical Shift-**
   In this one position moves each bit to the right one by one and the least
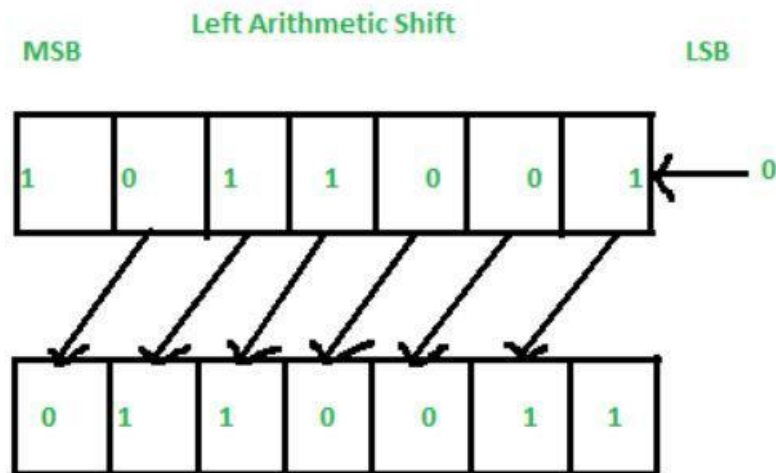   significant bit(LSB) is rejected and the empty MSB is filled with zero.

Right Logical Shift

MSB   LSB

0 → 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1

0 | 1 | 1 | 0 | 0 | 1 | 1 | 0

2. **Arithmetic :**
This micro-operation shifts a signed binary number to the left or to the right
position. In an arithmetic shift-left, it multiplies a signed binary number by 2 and In
an arithmetic shift-right, it divides the number by 2.

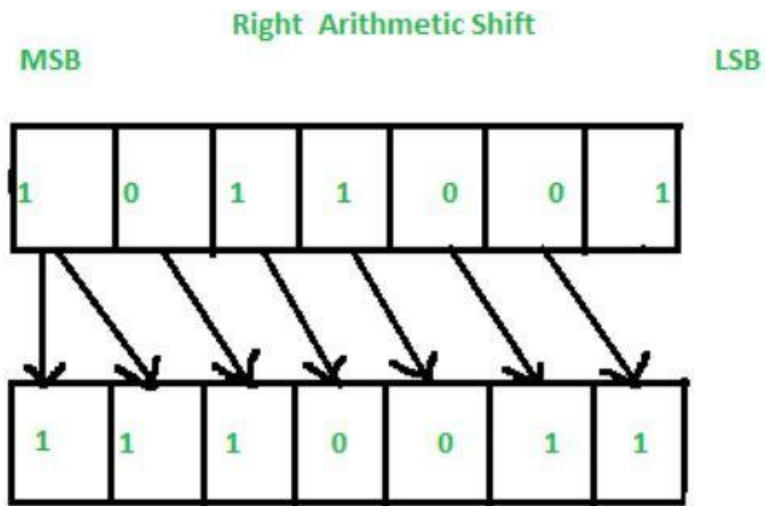1. **Left Arithmetic Shift –**
   In this one position moves each bit to the left one by one. The empty least
   significant bit (LSB) is filled with zero and the most significant bit (MSB) is
   rejected. Same as the Left Logical Shift.

Left Arithmetic Shift

MSB   LSB

1 | 0 | 1 | 1 | 0 | 0 | 1 ← 0

0 | 1 | 1 | 0 | 0 | 1 | 1

2. **Right Arithmetic Shift –**
   In this one position moves each bit to the right one by one and the least

significant bit is rejected and the empty MSB is filled with the value of the previous MSB.
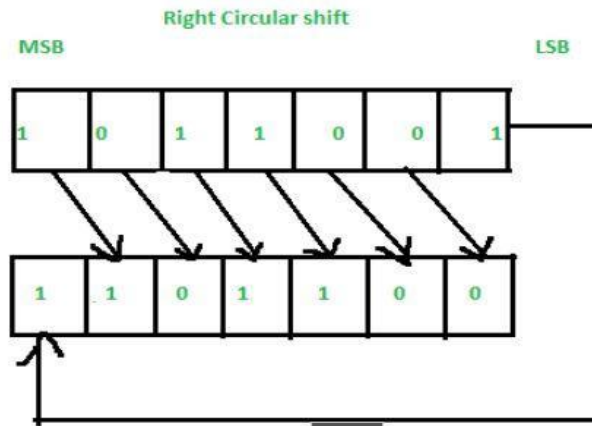
Right Arithmetic Shift

MSB   LSB

| 1 | 0 | 1 | 1 | 0 | 0 | 1 |

| 1 | 1 | 1 | 0 | 0 | 1 | 1 |

3. Circular :
The circular shift circulates the bits in the sequence of the register around the both ends without any loss of information.
   **1. Left Circular Shift –**

Left Circular shift

MSB   LSB

| 1 | 0 | 1 | 1 | 0 | 0 | 1 |

| 0 | 1 | 1 | 0 | 0 | 1 | 1 |

   2.Right Circular Shift –

Right Circular shift

MSB   LSB

| 1 | 0 | 1 | 1 | 0 | 0 | 1 |

| 1 | 1 | 0 | 1 | 1 | 0 | 0 |
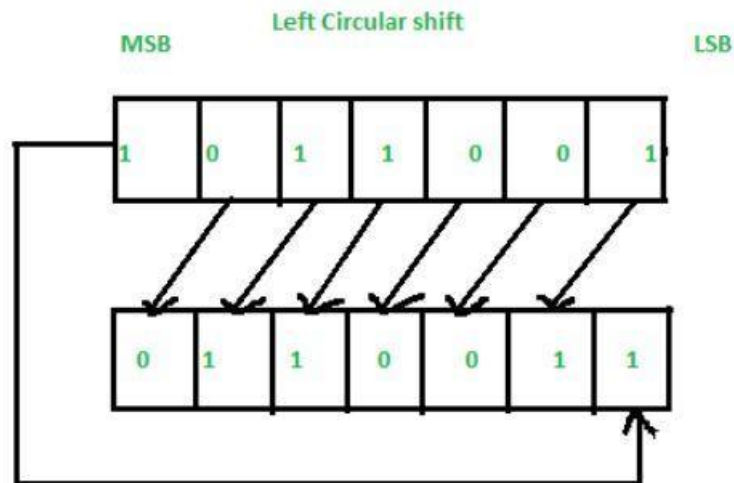
Arithmetic Logic Shift Unit (ALSU):

is a member of the Arithmetic Logic Unit (ALU) in a computer system. It is a digital circuit that performs logical, arithmetic, and shift operations. Rather than having individual registers calculating the micro operations directly, the computer deploys a number of storage registers which is connected to a common operational unit known as an arithmetic logic unit or ALU.

Now, to implement the micro operation, the contents of specified registers are allocated in the inputs of the common Arithmetic Logic Unit. The Arithmetic Logic Unit performs an operation that leads as a result and gets transferred to a destination register. Arithmetic Logic Unit may be a combinatory circuit in order that the complete register transfer operation from the supply registers through the ALU and into the destination register is performed throughout one clock pulse amount. Sometimes, the shift micro operations are performed in a separate unit, but sometimes it is made as a part of full ALU.
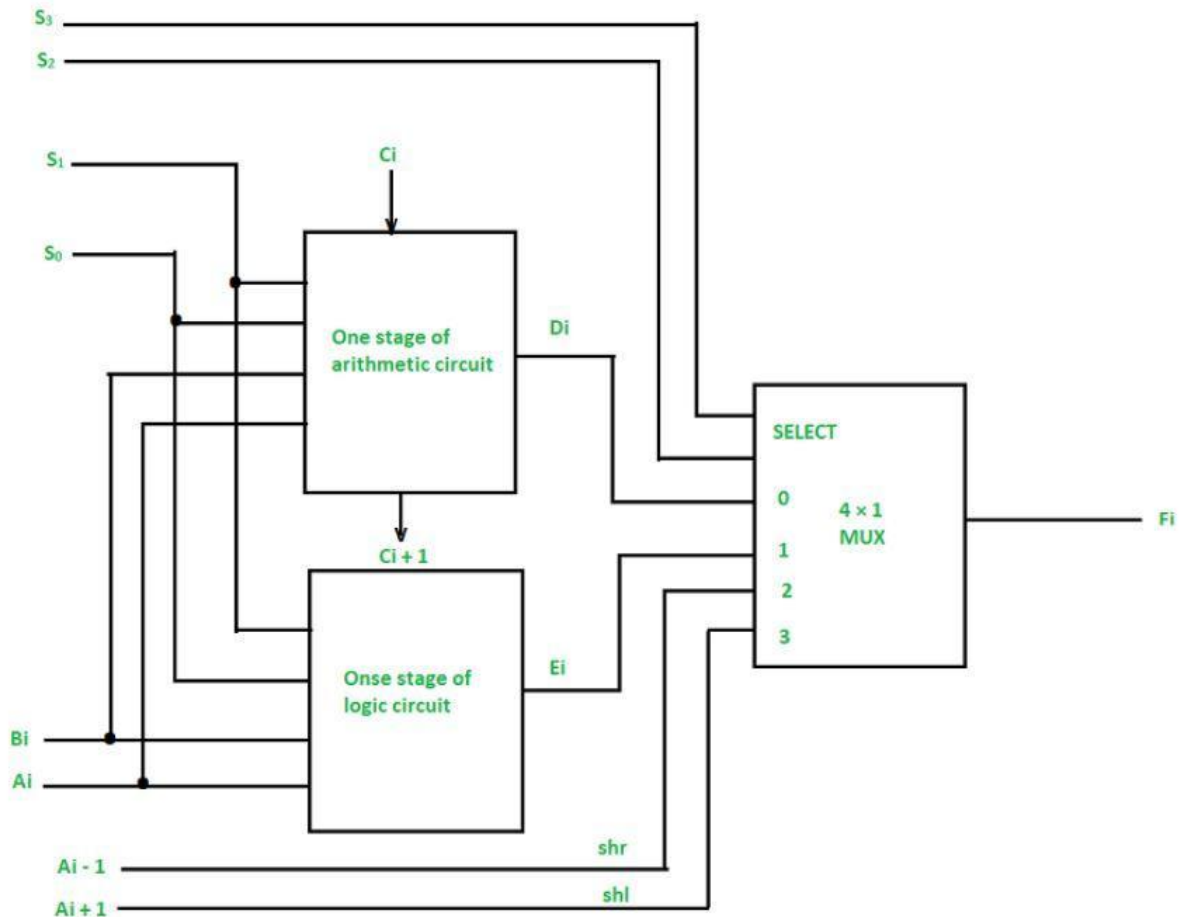
We can combine and make one ALU with common selection variables by adding arithmetic, logic, and shift circuits. We can see the, One stage of an arithmetic logic shift unit in the diagram below. Some particular micro operations are selected through the inputs S1 and S0.

4 x 1 multiplexer at the output chooses between associate arithmetic output between Ei and a logic output in Hi. The data in the multiplexer are selected through inputs S3 and S2 and the other two data inputs to the multiplexer obtain the inputs Ai – 1 for the *shr* operation and Ai + 1 for the *shl* operation.
Note: The output carry Ci + 1 of a specified arithmetic stage must be attached to the input carry Ci of the next stage in the sequence.
The circuit whose one stage is given in the below diagram provides 8 arithmetic operations, 4 logic operations, and 2 shift operations, and Each operation is selected by the 5 variables S3, S2, S1, S0, and Cin.

The below table shows the 14 operations perform by the Arithmetic Logic Unit:

1. The first 8 are arithmetic operations which are selected by S3 S2 = 00
2. The next 4 are logic operations which are selected by S3 S2 = 01
3. The last two are shift operations which are selected by S3 S2 = 10 & 11

Operation Select					Operation	Function
S_3	S_2	S_1	S_0	C_{in}		
0	0	0	0	0	F = A	Transfer A
0	0	0	0	1	F = A + 1	Increment A
0	0	0	1	0	F = A + B	Addition
0	0	0	1	1	F = A + B + 1	Add with carry
0	0	1	0	0	F = A + B'	Subtract with borrow
0	0	1	0	1	F = A + B' + 1	Subtraction
0	0	1	1	0	F = A - 1	Decrement A
0	0	1	1	1	F = A	Transfer A
0	1	0	0	×	F = A ^ B	AND
0	1	0	1	×	F = A v B	OR
0	1	1	0	×	F = A XOR B	XOR
0	1	1	1	×	F = A'	Complement A
1	0	×	×	×	F = shr A	Shift right A into F
1	1	×	×	×	F = shl A	Shift left A into F