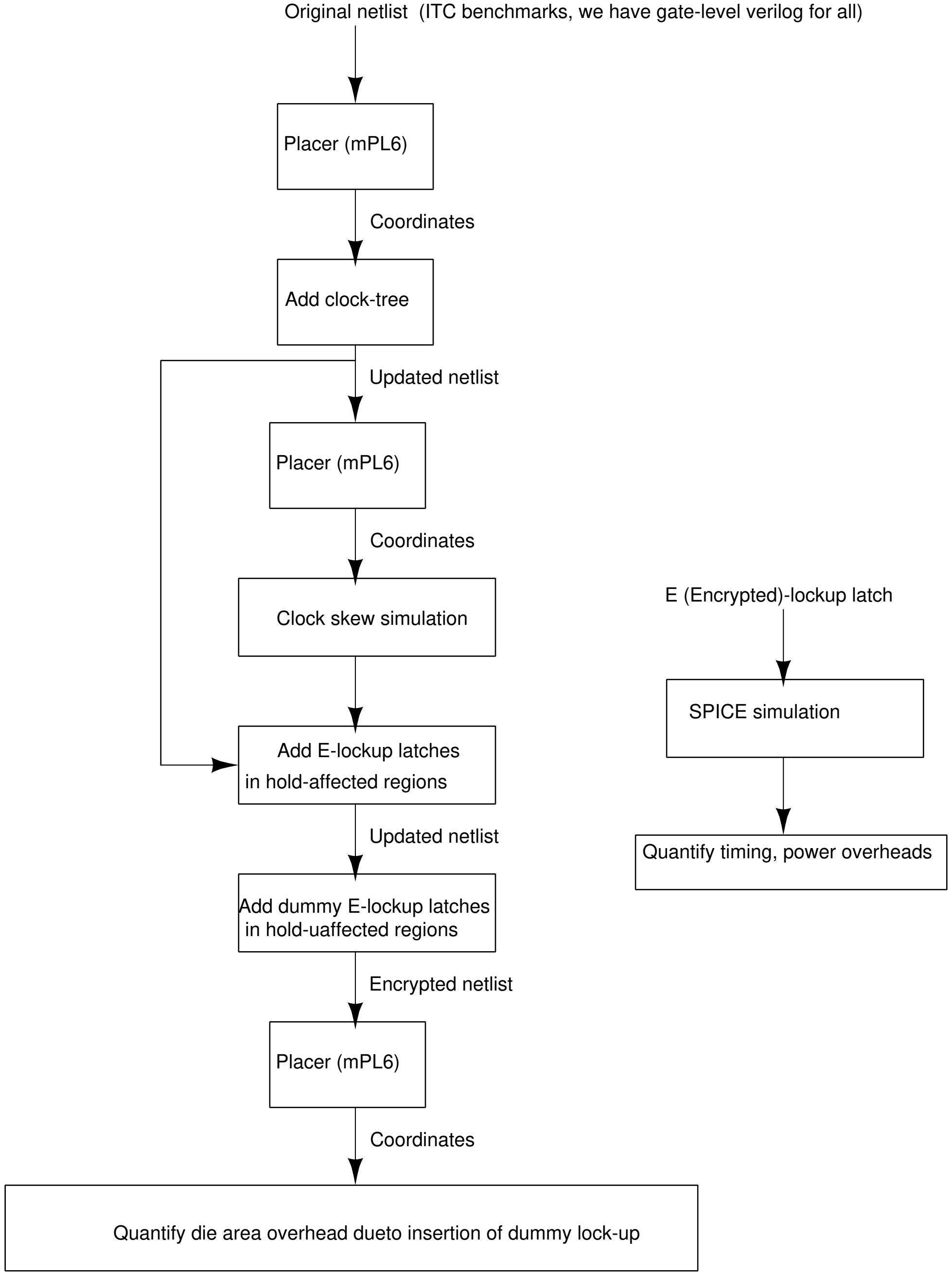
Original netlist (ITC benchmarks, we have gate-level verilog for all)
Placer (mPL6)
Coordinates
Add clock-tree
Updated netlist
Placer (mPL6)
Coordinates
Clock skew simulation
Add E-lockup latches
in hold-affected regions
Updated netlist
Add dummy E-lockup latches
in hold-uaffected regions
Encrypted netlist
Placer (mPL6)
Coordinates
Quantify die area overhead dueto insertion of dummy lock-up
E (Encrypted)-lockup latch
SPICE simulation
Quantify timing, power overheads