ρ-VEX core features (1/3)

- Focus on readability, maintainability and flexibility of the code
- Dynamic reconfiguration fixed, using hardware context switching
- Core code and interface is identical for static and dynamic designs
- Precise exceptions; trap model similar to ST200

ρ-VEX core features (2/3)

- Control regs are part of the core now and can exist per context
- Breakpoints and single step support built into the core
  - can be handled by the trap handler or by halting the core
- External debug interface can read and modify all registers even when core is running

ρ-VEX core features (3/3)

- Should be synthesized with ISE 14.7
  - ISE 13.4 synthesizes incorrectly for some reason
- Fully featured design has been synthesized at 37.5 MHz
- Much slower than the old core still, unfortunately
- Seems to be primarily due to routing delay

ρ-VEX support library (1/2)

- Compatible with grlib's library management
  - can be added to a grlib project makefile using EXTRALIBS instead of needing to add files manually
- Reconfigurable cache (as presented earlier)
  - made compatible with the new core
  - now generic-reconfigurable for heterogeneous designs

ρ-VEX support library (2/2)

- Simple bus system for use in standalone designs with bridge to and from AHB
- Two ready made system files for the core, one with on-chip memories and one with the cache and an AHB master and slave interface
- Debug UART peripheral

rvsrv/rvd debug toolchain (1/2)

- Connects to the debug UART peripheral, similar to grmon

- rvsrv (ρ-VEX server) runs in the background
  - bridges the serial port connection to two TCP servers, one for debug commands and one for stdin/stdout as seen by the application

- rvd (ρ-VEX debug) sends debug commands to rvsrv, designed to be easily scriptable

rvsrv/rvd debug toolchain (2/2)

- netcat can be used to connect to rvsrv to monitor stdout (puts, putchar) and write to stdin (getchar)

- There is no gdb support *yet*

Platforms (1/2)

- "Platforms" in this context refers to modelsim and/or ISE projects which implement the core somehow

- core-tests
  - Simulation-only platform which runs unit test suites on the core

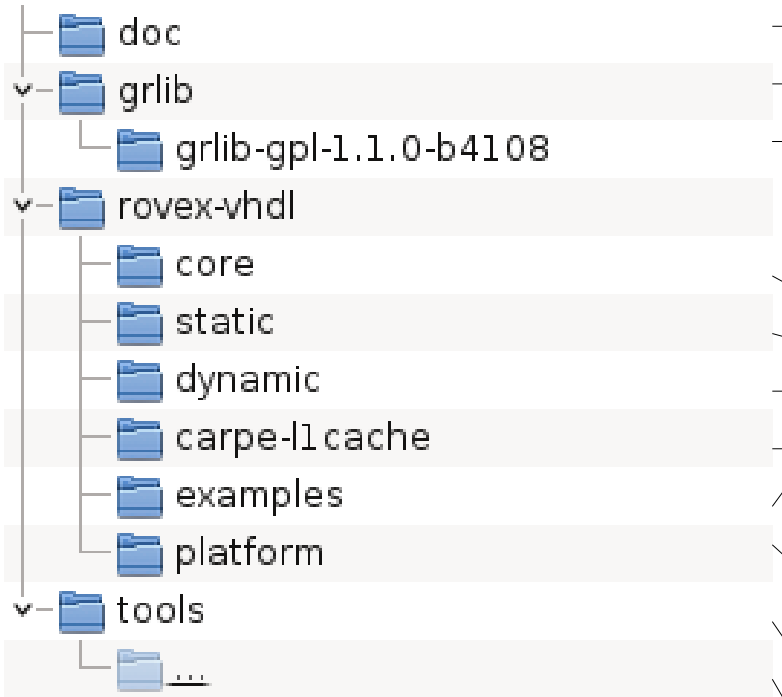
- cache-test
  - Simulation-only platform which tests the core and cache in a controlled environment with any compiled ρ-VEX application

Platforms (2/2)

- ml605-standalone
  - Standalone core design without grlib or cache using block RAMs as memory for the ML605 development board
- ml605-grlib (not functional yet)
  - ρ-VEX core(s) with cache added to the grlib ML605 LEON3 project, using the latest version of grlib
- zed-standalone (not functional yet)
  - Same as ml605-standalone, but for the zedboard

Repository structure

Old:



New: